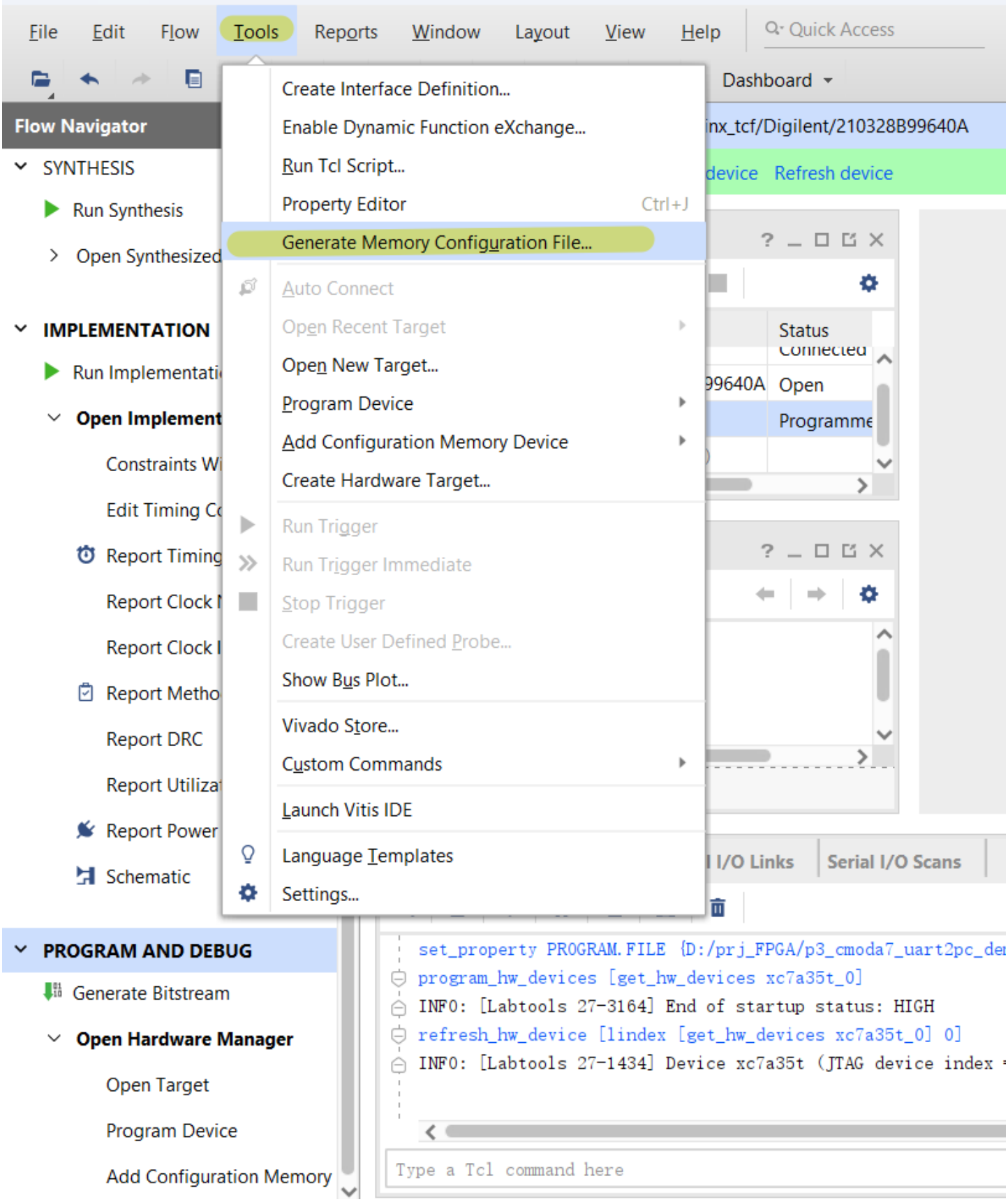
CMOD A7 Program Flash Tutorial

FPGAs do not inherently retain their configuration after power is removed. Flash memory provides non-volatile storage for the FPGA configuration bitstream. When the FPGA powers up, it loads its configuration from this flash memory, allowing it to "know" how to function according to the design it has been programmed with.

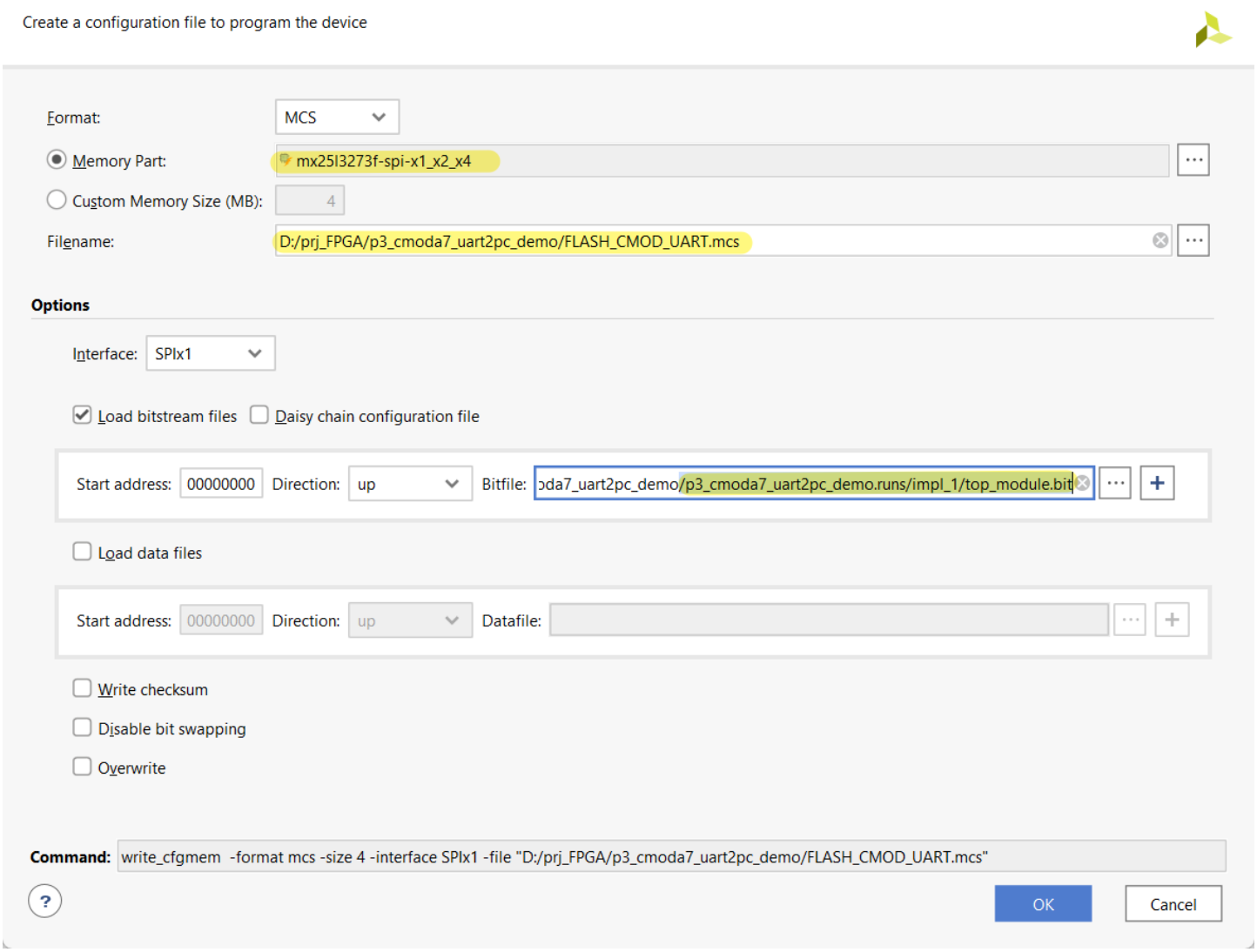
Recommended Steps

1. After generating the bitstream file, "Tools" -> "Generate Memory Configuration File"

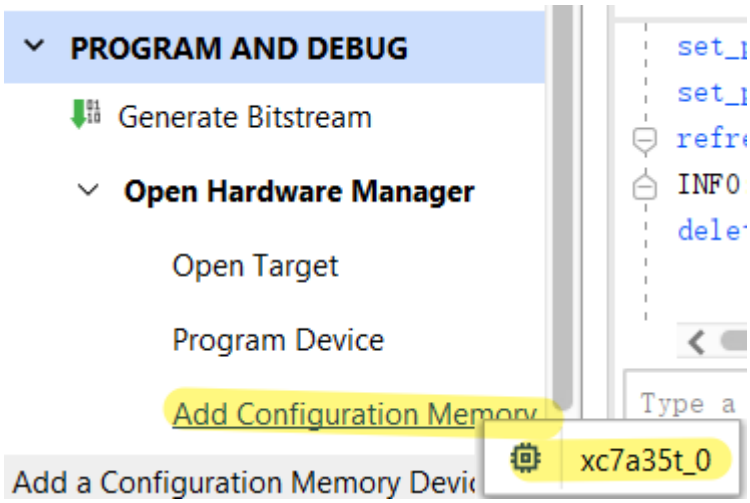


2. Config as following:
   a. Memory Part : mx25l3273f
   b. Filename: Create a file under your project folder;
   c. Enable "Load bitstream files";
   d. Select the BitFile from "<Project_Folder>/<Project_Name>.runs/impl_1/top_module.bit"

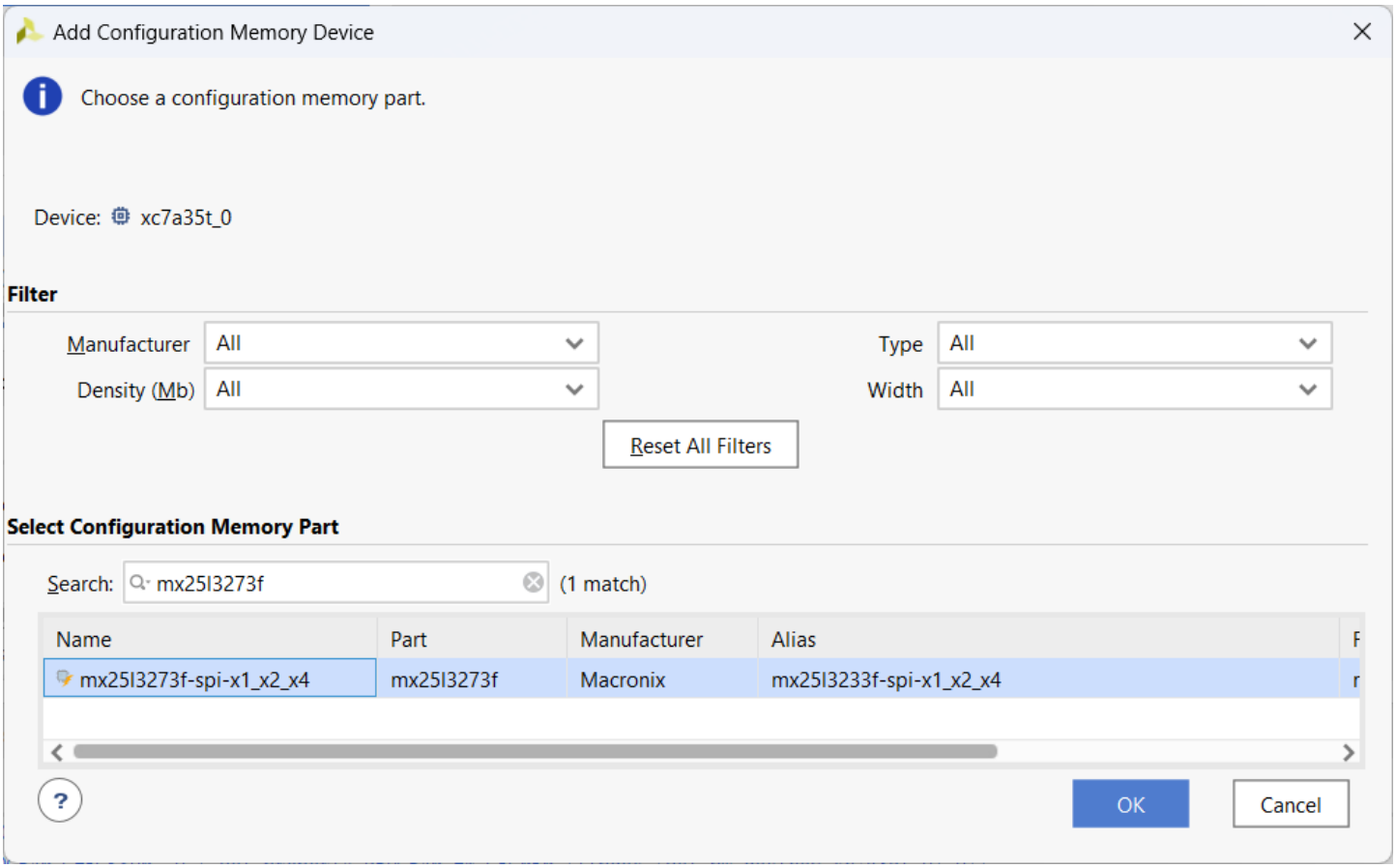
e. For Basys3 Board, Interface should be "SPIx4";



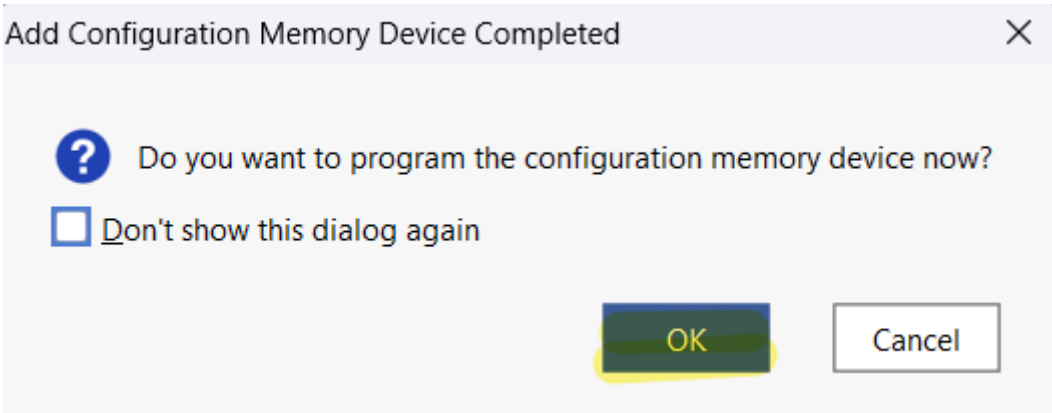
3. "Program and Debug" -> "Open Hardware Manager" -> "Add Configuration Memory"



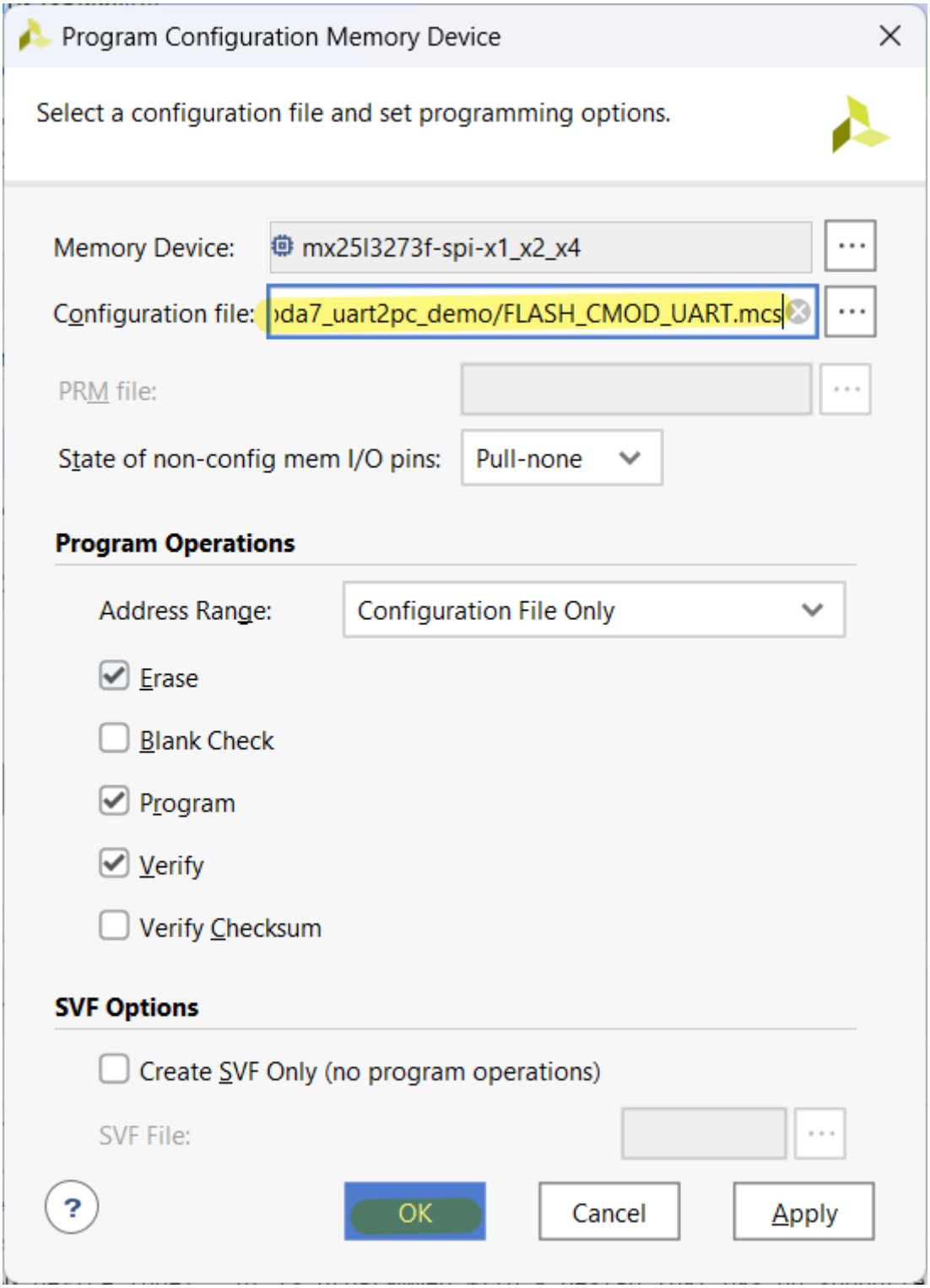
4. Search "mx25l3273f" -> select the part;



5. "OK"



6. Program Configuration Memory Deive
7. Select the MCS file which generates in Step2



8. Close the Vivado and reconnect the FPGA to your PC;
9. Check the "Done" LED;