**Intel® Speed Select Technology TPMI Interface**

**Introduction**

TPMI (Topology Aware Register and PM Capsule Interface), planned for future Intel® Xeon® processor generations, is an architectural, PCIe-standards based model, where feature support is provided cleanly as a driver and not as part of the base OS.

[TPMI](https://docs.intel.com/documents/pm_doc/src/server/GNR/Features/DVSEC%20MMIO/IC_tpmi.html) provides an enumerable and unified SW interface to support die disaggregation, hierarchical PM and improves product quality via an abstraction that minimizes software-hardware inter-dependences.

Software interfaces with TPMI could discover and control all aspects of Intel® Speed Select Technology (SST) including discovery and enumeration, select SST-PP level, enable/disable individual SST feature, setup CLOS priority and frequency limit, and assign core-CLOS mapping.

The legacy SST OS mailbox and PCU BAR based CLOS MMIO interfaces are being replaced with TPMI implementation in future Intel® Xeon® processors.

SST prioritization schemes (CP, TF, BF) are supported via CLOS interface. The legacy HWP interface will not be used for SST prioritization post-TPMI implementation.

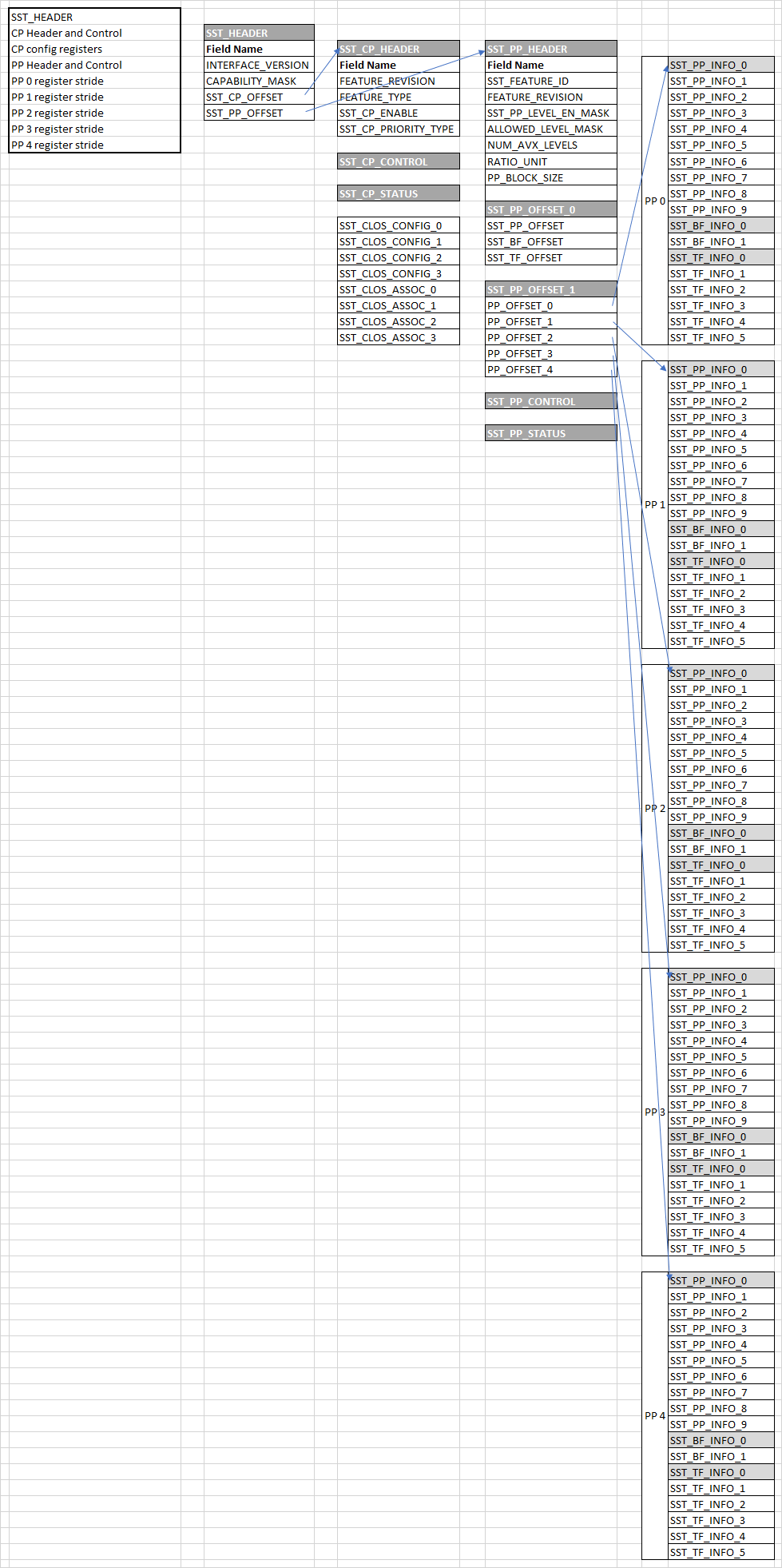
Note: The term "Software (SW)" throughout this document includes BIOS as one of the software entities.

**Register Structure**

SST registers are presented to SW in multi-layer structures as shown in the diagram below. This structure is extendable as need arises in the future. When this happens, a new value should be assigned to SST\_HEADER.INTERFACE\_VERSION and software is expected to interpret the structure accordingly to maintain backward compatibility.

The extendability includes things like changes in number of PP levels or AVX levels, PP/BF/TF/CP registers, adding or removing SST features, etc..

Note that the diagram below is for illustrative purpose only. It doesn't represent the actual register name/definition. This is provided in the “Register Spec” section of this document.

[](https://docs.intel.com/documents/pm_doc/src/server/Wave3_common/SST/embeddings/TPMI_SST_registers.xlsx)

**SST Register Hierarchy**

SST registers consist of a set of common registers and some per SST-PP level registers. Common registers are shared among all SST-PP config levels. Per SST-PP level registers are grouped together as "strides" and repeated for each config level.

The first SST register is SST\_HEADER. The first register of each stride is SST\_PP\_INF\_0. One SST-PP config level has one stride of registers.

The TPMI\_Offset of SST\_HEADER is 0x0. Other SST registers are SW enumerable based on SOC's feature capability. See the [section below](https://docs.intel.com/documents/pm_doc/src/server/Wave3_common/SST/IC_SST_TPMI.html#register-discovery-and-access) for SW enumeration mechanism.

**Register Spec**

**SST\_HEADER**

This register allows SW to discover SST capability and the offsets to CP and PP register banks.

SST feature set can be expanded over time, the INTERFACE\_VERSION field is used as an indication for feature evolution.

**SST Header (**[**source**](https://docs.intel.com/documents/pm_doc/src/server/Wave3_common/SST/embeddings/TPMI_SST_registers.xlsx)**)**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **SST\_HEADER** |  |  |  |  |  |
| **Field Name** | **Bits** | **Width** | **Access Type** | **Description** | **Default** |
| INTERFACE\_VERSION | 7:0 | 8 | RO | Version number for this interface | 0x1 |
| CAPABILITY\_MASK | 15:8 | 8 | RO | bitmask of the supported sub features. 1=the sub feature is enabled. 0=disabled.  Pcode populates the HW capability setting during early reset. SW uses this field to discover SST sub features.  Bit[8]= SST\_CP enable (1), disable (0)  bit[9]= SST\_PP enable (1), disable (0) | 0x2 |
| SST\_CP\_OFFSET | 23:16 | 8 | RO | *Qword (8 bytes) offset to the SST\_CP register bank* | 0x1 |
| SST\_PP\_OFFSET | 31:24 | 8 | RO | *Qword (8 bytes) offset to the SST\_PP register bank* | 0xC |
| RSVD | 63:32 | 32 | RO | *reserved offset for new features* | 0x0 |

**SST-CP Registers**

**SST-CP Registers (**[**source**](https://docs.intel.com/documents/pm_doc/src/server/Wave3_common/SST/embeddings/TPMI_SST_registers.xlsx)**)**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **SST\_CP\_HEADER** |  |  |  |  |  |
| **Field Name** | Bits | **Width** | **Access Type** | **Description** | **Default** |
| SST\_FEATURE\_ID | 3:0 | 4 | RO | Set to 0. (0=SST-CP, 1=SST-PP, 2=SST-BF, 3=SST-TF, 4-15 = reserved) | 0 |
| FEATURE\_REVISION | 11:4 | 8 | RO | Interface Version number for this SST feature | 1 |
| RATIO\_UNIT | 13:12 | 2 | RO | Frequency ratio unit. 00: 100MHz. All others : Reserved. Default=0. | 0 |
| RSVD | 63:14 | 50 | RO | Reserved | 0 |
|  |  |  |  |  |  |
| **SST\_CP\_CONTROL** |  |  |  |  |  |
| **Field Name** | Bits | **Width** | **Access Type** | **Description** | **Default** |
| SST\_CP\_ENABLE | 0:0 | 1 | RW | 1: Enable SST-CP. 0: Disable SST-CP | 0 |
| SST\_CP\_PRIORITY\_TYPE | 1:1 | 1 | RW | 0x0 (Default) =Proportional. 0x1=Ordered Throttling. | 0 |
| RSVD1 | 7:2 | 6 | RW | Reserved | 0 |
| RESET\_EXCURSION\_TO\_MIN | 11:8 | 4 | RW | Bitmask for the CLOS groups. SW clears SST\_CP\_STATUS.EXCURSION\_TO\_MIN bits by writing zero (0) to the respective RESET\_EXCURSIONS bit here. Pcode ignores the bit that SW writes 1 to.  Bit8=CLOS0, bit9=CLOS1, etc. | 0 |
| RSVD2 | 63:12 | 52 | RW | Reserved | 0 |
|  |  |  |  |  |  |
| **SST\_CP\_STATUS** |  |  |  |  |  |
| **Field Name** | Bits | **Width** | **Access Type** | **Description** | **Default** |
| SST\_CP\_ENABLE | 0:0 | 1 | RO | Returns 1 if SST-CP is enabled. | 0 |
| SST\_CP\_PRIORITY\_TYPE | 1:1 | 1 | RO | Returns current prioritization type. 0x0 (Default) =Proportional. 0x1=Ordered Throttling. | 0 |
| ERROR\_TYPE | 5:2 | 4 | RO | Returns the type of last error in this feature.  0x0: no error  0x1: SST-CP is not supported by the hardware.  all others: reserved. | 0 |
| RSVD1 | 7:6 | 2 | RO | Reserved | 0 |
| EXCURSION\_TO\_MIN | 11:8 | 4 | RO | Bitmask for the CLOS groups. If set (1), an excursion to Minimum Performance has occurred for the CLOS.  Bit8=CLOS0, bit9=CLOS1, etc. | 0 |
| RSVD2 | 63:12 | 52 | RO | Reserved | 0 |
|  |  |  |  |  |  |
| **SST\_CLOS\_CONFIG\_0** |  |  |  |  |  |
| **Field Name** | **Bits** | **Width** | **Access Type** | **Description** | **Default** |
| RSVD1 | 3:0 | 4 | RW | Reserved | 0 |
| PROPORTIONAL\_PRIORITY | 7:4 | 4 | RW | Used to set frequency weight when CLOS\_PRIORITY\_TYPE is set to Proportional.  (freq\_weight = 0xf -CLOS\_PROPORTIONAL\_PRIORITY)  0x0 = Max Perf (highest priority)  0xF = Min Perf (lowest priority) | 0 |
| MIN | 15:8 | 8 | RW | Hold the minimum PM CLOS frequency ratio (100MHz bins) for this CLOS group. | 0 |
| MAX | 23:16 | 8 | RW | Hold the maximum PM CLOS frequency ratio (100MHz bins) for this CLOS group. | 0xFF |
| RSVD2 | 63:24 | 40 | RW | Reserved | 0 |
|  |  |  |  |  |  |
| **SST\_CLOS\_CONFIG\_1** |  |  |  |  |  |
| **Field Name** | **Bits** | **Width** | **Access Type** | **Description** | **Default** |
| RSVD1 | 3:0 | 4 | RW | Reserved | 0 |
| PROPORTIONAL\_PRIORITY | 7:4 | 4 | RW | Used to set frequency weight when CLOS\_PRIORITY\_TYPE is set to Proportional.  (freq\_weight = 0xf -CLOS\_PROPORTIONAL\_PRIORITY)  0x0 = Max Perf (highest priority)  0xF = Min Perf (lowest priority) | 0 |
| MIN | 15:8 | 8 | RW | Hold the minimum PM CLOS frequency ratio (100MHz bins) for this CLOS group. | 0 |
| MAX | 23:16 | 8 | RW | Hold the maximum PM CLOS frequency ratio (100MHz bins) for this CLOS group. | 0xFF |
| RSVD2 | 63:24 | 40 | RW | Reserved | 0 |
|  |  |  |  |  |  |
| **SST\_CLOS\_CONFIG\_2** |  |  |  |  |  |
| **Field Name** | **Bits** | **Width** | **Access Type** | **Description** | **Default** |
| RSVD1 | 3:0 | 4 | RW | Reserved | 0 |
| PROPORTIONAL\_PRIORITY | 7:4 | 4 | RW | Used to set frequency weight when CLOS\_PRIORITY\_TYPE is set to Proportional.  (freq\_weight = 0xf -CLOS\_PROPORTIONAL\_PRIORITY)  0x0 = Max Perf (highest priority)  0xF = Min Perf (lowest priority) | 0 |
| MIN | 15:8 | 8 | RW | Hold the minimum PM CLOS frequency ratio (100MHz bins) for this CLOS group. | 0 |
| MAX | 23:16 | 8 | RW | Hold the maximum PM CLOS frequency ratio (100MHz bins) for this CLOS group. | 0xFF |
| RSVD2 | 63:24 | 40 | RW | Reserved | 0 |
|  |  |  |  |  |  |
| **SST\_CLOS\_CONFIG\_3** |  |  |  |  |  |
| **Field Name** | **Bits** | **Width** | **Access Type** | **Description** | **Default** |
| RSVD1 | 3:0 | 4 | RW | Reserved | 0 |
| PROPORTIONAL\_PRIORITY | 7:4 | 4 | RW | Used to set frequency weight when CLOS\_PRIORITY\_TYPE is set to Proportional.  (freq\_weight = 0xf -CLOS\_PROPORTIONAL\_PRIORITY)  0x0 = Max Perf (highest priority)  0xF = Min Perf (lowest priority) | 0 |
| MIN | 15:8 | 8 | RW | Hold the minimum PM CLOS frequency ratio (100MHz bins) for this CLOS group. | 0 |
| MAX | 23:16 | 8 | RW | Hold the maximum PM CLOS frequency ratio (100MHz bins) for this CLOS group. | 0xFF |
| RSVD2 | 63:24 | 40 | RW | Reserved | 0 |
|  |  |  |  |  |  |
| **SST\_CLOS\_ASSOC\_0** |  |  |  |  |  |
| **Field Name** | **Bits** | **Width** | **Access Type** | **Description** | **Default** |
| CLOS\_ID\_core0 | 3:0 | 4 | RW | CLOS\_ID for Core 0 | 0 |
| CLOS\_ID\_core1 | 7:4 | 4 | RW | CLOS\_ID for Core 1 | 0 |
| CLOS\_ID\_core2 | 11:8 | 4 | RW | CLOS\_ID for Core 2 | 0 |
| CLOS\_ID\_core3 | 15:12 | 4 | RW | CLOS\_ID for Core 3 | 0 |
| CLOS\_ID\_core4 | 19:16 | 4 | RW | CLOS\_ID for Core 4 | 0 |
| CLOS\_ID\_core5 | 23:20 | 4 | RW | CLOS\_ID for Core 5 | 0 |
| CLOS\_ID\_core6 | 27:24 | 4 | RW | CLOS\_ID for Core 6 | 0 |
| CLOS\_ID\_core7 | 31:28 | 4 | RW | CLOS\_ID for Core 7 | 0 |
| CLOS\_ID\_core8 | 35:32 | 4 | RW | CLOS\_ID for Core 8 | 0 |
| CLOS\_ID\_core9 | 39:36 | 4 | RW | CLOS\_ID for Core 9 | 0 |
| CLOS\_ID\_core10 | 43:40 | 4 | RW | CLOS\_ID for Core 10 | 0 |
| CLOS\_ID\_core11 | 47:44 | 4 | RW | CLOS\_ID for Core 11 | 0 |
| CLOS\_ID\_core12 | 51:48 | 4 | RW | CLOS\_ID for Core 12 | 0 |
| CLOS\_ID\_core13 | 55:52 | 4 | RW | CLOS\_ID for Core 13 | 0 |
| CLOS\_ID\_core14 | 59:56 | 4 | RW | CLOS\_ID for Core 14 | 0 |
| CLOS\_ID\_core15 | 63:60 | 4 | RW | CLOS\_ID for Core 15 | 0 |
|  |  |  |  |  |  |
| **SST\_CLOS\_ASSOC\_1** |  |  |  |  |  |
| **Field Name** | **Bits** | **Width** | **Access Type** | **Description** | **Default** |
| CLOS\_ID\_core16 | 3:0 | 4 | RW | CLOS\_ID for Core 16 | 0 |
| CLOS\_ID\_core17 | 7:4 | 4 | RW | CLOS\_ID for Core 17 | 0 |
| CLOS\_ID\_core18 | 11:8 | 4 | RW | CLOS\_ID for Core 18 | 0 |
| CLOS\_ID\_core19 | 15:12 | 4 | RW | CLOS\_ID for Core 19 | 0 |
| CLOS\_ID\_core20 | 19:16 | 4 | RW | CLOS\_ID for Core 20 | 0 |
| CLOS\_ID\_core21 | 23:20 | 4 | RW | CLOS\_ID for Core 21 | 0 |
| CLOS\_ID\_core22 | 27:24 | 4 | RW | CLOS\_ID for Core 22 | 0 |
| CLOS\_ID\_core23 | 31:28 | 4 | RW | CLOS\_ID for Core 23 | 0 |
| CLOS\_ID\_core24 | 35:32 | 4 | RW | CLOS\_ID for Core 24 | 0 |
| CLOS\_ID\_core25 | 39:36 | 4 | RW | CLOS\_ID for Core 25 | 0 |
| CLOS\_ID\_core26 | 43:40 | 4 | RW | CLOS\_ID for Core 26 | 0 |
| CLOS\_ID\_core27 | 47:44 | 4 | RW | CLOS\_ID for Core 27 | 0 |
| CLOS\_ID\_core28 | 51:48 | 4 | RW | CLOS\_ID for Core 28 | 0 |
| CLOS\_ID\_core29 | 55:52 | 4 | RW | CLOS\_ID for Core 29 | 0 |
| CLOS\_ID\_core30 | 59:56 | 4 | RW | CLOS\_ID for Core 30 | 0 |
| CLOS\_ID\_core31 | 63:60 | 4 | RW | CLOS\_ID for Core 31 | 0 |
|  |  |  |  |  |  |
| **SST\_CLOS\_ASSOC\_2** |  |  |  |  |  |
| **Field Name** | **Bits** | **Width** | **Access Type** | **Description** | **Default** |
| CLOS\_ID\_core32 | 3:0 | 4 | RW | CLOS\_ID for Core 32 | 0 |
| CLOS\_ID\_core33 | 7:4 | 4 | RW | CLOS\_ID for Core 33 | 0 |
| CLOS\_ID\_core34 | 11:8 | 4 | RW | CLOS\_ID for Core 34 | 0 |
| CLOS\_ID\_core35 | 15:12 | 4 | RW | CLOS\_ID for Core 35 | 0 |
| CLOS\_ID\_core36 | 19:16 | 4 | RW | CLOS\_ID for Core 36 | 0 |
| CLOS\_ID\_core37 | 23:20 | 4 | RW | CLOS\_ID for Core 37 | 0 |
| CLOS\_ID\_core38 | 27:24 | 4 | RW | CLOS\_ID for Core 38 | 0 |
| CLOS\_ID\_core39 | 31:28 | 4 | RW | CLOS\_ID for Core 39 | 0 |
| CLOS\_ID\_core40 | 35:32 | 4 | RW | CLOS\_ID for Core 40 | 0 |
| CLOS\_ID\_core41 | 39:36 | 4 | RW | CLOS\_ID for Core 41 | 0 |
| CLOS\_ID\_core42 | 43:40 | 4 | RW | CLOS\_ID for Core 42 | 0 |
| CLOS\_ID\_core43 | 47:44 | 4 | RW | CLOS\_ID for Core 43 | 0 |
| CLOS\_ID\_core44 | 51:48 | 4 | RW | CLOS\_ID for Core 44 | 0 |
| CLOS\_ID\_core45 | 55:52 | 4 | RW | CLOS\_ID for Core 45 | 0 |
| CLOS\_ID\_core46 | 59:56 | 4 | RW | CLOS\_ID for Core 46 | 0 |
| CLOS\_ID\_core47 | 63:60 | 4 | RW | CLOS\_ID for Core 47 | 0 |
|  |  |  |  |  |  |
| **SST\_CLOS\_ASSOC\_3** |  |  |  |  |  |
| **Field Name** | **Bits** | **Width** | **Access Type** | **Description** | **Default** |
| CLOS\_ID\_core48 | 3:0 | 4 | RW | CLOS\_ID for Core 48 | 0 |
| CLOS\_ID\_core49 | 7:4 | 4 | RW | CLOS\_ID for Core 49 | 0 |
| CLOS\_ID\_core50 | 11:8 | 4 | RW | CLOS\_ID for Core 50 | 0 |
| CLOS\_ID\_core51 | 15:12 | 4 | RW | CLOS\_ID for Core 51 | 0 |
| CLOS\_ID\_core52 | 19:16 | 4 | RW | CLOS\_ID for Core 52 | 0 |
| CLOS\_ID\_core53 | 23:20 | 4 | RW | CLOS\_ID for Core 53 | 0 |
| CLOS\_ID\_core54 | 27:24 | 4 | RW | CLOS\_ID for Core 54 | 0 |
| CLOS\_ID\_core55 | 31:28 | 4 | RW | CLOS\_ID for Core 55 | 0 |
| CLOS\_ID\_core56 | 35:32 | 4 | RW | CLOS\_ID for Core 56 | 0 |
| CLOS\_ID\_core57 | 39:36 | 4 | RW | CLOS\_ID for Core 57 | 0 |
| CLOS\_ID\_core58 | 43:40 | 4 | RW | CLOS\_ID for Core 58 | 0 |
| CLOS\_ID\_core59 | 47:44 | 4 | RW | CLOS\_ID for Core 59 | 0 |
| CLOS\_ID\_core60 | 51:48 | 4 | RW | CLOS\_ID for Core 60 | 0 |
| CLOS\_ID\_core61 | 55:52 | 4 | RW | CLOS\_ID for Core 61 | 0 |
| CLOS\_ID\_core62 | 59:56 | 4 | RW | CLOS\_ID for Core 62 | 0 |
| CLOS\_ID\_core63 | 63:60 | 4 | RW | CLOS\_ID for Core 63 | 0 |

**SST-PP Registers**

This register bank provides SW the interface to PP, BF and TF features.

**SST-PP Registers (**[**source**](https://docs.intel.com/documents/pm_doc/src/server/Wave3_common/SST/embeddings/TPMI_SST_registers.xlsx)**)**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **SST\_PP\_HEADER** |  |  |  |  |  |
| **Field Name** | **Bits** | **Width** | **Access Type** | **Description** | **Default** |
| SST\_FEATURE\_ID | 3:0 | 4 | RO | Set to 1. (0=SST-CP, 1=SST-PP, 2=SST-BF, 3=SST-TF, 4-15 = reserved) | 1 |
| FEATURE\_REVISION | 11:4 | 8 | RO | Interface Version number for this SST feature | 1 |
| SST\_PP\_LEVEL\_EN\_MASK | 19:12 | 8 | RO | SST-PP level enable/disable fuse mask.  SoftSKU can toggle fuse bit to enable/disable a specific level. | 0 |
| ALLOWED\_LEVEL\_MASK | 27:20 | 8 | RO | Allowed level mask used for dynamic config level switching.  Pcode programs the mask based on fuse and the current config. | 0 |
| RSVD1 | 31:28 | 4 | RO | Reserved | 0 |
| RATIO\_UNIT | 33:32 | 2 | RO | Core frequency ratio unit. 00: 100MHz. All others : Reserved. Default=0. | 0 |
| PP\_BLOCK\_SIZE | 41:34 | 8 | RO | Size of PP block (stride) in Qword unit (8 bytes) | 0x16 |
| DYNAMIC\_SWITCHING | 42:42 | 1 | RO | If set (1), dynamic switching of SST performance profiles is supported, else, not. | 0 |
| MEMORY\_RATIO\_UNIT | 44:43 | 2 | RO | Memory Controller frequency ratio unit. 00: 100MHz. All others : Reserved. Default=0. | 0 |
| RSVD2 | 63:45 | 19 | RO | Reserved | 0 |
|  |  |  |  |  |  |
| **SST\_PP\_OFFSET\_0** |  |  |  |  |  |
| **Field Name** | **Bits** | **Width** | **Access Type** | **Description** | **Default** |
| SST\_PP\_OFFSET | 7:0 | 8 | RO | Qword offset within PP level for the SST\_PP register bank | 0x0 |
| SST\_BF\_OFFSET | 15:8 | 8 | RO | Qword offset within PP level for the SST\_BF register bank | 0xC |
| SST\_TF\_OFFSET | 23:16 | 8 | RO | Qword offset within PP level for the SST\_TF register bank | 0xE |
| RSVD | 63:24 | 40 | RO | Reserved | 0 |
|  |  |  |  |  |  |
| **SST\_PP\_OFFSET\_1** |  |  |  |  |  |
| **Field Name** | **Bits** | **Width** | **Access Type** | **Description** | **Default** |
| PP\_OFFSET\_0 | 7:0 | 8 | RO | Qword offset to the register block (stride) of PP level 0 | 0x5 |
| PP\_OFFSET\_1 | 15:8 | 8 | RO | Qword offset to the register block (stride) of PP level 1 | 0x1B |
| PP\_OFFSET\_2 | 23:16 | 8 | RO | Qword offset to the register block (stride) of PP level 2 | 0x31 |
| PP\_OFFSET\_3 | 31:24 | 8 | RO | Qword offset to the register block (stride) of PP level 3 | 0x47 |
| PP\_OFFSET\_4 | 39:32 | 8 | RO | Qword offset to the register block (stride) of PP level 4 | 0x5D |
| RSVD | 63:40 | 24 | RO | Reserved | 0 |
|  |  |  |  |  |  |
| **SST\_PP\_CONTROL** |  |  |  |  |  |
| **Field Name** | **Bits** | **Width** | **Access Type** | **Description** | **Default** |
| SST\_PP\_LEVEL | 2:0 | 3 | RW | A SST-PP level that SW intends to switch to.  SW must program PP level setting to each SST instance per their instance-ID order. I.e. program instance 0 first, and follow by 1, 2, 3, etc. | 0 |
| SST\_PP\_LOCK | 3:3 | 1 | RW | SST-PP level select lock. 0 - unlocked. 1 - locked till next reset. | 0 |
| RSVD0 | 7:4 | 4 | RW | Reserved | 0 |
| FEATURE\_STATE | 15:8 | 8 | RW | Bit mask to control the enable(1)/disable(0) state of each feature of the current PP level  bit 0 = BF, bit 1 = TF, bit 2-7 = reserved. | 0 |
| RSVD1 | 63:16 | 48 | RW | Reserved | 0 |
|  |  |  |  |  |  |
| **SST\_PP\_STATUS** |  |  |  |  |  |
| **Field Name** | **Bits** | **Width** | **Access Type** | **Description** | **Default** |
| SST\_PP\_LEVEL | 2:0 | 3 | RO | Returns the current SST-PP level. | 0 |
| SST\_PP\_LOCK | 3:3 | 1 | RO | Returns the lock bit setting in SST\_PP\_CONTROL.SST\_PP\_LOCK | 0 |
| SST\_PP\_ERROR\_TYPE | 7:4 | 4 | RO | Returns last error of SST-PP control.  0x0: no error  0x1: dynamic PP switch is not allowed.  0x2..0xF: reserved. | 0 |
| FEATURE\_STATE | 15:8 | 8 | RO | Bit mask to indicate the enable(1)/disable(0) state of each feature of the current PP level  bit 0 = BF, bit 1 = TF, bit 2-7 = reserved. | 0 |
| RSVD0 | 31:16 | 16 | RO | Reserved | 0 |
| FEATURE\_ERROR\_TYPE | 55:32 | 24 | RO | Returns last error of the specific feature.  Three error\_type bits per feature. i.e. ERROR\_TYPE[2:0] for BF, ERROR\_TYPE[5:3] for TF, etc.  0x0: no error  0x1: The specific feature is not supported by the hardware.  0x2-0x6: Reserved  0x7: feature state change is not allowed. | 0 |
| RSVD1 | 63:56 | 8 | RO | Reserved | 0 |
|  |  |  |  |  |  |
| **SST\_PP\_INFO-0****[1](https://docs.intel.com/documents/pm_doc/src/server/Wave3_common/SST/IC_SST_TPMI.html" \l "__C1)** |  |  |  |  |  |
| **Field Name** | **Bits** | **Width** | **Access Type** | **Description** | **Default** |
| P1\_SSE | 7:0 | 8 | RO | Base frequency ratio of the TDP workload, a.k.a. SSE P1 | 0 |
| P1\_AVX2 | 15:8 | 8 | RO | P1 frequency ratio of the AVX2 representative workload | 0 |
| P1\_AVX512 | 23:16 | 8 | RO | P1 frequency ratio of the AVX512 representative workload | 0 |
| P1\_AMX | 31:24 | 8 | RO | P1 frequency ratio of the AMX representative workload | 0 |
| RSVD | 63:32 | 32 | RO | Reserved | 0 |
|  |  |  |  |  |  |
| **SST\_PP\_INFO-1** |  |  |  |  |  |
| **Field Name** | **Bits** | **Width** | **Access Type** | **Description** | **Default** |
| FUSED\_CORE\_COUNT | 7:0 | 8 | RO | Core Count of the fuse enabled cores. | 0 |
| RESOLVED\_CORE\_COUNT[2](https://docs.intel.com/documents/pm_doc/src/server/Wave3_common/SST/IC_SST_TPMI.html" \l "__C2) | 15:8 | 8 | RO | Core count of Pcode's resolved cores. | 0 |
| FUSED\_LLC\_COUNT | 23:16 | 8 | RO | LLC count of the fuse enabled LLC slices. | 0 |
| RSVD | 31:24 | 8 | RO | Reserved | 0 |
| TDP | 46:32 | 15 | RO | Power for this TDP level. In 1/8 W unit | 0 |
| T\_PROCHOT | 54:47 | 8 | RO | Provides the DTS max or external Prochot for the specific configuration | 0 |
| MAX\_MEMORY\_FREQ | 61:55 | 7 | RO | The max allowed memory controller frequency ratio for this config level. The ratio unit in defined in SST\_PP\_HEADER.memory\_ratio\_unit. | 0 |
| COOLING\_TYPE | 63:62 | 2 | RO | Cooling Type | 0 |
|  |  |  |  |  |  |
| **SST\_PP\_INFO-2** |  |  |  |  |  |
| **Field Name** | **Bits** | **Width** | **Access Type** | **Description** | **Default** |
| RESOLVED\_CORE\_MASK | 63:0 | 64 | RO | This is the logical core ID mask containing the functional (enabled in SKU) and non-defeatured (not in BIST failure or BIOS disables) cores. 1=enabled core, 0=disabled core. | 0 |
|  |  |  |  |  |  |
| **SST\_PP\_INFO-3** |  |  |  |  |  |
| **Field Name** | **Bits** | **Width** | **Access Type** | **Description** | **Default** |
| RSVD | 63:0 | 64 | RO | Reserved | 0 |
|  |  |  |  |  |  |
| **SST\_PP\_INFO-4** |  |  |  |  |  |
| **Field Name** | Bits | **Width** | **Access Type** | **Description** | **Default** |
| RATIO\_0 | 7:0 | 8 | RO | Turbo ratio limit level 0, bucket 0.  (Note: Ratio of 0x0 in the TRL registers implies that particular turbo limit level is not supported.) | 0 |
| RATIO\_1 | 15:8 | 8 | RO | Turbo ratio limit level 0, bucket 1 | 0 |
| RATIO\_2 | 23:16 | 8 | RO | Turbo ratio limit level 0, bucket 2 | 0 |
| RATIO\_3 | 31:24 | 8 | RO | Turbo ratio limit level 0, bucket 3 | 0 |
| RATIO\_4 | 39:32 | 8 | RO | Turbo ratio limit level 0, bucket 4 | 0 |
| RATIO\_5 | 47:40 | 8 | RO | Turbo ratio limit level 0, bucket 5 | 0 |
| RATIO\_6 | 55:48 | 8 | RO | Turbo ratio limit level 0, bucket 6 | 0 |
| RATIO\_7 | 63:56 | 8 | RO | Turbo ratio limit level 0, bucket 7 | 0 |
|  |  |  |  |  |  |
| **SST\_PP\_INFO-5** |  |  |  |  |  |
| **Field Name** | **Bits** | **Width** | **Access Type** | **Description** | **Default** |
| RATIO\_0 | 7:0 | 8 | RO | Turbo ratio limit level 1, bucket 0 | 0 |
| RATIO\_1 | 15:8 | 8 | RO | Turbo ratio limit level 1, bucket 1 | 0 |
| RATIO\_2 | 23:16 | 8 | RO | Turbo ratio limit level 1, bucket 2 | 0 |
| RATIO\_3 | 31:24 | 8 | RO | Turbo ratio limit level 1, bucket 3 | 0 |
| RATIO\_4 | 39:32 | 8 | RO | Turbo ratio limit level 1, bucket 4 | 0 |
| RATIO\_5 | 47:40 | 8 | RO | Turbo ratio limit level 1, bucket 5 | 0 |
| RATIO\_6 | 55:48 | 8 | RO | Turbo ratio limit level 1, bucket 6 | 0 |
| RATIO\_7 | 63:56 | 8 | RO | Turbo ratio limit level 1, bucket 7 | 0 |
|  |  |  |  |  |  |
| **SST\_PP\_INFO-6** |  |  |  |  |  |
| **Field Name** | **Bits** | **Width** | **Access Type** | **Description** | **Default** |
| RATIO\_0 | 7:0 | 8 | RO | Turbo ratio limit level 2, bucket 0 | 0 |
| RATIO\_1 | 15:8 | 8 | RO | Turbo ratio limit level 2, bucket 1 | 0 |
| RATIO\_2 | 23:16 | 8 | RO | Turbo ratio limit level 2, bucket 2 | 0 |
| RATIO\_3 | 31:24 | 8 | RO | Turbo ratio limit level 2, bucket 3 | 0 |
| RATIO\_4 | 39:32 | 8 | RO | Turbo ratio limit level 2, bucket 4 | 0 |
| RATIO\_5 | 47:40 | 8 | RO | Turbo ratio limit level 2, bucket 5 | 0 |
| RATIO\_6 | 55:48 | 8 | RO | Turbo ratio limit level 2, bucket 6 | 0 |
| RATIO\_7 | 63:56 | 8 | RO | Turbo ratio limit level 2, bucket 7 | 0 |
|  |  |  |  |  |  |
| **SST\_PP\_INFO-7** |  |  |  |  |  |
| **Field Name** | **Bits** | **Width** | **Access Type** | **Description** | **Default** |
| RATIO\_0 | 7:0 | 8 | RO | Turbo ratio limit level 3, bucket 0 | 0 |
| RATIO\_1 | 15:8 | 8 | RO | Turbo ratio limit level 3, bucket 1 | 0 |
| RATIO\_2 | 23:16 | 8 | RO | Turbo ratio limit level 3, bucket 2 | 0 |
| RATIO\_3 | 31:24 | 8 | RO | Turbo ratio limit level 3, bucket 3 | 0 |
| RATIO\_4 | 39:32 | 8 | RO | Turbo ratio limit level 3, bucket 4 | 0 |
| RATIO\_5 | 47:40 | 8 | RO | Turbo ratio limit level 3, bucket 5 | 0 |
| RATIO\_6 | 55:48 | 8 | RO | Turbo ratio limit level 3, bucket 6 | 0 |
| RATIO\_7 | 63:56 | 8 | RO | Turbo ratio limit level 3, bucket 7 | 0 |
|  |  |  |  |  |  |
| **SST\_PP\_INFO-8** |  |  |  |  |  |
| **Field Name** | **Bits** | **Width** | **Access Type** | **Description** | **Default** |
| RATIO\_0 | 7:0 | 8 | RO | Turbo ratio limit level 4, bucket 0 | 0 |
| RATIO\_1 | 15:8 | 8 | RO | Turbo ratio limit level 4, bucket 1 | 0 |
| RATIO\_2 | 23:16 | 8 | RO | Turbo ratio limit level 4, bucket 2 | 0 |
| RATIO\_3 | 31:24 | 8 | RO | Turbo ratio limit level 4, bucket 3 | 0 |
| RATIO\_4 | 39:32 | 8 | RO | Turbo ratio limit level 4, bucket 4 | 0 |
| RATIO\_5 | 47:40 | 8 | RO | Turbo ratio limit level 4, bucket 5 | 0 |
| RATIO\_6 | 55:48 | 8 | RO | Turbo ratio limit level 4, bucket 6 | 0 |
| RATIO\_7 | 63:56 | 8 | RO | Turbo ratio limit level 4, bucket 7 | 0 |
|  |  |  |  |  |  |
| **SST\_PP\_INFO-9** |  |  |  |  |  |
| **Field Name** | **Bits** | **Width** | **Access Type** | **Description** | **Default** |
| RATIO\_0 | 7:0 | 8 | RO | Turbo ratio limit level 5, bucket 0 | 0 |
| RATIO\_1 | 15:8 | 8 | RO | Turbo ratio limit level 5, bucket 1 | 0 |
| RATIO\_2 | 23:16 | 8 | RO | Turbo ratio limit level 5, bucket 2 | 0 |
| RATIO\_3 | 31:24 | 8 | RO | Turbo ratio limit level 5, bucket 3 | 0 |
| RATIO\_4 | 39:32 | 8 | RO | Turbo ratio limit level 5, bucket 4 | 0 |
| RATIO\_5 | 47:40 | 8 | RO | Turbo ratio limit level 5, bucket 5 | 0 |
| RATIO\_6 | 55:48 | 8 | RO | Turbo ratio limit level 5, bucket 6 | 0 |
| RATIO\_7 | 63:56 | 8 | RO | Turbo ratio limit level 5, bucket 7 | 0 |
|  |  |  |  |  |  |
| **SST\_PP\_INFO-10** |  |  |  |  |  |
| **Field Name** | **Bits** | **Width** | **Access Type** | **Description** | **Default** |
| NUM\_CORE\_0 | 7:0 | 8 | RO | TRL num\_core defines the active core ranges for TRL bucket 0 | 0 |
| NUM\_CORE\_1 | 15:8 | 8 | RO | TRL num\_core defines the active core ranges for TRL bucket 1 | 0 |
| NUM\_CORE\_2 | 23:16 | 8 | RO | TRL num\_core defines the active core ranges for TRL bucket 2 | 0 |
| NUM\_CORE\_3 | 31:24 | 8 | RO | TRL num\_core defines the active core ranges for TRL bucket 3 | 0 |
| NUM\_CORE\_4 | 39:32 | 8 | RO | TRL num\_core defines the active core ranges for TRL bucket 4 | 0 |
| NUM\_CORE\_5 | 47:40 | 8 | RO | TRL num\_core defines the active core ranges for TRL bucket 5 | 0 |
| NUM\_CORE\_6 | 55:48 | 8 | RO | TRL num\_core defines the active core ranges for TRL bucket 6 | 0 |
| NUM\_CORE\_7 | 63:56 | 8 | RO | TRL num\_core defines the active core ranges for TRL bucket 7 | 0 |
|  |  |  |  |  |  |
| **SST\_PP\_INFO-11** |  |  |  |  |  |
| **Field Name** | **Bits** | **Width** | **Access Type** | **Description** | **Default** |
| P0\_CORE\_RATIO[3](https://docs.intel.com/documents/pm_doc/src/server/Wave3_common/SST/IC_SST_TPMI.html" \l "__C3) | 7:0 | 8 | RO | Core maximum frequency ratio limit. | 0 |
| P1\_CORE\_RATIO | 15:8 | 8 | RO | Core TDP frequency ratio. | 0 |
| PN\_CORE\_RATIO | 23:16 | 8 | RO | Core maximum efficiency frequency ratio. | 0 |
| PM\_CORE\_RATIO | 31:24 | 8 | RO | Core minimum frequency ratio. | 0 |
| P0\_FABRIC\_RATIO | 39:32 | 8 | RO | Fabric (Uncore) maximum frequency ratio limit. | 0 |
| P1\_FABRIC\_RATIO | 47:40 | 8 | RO | Fabric (Uncore) TDP frequency ratio. | 0 |
| PM\_FABRIC\_RATIO | 55:48 | 8 | RO | Fabric (Uncore) minimum frequency ratio. | 0 |
| RESERVED | 63:56 | 8 | RO | Reserved | 0 |

|  |  |
| --- | --- |
|  |  |
|  |  |
|  |  |

**SST-BF Registers**

**SST-BF Registers (**[**source**](https://docs.intel.com/documents/pm_doc/src/server/Wave3_common/SST/embeddings/TPMI_SST_registers.xlsx)**)**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **SST\_BF\_INFO-0** |  |  |  |  |  |
| **Field Name** | Bits | **Width** | **Access Type** | **Description** | **Default** |
| SST\_FEATURE\_ID | 3:0 | 4 | RO | Set to 2. (0=SST-CP, 1=SST-PP, 2=SST-BF, 3=SST-TF, 4-15 = reserved) | 2 |
| FEATURE\_REVISION | 11:4 | 8 | RO | Interface Version number for this SST feature | 1 |
| FEATURE\_SUPPORTED | 12:12 | 1 | RO | 1: This SST feature is supported in this PP level. 0: This SST feature is not supported | 0 |
| P1\_HI | 20:13 | 8 | RO | base frequency for high priority cores | 0 |
| P1\_LO | 28:21 | 8 | RO | base frequency for low priority cores | 0 |
| RSVD0 | 31:29 | 3 | RO | Reserved | 0 |
| T\_CONTROL | 37:32 | 6 | RO | Fan Temperature Target Offset | 0 |
| T\_PROHOT | 45:38 | 8 | RO | Provides the DTS max or external Prochot for the specific configuration. | 0 |
| TDP | 60:46 | 15 | RO | TDP = SKU TDP - SST\_BF\_CONFIG\_n\_TDP\_OFFSET.  Pcode returns the resolved TDP in this configuration. In 1/8 W units. | 0 |
| RSVD1 | 63:61 | 3 | RO | Reserved | 0 |
|  |  |  |  |  |  |
| **SST\_BF\_INFO-1** |  |  |  |  |  |
| **Field Name** | Bits | **Width** | **Access Type** | **Description** | **Default** |
| P1\_HI\_CORE\_MASK | 63:0 | 64 | RO | Value of PBF\_P1\_HI\_CORE\_MASK for index provided as input. This is a logical core ID mask.  Bitmask polarity: 1=high priority core, 0=low priority core | 0 |

**SST-TF Registers**

**SST-TF Registers (**[**source**](https://docs.intel.com/documents/pm_doc/src/server/Wave3_common/SST/embeddings/TPMI_SST_registers.xlsx)**)**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **SST\_TF\_INFO-0** |  |  |  |  |  |
| **Field Name** | Bits | **Width** | **Access Type** | **Description** | **Default** |
| SST\_FEATURE\_ID | 3:0 | 4 | RO | Set to 3. (0=SST-CP, 1=SST-PP, 2=SST-BF, 3=SST-TF, 4-15 = reserved) | 3 |
| FEATURE\_REVISION | 11:4 | 8 | RO | Interface Version number for this SST feature | 1 |
| FEATURE\_SUPPORTED | 12:12 | 1 | RO | 1: This SST feature is supported in this PP level. 0: This SST feature is not supported | 0 |
| RSVD1 | 15:13 | 3 | RO | Reserved | 0 |
| LP\_CLIP\_RATIO\_0 | 23:16 | 8 | RO | Low priority cores frequency clipping ratio level 0 | 0 |
| LP\_CLIP\_RATIO\_1 | 31:24 | 8 | RO | Low priority cores frequency clipping ratio level 1 | 0 |
| LP\_CLIP\_RATIO\_2 | 39:32 | 8 | RO | Low priority cores frequency clipping ratio level 2 | 0 |
| LP\_CLIP\_RATIO\_3 | 47:40 | 8 | RO | Low priority cores frequency clipping ratio level 3 | 0 |
| LP\_CLIP\_RATIO\_4 | 55:48 | 8 | RO | Low priority cores frequency clipping ratio level 4 | 0 |
| LP\_CLIP\_RATIO\_5 | 63:56 | 8 | RO | Low priority cores frequency clipping ratio level 5 | 0 |
|  |  |  |  |  |  |
| **SST\_TF\_INFO-1** |  |  |  |  |  |
| **Field Name** | Bits | **Width** | **Access Type** | **Description** | **Default** |
| NUM\_CORE\_0 | 7:0 | 8 | RO | High Priority core count for bucket 0 | 0 |
| NUM\_CORE\_1 | 15:8 | 8 | RO | High Priority core count for bucket 1 | 0 |
| NUM\_CORE\_2 | 23:16 | 8 | RO | High Priority core count for bucket 2 | 0 |
| NUM\_CORE\_3 | 31:24 | 8 | RO | High Priority core count for bucket 3 | 0 |
| NUM\_CORE\_4 | 39:32 | 8 | RO | High Priority core count for bucket 4 | 0 |
| NUM\_CORE\_5 | 47:40 | 8 | RO | High Priority core count for bucket 5 | 0 |
| NUM\_CORE\_6 | 55:48 | 8 | RO | High Priority core count for bucket 6 | 0 |
| NUM\_CORE\_7 | 63:56 | 8 | RO | High Priority core count for bucket 7 | 0 |
|  |  |  |  |  |  |
| **SST\_TF\_INFO-2** |  |  |  |  |  |
| **Field Name** | Bits | **Width** | **Access Type** | **Description** | **Default** |
| RATIO\_0 | 7:0 | 8 | RO | SST-TF turbo ratio limit level 0, bucket 0 | 0 |
| RATIO\_1 | 15:8 | 8 | RO | SST-TF turbo ratio limit level 0, bucket 1 | 0 |
| RATIO\_2 | 23:16 | 8 | RO | SST-TF turbo ratio limit level 0, bucket 2 | 0 |
| RATIO\_3 | 31:24 | 8 | RO | SST-TF turbo ratio limit level 0, bucket 3 | 0 |
| RATIO\_4 | 39:32 | 8 | RO | SST-TF turbo ratio limit level 0, bucket 4 | 0 |
| RATIO\_5 | 47:40 | 8 | RO | SST-TF turbo ratio limit level 0, bucket 5 | 0 |
| RATIO\_6 | 55:48 | 8 | RO | SST-TF turbo ratio limit level 0, bucket 6 | 0 |
| RATIO\_7 | 63:56 | 8 | RO | SST-TF turbo ratio limit level 0, bucket 7 | 0 |
|  |  |  |  |  |  |
| **SST\_TF\_INFO-3** |  |  |  |  |  |
| **Field Name** | Bits | **Width** | **Access Type** | **Description** | **Default** |
| RATIO\_0 | 7:0 | 8 | RO | SST-TF turbo ratio limit level 1, bucket 0 | 0 |
| RATIO\_1 | 15:8 | 8 | RO | SST-TF turbo ratio limit level 1, bucket 1 | 0 |
| RATIO\_2 | 23:16 | 8 | RO | SST-TF turbo ratio limit level 1, bucket 2 | 0 |
| RATIO\_3 | 31:24 | 8 | RO | SST-TF turbo ratio limit level 1, bucket 3 | 0 |
| RATIO\_4 | 39:32 | 8 | RO | SST-TF turbo ratio limit level 1, bucket 4 | 0 |
| RATIO\_5 | 47:40 | 8 | RO | SST-TF turbo ratio limit level 1, bucket 5 | 0 |
| RATIO\_6 | 55:48 | 8 | RO | SST-TF turbo ratio limit level 1, bucket 6 | 0 |
| RATIO\_7 | 63:56 | 8 | RO | SST-TF turbo ratio limit level 1, bucket 7 | 0 |
|  |  |  |  |  |  |
| **SST\_TF\_INFO-4** |  |  |  |  |  |
| **Field Name** | Bits | **Width** | **Access Type** | **Description** | **Default** |
| RATIO\_0 | 7:0 | 8 | RO | SST-TF turbo ratio limit level 2, bucket 0 | 0 |
| RATIO\_1 | 15:8 | 8 | RO | SST-TF turbo ratio limit level 2, bucket 1 | 0 |
| RATIO\_2 | 23:16 | 8 | RO | SST-TF turbo ratio limit level 2, bucket 2 | 0 |
| RATIO\_3 | 31:24 | 8 | RO | SST-TF turbo ratio limit level 2, bucket 3 | 0 |
| RATIO\_4 | 39:32 | 8 | RO | SST-TF turbo ratio limit level 2, bucket 4 | 0 |
| RATIO\_5 | 47:40 | 8 | RO | SST-TF turbo ratio limit level 2, bucket 5 | 0 |
| RATIO\_6 | 55:48 | 8 | RO | SST-TF turbo ratio limit level 2, bucket 6 | 0 |
| RATIO\_7 | 63:56 | 8 | RO | SST-TF turbo ratio limit level 2, bucket 7 | 0 |
|  |  |  |  |  |  |
| **SST\_TF\_INFO-5** |  |  |  |  |  |
| **Field Name** | Bits | **Width** | **Access Type** | **Description** | **Default** |
| RATIO\_0 | 7:0 | 8 | RO | SST-TF turbo ratio limit level 3, bucket 0 | 0 |
| RATIO\_1 | 15:8 | 8 | RO | SST-TF turbo ratio limit level 3, bucket 1 | 0 |
| RATIO\_2 | 23:16 | 8 | RO | SST-TF turbo ratio limit level 3, bucket 2 | 0 |
| RATIO\_3 | 31:24 | 8 | RO | SST-TF turbo ratio limit level 3, bucket 3 | 0 |
| RATIO\_4 | 39:32 | 8 | RO | SST-TF turbo ratio limit level 3, bucket 4 | 0 |
| RATIO\_5 | 47:40 | 8 | RO | SST-TF turbo ratio limit level 3, bucket 5 | 0 |
| RATIO\_6 | 55:48 | 8 | RO | SST-TF turbo ratio limit level 3, bucket 6 | 0 |
| RATIO\_7 | 63:56 | 8 | RO | SST-TF turbo ratio limit level 3, bucket 7 | 0 |
|  |  |  |  |  |  |
| **SST\_TF\_INFO-6** |  |  |  |  |  |
| **Field Name** | Bits | **Width** | **Access Type** | **Description** | **Default** |
| RATIO\_0 | 7:0 | 8 | RO | SST-TF turbo ratio limit level 4, bucket 0 | 0 |
| RATIO\_1 | 15:8 | 8 | RO | SST-TF turbo ratio limit level 4, bucket 1 | 0 |
| RATIO\_2 | 23:16 | 8 | RO | SST-TF turbo ratio limit level 4, bucket 2 | 0 |
| RATIO\_3 | 31:24 | 8 | RO | SST-TF turbo ratio limit level 4, bucket 3 | 0 |
| RATIO\_4 | 39:32 | 8 | RO | SST-TF turbo ratio limit level 4, bucket 4 | 0 |
| RATIO\_5 | 47:40 | 8 | RO | SST-TF turbo ratio limit level 4, bucket 5 | 0 |
| RATIO\_6 | 55:48 | 8 | RO | SST-TF turbo ratio limit level 4, bucket 6 | 0 |
| RATIO\_7 | 63:56 | 8 | RO | SST-TF turbo ratio limit level 4, bucket 7 | 0 |
|  |  |  |  |  |  |
| **SST\_TF\_INFO-7** |  |  |  |  |  |
| **Field Name** | Bits | **Width** | **Access Type** | **Description** | **Default** |
| RATIO\_0 | 7:0 | 8 | RO | SST-TF turbo ratio limit level 5, bucket 0 | 0 |
| RATIO\_1 | 15:8 | 8 | RO | SST-TF turbo ratio limit level 5, bucket 1 | 0 |
| RATIO\_2 | 23:16 | 8 | RO | SST-TF turbo ratio limit level 5, bucket 2 | 0 |
| RATIO\_3 | 31:24 | 8 | RO | SST-TF turbo ratio limit level 5, bucket 3 | 0 |
| RATIO\_4 | 39:32 | 8 | RO | SST-TF turbo ratio limit level 5, bucket 4 | 0 |
| RATIO\_5 | 47:40 | 8 | RO | SST-TF turbo ratio limit level 5, bucket 5 | 0 |
| RATIO\_6 | 55:48 | 8 | RO | SST-TF turbo ratio limit level 5, bucket 6 | 0 |
| RATIO\_7 | 63:56 | 8 | RO | SST-TF turbo ratio limit level 5, bucket 7 | 0 |

**Register Discovery and Access**

SW responsibility includes (but not limited to) the following:

* Discover SST TPMI\_ID encoding (0x5) from the TPMI PFS structure and calculate SST's base MMIO address.
* Read SST\_HEADER and enumerate capability supported
* Calculate the offset to CP register banks. Enumerate CP header, control, and configuration registers
* Calculate the offset to PP register banks. Enumerate PP header, control, offsets, and register strides.
* Enumerate BF and TF registers within PP register bank.
* Handle SST as per-die scope feature.
* Enumerate the number of valid SST instances.
* Use {TPMI Register Name, TPMI ID, TPMI Offset} as documented in EDS/datasheet to construct MMIO address for register access.
* Write to all valid SST instances (lower numbered instance first, highest numbered instance last) and when performing SST\_PP config level switch and SST\_BF/SST\_TF state change.

**MMIO Address Calculation Details**

* Search for VSEC\_ID in extended PCIe config space
* Find VSEC\_ID=0x42 (TPMI Feature). Get the BARs of this BDF
* Calculate the MMIO Base Address for TPMI PM Features
  + BasePtr = BAR[tBIR] + Table\_Offset
* Search for SST TPMI\_ID in the PFS
* Calculate the MMIO Base Address of SST registers
  + BasePtr[SST] = BasePtr + Cap\_Offset[SST]
* Discover X, the number of SST instances
* valid = 1; p = 0;
* while (valid) {
* data= [BasePtr[SST] + p \* PFS.EntrySize\*4 + 0]; // read the first register of each instance
* valid = (data != -1); // All Fs indicates invalid data.
* p ++;
* }

X = p;

* Calc mmio\_addr of SST\_HEADER of instance k, where k = 0 .. X-1
  + mmio\_addr[k, SST\_HEADER] = BasePtr[SST] + k \* PFS.EntrySize \* 4 + SST\_HEADER.TPMI\_Offset
* Calc mmio\_addr of register in the CP register bank
  + BasePtr[SST] + k \* PFS.EntrySize \* 4 + SST\_HEADER.SST\_CP\_OFFSET \* 8 + (register).TPMI\_Offset
* Calc mmio\_addr of common register (non PP level specific) in the PP register bank
  + BasePtr[SST] + k \* PFS.EntrySize \* 4 + SST\_HEADER.SST\_PP\_OFFSET \* 8 + (register).TPMI\_Offset
* Calc mmio\_addr of PP[BF|TF] register in register stride S
  + BasePtr[SST] + k \* PFS.EntrySize \* 4 + SST\_HEADER.SST\_PP\_OFFSET \* 8 + SST\_PP\_OFFSET\_1.PP\_OFFSET\_[S] \* 8 + SST\_PP\_OFFSET\_0.SST\_PP[BF|TF]\_OFFSET \* 8 + (register).TPMI\_Offset

SW should look up register definition document (e.g. EDS, CPU datasheet, etc.) to determine the TPMI\_Offset of each register. An example is shown below.

**TPMI Offset (**[**source**](https://docs.intel.com/documents/pm_doc/src/server/Wave3_common/SST/embeddings/TPMI_SST_registers.xlsx)**)**

|  |  |  |  |
| --- | --- | --- | --- |
|  | **Name** | **TPMI ID** | **TPMI Offset** |
| All PP Level | SST\_HEADER | 5 | 0 |
| SST\_CP\_HEADER | 5 | 0 |
| SST\_CP\_CONTROL | 5 | 8 |
| SST\_CP\_STATUS | 5 | 16 |
| SST\_CLOS\_CONFIG\_0 | 5 | 24 |
| SST\_CLOS\_CONFIG\_1 | 5 | 32 |
| SST\_CLOS\_CONFIG\_2 | 5 | 40 |
| SST\_CLOS\_CONFIG\_3 | 5 | 48 |
| SST\_CLOS\_ASSOC\_0 | 5 | 56 |
| SST\_CLOS\_ASSOC\_1 | 5 | 64 |
| SST\_CLOS\_ASSOC\_2 | 5 | 72 |
| SST\_CLOS\_ASSOC\_3 | 5 | 80 |
| SST\_PP\_HEADER | 5 | 0 |
| SST\_PP\_OFFSET\_0 | 5 | 8 |
| SST\_PP\_OFFSET\_1 | 5 | 16 |
| SST\_PP\_CONTROL | 5 | 24 |
| SST\_PP\_STATUS | 5 | 32 |
| Per PP Level | SST\_PP\_INFO\_0 | 5 | 0 |
| SST\_PP\_INFO\_1 | 5 | 8 |
| SST\_PP\_INFO\_2 | 5 | 16 |
| SST\_PP\_INFO\_3 | 5 | 24 |
| SST\_PP\_INFO\_4 | 5 | 32 |
| SST\_PP\_INFO\_5 | 5 | 40 |
| SST\_PP\_INFO\_6 | 5 | 48 |
| SST\_PP\_INFO\_7 | 5 | 56 |
| SST\_PP\_INFO\_8 | 5 | 64 |
| SST\_PP\_INFO\_9 | 5 | 72 |
| SST\_PP\_INFO\_10 | 5 | 80 |
| SST\_PP\_INFO\_11 | 5 | 88 |
| SST\_BF\_INFO\_0 | 5 | 0 |
| SST\_BF\_INFO\_1 | 5 | 8 |
| SST\_TF\_INFO\_0 | 5 | 0 |
| SST\_TF\_INFO\_1 | 5 | 8 |
| SST\_TF\_INFO\_2 | 5 | 16 |
| SST\_TF\_INFO\_3 | 5 | 24 |
| SST\_TF\_INFO\_4 | 5 | 32 |
| SST\_TF\_INFO\_5 | 5 | 40 |
| SST\_TF\_INFO\_6 | 5 | 48 |
| SST\_TF\_INFO\_7 | 5 | 56 |
|  |  |  |  |
| Total Number of Registers | | 127 |  |
| PFS.EntrySize | | 254 |  |