Short Quiz on Timers

Due No due date **Points** 20 **Questions** 20
Available until Mar 8 at 3:30pm **Time Limit** 30 Minutes

Instructions

Choose the best answer from the choices.

This quiz was locked Mar 8 at 3:30pm.

Attempt History

	Attempt	Time	Score
LATEST	Attempt 1	30 minutes	15.75 out of 20

Correct answers are hidden.

Score for this quiz: **15.75** out of 20
Submitted Mar 8 at 3:23pm
This attempt took 30 minutes.

Question 1 — 1 / 1 pts

Match the registers to its correct description.

TMR1	Timer1 register
T1CON	Timer1 control regi
CCP1CON	CCP1 control regis

PR2	period register

Partial

Question 2 — 0.75 / 1 pts

Match the bits to its correct description.

TMR1IE	Timer1 interrupt er
TMR2IF	Timer2 interrupt fl
TMR1ON	Timer1 enable bit
TMR1CS	Timer1 oscillator c

clock Select

Question 3 — 1 / 1 pts

Match the registers to its correct description.

TMR2ON	Timer2 enable bit
PEIE	Peripheral interrup
TMR2IE	Timer2 interrupt e

GIE	Global interrupt er

Question 4 — 1 / 1 pts

If the duty cycle of the output signal generated by the CCP module is 60% at 1000Hz, what should be the value for the CCP1CON<5:4>? Assume F_{OSC} = 4MHz and Timer2 prescaler value of 1:16.

- (●) 10_2 (0.6/1000) (4*10^6)(1/16) = 150 = 100101 10
- ( ) 00_2
- ( ) 11_2
- ( ) 01_2

Incorrect

Question 5 — 0 / 1 pts

What is the event when the timer transitions from 0000h to FFFFh?

- ( ) Match
- (●) Interrupt
- ( ) Underflow
- ( ) Overflow

Question 6 — 1 / 1 pts

Which of the following timers does not generate an interrupt upon overflow?

- ( ) CCP Module
- ( ) Timer1
- (●) Timer2
- ( ) Timer0

Question 7 — 1 / 1 pts

What is a prescaler?

- ( ) A ration of the source clock to the instruction clock cycle.
- (●) A ratio of the source clock to the actual clock of the timer.
- ( ) None of the choices.
- ( ) A ratio between oscillator frequency to the actual clock of the timer.

Question 8 — 1 / 1 pts

If the duty cycle of the output signal generated by the CCP module is 60% at 1000Hz, what should be the value for the CCPR1L? Assume F_{OSC} = 4MHz and Timer2 prescaler value of 1:16.

- 00100101_2
- 00100101_2 (0.6/1000) (4*10^6)(1/16) = 150 = 00100101 10
- 10010110_2
- 00101100_2

Incorrect

Question 9 0 / 1 pts

When a capture event happens at RC2, which register the value of TMR1 is copied to?

- T1CON
- CCPR1
- TMR2
- PR2

Question 10 1 / 1 pts

What is a duty cycle?

- The percentage of the period where the signal is 'low' or 'off'.
- The sum of the Ton and Toff.
- The percentage of the period where the signal is 'high' or 'on'.
- The percentage of the frequency where the signal is 'high' or 'on'.

Incorrect

Question 11 0 / 1 pts

What should be the value of PR2 if a 1000Hz signal is generated by the PWM module? Assume F_{OSC} = 4MHz and Timer2 prescaler value of 1:16.

- 61
- 15
- 62
- 250

(0.6/1000) (4*10^6)(1/16) (1/4) - 1 = 61.5 = 61

Question 12 1 / 1 pts

Which of the following is true for the capture module?

- The value of CCPRx is copied to Timer1 when an event happens at RC2.
- None of the choices.
- The value of Timer1 is compared to CCPRx when an event happens at RC2.
- The value of TMR1 is copied to CCPRx when an event happens at RC2.

Question 13 1 / 1 pts

True or False: When TMR2 = PR2, an interrupt will generated if enabled.

- True
- False

Question 14 1 / 1 pts

Which of the following will happen when TMR1 = CCPR1 (match)?

- [ ] An overflow interrupt is generated.
- [x] Match interrupt is generated.
- [ ] RA0 will be high, low or unchanged.
- [x] RC2 will be high, low or unchanged.

Question 15 1 / 1 pts

True or False: PEIE bit should be set '0' inorder for Timer1 and Timer2 interrupts to work.

- True
- False

Question 16 1 / 1 pts

Given an F_{OSC} of 4MHz and a prescaler of 1:8, what is the timeout of Timer1 from 0000h to FFFFh?

- 0.52423 s
- 0.2621 s
- 0.0524 s
- 0.0262 s

[1/((4*10^6)/4)] * 4 * 65536 = 0.524288

Question 17 1 / 1 pts

What is the event when the timer transition from FFh to 00h?

- Overflow
- Underflow
- Interrupt
- Event

Incorrect

Question 18 0 / 1 pts

Given an F_{OSC} of 4MHz and a prescaler of 1:4, what should be the value of PR2 if a match interrupt is generated every 2 ms?

- 500
- None of the choices. (0.002)((4*10^6)/4)(1/4) - 1 = 499
- 1000
- 750

Question 19

1 / 1 pts

Which of the following timers are count up?

- PR2
- Timer1
- Timer2
- Timer0

Question 20

1 / 1 pts

Which of the following registers are used for the PWM resolution?

- CCPR2L
- CCP2CON<5:4>
- CCP1CON<5:4>
- CCPR1L

Quiz Score: **15.75** out of 20