
# DIGITAL DESIGN

# ASSIGNMENT REPORT

# ASSIGNMENT ID : 1

**Student Name: 罗嘉诚**

**Student ID: 12112910**

# Assignment 1

## Question 1 (10 point)

① $(234.5)_{10}$ → base 3

3 | 234 … 0
3 | 78 … 0
3 | 26 … 2
3 | 8 … 2
2

0.5 × 3 = 1.5 … 1
→ 0.5
0.5 × 3 = 1.5 … 1
→ 0.5 → ……

$(234)_{10} \rightarrow (22200)_3$

$(0.5)_{10} \rightarrow (0.11\cdots)_3$

所以 $(234.5)_{10} \rightarrow (22200.11\cdots)_3$

② $(234.5)_{10}$ → base 5

5 | 234 … 4
5 | 46 … 1
5 | 9 … 4
1

0.5 × 5 = 2.5 … 2
→ 0.5
0.5 × 5 = 2.5 … 2
→ 0.5 ……

$(234)_{10} \rightarrow (414)_5$

$(0.5)_{10} \rightarrow (0.22\cdots)$

所以 $(234.5)_{10} \rightarrow (1414.22\cdots)_5$ ✓

③ $(234.5)_{10}$ → base 6

6 | 234 … 0
6 | 39 … 3
6 | 6 … 0
1

0.5 × 6 = 3.0 … 3
→ 0

$(234)_{10} \rightarrow (1030)_6$ $(0.5)_{10} \rightarrow (0.3)_6$

所以 $(234.5)_{10} \rightarrow (1030.3)_6$ ✓

④ $(234.5)_{10}$ → base 12

12 | 234 … 6
12 | 19 … 7
1

0.5 × 12 = 6.0 … 6
→ 0

$(234)_{10} \rightarrow (176)_{12}$

$(0.5)_{10} = (0.6)_{12}$

所以 $(234.5)_{10} \rightarrow (176.6)_{12}$ ✓

⑤ $(234.5)_{10}$ → base 16

16 | 234 … 10 (A)
14 (E)

0.5 × 16 = 8.0 … 8
→ 0

$(234)_{10} = (EA)_{16}$ $(0.5)_{10} = (0.8)_{16}$

所以 $(234.5)_{10} \rightarrow (EA.8)_{16}$ ✓

## Question 2 (5 point)

$(791)_{11}$ 的反码 $(AAA)_{11} - (791)_{11} = (319)_{11}$

so. the 10's complement of $(791)_{11}$ is $(319)_{11}$ ✓

## Question 3 (15 point)

① $(a+b+c')(a'b'+c) = (a+b+c')(a'b') + (a+b+c')c$

$= aa'b' + a'b'b + a'b'c' + ac + bc + cc'$

$= 0 + 0 + a'b'c' + ac + bc + 0$

$= a'b'c' + ac + bc = a'b'c' + (a+b)c = (a+b)'c' + (a+b)c$

$= (a+b)' \oplus c$ ✓

② $a'b'c + ab'c + abc + a'bc$

$= a'c(b'+b) + ac(b'+b)$

$= a'c + ac = c(a'+a) = c$ ✓

③ $(a+c)(a'+b+c)(a'+b'+c)$

$= (aa' + ca' + ab + cb + ac + c)(a'+b'+c)$

$= (0 + c(a+a') + ab + cb + c)(a'+b'+c)$

$= (ab + cb + c)(a'+b'+c) = aa'b + a'bc + a'c$
$+ a'bc + cbb' + cb$
$+ a'c + b'c + c$

$= a'bc + a'c + cb + b'c + c$

$= bc + a'c + b'c + c = c$ ✓

## Question 4 (15 point)

① $F_1(A,B,C) = \sum(1,2,6,7) = A'B'C + A'BC' + ABC' + ABC$

$= A'B'C + (A'BC' + ABC') + (ABC' + ABC) = A'B'C + BC' + AB$

② $F_2(A,B,C) = \sum(0,1,2,3,5) = A'B'C' + A'BC + A'BC' + A'BC + AB'C$

$= A'B'(C+C') + A'B(C+C') + AB'C$

$= A'B' + A'B + AB'C = A'(B'+B) + AB'C$

$= A' + AB'C = A' + B'C$

③ $F_3(A,B,C) = \sum(3,5,6,7) = A'BC + AB'C + ABC' + ABC$

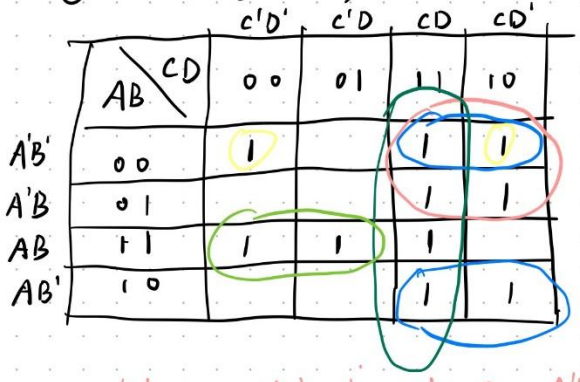
$= A'BC + ABC + AB'C + ABC + ABC' + ABC.$

$= BC(A'+A) + AC(B'+B) + AB(C+C')$

$= BC + AC + AB$

# Question 5 (15 point)

① $F_1(A,B,C,D) = \sum(0,2,3,6,7,10,11,12,13,15)$




0 → 0000 11 → 1011
2 → 0010 12 → 1100
3 → 0011 13 → 1101
6 → 0110 15 → 1111
7 → 0111
10 → 1010

$A'B'CD + A'B'CD' + A'BCD + A'BCD' = A'B'C + A'BC = A'C$

$ABC'D' + ABC'D = ABC'$

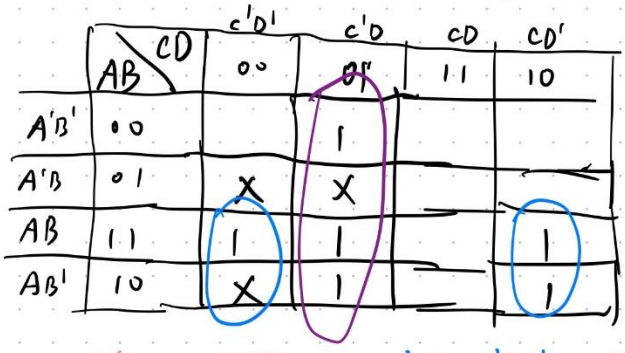
$A'B'C'D' + A'B'CD' = A'B'D'$

$A'B'CD + A'B'CD' + AB'CD + AB'CD' = A'B'C + AB'C = B'C$

$A'B'CD + A'BCD + ABCD + AB'CD = A'CD + ACD = CD$

$F_1(A,B,C,D) = A'C + B'C + CD + ABC' + A'B'D'$ ✓

② $F_2(A,B,C,D) = \sum(1,9,10,12,13,14) + d(4,5,8)$



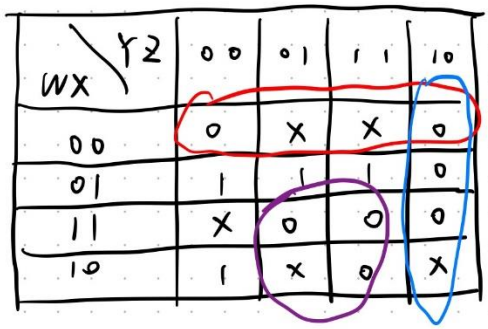

1 → 0001 4 → 0100
9 → 1001 5 → 0101
10 → 1010 8 → 1000
12 → 1100
13 → 1101
14 → 1110

$ABC'D' + AB'C'D' + ABCD' + AB'CD' = AC'D' + ACD' = AD'$

$AB'C'D + A'BC'D + ABC'D + AB'CD = A'C'D + AC'D = C'D$

$F_2(A,B,C,D) = AD' + C'D$ ✓

③ $F_3(W,X,Y,Z) = \prod(0,2,6,11,13,14,15) + d(1,3,9,10,12)$




$F_3' = W'X' + YZ' + WZ$

所以 $F_3(W,X,Y,Z) = (W+X)(Y'+Z)(W'+Z')$ ✓

## Question 6 (10 point)

$f(a,b,c,d) = abd' + c'd + a'cd' + b'cd'$

| ab \ CD | c'D' (00) | c'D (01) | CD (11) | CD' (10) |
|---|---|---|---|---|
| a'b' (00) | 0 | 1 | 0 | 1 |
| a'b (01) | 0 | 1 | 0 | 1 |
| ab (11) | 1 | 1 | 0 | 1 |
| ab' (10) | 0 | 1 | 0 | 1 |

| ab \ cd | c'd' (00) | c'd (01) | cd (11) | cd' (10) |
|---|---|---|---|---|
| a'b' (00) | 1 | 0 | 0 | 1 |
| a'b (01) | 1 | 1 | 1 | 0 |
| ab (11) | 1 | 0 | 1 | 0 |
| ab' (10) | 1 | 0 | 1 | 1 |

$g(a,b,c,d) = (a'b'd + bcd' + ac'd)'$

所以 fg 的真值表如下：

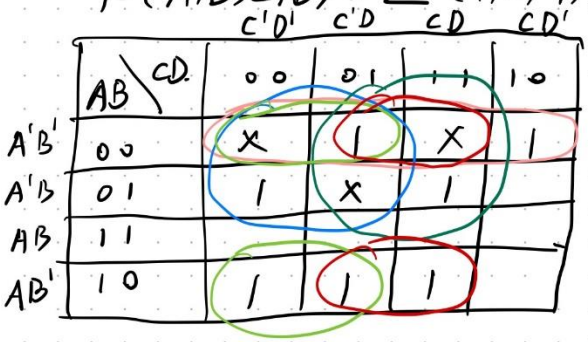
| ab \ cd | c'd' (00) | c'd (01) | cd (11) | cd' (10) |
|---|---|---|---|---|
| a'b' (00) | 0 | 0 | 0 | 1 |
| a'b (01) | 0 | 1 | 0 | 0 |
| ab (11) | 1 | 0 | 0 | 0 |
| ab' (10) | 0 | 0 | 0 | 1 |

$fg = abc'd' + a'bc'd + ab'cd' + a'b'cd'$

$= abc'd' + a'bc'd + b'cd'$ ✓

# Question 7 (15 point)

$F(A,B,C,D) = \sum(1,2,4,7,8,9,11) + d(0,3,5)$




$A'B'C'D' + A'B'C'D + A'B'CD + A'B'CD'$

$= A'B'C' + A'B'C = A'B'$

$A'B'C'D' + A'B'C'D + A'BC'D' + A'BC'D$

$= A'B'C' + A'BC' = A'C'$

$A'B'C'D + A'B'CD + A'BC'D + A'BCD$

$= A'B'D + A'BD = A'D$

$A'BC'D' + A'B'C'D + AB'C'D' + AB'C'D$

$= A'B'C' + AB'C' = B'C'$

$AB'C'D + AB'CD + A'B'C'D + A'B'CD$

$= AB'D + A'B'D = B'D$

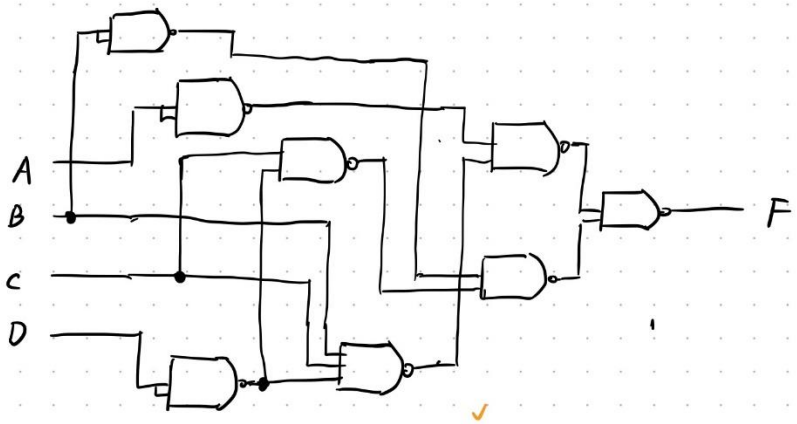
So $F(A,B,C,D) = A'B' + A'C' + A'D + B'C' + B'D$ ✓

① use XAND gates only

$F(A,B,C,D) = A'(B'+C'+D) + B'(C'+D)$

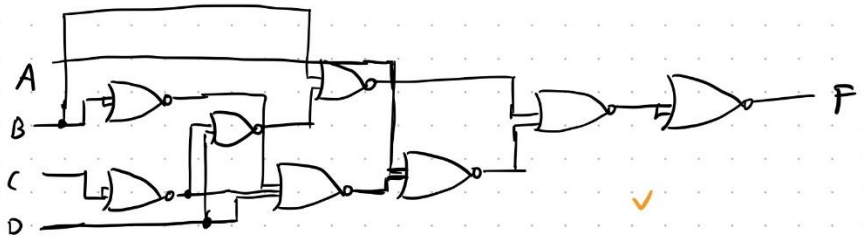
$= A'(BCD')' + B'(CD')'$

$= \left((A'(BCD')')'(B'(CD')')'\right)'$




② use NOR gates only.

$$
\begin{aligned}
F(A,B,C,D) &= A'B' + A'C' + A'D + B'C' + B'D \\
&= A'(B'+C'+D) + B'(C'+D) \\
&= \left(A + (B'+C'+D)'\right)' + \left(B + (C'+D)'\right)' \\
&= \left(\left(\left(A + (B'+C'+D)'\right)' + \left(B + (C'+D)'\right)'\right)'\right)'
\end{aligned}
$$



## Question 8 (15 point)

① $F_1(A,B,C,D) = \sum(1,3,5,7)$

$F_2(A,B,C,D) = \sum(2,3,6,7)$

$F = F_1 F_2$

| AB \ CD | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 00 | | 1 | 1 | |
| 01 | | 1 | 1 | |
| 11 | | | | |
| 10 | | | | |

$F_1 = \sum(1,3,5,7)$

| AB \ CD | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 00 | | | 1 | 1 |
| 01 | | | 1 | 1 |
| 11 | | | | |
| 10 | | | | |

$F_2 = \sum(2,3,6,7)$

So, $F = F_1 F_2$

| AB \ CD | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 00 | | | 1 | |
| 01 | | | 1 | |
| 11 | | | | |
| 10 | | | | |

$F = F_1 F_2 = A'B'CD + A'BCD$

$= A'CD$

② $F_1(A,B,C,D) = \sum(1,3,5,6,8,10,11,12,13)$

$F_2(A,B,C,D) = \sum(0,3,5,8,9,11,13,15)$

So, $F = F_1 F_2 = \sum(3,5,8,11,13)$

| AB \ CD | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 00 | | | 1 | |
| 01 | | 1 | | |
| 11 | | 1 | | |
| 10 | 1 | | 1 | |

$F = F_1 F_2 = BC'D + B'CD + AB'C'D'$

$A'BC'D + ABC'D = BC'D$

$A'B'CD + AB'CD = B'CD$

$AB'C'D'$

③ $F_1(A,B,C) = \prod L(0,3,6,7)$

$F_2(A,B,C) = \prod L(1,3,7)$

| AB \ C | 0 | 1 |
|---|---|---|
| 00 | 0 | 1 |
| 01 | 1 | 0 |
| 11 | 0 | 0 |
| 10 | 1 | 1 |

| AB \ C | 0 | 1 |
|---|---|---|
| 00 | 1 | 0 |
| 01 | 1 | 0 |
| 11 | 1 | 0 |
| 10 | 1 | 1 |

$F = F_1 F_2$

| AB \ C | 0 | 1 |
|---|---|---|
| 00 | 0 | 0 |
| 01 | 1 | 0 |
| 11 | 0 | 0 |
| 10 | 1 | 1 |

$F = AB'C' + AB'C + A'BC'$

$= AB' + A'BC'$

## PART 2: DIGITAL DESIGN LAB (TASK1)

### DESIGN

*Describe the design of your system by providing the following information:*

- *Truth-table*

设$a = (a_1a_0)_2, b = (b_1b_0)_2$ 其中$a_0, a_1, b_0, b_1 \in \{0,1\}$。

若$c = a \times b$，则 $c$ 使用二进制表示最少需要 4 位，即$c = (c_3c_2c_1c_0)_2$其中 $c_0c_1c_2c_3 \in \{0,1\}$。

| $a = (a_1a_0)_2$ | $b = (b_1b_0)_2$ | $c = (c_3c_2c_1c_0)_2$ |
|---|---|---|
| $(00)_2$ | $(00)_2$ | $(0000)_2$ |
| $(00)_2$ | $(01)_2$ | $(0000)_2$ |
| $(00)_2$ | $(10)_2$ | $(0000)_2$ |
| $(00)_2$ | $(11)_2$ | $(0000)_2$ |
| $(01)_2$ | $(00)_2$ | $(0000)_2$ |
| $(01)_2$ | $(01)_2$ | $(0001)_2$ |
| $(01)_2$ | $(10)_2$ | $(0010)_2$ |
| $(01)_2$ | $(11)_2$ | $(0011)_2$ |
| $(10)_2$ | $(00)_2$ | $(0000)_2$ |
| $(10)_2$ | $(01)_2$ | $(0010)_2$ |
| $(10)_2$ | $(10)_2$ | $(0100)_2$ |
| $(10)_2$ | $(11)_2$ | $(0110)_2$ |
| $(11)_2$ | $(00)_2$ | $(0000)_2$ |
| $(11)_2$ | $(01)_2$ | $(0011)_2$ |
| $(11)_2$ | $(10)_2$ | $(0110)_2$ |
| $(11)_2$ | $(11)_2$ | $(1001)_2$ |

$c_3, c_2, c_1, c_0$ 关于$a_0, a_1, b_0, b_1$的真值表：

1. $c_0$ 关于$a_0, a_1, b_0, b_1$的真值表

| $c_0$ | $b = (b_1b_0)_2$ | $(00)_2$ | $(01)_2$ | $(10)_2$ | $(11)_2$ |
|---|---|---|---|---|---|
| $a = (a_1a_0)_2$ | | | | | |
| $(00)_2$ | | 0 | 0 | 0 | 0 |
| $(01)_2$ | | 0 | 1 | 0 | 1 |
| $(10)_2$ | | 0 | 0 | 0 | 0 |
| $(11)_2$ | | 0 | 1 | 0 | 1 |

2. $c_1$ 关于$a_0, a_1, b_0, b_1$的真值表

| $c_1$ | $b = (b_1b_0)_2$ | $(00)_2$ | $(01)_2$ | $(10)_2$ | $(11)_2$ |
|---|---|---|---|---|---|
| $a = (a_1a_0)_2$ | | | | | |
| $(00)_2$ | | 0 | 0 | 0 | 0 |
| $(01)_2$ | | 0 | 0 | 1 | 1 |
| $(10)_2$ | | 0 | 1 | 0 | 1 |
| $(11)_2$ | | 0 | 1 | 1 | 0 |

3. $c_2$ 关于$a_0, a_1, b_0, b_1$的真值表

| $c_2$ | $b = (b_1b_0)_2$ | $(00)_2$ | $(01)_2$ | $(10)_2$ | $(11)_2$ |
|---|---|---|---|---|---|
| $a = (a_1a_0)_2$ | | | | | |
| $(00)_2$ | | 0 | 0 | 0 | 0 |
| $(01)_2$ | | 0 | 0 | 0 | 0 |
| $(10)_2$ | | 0 | 0 | 1 | 1 |
| $(11)_2$ | | 0 | 0 | 1 | 0 |

4. $c_3$ 关于$a_0, a_1, b_0, b_1$的真值表

| $c_3$ | $b = (b_1b_0)_2$ | $(00)_2$ | $(01)_2$ | $(10)_2$ | $(11)_2$ |
|---|---|---|---|---|---|
| $a = (a_1a_0)_2$ | | | | | |
| $(00)_2$ | | 0 | 0 | 0 | 0 |
| $(01)_2$ | | 0 | 0 | 0 | 0 |
| $(10)_2$ | | 0 | 0 | 0 | 0 |
| $(11)_2$ | | 0 | 0 | 0 | 1 |

- *Verilog design (provide the Verilog code)*

根据上述真值表，可以得到逻辑表达式：

$$c_0 = b_1'b_0a_1'a_0 + b_1b_0a_1'a_0 + b_1'b_0a_1a_0 + b_1b_0a_1a_0 = b_0a_1'a_0 + b_0a_1a_0 = b_0a_0$$

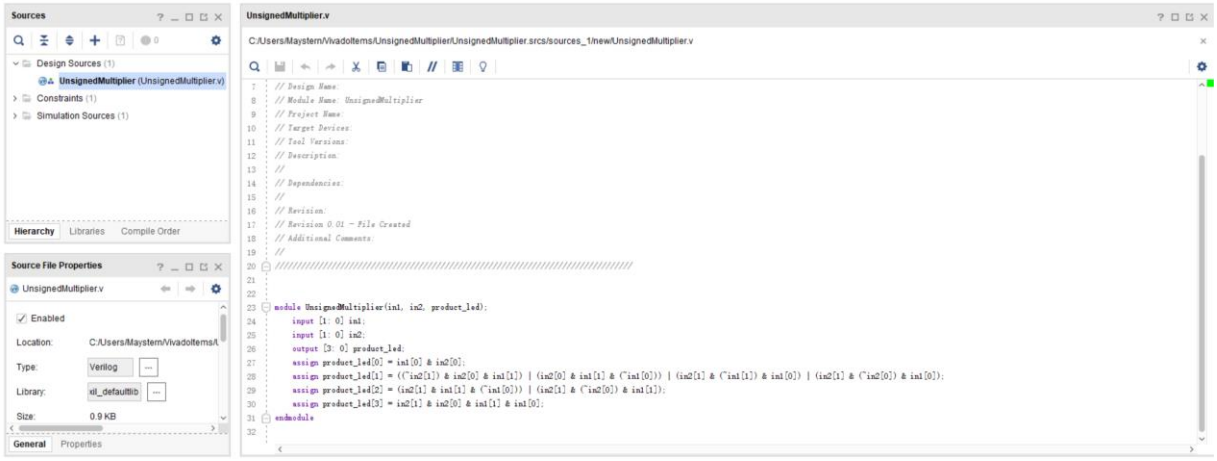
$$c_1 = b_1'b_0a_1a_0 + b_1'b_0a_1a_0' + b_1'b_0a_1a_0' + b_1b_0a_1a_0' + b_1b_0a_1'a_0 + b_1b_0'a_1'a_0 + b_1b_0'a_1'a_0 + b_1b_0'a_1a_0 = b_1'b_0a_1 + b_0a_1a_0' + b_1a_1'a_0 + b_1b_0'a_0$$

$$c_2 = b_1b_0a_1a_0' + b_1b_0'a_1a_0' + b_1b_0'a_1a_0' + b_1b_0'a_1a_0 = b_1a_1a_0' + b_1b_0'a_1$$

$$c_3 = b_1b_0a_1a_0$$

据此可以使用 verilog 进行编程实现两个 2-bit 二进制数的乘法器。

```
`timescale 1ns / 1ps
module UnsignedMultiplier(in1, in2, product_led);
    input [1: 0] in1;
    input [1: 0] in2;
    output [3: 0] product_led;
    assign product_led[0] = in1[0] & in2[0];
    assign product_led[1] = ((~in2[1]) & in2[0] & in1[1]) | (in2[0] & in1[1] & (~in1[0])) | (in2[1] & (~in1[1]) & in1[0]) | (in2[1] & (~in2[0]) & in1[0]);
    assign product_led[2] = (in2[1] & in1[1] & (~in1[0])) | (in2[1] & (~in2[0]) & in1[1]);
    assign product_led[3] = in2[1] & in2[0] & in1[1] & in1[0];
endmodule
```

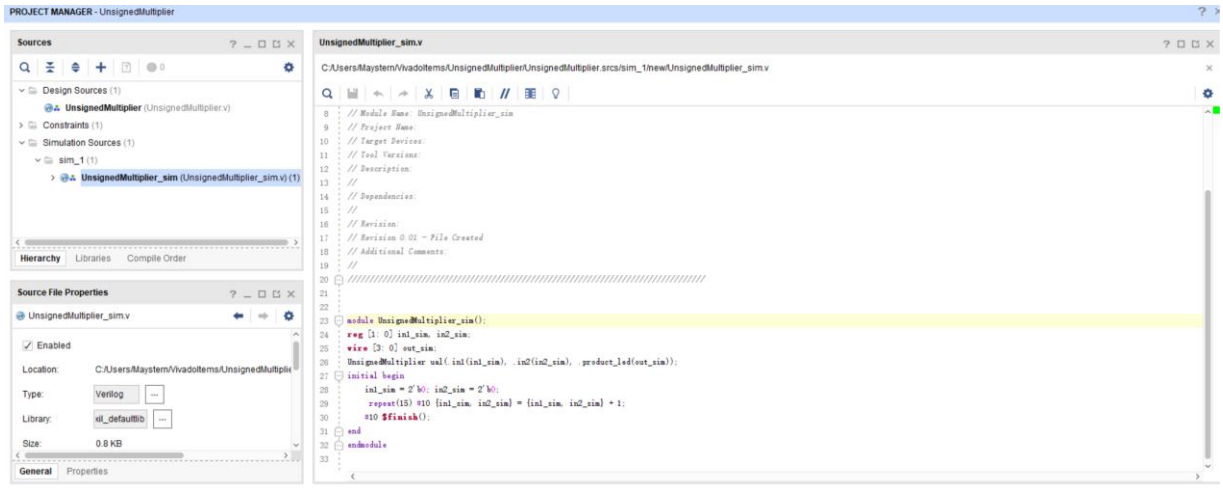



## SIMULATION

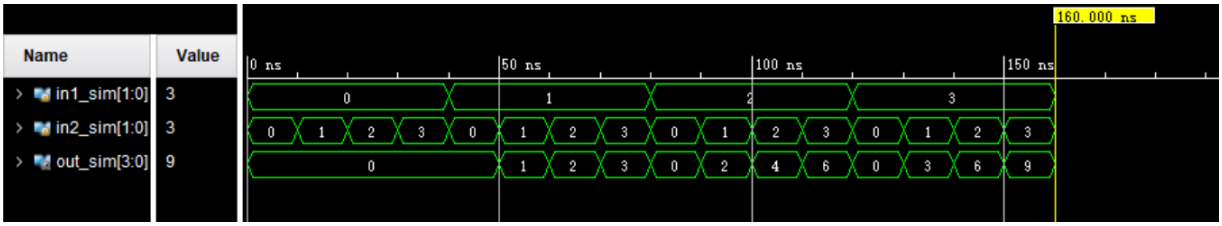
*Describe how you build the test bench and do the simulation.*

- *Using Verilog(provide the Verilog code)*

```
`timescale 1ns / 1ps
module UnsignedMultiplier_sim();
reg [1: 0] in1_sim, in2_sim;
wire [3: 0] out_sim;
UnsignedMultiplier ual(.in1(in1_sim), .in2(in2_sim), .product_led(out_sim));
initial begin
    in1_sim = 2'b0; in2_sim = 2'b0;
     repeat(15) #10 {in1_sim, in2_sim} = {in1_sim, in2_sim} + 1;
    #10 $finish();
end
endmodule
```




- *Wave form of simulation result (provide screen shots)*




- *The description on whether the simulation result is same as the truth-table, is the function of the design meet the expectation.*

在上图中，in1_sim, in2_sim 分别表示输入的两个 2-bit 二进制数，out_sim 表示计算得出的这两个无符号二进制数的乘积。

仿真遍历了输入数据的所有情况（共 16 种），都得到了预期输出，完成构建一个 2-bit 二进制数乘法器的实验目标。并且该视图采用 Full version，可以看到没有多余的仿真。

## THE DESCRIPTION OF OPERATION

*Describe the problem occurred while in the lab and your solution. Any suggestions are welcomed.*

- *Problems and solutions*

# PART 2: DIGITAL DESIGN LAB (TASK2)

## DESIGN

*Describe the design of your system by providing the following information:*

- *Truth-table*

| $(A+B)'$ | $B=(b_1b_0)_2$ | $(00)_2$ | $(01)_2$ | $(10)_2$ | $(11)_2$ |
|---|---|---|---|---|---|
| $A=(a_1a_0)_2$ | | | | | |
| $(00)_2$ | | 11 | 10 | 01 | 00 |
| $(01)_2$ | | 10 | 10 | 00 | 00 |
| $(10)_2$ | | 01 | 00 | 01 | 00 |
| $(11)_2$ | | 00 | 00 | 00 | 00 |

| $A'B'$ | $B=(b_1b_0)_2$ | $(00)_2$ | $(01)_2$ | $(10)_2$ | $(11)_2$ |
|---|---|---|---|---|---|
| $A=(a_1a_0)_2$ | | | | | |
| $(00)_2$ | | 11 | 10 | 01 | 00 |
| $(01)_2$ | | 10 | 10 | 00 | 00 |
| $(10)_2$ | | 01 | 00 | 01 | 00 |
| $(11)_2$ | | 00 | 00 | 00 | 00 |

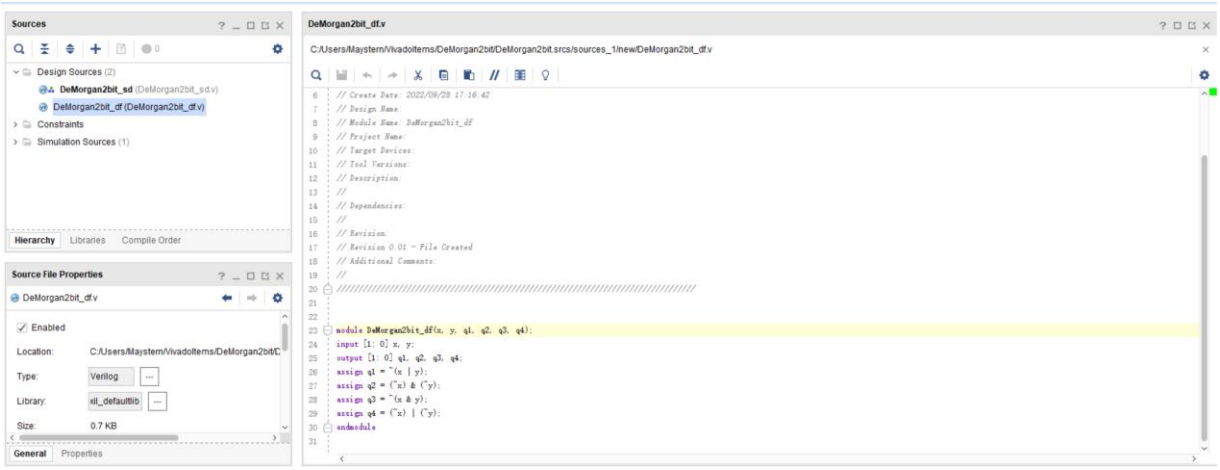
| $(AB)'$ | $B=(b_1b_0)_2$ | $(00)_2$ | $(01)_2$ | $(10)_2$ | $(11)_2$ |
|---|---|---|---|---|---|
| $A=(a_1a_0)_2$ | | | | | |
| $(00)_2$ | | 11 | 11 | 11 | 11 |
| $(01)_2$ | | 11 | 10 | 11 | 10 |
| $(10)_2$ | | 11 | 11 | 01 | 01 |

| | | | | | |
|---|---|---|---|---|---|
| $(11)_2$ | | 11 | 10 | 01 | 00 |

| $A' + B'$ | $B = (b_1 b_0)_2$ | $(00)_2$ | $(01)_2$ | $(10)_2$ | $(11)_2$ |
|---|---|---|---|---|---|
| $A = (a_1 a_0)_2$ | | | | | |
| $(00)_2$ | | 11 | 11 | 11 | 11 |
| $(01)_2$ | | 11 | 10 | 11 | 10 |
| $(10)_2$ | | 11 | 11 | 01 | 01 |
| $(11)_2$ | | 11 | 10 | 01 | 00 |

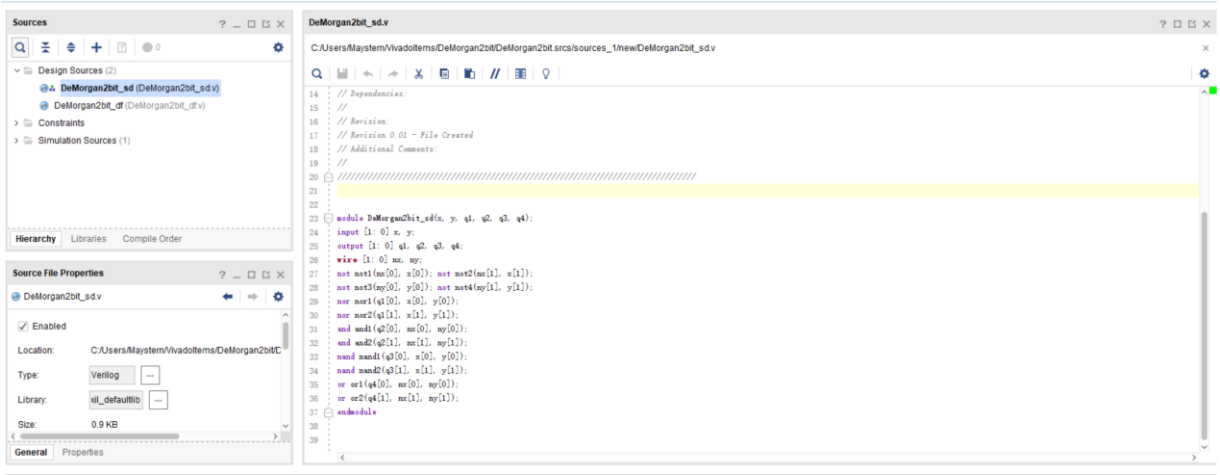
- *Verilog design while using data flow (provide the Verilog code)*

```
`timescale 1ns / 1ps
module DeMorgan2bit_df(x, y, q1, q2, q3, q4);
input [1: 0] x, y;
output [1: 0] q1, q2, q3, q4;
assign q1 = ~(x | y);
assign q2 = (~x) & (~y);
assign q3 = ~(x & y);
assign q4 = (~x) | (~y);
endmodule
```



- *Verilog design while using structured design (provide the Verilog code)*

```
`timescale 1ns / 1ps
module DeMorgan2bit_sd(x, y, q1, q2, q3, q4);
input [1: 0] x, y;
output [1: 0] q1, q2, q3, q4;
wire [1: 0] nx, ny;
not not1(nx[0], x[0]); not not2(nx[1], x[1]);
not not3(ny[0], y[0]); not not4(ny[1], y[1]);
nor nor1(q1[0], x[0], y[0]);
nor nor2(q1[1], x[1], y[1]);
and and1(q2[0], nx[0], ny[0]);
and and2(q2[1], nx[1], ny[1]);
nand nand1(q3[0], x[0], y[0]);
nand nand2(q3[1], x[1], y[1]);
or or1(q4[0], nx[0], ny[0]);
or or2(q4[1], nx[1], ny[1]);
endmodule
```

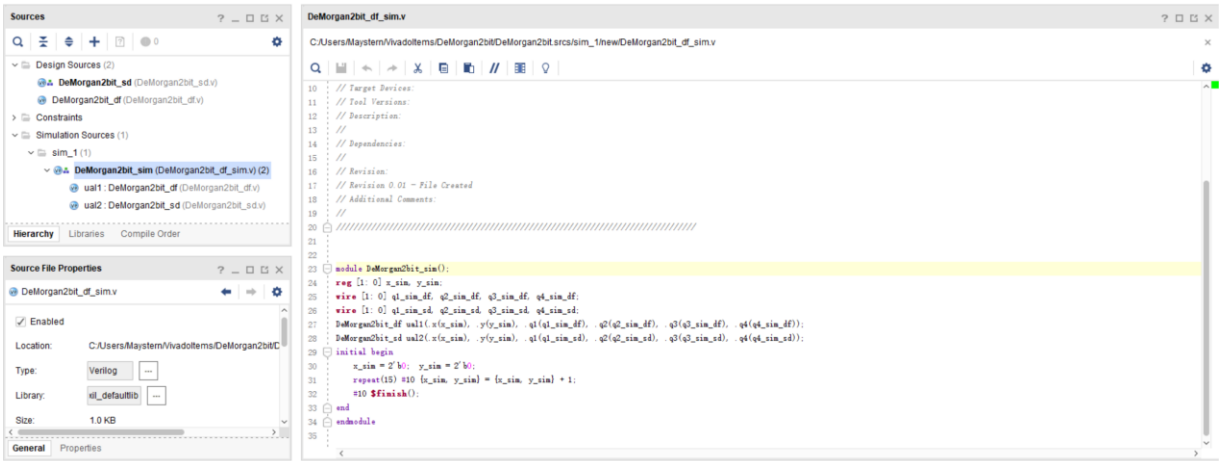


## SIMULATION

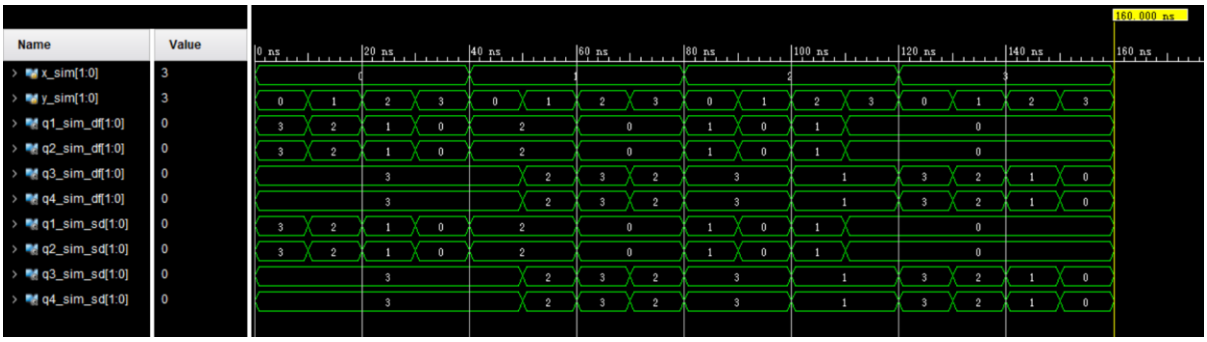
*Describe how you build the test bench and do the simulation.*

- *Using Verilog (provide the Verilog code)*

```
module DeMorgan2bit_sim();
reg [1: 0] x_sim, y_sim;
wire [1: 0] q1_sim_df, q2_sim_df, q3_sim_df, q4_sim_df;
wire [1: 0] q1_sim_sd, q2_sim_sd, q3_sim_sd, q4_sim_sd;
DeMorgan2bit_df
ual1(.x(x_sim), .y(y_sim), .q1(q1_sim_df), .q2(q2_sim_df), .q3(q3_sim_df), .q4(q4_sim_df));
DeMorgan2bit_sd
ual2(.x(x_sim), .y(y_sim), .q1(q1_sim_sd), .q2(q2_sim_sd), .q3(q3_sim_sd), .q4(q4_sim_sd));
initial begin
    x_sim = 2'b0;  y_sim = 2'b0;
    repeat(15) #10 {x_sim, y_sim} = {x_sim, y_sim} + 1;
    #10 $finish();
end
endmodule
```




- *Wave form of simulation result (provide screen shots)*




- *The description on whether the simulation result is same as the truth-table, is the function of the design meet the expectation*

  在上图中 x_sim 和 y_sim 分别表示给出的两个 2-bit 无符号二进制数$A, B$，q1_sim_df 表示采用数据流描述方式设计的输出 $(A+B)'$，q2_sim_df 表示采用数据流描述方式设计的输出 $A'B'$，q3_sim_df 表示采用数据流描述方式设计的输出 $(AB)'$，q4_sim_df 表示采用数据流描述方式设计的输出 $A'+B'$; q1_sim_sd 表示采用结构化描述方式设计的输出 $(A+B)'$，q2_sim_sd 表示采用结构化描述方式设计的输出 $A'B'$，q3_sim_sd 表示采用结构化描述方式设计的输出 $(AB)'$，q4_sim_sd 表示采用结构化描述方式设计的输出 $A'+B'$。

  仿真遍历了输入数据的所有情况（共 16 种），都得到了预期输出。并且该视图采用 Full version，可以看到没有多余的仿真。

  **结论：通过上述实验结果，我们有理由相信：DeMorgan Theorem 对 2-bit 二进制数依然成立。即对于两个 2-bit 二进制数 $A, B$ 等式 $(A+B)'=A'B', (AB)'=A'+B'$恒成立。**

## THE DESCRIPTION OF OPERATION

*Describe the problem occurred while in the lab and your solution. Any suggestions are welcomed.*

- *Problems and solutions*

# PART 2: DIGITAL DESIGN LAB (TASK3)

## DESIGN

*Describe the design of your system by providing the following information:*

- Sum of Minimum Term

$$F(A,B,C,D) = \sum(0,2,3,6,7,10,11,12,13,15) = A'B'C'D' + A'B'CD' + A'B'CD + A'BCD' + A'BCD + AB'CD' + AB'CD + ABC'D' + ABC'D + ABCD$$

- Product of Maximum Item

$$F(A,B,C,D) = \prod(1,4,5,8,9,14) = (A+B+C+D')(A+B'+C+D)\,(A+B'+C+D')(A'+B'+C'+D)(A'+B+C+D)(A'+B+C+D')$$

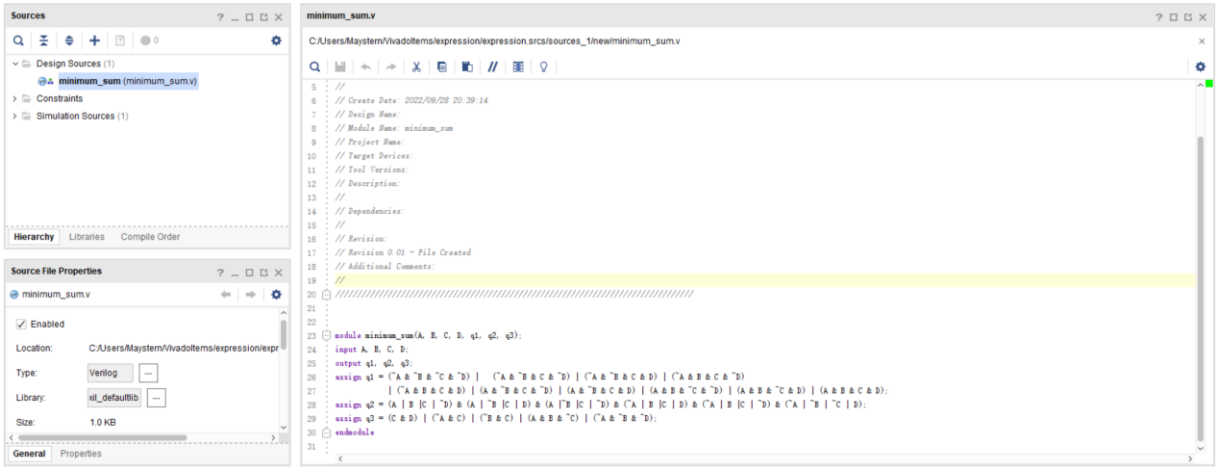
- Using a Karnaugh Map to Simplify the Circuit in Sum-of-Product

| F | $CD$ | $(00)_2$ | $(01)_2$ | $(11)_2$ | $(10)_2$ |
|---|---|---|---|---|---|
| $AB$ | | | | | |
| $(00)_2$ | | 1 | 0 | 1 | 1 |
| $(01)_2$ | | 0 | 0 | 1 | 1 |
| $(11)_2$ | | 1 | 1 | 1 | 0 |
| $(10)_2$ | | 0 | 0 | 1 | 1 |

$$F(A,B,C,D) = (A'B'CD + A'BCD + ABCD + AB'CD) + (A'B'CD + A'BCD + A'B'CD' + A'BCD') + (AB'CD + AB'CD' + A'B'CD + A'B'CD') + (ABC'D' + ABC'D) + (A'B'C'D' + A'B'CD') = CD + A'C + B'C + ABC' + A'B'D'$$

- *Verilog design while using data flow (provide the Verilog code)*

```
`timescale 1ns / 1ps
module minimum_sum(A, B, C, D, q1, q2, q3);
input A, B, C, D;
output q1, q2, q3;
assign q1 = (~A & ~B & ~C & ~D) | (~A & ~B & C & ~D) | (~A & ~B & C & D) |(~A & B & C & ~D) | (~A & B & C & D) | (A & ~B & C & ~D) | (A & ~B & C & D) | (A & B & ~C & ~D) | (A & B & ~C & D) | (A & B & C & D);
assign q2 = (A | B |C | ~D) & (A | ~B |C | D) & (A |~B |C | ~D) & (~A | B |C | D) & (~A | B |C | ~D) & (~A | ~B | ~C | D);
assign q3 = (C & D) | (~A & C) | (~B & C) | (A & B & ~C) | (~A & ~B & ~D);
endmodule
```

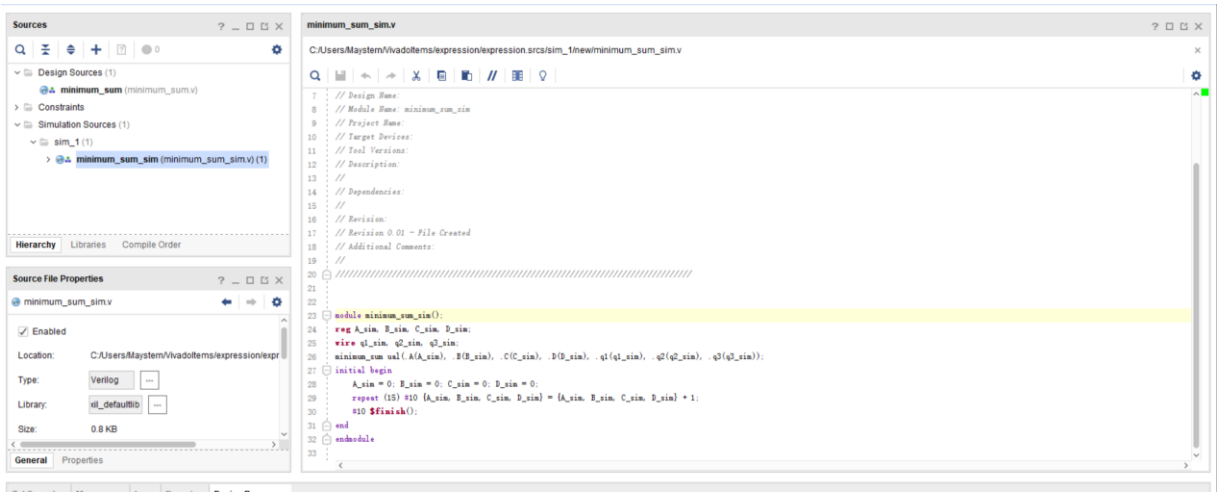



## SIMULATION

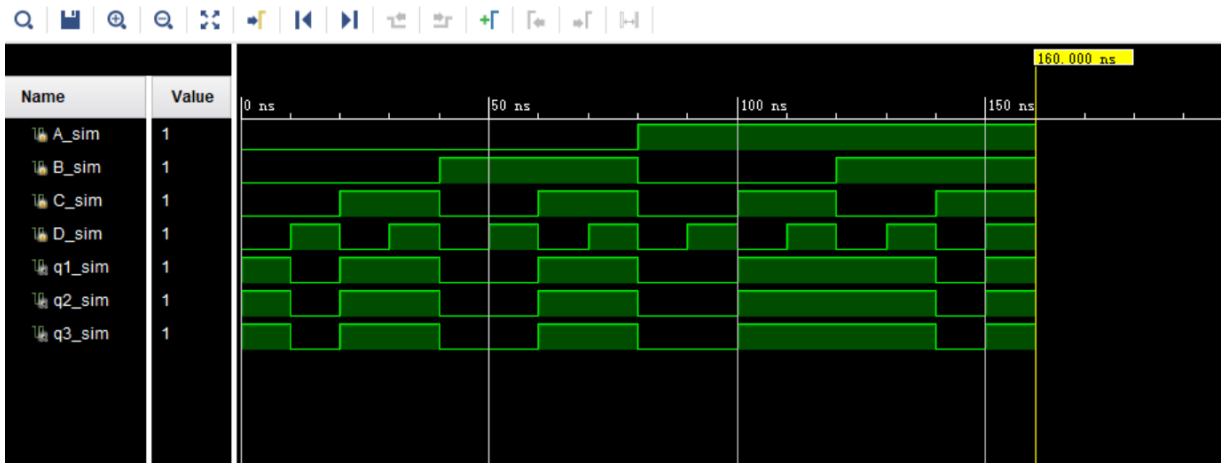
*Describe how you build the test bench and do the simulation.*

- *Using Verilog (provide the Verilog code)*

```
`timescale 1ns / 1ps
module minimum_sum_sim();
reg A_sim, B_sim, C_sim, D_sim;
wire q1_sim, q2_sim, q3_sim;
minimum_sum
ual(.A(A_sim), .B(B_sim), .C(C_sim), .D(D_sim), .q1(q1_sim), .q2(q2_sim), .q3(q3_sim));
initial begin
    A_sim = 0; B_sim = 0; C_sim = 0; D_sim = 0;
    repeat (15) #10 {A_sim, B_sim, C_sim, D_sim} = {A_sim, B_sim, C_sim, D_sim} + 1;
    #10 $finish();
end
endmodule
```




- *Wave form of simulation result (provide screen shots)*



- *The description on whether the simulation result is same as the truth-table, is the function of the design meet the expectation*

  在上图中，A_sim, B_sim, C_sim, D_sim 分别表示输入数据的 A,B,C,D 的取值，q1_sim 表示使用“Sum of Minimum Term”方式计算出表达式$F(A,B,C,D)$的值，q2_sim 表示使用“Product of Maximum Item”方式计算出表达式$F(A,B,C,D)$的值，q3_sim 表示使用卡诺图化简得到的表达式计算出表达式$F(A,B,C,D)$的值。

  仿真遍历了输入数据的所有情况（共 16 种），都得到了预期输出。并且该视图采用 Full version，可以看到没有多余的仿真。

## THE DESCRIPTION OF OPERATION

*Describe the problem occurred while in the lab and your solution. Any suggestions are welcomed.*

- *Problems and solutions*