Assignment 4

Question 1 ✓

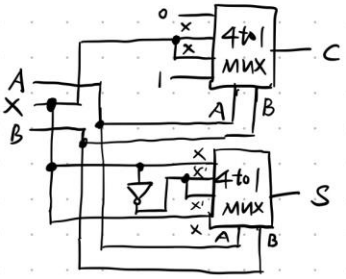
Input			Output	
A	B	X	C	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

当 A=0, B=0 时, C=0, S=X

当 A=0, B=1 时, C=X, S=X'

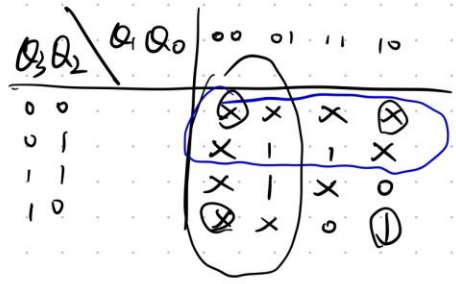
当 A=1, B=0 时, C=X, S=X'

当 A=1, B=1 时, C=1, S=X

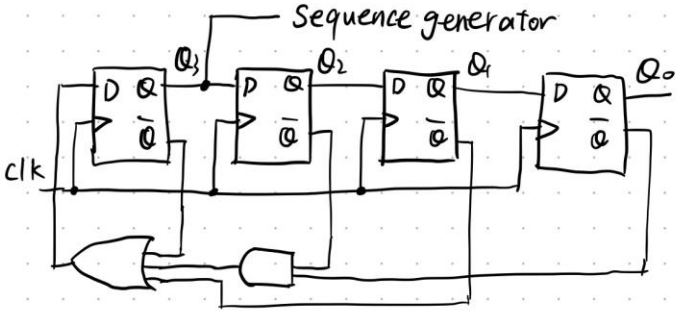


Question 2 ✓

clk	Q_3	Q_2	Q_1	Q_0	Z
↑	1	1	0	1	1
↑	1	1	1	0	0
↑	0	1	1	1	1
↑	1	0	1	1	0
↑	0	1	0	1	1
↑	1	0	1	0	1
↑	1	1	0	1	1
↑	1	1	1	0	0
↑	0	1	1	1	1
↑	1	0	1	1	0

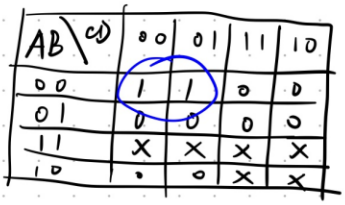


$Z = Q_3' + Q_1' + Q_2'Q_0'$



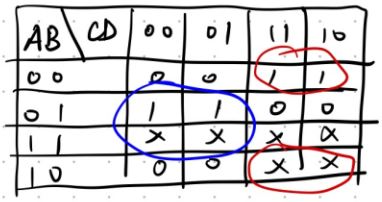
Question 3

Input				Output			
A	B	C	D	X	Y	Z	R
0	0	0	0	1	0	0	1
0	0	0	1	1	0	0	0
0	0	1	0	0	1	1	1
0	0	1	1	0	1	1	0
0	1	0	0	0	1	0	1
0	1	0	1	0	1	0	0
0	1	1	0	0	0	1	1
0	1	1	1	0	0	1	0
1	0	0	0	0	0	0	1
1	0	0	1	0	0	0	0



$X = A'B'C'$

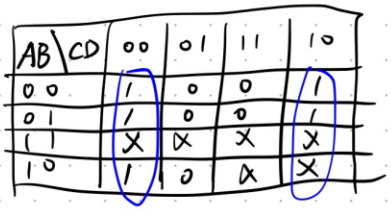
$= (A+B+C)'$



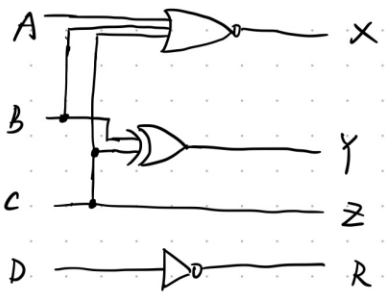
$Y = BC' + B'C$

$= B \oplus C$

$Z = C$



$R = D'$



Question 4

① 8个未使用状态

Q_A	Q_B	Q_C	Q_D
0	0	1	0
0	1	0	0
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	0	1	1
1	1	0	1

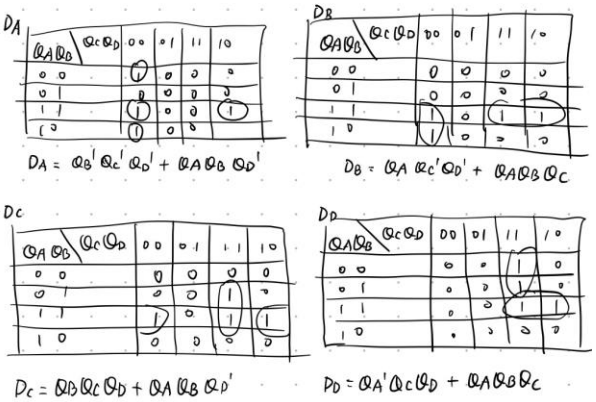
② 8个未使用状态与其接下来的状态

Q_A	Q_B	Q_C	Q_D	Q_A'	Q_B'	Q_C'	Q_D'
0	0	1	0	1	0	0	1
0	1	0	0	1	0	1	0
0	1	0	1	0	0	1	0
0	1	1	0	1	0	1	1
1	0	0	1	0	1	0	0
1	0	1	0	1	1	0	1
1	0	1	1	0	1	0	1
1	1	0	1	0	1	1	0

⇒ 电路一但输入非法状态，无法通过电路形成合法状态.

③ 可以将所有非法状态都在下一个时钟跳变沿变成初态 0000

Present				Next				DFF Input			
Q_A	Q_B	Q_C	Q_D	Q_A	Q_B	Q_C	Q_D	D_A	D_B	D_C	D_D
0	0	0	0	1	0	0	0	1	0	0	0
0	0	0	1	0	0	0	0	0	0	0	0
0	0	1	0	0	0	0	0	0	0	0	0
0	0	1	1	0	0	0	1	0	0	0	1
0	1	0	0	0	0	0	0	0	0	0	0
0	1	0	1	0	0	0	0	0	0	0	0
0	1	1	0	0	0	0	0	0	0	0	0
0	1	1	1	0	0	1	1	0	0	1	1
1	0	0	0	1	1	0	0	1	1	0	0
1	0	0	1	0	0	0	0	0	0	0	0
1	0	1	0	0	0	0	0	0	0	0	0
1	0	1	1	0	0	0	0	0	0	0	0
1	1	0	0	1	1	1	0	1	1	1	0
1	1	0	1	0	0	0	0	0	0	0	0
1	1	1	0	1	1	1	1	1	1	1	1
1	1	1	1	0	0	0	0	0	0	0	0



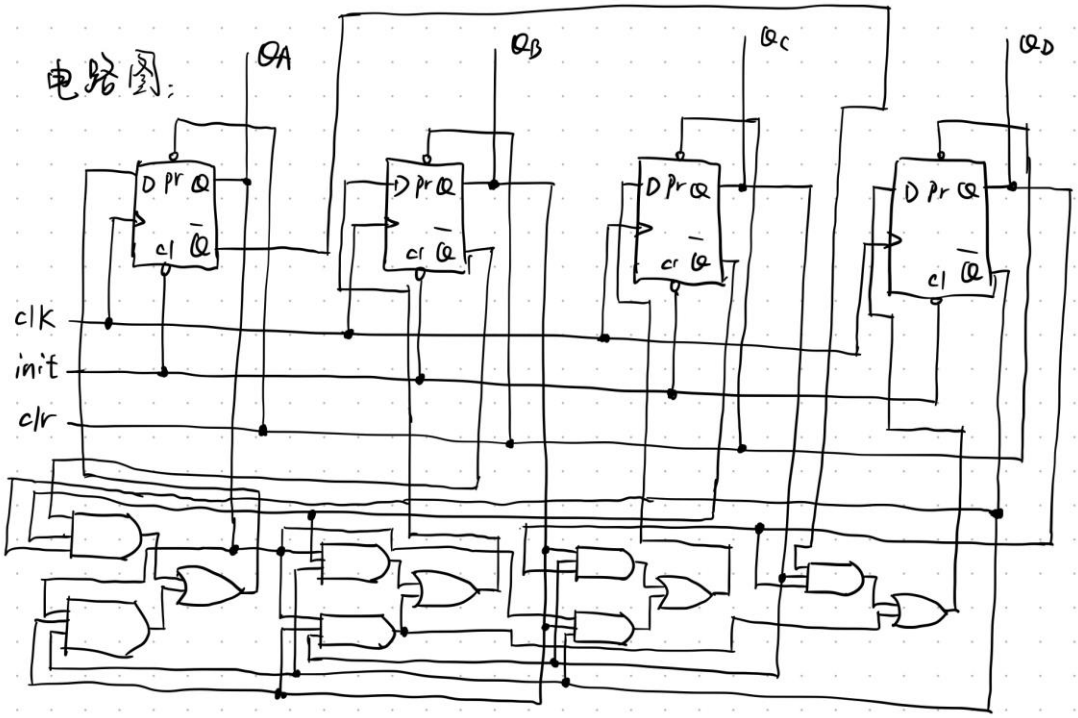
$D_A = Q_B' Q_C' Q_D' + Q_A Q_B Q_D'$

$D_B = Q_A Q_C' Q_D' + Q_A Q_B Q_C$

$D_C = Q_B Q_C Q_D + Q_A Q_B Q_D'$

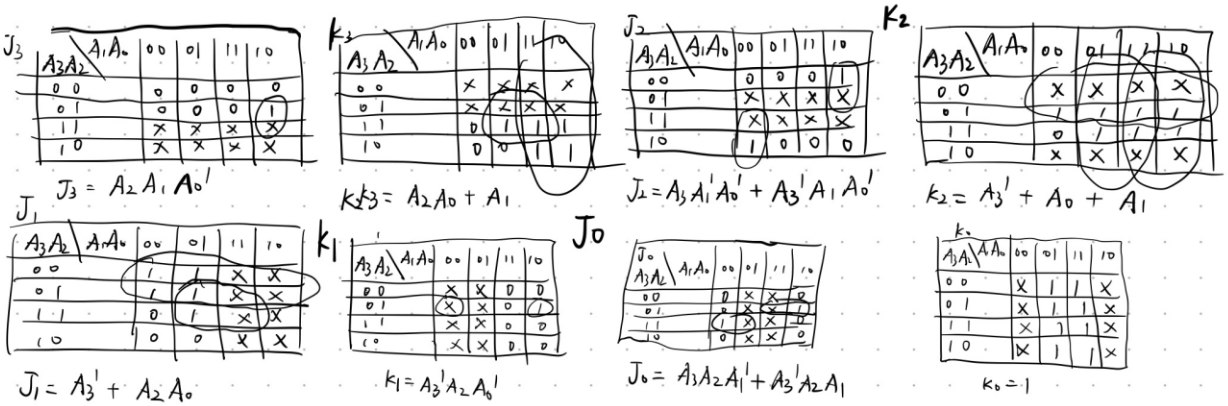
$D_D = Q_A' Q_C Q_D + Q_A Q_B Q_C$

电路图：



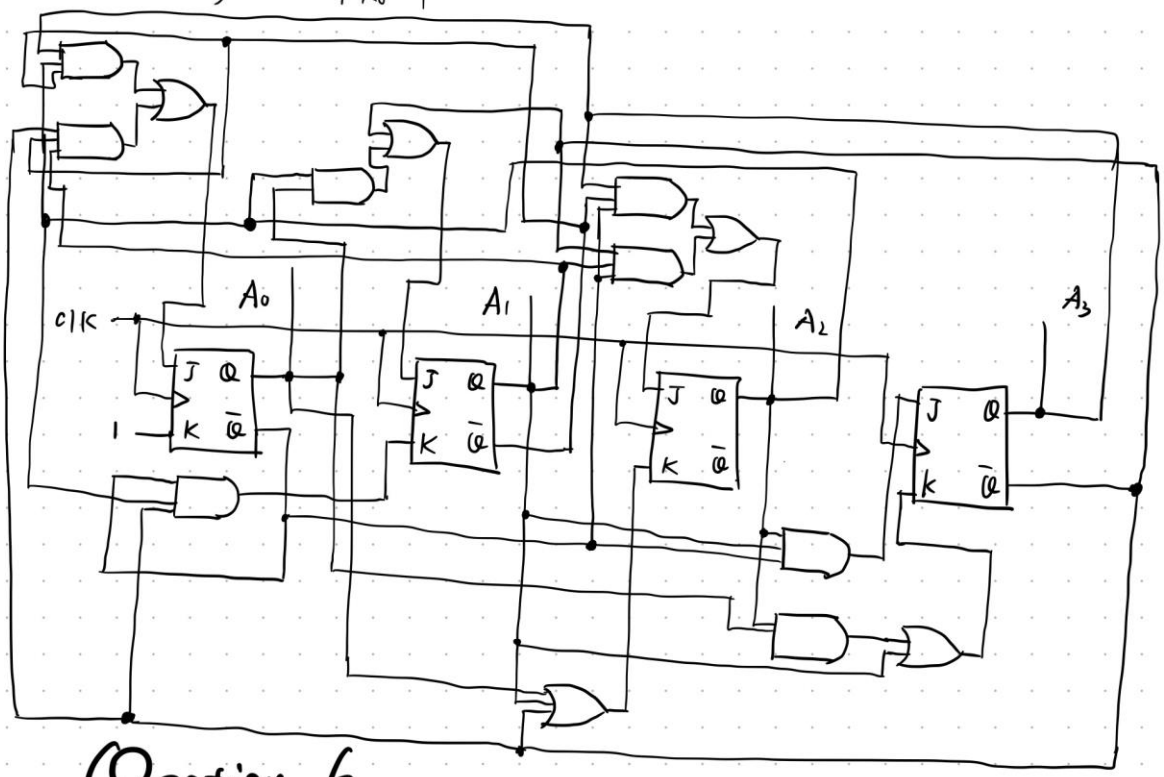
Question 5

Present				Next				JkFF Input							
A_3	A_2	A_1	A_0	A_3	A_2	A_1	A_0	J_3	k_3	J_2	k_2	J_1	k_1	J_0	k_0
0	0	0	0	0	0	1	0	0	X	0	X	1	X	0	X
0	0	0	1	0	0	1	0	0	X	0	X	1	X	X	1
0	0	1	0	0	1	1	0	0	X	1	X	X	0	0	X
0	0	1	1	0	0	1	0	0	X	0	X	X	0	X	1
0	1	0	0	0	0	1	0	0	X	X	X	1	X	0	X
0	1	0	1	0	0	1	0	0	X	X	X	1	X	X	1
0	1	1	0	0	1	0	1	0	X	X	X	1	X	1	X
0	1	1	1	0	0	1	0	0	X	X	X	1	X	0	X
1	0	0	0	1	1	0	0	X	0	1	X	0	X	0	X
1	0	0	1	1	0	0	0	X	0	0	X	0	X	X	1
1	0	1	0	0	0	1	0	X	1	0	X	X	0	X	1
1	0	1	1	0	0	1	0	X	1	0	X	X	0	X	1
1	1	0	0	1	1	0	1	X	0	X	0	0	X	1	X
1	1	0	1	0	0	1	0	X	1	X	1	1	X	X	1
1	1	1	0	0	0	1	0	X	1	X	1	X	0	0	X
1	1	1	1	0	0	1	0	X	1	X	1	X	0	X	1



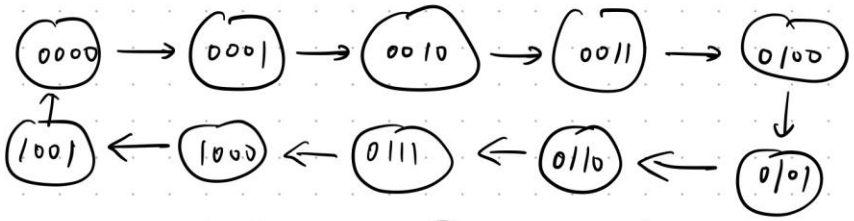
$\begin{cases} J_3 = A_2A_1A_0' \\ K_3 = A_2A_0 + A_1 \end{cases}$ $\begin{cases} J_2 = A_3A_1'A_0' + A_3'A_1A_0' \\ K_2 = A_3' + A_0 + A_1 \end{cases}$

$\begin{cases} J_1 = A_3' + A_2A_0 \\ K_1 = A_3'A_2A_0' \end{cases}$ $\begin{cases} J_0 = A_3A_2A_1' + A_3'A_2A_1 \\ K_0 = 1 \end{cases}$

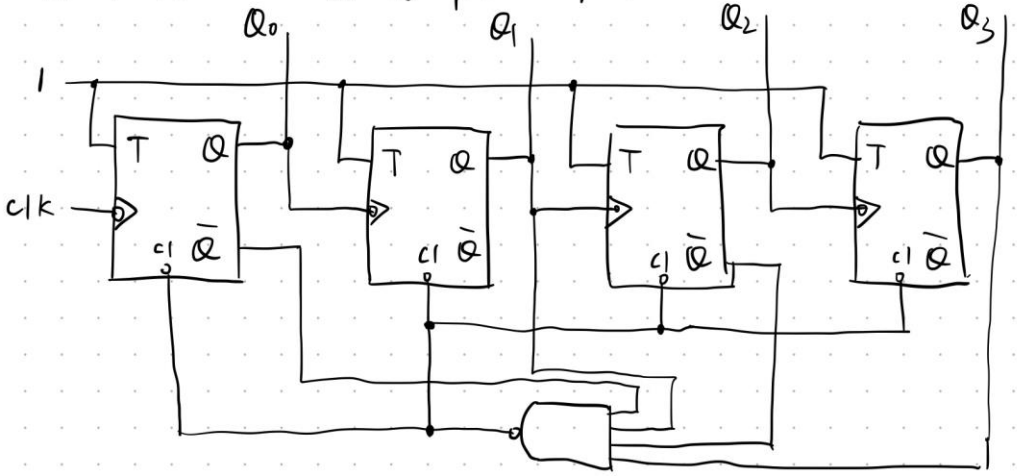


Question 6

State Diagram

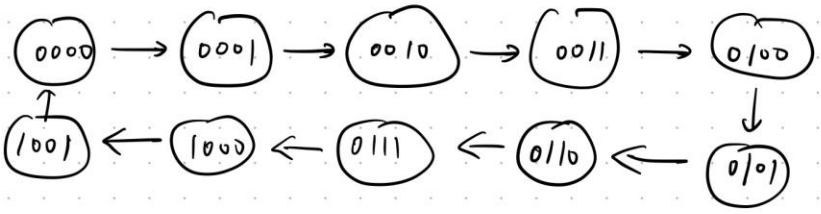


当状态为 1010 时，将利用 clr 端将 counter 置为 0000 状态



Question 7

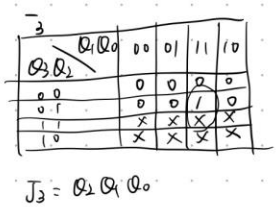
State Diagram



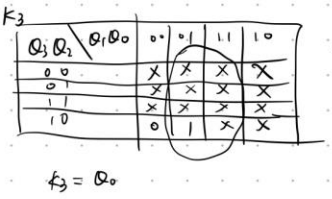
① JK flip-flops

JK flip-flops Input

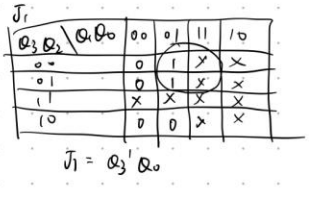
Present				Next											
Q_3	Q_2	Q_1	Q_0	Q_3	Q_2	Q_1	Q_0	J_3	K_3	J_2	K_2	J_1	K_1	J_0	K_0
0	0	0	0	0	0	0	1	0	X	0	X	0	X	1	X
0	0	0	1	0	0	1	0	0	X	0	X	1	X	X	1
0	0	1	0	0	0	1	1	0	X	0	X	X	0	1	X
0	0	1	1	0	1	0	0	0	X	1	X	X	1	X	1
0	1	0	0	0	1	0	1	0	X	X	0	0	X	1	X
0	1	0	1	0	1	1	0	0	X	X	0	1	X	X	1
0	1	1	0	0	1	1	1	0	X	X	0	X	0	1	X
0	1	1	1	1	0	0	0	1	X	X	1	X	1	X	1
1	0	0	0	1	0	0	1	X	0	0	X	0	X	1	X
1	0	0	1	0	0	0	0	X	1	0	X	0	X	X	1



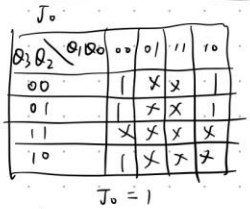
$J_3 = Q_2Q_1Q_0$



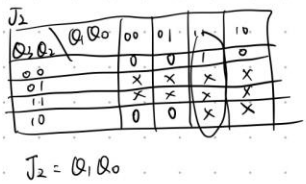
$K_3 = Q_0$



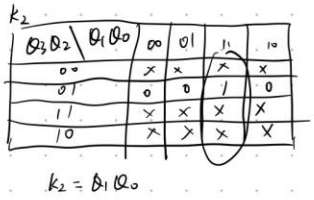
$J_1 = Q_3'Q_0$



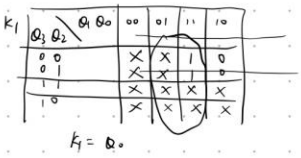
$J_0 = 1$



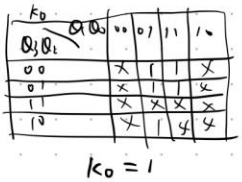
$J_2 = Q_1Q_0$



$K_2 = Q_1Q_0$



$K_1 = Q_0$



$K_0 = 1$

解以 $JQ_3 = Q_2Q_1Q_0$ $JQ_2 = Q_1Q_0$ $JQ_1 = Q_3'Q_0$ $JQ_0 = 1$

$KQ_3 = Q_0$ $KQ_2 = Q_1Q_0$ $KQ_1 = Q_0$ $KQ_0 = 1$

② D flip-flops

D flip-flops Input

Present				Next				D flip-flops Input			
Q_3	Q_2	Q_1	Q_0	Q_3	Q_2	Q_1	Q_0	D_3	D_2	D_1	D_0
0	0	0	0	0	0	0	1	0	0	0	1
0	0	0	1	0	0	1	0	0	0	1	0
0	0	1	0	0	0	1	1	0	0	1	1
0	0	1	1	0	1	0	0	0	1	0	0
0	1	0	0	0	1	0	1	0	1	0	1
0	1	0	1	0	1	1	0	0	1	1	0
0	1	1	0	0	1	1	1	0	1	1	1
0	1	1	1	1	0	0	0	1	0	0	0
1	0	0	0	1	0	0	1	1	0	0	1
1	0	0	1	0	0	0	0	0	0	0	0

D_3

Q_3Q_2 \ Q_1Q_0	00	01	11	10
00	0	0	0	0
01	0	0	1	0
11	X	X	X	X
10	1	0	X	X

$D_3 = Q_2Q_1Q_0 + Q_3Q_1'Q_0'$

D_2

Q_3Q_2 \ Q_1Q_0	00	01	11	10
00	0	0	1	0
01	1	1	0	1
11	X	X	X	X
10	0	0	X	X

$D_2 = Q_2Q_1' + Q_2'Q_1Q_0 + Q_2Q_1Q_0'$

D_1

Q_3Q_2 \ Q_1Q_0	00	01	11	10
00	0	1	0	1
01	0	1	0	1
11	X	X	X	X
10	0	0	X	X

$D_1 = Q_3'Q_1'Q_0 + Q_1Q_0'$

D_0

Q_3Q_2 \ Q_1Q_0	00	01	11	10
00	1	0	0	1
01	1	0	0	1
11	X	X	X	X
10	1	0	0	X

$D_0 = Q_0'$

整理

$$\begin{cases} D_3 = Q_2Q_1Q_0 + Q_3Q_1'Q_0' \\ D_2 = Q_2Q_1' + Q_2'Q_1Q_0 + Q_2Q_1Q_0' \\ D_1 = Q_3'Q_1'Q_0 + Q_1Q_0' \\ D_0 = Q_0' \end{cases}$$

若将上述两个设计与课件中只使用 TFF 的 4bit 同步的 counter，我认为课件中只使用 TFF 的 4bit 同步的 Counter 效率更高.

在课件中
$$\begin{cases} TQ_0 = 1 \\ TQ_1 = Q_1' Q_0 \\ TQ_2 = Q_1 Q_0 \\ TQ_3 = Q_1 Q_0 + Q_2 Q_1 Q_0 \end{cases}$$

AND gates: 4
OR gates: 1
Total gates: 5

在使用 JkFF 设计中

$JQ_3 = Q_2 Q_1 Q_0$ $JQ_2 = Q_1 Q_0$ $JQ_1 = Q_3' Q_0$ $JQ_0 = 1$

$kQ_3 = Q_0$ $kQ_2 = Q_1 Q_0$ $kQ_1 = Q_0$ $kQ_0 = 1$

AND gates: 4
OR gates: 0
→ Total gates: 4

在使用 DFF 设计中

$$\begin{cases} D_3 = Q_2 Q_1 Q_0 + Q_3 Q_1' Q_0' \\ D_2 = Q_2 Q_1' + Q_2' Q_1 Q_0 + Q_2 Q_1 Q_0' = Q_2 \oplus Q_1 Q_0 \\ D_1 = Q_3' Q_1' Q_0 + Q_1 Q_0' \\ D_0 = Q_0' \end{cases}$$

AND gates: 5
OR gates: 2
XOR gates: 1
→ Total gates: 8

所以，使用 Jk Flip-flops 的设计最有效率. 因为它需要最少的门电路