Lecture 10: Register

CS207: Digital Logic

Jialin Liu

Department of Computer Science and Engineering (CSE)
Southern University of Science and Technology (SUSTech)

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Acknowledgement

These slides were prepared based on the slides by Dr. Jianqiao Yu and the ones by Prof. Georgios Theodoropoulos of the Department of CSE at the SUSTech, as well as the contents of the following book:

M. M. Mano and M. Ciletti, *Digital design: with an introduction to the Verilog HDL*. Pearson, 2013

A. Saha and N. Manna, *Digital principles and logic design*. Jones & Bartlett Learning, 2009

Outline of This Lecture

Recap: Sequential Circuits

- A **sequential circuit** is specified by
  - a time sequence of inputs,
  - outputs, and
  - internal states.
- A combinational circuit, but with
  - **memory elements** (记忆元件) connected in a feedback path (反馈回路);
    - A *memory element* is a medium in which one bit of information (0 or 1) can be stored or retained until necessary, and thereafter its contents can be replaced by a new value.
  - outputs are binary functions of not only inputs, but also the present state of the circuit.

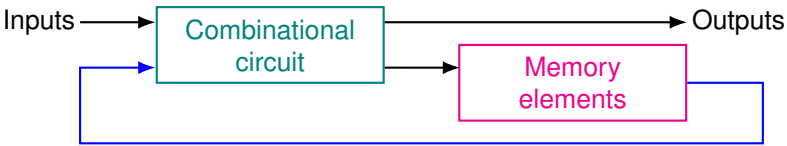
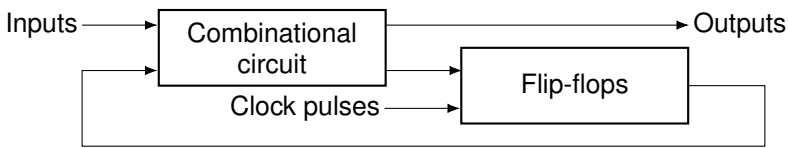


Figure: Block diagram of sequential circuit.

Outline of This Lecture

Clocked Sequential Circuits

- Clocked sequential circuits have flip-flops (FF) and combinational gates.
  - Flip-flops are essential, otherwise reduce to combinational.
  - Circuits that include flip-flops are usually classified by the function they perform rather than by the name of the sequential circuit.
  - Two such circuits are **registers** (寄存器) and **counters** (计数器).



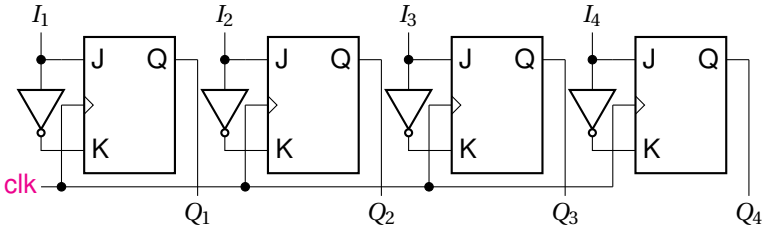
Commonly Used Circuits That Include Flip-flops

- **Register**:
  - A group of flip-flops, each one of which
    - shares a common clock and
    - is capable of storing one bit of binary information.
  - A flip-flop stores one bit of binary information.
    → An n-bit register consists of a group of n flip-flops capable of storing n bits of binary information.
  - In addition to the flip-flops, a register may have combinational gates that perform certain data-processing tasks.

- **Counter**:
  - A special type of register that goes through a predetermined sequence of binary states.

Registers

- Various types of registers are available.
  - The simplest possible register is one that contains no external gates, and is constructed of only flip-flops.
- **Example**: A 4-bit data storage register
  - The clock pulse enables all the flip-flops at the same instant so that the information available at the four inputs can be transferred into the 4-bit register.
  - All the flip-flops in a register should respond to the clock pulse transition.



All the bits are loaded simultaneously with a common clock pulse.

Outline of This Lecture

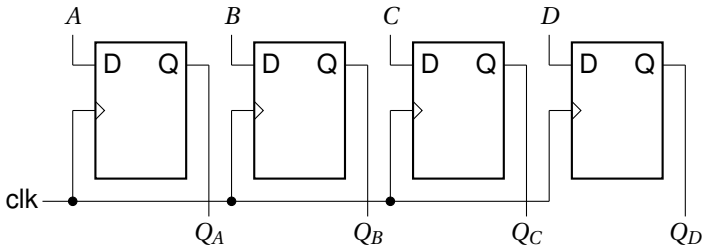
Shift Register

- A register capable of shifting its binary contents either to the left or to the right is called a **shift register** (移位寄存器). → A chain of FFs in cascade (串联).
- The shift register permits the stored data to move from a particular location to some other location within the register.
- The shift registers can be used to
  - transform between parallel/sequential or sequential/parallel data loading/output;
  - perform arithmetic operations;
  - perform some other data processing operations.

Types of Shift Registers

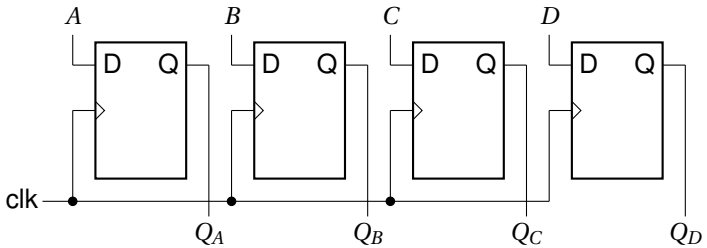
- The data in a shift register can be shifted in two possible ways:
  - **serial shifting** (串行移位) shifts one bit at a time for each clock pulse in a serial manner, beginning with either LSB or MSB.
  - **parallel shifting** (平行移位) shifts all the data (input or output) simultaneously during a single clock pulse.
- Parallel shifting operation is much faster than serial shifting operation.
- Types of shift registers:
  - Serial-in serial-out shift register (串入串出移位寄存器).
  - Serial-in parallel-out shift register (串入并出移位寄存器).
  - Parallel-in serial-out shift register (并入串出移位寄存器).
  - Parallel-in parallel-out shift register (并入并出移位寄存器).

Parallel-in Parallel-out Register (并入并出寄存器)



- Observations?

Parallel-in Parallel-out Register (并入并出寄存器)

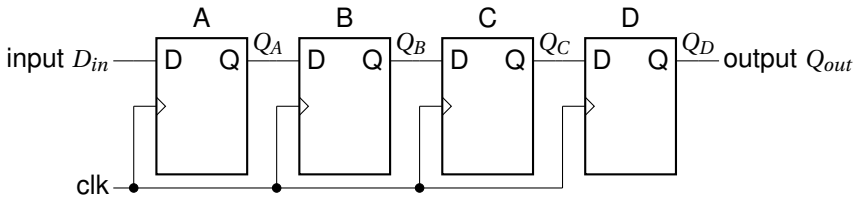


- Observations?
  - All the bits are loaded simultaneously with a common clock pulse.
  - Multiple input lines.
  - Multiple output lines.
  - Number of input lines == number of output lines.

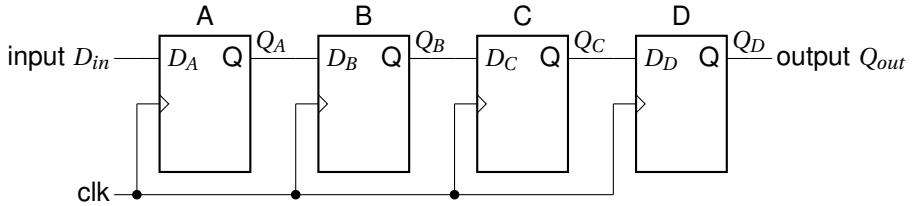
  ← A register with parallel load (并行寄存器).

Serial-in Serial-out Shift Register (串入串出移位寄存器)

- This type of register accepts data serially, i.e., 1 bit at a time at the single input line.
- The output is also obtained on a single output line in a serial fashion.
- The data within the register
  - may be shifted from left to right using **shift-left** register, or
  - may be shifted from right to left using **shift-right** register.
- **Example**: A shift-right register (单向右移寄存器).
  - For each clock pulse, data stored in the register is shifted to the right by one stage.
  - New data is entered into stage A, whereas the data present in stage D are shifted out (to the right).



Serial-in Serial-out Shift Register (串入串出移位寄存器)

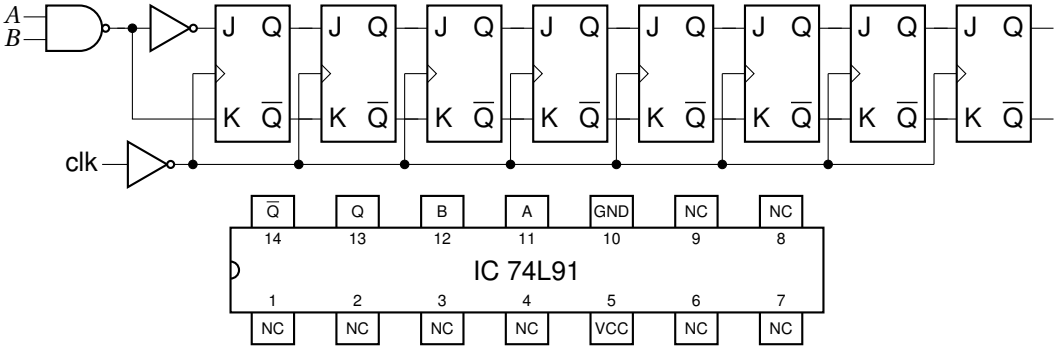


- An example of 1011 into the register. (Input from most right bit to most left bit)

$$
\begin{aligned}
D_A &= D_{in} \\
D_B &= Q_A \\
D_C &= Q_B \\
D_D &= Q_C \\
Q_{out} &= Q_D
\end{aligned}
$$

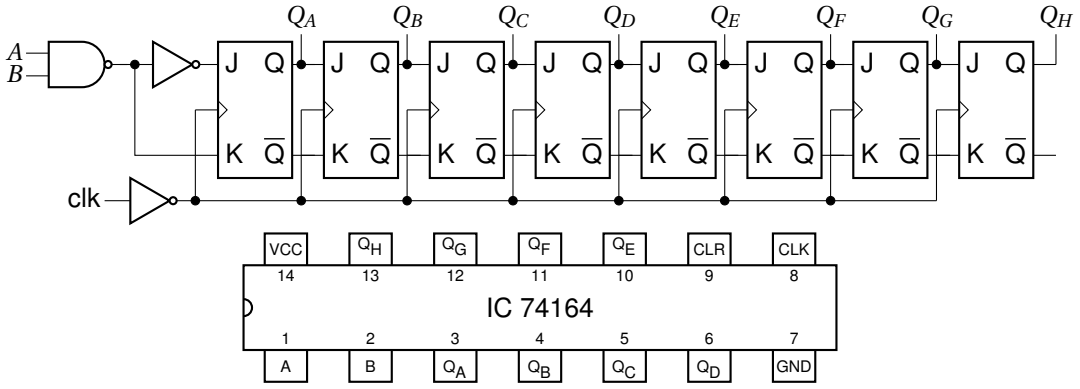
	Input	Q_A	Q_B	Q_C	Q_D	Serial output
Initial value	/	0	0	0	0	0
After 1st clock pulse	1	1	0	0	0	0
After 2nd clock pulse	1	1	1	0	0	0
After 3rd clock pulse	0	0	1	1	0	0
After 4th clock pulse	1	1	0	1	1	1

A Commonly Used Serial-in Serial-out Shift Register: IC 74L91



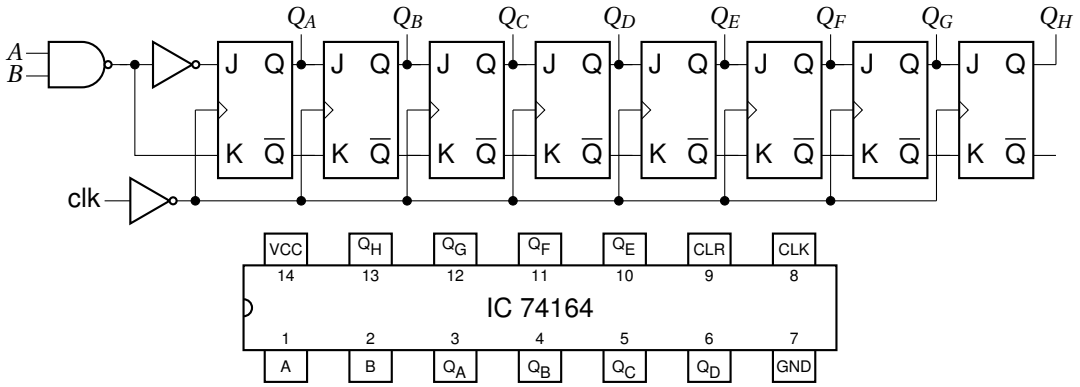
- NC: not connected
- VCC: power supply
- GND: ground

Serial-in Parallel-out Shift Register (串入并出移位寄存器)



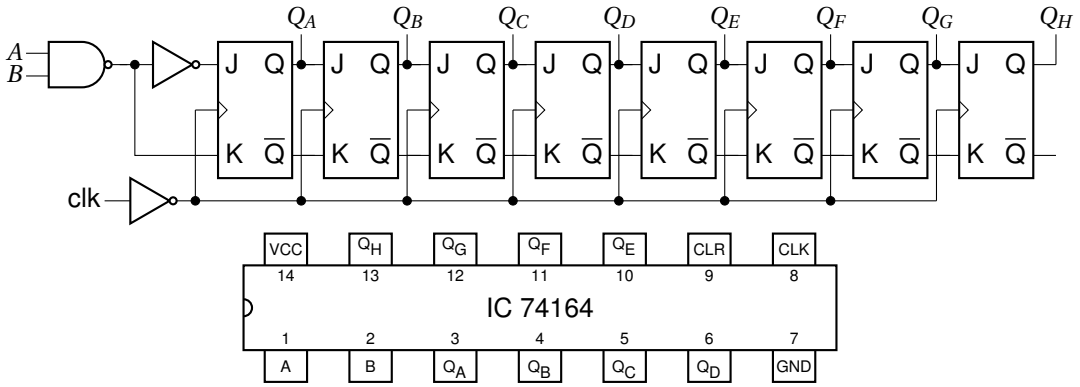
- In this type of register, the data is shifted in serially, but shifted out in parallel.
- To obtain the output data in parallel, it is required that all the output bits are available at the same time.
  → This can be accomplished by connecting the output of each flip-flop to an output pin.

Serial-in Parallel-out Shift Register (串入并出移位寄存器)



- How long will it take to shift an 8-bit number into a 74164 shift register if the clock is set at 1 MHz?

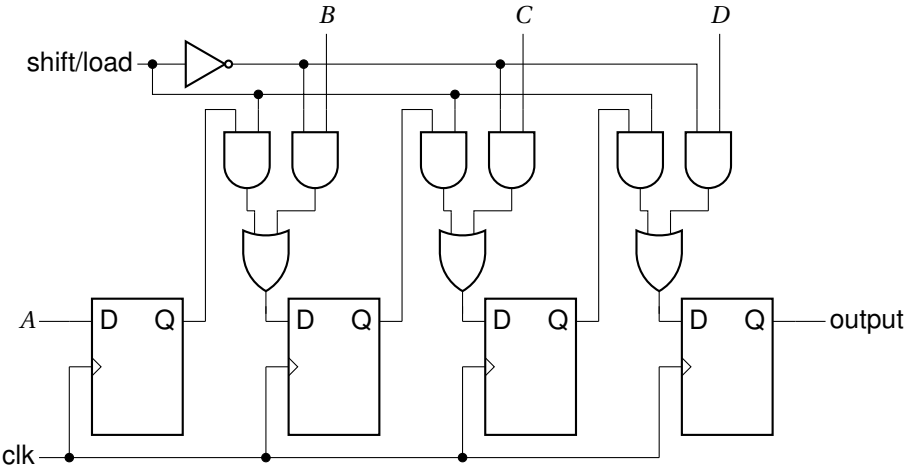
Serial-in Parallel-out Shift Register (串入并出移位寄存器)



- How long will it take to shift an 8-bit number into a 74164 shift register if the clock is set at 1 MHz?
  - A minimum of 8 clock pulses will be required since the data is entered serially. One clock pulse period is 1000 ns, so it will require 8000 ns minimum.

Parallel-in Serial-out Shift Register (并入串出移位寄存器)

- Parallel entry of data into the register.
- Example:



Outline of This Lecture

- If the flip-flop outputs of a shift register are accessible, then information entered serially by shifting can be taken out in parallel from the outputs of the flip-flops.
- If a parallel load capability is added to a shift register, then data entered in parallel can be taken out in serial fashion by shifting the data stored in the register.
- Some shift registers provide the necessary input and output terminals for parallel transfer.
- They may also have both shift-right and shift-left capabilities.

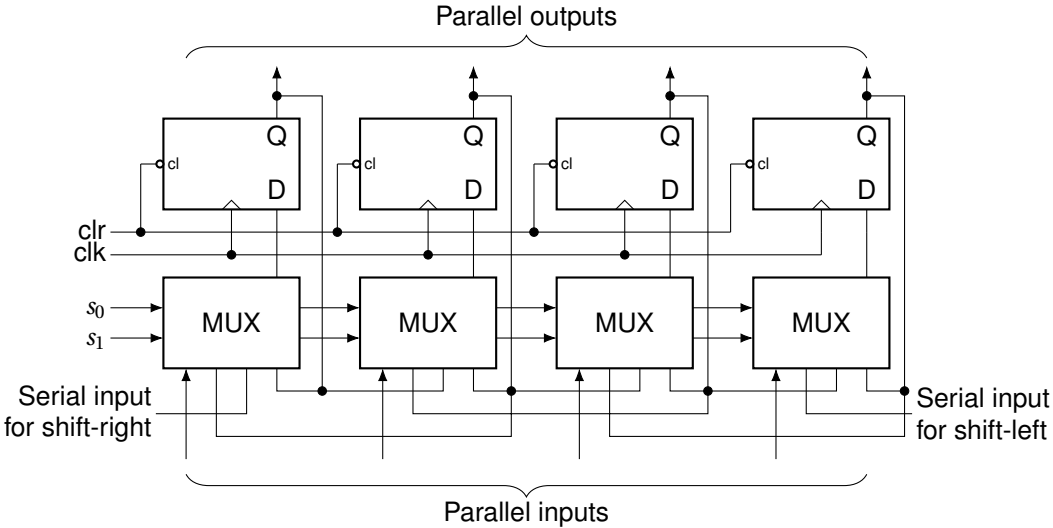
Universal Shift Register (通用移位寄存器)

- A register capable of shifting in one direction only is a **unidirectional shift register** (单向移位寄存器).
- One that can shift in both directions is a **bidirectional shift register** (双向移位寄存器).
- If the register has both shifts and parallel-load capabilities, it is referred to as a **universal shift register** (通用移位寄存器).

Universal Shift Register (通用移位寄存器)

- A clear control to clear the register to `0`.
- A clock input to synchronise the operations.
- A shift-right control to enable the shift-right operation and the serial input and output lines associated with the shift right.
- A shift-left control to enable the shift-left operation and the serial input and output lines associated with the shift left.
- A parallel-load control to enable a parallel transfer and the n input lines associated with the parallel transfer.
- n parallel output lines.
- A control state that leaves the information in the register unchanged in response to the clock.

Universal Shift Register (通用移位寄存器)



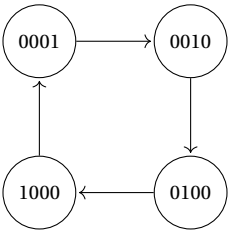
Outline of This Lecture

Shift Register Counters (移位寄存器型计数器)

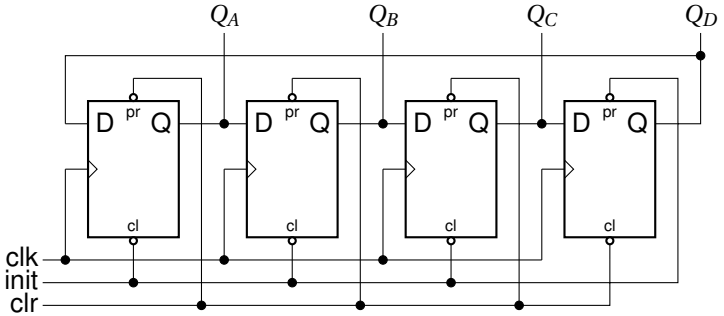
- Shift registers may be arranged to form different types of counters.
- These shift registers use feedback, where the output of the last flip-flop in the shift register is fed back to the first flip-flop.
- Based on the type of this feedback connection, the shift register counters are classified as
  - **ring counter** (环形计数器), and
  - **switch-tail ring counter** or **Johnson counter**.

Ring Counter (环形计数器)

- It is possible to devise a counter-like circuit in which each flip-flop reaches the state $Q = 1$ for exactly one count, while for all other counts $Q = 0$.
  - Then Q indicates directly an occurrence of the corresponding count.
  - Since this does not represent binary numbers, it is better to say that the outputs of the flip-flops represent a code.
- A **ring counter** is a circular shift register with only one flip-flop being set at any particular time and all others being cleared.
- The single bit is shifted from one flip-flop to the other to produce the sequence of timing signals.



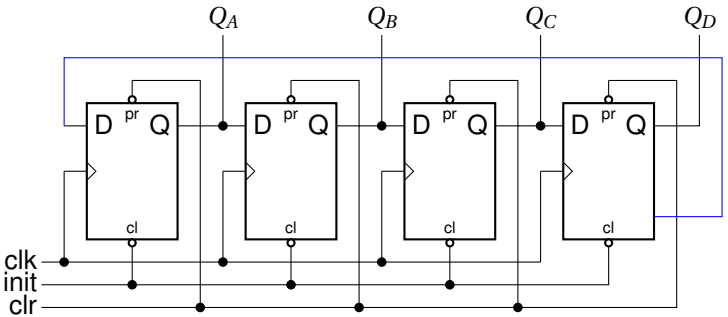
Ring Counter



init	clk	Q_A	Q_B	Q_C	Q_D
L	X	0	0	0	1
H	↑	1	0	0	0
H	↑	0	1	0	0
H	↑	0	0	1	0
H	↑	0	0	0	1

Johnson Counter

- A k-bit ring counter circulates a single bit among the flip-flops to provide k distinguishable states.
- The number of states can be doubled if the shift register is connected as a `switch-tail ring` counter.
  - A circular shift register with the complement of the last flip-flop being connected to the input of the first flip-flop.



Johnson Counter

init	clk	Q_A	Q_B	Q_C	Q_D
L	X	0	0	0	0
H	↑	1	0	0	0
H	↑	1	1	0	0
H	↑	1	1	1	0
H	↑	1	1	1	1
H	↑	0	1	1	1
H	↑	0	0	1	1
H	↑	0	0	0	1
H	↑	0	0	0	0

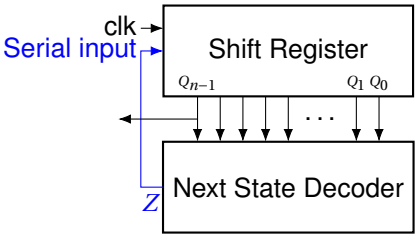
Johnson Counter

- One disadvantage of the circuit is that, if it finds itself in an unused state, it will persist in moving from one invalid state to another and never find its way to a valid state. → 自启动问题
  - The difficulty can be corrected by modifying the circuit to avoid this undesirable condition. (Assignment 4)

Outline of This Lecture

Sequence Generator (序列信号发生器)

- A **sequence generator** is a circuit that generates a desired sequence of bits in synchronisation with a clock.
  - Can be used as a random bit generator, code generator, and prescribed period generator.

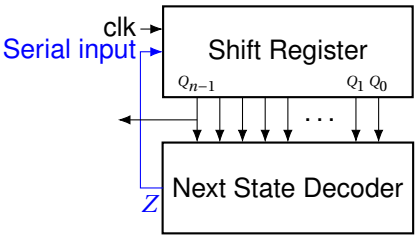


- The output of the next state decoder Z is a function of the shift register state and is connected to the serial input of the shift register.
  - This sequence generator is similar to a ring counter or a Johnson counter.

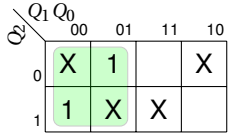
Example: Design A 4-bit Sequence Generator

- We consider the design of a sequence generator to generate a sequence of 1001.
  - The minimum number of flip-flops required to generate a sequence of length N is given by $N \leq 2^n - 1$.
    - In the example, the minimum value of n to satisfy the above condition is 3.
  - Use the output of the register as the input to the combinational circuit, and the sequence as the output of the combinational circuit.
  - Identify the states by the n-bit sequences that may appear in desired original sequence considering the shift.
  - For states that appear in the desired sequence without considering the shift, mark $Z = 1$, otherwise $Z = 0$.

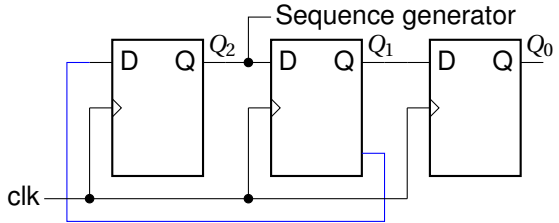
clk	FF outputs Q_2	Q_1	Q_0	Serial input Z
↑	1	1	0	0
↑	0	1	1	0
↑	0	0	1	1
↑	1	0	0	1
↑	1	1	0	0
↑	0	1	1	0



Design A 4-bit Sequence Generator



$$Z = Q_1'$$



Design A 5-bit Sequence Generator

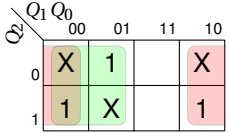
- We consider the design of a sequence generator to generate a sequence of 10011.
- `Have a try!`

Design A 5-bit Sequence Generator

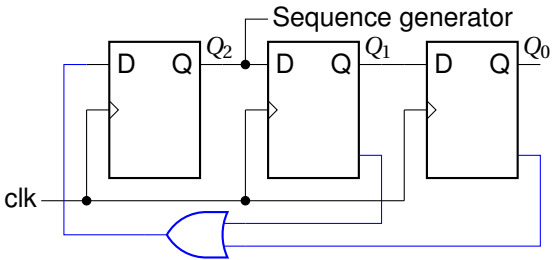
- We consider the design of a sequence generator to generate a sequence of 10011.
- The minimum number of flip-flops required to generate a sequence of length N is given by $N \leq 2^n - 1$.
  - The minimum value of n to satisfy the above condition is 3.

clk	Q_2	Q_1	Q_0	Z
↑	1	1	1	0
↑	0	1	1	0
↑	0	0	1	1
↑	1	0	0	1
↑	1	1	0	1
↑	1	1	1	0
↑	0	1	1	0

Design A 5-bit Sequence Generator



$$Z = Q_1' + Q_0'$$



Design A 6-bit Sequence Generator

- We consider the design of a sequence generator to generate a sequence of 110101.
- The minimum number of flip-flops required to generate a sequence of length N is given by

$$N \leq 2^n - 1$$

  - The minimum value of n to satisfy the above condition is 3.

Design A 6-bit Sequence Generator

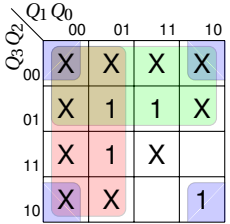
clk	Q_2	Q_1	Q_0
↑	1	1	0
↑	1	1	1
↑	0	1	1
↑	1	0	1
↑	0	1	0
↑	1	0	1

- `State 101 occurs twice!`
- Three flip-flops are not sufficient to generate the given sequence.

Design A 6-bit Sequence Generator

clk	Q_3	Q_2	Q_1	Q_0	Z
↑	1	1	0	1	1
↑	1	1	1	0	0
↑	0	1	1	1	1
↑	1	0	1	1	0
↑	0	1	0	1	1
↑	1	0	1	0	1
↑	1	1	0	1	1
↑	1	1	1	0	0
↑	0	1	1	1	1
↑	1	0	1	1	0

Design A 6-bit Sequence Generator



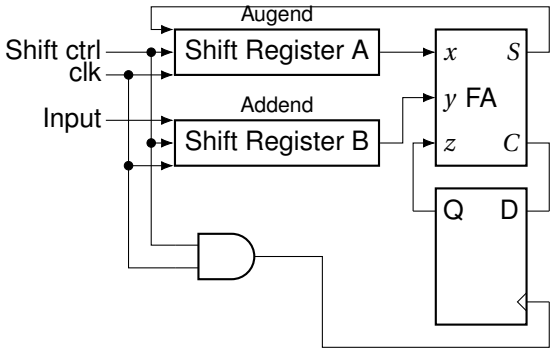
$$Z = Q_3' + Q_1' + Q_2' Q_0'$$

Draw the diagram by yourself!

Outline of This Lecture

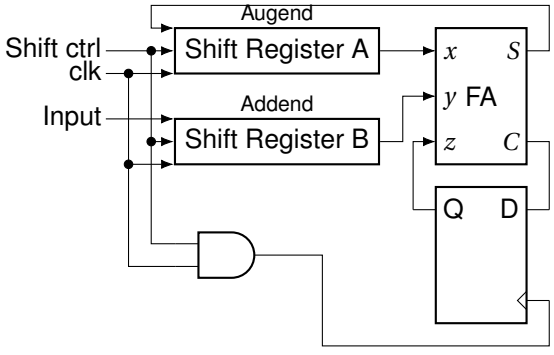
Serial Addition

- Operations in digital computers are usually done in parallel because that is a faster mode of operation.
- But serial operations have the advantage of requiring fewer hardware components.



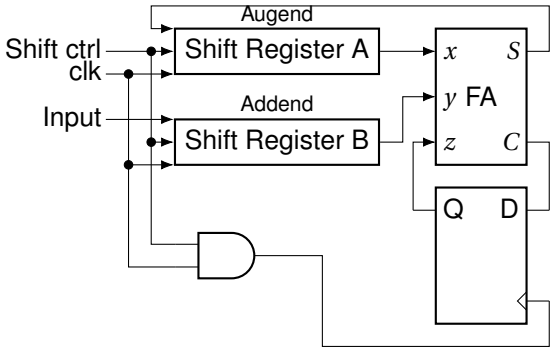
Serial Addition

- The two binary numbers to be added serially are stored in two shift registers.
- Beginning with the least significant pair of bits, the circuit adds one pair at a time through a single full-adder (FA) circuit.
- The carry out of the full adder is transferred to a D flip-flop, the output of which is then used as the carry input for the next pair of significant bits.



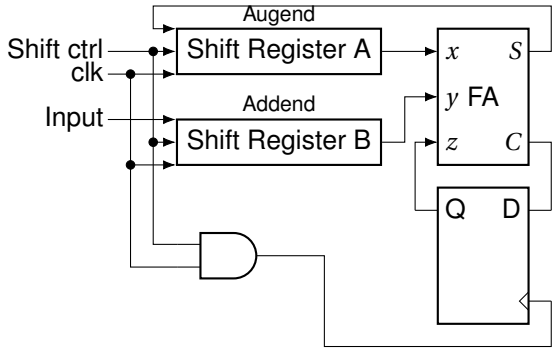
Serial Addition

- Initially, register A holds the augend, register B holds the addend, and the carry flip-flop is cleared to 0.
  - The outputs of A and B provide a pair of least significant bits for the full adder at x and y.
  - Output Q of the flip-flop provides the input carry at z.
- At the next clock pulse, both registers are shifted once to the right, the sum bit from S enters the leftmost flip-flop of A, and the output carry is transferred into flip-flop Q.



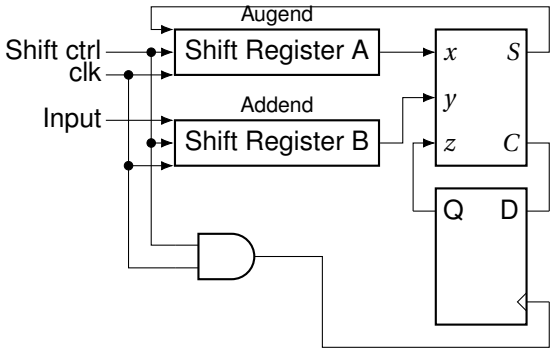
Serial Addition

- For each succeeding clock pulse, a new sum bit is transferred to A, a new carry is transferred to Q, and both registers are shifted once to the right.
- This process continues until the shift control is disabled.
- The addition is accomplished by passing each pair of bits together with the previous carry through a single full-adder circuit and transferring the sum, one bit at a time, into register A.



Serial Addition

- We note several differences on the serial adder with the parallel adder.
  - The parallel adder uses registers with a parallel load, whereas the serial adder uses shift registers.
  - The number of full-adder circuits in the parallel adder is equal to the number of bits in the binary numbers, whereas the serial adder requires only one full-adder circuit and a carry flip-flop.



Design A Serial Operation

- We will redesign the serial adder with the use of a state table.
- We assume that two shift registers are available to store the binary numbers to be added serially.
  - The serial outputs from the registers are designated by x and y.
- The sequential circuit has the two inputs, x and y, that provide a pair of significant bits, an output S that generates the sum bit, and flip-flop Q for storing the carry.
  - If a D flip-flop is used for Q, the circuit reduces to the previous one.

Design A Serial Operation

Present State Q (carry)	Inputs x	y	Next State Q (carry)	Output S	FF Inputs J_Q	K_Q
0	0	0	0	0	0	X
0	0	1	0	1	0	X
0	1	0	0	1	0	X
0	1	1	1	0	1	X
1	0	0	0	1	X	1
1	0	1	1	0	X	0
1	1	0	1	0	X	0
1	1	1	1	1	X	0

$$J_Q = xy,$$
$$K_Q = x'y' = (x+y)'$$
$$S = x \oplus y \oplus Q$$

Outline of This Lecture

Summary

- Various types of registers:
  - Serial-in serial-out shift register (串入串出移位寄存器).
  - Serial-in parallel-out shift register (串入并出移位寄存器).
  - Parallel-in serial-out shift register (并入串出移位寄存器).
  - Parallel-in parallel-out shift register (并入并出移位寄存器).
- Counters are a special type of registers.
- Registers can construct sequence generators together with combinational gates.
- Serial operations have the advantage of requiring fewer hardware components, e.g., serial addition.

Essential Reading

- Essential reading for this lecture: pages 255-266 of the textbook.
- Essential reading for next lecture: pages 266-283 of the textbook.

[1] M. M. Mano and M. Ciletti, *Digital design: with an introduction to the Verilog HDL*. Pearson, 2013