Lecture 12: Programmable Logic Devices

CS207: Digital Logic

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Acknowledgement

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M. M. Mano and M. Ciletti, *Digital design: with an introduction to the Verilog HDL*. Pearson, 2013

A. Saha and N. Manna, *Digital principles and logic design*. Jones & Bartlett Learning, 2009

Outline of This Lecture

Introduction to Memory

Random-access Memory

Memory Decoding

Read-only Memory

Programmable Logic Array

Outline of This Lecture

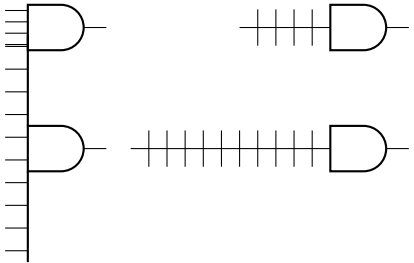
Memory

- A **memory** unit (存储单元) is a device to which binary information is transferred for storage (memory *write* operation) and from which information is retrieved when needed (memory *read* operation). [1]

- "A memory unit is a collection of cells capable of storing a large quantities of binary information." [1]
  - **Random-access memory** (RAM) (随机存取存储器)
    - Performs both read and write operations.
  - **Read-only memory** (ROM) (只读存储器)
    - Only read operation, information cannot be altered by writing.
    - Is a **programmable logic device** (PLD, 可编程逻辑器件).
    - Information storage in some fashion and embedded within hardware, called programming the device.

Programmable Logic Device (PLD, 可编程逻辑器件)

- PLD has many types, ROM is one. Others are
  - Programmable Array Logic (PAL, 可编程阵列逻辑) with programmable `AND` array and fixed `OR` array,
  - Programmable Logic Array (PLA, 可编程逻辑阵列) with programmable `AND` array and `OR` array, and the
  - Field-Programmable Gate Array (FPGA, 现场可编程门阵列).
- A PLD is an integrated circuit with internal logic gates connected through electronic paths similar to fuses.
- May have hundreds to millions of gates, thus requires a special gate symbology:



Left: conventional symbol; right: array logic symbol.

Outline of This Lecture

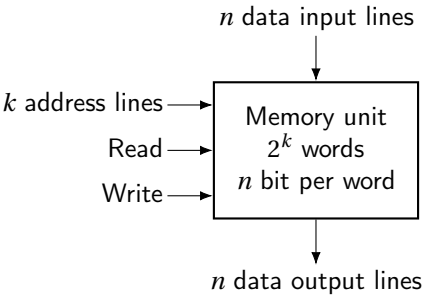
Random-access Memory (RAM)

- A memory unit is a collection of storage cells with associated circuits needed.
  - Information can be selectively retrieved from any of its internal locations.
  - Information retrieval time at any random location is the same, therefore **Random-access Memory**.

- Binary information stored are grouped in **words** (字).
  - Words are the unit of moving in and out of storage.
  - (Recall) 8 bits = 1 byte (字节).
  - Most computer memory has words multiple of 8 bits / 1 byte in length.

Random-access memory

- Communication achieved through:
  - Data input and output lines.
  - Address selection lines → specify the particular word chosen among the many available.
  - Control lines → specify the direction of transfer.
- To have n bits in a word,
  - n lines for input/output.
- To have m words,
  - k lines for address, such that $m \leq 2^k$.



Block diagram of a memory unit.

Random-access Memory

- Each word in the memory is assigned a unique **address** from 0 to $2^k - 1$.
- An internal decoder: k lines to 2^k addresses.
- On the right is 1K words of 16 bits. When a word is read or written, the memory operates on all 16 bits as a single unit.

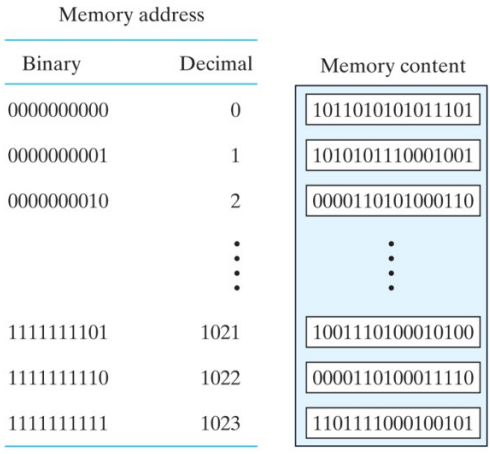
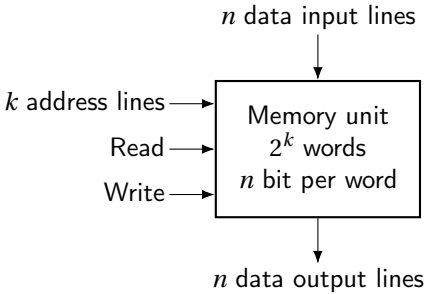


Figure: Contents of a 1024×16 memory. Figure 7.3 in [1].

Random-access Memory

- Two operations of RAM: read and write.
- Write
  - Apply binary address to address lines;
  - Apply data bits to data input lines;
  - Activate the write input
- Read
  - Apply binary address to address lines;
  - Activate the read output.



Random-access Memory

- Commercial memory components available in integrated-circuit chips:
  - One input selects the unit.
  - The other determines the operation.

Memory Enable (or “Chip Select”)	Read/Write	Memory Operation
0	X	None
1	0	Write to selected word
1	1	Read from selected word

Memory Description in HDL

- Memory is model;ed in the Verilog hardware description language (HDL) by an array of registers.
- It is declared with a `reg` keyword, using a two-dimensional array.
  - The first number in the array specifies the number of bits in a word (the word length) and
  - the second gives the number of words in memory (memory depth).
- Example: a memory of 1,024 words with 16 bits per word (a two-dimensional array of 1,024 registers, each containing 16 bits).

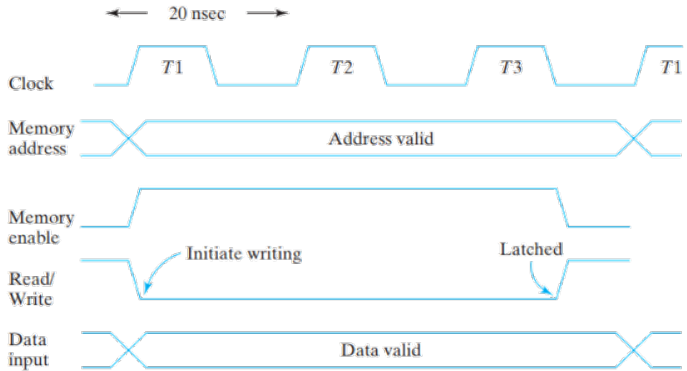
```
reg[15:  0] memword [0:  1023];
```

Random-access Memory

- Memory unit operation is controlled by an external device, e.g., central processing unit (CPU), synchronised by its own clock.
  - Memory does not employ an internal clock.
  - **Access time**: time required to select a word and read it.
  - **Cycle time**: complete a write operation.
  - CPU provides memory control signals to synchronise its internal clocked operations with the read and write operations of memory.
    - The access and cycle time within a time equal to a fixed number of CPU clock cycles.

Random-access Memory

- CPU: 50MHz – one clock cycle = 20ns
- Memory: access time = cycle time = 50ns
  - These times not always equal.



Random-access Memory

- Integrated circuit RAM units available in two operating modes:
  - Static RAM: essentially latches, available as long as powered.
    - Easier to use, has shorter read/write cycles.
  - Dynamic RAM: information stored in the form of electric charges (电荷) on capacitors (电容) provided inside the chip, discharge over time.
    - Capacitors periodically recharged by refreshing the memory. Refreshing is done by cycling through the words every few milliseconds to restore the decaying charge.
    - Reduced power consumption and larger storage capacity
- Memory units that lose stored information when power is turned off are **volatile** (不稳定的).
- Non-volatile memories retained information with magnetic components (磁性元件).
  - Data represented by direction of magnetisation (retained after power is turned off).

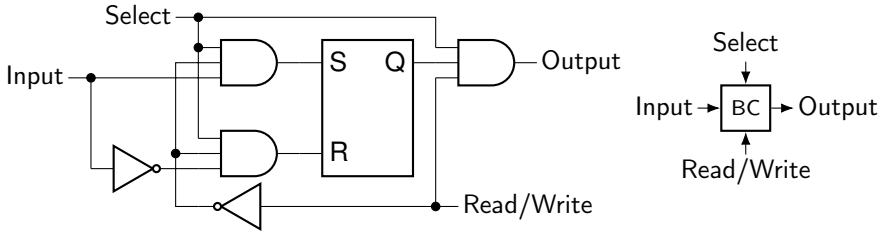
Nonvolatile Memory

- Non-volatile memories retained information with magnetic components (磁性元件).
  - Data represented by direction of magnetisation (retained after power is turned off).
- A nonvolatile memory enables digital computers to store programs that will be needed again after the computer is turned on.
- ROM is a nonvolatile memory. Programs and data that cannot be altered are stored in ROM, while other large programs are maintained on magnetic disks.
- The latter programs are transferred into the computer RAM as needed.
- Before the power is turned off, the binary information from the computer RAM is transferred to the disk so that the information will be retained.

Outline of This Lecture

Memory Decoding

- To require storage components in a memory unit, a **decoding circuit** is required:
  - Select memory word specified by input address.
- m words with n bits each consist of $m \times n$ binary storage cells as the basic building blocks.
- Example: A binary storage cell modelled by an SR latch with external gates to form a D latch.
  - Actual cells are circuits with 4 to 6 transistors.
  - Convenient to model it with logic symbols.



Memory cell. Left: logic diagram; right: block diagram.

Memory Decoding

- A binary storage cell must be very small.
  - Pack as many cells as possible in the small IC chip.

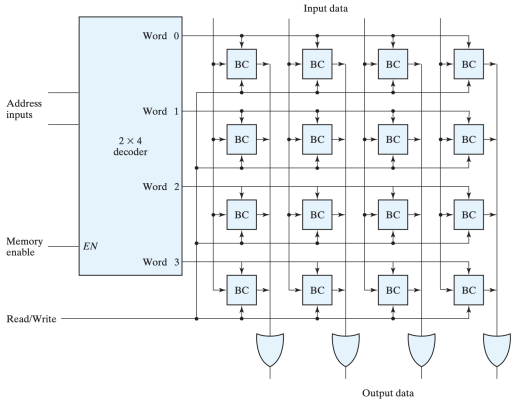
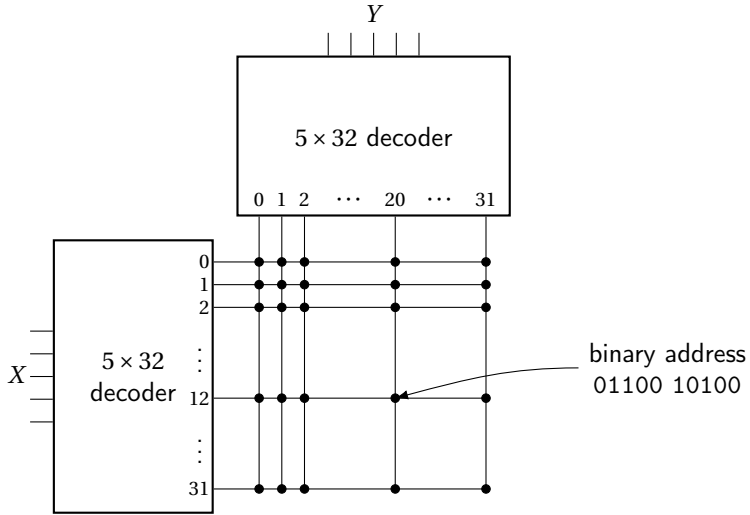


Figure: Diagram of a 4×4 RAM. Figure 7.6 in [1]. "BC" refers to binary cell.

Memory Decoding

- Commercial RAMs have a capacity of thousands of words, each 1 to 64 bits.
- $k-2^k$ decoder requires 2^k `AND` gates with k inputs.
  - Can be reduced by employing two decoders: **coincident decoding**.
  - Two $k/2$-input decoders: one decoder performs row selection, the other column selection.

Memory Decoding

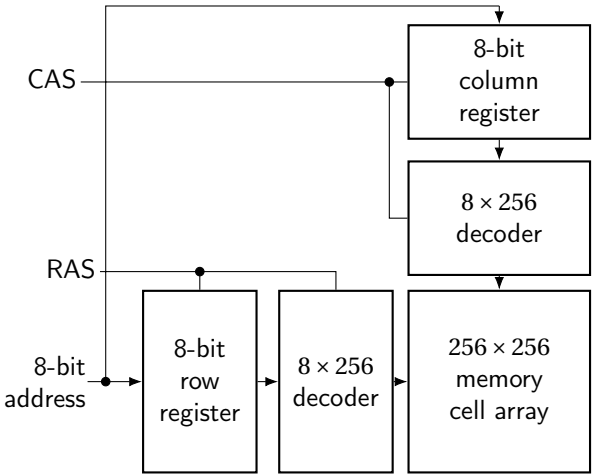


Two-dimensional decoding structure for a 1K-word memory. With a single 10×1024 decoder, we would need 1,024 AND gates with 10 inputs in each. In the two-decoder case, we need 64 AND gates with 5 inputs in each.

Memory Decoding

- DRAM compared to SRAM:
  - Four times the density of SRAM.
  - The cost per bit of DRAM storage is three to four times less than that of SRAM storage.
  - Preferred technology for large memories.
- Address decoding for DRAM is in two-dimensional array, larger memories have multiple arrays.
- Address multiplexing is used to reduce the number of pins in the IC package.
  - The same set of pins used for row and column selection.

Memory Decoding

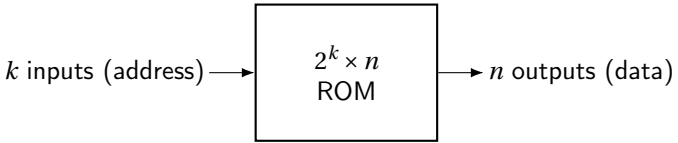


Row address strobe (RAS): enables the 8-bit row register.
Column address strobe (CAS): enables the 8-bit column register.

Outline of This Lecture

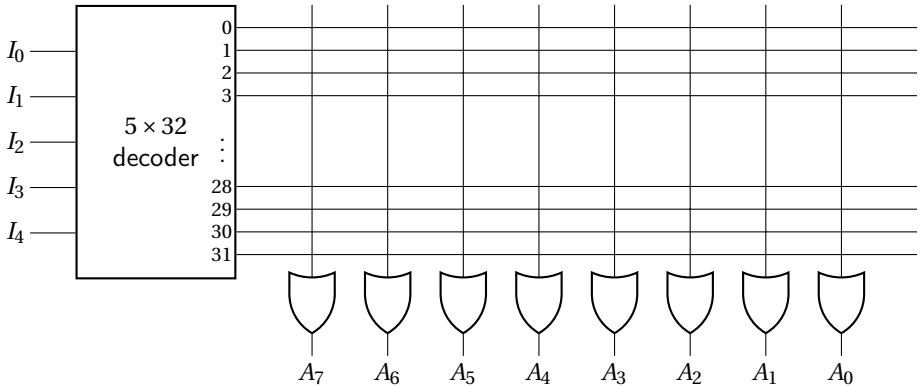
Read-only Memory

- ROM is a memory device in which permanent binary information is stored.
- Once the pattern is established, stays within the unit even when power is turned off.



Read-only Memory

- Consider a 32×8 ROM:
- Five input lines for address.
- 32 input connections and 8 `OR` gates = 256 internal connections.



Read-only Memory

- These $32 * 8 = 256$ intersections are programmable:
  - Logically equivalent to a switch that can be closed (connected) or open (disconnected).
  - Also called **crosspoint**s.
- One of the simplest technology employs a fuse.
  - Normally connects the two points.
  - Opened or “blown” by high-voltage pulse into the fuse.

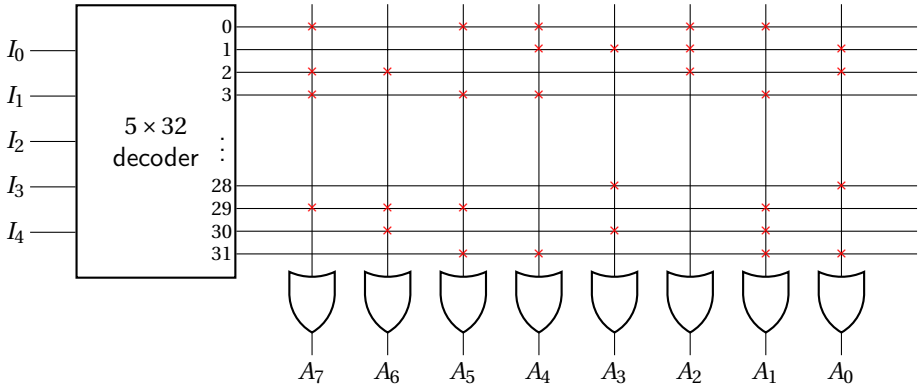
Read-only Memory

- Internal binary storage of a ROM specified by a truth table.
  - Each address stores a word of 8 bits.

Inputs					Outputs							
I_4	I_3	I_2	I_1	I_0	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0
0	0	0	0	0	1	0	1	1	0	1	1	0
0	0	0	0	1	0	0	0	1	1	1	0	1
0	0	0	1	0	1	1	0	0	0	1	0	1
0	0	0	1	1	1	0	1	1	0	0	1	0
		...						...				
1	1	1	0	0	0	0	0	0	1	0	0	1
1	1	1	0	1	1	1	1	0	0	0	1	0
1	1	1	1	0	0	1	0	0	1	0	1	0
1	1	1	1	1	0	0	1	1	0	0	1	1

Read-only Memory

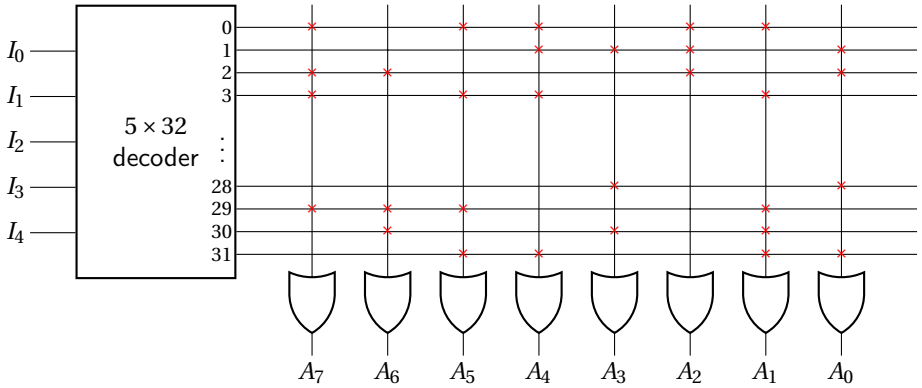
- Program the ROM: blows fuse links in accordance with the truth table
  - 10110110 in the first row.



X denotes a temporary connection.

Read-only Memory

- Combinational circuit
  - (Recall) Decoder: k input = 2^k minterms.
  - By choosing connections for those minterms.
  - For example, eight functions of five binary inputs.



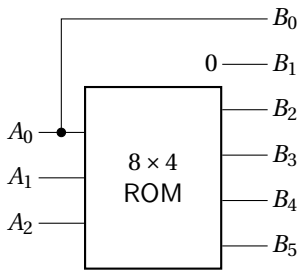
Example

- Design a combinational circuit using a ROM. The circuit accepts a three-bit number and outputs a binary number equal to the square of the input number.
  - $B_0 \equiv A_0$, $B_1 \equiv 0$, no need to generate.

Inputs			Outputs						Decimal
A_2	A_1	A_0	B_5	B_4	B_3	B_2	B_1	B_0	
0	0	0	0	0	0	0	0	0	0
0	0	1	0	0	0	0	0	1	1
0	1	0	0	0	0	1	0	0	4
0	1	1	0	0	1	0	0	1	9
1	0	0	0	1	0	0	0	0	16
1	0	1	0	1	1	0	0	1	25
1	1	0	1	0	0	1	0	0	36
1	1	1	1	1	0	0	0	1	49

Example

- 3 inputs, 4 outputs: 8×4 ROM.



Inputs			Outputs			
A_2	A_1	A_0	B_5	B_4	B_3	B_2
0	0	0	0	0	0	0
0	0	1	0	0	0	0
0	1	0	0	0	0	1
0	1	1	0	0	1	0
1	0	0	0	1	0	0
1	0	1	0	1	1	0
1	1	0	1	0	0	1
1	1	1	1	1	0	0

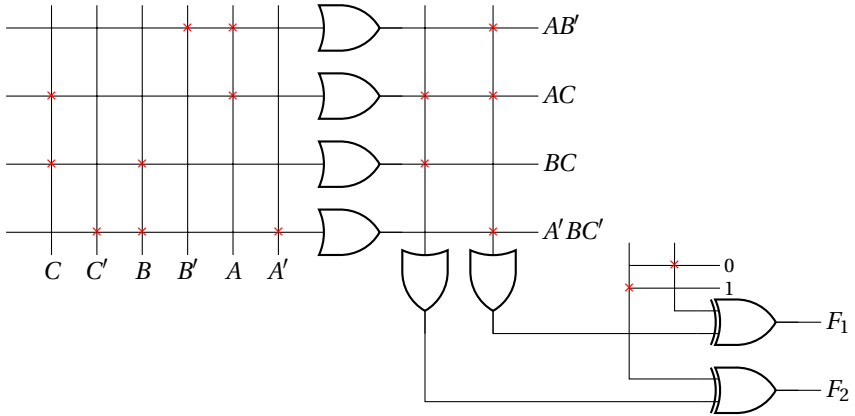
Read-only Memory

- A **programmable ROM** (PROM) is a kind of combinational programmable logic device (PLD) with fixed `AND` array (decoder) and programmable `OR` array.
- Others are programmable array logic (PAL) with programmable `AND` array and fixed `OR` array,
- and programmable logic array (PLA) with programmable `AND` and `OR` arrays.

Outline of This Lecture

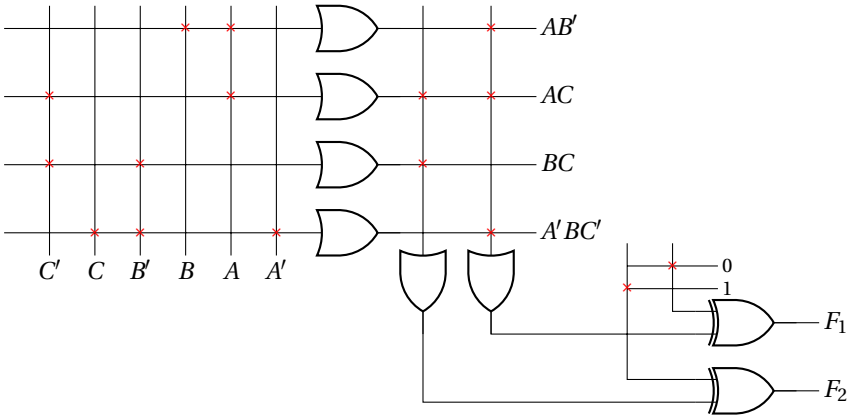
Programmable Logic Array

- Similar to PROM, but no full decoding of variables, i.e., not all minterms.
- Decoder replaced by an array of `AND` gates.



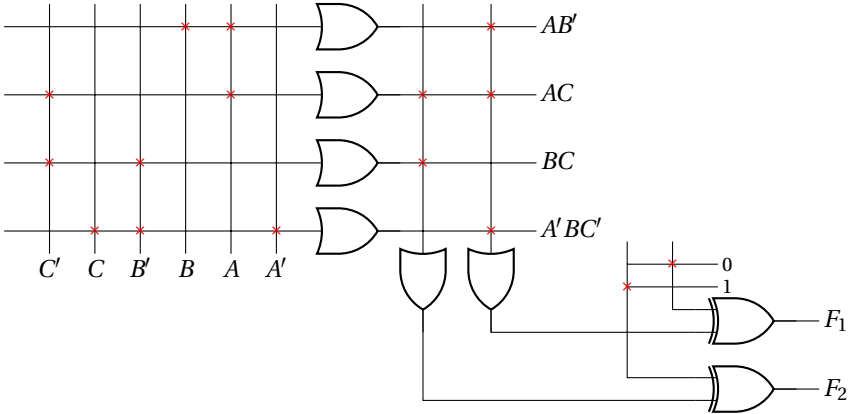
Programmable Logic Array

- `XOR` receives logic `0` or `1`: complement on `1`.



Programmable Logic Array

- $F_1 = AB' + AC + A'BC'$
- $F_2 = (AC + BC)'$



Programmable Logic Array

- $F_1 = AB' + AC + A'BC'$
- $F_2 = (AC + BC)'$
- Fuse map can be specified in a tabular form.

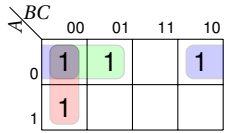
		Inputs			Outputs (T)	(C)
	Product Term	A	B	C	F_1	F_2
AB'	1	1	0	–	1	–
AC	2	1	–	1	1	1
BC	3	–	1	1	–	1
$A'BC'$	4	0	1	0	1	–

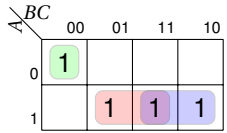
Programmable Logic Array

- Size of a PLA is specified by the number of inputs, product terms, and outputs.
  - Typically have 16 inputs, 48 product terms, 8 outputs.
- For n inputs, k products, m outputs:
  - n buffer-inverter gates;
  - k `AND` gates;
  - m `OR` gates, and m `XOR` gates;
  - $2n \times k$ connections between inputs and `AND` array;
  - $k \times m$ connections between `AND` and `OR` arrays;
  - m connections associated with `XOR` gates.

Example

- Implement the following two Boolean functions with a PLA:
  - $F_1(A,B,C) = \sum(0,1,2,4) = (AB + AC + BC)'$.
  - $F_2(A,B,C) = \sum(0,5,6,7) = AB + AC + A'B'C'$.





	Product Term	Inputs A	B	C	Outputs (T) F_1	(C) F_2
AB	1	1	1	–	1	1
AC	1	1	–	1	1	1
BC	1	–	1	1	1	–
$A'B'C'$	1	0	0	0	0	1

Essential Reading

- Essential reading for this lecture: pages 299-324 of the textbook.

[1] M. M. Mano and M. Ciletti, *Digital design: with an introduction to the Verilog HDL*. Pearson, 2013