Course Overview

CS207: Digital Logic

Jialin Liu

Department of Computer Science and Engineering
Southern University of Science and Technology (SUSTech)

9 September 2022

Basic Info of This Course

- **Course Name:** Digital Logic (CS207)
- **Credits:** 3 (32 lecture hours + 32 lab hours)
- **Teaching Method:** 100 mins' lecture + 100 mins' lab every Friday
- **Language:** English
- **Course on Sakai:** *CS207-02-fall2022* for both CS207-02-1 and CS207-02-2
  `https://sakai.sustech.edu.cn/portal/directtool/61e1db25-a1a0-4ad4-b519-82e4a24179bc/`

Instructors

- **Lecture Instructor (CS207-02):**
  - CS207-02 (Friday 3-4): Dr. Jialin Liu (*liujl@sustech.edu.cn*)
    - Office: South-514, Engineering Building (工学院南楼514)
    - Office hour: 10am–12pm (2 hours), Monday
- **Lab Instructors:**
  - CS207-02-2 (Friday 5-6): Mrs. Wei Wang (*wangw6@sustech.edu.cn*)
  - CS207-02-1 (Friday 7-8): Dr. Jialin Liu (*liujl@sustech.edu.cn*)
- **Student assistants:**
  - Friday 5-6: Linkai Peng (*11912922@mail.sustech.edu.cn*)
  - Friday 5-6: Jiaqin Yan (*12010320@mail.sustech.edu.cn*)
  - Friday 7-8: Siyu Chen (*12232405@mail.sustech.edu.cn*)
  - Friday 7-8: Qinan Chen (*12232428@sustech.edu.cn*)

Course Description

- This is a foundational course in digital design that aims to provide an understanding of the fundamental concepts, circuits in digital design, and expose students to the mainstream approaches and technologies used in digital design.
- It is the basis for digital computing and provides a fundamental understanding on how circuits and hardware communicate within a computer.
  - Core logical operations and elementary methods to design logic circuits to achieve a desired function.
  - Fundamentals of combinational and sequential circuits.
  - Hands-on experimentation knowledge of the digital design process using HDLs.

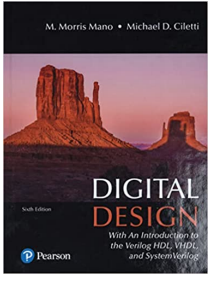
Learning Outcomes

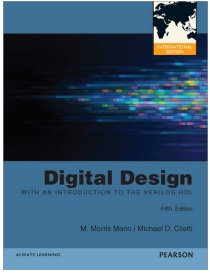
Upon finishing this course, students are expected to:

- understand fundamental logic operations (e.g., AND, OR, NOT, NAND, NOR, etc.), schematic symbols and diagrams, and truth tables;
- optimise Boolean functions and algebra with Karnaugh maps method;
- design combinational logic circuits with Boolean functions or truth tables, and design sequential logic circuits with timing diagrams;
- understand the theory, usage, and design principle of registers;
- understand how to implement practical logic functions with digital logic theory.

Recommended Literature for This Course

- M. Morris Mano and Michael Ciletti. 2017. *Digital Design: With an Introduction to the Verilog HDL, VHDL, and SystemVerilog* (5th. ed.). Pearson.
- Arijit Saha and Nilotpal Manna. 2007. *Digital Principles and Logic Design* (5th. ed.). Jones and Bartlett Publishers, Inc., USA.





PDF available on Sakai !

Tentative Course Plan

- Week 1 (Sept. 9): Lecture 1 - Binary Numbers
- Week 2 (Sept. 16): Lecture 2 - Boolean Algebra and Logic Gates
- Week 3 (Sept. 23): Lecture 3 - Gate-Level Minimisation
- Week 4 (Sept. 30): Lecture 4 - Two-Level Implementation
- ——— (Oct. 9): Lecture 5 - Combinational Logic & Assignment 1 Analysis
- Week 5 (Oct. 14): Lecture 6 - Combinational Logic (cont'd)
- Week 6 (Oct. 21): Lecture 7 - Latches and Flip-flops
- Week 7 (Oct. 28): Lecture 8 - Synchronous Sequential Logic & Assignment 2 Analysis
- Week 8 (Nov. 4): Lecture 9 - Synchronous Sequential Logic (cont'd)
- Week 9 (Nov. 11): Mid-term Assessment (Lectures 1–7)

Tentative Course Plan (continued)

- Week 10 (Nov. 18): TBD (University Sports Day)
- Week 11 (Nov. 25): Lecture 10 - Arithmetic Circuits
- Week 12 (Dec. 2): Lecture 11 - Registers & Assignment 3 Analysis
- Week 13 (Dec. 9): Lecture 12 - Registers (cont'd) and Counters
- Week 14 (Dec. 16): Lecture 13 - Counters (cont'd)
- Week 14 or 15: Project Inspection #1
- Week 15 (Dec. 23): Lecture 14 - Programmable Logic Devices & Assignment 4 Analysis
- Week 16: Project Inspection #2
- Week 16 (Dec. 30): Revision
- Week 17: Exam week
- Week 18: Exam week

About Labs

- Topic: related to the lecture of the same week.
- Hands-on sessions (*Verilog*, *Xilinx Vivado*, *FPGA boards*).
- Individual lab works + group project.
- Lab works help you succeed in projects.
- If you don't come, never ask us questions that we've answered / presented in labs.

Course Assessment

- **Attendance / Quiz in lectures (5%)**
- **Attendance / Quiz in labs (5%)**
- **Assignments (20%)**: 5% * 4 assignments
  - Individual work
  - **Late submission will be marked as 0.** No late submission is allowed without formal approval from the lecturer before deadline.
  - No re-submission is allowed for student reasons, e.g., corrupted file uploaded.
  - Discussions are encouraged, but **no plagiarism**.
- **Project (20%)**
  - Group work (evaluated on program + report + demo in labs).
  - **Late submission will be marked as 0**.
  - Discussions are encouraged, but **no plagiarism**.
- **Open-book mid-term assessment (10%)** – Nov. 11th
- **Close-book final exam (40%)**

Regrade Policy

- You have **three days** after the day each assignment or examination is returned to you to ask for a grade change.
- Grades will be changed only during that period of time and only if:
  - we added up your score wrong, or
  - we made an error in grading a particular problem.
- At the end of the term, we will not argue about grades on the assignment or on the examinations.
- Request to regrade will lead to **a complete regrade on all questions** in the assignment or examination. **Final grades may increase or decrease.**

Important Notes

- If you do not attend a lecture/lab, we will assume that you know all the contents of that lecture/lab and information given at the lecture/lab. We will not repeat any content and information about that lecture/lab to you outside the lecture.
- **Learning to learn is absolutely essential.**
- **Professional Behaviours**
  - Be polite and cooperative to others.
  - Respect each other.
  - Follow rules and regulations. There will be **no** exceptions.
  - Plagiarism or unethical behaviours will be punished.
  - Do not play mobile phone or talk to each other during classes.