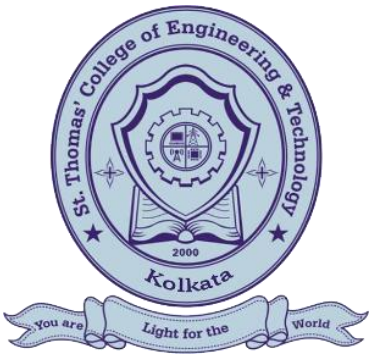


Academic Year: 2019 -2020

Department

of

Electronics &Communication Engineering

St. Thomas' College of Engineering & Technology

Laboratory Report on

Analog& Digital ElectronicsLab

Code:ESC 391

Name: _____Mayukh Barman Ray_____

Year:__2nd__ Stream: *Computer Science & Engineering*

Semester: ___3rd___Class Roll No: ___04____

Group: __1-31(Even)_____

University Roll No.: 12200119061

General Information

Course Name	Analog& Digital ElectronicsLab	**Semester**	III
Course Code	ESC 391	**Year with stream**	2NDyearCS
Course Credit	2	**Session**	2019-2020
Faculty Instructor/s	SMC	**Class hours and total class load**	4hrs
Technical Assistant/s		**Laboratory**	ElectronicsLab. [Room No. 106]

Course objectives	This laboratory courses on hands-on experiments are for undergraduate Engineering students studying the course of Analog &Digital ElectronicsLab. After completion of this course , the students will be able to perform various experiments to supplement their theoretical understanding ofanalog& digital electronics.

Course Outcome:

After completion of the course student will be able to

CO	CO Statements	Bloom's Level
C.1	**Analyze** the truth table of basic combinational circuits and sequential circuits.	**Analyze**
C.2	**Apply** the design knowledge of flip-flops to realise them with logic gates.	**Apply**
C.3	**Apply** the knowledge to **design** Shift Registers using J-K / D Flip Flop.	**Create**
C.4	Able to **Analyze** the timing diagram of different sequential logic diagram.	**Analyze**
C.5	**Analyze** the frequency of oscillation condition of an electrical circuit.	**Analyze**
C.6	**Design** of a Schmitt Trigger using 555 timer & realization of the in input /output waveform.	**Create**

CO--PO/PSO/BLOOM'S LEVEL matrix of the course:

CO	PO												PSO 1	PSO 2
	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12		
CO1														
CO2														
CO3														
CO4														
CO5														
CO6														

Recommended books	1. Sedra& Smith-Microelectronic Circuits- Oxford UP 2. Boylested&Nashelsky- Electronic Devices - Pearson/PHI 3. Millman&Halkias – Integrated El;ectronics, McGraw Hill. 4. A.Anand Kumar, Fundamentals of Digital Circuits- PHI 5. D.RayChaudhuri- Digital Circuits-Vol-I & II, 2/e- Platinum 6. H.Taub&D.Shilling, Digital Integrated Electronics- McGraw Hill

Grading: Grading to be done as per university rule.

List of Experiments

Expt. No.	Name of Experiment	Page No.	Date of Expt.	Signature	Grade awarded
1	Design a Full Adder using basic gates and verify its output / Design a Full Subtractor circuit using basic gates and verify its output.	4-11	15.09.20 & 22.09.20		
2	Construction of Decoder & Multiplexer circuits using logic gates.	12-17	29.09.20		
3	Realization of RS / JK / D flip flops using logic gates.				
4	Design of Shift Register using J-K / D Flip Flop.				
5	Realization of Synchronous Up/Down counter.				
6	Design a Phase-Shift Oscillator.				
7	Design of a Schmitt Trigger using 555 timer.				

EXPERIMENT NO: 2

Title:Design of Decoder& Multiplexer circuits using logic gates.

Objective: To construct a 2 to 4 decoder & 4:1 multiplexer using logic gates.

The Experiment Covers the Course Outcome:	**Analyze** the truth table of basic combinational circuits and sequential circuits.
Bloom's Cognitive Domain:	**Analyze**

Function Table:

FOR 2 TO 4 DECODER

Enable	INPUTs		OUTPUTs			
E	A (MSB)	B (LSB)	D_0	D_1	D_2	D_3
1	0	0	1	0	0	0
1	0	1	0	1	0	0
1	1	0	0	0	1	0
1	1	1	0	0	0	1
0	x	x	0	0	0	0

BOOLEAN EXPRESSION:

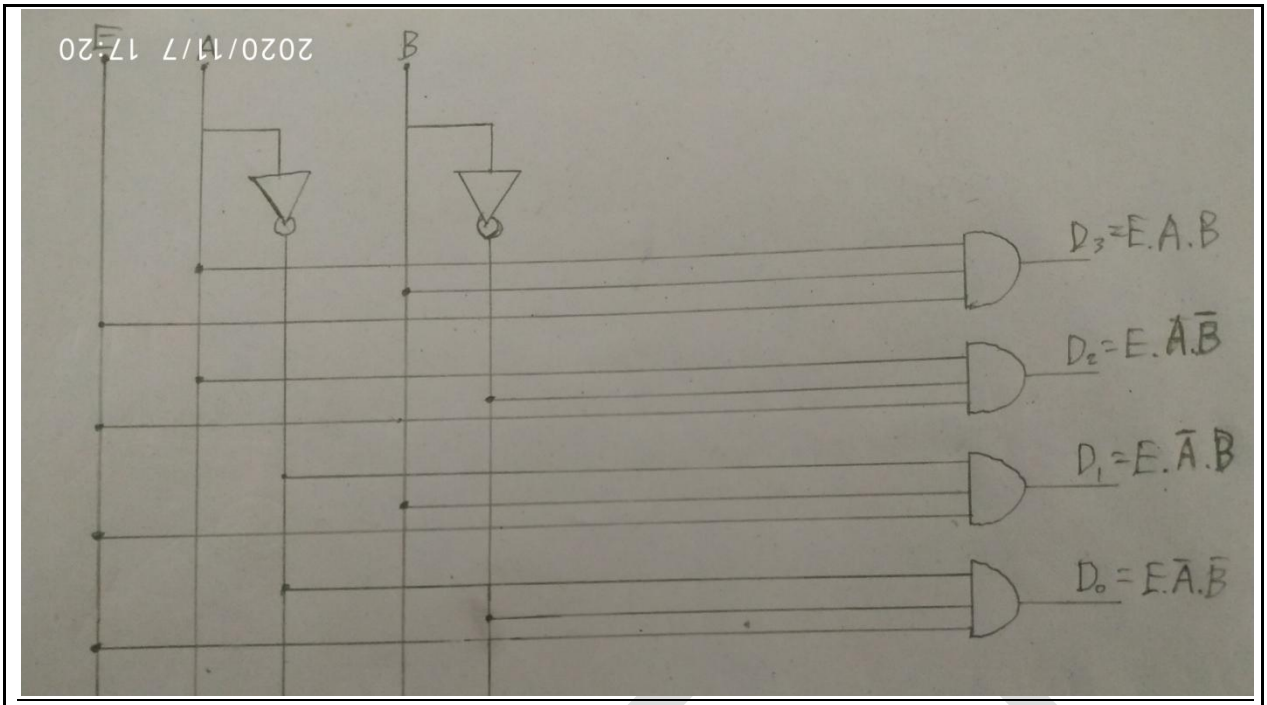
D_0 = E.A'.B'

D_1 = E.A'.B

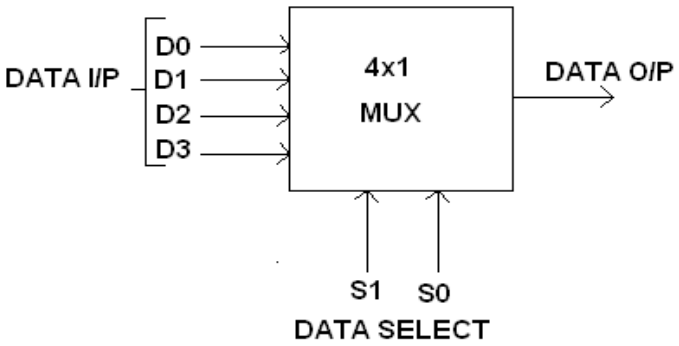
D_2 = E.A.B'

D_3 = E.A.B

LOGIC CIRCUIT DIAGRAM FOR DECODER :



BLOCK DIAGRAM FOR 4:1 MULTIPLEXER:



FUNCTION TABLE:

S1	S0	INPUTS Y
0	0	D0 → D0 S1' S0'
0	1	D1 → D1 S1' S0
1	0	D2 → D2 S1 S0'
1	1	D3 → D3 S1 S0

BOOLEAN EXPRESSION:

Y = D0 S1' S0' + D1 S1' S0 + D2 S1 S0' + D3 S1 S0

CIRCUIT DIAGRAM FOR MULTIPLEXER:

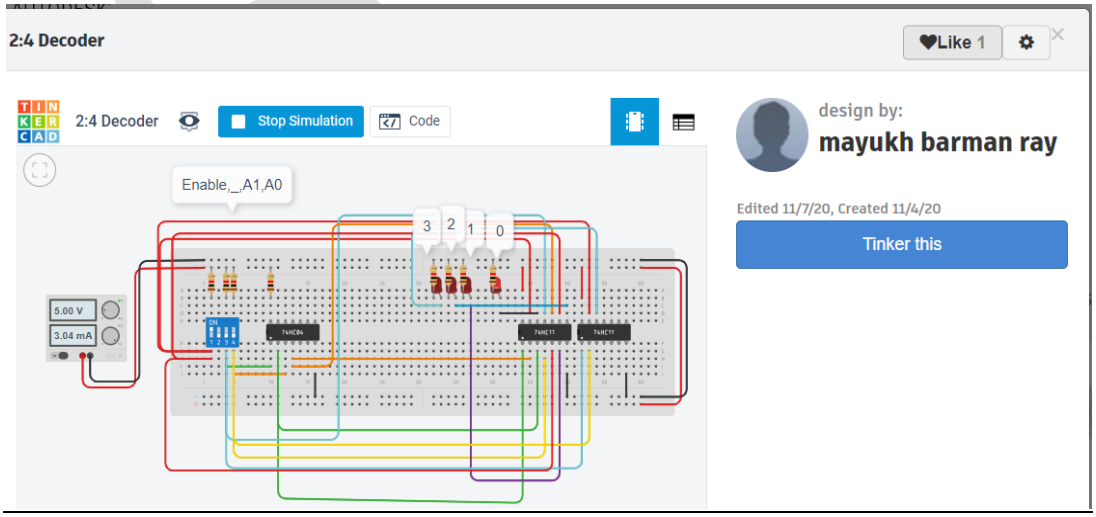
APPARATUS: 1. Trainer Kit.

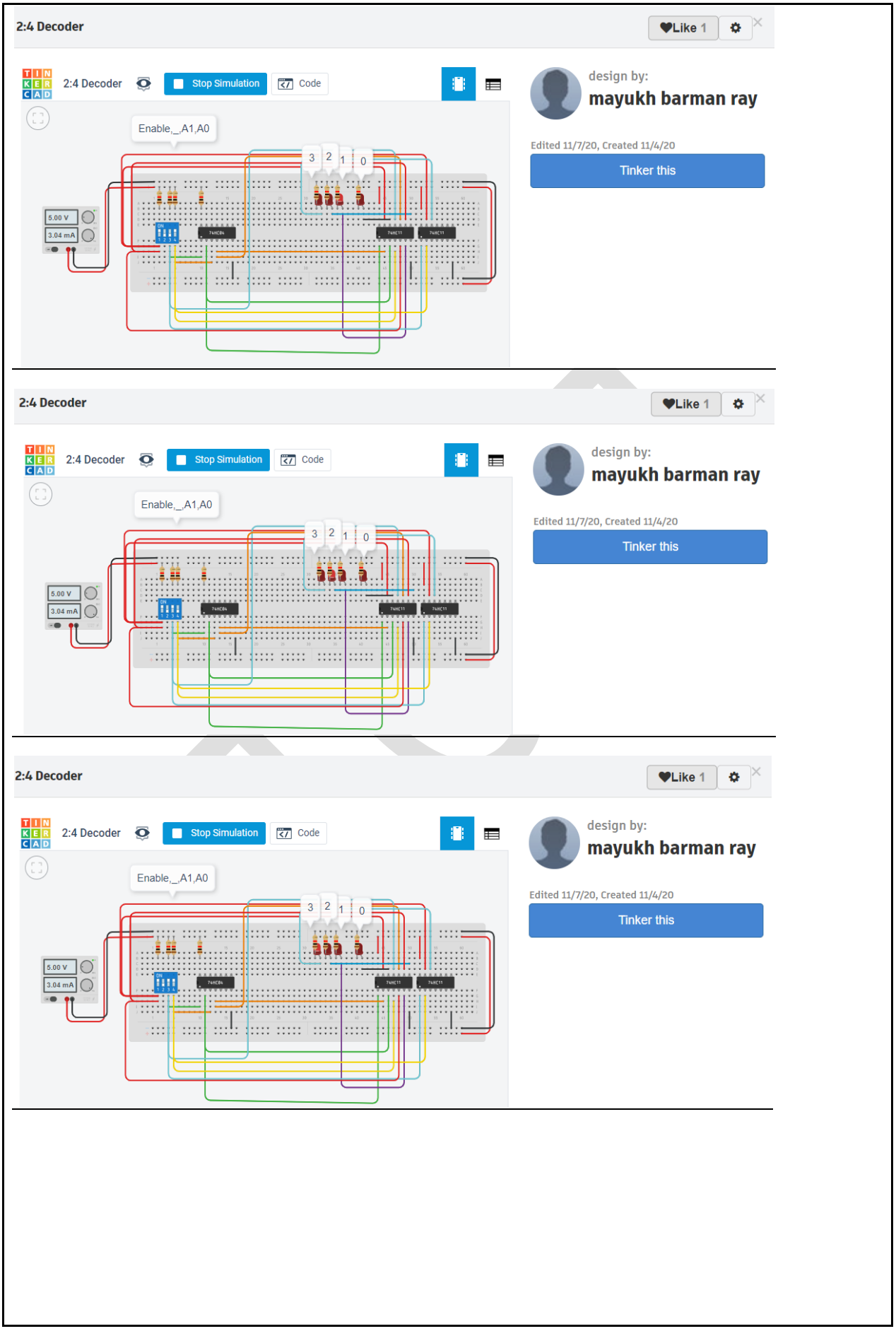
COMPONENTS:

Complete the following table as per circuit diagram and collect the component from Laboratory.

Sl.no	IC no.	IC Description	Qty
1	74HC04	Hex Inverter	1
2	74HC11	Triple 3-Input AND gate	2

OBSERVATION: The decoder circuit made in this experiment verified the above truth table.




2:4 Decoder
Like 1
2:4 Decoder
Stop Simulation
Code
Enable,_,A1,A0
3
2
1
0
5.00 V
3.04 mA
design by:
mayukh barman ray
Edited 11/7/20, Created 11/4/20
Tinker this
2:4 Decoder
Like 1
2:4 Decoder
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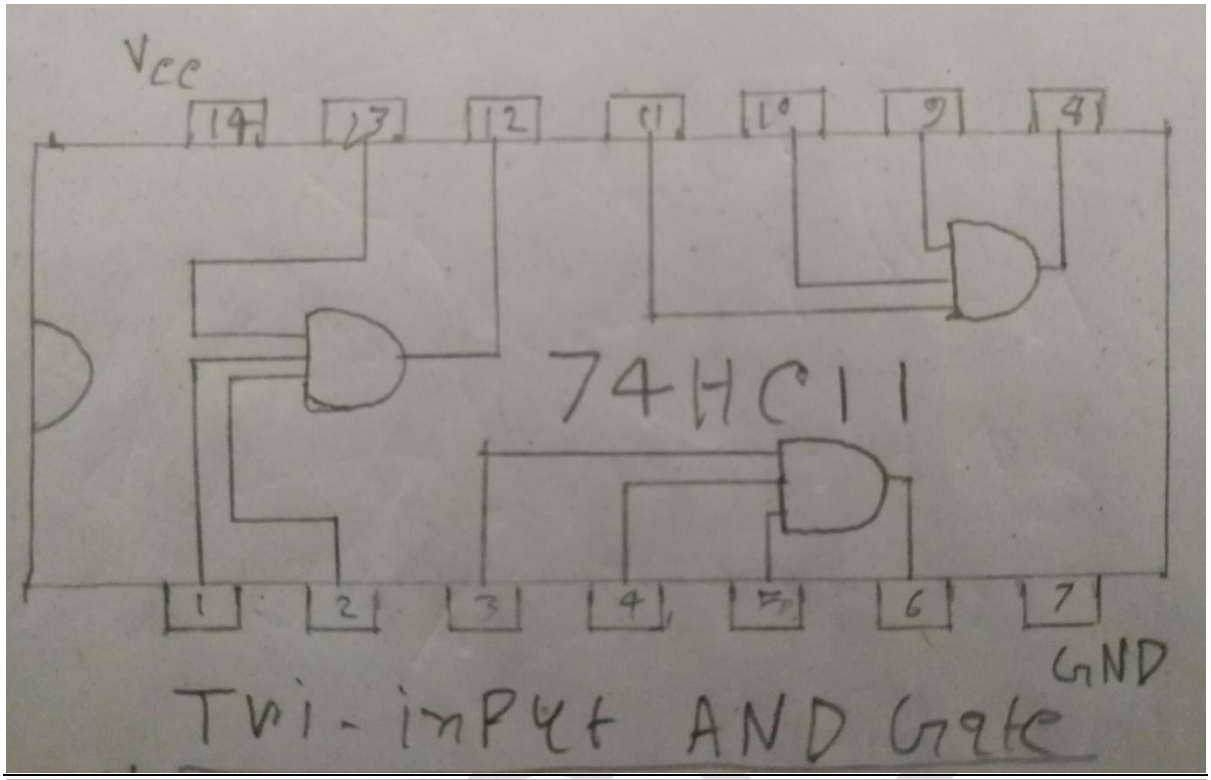
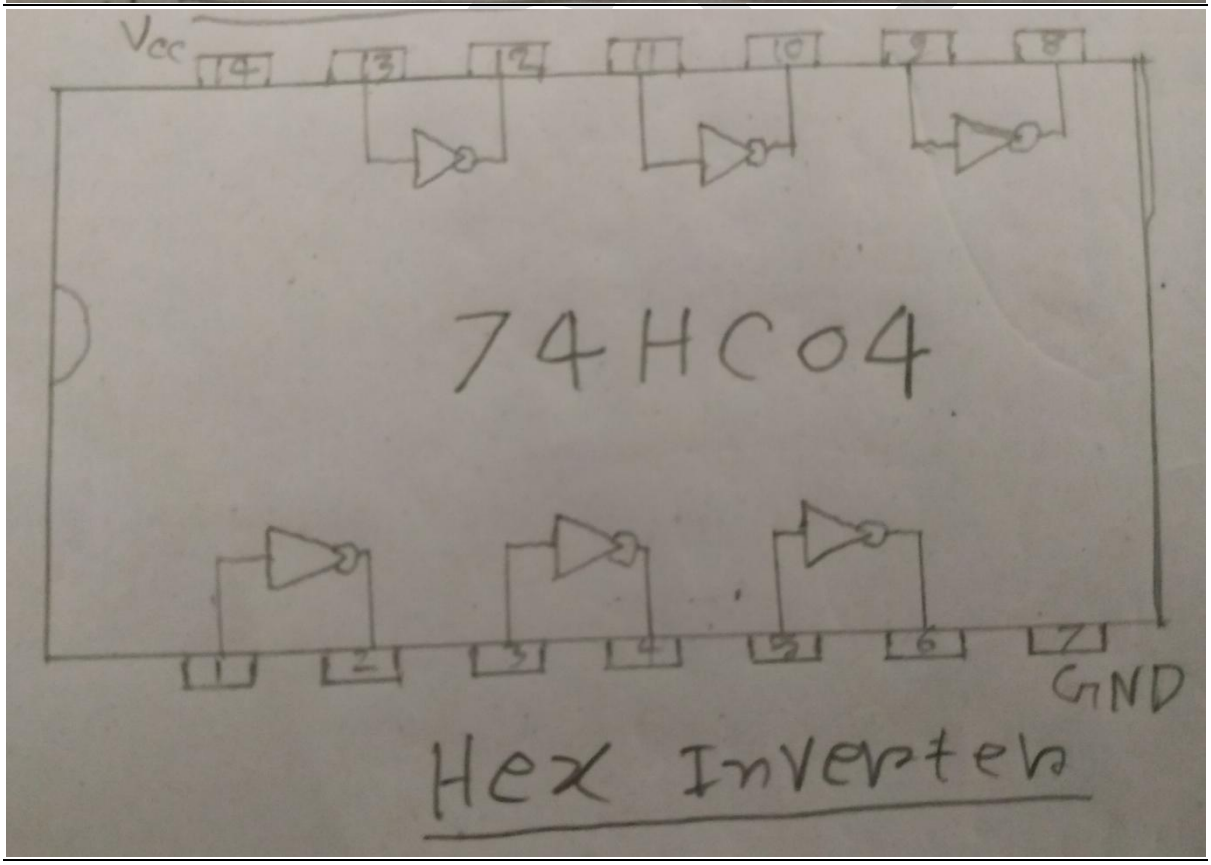
Tinker this

Discussion:-


Vcc
14
13
12
11
10
9
8
74HC11
1
2
3
4
5
6
7
GND
Two-input AND Gate


Vcc
14
13
12
11
10
9
8
74HC04
1
2
3
4
5
6
7
GND
Hex Inverter

Questionnaires:

1. Design Full adder using 3 to 8 decoder.
2. Design Full subtractor using 3 to 8 decoder.
3. Design and implement F(A,B,C)=∑m(1,2,4,7) using suitable MUX.
4. Design and implement F(A,B,C) = $\sum_m$(1,2,4,7) using suitable Decoder.

Teacher's signature with date	