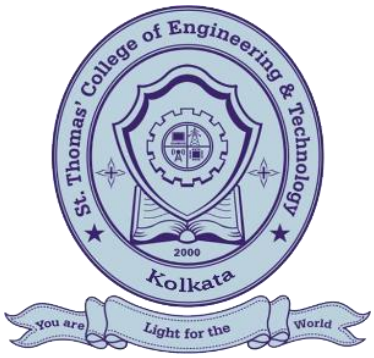


Academic Year: 2019 -2020

Department

of

Electronics &Communication Engineering

St. Thomas' College of Engineering & Technology

Laboratory Report on

Analog& Digital ElectronicsLab

Code:ESC 391

Name: Mayukh Barman Ray

Year: 2nd Stream: *Computer Science & Engineering*

Semester: 3rd Class Roll No: 04

Group: _____

University Roll No.: 12200119061

General Information

Course Name	Analog& Digital ElectronicsLab	**Semester**	III
Course Code	ESC 391	**Year with stream**	2NDyearCS
Course Credit	2	**Session**	2019-2020
Faculty Instructor/s	SMC	**Class hours and total class load**	4hrs
Technical Assistant/s		**Laboratory**	ElectronicsLab. [Room No. 106]

Course objectives	This laboratory courses on hands-on experiments are for undergraduate Engineering students studying the course of Analog &Digital ElectronicsLab. After completion of this course , the students will be able to perform various experiments to supplement their theoretical understanding of analog & digital electronics.

Course Outcome:

After completion of the course student will be able to

CO	CO Statements	Bloom's Level
C.1	**Analyze** the truth table of basic combinational circuits and sequential circuits.	**Analyze**
C.2	**Apply** the design knowledge of flip-flops to realise them with logic gates.	**Apply**
C.3	**Apply** the knowledge to **design** Shift Registers using J-K / D Flip Flop.	**Create**
C.4	Able to **Analyze** the timing diagram of different sequential logic diagram.	**Analyze**
C.5	**Analyze** the frequency of oscillation condition of an electrical circuit.	**Analyze**
C.6	**Design** of a Schmitt Trigger using 555 timer & realization of the in input /output waveform.	**Create**

CO--PO/PSO/BLOOM'S LEVEL matrix of the course:

CO	PO												PSO 1	PSO 2
	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12		
CO1														
CO2														
CO3														
CO4														
CO5														
CO6														

Recommended books	1. Sedra& Smith-Microelectronic Circuits- Oxford UP 2. Boylested&Nashelsky- Electronic Devices - Pearson/PHI 3. Millman&Halkias – Integrated El;ectronics, McGraw Hill. 4. A.Anand Kumar, Fundamentals of Digital Circuits- PHI 5. D.RayChaudhuri- Digital Circuits-Vol-I & II, 2/e- Platinum 6. H.Taub&D.Shilling, Digital Integrated Electronics- McGraw Hill

Grading: Grading to be done as per university rule.

List of Experiments

Expt. No.	Name of Experiment	Page No.	Date of Expt.	Signature	Grade awarded
1	Design a Full Adder using basic gates and verify its output / Design a Full Subtractor circuit using basic gates and verify its output.	4 - 11	15.09.20 & 22.09.20		
2	Construction of Decoder & Multiplexer circuits using logic gates.				
3	Realization of RS / JK / D flip flops using logic gates.				
4	Design of Shift Register using J-K / D Flip Flop.				
5	Realization of Synchronous Up/Down counter.				
6	Design a Phase-Shift Oscillator.				
7	Design of a Schmitt Trigger using 555 timer.				

EXPERIMENT NO : 1

Title : Design and implementation of Full Adder & Full Subtractor circuit using Logic Gates.

Objective: To realize the truth table of Full Adder & Full Subtractor circuit using Logic Gates.

The Experiment will Cover the Course Outcome (CO):	**CO1: Analyze** the truth table of basic combinational circuits and sequential circuits.
Bloom's Cognitive Domain:	**Analyze**

For Full Adder

TRUTH TABLE :(Fill up the table)

INPUT			OUTPUT	
A	B	C_{IN}(Carry in)	S (Sum)	C_{OUT}(Carry out)
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Boolean Expression (applying simplification technique) for Sum and Carry

Sum (S) = $A'B'C_{IN} + A'BC_{IN}' + AB' C_{IN}' + ABC_{IN}$

$= A'(B'C_{IN} + BC_{IN}') + A(B' C_{IN}' + BC_{IN})$

$= A'(B \text{ xor } C_{IN}) + A(B \text{ xnor } C_{IN})$

$= A'(B \text{ xor } C_{IN}) + A(B \text{ xor } C_{IN})'$

$= A \text{ xor } (B \text{ xor } C_{IN})$

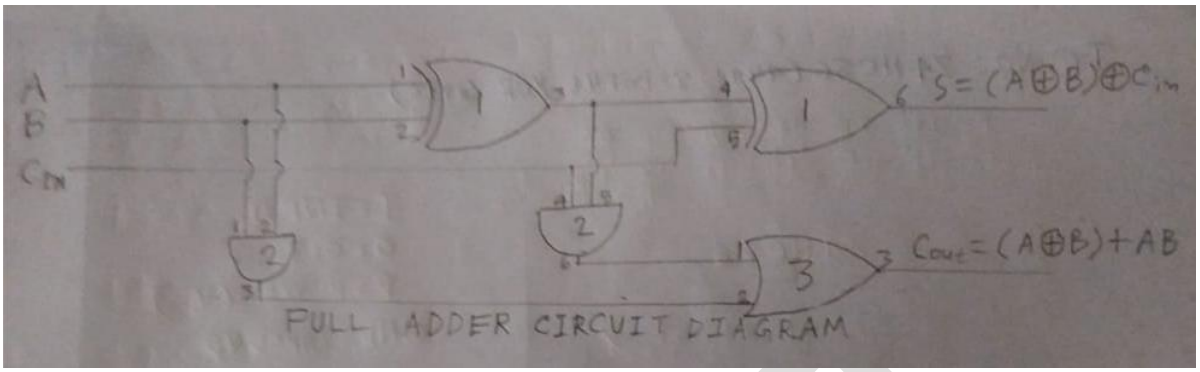
$= A \text{ xor } B \text{ xor } C_{IN}$

Carry-out(C_{out})= $A'BC_{IN} + AB'C_{IN} + ABC_{IN}' + ABC_{IN}$

$= (A'B + AB')C_{IN} + AB(C_{IN}' + C_{IN})$

$= (A \text{ xor } B)C_{IN} + AB$

<u>CIRCUIT DIAGRAM</u>(IC no. and its connecting pin nos. should be indicated)



For Full subtractor

<u>TRUTH TABLE</u> :(Fill up the table)

INPUTs			OUTPUTs	
X	Y	B_{IN} (Borrow in)	D (Difference)	B_{OUT}(Borrow out)
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

Boolean Expression (applying simplification technique) for Difference and Borrow

Difference (D) $= A'B'B_{IN} + A'BB_{IN}' + AB'B_{IN}' + ABB_{IN}$

$= (A'B + AB')\ B_{IN}' + (A'B' + AB)\ B_{IN}$

$= (A \text{ xor } B)\ B_{IN}' + (A \text{ xnor } B)\ B_{IN}$

$= (A \text{ xor } B)\ B_{IN}' + (A \text{ xor } B)'\ B_{IN}$

$= (A \text{ xor } B) \text{ xor } B_{IN}$

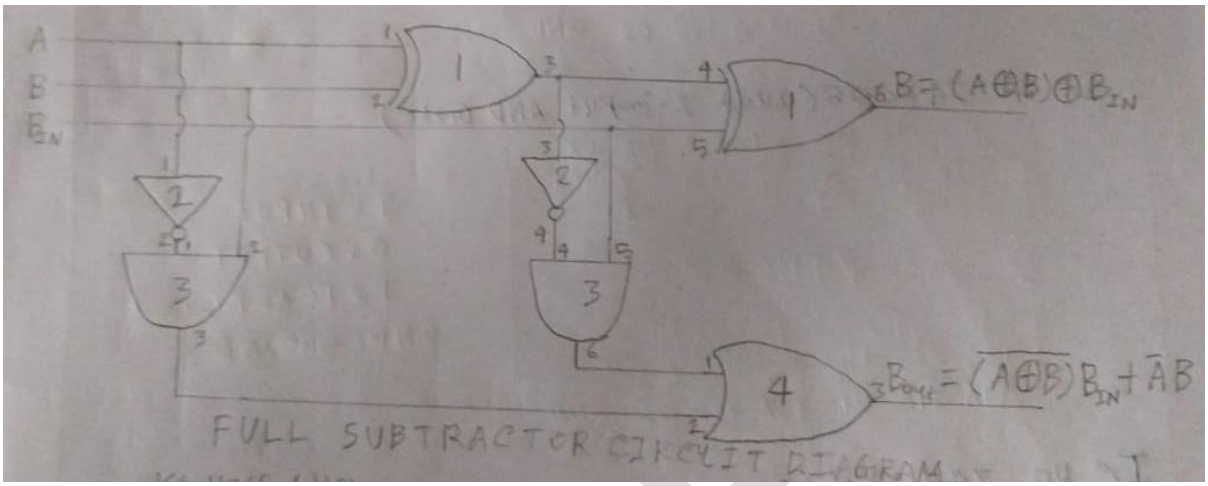
Borrow-out (B_{OUT}) = $A'B'B_{IN} + A'BB_{IN}' + A'BB_{IN} + ABB_{IN}$

= $(A'B' + AB)B_{IN} + A'B(B_{IN}' + B_{IN})$

= $(A \text{ xnor } B)B_{IN} + A'B$

= $(A \text{ xor } B)'B_{IN} + A'B$

CIRCUIT DIAGRAM (IC no. and its connecting pin nos. are to be indicated)



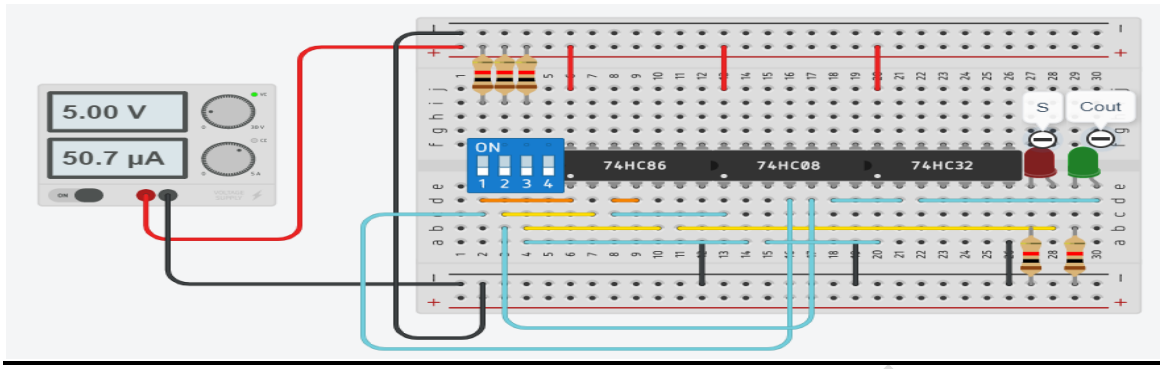
APPARATUS: 1. Trainer Kit.

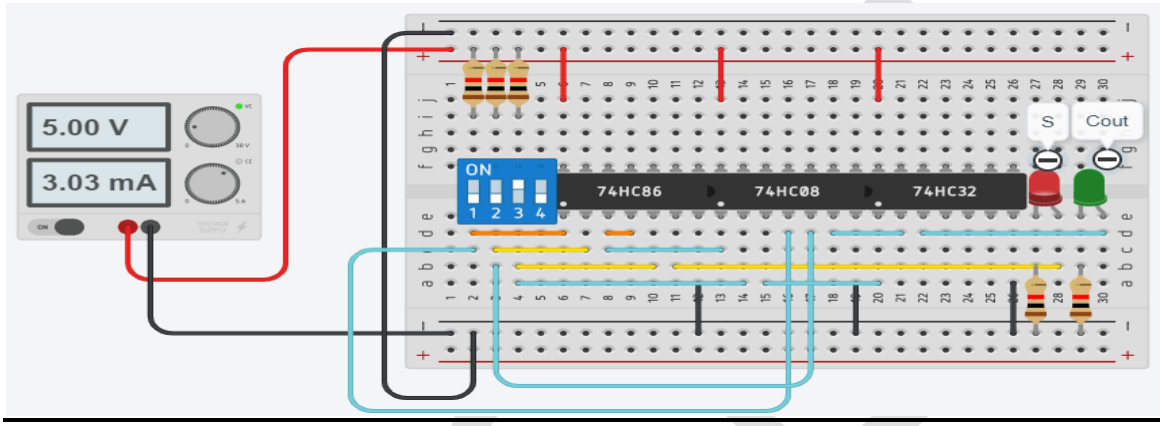
COMPONENTS:

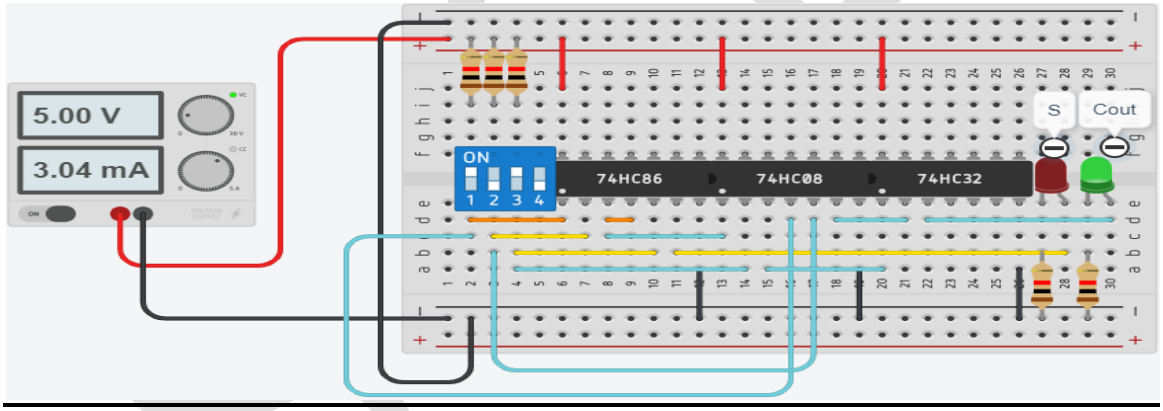
Complete the following table as per circuit diagram and collect the component from Laboratory.

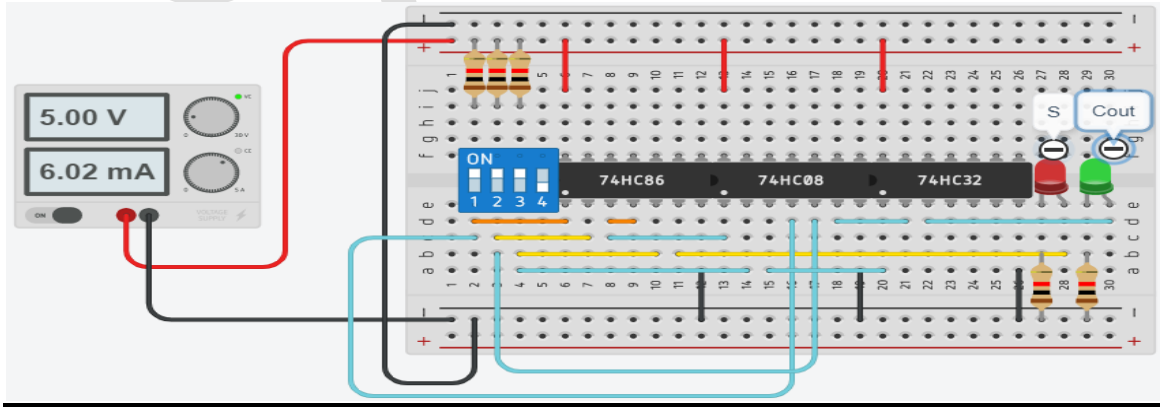
Sl.no	IC no.	IC Description	Qty
1	74HC86	Quad 2-input XOR gate	1
2	74HC08	Quad 2-input AND gate	1
3	74HC32	Quad 2-input OR gate	1
4	74HC04	Hex invertor	1

Full adder circuit on breadboard:



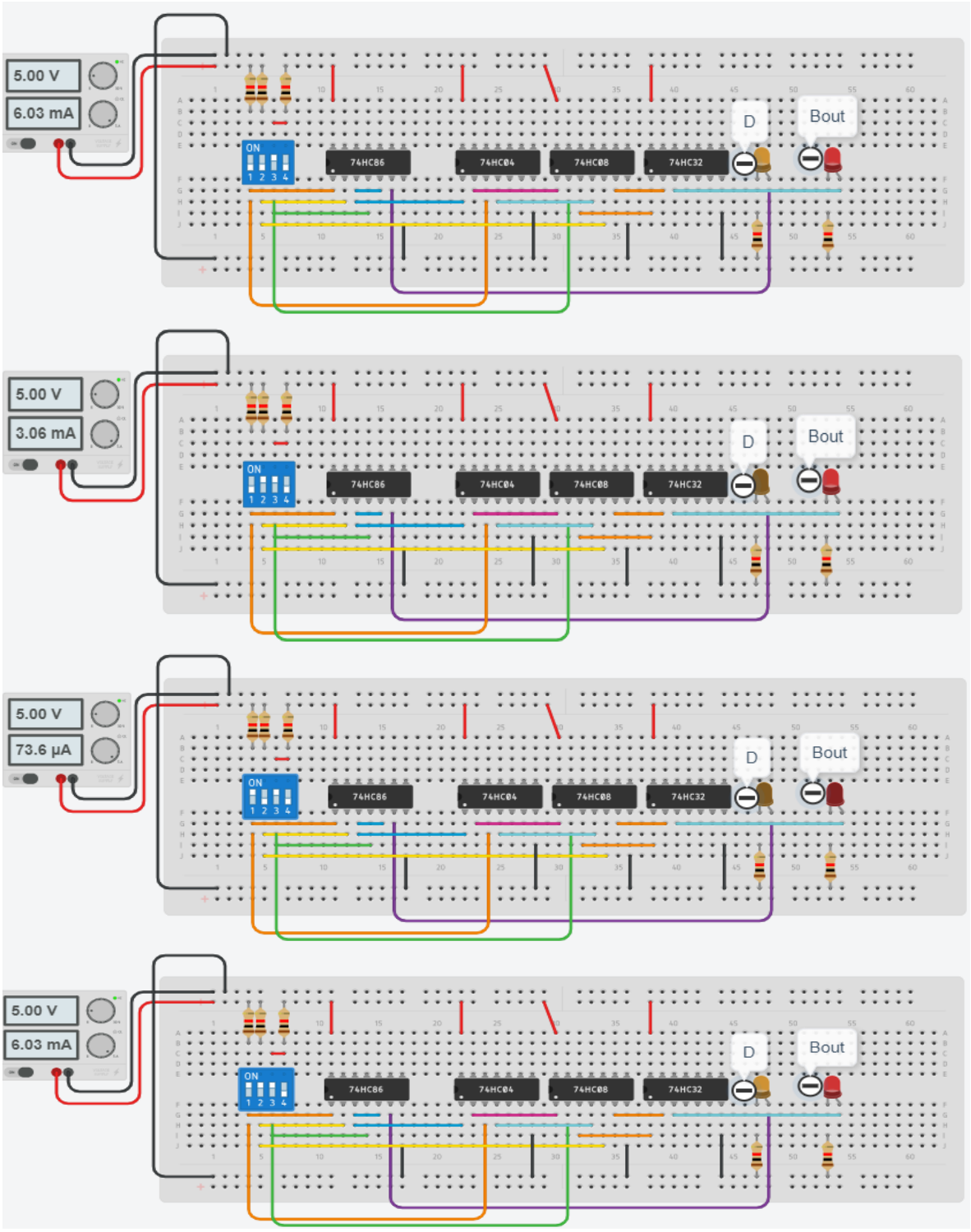






1ST input: 0 0 0 2nd input: 0 0 1 3rd input: 1 0 1 4th input: 1 1 1

Full Subtractor Circuit on breadboard:



1st input: 0 0 1 2nd inpur: 0 1 1 3rd input: 1 0 1 4th input: 1 1 1

OBSERVATION:

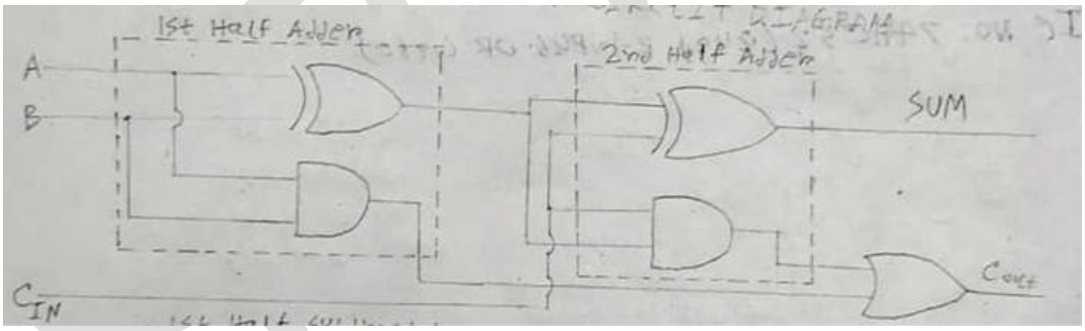
We examined the working mechanism of the Full Adder and Full Subtractor circuits and build them with XOR, AND, OR and invertor. We also tallied our outputs with the truth table of the respective circuits.

Questionnaires:

1. Design a Full adder circuit using 2 half adder circuits.
2. Design a Full subtractor circuit using 2 half subtractor circuits.
3. Design a Full adder circuit using only 2 input NAND gates.
4. Design a Full subtractor circuit using only 2 input NAND gates.

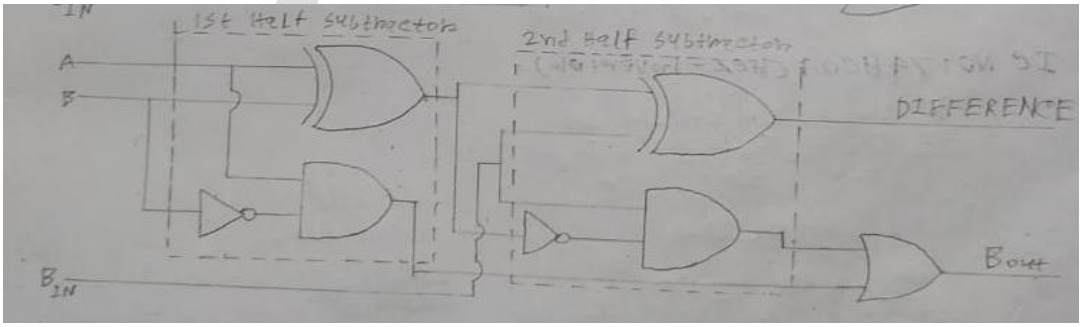
Answer :

1. Ans:



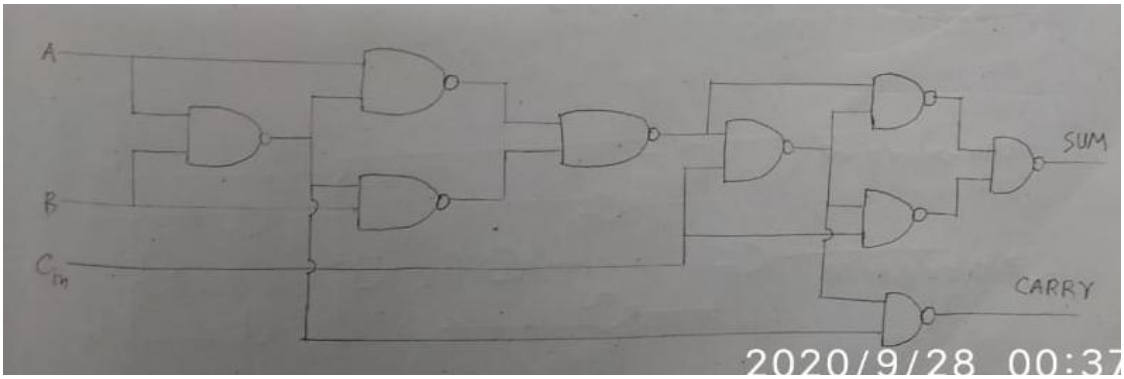
Full Adder using 2 half adder circuits

2. Ans:



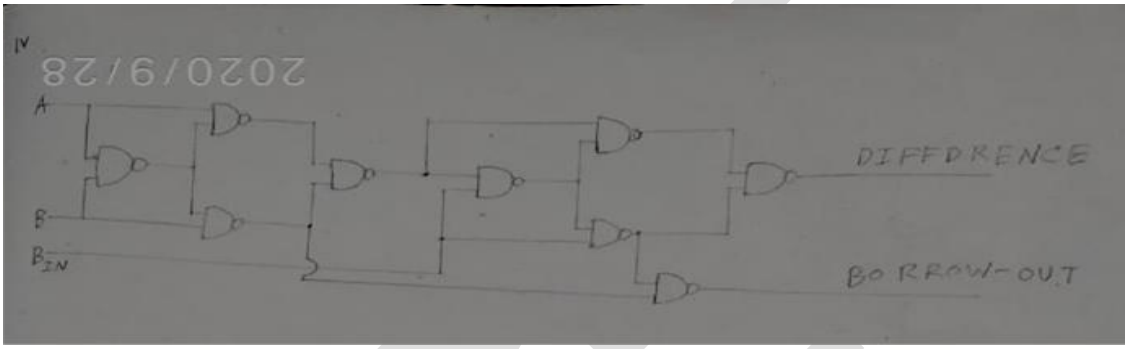
Full subtractor using 2 half subtractor circuits

3. Ans:



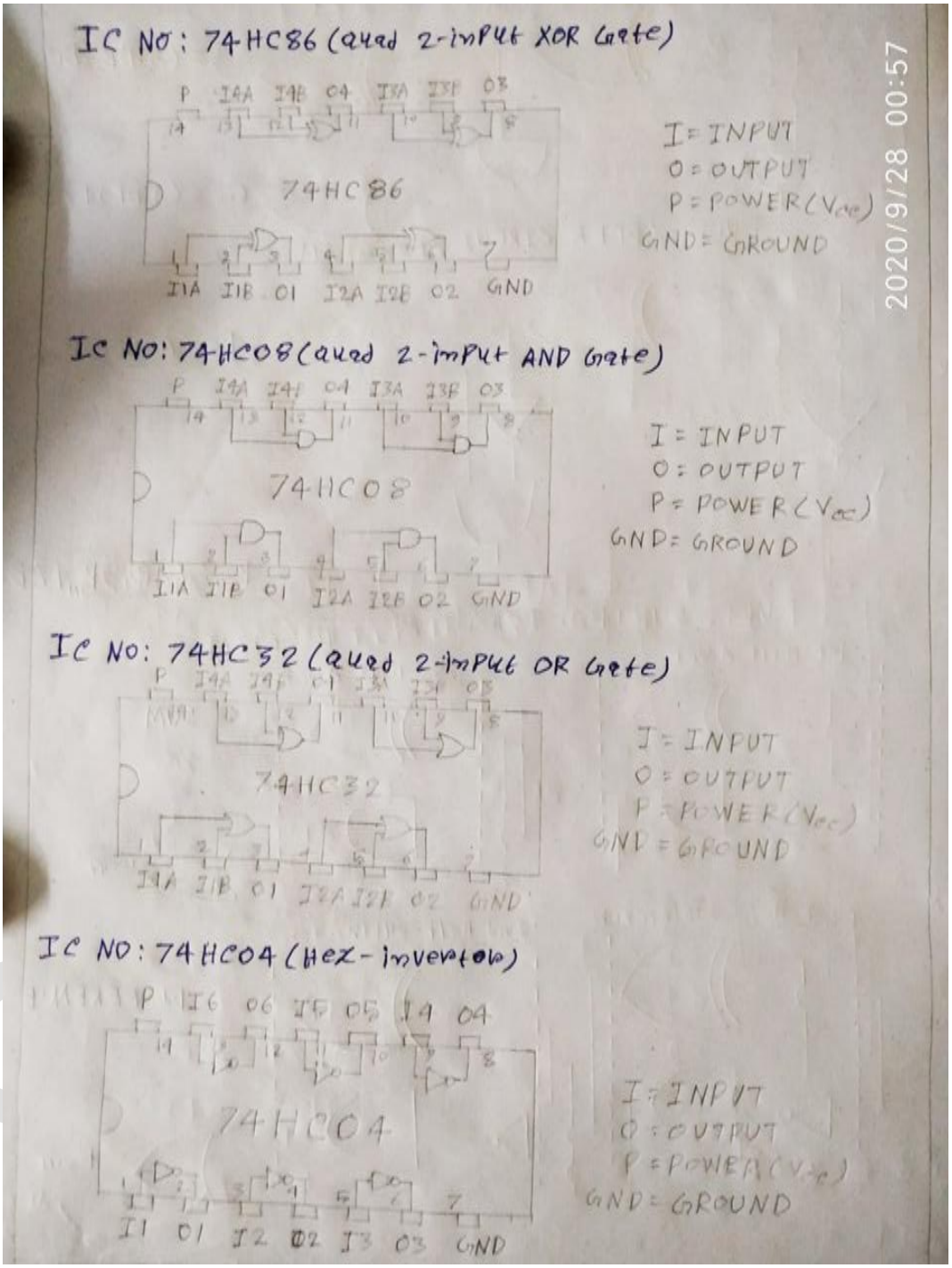
Full Adder circuit using 2 input NAND gates

4. Ans:



Full Subtractor circuit using 2 input NAND gates

Discussion:



Teacher's Signature with date	