Viva Questions for DDCO Lab

All the questions here are taken from the lab materials in the shared Google Drive link, so please study them well!
Note: One question on testbench writing will definitely be asked for some input combination

Basics of Verilog

1. What is Verilog?
2. Why do we use Verilog instead of schematic entry?
3. What are the 4 levels of abstraction in Verilog?
4. Give examples of valid and invalid identifiers in Verilog.
5. Is Verilog case sensitive? Give an example.
6. What is a module in Verilog?
7. What keyword is used to end a module definition?
8. What is the difference between *ports* and *signals*?
9. Explain the rules for connecting input, output, and inout ports.
10. What are vector data types in Verilog? Give an example.

Data Types

11. What are nets in Verilog?
12. What is the default type of a net?
13. What are registers (reg)?
14. Difference between `wire` and `reg`.
15. What is a memory in Verilog? Give an example declaration.
16. What is the difference between integers and reals in Verilog?
17. What is the default width of an integer in Verilog?
18. How is `time` represented in Verilog?
19. What are parameters in Verilog?
20. What is an event variable used for?

Number System and Logic

21. How do you represent numbers in binary, octal, decimal, and hexadecimal in Verilog?
22. Write the Verilog representation of the decimal number 13 in binary, octal, and hexadecimal.
23. What are the 4 possible logic values in Verilog?
24. What does `Z` represent?
25. What does `X` represent?
26. What is the truth table of AND gate when one input is Z?

27. Write the reduction operator equivalent for "all bits ANDed together".

Operators

28. List all arithmetic operators in Verilog.
29. List all logical operators in Verilog.
30. What is the difference between bitwise `&` and logical `&&`?
31. What does the concatenation operator `{}` do? Give an example.
32. Write the Verilog code to reverse the bits of a 4-bit bus `a`.
33. Write the ternary operator equivalent of a NOT gate
34. What is the difference between blocking (`=`) and non-blocking (`<=`) assignments?

System Tasks

35. What is `$display` used for?
36. Difference between `$display` and `$write`.
37. What is `$strobe` used for?
38. How is `$monitor` different from `$display`?
39. Write a `$display` command to print a variable in binary and decimal format.
40. What are `$fopen` and `$fclose` used for?

Delays & Timescale

41. What does `#20` mean in Verilog?
42. What does `timescale 1ns/1ps` mean?
43. Give an example of specifying rise and fall delays in a gate.
44. Differentiate between rise, fall, and turn-off delay.

Modeling Styles

45. Define Gate-level modeling.
46. Define Data-flow modeling.
47. Define Behavioral modeling.
48. Write a gate-level model of a 2-input AND gate.
49. Write a data-flow model of a 2-input AND gate.
50. Write a behavioral model of a 2-input AND gate.
51. Why is a behavioural output declared as `reg`?
52. Write the RTL code for a 2:1 MUX using `assign`.

53. Write a behavioral code for a 2:1 MUX using `if-else`.
54. Write a behavioral code for a 2:1 MUX using `case`.

Circuits

55. Write the data-flow code for a NOT gate.
56. Write the behavioral code for a NOT gate.
57. Write a gate-level code for a half-adder.
58. Write data-flow code for a half-adder.
59. Write behavioral code for a half-adder.
60. Write the gate-level code for a full-adder.
61. Write data-flow code for a full-adder.
62. Write behavioral code for a full-adder.
63. Why is it called a ripple carry adder?
64. Write code for a 4-bit ripple carry adder.
65. Write code for a 4:1 multiplexer using gate-level modeling.
66. Write data-flow code for a 4:1 multiplexer.
67. Write behavioral code for a 4:1 multiplexer.
68. Write code for a simple digital fan controller where Fan = T & P | O.

Test Benches

69. What is a test bench?
70. Can a test bench have input/output ports? Why/why not?
71. Write a test bench for a NOT gate.
72. **Test bench for 2:1 MUX?**
    Ans:
    ```
    sel = 1'b0; d0=1'b0; d1=1'b1;
    #10 sel = 1'b1; d0=1'b0; d1=1'b1;
    #10 sel = 1'b0; d0=1'b1; d1=1'b0;
    #10 sel = 1'b1; d0=1'b1; d1=1'b0;
    ```

73. **Test bench for half-adder?** →
    Ans:
    ```
    a = 1'b0; b=1'b0;
    #10 a = 1'b0; b=1'b1;
    #10 a = 1'b1; b=1'b0;
    #10 a = 1'b1; b=1'b1;
    ```

74. **Test bench for full-adder?** →
    Ans:
    ```
    a=0; b=0; cin=0;
    #10 a=0; b=0; cin=1;
    #10 a=0; b=1; cin=0;
    #10 a=0; b=1; cin=1;
    #10 a=1; b=0; cin=0;
    #10 a=1; b=0; cin=1;
    #10 a=1; b=1; cin=0;
    #10 a=1; b=1; cin=1;
    ```
75. **Test bench for RCA?** → Apply multiple 4-bit combinations.
    Ans:
    ```
    a = 4'b0000; b = 4'b0000; cin = 0;
    #10 a = 4'b0001; b = 4'b0010; cin = 0;
    #10 a = 4'b0011; b = 4'b0100; cin = 1;
    #10 a = 4'b1111; b = 4'b0001; cin = 0;
    #10 a = 4'b1010; b = 4'b0101; cin = 1;
    ```
76. Write a test bench for a 4:1 multiplexer.
77. What is `$dumpfile` used for in a test bench?
78. What is `$dumpvars` used for?

Simulation & Tools

79. What is Icarus Verilog?
80. What is GTKWave used for?
81. What commands are used to compile and run a Verilog file in Icarus Verilog?
82. Write the command to run `iverilog` on two files: `comparator.v` and `stimulus.v`.
83. What is a `.vcd` file?
84. How do you view a `.vcd` file?

Advanced / Conceptual

85. What are User Defined Primitives (UDP)?
86. Can UDPs have multiple outputs? Why/why not?
87. What is the difference between combinational and sequential UDP?
88. What are events used for in Verilog?
89. Differentiate between `initial` and `always` blocks.
90. Can an `initial` block be synthesized in hardware? Why not?
91. Explain the difference between blocking and non-blocking assignments with an example.
92. What is sensitivity list in an `always` block?
93. What is the use of `case` statement in Verilog?

94. What is a synthesizable construct? Give examples.
95. What is a non-synthesizable construct? Give examples.

Code-Based (Value Combinations)

96. Write a test bench for a 4-bit ripple carry adder to test values A=1010, B=0101, Cin=1.
