1. Problem Statement

Two-Stage Operational Amplifier at 1 um technology

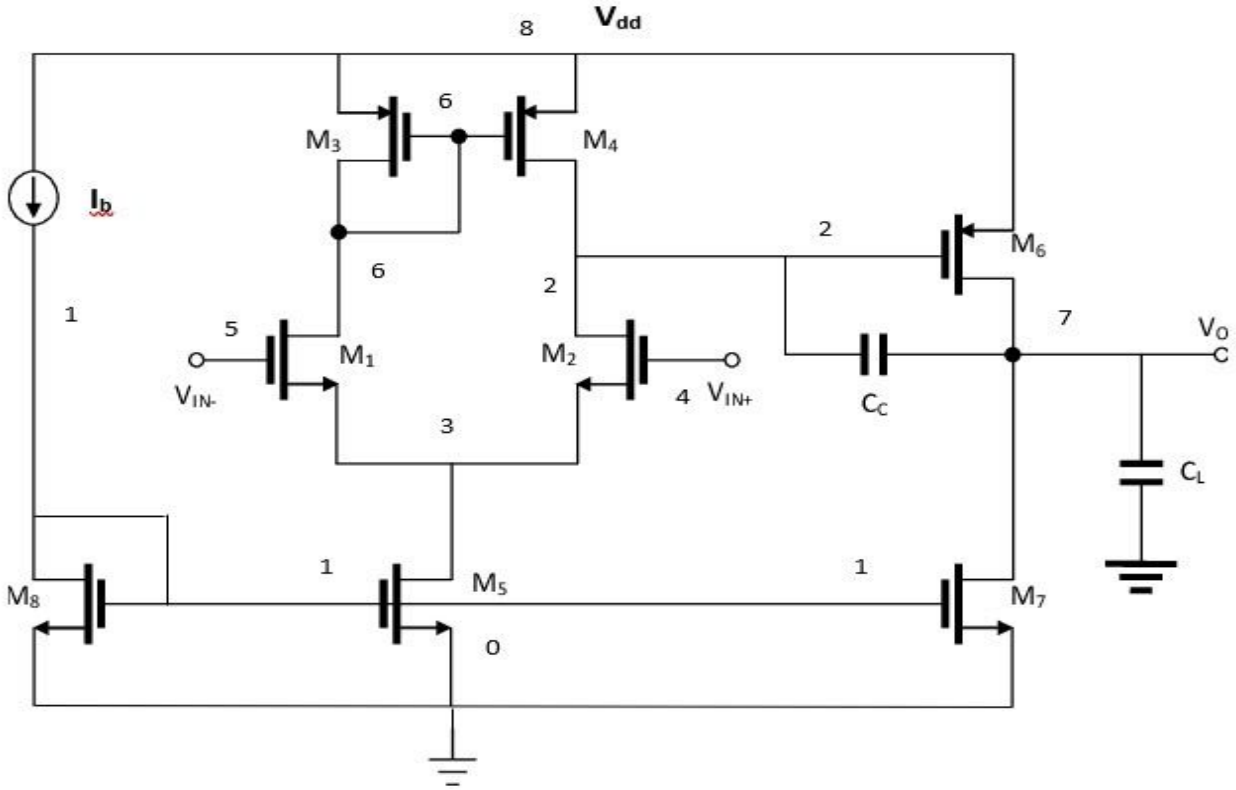
If K_N'=120µA/V^2, K_P'= 25µA/V^2, *VTN* = |*VTP*| = 0.5, λn= 0.06V^{-1}, and λp =0.08 V^{-1}.

Design a two-stage, CMOS op amp that meets the following specifications. Assume the channel length is to be 1µm and the load capacitor is *CL* = 10pF.

Note: For 1um design consider the standard model used in the lab.

***Av* > 3000V/V**	***VDD* =2.5V**	***GB* = 5MHz**	***SR* > 10V/µs**
60° phase margin	**0.5V<Vout range<2V**	***ICMR* = 1.25V to 2V**	***Pdiss* 2mW**

2. Circuit Diagram



3. Spice Code

a) SPICE CODE for AC Analysis of circuit:

```
*mini project
.include "1um_model.sp"
*set sizing of MOS
m1 1 3 2 0 N_1u w=1.644u l=1u
m2 4 5 2 0 N_1u w=1.644u l=1u
m3 1 1 6 6 P_1u w=20u l=1u
m4 4 1 6 6 P_1u w=20u l=1u
m5 2 9 0 0 N_1u w=4.25u l=1u
m6 7 4 6 6 P_1u w=209.6u l=1u
m7 7 9 0 0 N_1u w=20.77u l=1u
m8 9 9 0 0 N_1u w=4.25u l=1u
*capacitors
ib 6 9 30ua
Cc 7 4 2pf
Cl 7 0 10pf
vdd 6 0 2.5v
*set Vin val
vin1 3 10 dc 1.8v
vin2 5 12 dc 1.8v
vac 12 10 ac 1v
.ac dec 10 1 1g
.op
.probe
.end
```

b) SPICE CODE FOR Transient Analysis:

```
*mini project
.include "1um_model.sp"
*set sizing of MOS
m1 1 3 2 0 N_1u w=1.644u l=1u
m2 4 5 2 0 N_1u w=1.644u l=1u
m3 1 1 6 6 P_1u w=20u l=1u
m4 4 1 6 6 P_1u w=20u l=1u
m5 2 9 0 0 N_1u w=4.25u l=1u
m6 7 4 6 6 P_1u w=209.6u l=1u
m7 7 9 0 0 N_1u w=20.77u l=1u
m8 9 9 0 0 N_1u w=4.25u l=1u
*capacitors
ib 6 9 30ua
Cc 7 4 2pf
Cl 7 0 10pf
vdd 6 0 2.5v
*set Vin val
vin1 3 10 dc 1.8v
vin2 5 11 dc 1.8v
vin3 12 11 ac sin(0 0.0002 1000)
.op
.tran 1u 40ms
.probe
.end
```

4. Calculations

1.) The first step is to calculate the minimum value of the compensation capacitor C_c,
$C_c > (2/10)(10\text{ pF}) = 2\text{ pF}$

2.) Choose C_c as 3pF. Using the slew-rate specification and C_c calculate I_5. I_5 $= (2\text{x}10^{-12})(10\text{x}10^{6}) = 20\ \mu\text{A}$

3.) Next calculate $(W/L)_3$ using ICMR requirements

$$(\text{W/L})_3 = \frac{30\text{X}10^{-6}}{25\text{X}10^{-6}[2.5 - 2 - 0.65 + 0.25]} = 20 \rightarrow (W/L)_3 = (W/L)_4 = 20$$

4.) Now we can check the value of the mirror pole, $p3$, to make sure that it is in fact greater than $10GB$. Assume the $C_{ox} = 6\text{fF}/\mu\text{m}^2$. The mirror pole can be found as

$$p_3 \approx \frac{-g_{m3}}{2C_{gs3}} = \frac{-\sqrt{2K'_p S_3 I_3}}{2(0.667)W_3 L_3 C_{ox}} = \frac{(2\text{x}25\text{x}10^{6})\text{x}(30)\text{x}(15\text{x}10^{-6})^{1/2}}{2\text{x}(0.667)\text{x}30\text{x}1(6\text{x}10^{-3})^{1/2}} = 0.62\text{GHz}$$

or 622 MHz. Thus, p_3, is not of concern in this design because $p_3 >> 10GB$.

5.) The next step in the design is to calculate g_{m1} to get

$$g_{m1} = (5\text{x}10^{6})(2\pi)(2\text{x}10^{-12}) = 62.83\mu\text{S}$$

Therefore, $(W/L)_1$ is

$$(\text{W/L})_1 = (\text{W/L})_2 = \frac{g_{m1}^2}{2K_N I_1} = \frac{(62.83\text{x}10^{-6})^2}{2\text{x}120\text{x}15} = 1.644$$

$$\Rightarrow (\text{W/L})_1 = (\text{W/L})_2 = 1.644$$

6.) Next calculate V_{DS5},

$$V_{DS5} = (-1) - (-2.5) - \sqrt{\frac{20\text{x}10^{-6}}{120\text{x}10^{-6}\text{x}1.6449}} - \cdot 65 = 0.28168\text{V}$$

Using V_{DS5} calculate $(W/L)_5$ from the saturation relationship.

$$(\text{W/L})_5 = \frac{2(20\text{x}10^{-6})}{(120\text{x}10^{-6})(0.2816)^2} = 4.25$$

7.) For 60° phase margin, we know that

$$g_{m6} \geq 10g_{m1} = 691.3\mu\text{S}$$

Assuming that $g_{m6} = 691.3\mu\text{S}$ and knowing that $g_{m4} = 150\mu\text{S}$, we calculate $(W/L)_6$ as

$$(\text{W/L})_6 = 20\ \text{X}\ \frac{691.3\text{X}10^{-6}}{(150\text{X}10^{-6})} = 97.74$$

8.) Calculate $I6$ using the small-signal gm expression:

$$I_6 = \frac{(691.13\text{x}10^{-6})^2}{(2)(25\text{x}10\text{-}6)(97.74)} = 94.256\mu\text{A}$$

If we calculate $(W/L)6$ based on V_{out}(max), the value is approximately 15. Since 94 exceeds the specification and maintains better phase margin, we will stay with $(W/L)6 = 94$ and $I6 = 94.256\mu\text{A}$.

With $I6 = 94.256\mu\text{A}$ the power dissipation is

$$P_{diss} = 5\text{V}\cdot(30\mu\text{A}+94.256\mu\text{A}) = 0.6218\text{mW}$$

9.) Finally, calculate $(W/L)7$

$$(W/L)7 = \frac{4.2 \text{ x } 97.74\text{x}10^{-6}}{20\text{x}10\text{-}6} = 20.77$$

Let us check the V_{out}(min) specification although the W/L of M7 is so large that this is probably not necessary. The value of V_{out}(min) is

$$V_{out}(\text{min}) = V_{DS7}(\text{sat}) = \sqrt{\frac{2\cdot 97.74}{120\cdot 20.77}} = 0.28\text{V}$$

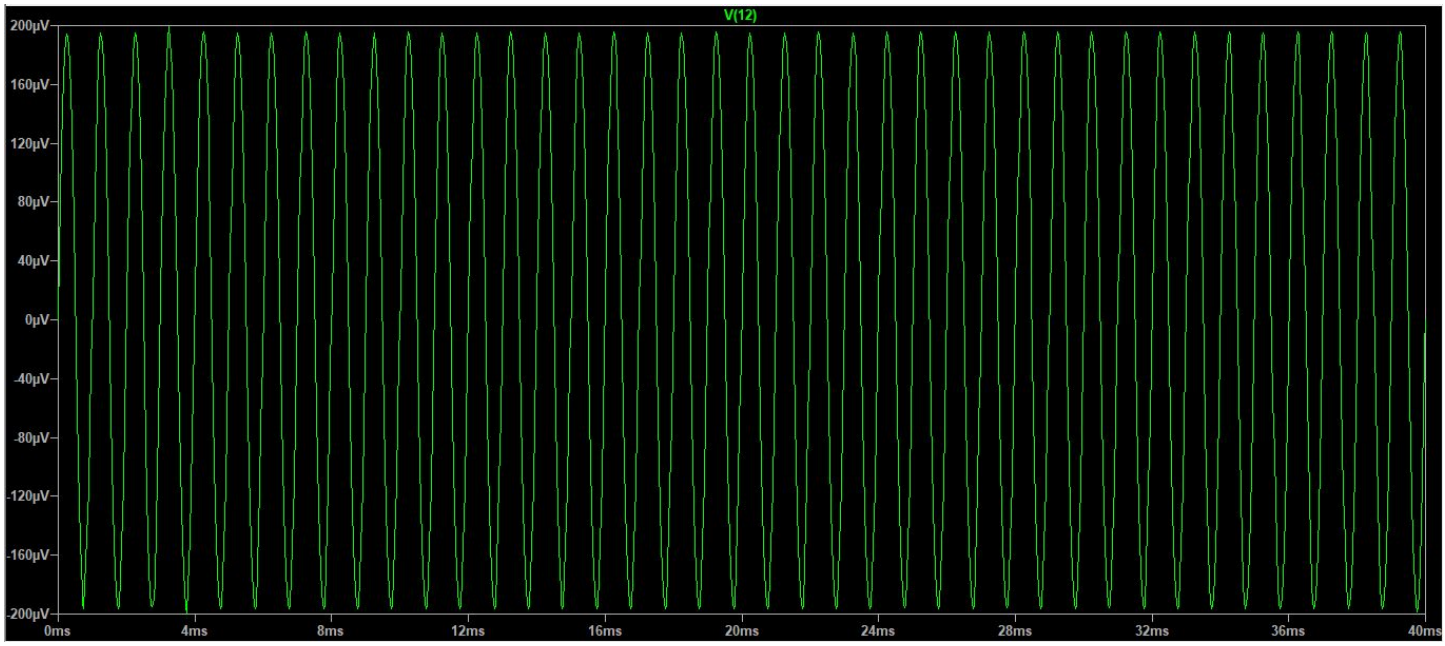
which is less than required. At this point, the first-cut design is complete.

10.) Now check to see that the gain specification has been met

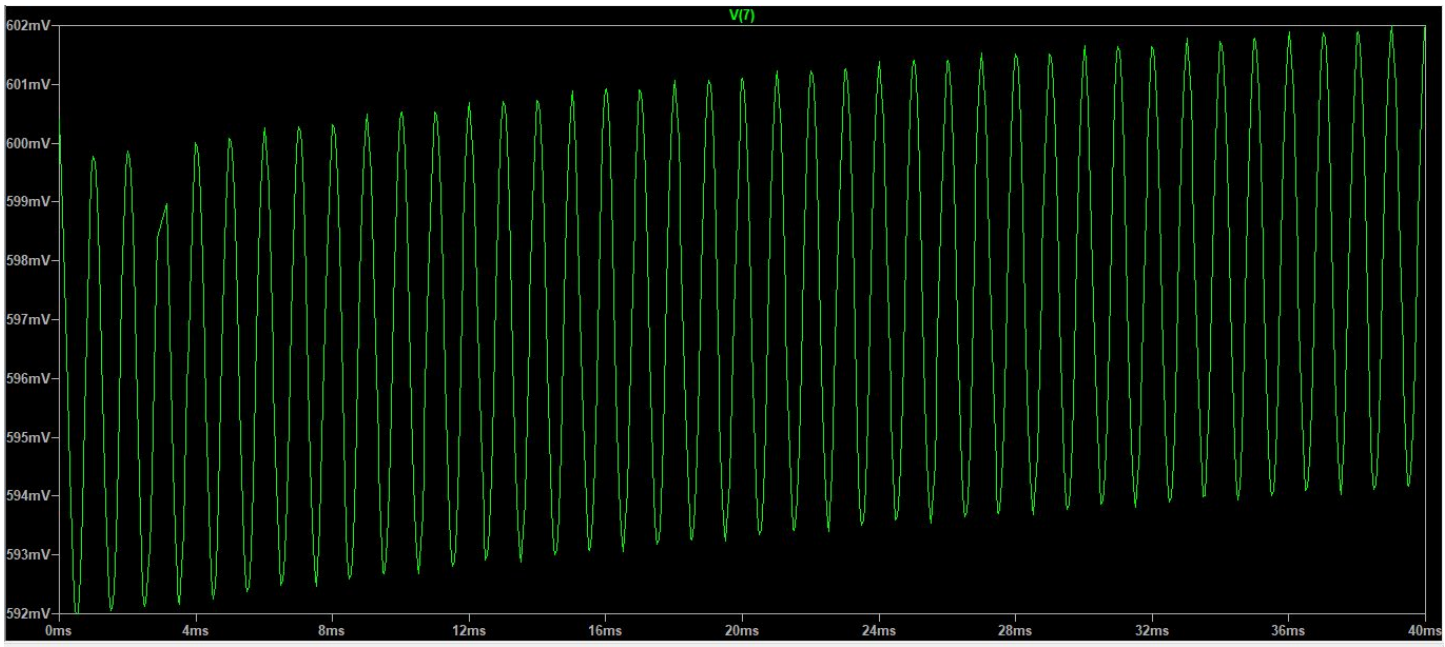
$$A_v = \frac{(62.83\text{x}10^{-6})(691.3\text{x}10^{-6})}{20\text{ x}10^{-6}\,(.08 + .06)\;97.74\text{x}10^{-6}\,(.08 + .06)} = 1133.36\text{V/V}$$

If the gain specification is not met, then the currents, I5 and I6, can be decreased or the W/L ratios of M2 and/or M6 increased. So I have increased W/L ratio of M6 in the final design to get a desired value of Av > 3000

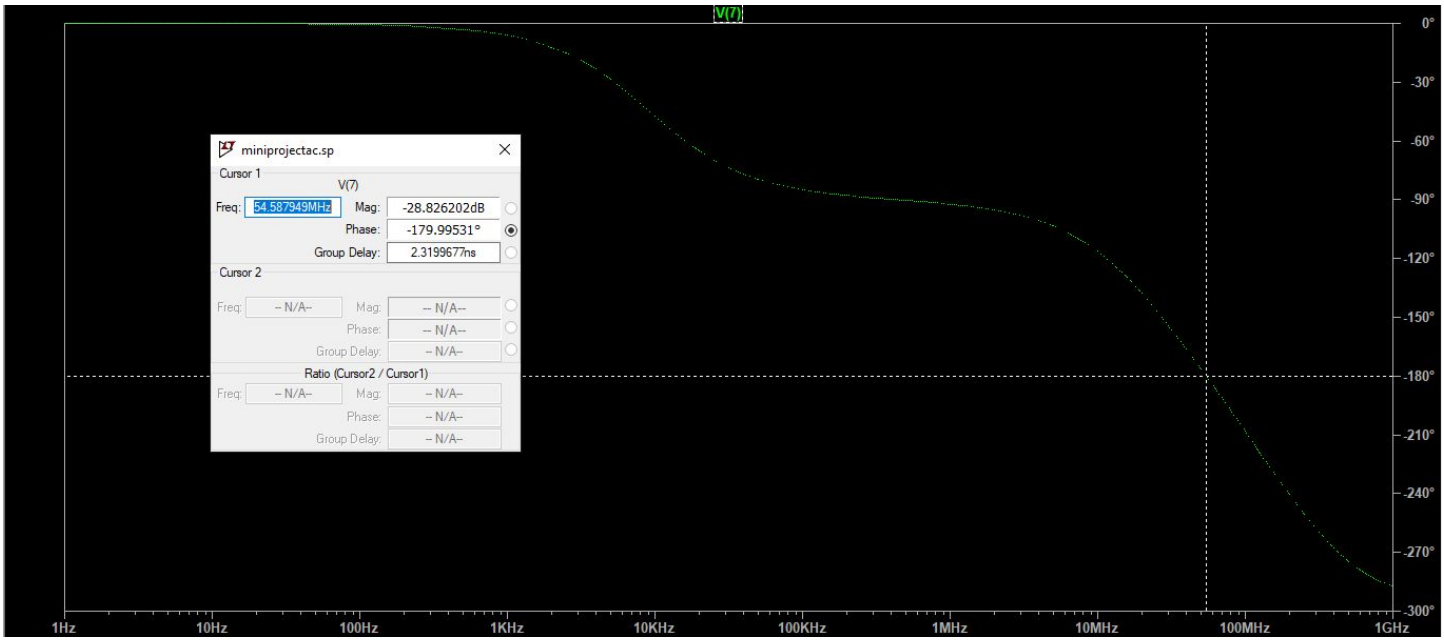
5. Simulation



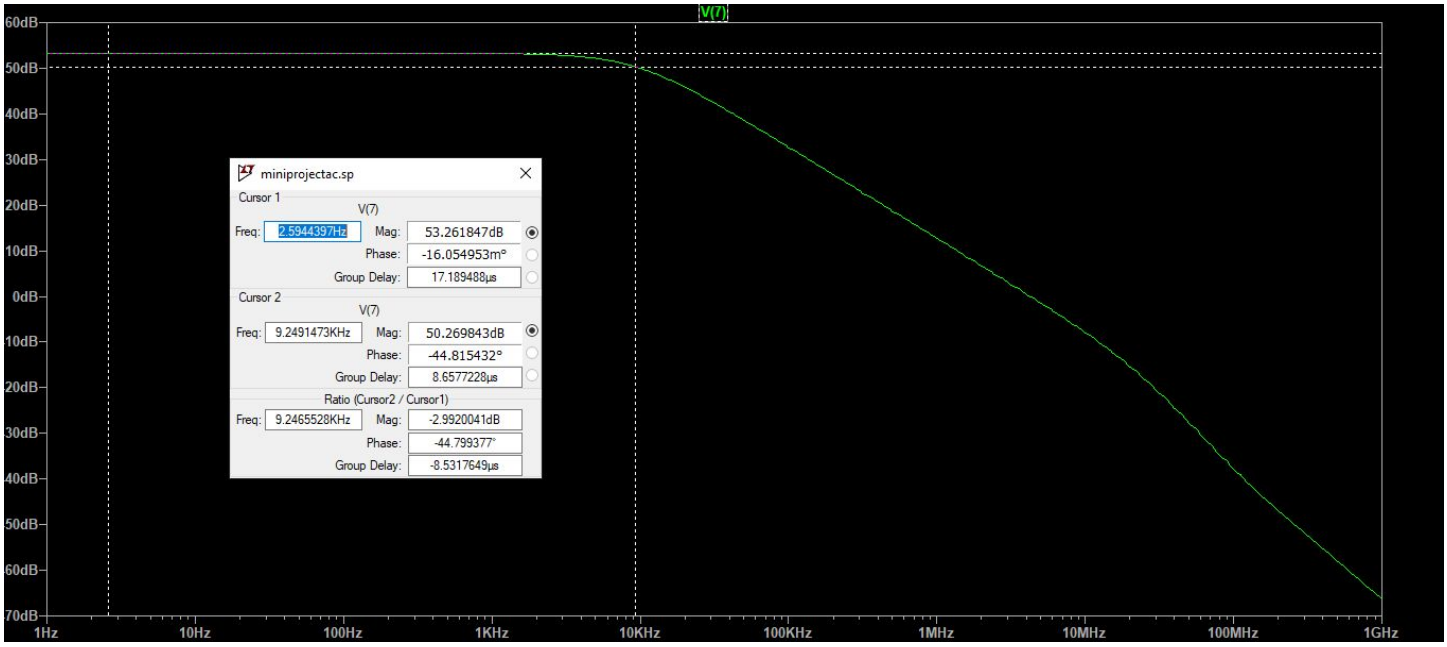
200uV input



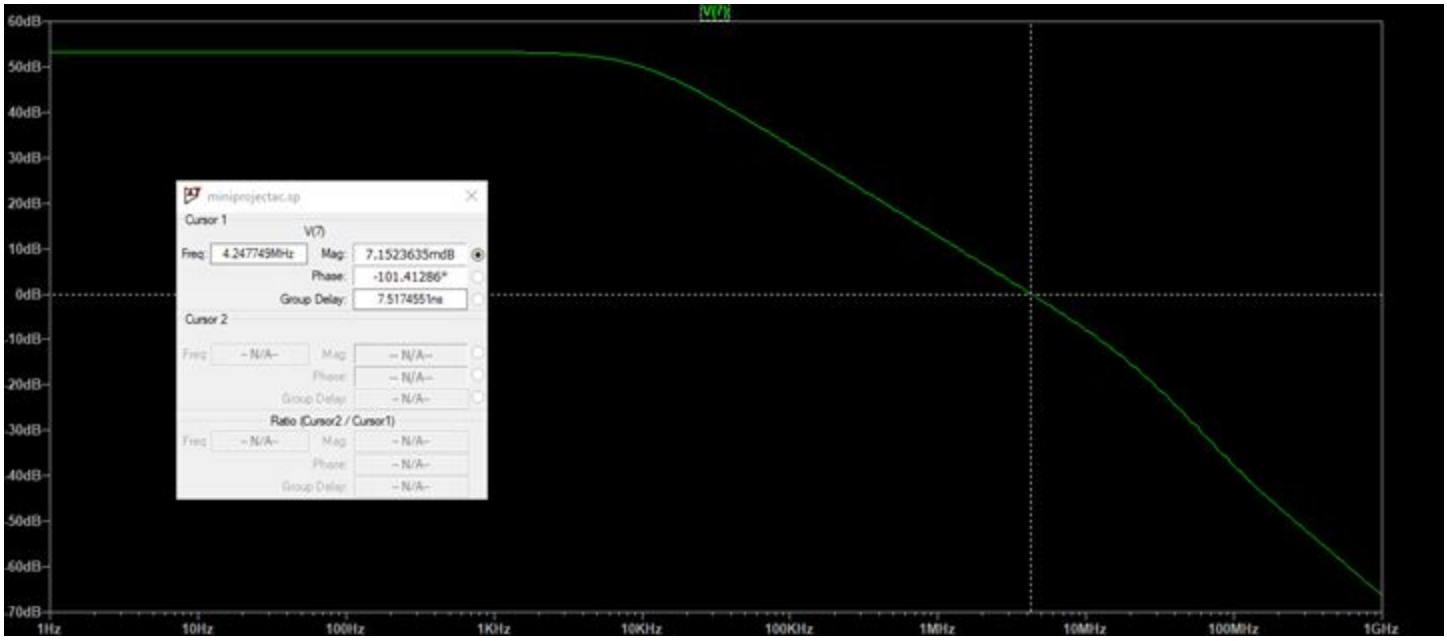
Vout in transient analysis



Phase plot in AC analysis



-3db frequency in AC analysis



Magnitude Plot in AC Analysis

6. Observation Tables

S.No.	(W/L)6	gm1 (uS)	VDS5 (V)	gm6 (uS)	Av (V/V)	I5 (uA)	I6 (uA)	-3db freq (KHz)	GM (db)	PM (deg)
1.	97.7	58.3	3.69e-1	766	360.945	28.7	74.5	163.27562	-28.761048	88.10
2.	150	58.3	3.69e-1	1170	627.5	28.7	114	109.90343	-29.443602	84.35
3.	180	58.3	3.69e-1	1410	831.9	28.7	137	80.56	-29.632364	82.70
4.	209.6	58.3	3.69e-1	1630	1131.3	28.7	159	51.565538	-29.556951	81.15
5.	234.5	58.3	3.69e-1	1790	3010	28.7	175	9.2509604	-28.894108	79.6

7. Conclusion

1. A two stage differential amplifier was designed using the given specifications. It was found that increasing the value of (W/L)6 increased the gain of the differential amplifier which is visible in the above observations.
2. The 2-Stage Opamp using CMOS had an equivalent effect on increasing I6.
3. 3db Frequency decreases with increasing (W/L)6 or I6 equivalently.

4. **Table for calculated values of circuit parameters for S6 = 97.7 vs Simulated results**

S.No.	Parameter	Calculated Value	Simulated Value	Deviation
1	I6 (uA)	97.74	74.5	23.77%
2	gm1 (uS)	62.83	58.3	7.21%
3	gm4 (uS)	141.42	145	2.53%
4	gm6 (uS)	691.13	766	10.83%
5	Av (V/V)	1133.36	360.945	68.15%

8. Result

1. We have successfully designed a two-stage, CMOS op amp that met the criterion specified in the problem statement.
2. We have done AC and Transient Analysis of the circuit & observed the 3dB Frequency, Phase Margin, Gain Margin and Voltage Gain for different values of (W/L)6
3. **DESIGN -**