Experiment 5
Tone Synthesizer

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Overview of the experiment

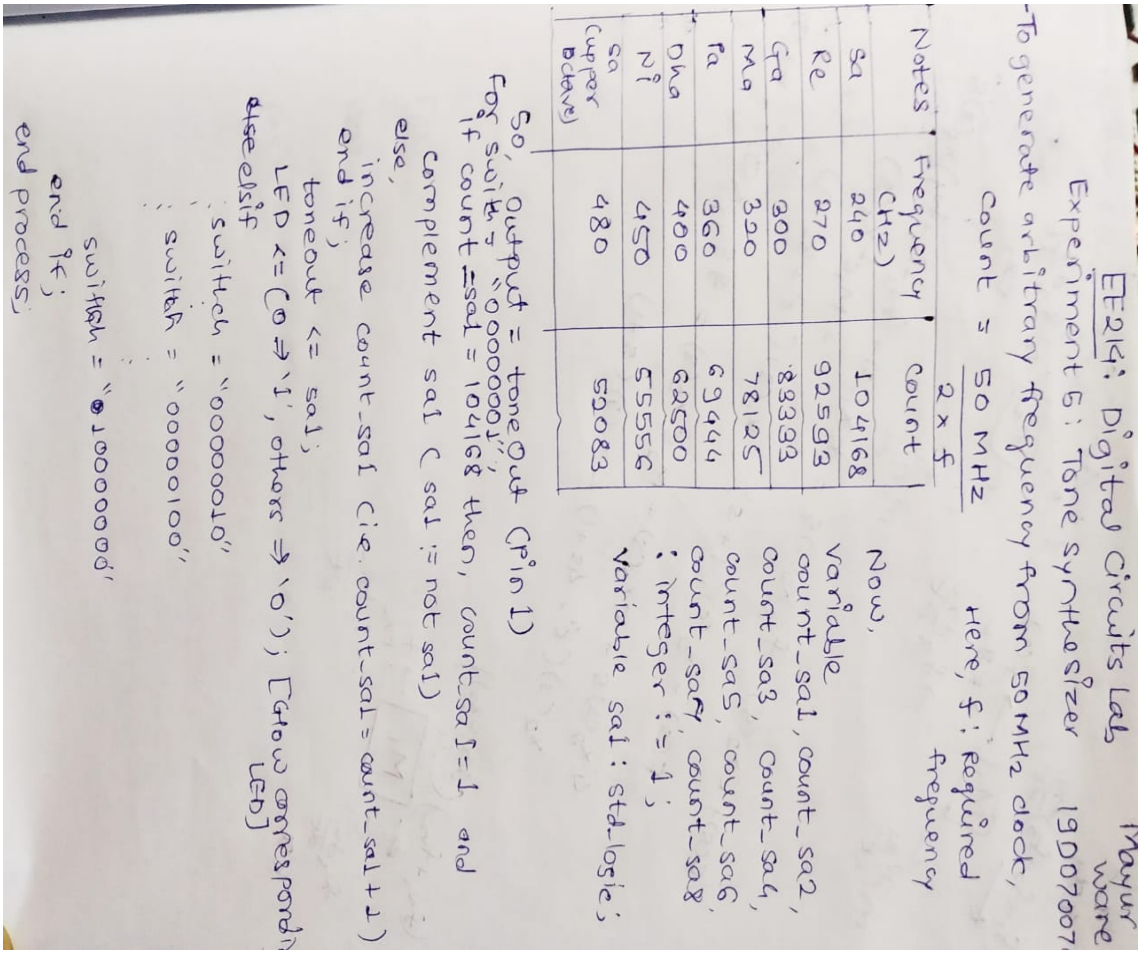
- The purpose of the experiment is to design a circuit which will generate the seven major notes in the Indian classical music named Sa, Re, Ga, Ma, Pa, Dha, Ni and Sa (upper octave) on the speaker.
- I used the 50MHz Master Clock (Krypton's On-board clock) to calculate the count value for each note by using the fomula $\frac{50MHz}{2*f}$ where 'f' is the required frequency and using the if elsif loops I implemented my logic.
- The report contains a handmade diagram which describes my approach, some important extracts of VHDL code, the output waveforms, Krypton Board Observations and Circuit Images.

Approach to the experiment

First, I calculated the counts for each Note using the formula given above.
The counts for each Note are given in this table:

Note	Frequency (Hz)	Count Value
Sa	240	**104168**
Re	270	**92593**
Ga	300	**83333**
Ma	320	**78125**
Pa	360	**69444**
Dha	400	**62500**
Ni	450	**55556**
Sa (Upper Octave)	480	**52083**

Then, using if else, if elsif loops and this count values, I implemented the logic.



Design document and VHDL code if relevant

Main Entity :

```
entity toneGenerator is
port (toneOut : out std_logic;              –this pin will give your notes output
clk : in std_logic;
LED : out std_logic_vector(7 downto 0);
switch : in std_logic_vector(7 downto 0));
end entity toneGenerator;
```

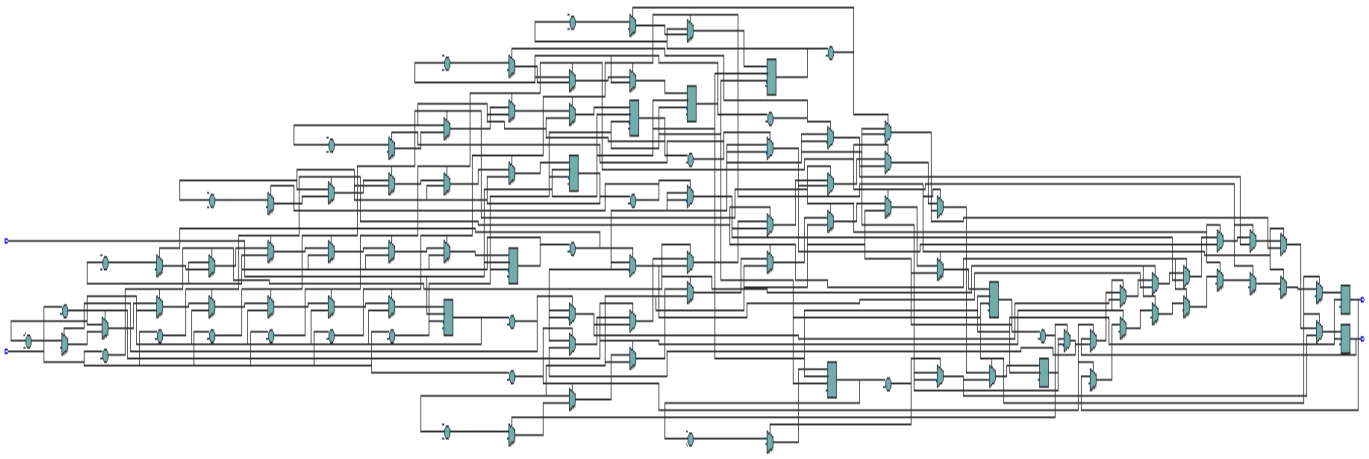
BCD_Adder :

```
if (count_sa1 = 104168) then              –240Hz for "Sa"
count_sa1 := 1;
sa1 := not sa1;
else
count_sa1 := count_sa1 + 1;
end if;
toneOut <= sa1;
LED <= (0 => '1', others => '0');
```

```
elsif switch= "00000010" then
if (count_sa2 = 92593) then               –270Hz for "Re"
count_sa2 := 1;
sa1 := not sa1;
else
count_sa2 := count_sa2 + 1;
end if;
toneOut <= sa1;
LED <= (1 => '1', others => '0');
```

Similar for 'Ga', 'Ma', 'Pa', 'Dha', 'Ni' and 'Sa (Upper Octave)'

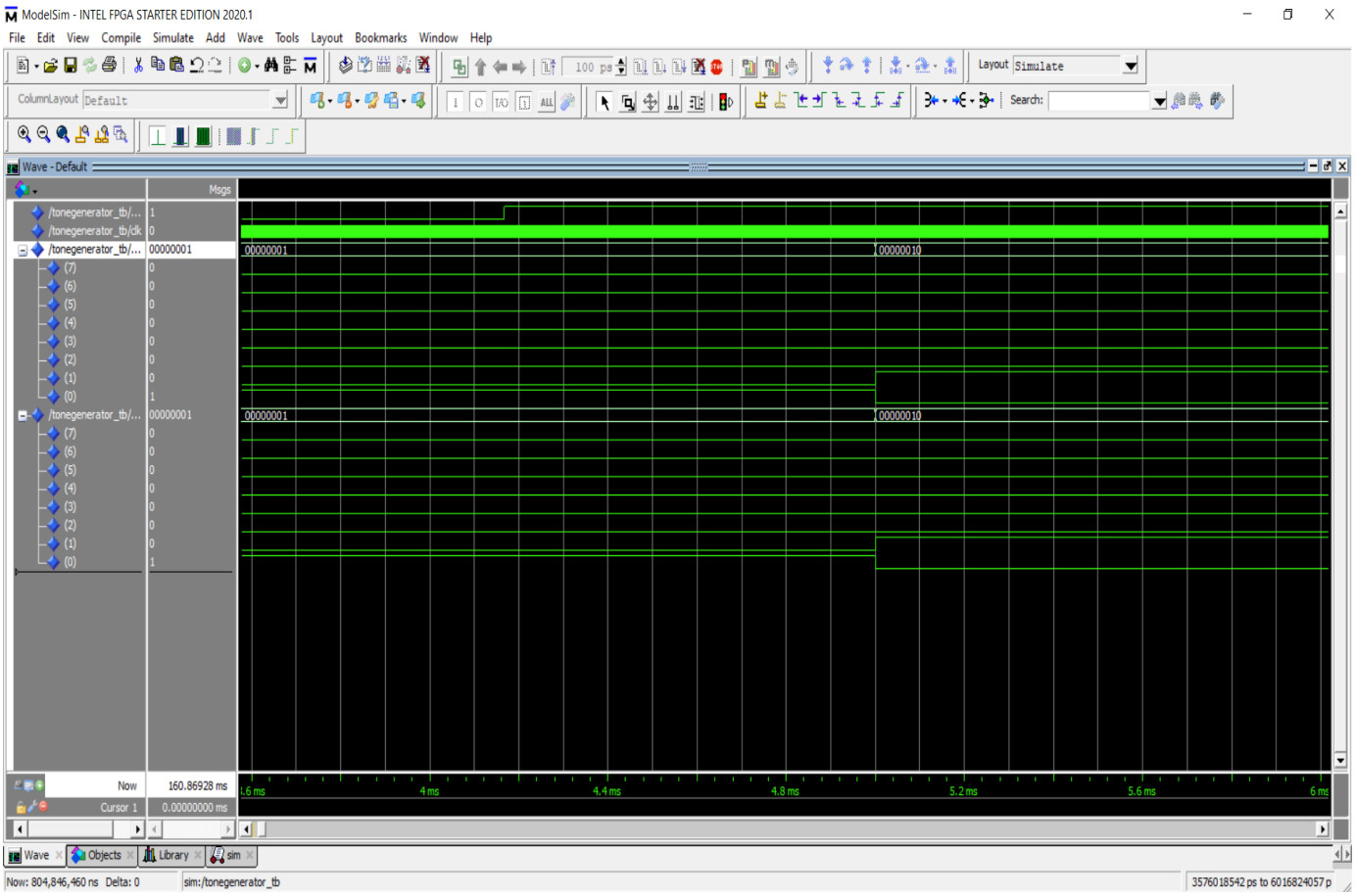
RTL View



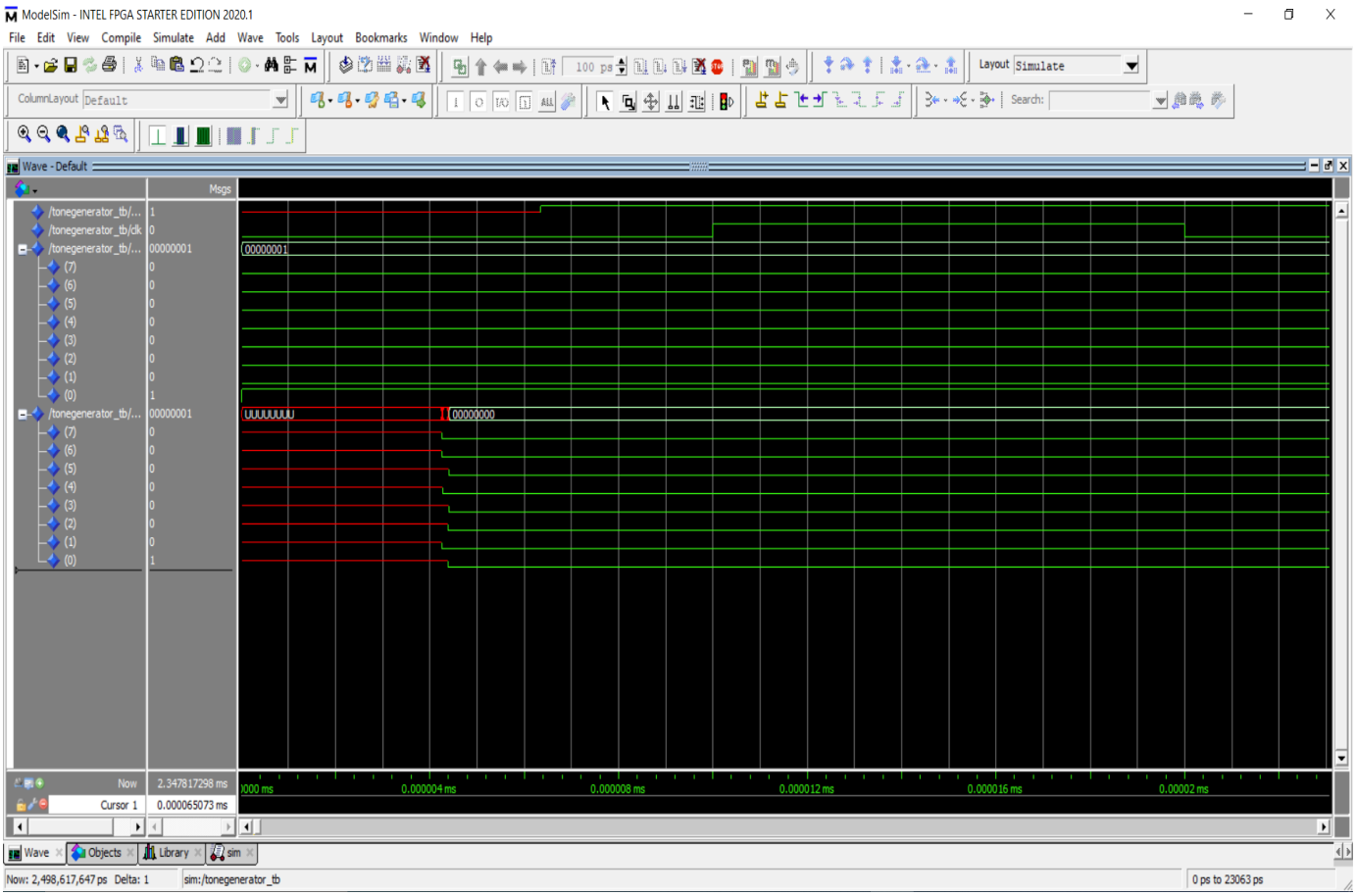
DUT Input/Output Format

```
toneOut : out std_logic;
clk : in std_logic;
LED : out std_logic_vector(7 downto 0);
switch : in std_logic_vector(7 downto 0));
```

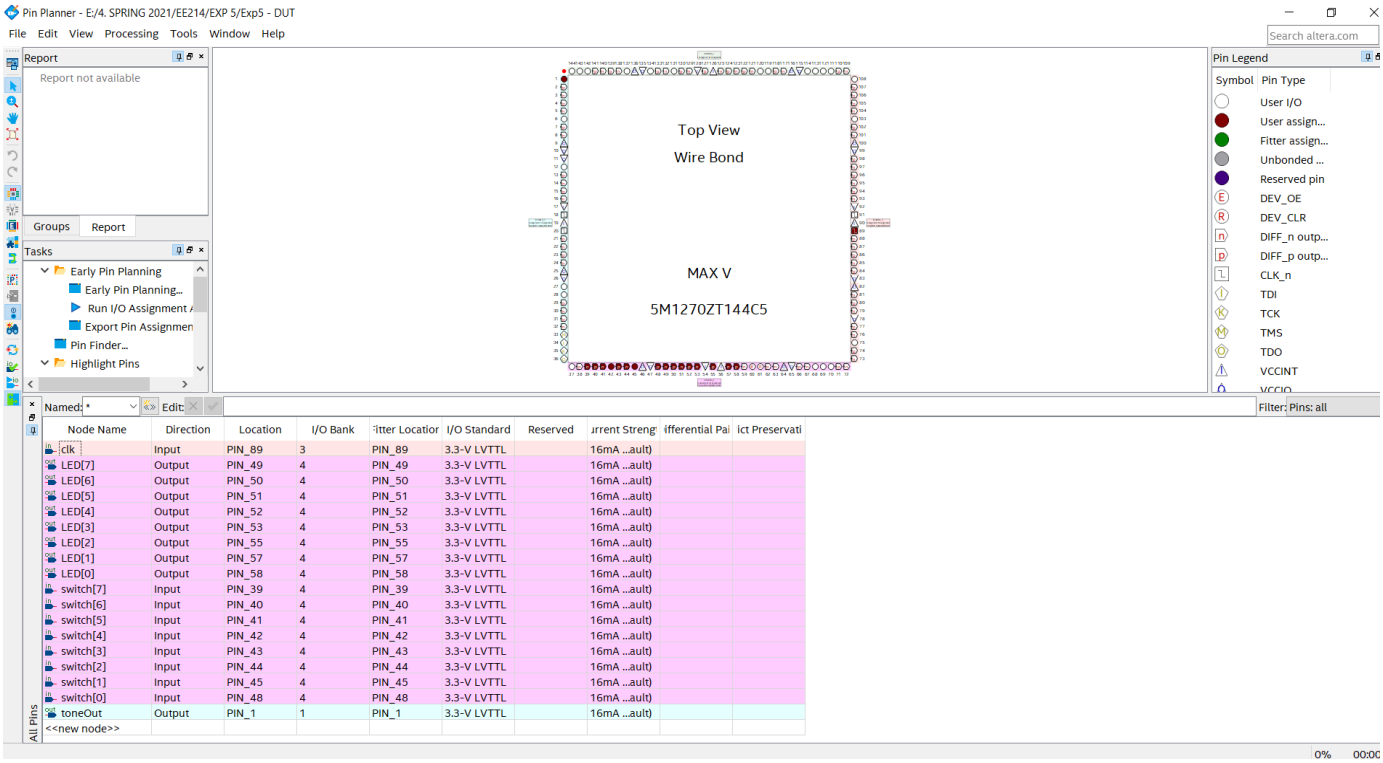
RTL Simulation



Gate-level Simulation



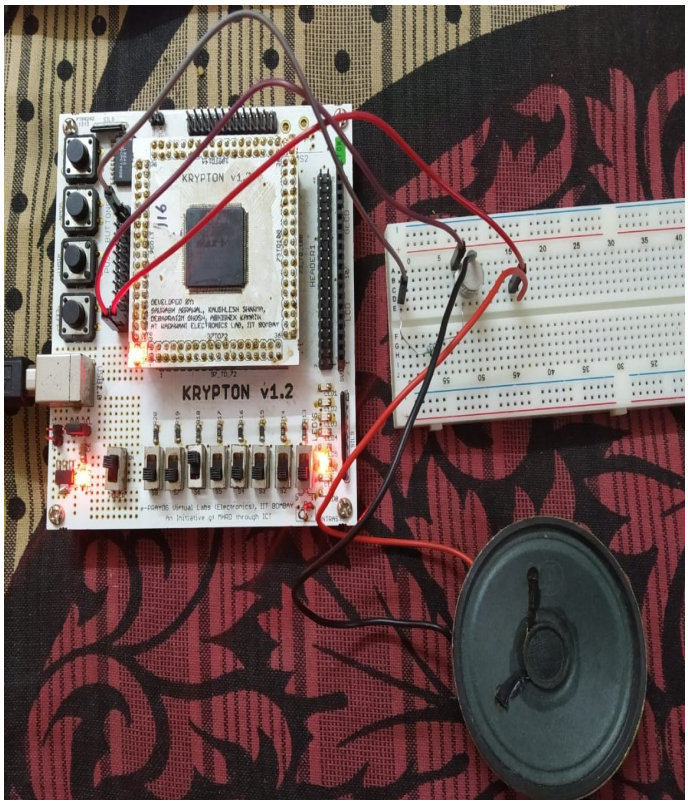
Krypton board



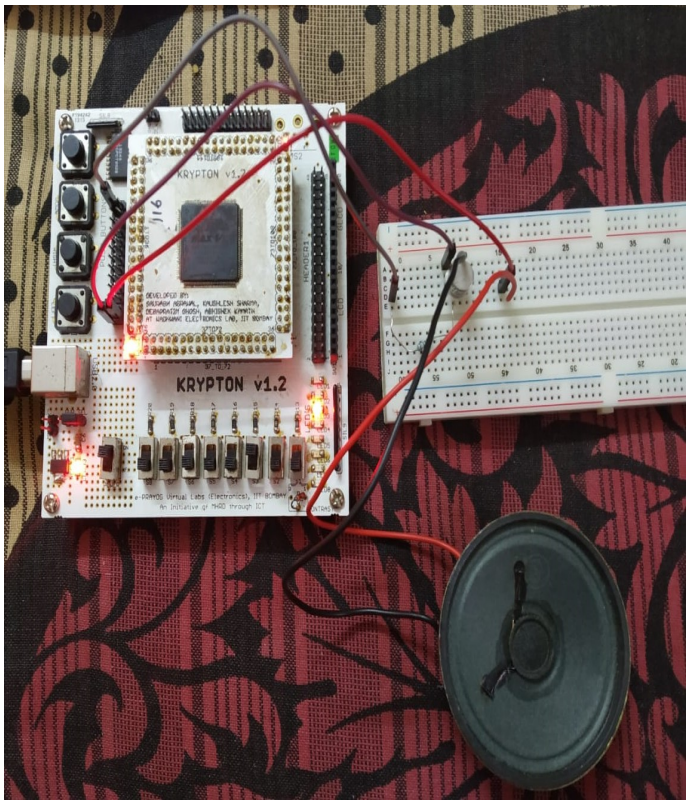
Pin Planner

Observations

Some of the observations were :



Observation 1



Observation 2

Observation 1 : Switch 6 was ON. LED 6 was glowing and Musical Note 'Dha' was audible.
Observation 2 : Switch 3 was ON. LED 3 was glowing and Musical Note 'Ga' was audible.

References

Clock Divider Tutorial by Teaching Assistant Mr. Sandesh Goyal
Quartus 20.1 Lite Software
EE214_Tone_Synthesizer.pdf for code snippets