

# Four Bit Adder Report

Mayur Ware, 19D070070

EE-214, WEL, IIT Bombay

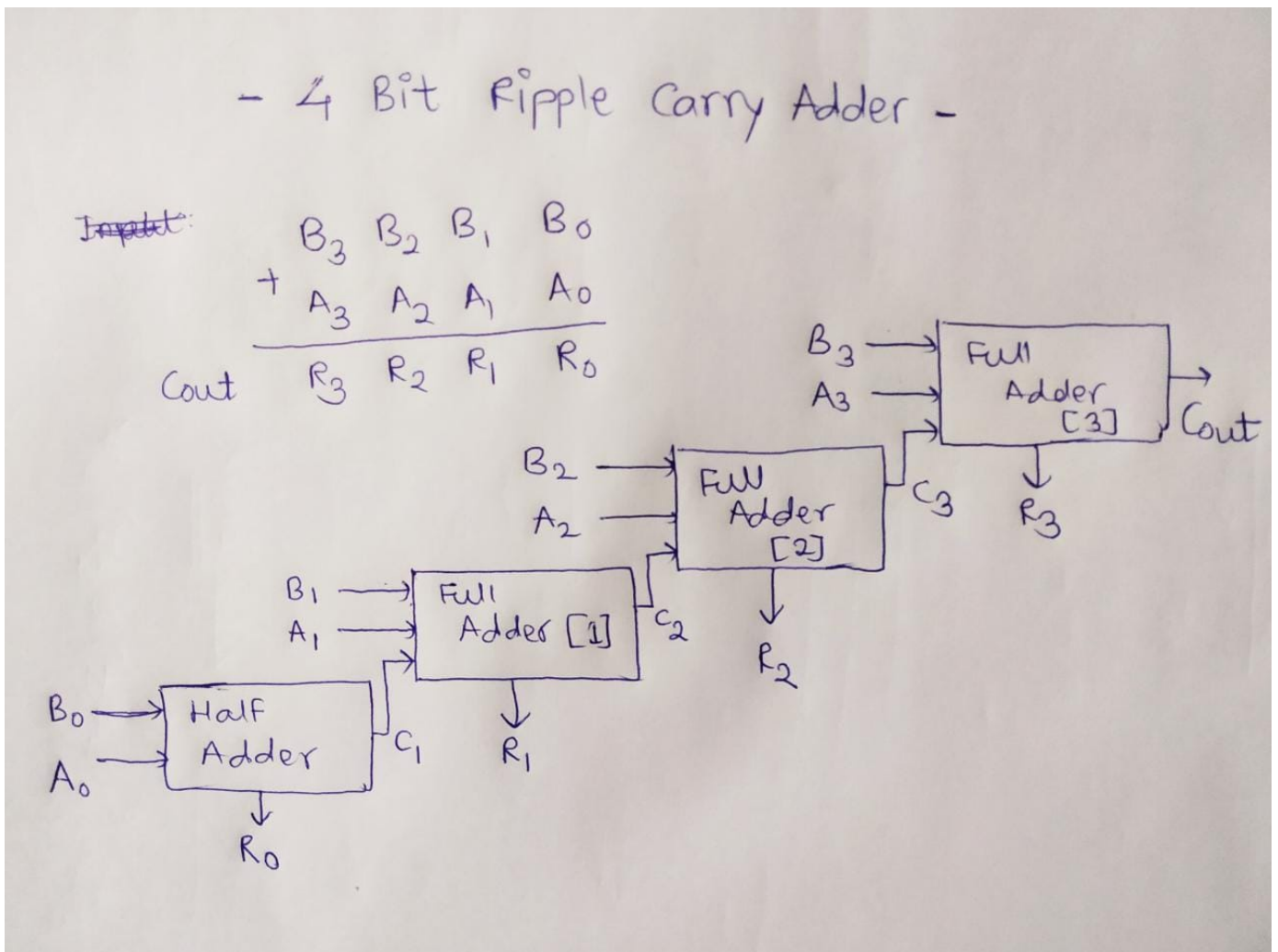
January 28, 2021

## Overview of the experiment

- The purpose of the experiment is to make a digital device which can add two 4 bit numbers and will return the 4 bit sum along with carry-out.
- I used Full\_Adder and Half\_Adder as components in a sequence to perform this experiment.
- The report contains a handmade diagram which describes my approach, some important extracts of VHDL code and the output waveforms.

## Approach to the experiment

I used 3 Full Adders and 1 Half Adder in the design which give the sum and send carry-out to the immediate next Adder. The sum bits will be the sum of the two numbers and the carry-out of the last Full Adder will be it's carry-out.



## Design document and VHDL code if relevant

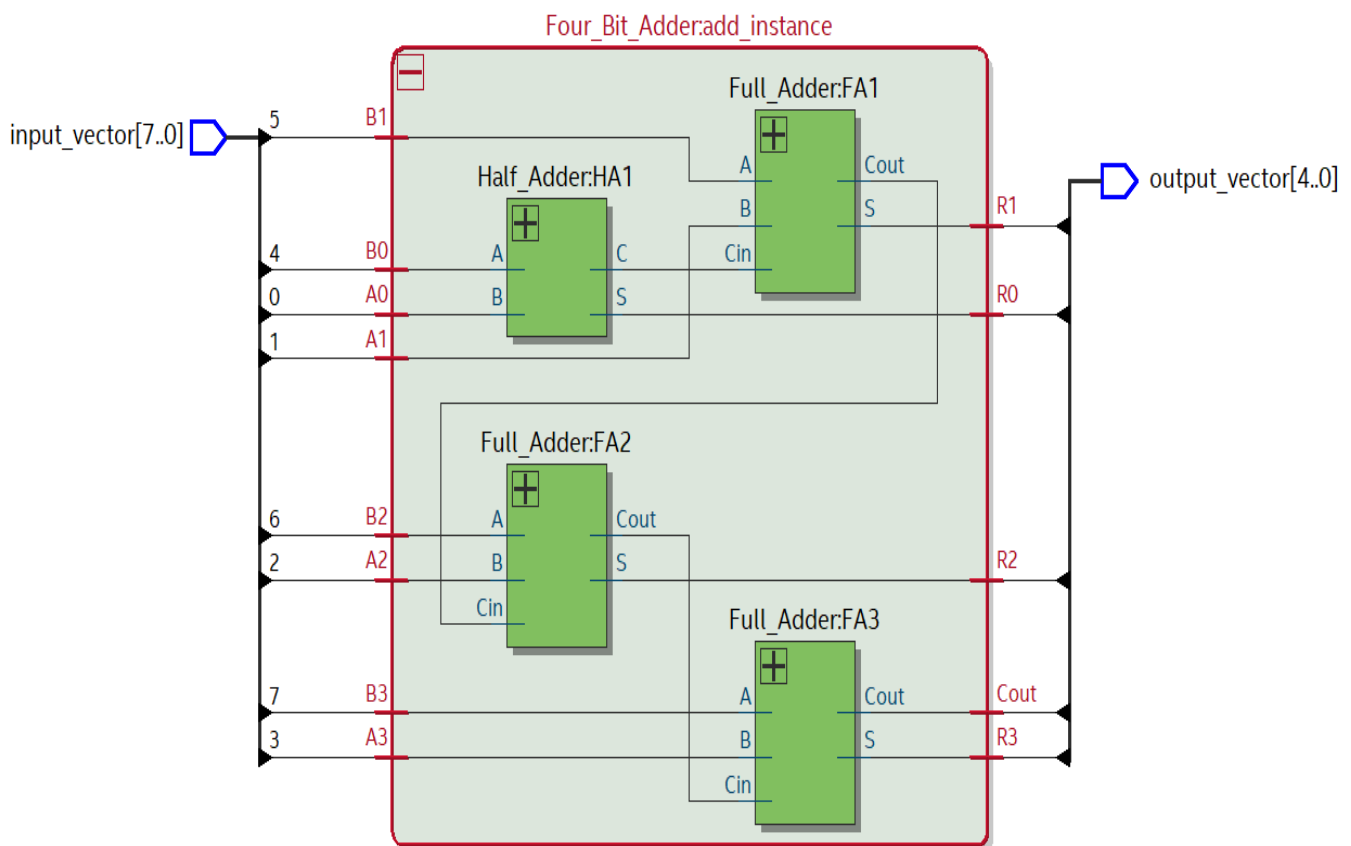
### Full\_Adder :

```
entity Full_Adder is
port (A, B, Cin: in std_logic; S, Cout: out std_logic);    --Assigned Ports
end entity Full_Adder;
architecture Equations of Full_Adder is
begin
S <= (A xor B) xor Cin;
Cout <= (A and B) or ((A or B) and Cin);
end Equations;
```

### Four\_Bit\_Adder :

```
entity Four_Bit_Adder is
port (B3, A3, B2, A2, B1, A1, B0, A0: in std_logic; R3, R2, R1, R0, Cout: out std_logic);    --Assigned Ports
end entity Four_Bit_Adder;
architecture Struct of Four_Bit_Adder is
signal C3, C2, C1: std_logic;
begin
HA1: Half_Adder port map (A => B0, B => A0, S => R0, C => C1);    --Half_Adder Instance
FA1: Full_Adder port map (A => B1, B => A1, Cin => C1, S => R1, Cout => C2);    --Full_Adder Instance
FA2: Full_Adder port map (A => B2, B => A2, Cin => C2, S => R2, Cout => C3);    --Full_Adder Instance
FA3: Full_Adder port map (A => B3, B => A3, Cin => C3, S => R3, Cout => Cout);    --Full_Adder Instance
end Struct;
```

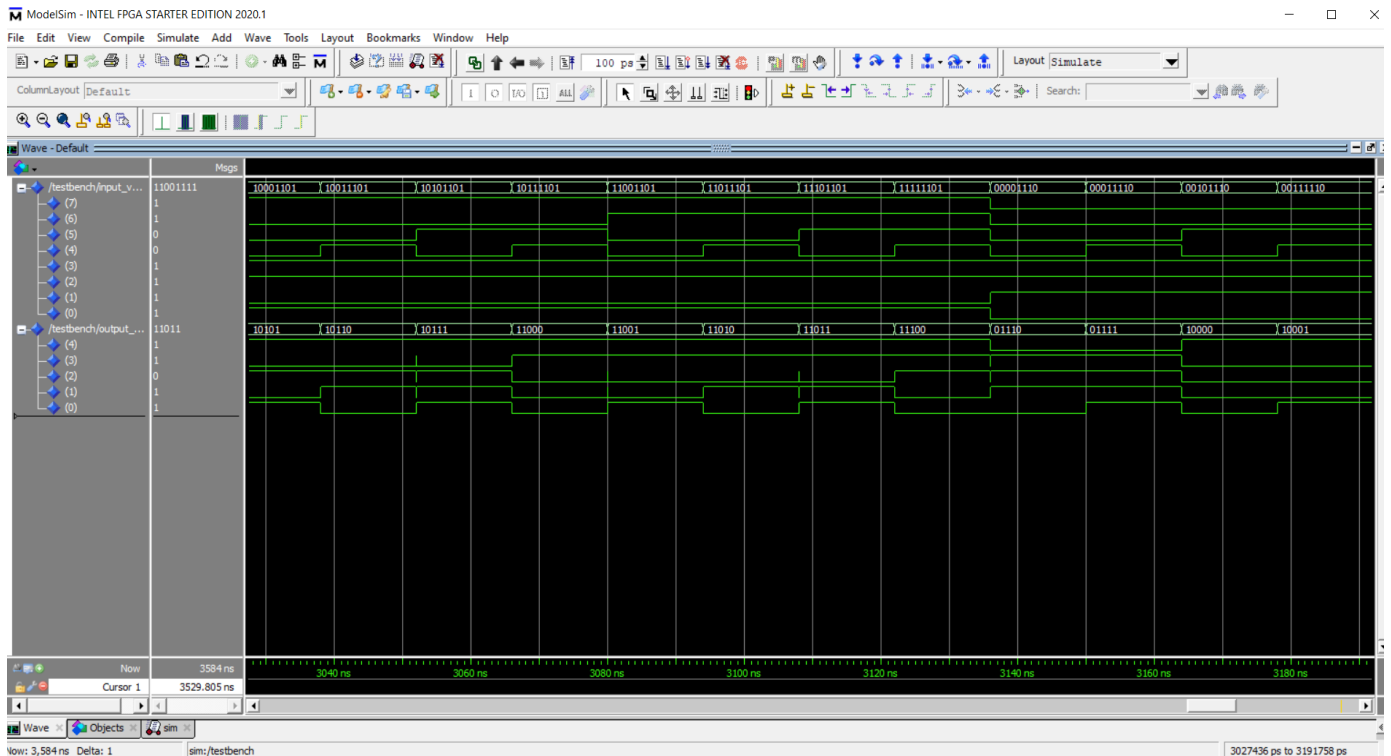
## RTL View



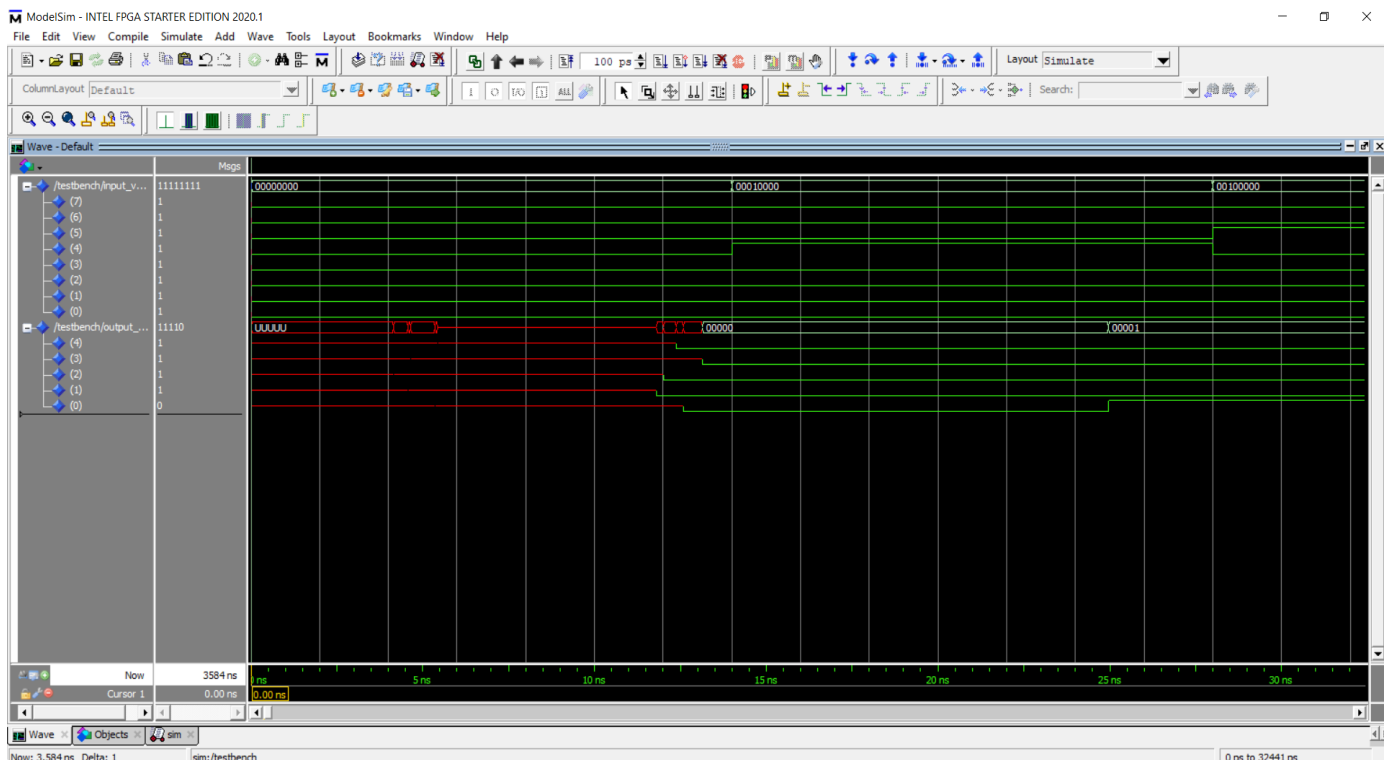
## DUT Input/Output Format

B3, A3, B2, A2, B1, A1, B0, A0: in std_logic;	--Input Bits
R3, R2, R1, R0, Cout: out std_logic);	--Output Bits
11101111    11101    11111	--Input Bits, Output Bits, Mask Bits

# RTL Simulation



# Gate-level Simulation



# Krypton board\*

Map the logic circuit to the Krypton board and attach the images of the pin assignment and output observed on the board (switches/LEDs).

# Observations\*

You must summarize your observations, either in words, using figures and/or tables.

# References

EE224 : Digital Design by Prof. Virendra Singh Video Lectures for understanding the design of 4 bit adder.

\* To be submitted after the tutorial on "Using Krypton."