EE214_Online Midsem Lab exam

Wadhwani Electronics Lab, IIT Bombay

Saturday 6th March, 2021

Duration: 2 hrs **Total Marks: 25**

Important instructions

1. This assignment is expected to be attempted using "structural style of modelling" only.
2. Spend enough time to make it compact so that it will be easy for you to describe and debug.
3. You are allowed to use only the components in **Gates.vhdl** and your **own** VHDL descriptions in the experiments/ homework problems so far.
4. Demonstrate your RTL and gate level simulation to your TA using the given tracefile for overall design. You are encouraged to break down your design conveniently (you may have to generate your own tracefiles for sub-parts) to demonstrate the working of the sub parts if necessary. This will help you get partial credits.

Uploading on moodle

1. There will be two submission links created for the midsem.
2. Your neatly handwritten/hand drawn design comprising of truth-tables, K-maps, Boolean equations, justifications for the boolean equations by inspection (as the case may be) to explain your approach along with the entities of the overall design and the decomposed components in a single zip file. **The upload link for the design will close after 45 mins after commencement of the exam.**
3. After successful demonstration, upload your project files in a single zipped file. **Submission of project files without demo will not be considered for evaluation.**

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1. Design the logic circuit to meet the specifications as follows (Refer the block schematic on Page 2):
   (a) The circuit has two four bit inputs A(a3a2a1a0) and B(b3b2b1b0) and six bits: $Y(y_5y_4y_3y_2y_1y_0)$ represent the output Y. The Tracefile format is : $A_3A_2A_1A_0B_3B_2B_1B_0 < space > Y_5Y_4Y_3Y_2Y_1Y_0 < space > 111111$
   (b) The unused most significant bits of the output should be made 0 as the case may be.
   (c) Design blocks MUL 3, ADD AB, DCR A, XOR AB, and MUX for the functionalities described as follows:
   - MUL 3: This block performs multiplication by 3 with A iff any two consecutive bits of the A are 1 else it outputs 0000. Marks: 3
   - ADD AB: This block performs addition of A , B. Marks: 1
   - DCR A: This block generates decrements A by 1. Marks: 2
   - XOR AB: This block performs bit-wise ex-OR operation between A and B. Marks: 1
   - MUX: selects one of $(I_0, I_1, I_2 and I_3)$ depending on the select lines S_1 and S_0) to the output Y. Note that I_0, I_1, I_2, I_3 and Y are all 6-bit wide. Marks: 2
   - **Note:** b_1, b_0 form the select lines of the multiplexer and are also the LSBs of the input B.
2. Upload the design (comprising of truth tables, K-maps, logic equations, block diagram) and the entities of the components you will use in your design along with the top level entity.
3. Write VHDL description for these blocks. Marks: 12
4. Demonstrate the RTL and Gate Level simulation for **complete** design to your TA using the generic Testbench and the given Tracefile. Marks: 4
5. Upload the zipped Quartus project on the moodle link.

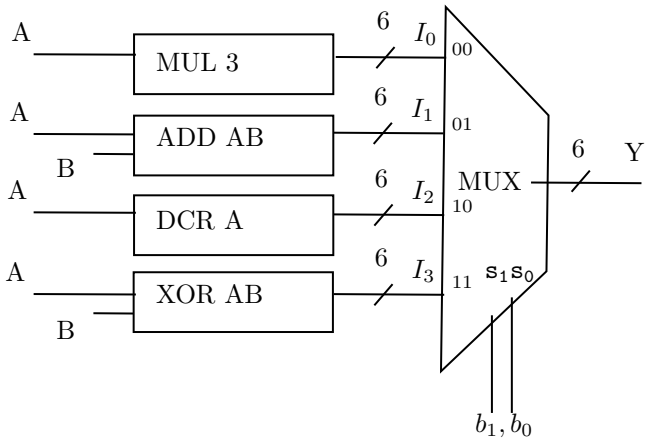

Figure 1: This is a simple block diagram for your understanding.