EE214: Homework

Wadhwani Electronics Lab, IIT Bombay

Thursday 4$^{\text{th}}$ February, 2021

Please complete the following assignments before your next lab turn.

1. Revise logic design using K maps, binary and BCD arithmetic circuits.

2. Revise Prof Virendra Singh's lecture no 6 and 22A. Prof Dinesh Sharma's lecture on 21/1/2021 will help to understand BCD addition clearly.

3. Write the VHDL description of a 2-1 multiplexer as shown in figure below. Write the tracefile to test all possible combinations of inputs.
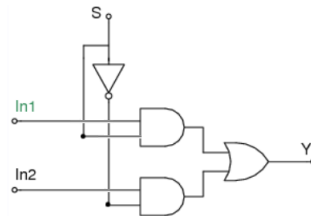
Figure 1: 2-1 Multiplexer

4. Using this MUX as a component, design a 2bit multiplexer. The truthtable and the block diagram of the required multiplexer is given below.

S	Y1	Y0
0	A1	A0
1	B1	B0

(Truth table)

Note: A1A0 and B1B0 are two 2-bit inputs
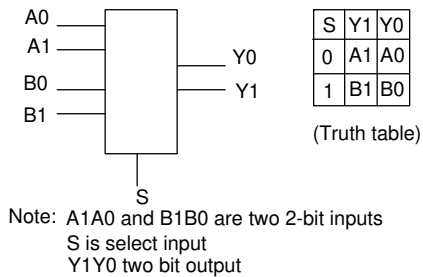S is select input
Y1Y0 two bit output

Figure 2: 2 Bit Multiplexer

5. Simulate it using the generic test bench and check the correctness of your description.

6. Generate the .svf file for this design lines.

7. Use the on-board switches and LEDs appropriately to demonstrate the working of your design..

8. Be ready with the demo for this design before next lab session

9. You will be required to use similar design in the next week's Lab.