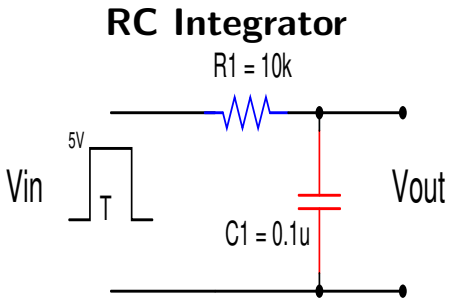
EE230 : Analog Circuits Lab

Mayur Ware | **19D070070**, Section 6

Experiment 1: Familiarization with NGSPICE Circuit Simulator and Lab Equipment

July 31, 2021

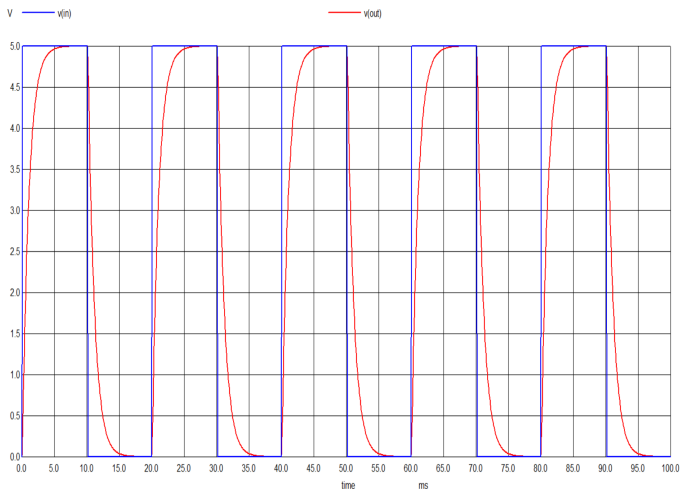
NGSPICE Simulation of RC and RLC Circuits



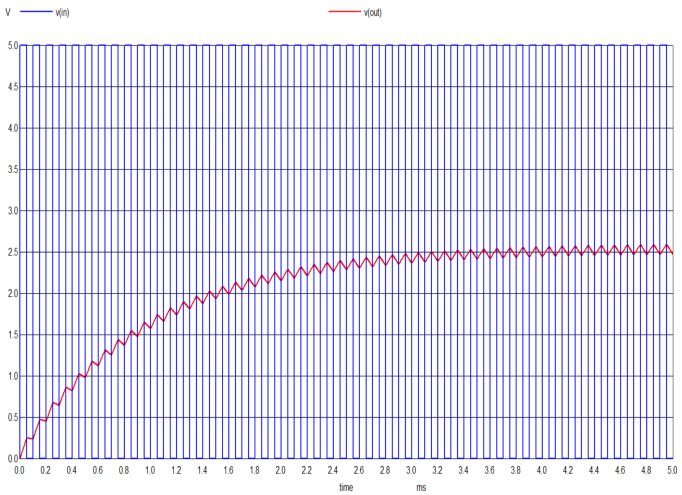
Integrator.CIR :

```
RC Integrator Circuit [Mayur Ware, 19D070070]
*Resistor connected between In and Out
R1 In Out 10k
*Capacitor connected between Out and GND
C1 Out GND 0.1u
*Voltage Source between In and GND
Vin In GND pulse(0 5 0 0 0 10m 20m)
.tran 0.1m 100m
*Control Commands
.control
run
set color0 = white
set color1 = black
set color2 = blue
set color3 = red
set xbrushwidth = 2
plot V(In) V(Out)
.endc
.end
```

Plots :



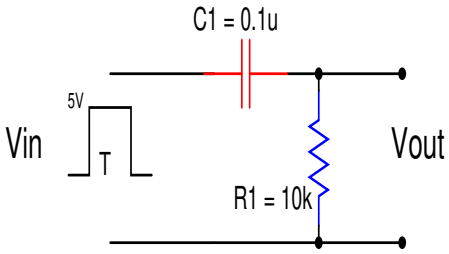
Case 1 : $\mathbf{T = 10}\ \tau$



Case 2 : $T = \mathbf{0.05}\ \tau$

As, we can notice, V_{Out} is settling properly in Case 1, whereas it is not settling in Case 2 due to very low time period

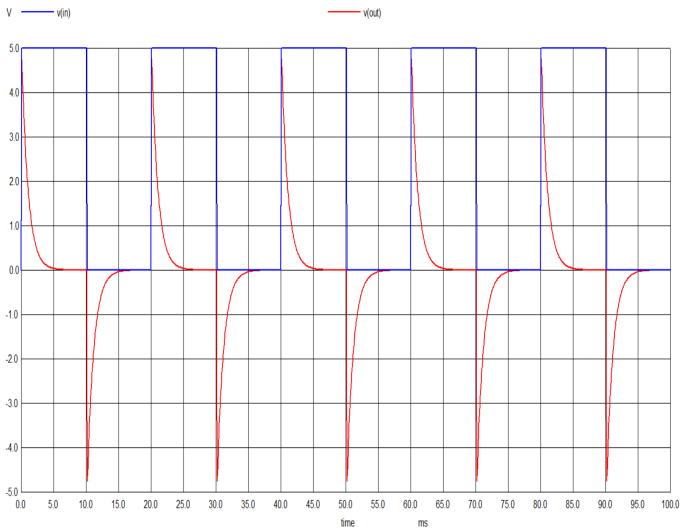
RC Differentiator



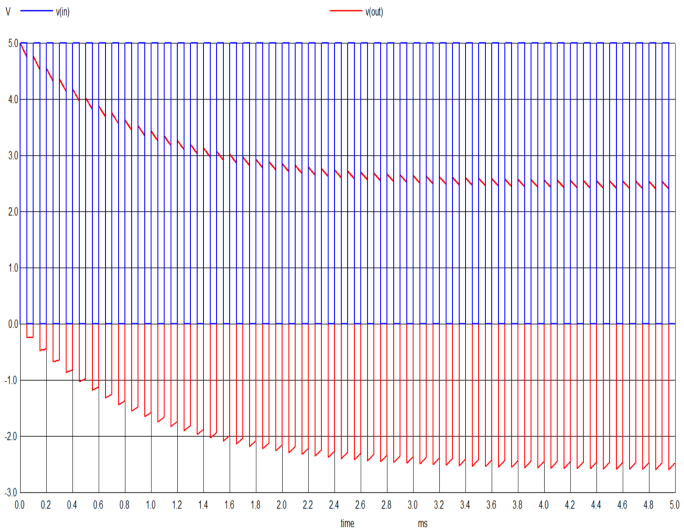
Differentiator.CIR :

```
RC Differentiator Circuit [Mayur Ware, 19D070070]
*Capacitor connected between In and Out
C1 In Out 0.1u
*Resistor connected between Out and GND
R1 Out GND 10k
*Voltage Source between In and GND
Vin In GND pulse(0 5 0 0 0 10m 20m)
.tran 0.1m 100m
*Control Commands
.control
run
set color0 = white
set color1 = black
set color2 = blue
set color3 = red
set xbrushwidth = 2
plot V(In) V(Out)
.endc
.end
```

Plots :



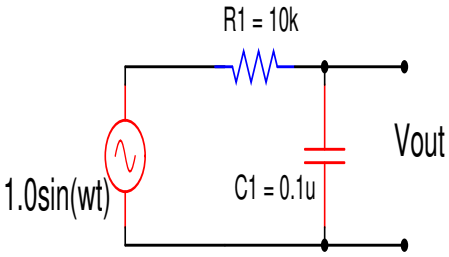
Case 1 : **T = 10** τ



Case 2 : T = **0.05** τ

As, we can notice, V_{Out} is settling properly in Case 1, whereas it is not settling in Case 2 due to very low time period

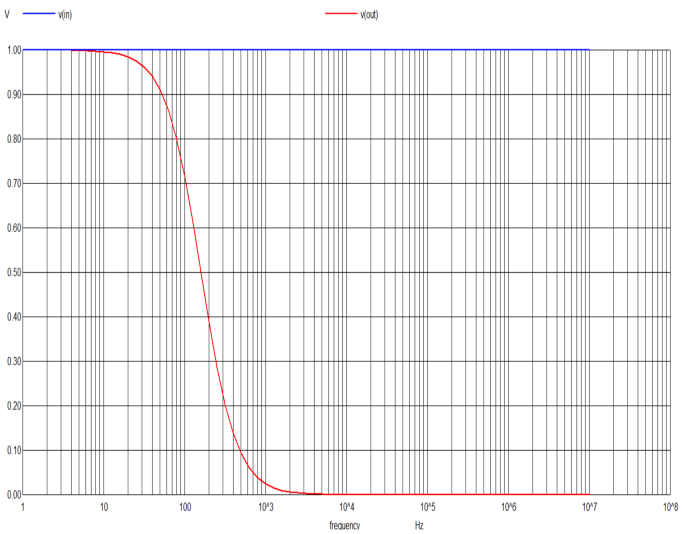
RC Lowpass Filter



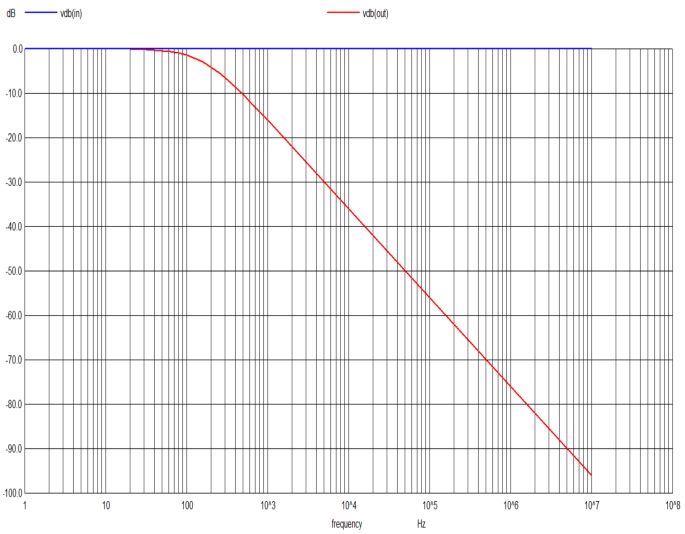
RC_Low.CIR :

```
RC Lowpass Filter Circuit [Mayur Ware, 19D070070]
*Resistor connected between In and Out
R1 In Out 10k
*Capacitor connected between Out and GND
C1 Out GND 0.1u
*Voltage Source between In and GND
Vin In GND dc 0 ac 1
.ac DEC 10 1 10e6
*Control Commands
.control
run
set color0 = white
set color1 = black
set color2 = blue
set color3 = red
set xbrushwidth = 2
plot Vdb(In) Vdb(Out)
.endc
.end
```

Plots :

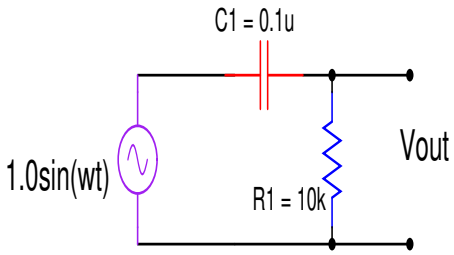


Case 1 : Frequency without log scale



Case 2 : Frequency in log scale

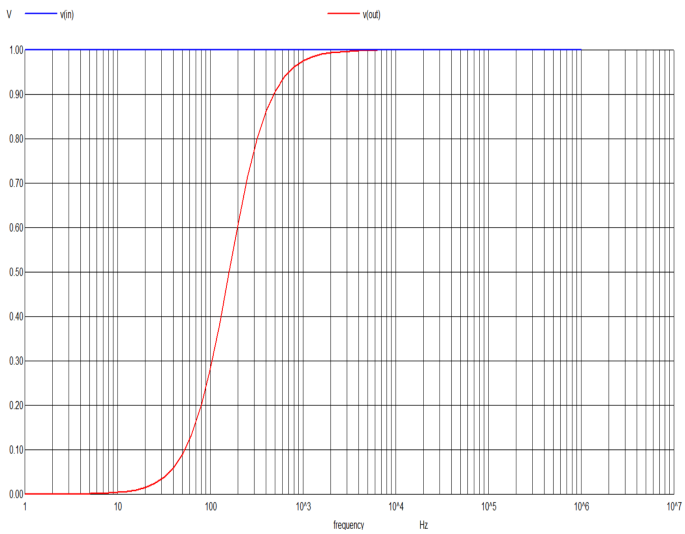
RC Highpass Filter



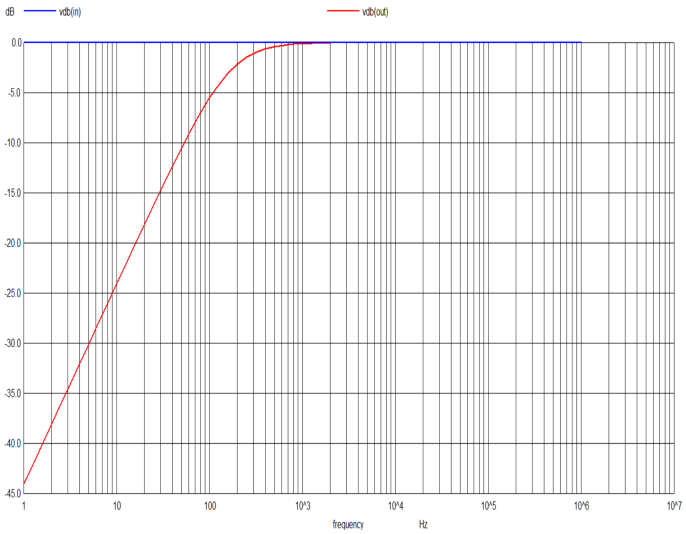
RC_High.CIR :

```
RC Highpass Filter Circuit [Mayur Ware, 19D070070]
*Capacitor connected between In and Out
C1 In Out 0.1u
*Resistor connected between Out and GND
R1 Out GND 10k
*Voltage Source between In and GND
Vin In GND dc 0 ac 1
.ac DEC 10 1 10e5
*Control Commands
.control
run
set color0 = white
set color1 = black
set color2 = blue
set color3 = red
set xbrushwidth = 2
plot V(In) V(Out)
.endc
.end
```

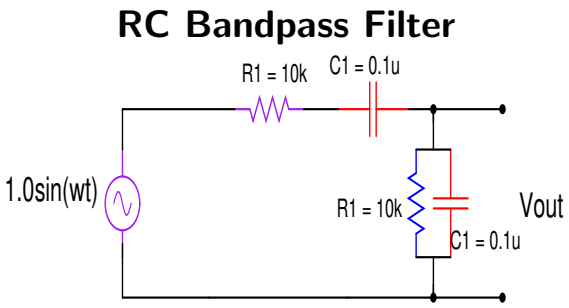
Plots :



Case 1 : Frequency without log scale



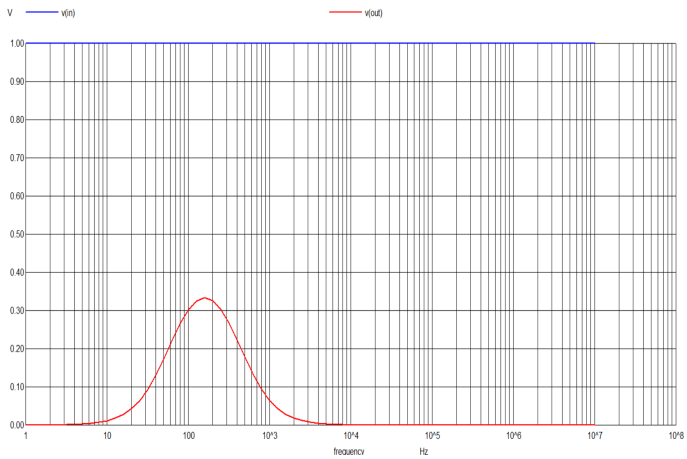
Case 2 : Frequency in log scale



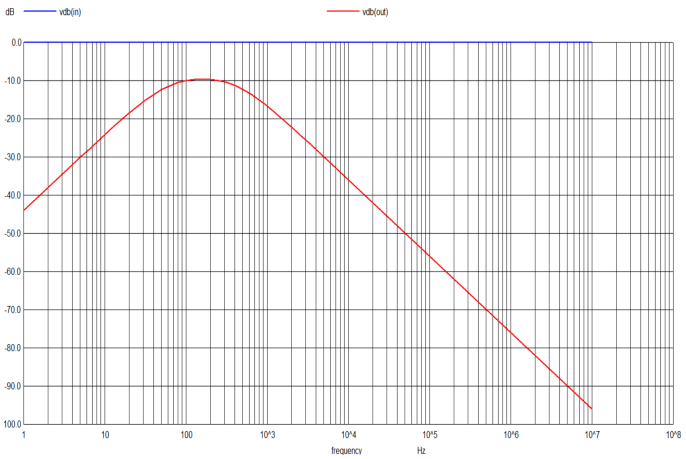
RC_Bandpass.CIR :

```
RC Bandpass Filter Circuit [Mayur Ware, 19D070070]
*Resistor connected between In and Out
R1 In Mid 10k
*Capacitor connected between Out and GND
C1 Mid Out 0.1u
*Parallel RC Components
R2 Out GND 10k
C2 Out GND 0.1u
*Voltage Source between In and GND
Vin In GND dc 0 ac 1
.ac DEC 10 1 10e5
*Control Commands
.control
run
set color0 = white
set color1 = black
set color2 = blue
set color3 = red
set xbrushwidth = 2
plot Vdb(In) Vdb(Out)
meas ac peak MAX vmag(Out)
meas ac fpeak WHEN vmag(Out)=peak
let f3db = peak/sqrt(2)
meas ac f1 WHEN vmag(Out)=f3db RISE=1
meas ac f2 WHEN vmag(Out)=f3db FALL=1
.endc
.end
```

Plots :



Case 1 : Frequency without log scale

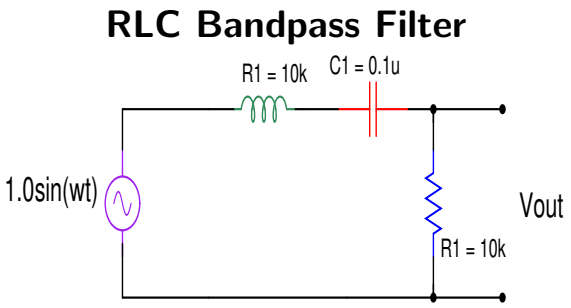


Case 2 : Frequency in log scale

Transfer Function for this circuit is $\frac{1000s}{s^2+3000s+10^6}$. By comparing it with $\frac{a_1 s}{s^2+\frac{\omega}{Q}s+\omega^2}$ where Upper and Lower -3dB frequencies $= \omega_1, \omega_2 = \omega_0\sqrt{1+\frac{1}{4Q^2}} \pm \frac{\omega_0}{2Q}$ and Center-frequency gain $= \frac{a_1 Q}{\omega_0}$

Theoretical Results : Centre Frequency (f_0) = 159.15 Hz, Lower Frequency (f_L) = 47.74 Hz and Upper Frequency (f_H) = 525.51 Hz

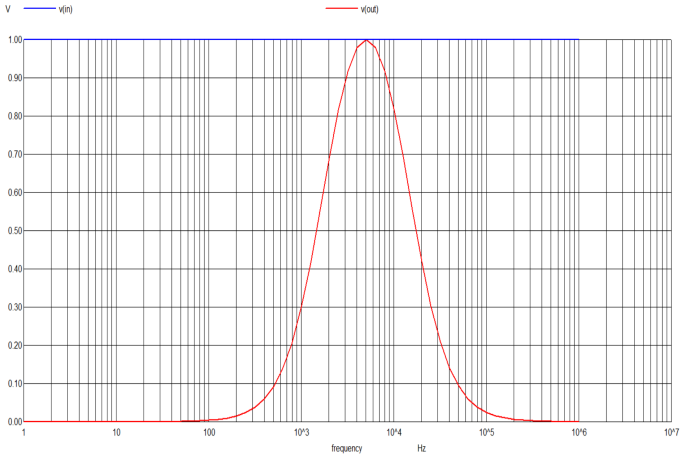
Simulation Results : = Centre Frequency (f_0) = 1.584891e+02, Lower Frequency (f_L) = 4.838534e+01 and Upper Frequency (f_H) = 5.276607e+02



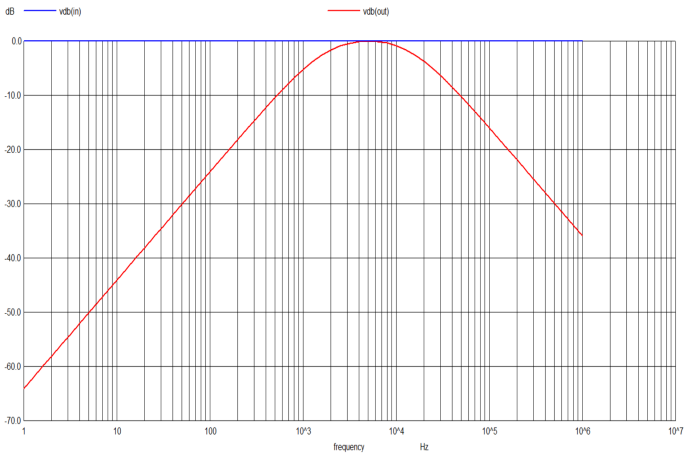
RLC_Bandpass.CIR :

```
RLC Bandpass Filter Circuit [Mayur Ware, 19D070070]
*Resistor connected between In and Mid
L1 In Mid 10m
*Capacitor connected between Out and GND
C1 Mid Out 0.1u
*Resistor connected between Out and GND
R1 Out GND 1k
*Voltage Source between In and GND
Vin In GND dc 0 ac 1
.ac DEC 10 1 10e7
*Control Commands
.control
run
set color0 = white
set color1 = black
set color2 = blue
set color3 = red
set xbrushwidth = 2
*plot Vdb(In) Vdb(Out)
meas ac peak MAX vmag(Out)
meas ac fpeak WHEN vmag(Out)=peak
let f3db = peak/sqrt(2)
meas ac f1 WHEN vmag(Out)=f3db RISE=1
meas ac f2 WHEN vmag(Out)=f3db FALL=1
.endc
.end
```

Plots :



Case 1 : Frequency without log scale



Case 2 : Frequency in log scale

Transfer Function for this circuit is $\frac{10^5 s}{s^2+10000s+10^9}$. By comparing it with $\frac{a_1 s}{s^2+\frac{\omega}{Q}s+\omega^2}$ where Upper and Lower -3dB frequencies $= \omega_1, \omega_2 = \omega_0\sqrt{1+\frac{1}{4Q^2}} \pm \frac{\omega_0}{2Q}$ and Center-frequency gain $= \frac{a_1 Q}{\omega_0}$

Theoretical Results : Center Frequency (f_0) = 174605.15 Hz, Lower Frequency (f_L) = 1475.98 Hz and Upper Frequency (f_H) = 17460.64 Hz

Simulation Results : = Center Frequency (f_0) = 1.74611e+05, Lower Frequency (f_L) = 1.468642e+03 and Upper Frequency (f_H) = 1.745991e+04

• **Major Learnings from this Experiment :**
- Circuit simulations using NGSpice Software
- Introduction of Lab Equipments
- XCircuit Software for Circuit Drawing
- Various RC and RLC Filter Circuits

• **Challenges faced :**
- Unfamilarities with NGSpice Syntax
- Calculation of Center, Upper and Lower -3dB Frequencies

• **Questions or Clarifications (if any) :**
None

References

WEL Resources for NGSpice