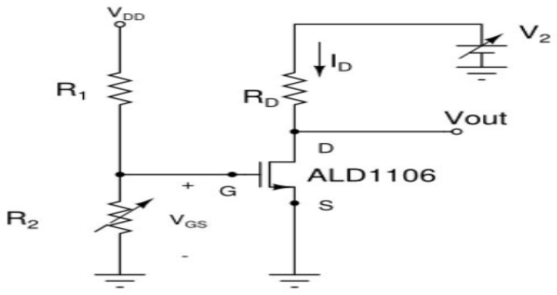
EE230 : Analog Circuits Lab

Mayur Ware | 19D070070, **Section 6**

Experiment 5 : NMOS Output Characteristics

August 29, 2021

NMOS Output Characteristics




```
Mayur Ware | 19D070070
*NMOS Output Characteristics
.model NXYAA5U nmos Level=1 Vto=0.7 KP=80u w=14.8u L=1u
+ Gamma=0 Phi=0.65 Lambda=0.0
*Voltage Sources
V1 B D 0
V2 A GND 1
VGS G GND 2
*NMOS
M1 D G GND GND NXYAA5U
*Resistor
RD A B 2.2k
*Control Commands
.control
dc V2 0 50 0.2 VGS 2 5 1
run
plot i(V1)
.endc
.end
```

Simulation Results :

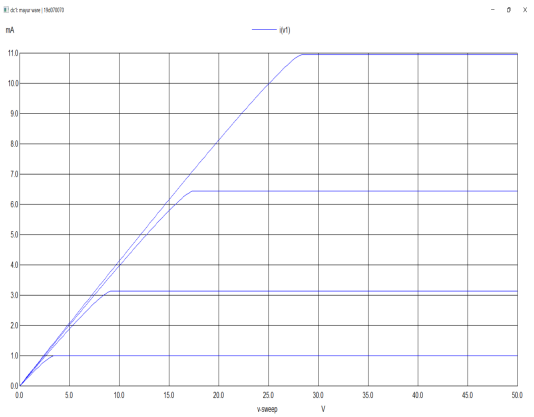
For different values of V_{GS}, we get different values of I_{DS}

1) For $V_{GS} = 2$V, $I_{DS} = 1.02$mA

2) For $V_{GS} = 3$V, $I_{DS} = 3.12$mA

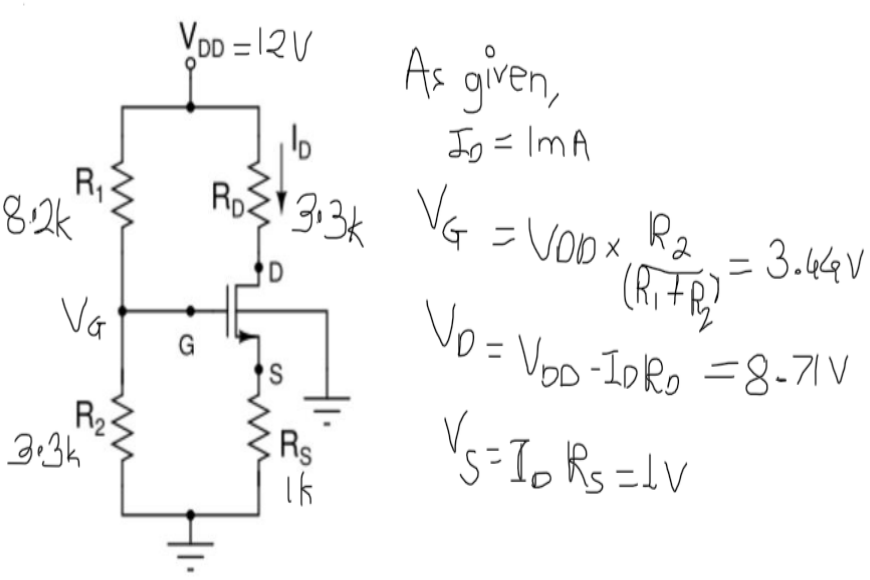
3) For $V_{GS} = 4$V, $I_{DS} = 6.51$mA

4) For $V_{GS} = 5$V, $I_{DS} = 10.98$mA



I learned variation of I_{DS} with V_{GS} and V_{DS}

NMOS Common-Source Amplifier (Bias Circuit)
Biasing Analysis

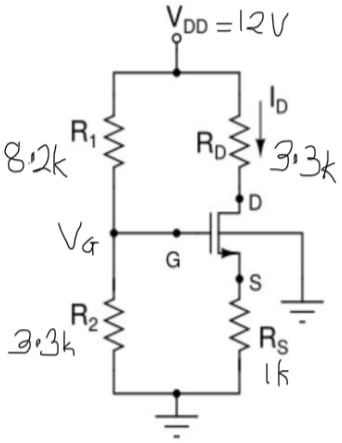



```
Mayur Ware | 19D070070
*Common Source Amplifier
.model NXYAA5U nmos Level =1 Vto =1 KP =100 u w=10u L=1u
+ Gamma =0 Phi =0.65 Lambda =0.01
*Voltage Sources
VDD DD 0 dc 12V
VDS Out D dc 0V
Vin In 0 sin (0 50m 1k 0 0)
*Resistances
R1 DD G 8.2k
R2 G 0 3.3k
Rd DD Out 3.3k
Rs S 0 1k
*Capacitors
C1 G In 10u
Cs S 0 100u
*NMOS
M1 D G S 0 NXYAA5U

.tran 0.1u 3m
.control
run
set color0 = white
set color1 = black
set color2 = blue
set color3 = red
print i(VDS) V(G) V(S) V(D)
.endc
.end
```

Simulation Results : i(VDS) = 1.011256mA
V(G) = 3.442654V
V(S) = 1.011256V
V(D) = 8.643329V

NMOS Common-Source Amplifier (Bias Circuit)
Gain Analysis



Assuming,
$I_D = 1mA$
$V_A = 100V$
So,
$g_m = \sqrt{2\mu_n C_{ox} \left(\frac{W}{L}\right) I_D} = 1.414m$ mho
$r_o = \frac{V_A}{I_D} = 100k\Omega$
$Gain = -g_m (R_D \| r_o) = -4.52$

```
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*Common Source Amplifier
.model NXYAA5U nmos Level =1 Vto =1 KP =100 u w=10u L=1u
+ Gamma =0 Phi =0.65 Lambda =0.01
*Voltage Sources
VDD DD 0 dc 12V
VDS Out D dc 0V
Vin In 0 sin (0 50m 1k 0 0)
*Resistances
R1 DD G 8.2k
R2 G 0 3.3k
Rd DD Out 3.3k
Rs S 0 1k
*Capacitors
C1 G In 10u
Cs S 0 100u
*NMOS
M1 D G S 0 NXYAA5U
.tran 0.1u 3m
.control
run
meas tran a pp v(Out)
meas tran b pp v(In)
gain = -1*a/b
print gain
.endc
.end
```
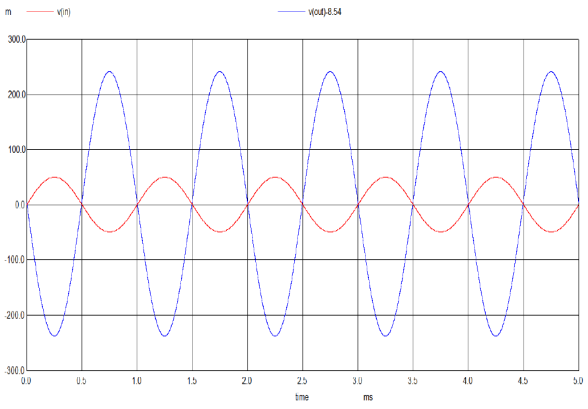
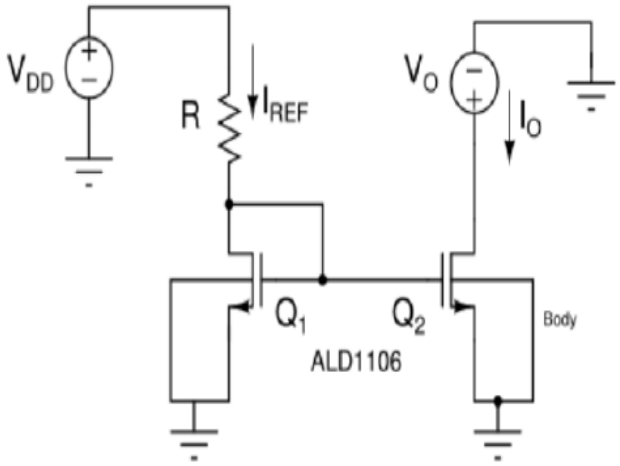
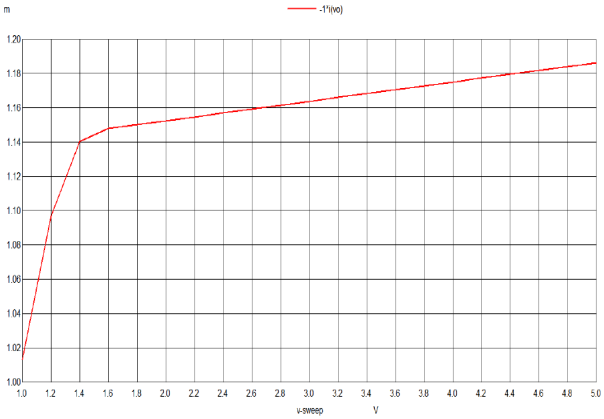



I learned about how to calculate the biasing conditions of a common source amplifier and how to do the small signal analysis for the same.

NMOS Current Mirror based Current Source




```
Mayur Ware | 19D070070
*NMOS Current Mirror
.model NXYAA5U nmos Level =1 Vto =1 KP =100 u w=10u L=1u
+ Gamma =0 Phi =0.65 Lambda =0.01
*Voltage Sources
VDD DD 0 dc 12V
VO D 0 dc 1V
*Resistances
R DD G 8.2k
*NMOS
M1 G G 0 0 NXYAA5U
M2 D G 0 0 NXYAA5U

.dc Vo 1V 5V 0.2V
.control
run
print i(VDD) i(VO)
plot i(VO)
.endc
.end
```



I learned how a current mirror is created using NMOS

References

1) Lecture Slides
2) Sedra-Smith
3) WEL Resources for NGSpice