EXERCISES

2.18 Consider a symmetrical square wave of 20-V peak-to-peak, 0 average, and 2-ms period applied to a Miller integrator. Find the value of the time constant CR such that the triangular waveform at the output has a 20-V peak-to-peak amplitude.
Ans. 0.5 ms

D2.19 Use an ideal op amp to design an inverting integrator with an input resistance of 10 kΩ and an integration time constant of 10^{-3} s. What is the gain magnitude and phase angle of this circuit at 10 rad/s and at 1 rad/s? What is the frequency at which the gain magnitude is unity?
Ans. $R = 10$ kΩ, $C = 0.1$ μF; at $\omega = 10$ rad/s: $|V_o/V_i| = 100$ V/V and $\phi = +90°$; at $\omega = 1$ rad/s: $|V_o/V_i| = 1000$ V/V and $\phi = +90°$; 1000 rad/s

D2.20 Design a differentiator to have a time constant of 10^{-2} s and an input capacitance of 0.01 μF. What is the gain magnitude and phase of this circuit at 10 rad/s, and at 10^3 rad/s? In order to limit the high-frequency gain of the differentiator circuit to 100, a resistor is added in series with the capacitor. Find the required resistor value.
Ans. $C = 0.01$ μF; $R = 1$ MΩ; at $\omega = 10$ rad/s: $|V_o/V_i| = 0.1$ V/V and $\phi = -90°$; at $\omega = 1000$ rad/s: $|V_o/V_i| = 10$ V/V and $\phi = -90°$; 10 kΩ

2.6 DC Imperfections

Thus far we have considered the op amp to be ideal. The only exception has been a brief discussion of the effect of the op-amp finite gain A on the closed-loop gain of the inverting and noninverting configurations. Although in many applications the assumption of an ideal op amp is not a bad one, a circuit designer has to be thoroughly familiar with the characteristics of practical op amps and the effects of such characteristics on the performance of op-amp circuits. Only then will the designer be able to use the op amp intelligently, especially if the application at hand is not a straightforward one. The nonideal properties of op amps will, of course, limit the range of operation of the circuits analyzed in the previous examples.

In this and the two sections that follow, we consider some of the important nonideal properties of the op amp.[4] We do this by treating one nonideality at a time, beginning in this section with the dc problems to which op amps are susceptible.

2.6.1 Offset Voltage

Because op amps are direct-coupled devices with large gains at dc, they are prone to dc problems. The first such problem is the dc offset voltage. To understand this problem consider

[4]We should note that real op amps have nonideal effects additional to those discussed in this chapter. These include finite (nonzero) common-mode gain or, equivalently, noninfinite CMRR, noninfinite input resistance, and nonzero output resistance. The effect of these, however, on the performance of most of the closed-loop circuits studied here is not very significant, and their study will be postponed to later chapters (in particular, Chapters 9, 10, and 13).

the following *conceptual* experiment: If the two input terminals of the op amp are tied together and connected to ground, it will be found that despite the fact that $v_{Id} = 0$, a finite dc voltage exists at the output. In fact, if the op amp has a high dc gain, the output will be at either the positive or negative saturation level. The op-amp output can be brought back to its ideal value of 0 V by connecting a dc voltage source of appropriate polarity and magnitude between the two input terminals of the op amp. This external source balances out the input offset voltage of the op amp. It follows that the **input offset voltage** (V_{OS}) must be of equal magnitude and of opposite polarity to the voltage we applied externally.

The input offset voltage arises as a result of the unavoidable mismatches present in the input differential stage inside the op amp. In later chapters (in particular Chapters 9 and 13) we shall study this topic in detail. Here, however, our concern is to investigate the effect of V_{OS} on the operation of closed-loop op-amp circuits. Toward that end, we note that general-purpose op amps exhibit V_{OS} in the range of 1 mV to 5 mV. Also, the value of V_{OS} depends on temperature. The op-amp data sheets usually specify typical and maximum values for V_{OS} at room temperature as well as the temperature coefficient of V_{OS} (usually in μV/°C). They do not, however, specify the polarity of V_{OS} because the component mismatches that give rise to V_{OS} are obviously not known a priori; different units of the same op-amp type may exhibit either a positive or a negative V_{OS}.

To analyze the effect of V_{OS} on the operation of op-amp circuits, we need a circuit model for the op amp with input offset voltage. Such a model is shown in Fig. 2.28. It consists of a dc source of value V_{OS} placed in series with the positive input lead of an offset-free op amp. The justification for this model follows from the description above.

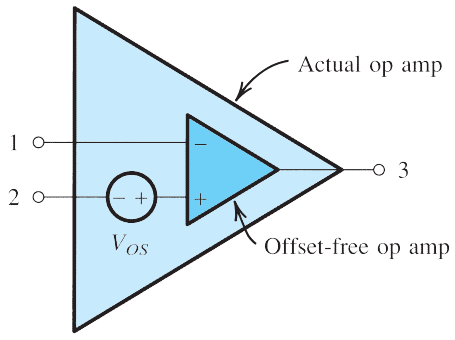

Figure 2.28 Circuit model for an op amp with input offset voltage V_{OS}.

EXERCISE

2.21 Use the model of Fig. 2.28 to sketch the transfer characteristic v_O versus v_{Id} ($v_O \equiv v_3$ and $v_{Id} \equiv v_2 - v_1$) of an op amp having an open-loop dc gain $A_0 = 10^4$ V/V, output saturation levels of ±10 V, and V_{OS} of +5 mV.

Ans. See Fig. E2.21. Observe that true to its name, the input offset voltage causes an offset in the voltage-transfer characteristic; rather than passing through the origin it is now shifted to the left by V_{OS}.

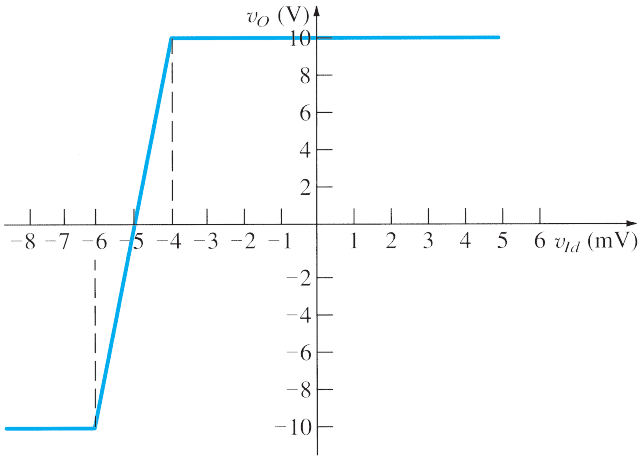

Figure E2.21 Transfer characteristic of an op amp with $V_{OS} = 5$ mV.

Analysis of op-amp circuits to determine the effect of the op-amp V_{OS} on their performance is straightforward: The input voltage signal source is short-circuited and the op amp is replaced with the model of Fig. 2.28. (Eliminating the input signal, done to simplify matters, is based on the principle of superposition.) Following this procedure, we find that both the inverting and the noninverting amplifier configurations result in the same circuit, that shown in Fig. 2.29, from which the output dc voltage due to V_{OS} is found to be

$$V_O = V_{OS}\left[1 + \frac{R_2}{R_1}\right] \tag{2.36}$$

This output dc voltage can have a large magnitude. For instance, a noninverting amplifier with a closed-loop gain of 1000, when constructed from an op amp with a 5-mV input offset voltage, will have a dc output voltage of +5 V or −5 V (depending on the polarity of V_{OS}) rather than the ideal value of 0 V. Now, when an input signal is applied to the amplifier, the corresponding signal output will be superimposed on the 5-V dc. Obviously then, the

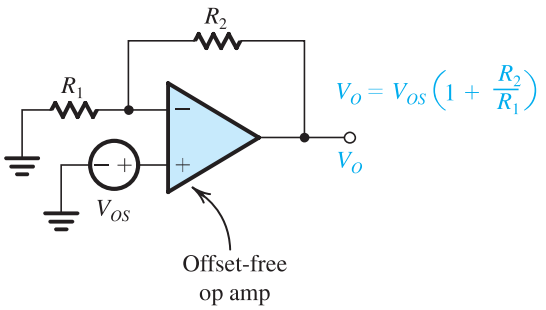

Figure 2.29 Evaluating the output dc offset voltage due to V_{OS} in a closed-loop amplifier.

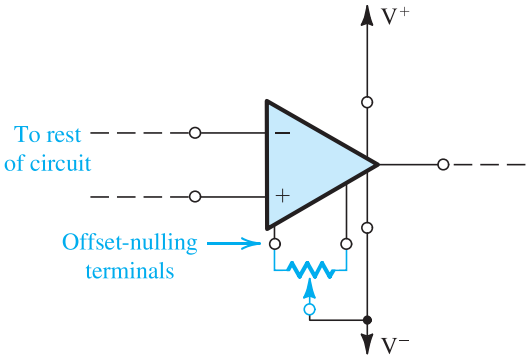

Figure 2.30 The output dc offset voltage of an op amp can be trimmed to zero by connecting a potentiometer to the two offset-nulling terminals. The wiper of the potentiometer is connected to the negative supply of the op amp.

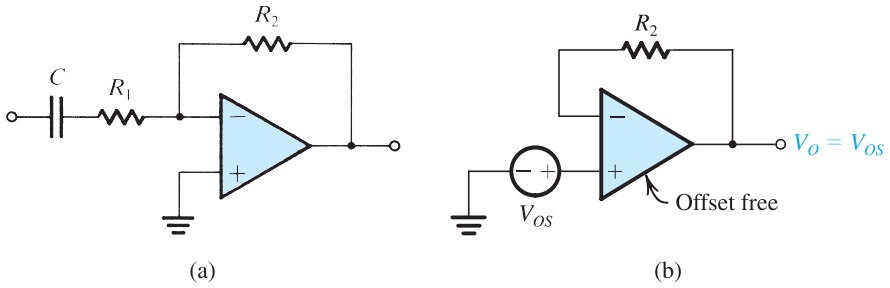

Figure 2.31 **(a)** A capacitively coupled inverting amplifier. **(b)** The equivalent circuit for determining its dc output offset voltage V_O.

allowable signal swing at the output will be reduced. Even worse, if the signal to be amplified is dc, we would not know whether the output is due to V_{OS} or to the signal!

Some op amps are provided with two additional terminals to which a specified circuit can be connected to trim to zero the output dc voltage due to V_{OS}. Figure 2.30 shows such an arrangement that is typically used with general-purpose op amps. A potentiometer is connected between the offset-nulling terminals with the wiper of the potentiometer connected to the op-amp negative supply. Moving the potentiometer wiper introduces an imbalance that counteracts the asymmetry present in the internal op-amp circuitry and that gives rise to V_{OS}. We shall return to this point in the context of our study of the internal circuitry of op amps in Chapter 13. It should be noted, however, that even though the dc output offset can be trimmed to zero, the problem remains of the variation (or drift) of V_{OS} with temperature.

One way to overcome the dc offset problem is by capacitively coupling the amplifier. This, however, will be possible only in applications where the closed-loop amplifier is not required to amplify dc or very-low-frequency signals. Figure 2.31(a) shows a capacitively coupled amplifier. Because of its infinite impedance at dc, the coupling capacitor will cause the gain to be zero at dc. As a result, the equivalent circuit for determining the dc output voltage resulting from the op-amp input offset voltage V_{OS} will be that shown in Fig. 2.31(b). Thus V_{OS} sees in effect a unity-gain voltage follower, and the dc output voltage V_O will be equal to V_{OS} rather than $V_{OS}(1 + R_2/R_1)$, which is the case without the coupling capacitor. As far as input signals are concerned, the coupling capacitor C forms together with R_1 an STC high-pass circuit with a corner frequency of $\omega_0 = 1/CR_1$. Thus the gain of the capacitively

coupled amplifier will fall off at the low-frequency end [from a magnitude of $(1 + R_2/R_1)$ at high frequencies] and will be 3 dB down at ω_0.

EXERCISES

2.22 Consider an inverting amplifier with a nominal gain of 1000 constructed from an op amp with an input offset voltage of 3 mV and with output saturation levels of ±10 V. (a) What is (approximately) the peak sine-wave input signal that can be applied without output clipping? (b) If the effect of V_{OS} is nulled at room temperature (25°C), how large an input can one now apply if: (i) the circuit is to operate at a constant temperature? (ii) the circuit is to operate at a temperature in the range 0°C to 75°C and the temperature coefficient of V_{OS} is 10 μV/°C?

Ans. (a) 7 mV; (b) 10 mV, 9.5 mV

2.23 Consider the same amplifier as in Exercise 2.22—that is, an inverting amplifier with a nominal gain of 1000 constructed from an op amp with an input offset voltage of 3 mV and with output saturation levels of ±10 V—except here let the amplifier be capacitively coupled as in Fig. 2.31(a). (a) What is the dc offset voltage at the output, and what (approximately) is the peak sine-wave signal that can be applied at the input without output clipping? Is there a need for offset trimming? (b) If $R_1 = 1$ kΩ and $R_2 = 1$ MΩ, find the value of the coupling capacitor C_1 that will ensure that the gain will be greater than 57 dB down to 100 Hz.

Ans. (a) 3 mV, 10 mV, no need for offset trimming; (b) 1.6 μF

2.6.2 Input Bias and Offset Currents

The second dc problem encountered in op amps is illustrated in Fig. 2.32. In order for the op amp to operate, its two input terminals have to be supplied with dc currents, termed the **input bias currents**.[5] In Fig. 2.32 these two currents are represented by two current sources, I_{B1} and I_{B2}, connected to the two input terminals. It should be emphasized that the input bias currents are independent of the fact that a real op amp has finite (though large) input resistance (not shown in Fig. 2.32). The op-amp manufacturer usually specifies the average value of I_{B1} and I_{B2} as well as their expected difference. The average value I_B is called the **input bias current**,

$$I_B = \frac{I_{B1} + I_{B2}}{2}$$

and the difference is called the **input offset current** and is given by

$$I_{OS} = |I_{B1} - I_{B2}|$$

Typical values for general-purpose op amps that use bipolar transistors are $I_B = 100$ nA and $I_{OS} = 10$ nA.

[5]This is the case for op amps constructed using bipolar junction transistors (BJTs). Those using MOSFETs in the first (input) stage do not draw an appreciable input bias current; nevertheless, the input terminals should have continuous dc paths to ground. More on this in later chapters.

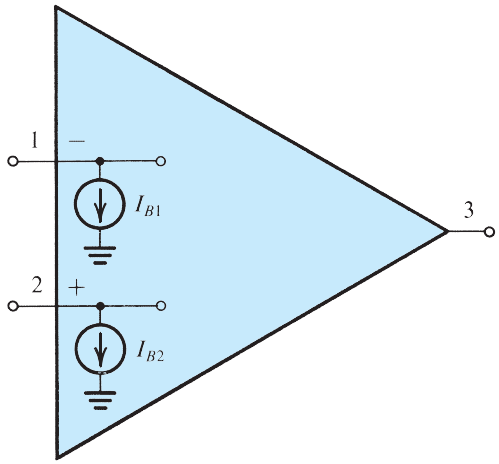

Figure 2.32 The op-amp input bias currents represented by two current sources I_{B1} and I_{B2}.

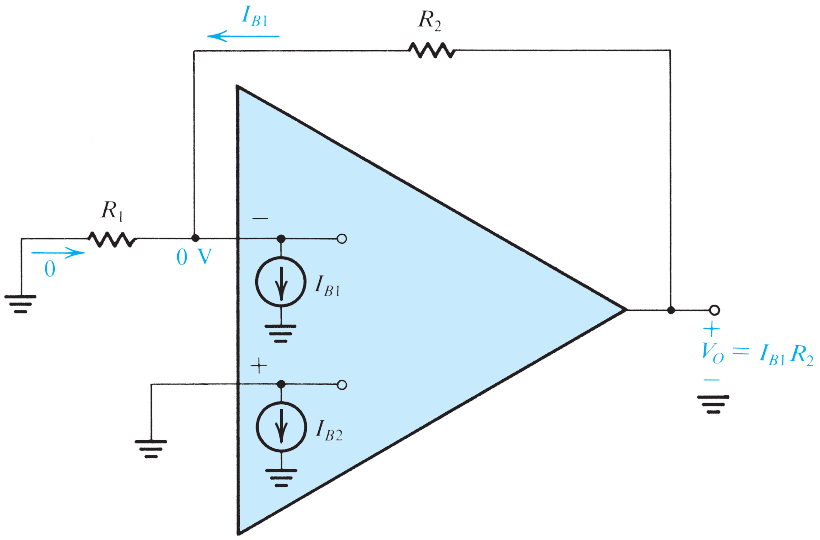

Figure 2.33 Analysis of the closed-loop amplifier, taking into account the input bias currents.

We now wish to find the dc output voltage of the closed-loop amplifier due to the input bias currents. To do this we ground the signal source and obtain the circuit shown in Fig. 2.33 for both the inverting and noninverting configurations. As shown in Fig. 2.33, the output dc voltage is given by

$$V_O = I_{B1}R_2 \simeq I_B R_2 \tag{2.37}$$

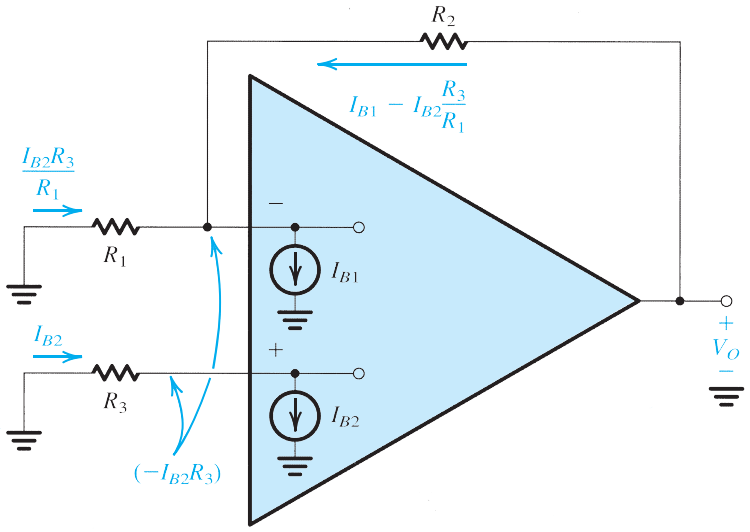

Figure 2.34 Reducing the effect of the input bias currents by introducing a resistor R_3.

This obviously places an upper limit on the value of R_2. Fortunately, however, a technique exists for reducing the value of the output dc voltage due to the input bias currents. The method consists of introducing a resistance R_3 in series with the noninverting input lead, as shown in Fig. 2.34. From a signal point of view, R_3 has a negligible effect (ideally no effect). The appropriate value for R_3 can be determined by analyzing the circuit in Fig. 2.34, where analysis details are shown, and the output voltage is given by

$$V_O = -I_{B2}R_3 + R_2(I_{B1} - I_{B2}R_3/R_1) \tag{2.38}$$

Consider first the case $I_{B1} = I_{B2} = I_B$, which results in

$$V_O = I_B[R_2 - R_3(1 + R_2/R_1)]$$

Thus we can reduce V_O to zero by selecting R_3 such that

$$R_3 = \frac{R_2}{1 + R_2/R_1} = \frac{R_1R_2}{R_1 + R_2} \tag{2.39}$$

That is, R_3 should be made equal to the parallel equivalent of R_1 and R_2.

Having selected R_3 as above, let us evaluate the effect of a finite offset current I_{OS}. Let $I_{B1} = I_B + I_{OS}/2$ and $I_{B2} = I_B - I_{OS}/2$, and substitute in Eq. (2.38). The result is

$$V_O = I_{OS}R_2 \tag{2.40}$$

which is usually about an order of magnitude smaller than the value obtained without R_3 (Eq. 2.37). We conclude that to minimize the effect of the input bias currents, one should *place in the positive lead a resistance equal to the equivalant* dc *resistance seen by the inverting terminal.* We emphasize the word *dc* in the last statement; note that if the amplifier is ac-coupled, we should select $R_3 = R_2$, as shown in Fig. 2.35.

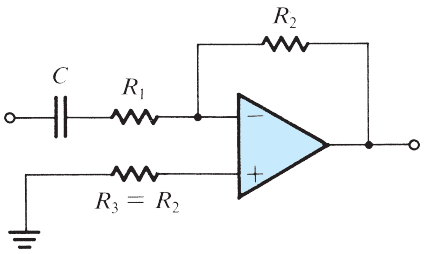

Figure 2.35 In an ac-coupled amplifier the dc resistance seen by the inverting terminal is R_2; hence R_3 is chosen equal to R_2.

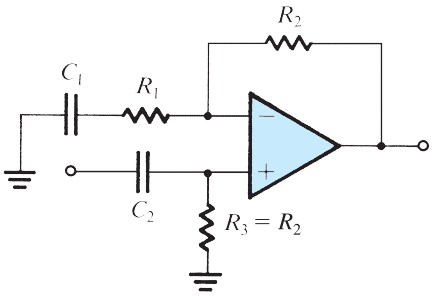

Figure 2.36 Illustrating the need for a continuous dc path for each of the op-amp input terminals. Specifically, note that the amplifier will *not* work without resistor R_3.

While we are on the subject of ac-coupled amplifiers, we should note that one must always provide a continuous dc path between each of the input terminals of the op amp and ground. This is the case no matter how small I_B is. For this reason the ac-coupled noninverting amplifier of Fig. 2.36 will *not* work without the resistance R_3 to ground. Unfortunately, including R_3 lowers considerably the input resistance of the closed-loop amplifier.

EXERCISE

2.24 Consider an inverting amplifier circuit designed using an op amp and two resistors, $R_1 = 10$ kΩ and $R_2 = 1$ MΩ. If the op amp is specified to have an input bias current of 100 nA and an input offset current of 10 nA, find the output dc offset voltage resulting and the value of a resistor R_3 to be placed in series with the positive input lead in order to minimize the output offset voltage. What is the new value of V_O?

Ans. 0.1 V; 9.9 kΩ (≃ 10 kΩ); 0.01 V

2.6.3 Effect of V_{OS} and I_{OS} on the Operation of the Inverting Integrator

Our discussion of the inverting integrator circuit in Section 2.5.2 mentioned the susceptibility of this circuit to saturation in the presence of small dc voltages or currents. It behooves us therefore to consider the effect of the op-amp dc offsets on its operation. As will be seen, these effects can be quite dramatic.

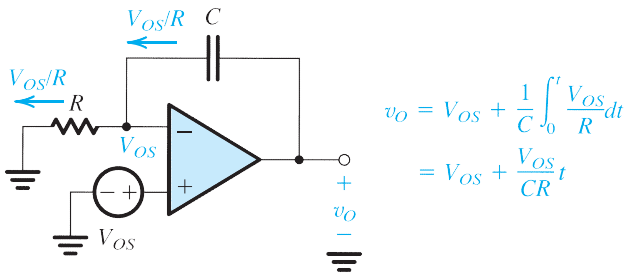

Figure 2.37 Determining the effect of the op-amp input offset voltage V_{OS} on the Miller integrator circuit. Note that since the output rises with time, the op amp eventually saturates.

To see the effect of the input dc offset voltage V_{OS}, consider the integrator circuit in Fig. 2.37, where for simplicity we have short-circuited the input signal source. Analysis of the circuit is straightforward and is shown in Fig. 2.37. Assuming for simplicity that at time $t = 0$ the voltage across the capacitor is zero, the output voltage as a function of time is given by

$$v_O = V_{OS} + \frac{V_{OS}}{CR}t \tag{2.41}$$

Thus v_O increases linearly with time until the op amp saturates—clearly an unacceptable situation! As should be expected, the dc input offset current I_{OS} produces a similar problem. Figure 2.38 illustrates the situation. Observe that we have added a resistance R in the op-amp positive-input lead in order to keep the input bias current I_B from flowing through C. Nevertheless, the offset current I_{OS} will flow through C and cause v_O to ramp linearly with time until the op amp saturates.

As mentioned in Section 2.5.2 the dc problem of the integrator circuit can be alleviated by connecting a resistor R_F across the integrator capacitor C, as shown in Fig. 2.25. Such a resistor provides a dc path through which the dc currents (V_{OS}/R) and I_{OS} can flow (assuming a resistance equal to $R \| R_F$ is connected in the positive op-amp lead), with the result that v_O will now have a dc component $[V_{OS}(1 + R_F/R) + I_{OS}R_F]$ instead of rising linearly. To keep the dc offset at the output small, one would select a low value for R_F. Unfortunately, however, the lower the value of R_F, the less ideal the integrator circuit becomes.

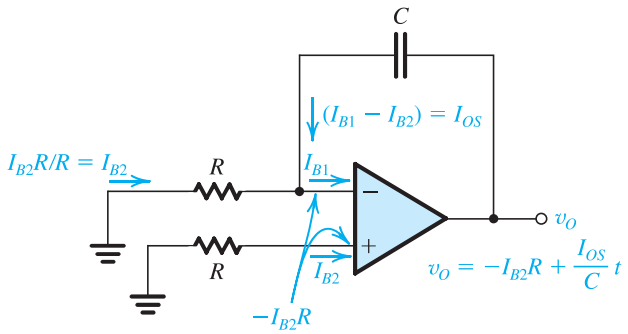

Figure 2.38 Effect of the op-amp input bias and offset currents on the performance of the Miller integrator circuit.