Expt 5 – NMOS Output Characteristics, CS Amplifier, and Current Mirror

EE 230 Analog Circuits Lab

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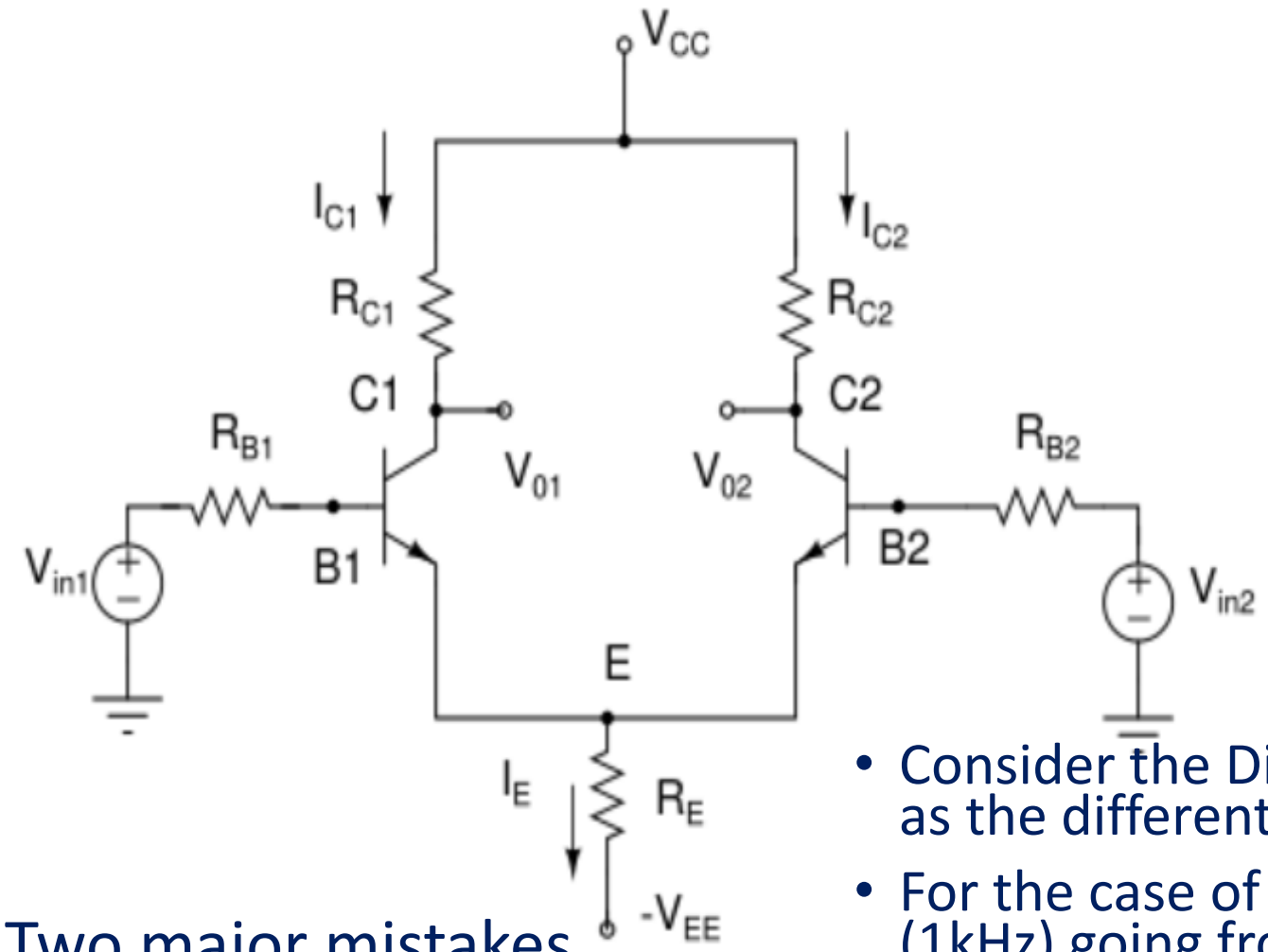
Summary

- Quiz 4, Question 6 – Diff Pair - Large Signal response

- Expt 5
  - Part A - NMOS Output Characteristics
  - Part B - CS Amplifier
  - Part C - Current Mirror based Current Source

Quiz 4, Ques.6



- Circuit values and parameters:
  - Vcc = + 10 V,
  - $-V_{EE}$ = - 10 V,
  - $R_{C1} = R_{C2}$ = 2 kΩ,
  - $R_{B1} = R_{B2}$ = 1 kΩ,
  - R_E = 5 kΩ.

- Two major mistakes
  - Large signal vs small signal
  - Max Vout?

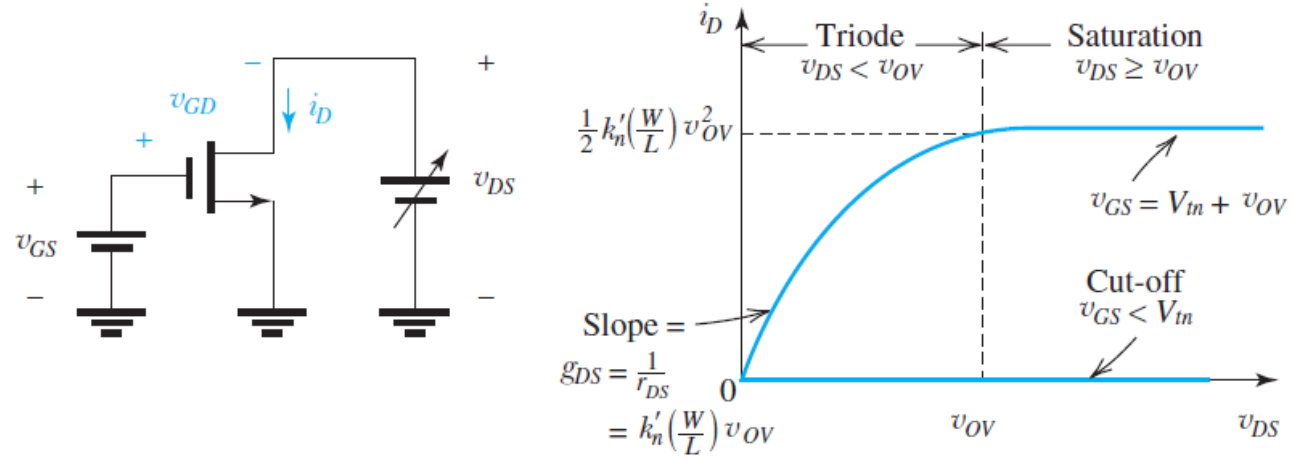
- Consider the Differential pair circuit of Expt 4 (same as the differential pair shown in Question 3).
- For the case of V_{in2} = 0 and V_{in1} a pulse waveform (1kHz) going from – 2 V to +2 V, sketch the V_{O2} output.
- Your sketch should show both V_{in1} and V_{O2} and also the voltage levels.

BJT Capacitances

- Cπ and Cμ – parasitic capacitances or internal capacitances?

- **Cπ and Cμ are internal capacitances (Ref Sedra & Smith – Microelectronic Circuits)**

Table 5.1 Regions of Operation of the Enhancement NMOS Transistor



- $v_{GS} < V_{tn}$: no channel; transistor in cut-off; $i_D = 0$
- $v_{GS} = V_{tn} + v_{OV}$: a channel is induced; transistor operates in the triode region or the saturation region depending on whether the channel is continuous or pinched-off at the drain end;

Triode Region

Continuous channel, obtained by:

$$v_{GD} > V_{tn}$$

or equivalently:

$$v_{DS} < v_{OV}$$

Then,

$$i_D = k_n'\left(\frac{W}{L}\right)\left[(v_{GS} - V_{tn})v_{DS} - \frac{1}{2}v_{DS}^2\right]$$

or equivalently,

$$i_D = k_n'\left(\frac{W}{L}\right)\left(v_{OV} - \frac{1}{2}v_{DS}\right)v_{DS}$$

Saturation Region

Pinched-off channel, obtained by:

$$v_{GD} \leq V_{tn}$$

or equivalently:

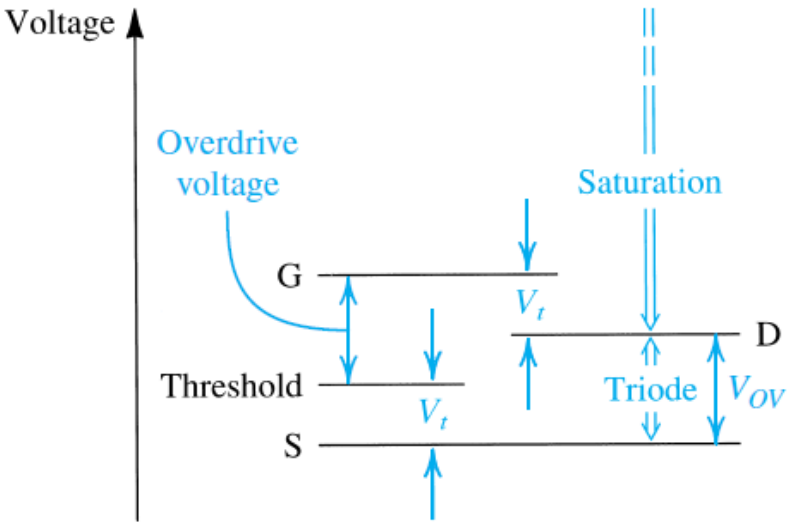
$$v_{DS} \geq v_{OV}$$

Then

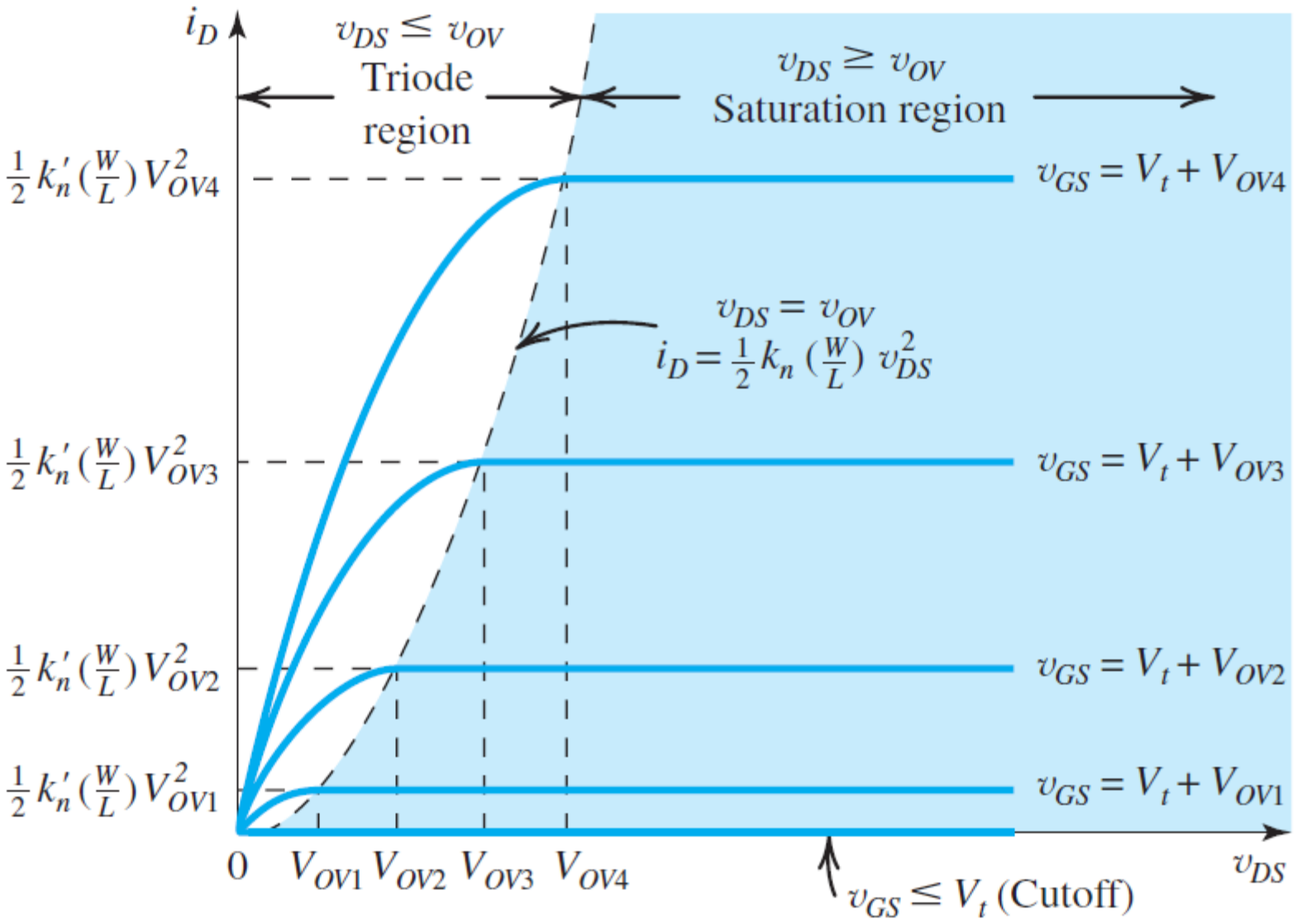
$$i_D = \frac{1}{2}k_n'\left(\frac{W}{L}\right)(v_{GS} - V_{tn})^2$$

or equivalently,

$$i_D = \frac{1}{2}k_n'\left(\frac{W}{L}\right)v_{OV}^2$$

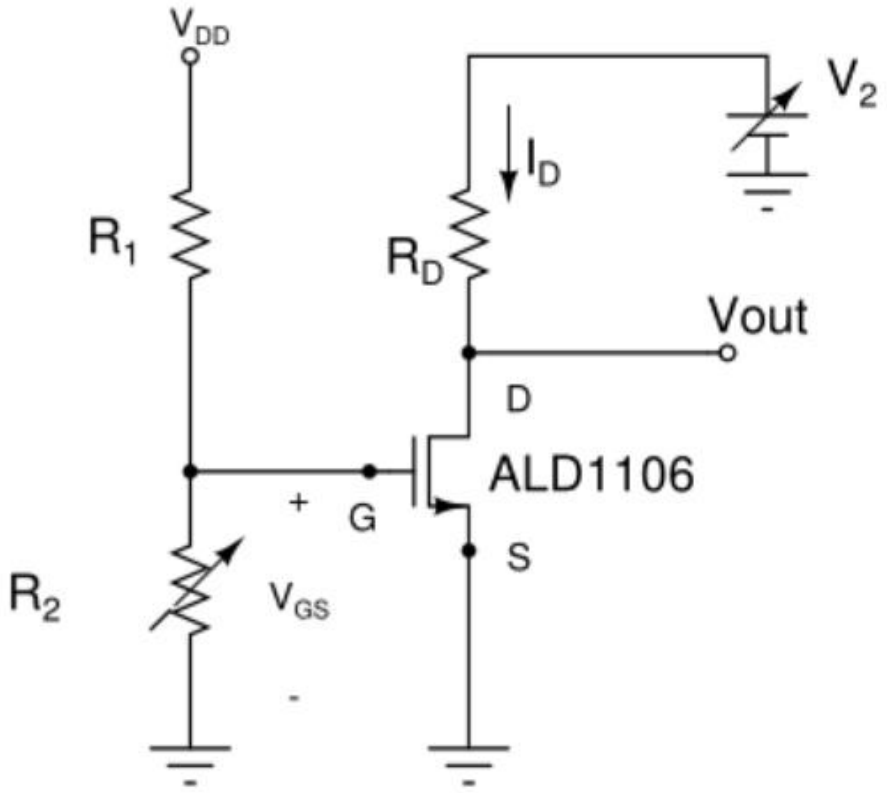


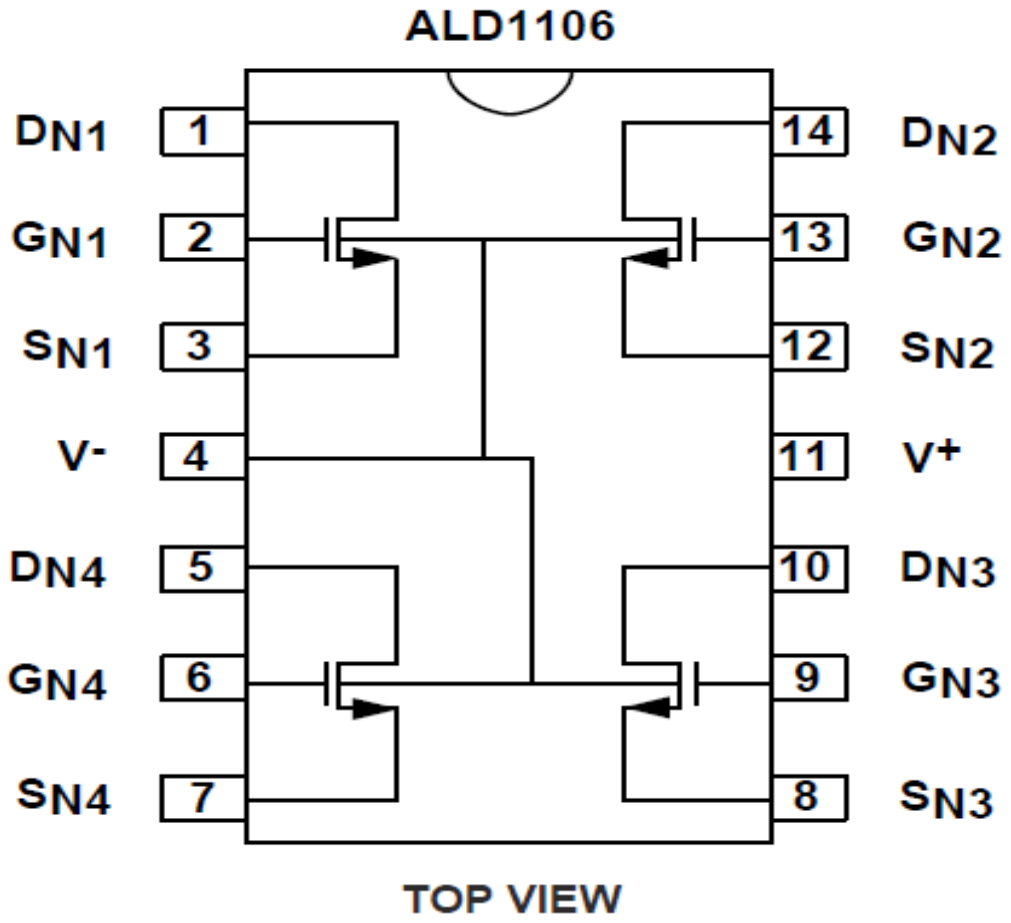
Source: Sedra & Smith – Microelectronic Circuits, 6ed., Chap 5



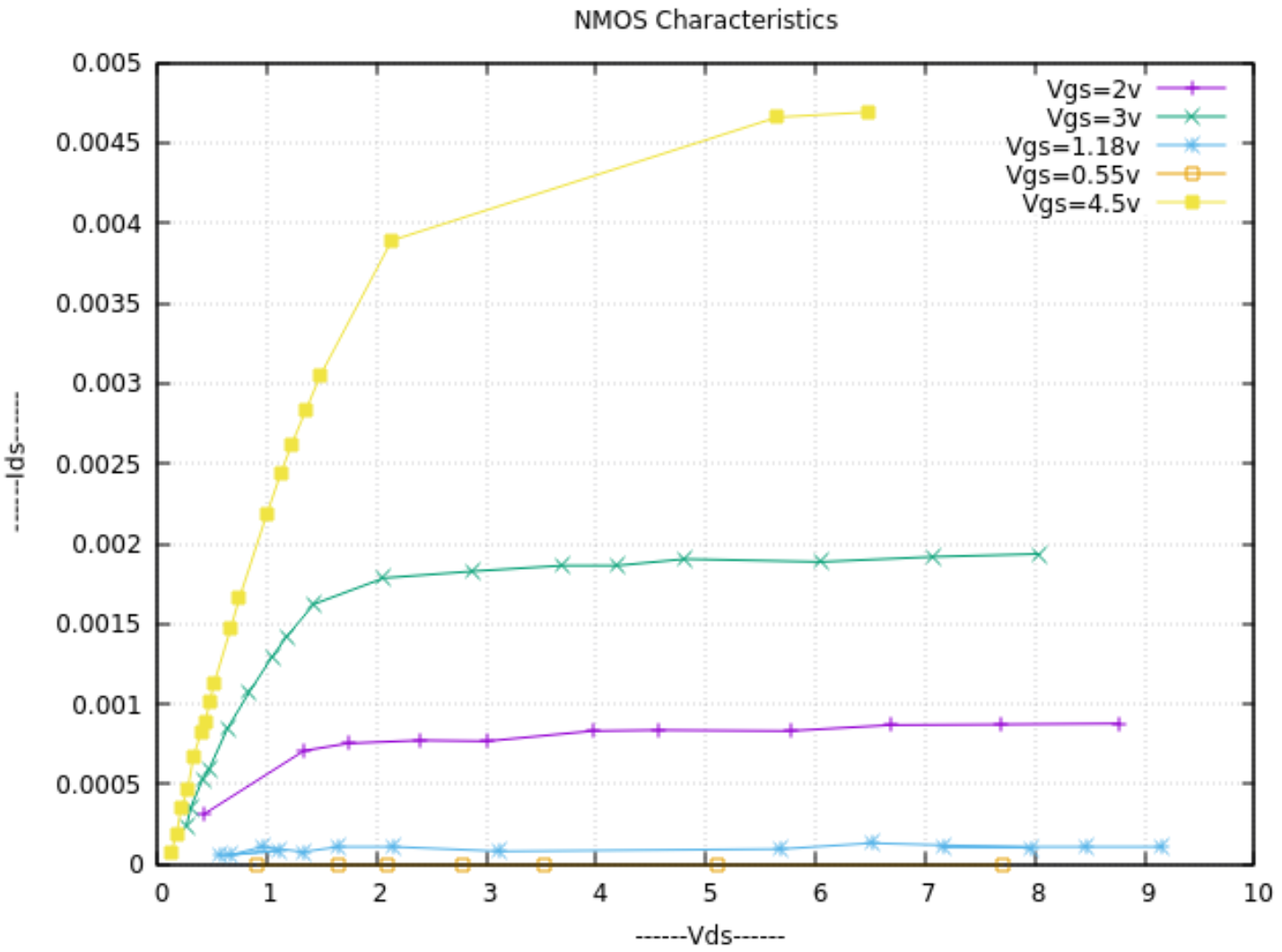
Source: Sedra & Smith – Microelectronic Circuits, 6ed., Chap 5

Part A - NMOS Output Characteristics





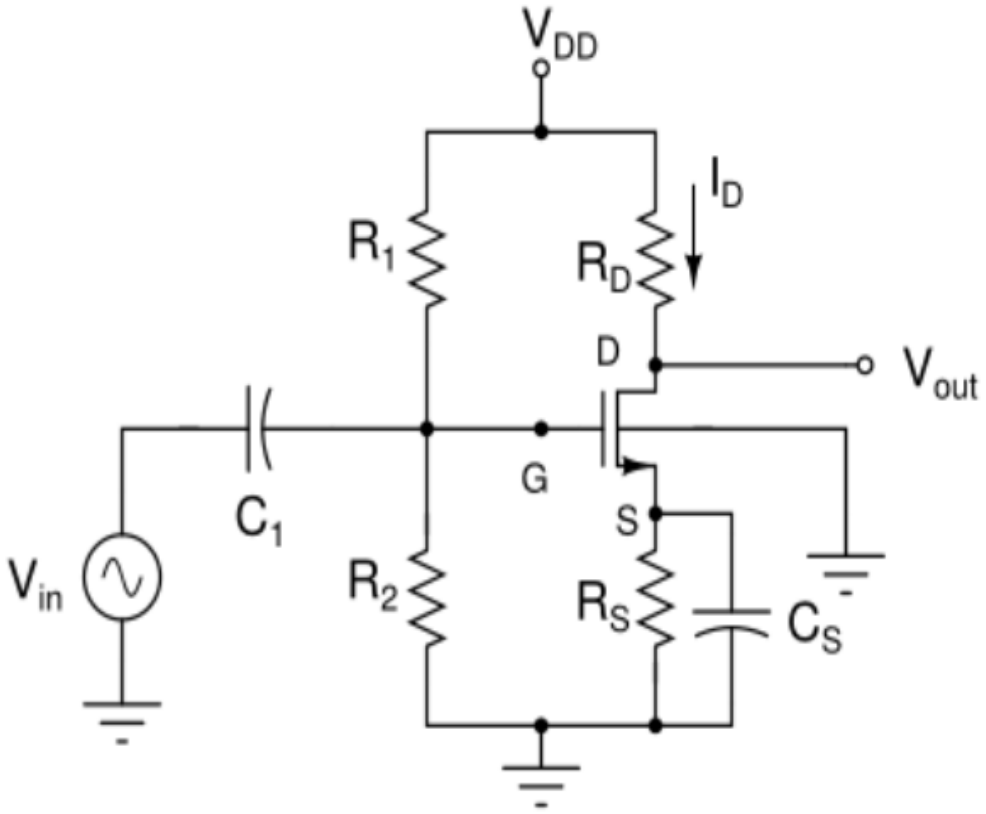
I_D vs V_{DS} plots: Measured Results



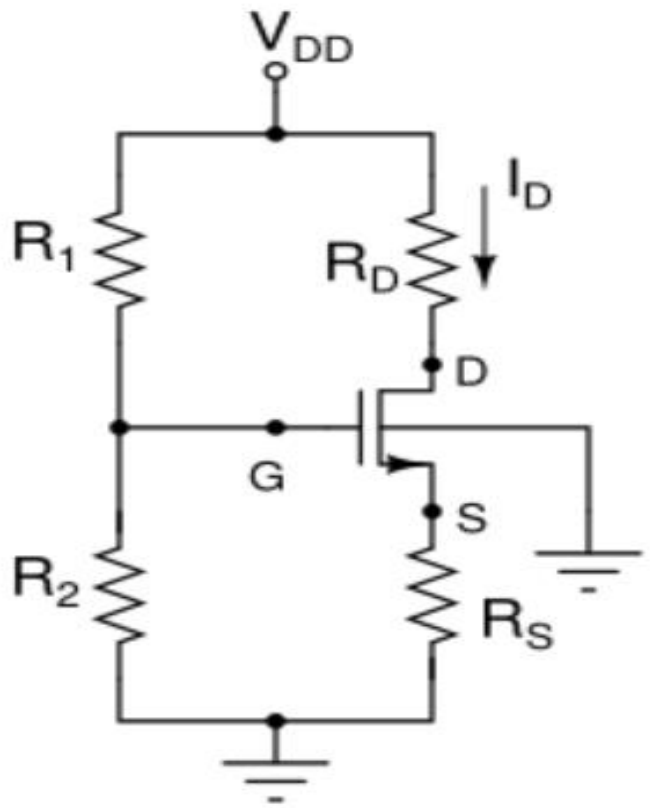
Part B - CS Amplifier

Features

- High input resistance
  - Limited only by the bias Ckt
- Low Voltage gain
  - Due to low g_m values
- Discrete CS Amplifiers seldom used



Part B - CS Amplifier – Bias Circuit



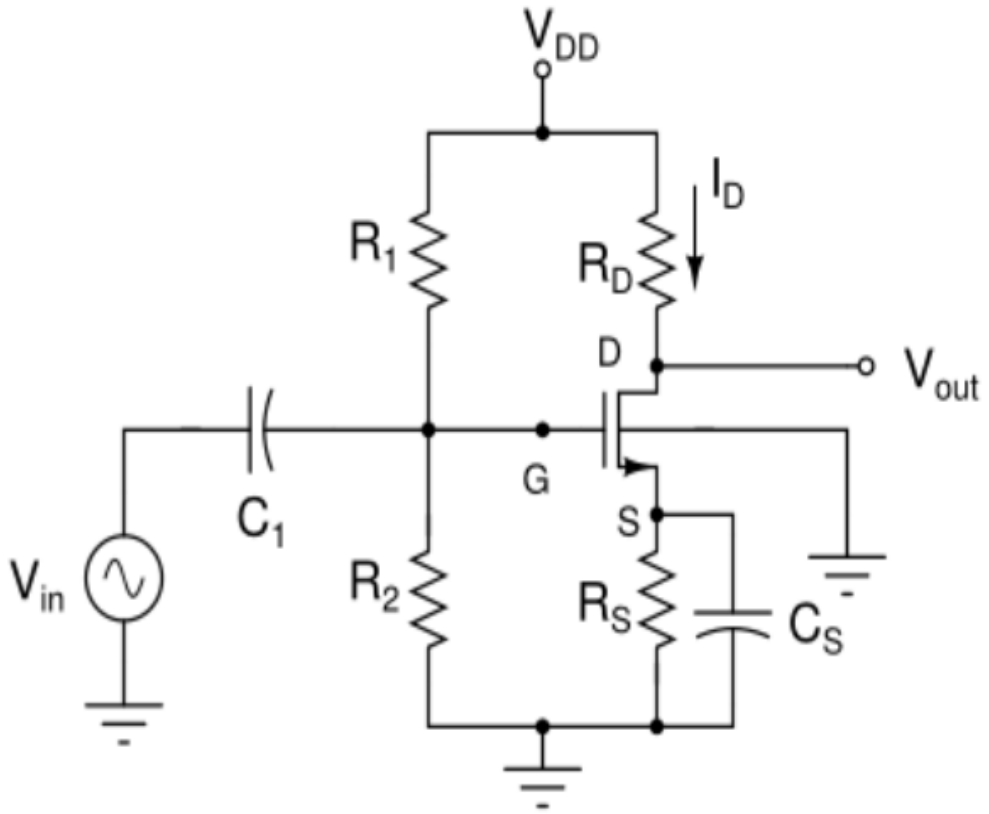
- V_{DD} = 12 V
- R_1 = 8.2 kΩ
- R_2 = 3.3 kΩ
- R_S = 1 kΩ
- R_D = 3.3 kΩ

- Design values
  - $V_{GS} \approx 2$ V
  - V_G = 3.44 V

- Choice of R_1, R_2, R_S and R_D
- Decide on I_D
- Choose V_{GS}
  - From the I_D vs V_{DS} Characteristics

- Measured Voltages
  - V_G = 3.4 V
  - V_S = 0.98 V
  - V_D = 8.72 V
  - V_{GS} = 2.42 V
  - I_D (=$[(V_{DD}-V_D)/R_D]$= 0.99 mA

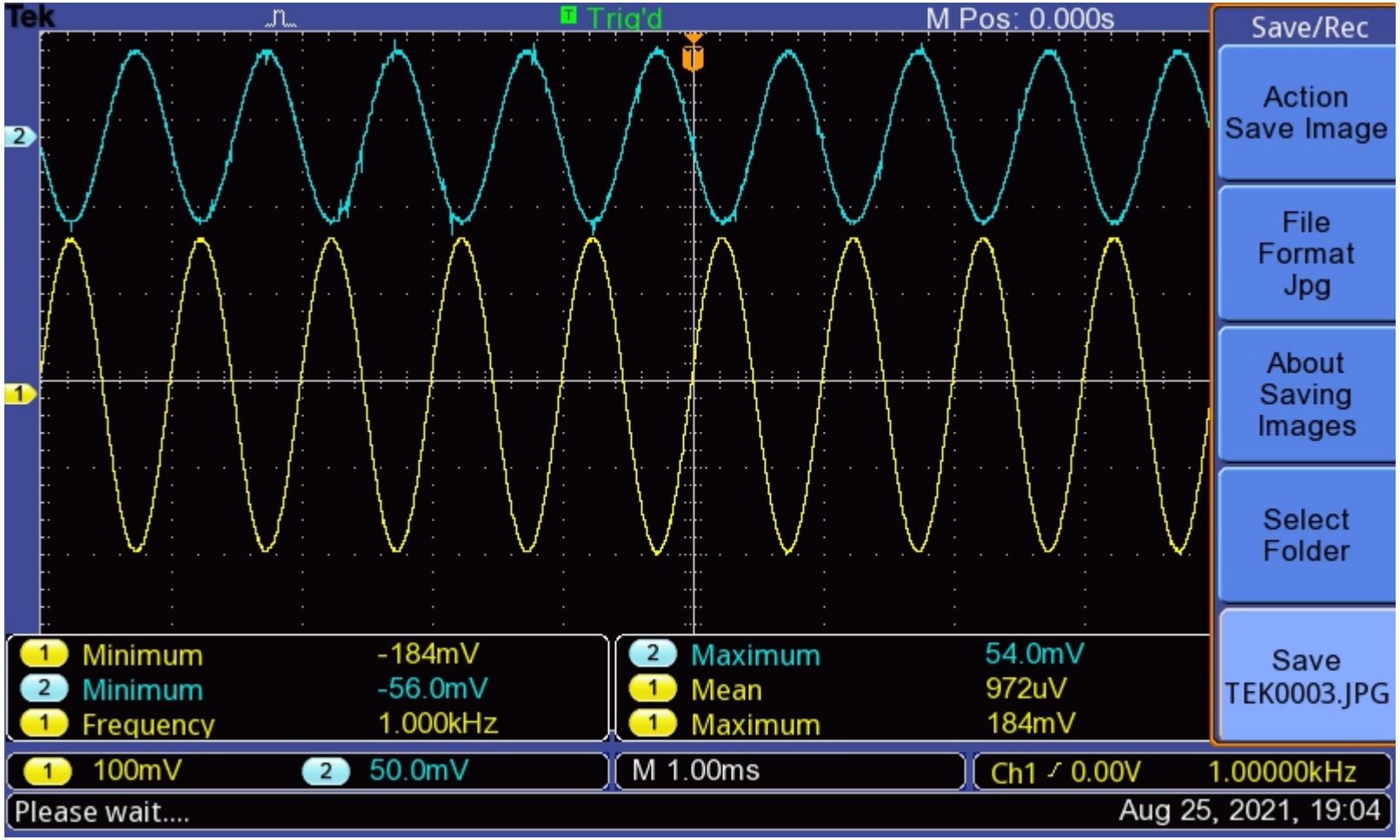
CS Amplifier



- C_1 = 10 µF
- C_S = 100 µF

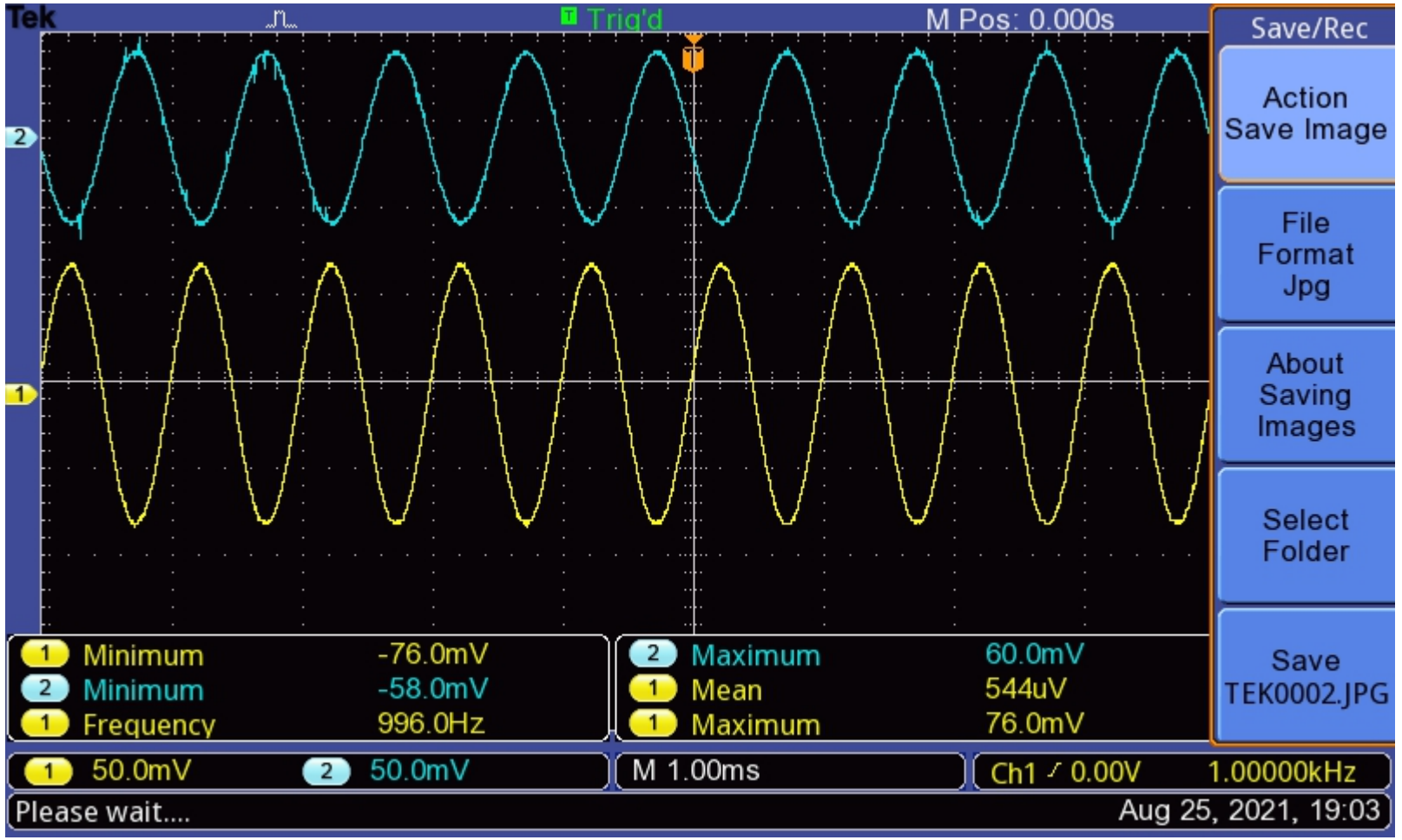
- V_{DD} = 12 V
- R_1 = 8.2 kΩ
- R_2 = 3.3 kΩ
- R_S = 1 kΩ
- R_D = 3.3 kΩ

CS Amplifier (C_1 = 10 µF; C_S = 100 µF)



- V_{in} = 50 sin ωt (1 kHz)
  - V_{in} (p-to-p) = 100 mV
- V_{out} : 368 mV p-to-p
- Voltage gain = 3.68 V/V
  - (R_D = 3.3 kΩ, R_L – open)
- NGSPICE Simulation
  - V_{out} = 465 mV (p-p)
  - (W/L)=10; KP= 100u
  - Vto = 1

CS Amplifier (C_1 = 10 µF; No C_S)

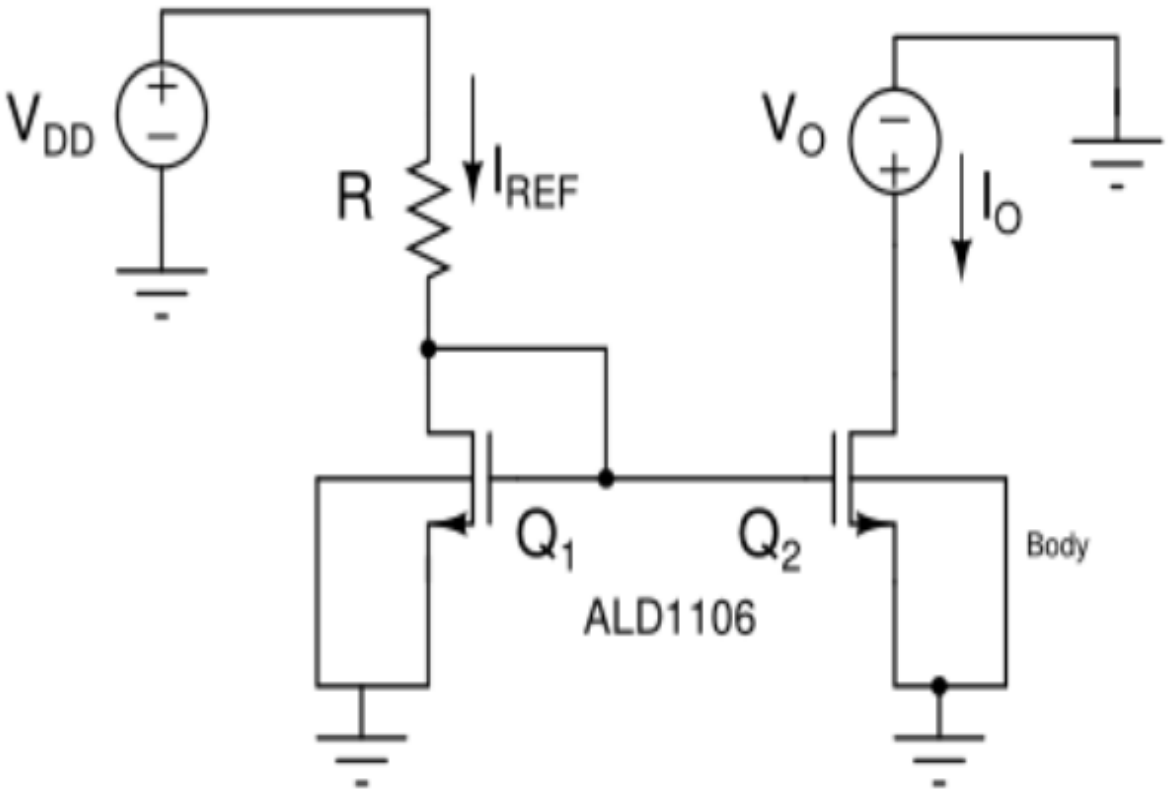


- V_{in} = 50 sin ωt (1 kHz)
  - V_{in} (p-to-p) = 100 mV
- V_{out} : 120 mV p-to-p
- Voltage gain = 1.2 V/V
- NGSPICE Simulation
  - V_{out} = 190 mV (p-p)
  - (W/L)=10; KP= 100u
  - Vto = 1

Summary of CS Amplifier Features

- Very high input resistance (due to zero gate current)
  - Input resistance of the CS amp limited primarily due to the biasing circuit.
  - Solution - choose large resistor values at the input side for biasing
- Very low g_m
- Expression for gm: $$g_m = \sqrt{2\mu_n C_{ox}\left(\frac{W}{L}\right) I_D}$$
- Observation regarding g_m dependence:
  - Proportional to $\sqrt{I_D}$
  - Proportional to $\sqrt{\frac{W}{L}}$
  - Proportional to $\sqrt{\mu_n C_{ox}}$
  - Depends on both biasing current and on the process

Part C - Current Mirror based Current Source



- V_{DD} = 12 V
- R = 8.2 kΩ

- NGSPICE Simulation
  - VGS = 2.5 V
  - I_{REF} = 1.158 mA
  - I_O = 1.186 mA @ V_O = 5V
  - (W/L)=10; KP= 100u
  - Vto = 1
  - Lambda = 0.01

Current Mirror - Measurements

```
1  ##########################################
2  #   Current Mirror Experiment            #
3  #    Rout = 1k , biasing resistor = 8.2k #
4  #             Vgs=2.08V(measured)        #
5  ##########################################
6  # Vdd(V)   |   Vout(V)   |  Io(mA)
7    1             0.47        0.53
8    2             1.19        0.81
9    3             2.18        0.82
10   4             3.22        0.78
11   5             4.19        0.81
12   6             5.22        0.78
13
```

```
1  ##########################################
2  #   Current Mirror Experiment            #
3  #    Rout = 1k , biasing resistor = 6.8k #
4  #             Vgs=2.25V(measured)        #
5  ##########################################
6  # Vdd(V)   |   Vout(V)   |  Io(mA)
7    1             0.44        0.56
8    2             1.08        0.92
9    3             2.03        0.97
10   4             3.04        0.96
11   5             4.03        0.97
12   6             5.02        0.98
13
```