EE230 : Analog Circuits Lab

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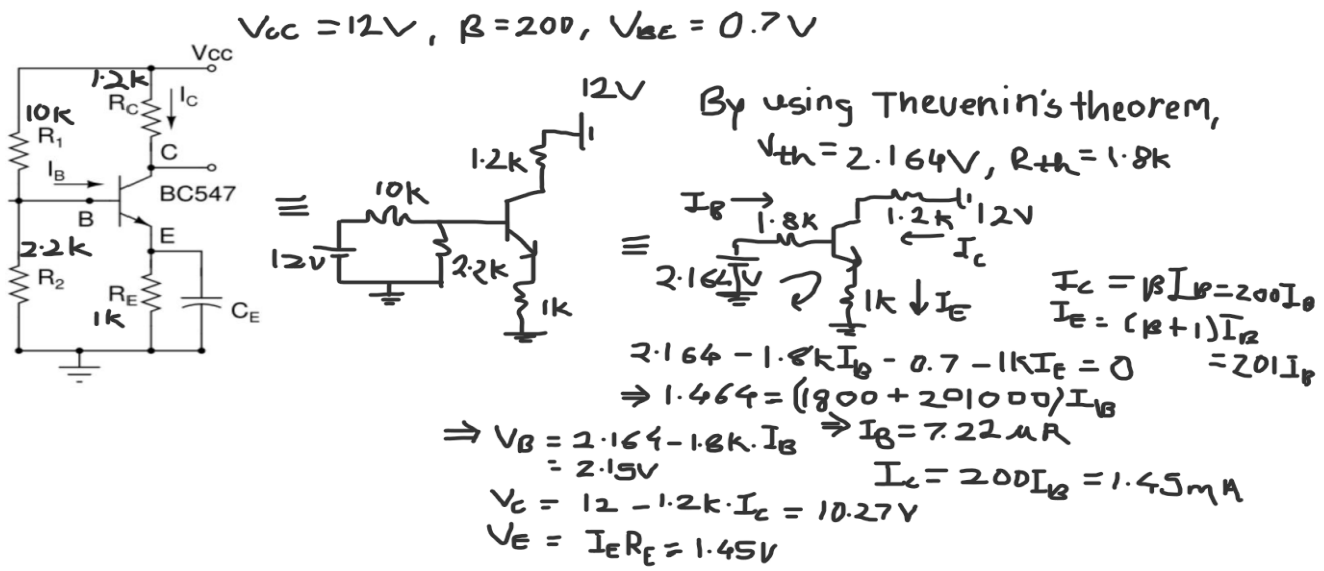
Experiment 3: BJT Voltage Amplifiers (CE and CC)

August 13, 2021

Common-Emitter Amplifier : Biasing Circuit

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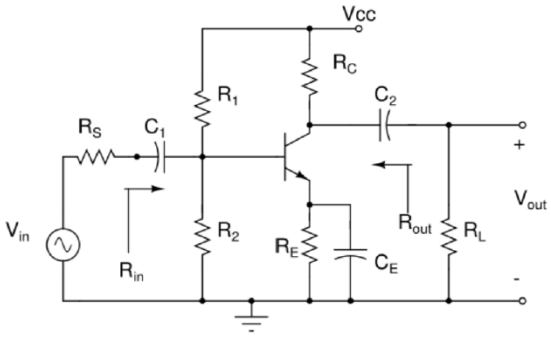
19D070070 | Mayur Ware
*Common-Emitter Amplifier: Biasing Circuit
.model bc547a NPN IS=10f BF=200 ISE=10.3f IKF=50m NE=1.3
+ BR=9.5 VAF=80 IKR=12m ISC=47p NC=2 VAR=10 RB=280 RE=1 RC=40
+ tr=0.3u tf=0.5n cje=12p vje=0.48 mje=0.5 cjc=6p vjc=0.7 mjc=0.33 kf=2f
*BJT
Q1 2 3 5 bc547a
*Voltage Sources
Vin In GND 12
V1 1 2 0
V2 4 3 0
*Resistors
R1 In 4 10k
R2 4 GND 2.2k
Rc In 1 1.2k
Re 5 GND 1k
*Control Commands
.op
.control
run
print i(V2) i(V1) V(2) V(3) V(5)
.endc
.end
```

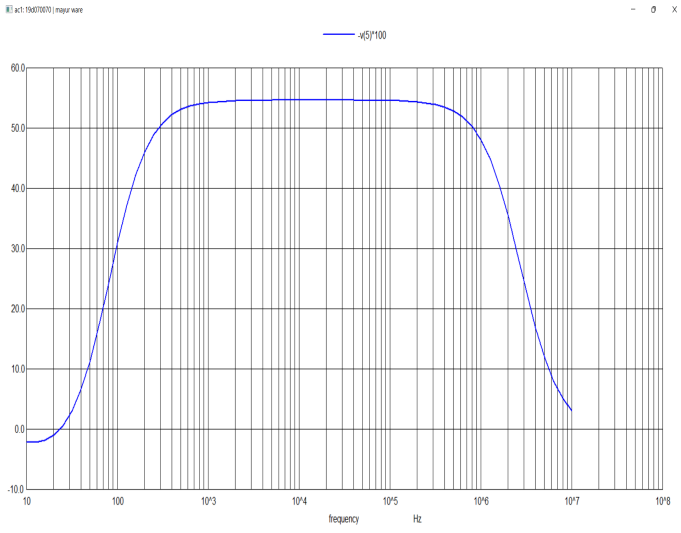
Simulation Results :
i(v2) = 7.235117e-06
i(v1) = 1.462957e-03
v(2) = 1.024445e+01
v(3) = 2.143645e+00
v(5) = 1.474208e+00
As V_{CE} is greater than 0.2 (V_{CESat}), we can verify that the BJT is in Active Mode.
Correct biasing in this circuit is very important because of this.

Common-Emitter Amplifier (with bypass Capacitor CE) : Midband Voltage Gain




```
19D070070 | Mayur Ware
*Midband Voltage Gain
.model bc547a NPN IS=10f BF=200 ISE=10.3f IKF=50m NE=1.3
+ BR=9.5 VAF=80 IKR=12m ISC=47p NC=2 VAR=10 RB=280 RE=1 RC=40
+ tr=0.3u tf=0.5n cje=12p vje=0.48 mje=0.5 cjc=6p vjc=0.7 mjc=0.33 kf=2f
*BJT
Q1 1 2 3 bc547a
*Voltage Sources
Vin In GND 12
V1 4 GND dc 0 ac 0.01
*Resistors
R1 In 2 10k
R2 2 GND 2.2k
Rc In 1 1.2k
Re 3 GND 1k
Rl 5 GND 100k
*Capacitors
C1 2 4 10u
C2 1 5 10u
Ce 3 GND 100u
*Control Commands
.ac dec 10 10 10Meg
.control
run
plot -V(5)*100
.endc
.end
```

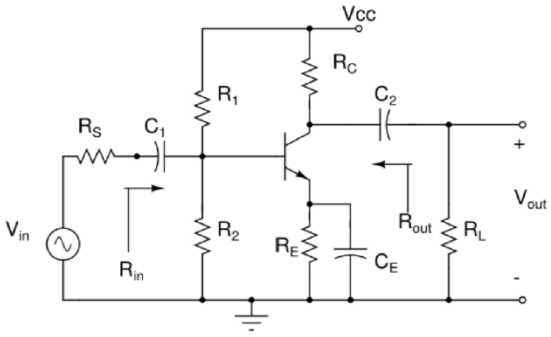
Plots :



Observations :

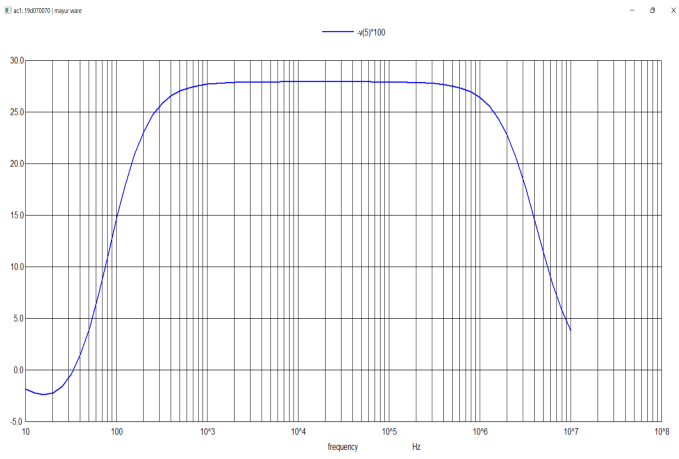
I learned small signal analysis using NGSpice.
Average Midband, as we can notice, is -54.

Common-Emitter Amplifier (with bypass Capacitor CE) : Effect of RL on the Midband Gain

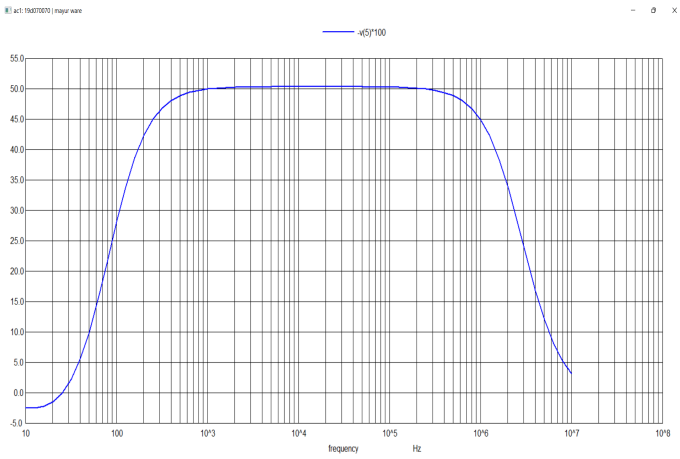



```
19D070070 | Mayur Ware
*Effect of RL on the Midband Gain
.model bc547a NPN IS=10f BF=200 ISE=10.3f IKF=50m NE=1.3
+ BR=9.5 VAF=80 IKR=12m ISC=47p NC=2 VAR=10 RB=280 RE=1 RC=40
+ tr=0.3u tf=0.5n cje=12p vje=0.48 mje=0.5 cjc=6p vjc=0.7 mjc=0.33 kf=2f
*BJT
Q1 1 2 3 bc547a
*Voltage Sources
Vin In GND 12
V1 4 GND dc 0 ac 0.01
*Resistors
R1 In 2 10k
R2 2 GND 2.2k
Rc In 1 1.2k
Re 3 GND 1k
Rl 5 GND 1.2k
*Capacitors
C1 2 4 10u
C2 1 5 10u
Ce 3 GND 100u
*Control Commands
.ac dec 10 10 10Meg
.control
run
plot -V(5)*100
.endc
.end
```

Plots :



RL = 1.2k

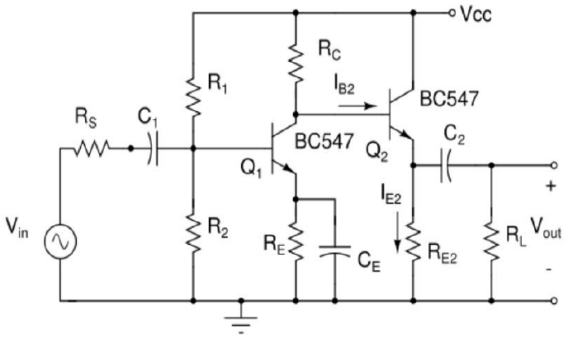


RL = 12k

Learning :

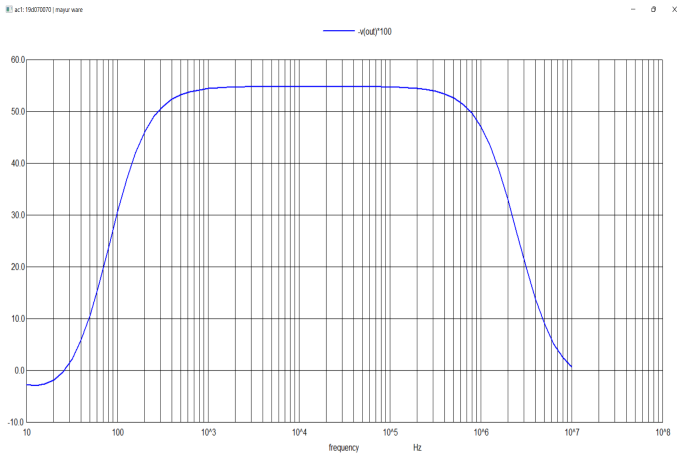
As we increase RL, midband gain voltage increases. Although, band frequencies are nearly same.

Two Stage Amplifier (CE and CC)




```
19D070070 | Mayur Ware
*Two-stage Amplifier (CE and CC): Biasing Circuit
*BJT
Q1 1 2 3 bc547a
Q2 In 5 6 bc547a
*Voltage Sources
Vin In GND dc 12
V1 8 GND dc 0 ac 0.01
V2 1 5 dc 0V
V3 6 7 dc 0V
*Resistors
R1 In 2 10k
R2 2 GND 2.2k
Rc In 1 1.2k
Re 3 GND 1k
Re2 7 GND 10k
Rl Out GND 10k
*Capacitors
C1 2 8 10u
C2 6 Out 10u
Ce 3 GND 100u
*Control Commands
.ac dec 10 10 10Meg
.control
run
*print i(V2) i(V3) V(6)
plot -V(Out)*100
.endc
.end
```

Plots :



Observations :

i(V2) = 8.075083e-06 i(V3) = 9.576092e-04 V(6) = 9.576092e+00/

CE has high gain but not good Rin and Rout. CC has gain only 1 but good Rin and Rout. Thus, using them together we get good gain and good Rout