

Figure 5.20 The relative levels of the terminal voltages of the enhancement-type PMOS transistor for operation in the triode region and in the saturation region.

EXERCISE

5.7 The PMOS transistor shown in Fig. E5.7 has $V_{tp} = -1$ V, $k'_p = 60 \mu\text{A/V}^2$, and $W/L = 10$.

- Find the range of V_G for which the transistor conducts.
- In terms of V_G , find the range of V_D for which the transistor operates in the triode region.
- In terms of V_G , find the range of V_D for which the transistor operates in saturation.
- Neglecting channel-length modulation (i.e., assuming $\lambda = 0$), find the values of $|V_{ov}|$ and V_G and the corresponding range of V_D to operate the transistor in the saturation mode with $I_D = 75 \mu\text{A}$.
- If $\lambda = -0.02 \text{ V}^{-1}$, find the value of r_o corresponding to the overdrive voltage determined in (d).
- For $\lambda = -0.02 \text{ V}^{-1}$ and for the value of V_{ov} determined in (d), find I_D at $V_D = +3$ V and at $V_D = 0$ V; hence, calculate the value of the apparent output resistance in saturation. Compare to the value found in (e).

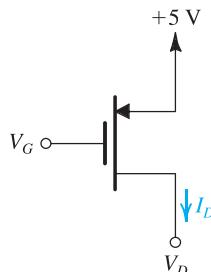


Figure E5.7

Ans. (a) $V_G \leq +4$ V; (b) $V_D \geq V_G + 1$; (c) $V_D \leq V_G + 1$; (d) 0.5 V, 3.5 V, ≤ 4.5 V; (e) $0.67 \text{ M}\Omega$; (f) $78 \mu\text{A}$, $82.5 \mu\text{A}$, $0.67 \text{ M}\Omega$ (same)

5.3 MOSFET Circuits at DC

Having studied the current–voltage characteristics of MOSFETs, we now consider circuits in which only dc voltages and currents are of concern. Specifically, we shall present a series of design and analysis examples of MOSFET circuits at dc. The objective is to instill in the reader a familiarity with the device and the ability to perform MOSFET circuit analysis both rapidly and effectively.

In the following examples, to keep matters simple and thus focus attention on the essence of MOSFET circuit operation, we will generally neglect channel-length modulation; that is, we will assume $\lambda = 0$. We will find it convenient to work in terms of the overdrive voltage; $V_{ov} = V_{GS} - V_m$ for NMOS and $|V_{ov}| = V_{SG} - |V_{tp}|$ for PMOS.

Example 5.3

Design the circuit of Fig. 5.21, that is, determine the values of R_D and R_S , so that the transistor operates at $I_D = 0.4$ mA and $V_D = +0.5$ V. The NMOS transistor has $V_t = 0.7$ V, $\mu_n C_{ox} = 100 \mu\text{A/V}^2$, $L = 1 \mu\text{m}$, and $W = 32 \mu\text{m}$. Neglect the channel-length modulation effect (i.e., assume that $\lambda = 0$).

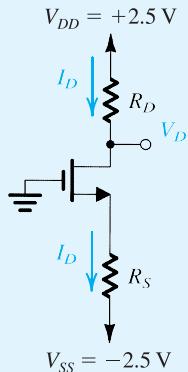


Figure 5.21 Circuit for Example 5.3.

Solution

To establish a dc voltage of +0.5 V at the drain, we must select R_D as follows:

$$\begin{aligned} R_D &= \frac{V_{DD} - V_D}{I_D} \\ &= \frac{2.5 - 0.5}{0.4} = 5 \text{ k}\Omega \end{aligned}$$

To determine the value required for R_S , we need to know the voltage at the source, which can be easily found if we know V_{GS} . This in turn can be determined from V_{OV} . Toward that end, we note that since $V_D = 0.5$ V is greater than V_G , the NMOS transistor is operating in the saturation region, and we can use the saturation-region expression of i_D to determine the required value of V_{OV} ,

$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} V_{OV}^2$$

Then substituting $I_D = 0.4$ mA = 400 μA , $\mu_n C_{ox} = 100 \mu\text{A/V}^2$, and $W/L = 32/1$ gives

$$400 = \frac{1}{2} \times 100 \times \frac{32}{1} V_{OV}^2$$

which results in

$$V_{OV} = 0.5 \text{ V}$$

Thus,

$$V_{GS} = V_t + V_{OV} = 0.7 + 0.5 = 1.2 \text{ V}$$

Referring to Fig. 5.21, we note that the gate is at ground potential. Thus, the source must be at -1.2 V, and the required value of R_S can be determined from

$$\begin{aligned} R_S &= \frac{V_S - V_{SS}}{I_D} \\ &= \frac{-1.2 - (-2.5)}{0.4} = 3.25 \text{ k}\Omega \end{aligned}$$

EXERCISE

D5.8 Redesign the circuit of Fig. 5.21 for the following case: $V_{DD} = -V_{SS} = 2.5$ V, $V_t = 1$ V, $\mu_n C_{ox} = 60 \mu\text{A/V}^2$, $W/L = 120 \mu\text{m}/3 \mu\text{m}$, $I_D = 0.3$ mA, and $V_D = +0.4$ V.

Ans. $R_D = 7 \text{ k}\Omega$; $R_S = 3.3 \text{ k}\Omega$

Example 5.4

Figure 5.22 shows an NMOS transistor with its drain and gate terminals connected together. Find the $i-v$ relationship of the resulting two-terminal device in terms of the MOSFET parameters $k_n = k'_n(W/L)$ and V_{tn} . Neglect channel-length modulation (i.e., $\lambda = 0$). Note that this two-terminal device is known as a **diode-connected transistor**.

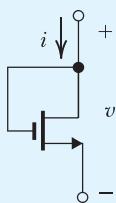


Figure 5.22

Solution

Since $v_D = v_G$ implies operation in the saturation mode,

$$i_D = \frac{1}{2}k'_n\left(\frac{W}{L}\right)(v_{GS} - V_{tn})^2$$

Now, $i = i_D$ and $v = v_{GS}$, thus

$$i = \frac{1}{2}k'_n\left(\frac{W}{L}\right)(v - V_{tn})^2$$

Replacing $k'_n\left(\frac{W}{L}\right)$ by k_n results in

$$i = \frac{1}{2}k_n(v - V_{tn})^2$$

EXERCISES

D5.9 For the circuit in Fig. E5.9, find the value of R that results in $V_D = 0.8$ V. The MOSFET has $V_{tn} = 0.5$ V, $\mu_n C_{ox} = 0.4$ mA/V², $W/L = \frac{0.72 \mu\text{m}}{0.18 \mu\text{m}}$, and $\lambda = 0$.

Ans. 13.9 kΩ

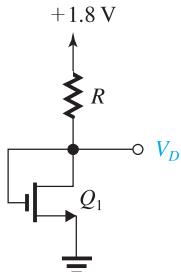


Figure E5.9

D5.10 Figure E5.10, shows a circuit obtained by augmenting the circuit of Fig. E5.9 considered in Exercise 5.9 with a transistor Q_2 identical to Q_1 and a resistance R_2 . Find the value of R_2 that results in Q_2 operating at the edge of the saturation region. Use your solution to Exercise 5.9.

Ans. 20.8 kΩ

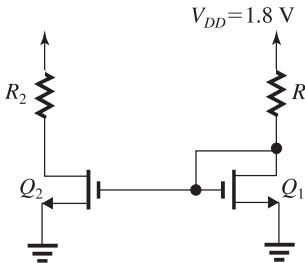


Figure E5.10

Example 5.5

Design the circuit in Fig. 5.23 to establish a drain voltage of 0.1 V. What is the effective resistance between drain and source at this operating point? Let $V_{tn} = 1$ V and $k'_n(W/L) = 1$ mA/V².

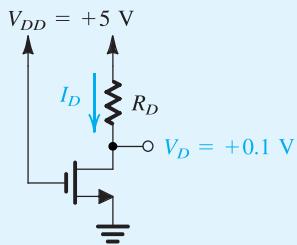


Figure 5.23 Circuit for Example 5.5.

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Example 5.5 *continued*

Solution

Since the drain voltage is lower than the gate voltage by 4.9 V and $V_{tn} = 1$ V, the MOSFET is operating in the triode region. Thus the current I_D is given by

$$\begin{aligned}I_D &= k' \frac{W}{L} \left[(V_{GS} - V_{tn}) V_{DS} - \frac{1}{2} V_{DS}^2 \right] \\I_D &= 1 \times \left[(5 - 1) \times 0.1 - \frac{1}{2} \times 0.01 \right] \\&= 0.395 \text{ mA}\end{aligned}$$

The required value for R_D can be found as follows:

$$\begin{aligned}R_D &= \frac{V_{DD} - V_D}{I_D} \\&= \frac{5 - 0.1}{0.395} = 12.4 \text{ k}\Omega\end{aligned}$$

In a practical discrete-circuit design problem, one selects the closest standard value available for, say, 5% resistors—in this case, 12 kΩ; see Appendix G. Since the transistor is operating in the triode region with a small V_{DS} , the effective drain-to-source resistance can be determined as follows:

$$\begin{aligned}r_{DS} &= \frac{V_{DS}}{I_D} \\&= \frac{0.1}{0.395} = 253 \text{ }\Omega\end{aligned}$$

EXERCISE

- 5.11** If in the circuit of Example 5.5 the value of R_D is doubled, find approximate values for I_D and V_D .

Ans. 0.2 mA; 0.05 V

Example 5.6

Analyze the circuit shown in Fig. 5.24(a) to determine the voltages at all nodes and the currents through all branches. Let $V_{tn} = 1$ V and $k'_n(W/L) = 1 \text{ mA/V}^2$. Neglect the channel-length modulation effect (i.e., assume $\lambda = 0$).

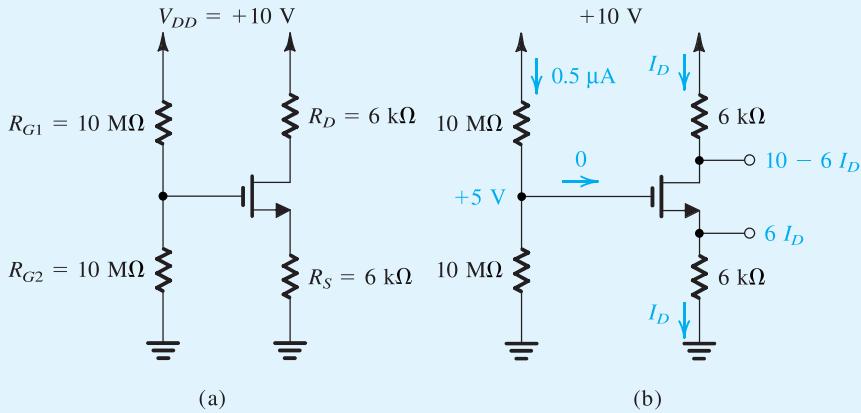


Figure 5.24 (a) Circuit for Example 5.6. (b) The circuit with some of the analysis details shown.

Solution

Since the gate current is zero, the voltage at the gate is simply determined by the voltage divider formed by the two 10-M Ω resistors,

$$V_G = V_{DD} \frac{R_{G2}}{R_{G2} + R_{G1}} = 10 \times \frac{10}{10 + 10} = +5 \text{ V}$$

With this positive voltage at the gate, the NMOS transistor will be turned on. We do not know, however, whether the transistor will be operating in the saturation region or in the triode region. We shall assume saturation-region operation, solve the problem, and then check the validity of our assumption. Obviously, if our assumption turns out not to be valid, we will have to solve the problem again for triode-region operation.

Refer to Fig. 5.24(b). Since the voltage at the gate is 5 V and the voltage at the source is I_D (mA) \times 6 (k Ω) = $6I_D$, we have

$$V_{GS} = 5 - 6I_D$$

Thus, I_D is given by

$$\begin{aligned} I_D &= \frac{1}{2} k'_n \frac{W}{L} (V_{GS} - V_{tn})^2 \\ &= \frac{1}{2} \times 1 \times (5 - 6I_D - 1)^2 \end{aligned}$$

which results in the following quadratic equation in I_D :

$$18I_D^2 - 25I_D + 8 = 0$$

Example 5.6 *continued*

This equation yields two values for I_D : 0.89 mA and 0.5 mA. The first value results in a source voltage of $6 \times 0.89 = 5.34$ V, which is greater than the gate voltage and does not make physical sense as it would imply that the NMOS transistor is cut off. Thus,

$$I_D = 0.5 \text{ mA}$$

$$V_S = 0.5 \times 6 = +3 \text{ V}$$

$$V_{GS} = 5 - 3 = 2 \text{ V}$$

$$V_D = 10 - 6 \times 0.5 = +7 \text{ V}$$

Since $V_D > V_G - V_{tn}$, the transistor is operating in saturation, as initially assumed.

EXERCISES

- 5.12** For the circuit of Fig. 5.24, what is the largest value that R_D can have while the transistor remains in the saturation mode?

Ans. 12 kΩ

- D5.13** Redesign the circuit of Fig. 5.24 for the following requirements: $V_{DD} = +5$ V, $I_D = 0.32$ mA, $V_s = 1.6$ V, $V_p = 3.4$ V, with a 1-μA current through the voltage divider R_{G1}, R_{G2} . Assume the same MOSFET as in Example 5.6.

Ans. $R_{G1} = 1.6 \text{ M}\Omega$; $R_{G2} = 3.4 \text{ M}\Omega$, $R_s = R_D = 5 \text{ k}\Omega$

Example 5.7

Design the circuit of Fig. 5.25 so that the transistor operates in saturation with $I_D = 0.5$ mA and $V_D = +3$ V. Let the enhancement-type PMOS transistor have $V_{tp} = -1$ V and $k'_p(W/L) = 1 \text{ mA/V}^2$. Assume $\lambda = 0$. What is the largest value that R_D can have while maintaining saturation-region operation?

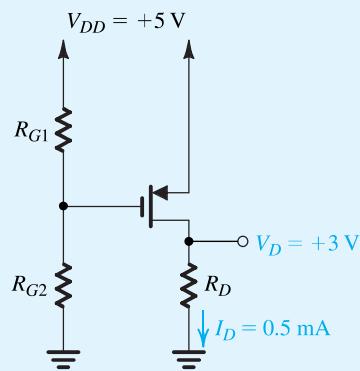


Figure 5.25 Circuit for Example 5.7.

Solution

Since the MOSFET is to be in saturation, we can write

$$I_D = \frac{1}{2} k'_p \frac{W}{L} |V_{OV}|^2$$

Substituting $I_D = 0.5$ mA and $k'_p W/L = 1$ mA/V², we obtain

$$|V_{OV}| = 1 \text{ V}$$

and

$$V_{SG} = |V_{tp}| + |V_{OV}| = 1 + 1 = 2 \text{ V}$$

Since the source is at +5 V, the gate voltage must be set to +3 V. This can be achieved by the appropriate selection of the values of R_{G1} and R_{G2} . A possible selection is $R_{G1} = 2 \text{ M}\Omega$ and $R_{G2} = 3 \text{ M}\Omega$.

The value of R_D can be found from

$$R_D = \frac{V_D}{I_D} = \frac{3}{0.5} = 6 \text{ k}\Omega$$

Saturation-mode operation will be maintained up to the point that V_D exceeds V_G by $|V_{tp}|$; that is, until

$$V_{D_{\max}} = 3 + 1 = 4 \text{ V}$$

This value of drain voltage is obtained with R_D given by

$$R_D = \frac{4}{0.5} = 8 \text{ k}\Omega$$

EXERCISE

D5.14 For the circuit in Fig. E5.14, find the value of R that results in the PMOS transistor operating with an overdrive voltage $|V_{OV}| = 0.6$ V. The threshold voltage is $V_{tp} = -0.4$ V, the process transconductance parameter $k'_p = 0.1$ mA/V², and $W/L = 10 \mu\text{m}/0.18 \mu\text{m}$.

Ans. 800 Ω

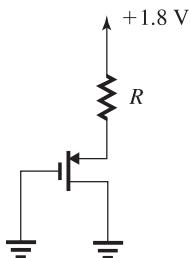


Figure E5.14

Example 5.8

The NMOS and PMOS transistors in the circuit of Fig. 5.26(a) are matched, with $k'_n(W_n/L_n) = k'_p(W_p/L_p) = 1 \text{ mA/V}^2$ and $V_{tn} = -V_{tp} = 1 \text{ V}$. Assuming $\lambda = 0$ for both devices, find the drain currents i_{DN} and i_{DP} , as well as the voltage v_O , for $v_I = 0 \text{ V}$, $+2.5 \text{ V}$, and -2.5 V .

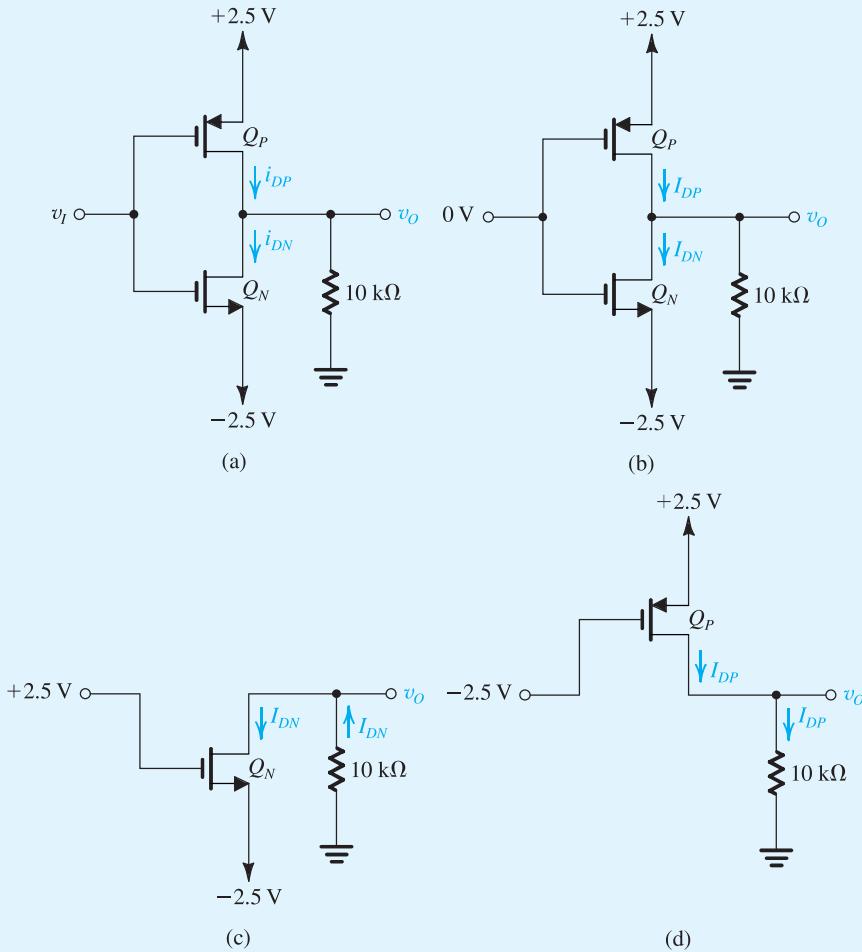


Figure 5.26 Circuits for Example 5.8.

Solution

Figure 5.26(b) shows the circuit for the case $v_I = 0 \text{ V}$. We note that since Q_N and Q_P are perfectly matched and are operating at equal values of $|V_{GS}|$ (2.5 V), the circuit is symmetrical, which dictates that $v_O = 0 \text{ V}$. Thus both Q_N and Q_P are operating with $|V_{DG}| = 0$ and, hence, in saturation. The drain currents can now be found from

$$I_{DP} = I_{DN} = \frac{1}{2} \times 1 \times (2.5 - 1)^2 = 1.125 \text{ mA}$$

Next, we consider the circuit with $v_I = +2.5$ V. Transistor Q_P will have a V_{SG} of zero and thus will be cut off, reducing the circuit to that shown in Fig. 5.26(c). We note that v_O will be negative, and thus v_{GD} will be greater than V_{tn} , causing Q_N to operate in the triode region. For simplicity we shall assume that v_{DS} is small and thus use

$$\begin{aligned} I_{DN} &\approx k'_n(W_n/L_n)(V_{GS} - V_{tn})V_{DS} \\ &= 1[2.5 - (-2.5) - 1][v_O - (-2.5)] \end{aligned}$$

From the circuit diagram shown in Fig. 5.26(c), we can also write

$$I_{DN}(\text{mA}) = \frac{0 - v_O}{10(\text{k}\Omega)}$$

These two equations can be solved simultaneously to yield

$$I_{DN} = 0.244 \text{ mA} \quad v_O = -2.44 \text{ V}$$

Note that $V_{DS} = -2.44 - (-2.5) = 0.06$ V, which is small as assumed.

Finally, the situation for the case $v_I = -2.5$ V [Fig. 5.26(d)] will be the exact complement of the case $v_I = +2.5$ V: Transistor Q_N will be off. Thus $I_{DN} = 0$, Q_P will be operating in the triode region with $I_{DP} = 2.44$ mA and $v_O = +2.44$ V.

EXERCISE

- 5.15** The NMOS and PMOS transistors in the circuit of Fig. E5.15 are matched with $k'_n(W_n/L_n) = k'_p(W_p/L_p) = 1 \text{ mA/V}^2$ and $V_{tn} = -V_{tp} = 1 \text{ V}$. Assuming $\lambda = 0$ for both devices, find the drain currents i_{DN} and i_{DP} and the voltage v_O for $v_I = 0 \text{ V}$, $+2.5 \text{ V}$, and -2.5 V .

Ans. $v_I = 0 \text{ V}$: 0 mA, 0 mA, 0 V; $v_I = +2.5 \text{ V}$: 0.104 mA, 0 mA, 1.04 V; $v_I = -2.5 \text{ V}$: 0 mA, 0.104 mA, -1.04 V

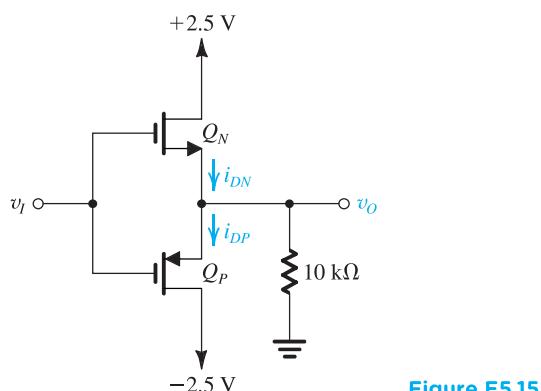


Figure E5.15

5.4 Applying the MOSFET in Amplifier Design

We now begin our study of the utilization of the MOSFET in the design of amplifiers. The basis for this important application is that when operated in saturation, the MOSFET functions as voltage-controlled current source: The gate-to-source voltage v_{GS} controls the drain current i_D . Although the control relationship is nonlinear (square law), we will shortly devise a method for obtaining almost-linear amplification from this fundamentally nonlinear device.

5.4.1 Obtaining a Voltage Amplifier

In the introduction to amplifier circuits in Section 1.5, we learned that a voltage-controlled current source can serve as a transconductance amplifier; that is, an amplifier whose input signal is a voltage and whose output signal is a current. More commonly, however, one is interested in voltage amplifiers. A simple way to convert a transconductance amplifier to a voltage amplifier is to pass the output current through a resistor and take the voltage across the resistor as the output. Doing this for a MOSFET results in the simple amplifier circuit shown in Fig. 5.27(a). Here v_{GS} is the input voltage, R_D (known as a **load resistance**) converts the drain current i_D to a voltage ($i_D R_D$), and V_{DD} is the supply voltage that powers up the amplifier and, together with R_D , establishes operation in the saturation region, as will be shown shortly.

In the amplifier circuit of Fig. 5.27(a) the output voltage is taken between the drain and ground, rather than simply across R_D . This is done because of the need to maintain a ground reference throughout the circuit. The output voltage v_{DS} is given by

$$v_{DS} = V_{DD} - i_D R_D \quad (5.30)$$

Thus it is an inverted version (note the minus sign) of $i_D R_D$ that is shifted by the constant value of the supply voltage V_{DD} .

5.4.2 The Voltage Transfer Characteristic (VTC)

A very useful tool that yields great insight into the operation of an amplifier circuit is its voltage transfer characteristic (VTC). This is simply a plot (or a clearly labeled sketch) of the output voltage versus the input voltage. For the MOS amplifier in Fig. 5.27(a), this is the plot of v_{DS} versus v_{GS} shown in Fig. 5.27(b).

Observe that for $v_{GS} < V_t$, the transistor is cut off, $i_D = 0$ and, from Eq. (5.30), $v_{DS} = V_{DD}$. As v_{GS} exceeds V_t , the transistor turns on and v_{DS} decreases. However, since initially v_{DS} is still high, the MOSFET will be operating in saturation. This continues as v_{GS} is increased until the value of v_{GS} is reached that results in v_{DS} becoming lower than v_{GS} by V_t volts (point B on the VTC in Fig. 5.27b). For v_{GS} greater than that at point B, the transistor operates in the triode region and v_{DS} decreases more slowly.

The VTC in Fig. 5.27(b) indicates that the segment of greatest slope (and hence potentially the largest amplifier gain) is that labeled AB, which corresponds to operation in the saturation region. An expression for the segment AB can be obtained by substituting for i_D in Eq. (5.30) by its saturation-region value

$$i_D = \frac{1}{2} k_n (v_{GS} - V_t)^2 \quad (5.31)$$

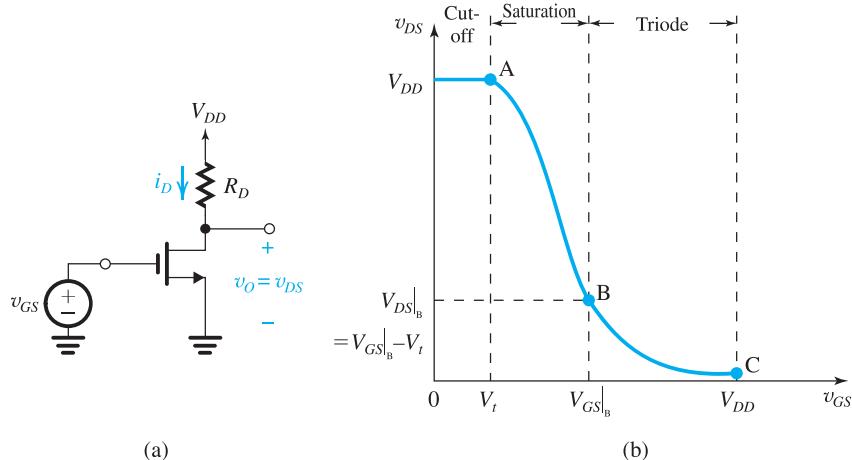


Figure 5.27 (a) Simple MOSFET amplifier with input v_{GS} and output v_{DS} . (b) The voltage transfer characteristic (VTC) of the amplifier in (a). The three segments of the VTC correspond to the three regions of operation of the MOSFET.

where we have for simplicity neglected channel-length modulation. The result is

$$v_{DS} = V_{DD} - \frac{1}{2}k_n R_D (v_{GS} - V_t)^2 \quad (5.32)$$

This is obviously a nonlinear relationship. Nevertheless, linear (or almost-linear) amplification can be obtained by using the technique of biasing the MOSFET. Before considering biasing, however, it is useful to determine the coordinates of point B, which is at the boundary between the saturation and the triode regions of operation. These can be obtained by substituting in Eq. (5.32), $v_{GS} = V_{GS}|_B$ and $v_{DS} = V_{DS}|_B = V_{GS}|_B - V_t$. The result is

$$V_{GS}|_B = V_t + \frac{\sqrt{2k_n R_D V_{DD} + 1} - 1}{k_n R_D} \quad (5.33)$$

EXERCISE

- 5.16** Consider the amplifier of Fig. 5.27(a) with $V_{DD} = 1.8$ V, $R_D = 17.5$ k Ω , and with a MOSFET specified to have $V_t = 0.4$ V, $k_n = 4$ mA/V 2 , and $\lambda = 0$. Determine the coordinates of the end points of the saturation-region segment of the VTC. Also, determine $V_{DS}|_C$ assuming $V_{GS}|_C = V_{DD}$.

Ans. A: 0.4 V, 1.8 V; B: 0.613 V, 0.213 V; $V_{DS}|_C = 18$ mV

5.4.3 Biasing the MOSFET to Obtain Linear Amplification

Biasing enables us to obtain almost-linear amplification from the MOSFET. The technique is illustrated in Fig. 5.28(a). A dc voltage V_{GS} is selected to obtain operation at a point Q on the segment AB of the VTC. How to select an appropriate location for the bias point Q will be discussed shortly. For the time being, observe that the coordinates of Q are the dc

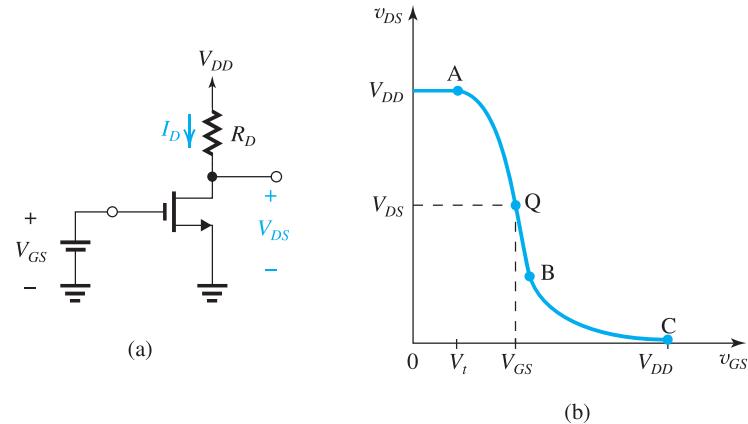


Figure 5.28 Biasing the MOSFET amplifier at a point Q located on the segment AB of the VTC.

voltages \$V_{GS}\$ and \$V_{DS}\$, which are related by

$$V_{DS} = V_{DD} - \frac{1}{2}k_n R_D (V_{GS} - V_t)^2 \quad (5.34)$$

Point Q is known as the **bias point** or the **dc operating point**. Also, since at Q no signal component is present, it is also known as the **quiescent point** (which is the origin of the symbol Q).

Next, the signal to be amplified, \$v_{gs}\$, a function of time \$t\$, is superimposed on the bias voltage \$V_{GS}\$, as shown in Fig. 5.29(a). Thus the total instantaneous value of \$v_{GS}\$ becomes

$$v_{GS}(t) = V_{GS} + v_{gs}(t)$$

The resulting \$v_{DS}(t)\$ can be obtained by substituting for \$v_{GS}(t)\$ into Eq. (5.32). Graphically, we can use the VTC to obtain \$v_{DS}(t)\$ point-by-point, as illustrated in Fig. 5.29(b). Here we show the case of \$v_{gs}\$ being a triangular wave of “small” amplitude. Specifically, the amplitude of \$v_{gs}\$ is small enough to restrict the excursion of the instantaneous operating point to a short, almost-linear segment of the VTC around the bias point Q. The shorter the segment, the greater the linearity achieved, and the closer to an ideal triangular wave the signal component at the output, \$v_{ds}\$, will be. This is the essence of obtaining linear amplification from the nonlinear MOSFET.

5.4.4 The Small-Signal Voltage Gain

If the input signal \$v_{gs}\$ is kept small, the corresponding signal at the output \$v_{ds}\$ will be nearly proportional to \$v_{gs}\$ with the constant of proportionality being the slope of the almost-linear segment of the VTC around Q. This is the voltage gain of the amplifier, and its value can be determined by evaluating the slope of the tangent to the VTC at the bias point Q,

$$A_v \equiv \left. \frac{dv_{DS}}{dv_{GS}} \right|_{v_{GS}=V_{GS}} \quad (5.35)$$

Utilizing Eq. (5.32) we obtain

$$A_v = -k_n(V_{GS} - V_t)R_D \quad (5.36)$$

which can be expressed in terms of the overdrive voltage at the bias point \$V_{OV}\$ as

$$A_v = -k_n V_{OV} R_D \quad (5.37)$$

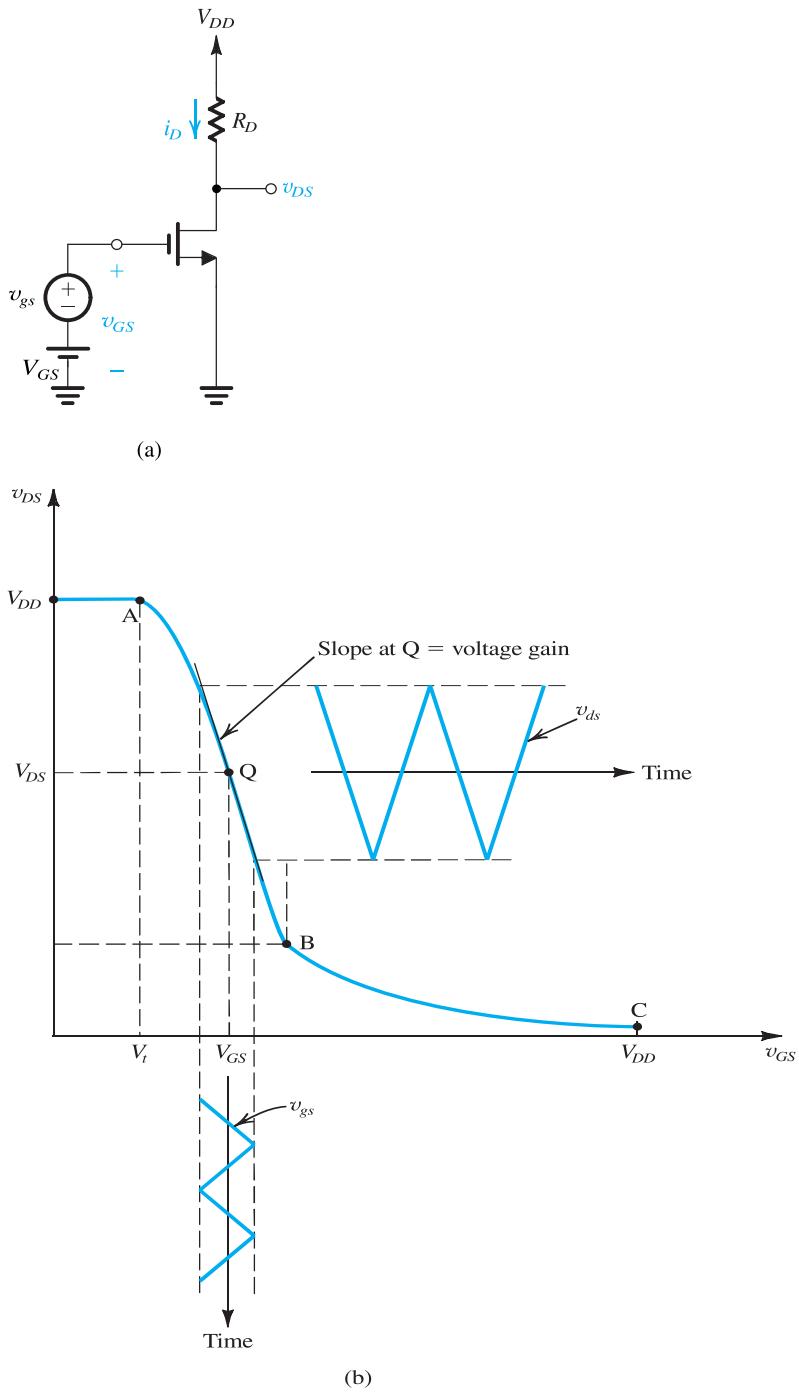


Figure 5.29 The MOSFET amplifier with a small time-varying signal $v_{gs}(t)$ superimposed on the dc bias voltage V_{GS} . The MOSFET operates on a short almost-linear segment of the VTC around the bias point Q and provides an output voltage $v_{ds} = A_v v_{gs}$.

We make the following observations on this expression for the voltage gain.

1. The gain is negative, which signifies that the amplifier is inverting; that is, there is a 180° phase shift between the input and the output. This inversion is obvious in Fig. 5.29(b) and should have been anticipated from Eq. (5.32).
2. The gain is proportional to the load resistance R_D , to the transistor transconductance parameter k_n' , and to the overdrive voltage V_{OV} . This all makes intuitive sense.

Another simple and insightful expression for the voltage gain A_v can be derived by recalling that the dc current in the drain at the bias point is related to V_{OV} by

$$I_D = \frac{1}{2}k_n'V_{OV}^2$$

This equation can be combined with Eq. (5.37) to yield

$$\textcircled{1} \quad A_v = -\frac{I_D R_D}{V_{OV}/2} \quad (5.38)$$

That is, the gain is simply the ratio of the dc voltage drop across the load resistance R_D to $V_{OV}/2$. This relationship allows one to find an absolute upper limit on the magnitude of voltage gain achievable from this amplifier circuit. Simply note that $I_D R_D$ can approach but never exceed the power-supply voltage V_{DD} ; thus,

$$|A_{v\max}| = \frac{V_{DD}}{V_{OV}/2}$$

For modern CMOS technologies V_{OV} is usually no lower than about 0.2 V, with the result that the maximum achievable gain is about $10 V_{DD}$. Thus for a 0.13- μm CMOS technology that utilizes $V_{DD} = 1.3$ V, the approximate value of $|A_{\max}|$ is 13 V/V. In actual circuits, however, the maximum gain achievable is lower than this absolute maximum.

Example 5.9

Consider the amplifier circuit shown in Fig. 5.29(a). The transistor is specified to have $V_t = 0.4$ V, $k_n' = 0.4$ mA/V 2 , $W/L = 10$, and $\lambda = 0$. Also, let $V_{DD} = 1.8$ V, $R_D = 17.5$ k Ω , and $V_{GS} = 0.6$ V.

(a) For $v_{gs} = 0$ (and hence $v_{ds} = 0$), find V_{OV} , I_D , V_{DS} , and A_v .

(b) What is the maximum symmetrical signal swing allowed at the drain? Hence find the maximum allowable amplitude of a sinusoidal v_{gs} .

Solution

(a) With $V_{GS} = 0.6$ V, $V_{OV} = 0.6 - 0.4 = 0.2$ V.

Thus,

$$I_D = \frac{1}{2} \times 0.4 \times 10 \times 0.2^2 = 0.08 \text{ mA}$$

$$\begin{aligned} V_{DS} &= V_{DD} - R_D I_D \\ &= 1.8 - 17.5 \times 0.08 = 0.4 \text{ V} \end{aligned}$$

Since V_{DS} is greater than V_{OV} , the transistor is indeed operating in saturation. The voltage gain can be found from Eq. (5.37),

$$\begin{aligned} A_v &= -k_n V_{OV} R_D \\ &= -0.4 \times 10 \times 0.2 \times 17.5 \\ &= -14 \text{ V/V} \end{aligned}$$

An identical result can be found using Eq. (5.38).

(b) Since $V_{OV} = 0.2$ V and $V_{DS} = 0.4$ V, we see that the maximum allowable negative signal swing at the drain is 0.2 V. In the positive direction, a swing of +0.2 V would not cause the transistor to cut off and thus is allowed. Thus the maximum symmetrical signal swing allowable at the drain is ± 0.2 V. The corresponding amplitude of v_{gs} can be found from

$$\hat{v}_{gs} = \frac{\hat{v}_{ds}}{|A_v|} = \frac{0.2 \text{ V}}{14} = 14.2 \text{ mV}$$

Since $\hat{v}_{gs} \ll V_{OV}$, the operation will be reasonably linear (more on this in later sections).

Greater insight into the issue of allowable signal swing can be obtained by examining the signal waveforms shown in Fig. 5.30. Note that for the MOSFET to remain in saturation at the negative peak of v_{ds} , we must ensure that

$$v_{DS\min} \geq v_{GS\max} - V_t$$

that is,

$$0.4 - |A_v| \hat{v}_{gs} \geq 0.6 + \hat{v}_{gs} - 0.4$$

which results in

$$\hat{v}_{gs} \leq \frac{0.2}{|A_v| + 1} = 13.3 \text{ mV}$$

This is a more precise result than the one obtained earlier.

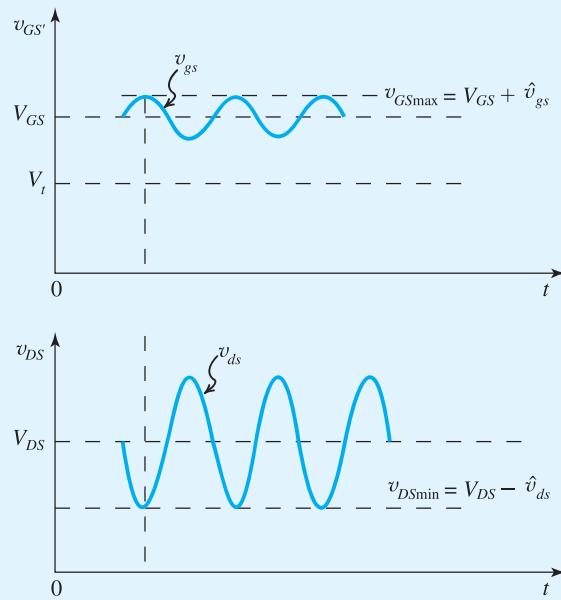


Figure 5.30 Signal waveforms at gate and drain for the amplifier in Example 5.9. Note that to ensure operation in the saturation region at all times, $v_{DS\min} \geq v_{GS\max} - V_t$.

EXERCISE

- 5.17** For the amplifier circuit studied in Example 5.9, provide two alternative designs, each providing a voltage gain of 10 by (a) changing R_D while keeping V_{OV} constant, and (b) changing V_{OV} while keeping R_D constant. For each design, specify V_{GS} , I_D , R_D , and V_{DS} .

Ans. (a) 0.6 V, 0.08 mA, 12.5 k Ω , 0.8 V; (b) 0.54 V, 0.04 mA, 17.5 k Ω , 1.1 V

5.4.5 Determining the VTC by Graphical Analysis

Figure 5.31 shows a graphical method for determining the VTC of the amplifier of Fig. 5.29(a). Although graphical analysis of transistor circuits is rarely employed in practice, it is useful for us at this stage for gaining greater insight into circuit operation, especially in answering the question of where to locate the bias point Q.

The graphical analysis is based on the observation that for each value of v_{GS} , the circuit will be operating at the point of intersection of the i_D-v_{DS} graph corresponding to the particular value of v_{GS} and the straight line representing Eq. (5.30), which can be rewritten in the form

$$i_D = \frac{V_{DD}}{R_D} - \frac{1}{R_D}v_{DS} \quad (5.39)$$

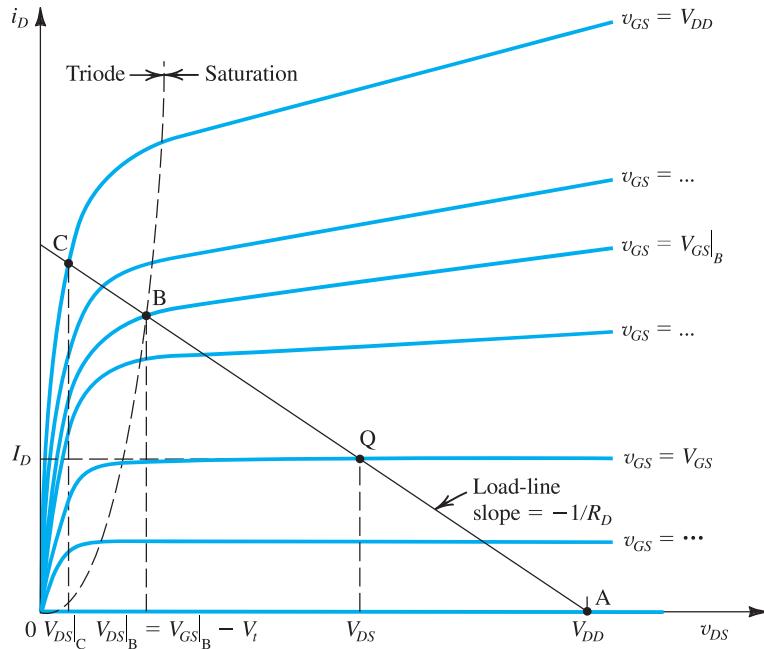


Figure 5.31 Graphical construction to determine the voltage transfer characteristic of the amplifier in Fig. 5.29(a).

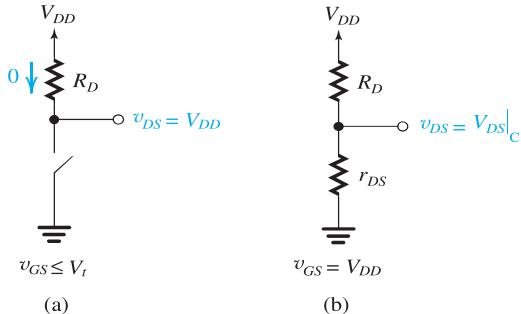


Figure 5.32 Operation of the MOSFET in Figure 5.29(a) as a switch: (a) Open, corresponding to point A in Figure 5.31; (b) Closed, corresponding to point C in Figure 5.31. The closure resistance is approximately equal to r_{DS} because V_{DS} is usually very small.

The straight line representing this relationship is superimposed on the i_D-v_{DS} characteristics in Fig. 5.31. It intersects the horizontal axis at $v_{DS}=V_{DD}$ and has a slope of $-1/R_D$. Since this straight line represents in effect the load resistance R_D , it is called the **load line**. The VTC is then determined point by point. Note that we have labeled four important points: point A at which $v_{GS}=V_t$, point Q at which the MOSFET can be biased for amplifier operation ($v_{GS}=V_{GS}$ and $v_{DS}=V_{DS}$), point B at which the MOSFET leaves saturation and enters the triode region, and point C, which is deep into the triode region and for which $v_{GS}=V_{DD}$. If the MOSFET is to be used as a switch, then operating points A and C are applicable: At A the transistor is off (open switch), and at C the transistor operates as a low-valued resistance r_{DS} and has a small voltage drop (closed switch). The incremental resistance at point C is also known as the **closure resistance**. The operation of the MOSFET as a switch is illustrated in Fig. 5.32. A detailed study of the application of the MOSFET as a switch is undertaken in Chapter 13 dealing with CMOS digital logic circuits.

5.4.6 Locating the Bias Point Q

The bias point Q is determined by the value of V_{GS} and that of the load resistance R_D . Two important considerations in deciding on the location of Q are the required gain and the allowable signal swing at the output. To illustrate, consider the VTC shown in Fig. 5.29(b). Here the value of R_D is fixed and the only variable remaining is the value of V_{GS} . Since the slope increases as we move closer to point B, we obtain higher gain by locating Q as close to B as possible. However, the closer Q is to the boundary point B, the smaller the allowable magnitude of negative signal swing. Thus, as often happens in engineering design, we encounter a situation requiring a trade-off.

In deciding on a value for R_D , it is useful to refer to the i_D-v_{DS} plane. Figure 5.33 shows two load lines resulting in two extreme bias points: Point Q_1 is too close to V_{DD} , resulting in a severe constraint on the positive signal swing of v_{ds} . Exceeding the allowable positive maximum results in the positive peaks of the signal being clipped off, since the MOSFET will turn off for the part of each cycle near the positive peak. We speak of this situation by saying that the circuit does not have sufficient “headroom.” Similarly, point Q_2 is too close to the boundary of the triode region, thus severely limiting the allowable negative signal swing of v_{ds} . Exceeding this limit would result in the transistor entering the triode region for part of each cycle near the negative peaks, resulting in a distorted output signal. In this situation we say that the circuit does not have sufficient “legroom.” We will have more to say on bias design in the Section 5.7.

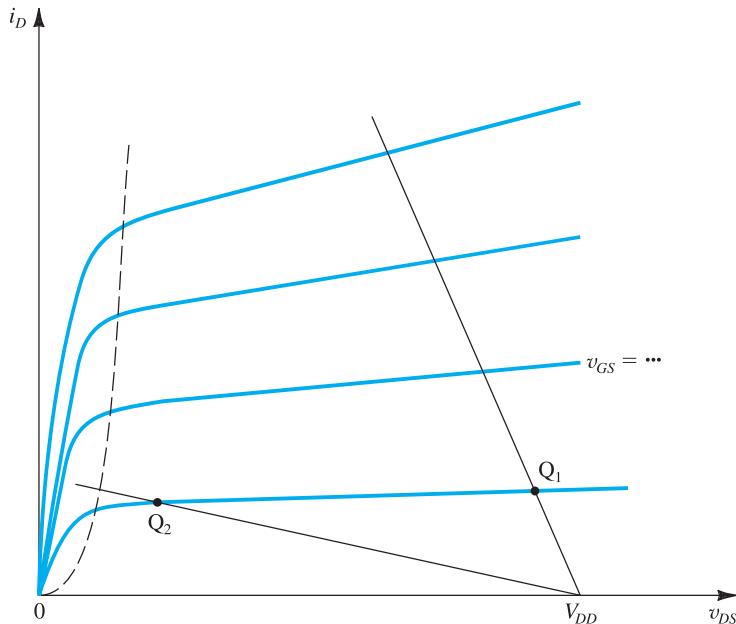


Figure 5.33 Two load lines and corresponding bias points. Bias point Q_1 does not leave sufficient room for positive signal swing at the drain (too close to V_{DD}). Bias point Q_2 is too close to the boundary of the triode region and might not allow for sufficient negative signal swing.

5.5 Small-Signal Operation and Models

In our study of the operation of the MOSFET amplifier in Section 5.4 we learned that linear amplification can be obtained by biasing the MOSFET to operate in the saturation region and by keeping the input signal small. In this section, we explore the small-signal operation in some detail. For this purpose we utilize the conceptual amplifier circuit shown in Fig. 5.34. Here the MOS transistor is biased by applying a dc voltage⁸ V_{GS} , and the input signal to be amplified, v_{gs} , is superimposed on the dc bias voltage V_{GS} . The output voltage is taken at the drain.

5.5.1 The DC Bias Point

The dc bias current I_D can be found by setting the signal v_{gs} to zero; thus,

$$I_D = \frac{1}{2} k_n (V_{GS} - V_t)^2 = \frac{1}{2} k_n V_{OV}^2 \quad (5.40)$$

where we have neglected channel-length modulation (i.e., we have assumed $\lambda = 0$). Here $V_{OV} = V_{GS} - V_t$ is the overdrive voltage at which the MOSFET is biased to operate. The dc

⁸Practical biasing arrangements will be studied in Section 5.7.

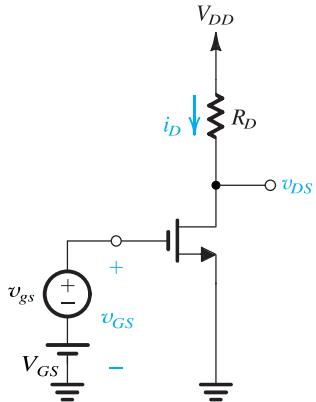


Figure 5.34 Conceptual circuit utilized to study the operation of the MOSFET as a small-signal amplifier.

voltage at the drain, V_{DS} , will be

$$V_{DS} = V_{DD} - R_D I_D \quad (5.41)$$

To ensure saturation-region operation, we must have

$$V_{DS} > V_{OV}$$

Furthermore, since the total voltage at the drain will have a signal component superimposed on V_{DS} , V_{DS} has to be sufficiently greater than (V_{OV}) to allow for the required signal swing.

5.5.2 The Signal Current in the Drain Terminal

Next, consider the situation with the input signal v_{gs} applied. The total instantaneous gate-to-source voltage will be

$$v_{GS} = V_{GS} + v_{gs} \quad (5.42)$$

resulting in a total instantaneous drain current i_D ,

$$\begin{aligned} i_D &= \frac{1}{2} k_n (V_{GS} + v_{gs} - V_t)^2 \\ &= \frac{1}{2} k_n (V_{GS} - V_t)^2 + k_n (V_{GS} - V_t)v_{gs} + \frac{1}{2} k_n v_{gs}^2 \end{aligned} \quad (5.43)$$

The first term on the right-hand side of Eq. (5.43) can be recognized as the dc bias current I_D (Eq. 5.40). The second term represents a current component that is directly proportional to the input signal v_{gs} . The third term is a current component that is proportional to the square of the input signal. This last component is undesirable because it represents *nonlinear distortion*. To reduce the nonlinear distortion introduced by the MOSFET, the input signal should be kept small so that

$$\frac{1}{2} k_n v_{gs}^2 \ll k_n (V_{GS} - V_t)v_{gs}$$

resulting in

$$\textcircled{1} \quad v_{gs} \ll 2(V_{GS} - V_t) \quad (5.44)$$

or, equivalently,

$$\textcircled{1} \quad v_{gs} \ll 2V_{ov} \quad (5.45)$$

If this **small-signal condition** is satisfied, we may neglect the last term in Eq. (5.43) and express i_D as

$$i_D \simeq I_D + i_d \quad (5.46)$$

where

$$i_d = k_n(V_{GS} - V_t)v_{gs}$$

The parameter that relates i_d and v_{gs} is the MOSFET **transconductance** g_m ,

$$g_m \equiv \frac{i_d}{v_{gs}} = k_n(V_{GS} - V_t) \quad (5.47)$$

or in terms of the overdrive voltage V_{ov} ,

$$\textcircled{1} \quad g_m = k_n V_{ov} \quad (5.48)$$

Figure 5.35 presents a graphical interpretation of the small-signal operation of the MOSFET amplifier. Note that g_m is equal to the slope of the $i_D - v_{GS}$ characteristic at the bias point,

$$g_m = \left. \frac{\partial i_D}{\partial v_{GS}} \right|_{v_{GS}=V_{GS}} \quad (5.49)$$

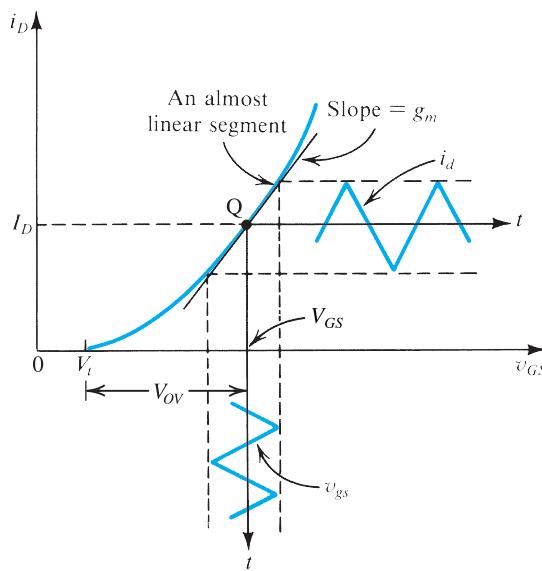


Figure 5.35 Small-signal operation of the MOSFET amplifier.

This is the formal definition of g_m , which can be shown to yield the expressions given in Eqs. (5.47) and (5.48).

5.5.3 The Voltage Gain

Returning to the circuit of Fig. 5.34, we can express the total instantaneous drain voltage v_{DS} as follows:

$$v_{DS} = V_{DD} - R_D i_D$$

Under the small-signal condition, we have

$$v_{DS} = V_{DD} - R_D(I_D + i_d)$$

which can be rewritten as

$$v_{DS} = V_{DS} - R_D i_d$$

Thus the signal component of the drain voltage is

$$v_{ds} = -i_d R_D = -g_m v_{gs} R_D \quad (5.50)$$

which indicates that the voltage gain is given by

$$A_v \equiv \frac{v_{ds}}{v_{gs}} = -g_m R_D \quad (5.51)$$

The minus sign in Eq. (5.51) indicates that the output signal v_{ds} is 180° out of phase with respect to the input signal v_{gs} . This is illustrated in Fig. 5.36, which shows v_{GS} and v_{DS} . The input signal is assumed to have a triangular waveform with an amplitude much smaller than $2(V_{GS} - V_t)$, the small-signal condition in Eq. (5.44), to ensure linear operation. For operation in the saturation region at all times, the minimum value of v_{DS} should not fall below the corresponding value of v_{GS} by more than V_r . Also, the maximum value of v_{DS} should be smaller than V_{DD} ; otherwise the FET will enter the cutoff region and the peaks of the output signal waveform will be clipped off.

Finally, we note that by substituting for g_m from Eq. (5.48) the voltage gain expression in Eq. (5.51) becomes identical to that derived in Section 5.4—namely, Eq. (5.37).

5.5.4 Separating the DC Analysis and the Signal Analysis

From the preceding analysis, we see that under the small-signal approximation, signal quantities are superimposed on dc quantities. For instance, the total drain current i_D equals the dc current I_D plus the signal current i_d , the total drain voltage $v_{DS} = V_{DS} + v_{ds}$, and so on. It follows that the analysis and design can be greatly simplified by separating dc or bias calculations from small-signal calculations. That is, once a stable dc operating point has been established and all dc quantities calculated, we may then perform signal analysis ignoring dc quantities.

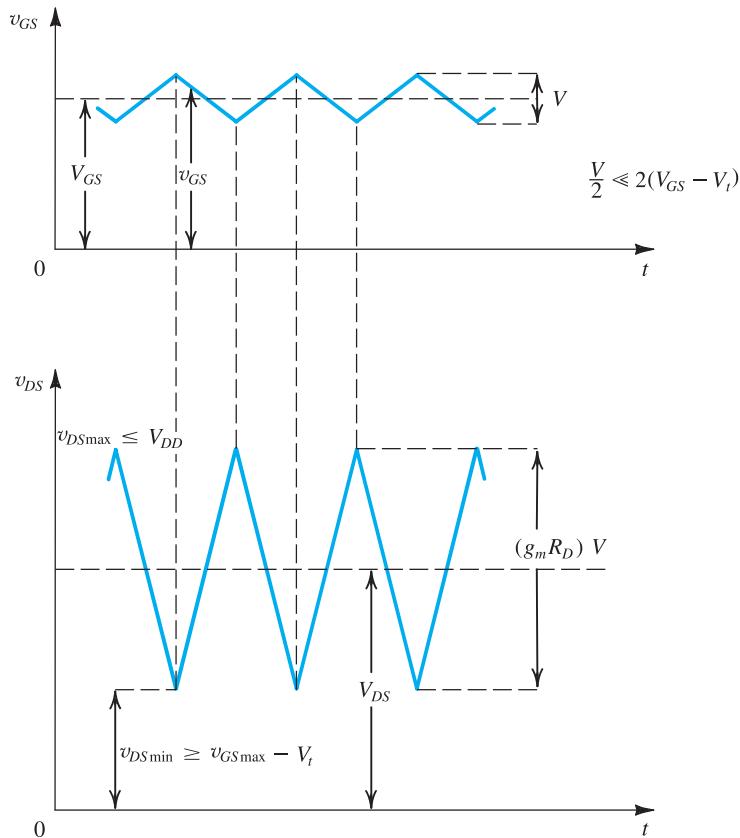


Figure 5.36 Total instantaneous voltages v_{GS} and v_{DS} for the circuit in Fig. 5.34.

5.5.5 Small-Signal Equivalent-Circuit Models

From a signal point of view, the FET behaves as a voltage-controlled current source. It accepts a signal v_{gs} between gate and source and provides a current $g_m v_{gs}$ at the drain terminal. The input resistance of this controlled source is very high—ideally, infinite. The output resistance—that is, the resistance looking into the drain—also is high, and we have assumed it to be infinite thus far. Putting all of this together, we arrive at the circuit in Fig. 5.37(a), which represents the small-signal operation of the MOSFET and is thus a **small-signal model** or a **small-signal equivalent circuit**.

In the analysis of a MOSFET amplifier circuit, the transistor can be replaced by the equivalent circuit model shown in Fig. 5.37(a). The rest of the circuit remains unchanged except that *ideal constant dc voltage sources are replaced by short circuits*. This is a result of the fact that the voltage across an ideal constant dc voltage source does not change, and thus there will always be a zero voltage signal across a constant dc voltage source. A dual statement applies for constant dc current sources; namely, the signal current of an ideal constant dc current source will always be zero, and thus *an ideal constant dc current source can be replaced by an open circuit* in the small-signal equivalent circuit of the amplifier. The

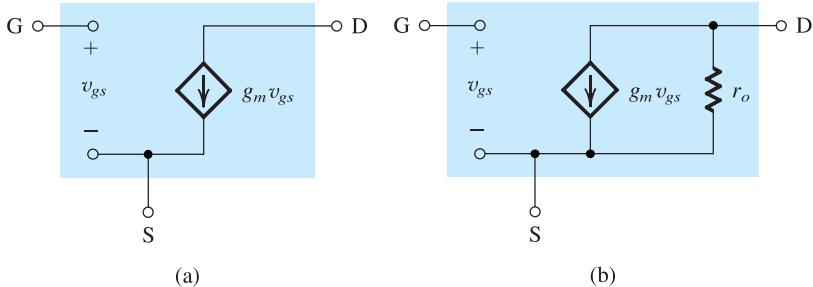


Figure 5.37 Small-signal models for the MOSFET: (a) neglecting the dependence of i_D on v_{DS} in saturation (the channel-length modulation effect); and (b) including the effect of channel-length modulation, modeled by output resistance $r_o = |V_A|/I_D$.

circuit resulting can then be used to perform any required signal analysis, such as calculating voltage gain.

The most serious shortcoming of the small-signal model of Fig. 5.37(a) is that it assumes the drain current in saturation to be independent of the drain voltage. From our study of the MOSFET characteristics in saturation, we know that the drain current does in fact depend on v_{DS} in a linear manner. Such dependence was modeled by a finite resistance r_o between drain and source, whose value was given by Eq. (5.27) in Section 5.2.4, which we repeat here as

$$r_o = \frac{|V_A|}{I_D} \quad (5.52)$$

where $V_A = 1/\lambda$ is a MOSFET parameter that either is specified or can be measured. It should be recalled that for a given process technology, V_A is proportional to the MOSFET channel length. The current I_D is the value of the dc drain current without the channel-length modulation taken into account; that is,

$$I_D = \frac{1}{2} k_n V_{OV}^2 \quad (5.53)$$

Typically, r_o is in the range of 10 kΩ to 1000 kΩ. It follows that the accuracy of the small-signal model can be improved by including r_o in parallel with the controlled source, as shown in Fig. 5.37(b).

It is important to note that the small-signal model parameters g_m and r_o depend on the dc bias point of the MOSFET.

Returning to the amplifier of Fig. 5.34, we find that replacing the MOSFET with the small-signal model of Fig. 5.37(b) results in the voltage-gain expression

$$A_v = \frac{v_{ds}}{v_{gs}} = -g_m(R_D \parallel r_o) \quad (5.54)$$

Thus, the finite output resistance r_o results in a reduction in the magnitude of the voltage gain.

Although the analysis above is performed on an NMOS transistor, the results, and the equivalent circuit models of Fig. 5.37, apply equally well to PMOS devices, except for using $|V_{GS}|$, $|V_t|$, $|V_{OV}|$, and $|V_A|$ and replacing k_n with k_p .

5.5.6 The Transconductance g_m

We shall now take a closer look at the MOSFET transconductance given by Eq. (5.47), which we rewrite with $k_n = k'_n (W/L)$ as follows:

$$\textcircled{1} \quad g_m = k'_n (W/L) (V_{GS} - V_t) = k'_n (W/L) V_{OV} \quad (5.55)$$

This relationship indicates that g_m is proportional to the process transconductance parameter $k'_n = \mu_n C_{ox}$ and to the W/L ratio of the MOS transistor; hence to obtain relatively large transconductance the device must be short and wide. We also observe that for a given device the transconductance is proportional to the overdrive voltage, $V_{OV} = V_{GS} - V_t$, the amount by which the bias voltage V_{GS} exceeds the threshold voltage V_t . Note, however, that increasing g_m by biasing the device at a larger V_{GS} has the disadvantage of reducing the allowable voltage signal swing at the drain.

Another useful expression for g_m can be obtained by substituting for V_{OV} in Eq. (5.55) by $\sqrt{2I_D/(k'_n (W/L))}$ [from Eq. (5.40)]:

$$\textcircled{1} \quad g_m = \sqrt{2k'_n} \sqrt{W/L} \sqrt{I_D} \quad (5.56)$$

This expression shows two things:

1. For a given MOSFET, g_m is proportional to the square root of the dc bias current.
2. At a given bias current, g_m is proportional to $\sqrt{W/L}$.

In contrast, the transconductance of the bipolar junction transistor (BJT) studied in Chapter 6 is proportional to the bias current and is independent of the physical size and geometry of the device.

To gain some insight into the values of g_m obtained in MOSFETs consider an integrated-circuit device operating at $I_D = 0.5$ mA and having $k'_n = 120 \mu\text{A/V}^2$. Equation (5.56) shows that for $W/L = 1$, $g_m = 0.35$ mA/V, whereas a device for which $W/L = 100$ has $g_m = 3.5$ mA/V. In contrast, a BJT operating at a collector current of 0.5 mA has $g_m = 20$ mA/V.

Yet another useful expression for g_m of the MOSFET can be obtained by substituting for $k'_n (W/L)$ in Eq. (5.55) by $2I_D/(V_{GS} - V_t)^2$:

$$\textcircled{1} \quad g_m = \frac{2I_D}{V_{GS} - V_t} = \frac{2I_D}{V_{OV}} \quad (5.57)$$

A convenient graphical construction that clearly illustrates this relationship is shown in Fig. 5.38.

In summary, there are three different relationships for determining g_m —Eqs. (5.55), (5.56), and (5.57)—and there are three design parameters— (W/L) , V_{OV} , and I_D , any two of which can be chosen independently. That is, the designer may choose to operate the MOSFET with a certain overdrive voltage V_{OV} and at a particular current I_D ; the required W/L ratio can then be found and the resulting g_m determined.

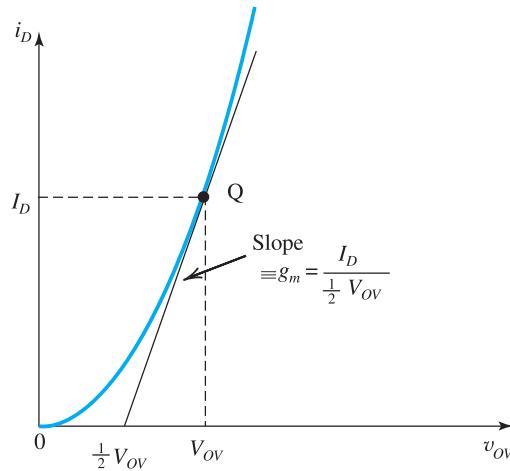
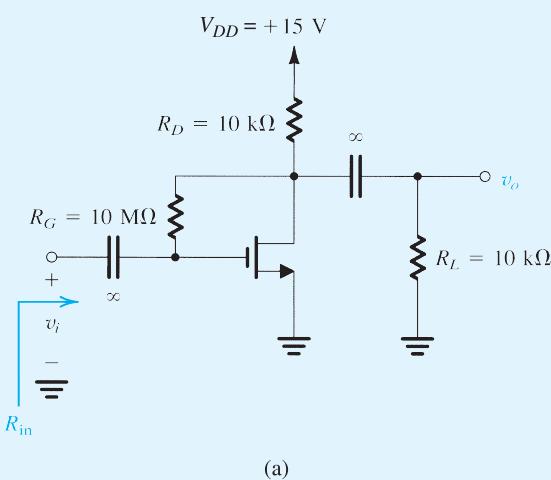


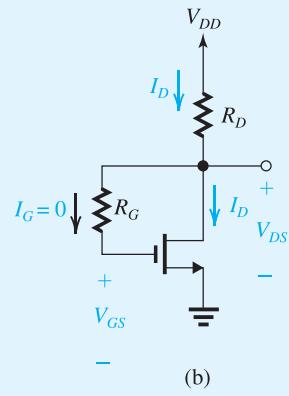
Figure 5.38 The slope of the tangent at the bias point Q intersects the v_{ov} axis at $\frac{1}{2} V_{ov}$. Thus, $g_m = I_D / (\frac{1}{2} V_{ov})$.

Example 5.10

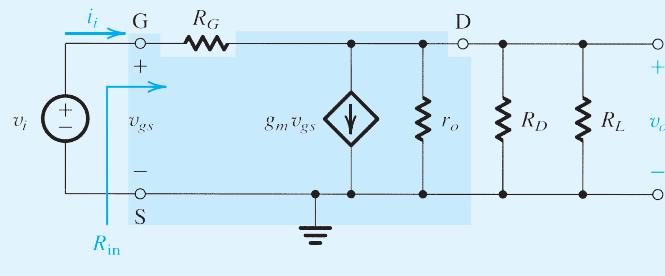
Figure 5.39(a) shows a discrete common-source MOSFET amplifier utilizing a drain-to-gate resistance R_G for biasing purposes. Such a biasing arrangement will be studied in Section 5.7. The input signal v_i is coupled to the gate via a large capacitor, and the output signal at the drain is coupled to the load resistance R_L via another large capacitor. We wish to analyze this amplifier circuit to determine its small-signal voltage gain, its input resistance, and the largest allowable input signal. The transistor has $V_t = 1.5$ V, $k'_n(W/L) = 0.25$ mA/V², and $V_A = 50$ V. Assume the coupling capacitors to be sufficiently large so as to act as short circuits at the signal frequencies of interest.



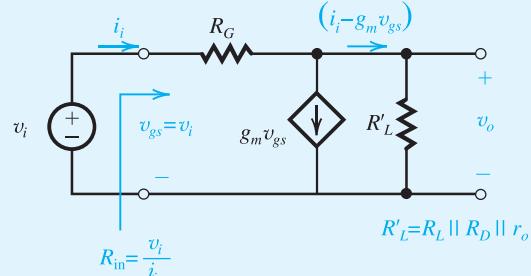
Example 5.10 *continued*



(b)



(c)



(d)

Figure 5.39 Example 5.10: (a) amplifier circuit; (b) circuit for determining the dc operating point; (c) the amplifier small-signal equivalent circuit; (d) a simplified version of the circuit in (c).

Solution

We first determine the dc operating point. For this purpose, we eliminate the input signal v_i , and open-circuit the two coupling capacitors (since they block dc currents). The result is the circuit shown in Fig. 5.39(b). We note that since $I_G = 0$, the dc voltage drop across R_G will be zero, and

$$V_{GS} = V_{DS} = V_{DD} - R_D I_D \quad (5.58)$$

With $V_{DS} = V_{GS}$, the NMOS transistor will be operating in saturation. Thus,

$$I_D = \frac{1}{2} k_n (V_{GS} - V_t)^2 \quad (5.59)$$

where, for simplicity, we have neglected the effect of channel-length modulation on the dc operating point. Substituting $V_{DD} = 15$ V, $R_D = 10$ kΩ, $k_n = 0.25$ mA/V², and $V_t = 1.5$ V in Eqs. (5.58) and (5.59), and substituting for V_{GS} from Eq. (5.58) into Eq. (5.59) results in a quadratic equation in I_D . Solving the latter and discarding the root that is not physically meaningful yields the solution

$$I_D = 1.06 \text{ mA}$$

which corresponds to

$$V_{GS} = V_{DS} = 4.4 \text{ V}$$

and

$$V_{OV} = 4.4 - 1.5 = 2.9 \text{ V}$$

Next we proceed with the small-signal analysis of the amplifier. Toward that end we replace the MOSFET with its small-signal model to obtain the small-signal equivalent circuit of the amplifier, shown in Fig. 5.39(c). Observe that we have replaced the coupling capacitors with short circuits. The dc voltage supply V_{DD} has also been replaced with a short circuit to ground.

The values of the transistor small-signal parameters g_m and r_o can be determined by using the dc bias quantities found above, as follows:

$$\begin{aligned} g_m &= k_n V_{OV} \\ &= 0.25 \times 2.9 = 0.725 \text{ mA/V} \\ r_o &= \frac{V_A}{I_D} = \frac{50}{1.06} = 47 \text{ k}\Omega \end{aligned}$$

Next we use the equivalent circuit of Fig. 5.39(c) to determine the input resistance $R_{in} \equiv v_i/i_i$ and the voltage gain $A_v \equiv v_o/v_i$. Toward that end we simplify the circuit by combining the three parallel resistances r_o , R_D , and R_L in a single resistance R'_L ,

$$\begin{aligned} R'_L &= R_L \| R_D \| r_o \\ &= 10 \| 10 \| 47 = 4.52 \text{ k}\Omega \end{aligned}$$

as shown in Fig. 5.39(d). For the latter circuit we can write the two equations

$$v_o = (i_i - g_m v_{gs}) R'_L \quad (5.60)$$

Example 5.10 *continued*

and

$$i_i = \frac{v_{gs} - v_o}{R_G} \quad (5.61)$$

Substituting for i_i from Eq. (5.61) into Eq. (5.60) results in the following expression for the voltage gain $A_v \equiv v_o/v_i = v_o/v_{gs}$:

$$A_v = -g_m R'_L \frac{1 - (1/g_m R_G)}{1 + (R'_L/R_G)}$$

Since R_G is very large, $g_m R_G \gg 1$ and $R'_L/R_G \ll 1$ (the reader can easily verify this), and the gain expression can be approximated as

$$A_v \approx -g_m R'_L \quad (5.62)$$

Substituting, $g_m = 0.725 \text{ mA/V}$ and $R'_L = 4.52 \text{ k}\Omega$ yields

$$A_v = -3.3 \text{ V/V}$$

To obtain the input resistance, we substitute in Eq. (5.61) for $v_o = A_v v_{gs} = -g_m R'_L v_{gs}$, then use $R_{in} \equiv v_i/i_i = v_{gs}/i_i$ to obtain

$$R_{in} = \frac{R_G}{1 + g_m R'_L} \quad (5.63)$$

This is an interesting relationship: The input resistance decreases as the gain ($g_m R'_L$) is increased. The value of R_{in} can now be determined; it is

$$R_{in} = \frac{10 \text{ M}\Omega}{1 + 3.3} = 2.33 \text{ M}\Omega$$

which is still very large.

The largest allowable input signal \hat{v}_i is constrained by the need to keep the transistor in saturation at all times; that is,

$$v_{DS} \geq v_{GS} - V_t$$

Enforcing this condition with equality at the point v_{GS} is maximum and v_{DS} is minimum, we write

$$\begin{aligned} v_{DS\min} &= v_{GS\max} - V_t \\ V_{DS} - |A_v| \hat{v}_i &= V_{GS} + \hat{v}_i - V_t \end{aligned}$$

Since $V_{DS} = V_{GS}$, we obtain

$$\hat{v}_i = \frac{V_t}{|A_v| + 1}$$

This is a general relationship that applies to this circuit irrespective of the component values. Observe that it simply states that the maximum signal swing is determined by the fact that the bias arrangement makes $V_D = V_G$ and thus, to keep the MOSFET out of the triode region, the signal between D and G is constrained to be equal to V_t . For our particular design,

$$\hat{v}_i = \frac{1.5}{3.3 + 1} = 0.35 \text{ V}$$

A modification of this circuit that increases the allowable signal swing is investigated in Problem 5.80.

EXERCISE

D5.18 Consider the amplifier circuit of Fig. 5.39(a) without the load resistance R_L and with channel length modulation neglected. Let $V_{DD} = 5$ V, $V_t = 0.7$ V, and $k_n = 1$ mA/V². Find V_{OV} , I_D , R_D , and R_G to obtain a voltage gain of 25 V/V and an input resistance of 0.5 MΩ. What is the maximum allowable input signal, \hat{v}_i ?

Ans. 0.319 V; 50.7 μA; 78.5 kΩ; 13 MΩ; 27 mV

5.5.7 The T Equivalent-Circuit Model

Through a simple circuit transformation it is possible to develop an alternative equivalent-circuit model for the MOSFET. The development of such a model, known as the T model, is illustrated in Fig. 5.40. Figure 5.40(a) shows the equivalent circuit studied

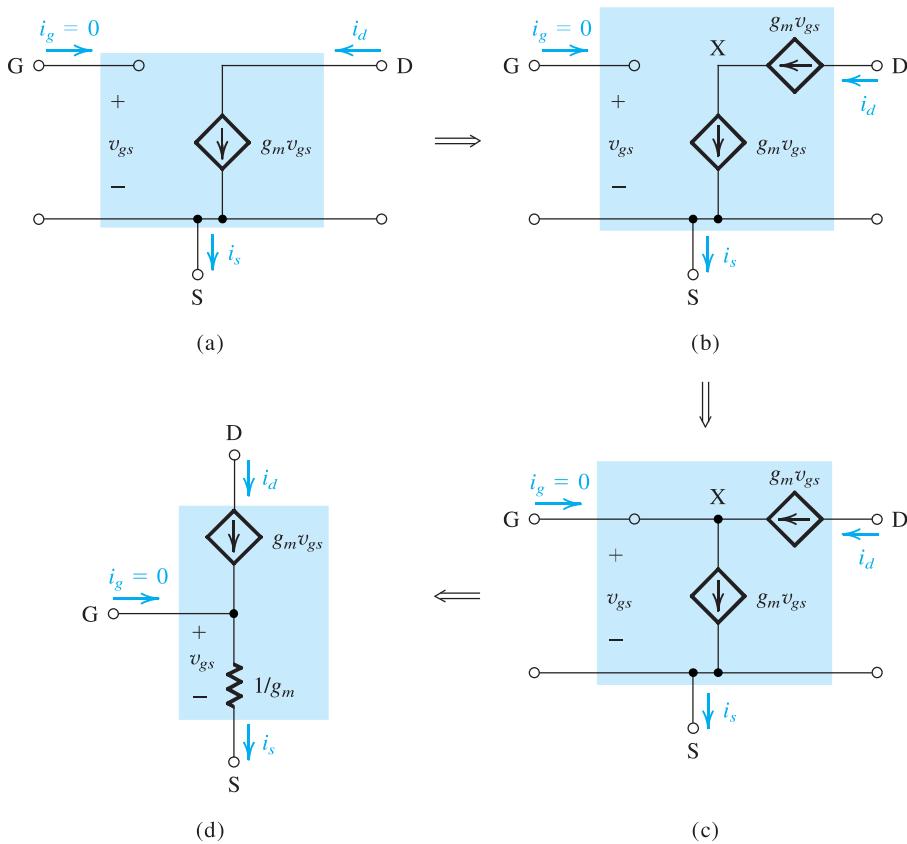


Figure 5.40 Development of the T equivalent-circuit model for the MOSFET. For simplicity, r_o has been omitted; however, it may be added between D and S in the T model of (d).

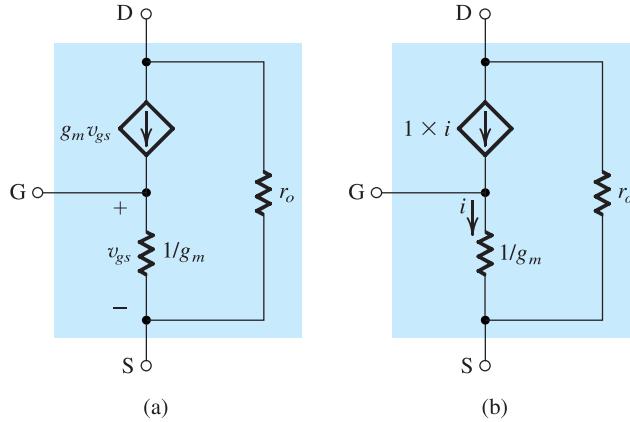


Figure 5.41 (a) The T model of the MOSFET augmented with the drain-to-source resistance r_o . (b) An alternative representation of the T model.

above without r_o . In Fig. 5.40(b) we have added a second $g_m v_{gs}$ current source in series with the original controlled source. This addition obviously does not change the terminal currents and is thus allowed. The newly created circuit node, labeled X, is joined to the gate terminal G in Fig. 5.40(c). Observe that the gate current does not change—that is, it remains equal to zero—and thus this connection does not alter the terminal characteristics. We now note that we have a controlled current source $g_m v_{gs}$ connected across its control voltage v_{gs} . We can replace this controlled source by a resistance as long as this resistance draws an equal current as the source. (See the source-absorption theorem in Appendix D.) Thus the value of the resistance is $v_{gs}/g_m v_{gs} = 1/g_m$. This replacement is shown in Fig. 5.40(d), which depicts the alternative model. Observe that i_g is still zero, $i_d = g_m v_{gs}$, and $i_s = v_{gs}/(1/g_m) = g_m v_{gs}$, all the same as in the original model in Fig. 5.40(a).

The model of Fig. 5.40(d) shows that the resistance between gate and source looking into the source is $1/g_m$. This observation and the T model prove useful in many applications. Note that the resistance between gate and source, looking into the gate, is infinite.

In developing the T model we did not include r_o . If desired, this can be done by incorporating in the circuit of Fig. 5.40(d) a resistance r_o between drain and source, as shown in Fig. 5.41(a). An alternative representation of the T model, in which the voltage-controlled current source is replaced with a current-controlled current source, is shown in Fig. 5.41(b).

Finally, we should note that in order to distinguish the model of Fig. 5.37(b) from the equivalent T model, the former is sometimes referred to as the **hybrid- π model**, a carryover from the bipolar transistor literature. The origin of this name will be explained in the next chapter.

Example 5.11

Figure 5.42(a) shows a MOSFET amplifier biased by a constant-current source I . Assume that the values of I and R_D are such that the MOSFET operates in the saturation region. The input signal v_i is coupled to

the source terminal by utilizing a large capacitor C_{C1} . Similarly, the output signal at the drain is taken through a large coupling capacitor C_{C2} . Find the input resistance R_{in} and the voltage gain v_o/v_i . Neglect channel-length modulation.

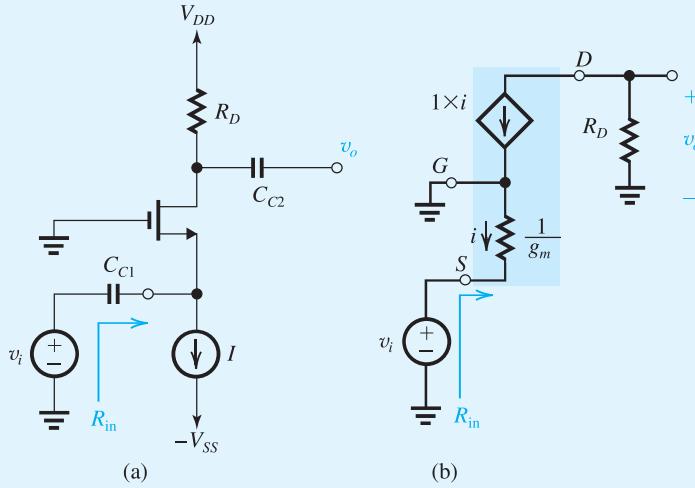


Figure 5.42 (a) Amplifier circuit for Example 5.11; (b) Small-signal equivalent circuit of the amplifier in (a).

Solution

Replacing the MOSFET with its T equivalent-circuit model results in the amplifier equivalent circuit shown in Fig. 5.42(b). Observe that the dc current source I is replaced with an open circuit and the dc voltage source V_{DD} is replaced by a short circuit. The large coupling capacitors have been replaced by short circuits. From the equivalent circuit-model we determine

$$R_{in} = \frac{v_i}{-i} = 1/g_m$$

and

$$v_o = -iR_D = \left(\frac{v_i}{1/g_m}\right)R_D = g_m R_D v_i$$

Thus,

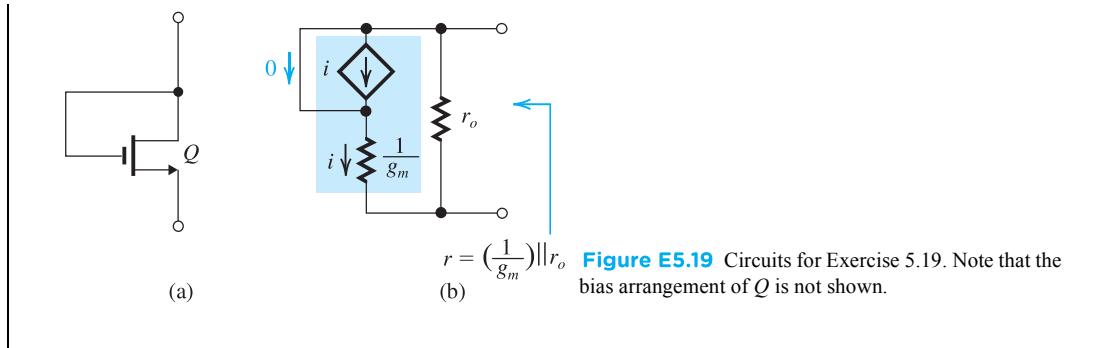
$$A_v \equiv \frac{v_o}{v_i} = g_m R_D$$

We note that this amplifier, known as the common-gate amplifier because the gate at ground potential is common to both the input and output ports, has a low input resistance ($1/g_m$) and a noninverting gain. We shall study this amplifier type in Section 5.6.5.

EXERCISE

- 5.19** Use the T model of Fig. 5.41(b) to show that a MOSFET whose drain is connected to its gate exhibits an incremental resistance equal to $[(1/g_m) \parallel r_o]$.

Ans. See Fig. E5.19.



5.5.8 Summary

We conclude this section by presenting in Table 5.3 a summary of the formulas for calculating the values of the small-signal MOSFET parameters. Observe that for g_m we have three different formulas, each providing the circuit designer with insight regarding design choices. We shall make frequent comments on these in later sections and chapters.

Table 5.3 Small-Signal Equivalent-Circuit Models for the MOSFET

Small-Signal Parameters

NMOS transistors

- Transconductance:

$$g_m = \mu_n C_{ox} \frac{W}{L} V_{OV} = \sqrt{2\mu_n C_{ox} \frac{W}{L} I_D} = \frac{2I_D}{V_{OV}}$$

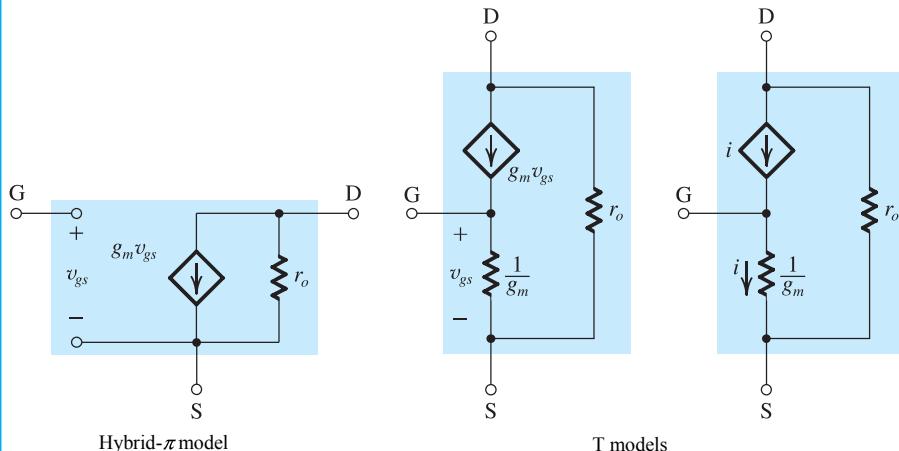
- Output resistance:

$$r_o = V_A / I_D = 1 / \lambda I_D$$

PMOS transistors

Same formulas as for NMOS except using $|V_{ov}|$, $|V_A|$, and replacing μ_n with μ_p .

Small-Signal Equivalent Circuit Models



EXERCISES

5.20 For the amplifier in Fig. 5.34, let $V_{DD} = 5$ V, $R_D = 10$ k Ω , $V_t = 1$ V, $k'_n = 20$ $\mu\text{A}/\text{V}^2$, $W/L = 20$, $V_{GS} = 2$ V, and $\lambda = 0$.

- (a) Find the dc current I_D and the dc voltage V_{DS} .
- (b) Find g_m .
- (c) Find the voltage gain.
- (d) If $v_{gs} = 0.2 \sin \omega t$ volts, find v_{ds} assuming that the small-signal approximation holds. What are the minimum and maximum values of v_{ds} ?
- (e) Use Eq. (5.43) to determine the various components of i_D . Using the identity $(\sin^2 \omega t = \frac{1}{2} - \frac{1}{2} \cos 2\omega t)$, show that there is a slight shift in I_D (by how much?) and that there is a second-harmonic component (i.e., a component with frequency 2ω). Express the amplitude of the second-harmonic component as a percentage of the amplitude of the fundamental. (This value is known as the second-harmonic distortion.)

Ans. (a) 200 μA , 3 V; (b) 0.4 mA/V; (c) -4 V/V; (d) $v_{ds} = -0.8 \sin \omega t$ volts, 2.2 V, 3.8 V; (e) $i_D = (204 + 80 \sin \omega t - 4 \cos 2\omega t) \mu\text{A}$, 5%

5.21 An NMOS transistor has $\mu_n C_{ox} = 60$ $\mu\text{A}/\text{V}^2$, $W/L = 40$, $V_t = 1$ V, and $V_A = 15$ V. Find g_m and r_o when (a) the bias voltage $V_{GS} = 1.5$ V, (b) the bias current $I_D = 0.5$ mA.

Ans. (a) 1.2 mA/V, 50 k Ω ; (b) 1.55 mA/V, 30 k Ω

5.22 A MOSFET is to operate at $I_D = 0.1$ mA and is to have $g_m = 1$ mA/V. If $k'_n = 50$ $\mu\text{A}/\text{V}^2$, find the required W/L ratio and the overdrive voltage.

Ans. 100; 0.2 V

5.23 For a fabrication process for which $\mu_p \approx 0.4\mu_n$, find the ratio of the width of a PMOS transistor to the width of an NMOS transistor so that the two devices have equal g_m for the same bias conditions. The two devices have equal channel lengths.

Ans. 2.5

5.24 A PMOS transistor has $V_t = -1$ V, $k'_p = 60$ $\mu\text{A}/\text{V}^2$, and $W/L = 16$ $\mu\text{m}/0.8 \mu\text{m}$. Find I_D and g_m when the device is biased at $V_{GS} = -1.6$ V. Also, find the value of r_o if λ (at $L = 1 \mu\text{m}$) = -0.04 V^{-1} .

Ans. 216 μA ; 0.72 mA/V; 92.6 k Ω

5.25 Use the formulas in Table 5.3 to derive an expression for $(g_m r_o)$ in terms of V_A and V_{OV} . As we shall see in Chapter 7, this is an important transistor parameter and is known as the intrinsic gain. Evaluate the value of $g_m r_o$ for an NMOS transistor fabricated in a 0.8- μm CMOS process for which $V'_A = 12.5$ V/ μm of channel length. Let the device have minimum channel length and be operated at an overdrive voltage of 0.2 V.

Ans. $g_m r_o = 2V_A/V_{OV}$; 100 V/V

5.6 Basic MOSFET Amplifier Configurations

It is useful at this point to take stock of where we are and where we are going in our study of MOSFET amplifiers. In Section 5.4 we examined the essence of the use of the MOSFET as an amplifier. There we found that almost-linear amplification can be obtained by biasing the MOSFET at an appropriate point in its saturation region of operation and by keeping the signal v_{gs} small. We then took a closer look at the small-signal operation of the MOSFET in Section 5.5 and developed circuit models to represent the transistor, thus facilitating the determination of amplifier parameters such as voltage gain and input and output resistances.

We are now ready to consider the various possible configurations of MOSFET amplifiers, and we will do that in the present section. To focus our attention on the salient features of the various configurations, we shall present them in their most simple, or “stripped down” version. Thus, we will not show the dc biasing arrangements, leaving the study of bias design to the next section. Finally, in Section 5.8 we will bring everything together and present practical circuits for discrete-circuit MOSFET amplifiers; namely, those amplifier circuits that can be constructed using discrete components. The study of integrated-circuit amplifiers begins in Chapter 7.

5.6.1 The Three Basic Configurations

There are three basic configurations for connecting the MOSFET as an amplifier. Each of these configurations is obtained by connecting one of the three MOSFET terminals to ground, thus creating a two-port network with the grounded terminal being *common* to the input and output ports. Figure 5.43 shows the resulting three configurations with the biasing arrangements omitted.

In the circuit of Fig. 5.43(a) the source terminal is connected to ground, the input voltage signal v_i is applied between the gate and ground, and the output voltage signal v_o is taken between the drain and ground, across the resistance R_D . This configuration, therefore, is called the **grounded-source or common-source (CS) amplifier**. It is by far the most popular MOS amplifier configuration and is the one we utilized in Sections 5.4 and 5.5 to study MOS amplifier operation.

The **common-gate (CG)** or grounded-gate amplifier is shown in Fig. 5.43(b). It is obtained by connecting the gate to ground, applying the input v_i between the source and

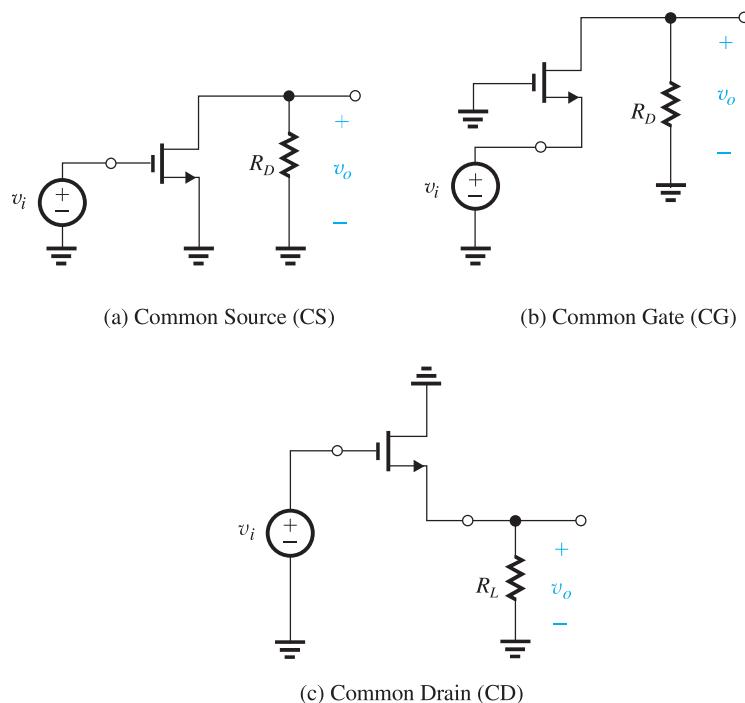


Figure 5.43 The three basic MOSFET amplifier configurations.

ground, and taking the output v_o across the resistance R_D connected between the drain and ground. We encountered a CG amplifier in Example 5.11.

Finally, Fig. 5.43(c) shows the **common-drain (CD)** or grounded-drain amplifier. It is obtained by connecting the drain terminal to ground, applying the input voltage signal v_i between gate and ground, and taking the output voltage signal between the source and ground, across a load resistance R_L . For reasons that will become apparent shortly, this configuration is more commonly called the **source follower**.

Our study of the three basic MOS amplifier configurations will reveal that each has distinctly different attributes and hence areas of application.

5.6.2 Characterizing Amplifiers

Before we begin our study of the different MOSFET amplifier configurations, we consider how to characterize the performance of an amplifier as a circuit building block. An introduction to this topic was presented in Section 1.5.

Figure 5.44(a) shows an amplifier fed with a signal source having an open-circuit voltage v_{sig} and an internal resistance R_{sig} . These can be the parameters of an actual signal source or, in a cascade amplifier, the Thévenin equivalent of the output circuit of another amplifier stage preceding the one under study. The amplifier is shown with a load resistance R_L

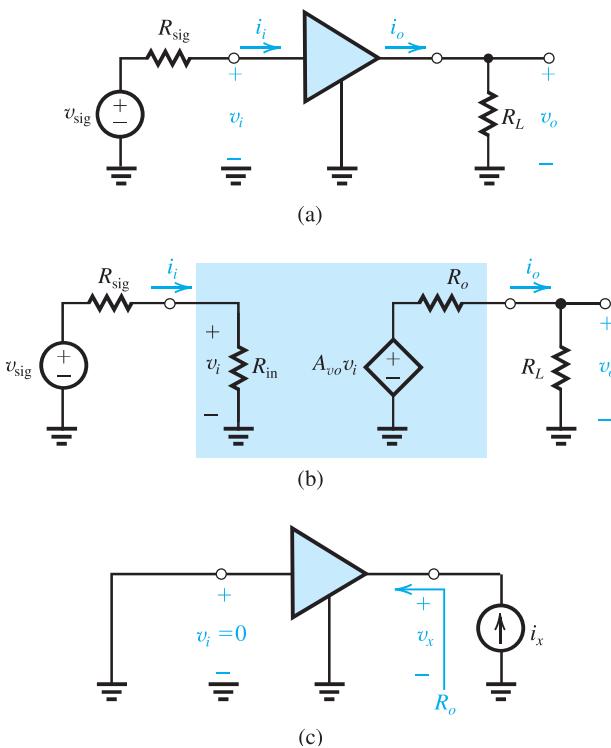


Figure 5.44 Characterization of the amplifier as a functional block: (a) An amplifier fed with a voltage signal v_{sig} having a source resistance R_{sig} and feeding a load resistance R_L ; (b) Equivalent-circuit representation of the circuit in (a); (c) Determining the amplifier output resistance R_o .

connected to the output terminal. Here, R_L can be an actual load resistance or the input resistance of a succeeding amplifier stage in a cascade amplifier.

Figure 5.44(b) shows the amplifier circuit with the amplifier block replaced by its equivalent-circuit model. The input resistance R_{in} represents the loading effect of the amplifier input on the signal source. It is found from

$$R_{\text{in}} \equiv \frac{v_i}{i_i}$$

and together with the resistance R_{sig} forms a voltage divider that reduces v_{sig} to the value v_i that appears at the amplifier input,

$$v_i = \frac{R_{\text{in}}}{R_{\text{in}} + R_{\text{sig}}} v_{\text{sig}} \quad (5.65)$$

All the amplifier circuits studied in this section are **unilateral**. That is, they do not contain internal feedback, and thus R_{in} will be independent of R_L . However, as will be seen in subsequent chapters, this is not always the case.

The second parameter in characterizing amplifier performance is the **open-circuit voltage gain** A_{vo} , defined as

$$A_{vo} \equiv \left. \frac{v_o}{v_i} \right|_{R_L=\infty}$$

The third and final parameter is the output resistance R_o . Observe from Fig. 5.44(b) that R_o is the resistance seen looking back into the amplifier output terminal with v_i set to zero. Thus R_o can be determined, at least conceptually, as indicated in Fig. 5.44(c) with

$$R_o = \frac{v_x}{i_x}$$

The controlled source $A_{vo}v_i$ and the output resistance R_o represent the Thévenin equivalent of the amplifier output circuit, and the output voltage v_o can be found from

$$v_o = \frac{R_L}{R_L + R_o} A_{vo} v_i \quad (5.66)$$

Thus the voltage gain of the amplifier proper, A_v , can be found as

$$A_v \equiv \frac{v_o}{v_i} = A_{vo} \frac{R_L}{R_L + R_o} \quad (5.67)$$

and the overall voltage gain G_v ,

$$G_v \equiv \frac{v_o}{v_{\text{sig}}}$$

can be determined by combining Eqs. (5.65) and (5.67):

$$G_v = \frac{R_{\text{in}}}{R_{\text{in}} + R_{\text{sig}}} A_{vo} \frac{R_L}{R_L + R_o} \quad (5.68)$$

5.6.3 The Common-Source (CS) Amplifier

Of the three basic MOS amplifier configurations, the common source is the most widely used. Typically, in an amplifier formed by cascading a number of stages, the bulk of the voltage gain is obtained by using one or more common-source stages in the cascade.

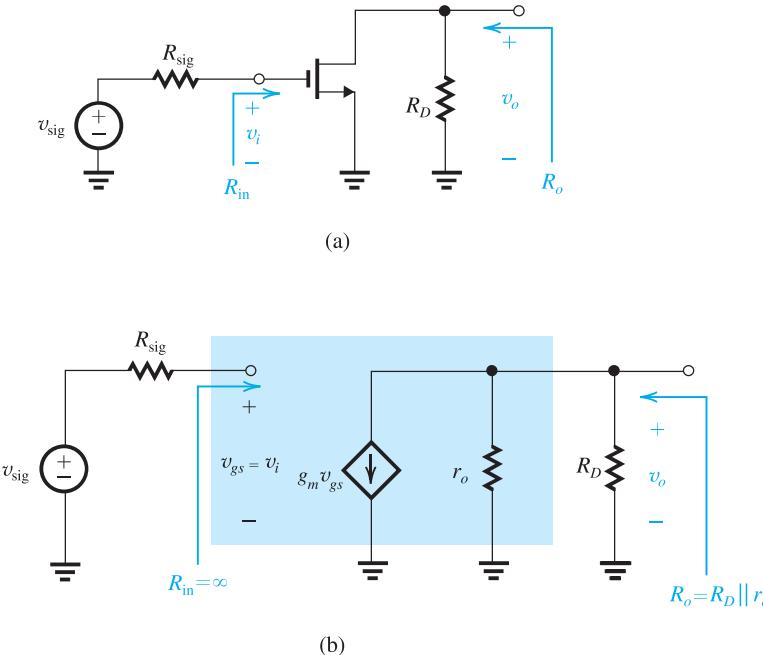


Figure 5.45 (a) Common-source amplifier fed with a signal v_{sig} from a generator with a resistance R_{sig} . The bias circuit is omitted. (b) The common-source amplifier with the MOSFET replaced with its hybrid- π model.

Figure 5.45(a) shows a common-source amplifier (with the biasing arrangement omitted) fed with a signal source v_{sig} having a source resistance R_{sig} . We wish to analyze this circuit to determine R_{in} , A_{vo} , R_o , and G_v . For this purpose we shall assume that R_D is part of the amplifier; thus if a load resistance R_L is connected to the amplifier output, it appears in parallel with R_D .

Characteristic Parameters of the CS Amplifier Replacing the MOSFET with its hybrid- π model, we obtain the CS amplifier equivalent circuit shown in Fig 5.45(b). We shall use this equivalent circuit to determine the characteristic parameters R_{in} , A_{vo} , and R_o as follows.

The input resistance R_{in} is obviously infinite,

$$R_{\text{in}} = \infty \quad (5.69)$$

The output voltage v_o is found by multiplying the current ($g_m v_{gs}$) by the total resistance between the output node and ground,

$$v_o = -(g_m v_{gs})(R_D \parallel r_o)$$

Since $v_{gs} = v_i$, the open-circuit voltage gain $A_{vo} \equiv v_o/v_i$ can be obtained as

$$A_{vo} = -g_m(R_D \parallel r_o) \quad (5.70)$$

Observe that the transistor output resistance r_o reduces the magnitude of the voltage gain. In discrete-circuit amplifiers, which are of interest to us in this chapter, R_D is usually much

lower than r_o and the effect of r_o on reducing $|A_{vo}|$ is slight (less than 10% or so). Thus in many cases we can neglect r_o and express A_{vo} simply as

$$A_{vo} \approx (-g_m R_D) \quad (5.71)$$

The reader is cautioned, however, that neglecting r_o is allowed only in discrete-circuit design. As will be seen in Chapter 7, r_o plays a central role in IC amplifiers.

The output resistance R_o is the resistance seen looking back into the output terminal with v_i set to zero. From Fig. 5.45(b) we see that with v_i set to zero, v_{gs} will be zero, and thus $g_m v_{gs}$ will be zero, resulting in

$$R_o = R_D \parallel r_o \quad (5.72)$$

Here, r_o has the beneficial effect of reducing the value of R_o . In discrete circuits, however, this effect is slight and we can make the approximation

$$R_o \approx R_D \quad (5.73)$$

This concludes the analysis of the CS amplifier proper. We can now make the following observations.

1. The input resistance is ideally infinite.
2. The output resistance is moderate to high (in the kilohms to tens of kilohms range). Reducing R_D to lower R_o is not a viable proposition, since the voltage gain is also reduced. Alternatively, if a low output resistance (in the ohms to tens of ohms range) is needed, a source follower stage is called for, as will be discussed in Section 5.6.6.
3. The open-circuit voltage gain A_{vo} can be high, making the CS configuration the workhorse in MOS amplifier design. Unfortunately, however, the bandwidth of the CS amplifier is severely limited. We shall study amplifier frequency response in Chapter 9.

Overall Voltage Gain To determine the overall voltage gain G_v , we first note that the infinite input resistance will make the entire signal v_{sig} appear at the amplifier input,

$$v_i = v_{sig} \quad (5.74)$$

an obviously ideal situation. At this point we should remind the reader that to maintain a reasonably linear operation, v_i and hence v_{sig} should be kept much smaller than $2V_{OV}$.

If a load resistance R_L is connected to the output terminal of the amplifier, this resistance will appear in parallel with R_D . It follows that the voltage gain A_v can be obtained by simply replacing R_D in the expression for A_{vo} in Eq. (5.70) by $R_D \parallel R_L$,

$$A_v = -g_m (R_D \parallel R_L \parallel r_o) \quad (5.75)$$

This expression together with the fact that $v_i = v_{sig}$, provides the overall voltage gain,

$$G_v = A_v = -g_m (R_D \parallel R_L \parallel r_o) \quad (5.76)$$

EXERCISE

- 5.26** Use A_{vo} in Eq. (5.70) together with R_o in Eq. (5.72) to obtain A_v . Show that the result is identical to that in Eq. (5.75).

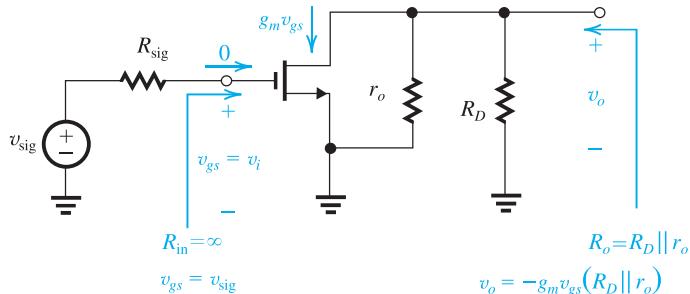


Figure 5.46 Performing the analysis directly on the circuit diagram with the MOSFET model used implicitly.

Performing the Analysis Directly on the Circuit Diagram Although small-signal, equivalent-circuit models provide a systematic process for the analysis of any amplifier circuit, the effort involved in drawing the equivalent circuit is sometimes not justified. That is, in simple situations and after a lot of practice, one can perform the small-signal analysis directly on the circuit schematic. Because in this way one remains closer to the actual circuit, the direct analysis can yield greater insight into circuit operation. Figure 5.46 shows the direct analysis of the CS amplifier. Observe that we have “pulled out” the resistance r_o from the transistor, thus making the transistor drain conduct $g_m v_{gs}$ while still accounting for the effect of r_o .

EXERCISE

- 5.27** A CS amplifier utilizes a MOSFET biased at $I_D = 0.25$ mA with $V_{OV} = 0.25$ V and $R_D = 20$ k Ω . The device has $V_A = 50$ V. The amplifier is fed with a source having $R_{sig} = 100$ k Ω , and a 20-k Ω load is connected to the output. Find R_{in} , A_{vo} , R_o , A_{vo} and G_v . If to maintain reasonable linearity, the peak of the input sine-wave signal is limited to 10% of $(2V_{OV})$ what is the peak of the sine-wave voltage at the output?

Ans. ∞ ; -36.4 V/V; 18.2 k Ω ; -19 V/V; -19 V/V; 0.95 V

5.6.4 The Common-Source Amplifier with a Source Resistance

It is often beneficial to insert a resistance R_s in the source lead of the common-source amplifier as shown in Fig. 5.47(a). The corresponding small-signal equivalent circuit is shown in Fig. 5.47(b), where we note that the MOSFET has been replaced with its T equivalent-circuit model. The T model is used in preference to the π model because it makes the analysis in this case somewhat simpler. In general, *whenever a resistance is connected in the source lead, the T model is preferred*. The source resistance then simply appears in series with the resistance $1/g_m$ and can be added to it.

It should be noted that we have not included r_o in the equivalent-circuit model. Including r_o would complicate the analysis considerably; r_o would connect the output node of the amplifier to the input side and thus would make the amplifier *nonunilateral*.

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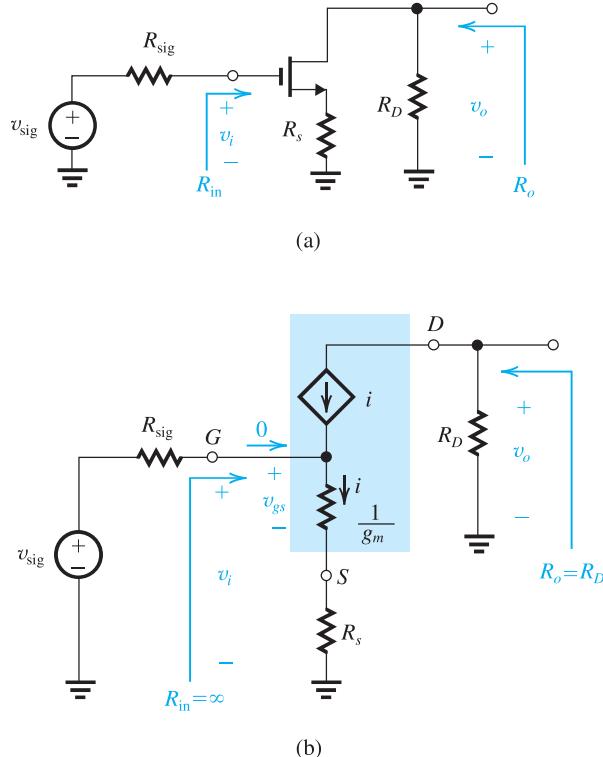


Figure 5.47 The CS amplifier with a source resistance R_s : (a) Circuit without bias details; (b) Equivalent circuit with the MOSFET represented by its T model.

Fortunately, it turns out that the effect of r_o on the operation of the discrete-circuit amplifier is not important. This can be verified by computer simulation, using for instance SPICE. This is not the case, however, for the integrated-circuit version of the circuit, where r_o plays a major role and must be taken into account, as we shall do in Chapter 7.

From Fig. 5.47(b) we see that the input resistance R_{in} is infinite and thus $v_i = v_{sig}$. Unlike the CS amplifier, however, here only a fraction of v_i appears between gate and source as v_{gs} . It can be determined from the voltage divider composed of $1/g_m$ and R_s that appears across the amplifier input, as follows:

$$v_{gs} = v_i \frac{1/g_m}{1/g_m + R_s} = \frac{v_i}{1 + g_m R_s} \quad (5.77)$$

Thus we can use the value of R_s to control the magnitude of the signal v_{gs} and thereby ensure that v_{gs} does not become too large and cause unacceptably high nonlinear distortion. This is the first benefit of including resistor R_s . Other benefits will be encountered in later sections and chapters. For instance, it will be shown in Chapter 9 that R_s causes the useful bandwidth of the amplifier to be extended. The mechanism by which R_s causes such improvements in amplifier performance is negative feedback. To see how R_s introduces

negative feedback, refer to Fig. 5.47(a): If while keeping v_i constant, for some reason the drain current increases, the source current also will increase, resulting in an increased voltage drop across R_s . Thus the source voltage rises, and the gate-to-source voltage decreases. The latter effect causes the drain current to decrease, counteracting the initially assumed change, an indication of the presence of negative feedback. In Chapter 10 we shall study negative feedback formally. There we will learn that the improvements that negative feedback provides are obtained at the expense of a reduction in gain. We will now show this to be the case in the circuit of Fig. 5.47.

The output voltage v_o is obtained by multiplying the controlled-source current i by R_D ,

$$v_o = -i R_D$$

The current i in the source lead can be found by dividing v_i by the total resistance in the source,

$$i = \frac{v_i}{1/g_m + R_s} = \left(\frac{g_m}{1 + g_m R_s} \right) v_i \quad (5.78)$$

Thus, the voltage gain A_{vo} can be found as

$$A_{vo} = \frac{v_o}{v_i} = -\frac{R_D}{1/g_m + R_s} \quad (5.79) \quad \text{I}$$

which can also be expressed as

$$A_{vo} = -\frac{g_m R_D}{1 + g_m R_s} \quad (5.80) \quad \text{I}$$

Equation (5.80) indicates that including the resistance R_s reduces the voltage gain by the factor $(1 + g_m R_s)$. This is the price paid for the improvements that accrue as a result of R_s . It is interesting to note that in Chapter 10, we will find that the factor $(1 + g_m R_s)$ is the “amount of negative feedback” introduced by R_s . It is also the same factor by which bandwidth and other performance parameters improve. Because of the negative-feedback action of R_s , it is known as a **source-degeneration resistance**.

There is another useful interpretation of the expression for the drain current in Eq. (5.78): The quantity between brackets on the right-hand side can be thought of as the “effective transconductance with R_s included.” Thus, including R_s reduces the transconductance by the factor $(1 + g_m R_s)$. This, of course, is simply the result of the fact that only a fraction $1/(1 + g_m R_s)$ of v_i appears as v_{gs} (see Eq. 5.77.).

The alternative gain expression in Eq. (5.79) has a powerful and insightful interpretation: The voltage gain between gate and drain is equal to the ratio of the total resistance in the drain (R_D) to the total resistance in the source ($1/g_m + R_s$),

$$\text{Voltage gain from gate to drain} = \frac{\text{Total resistance in drain}}{\text{Total resistance in source}} \quad (5.81) \quad \text{I}$$

This is a general expression. For instance, setting $R_s = 0$ in Eq. (5.79) yields A_{vo} of the CS amplifier.

Finally, we consider the situation of a load resistance R_L connected at the output. We can obtain the gain A_v using the open-circuit voltage gain A_{vo} together with the output resistance R_o , which can be found by inspection to be

$$R_o = R_D$$

Alternatively, A_v can be obtained by simply replacing R_D in Eq. (5.79) or (5.80) by $(R_D \parallel R_L)$; thus,

$$\textcircled{1} \quad A_v = -\frac{R_D \parallel R_L}{1/g_m + R_s} \quad (5.82)$$

or

$$\textcircled{1} \quad A_v = \frac{g_m(R_D \parallel R_L)}{1 + g_m R_s} \quad (5.83)$$

Observe that Eq. (5.82) is a direct application of the ratio of total resistance rule of Eq. (5.81). Finally, note that because R_{in} is infinite, $v_i = v_{sig}$ and the overall voltage gain G_v is equal to A_v .

EXERCISE

- 5.28** In Exercise 5.27 we applied an input signal v_{sig} of 50 mV peak and obtained an output signal of approximately 1 V peak. Assume that for some reason we now have an input signal v_{sig} that is 0.2 V peak and that we wish to modify the circuit to keep v_{gs} unchanged, and thus keep the nonlinear distortion from increasing. What value should we use for R_s ? What value of G_v will result? What will the peak signal at the output become? Assume $r_o = \infty$.

Ans. 1.5 kΩ; -5 V/V; 1 V

5.6.5 The Common-Gate (CG) Amplifier

Figure 5.48(a) shows a common-gate amplifier with the biasing circuit omitted. The amplifier is fed with a signal source characterized by v_{sig} and R_{sig} . Since R_{sig} appears in series with the source, it is more convenient to represent the transistor with the T model than with the π model. Doing this, we obtain the amplifier equivalent circuit shown in Fig. 5.48(b). Note that we have not included r_o : This would have complicated the analysis considerably, for r_o would have appeared between the output and the input side of the amplifier. Fortunately, it

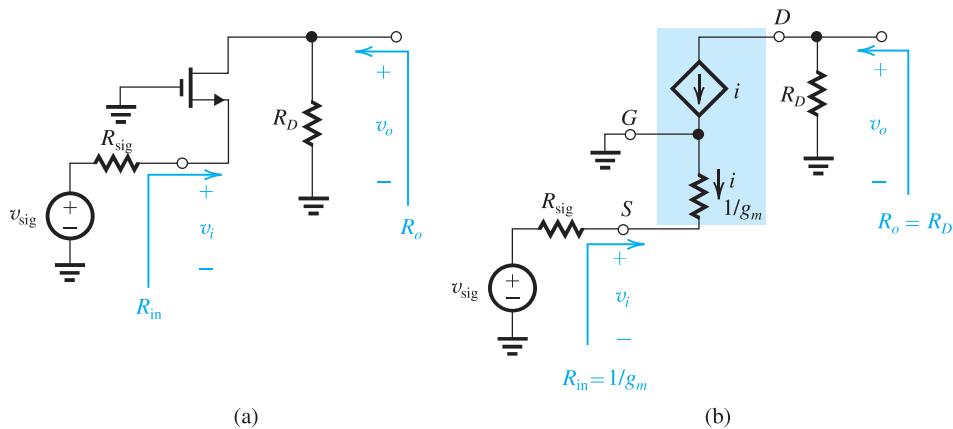


Figure 5.48 (a) Common-gate (CG) amplifier with bias arrangement omitted. (b) Equivalent circuit of the CG amplifier with the MOSFET replaced with its T model.

turns out that the effect of r_o on the performance of a discrete CG amplifier is very small. We will consider the effect of r_o when we study the IC form of the CG amplifier in Chapter 7.

From inspection of the equivalent circuit of Fig. 5.48(b), we see that the input resistance

$$R_{in} = \frac{1}{g_m} \quad (5.84) \quad \text{I}$$

This should have been expected, since we are looking into the source and the gate is grounded. Typically $1/g_m$ is a few hundred ohms; thus the CG amplifier has a low input resistance.

To determine the voltage gain A_{vo} , we write at the drain node

$$v_o = -iR_D$$

and substitute for the source current i from

$$i = -\frac{v_i}{1/g_m}$$

to obtain

$$A_{vo} \equiv \frac{v_o}{v_i} = g_m R_D \quad (5.85) \quad \text{I}$$

which except for the positive sign is identical to the expression for A_{vo} of the CS amplifier (when r_o is neglected).

The output resistance of the CG circuit can be found by inspection of the circuit in Fig. 5.48(b) as

$$R_o = R_D \quad (5.86)$$

which is the same as in the case of the CS amplifier (with r_o neglected).

Although the gain of the CG amplifier proper has the same magnitude as that of the CS amplifier, this is usually not the case as far as the overall voltage gain is concerned. The low input resistance of the CG amplifier can cause the input signal to be severely attenuated. Specifically,

$$\frac{v_i}{v_{sig}} = \frac{R_{in}}{R_{in} + R_{sig}} = \frac{1/g_m}{1/g_m + R_{sig}} \quad (5.87)$$

from which we see that except for situations in which R_{sig} is on the order of $1/g_m$, the signal transmission factor v_i/v_{sig} can be very small and the overall voltage gain G_v can be correspondingly small. Specifically, with a resistance R_L connected at the output

$$G_v = \frac{1/g_m}{R_{sig} + 1/g_m} [g_m(R_D \parallel R_L)]$$

Thus,

$$G_v = \frac{(R_D \parallel R_L)}{R_{sig} + 1/g_m} \quad (5.88) \quad \text{I}$$

Observe that *the overall voltage gain is simply the ratio of the total resistance in the drain circuit to the total resistance in the source circuit*. If R_{sig} is of the same order as R_D and R_L , G_v will be very small.

Because of its low input resistance, the CG amplifier alone has very limited application. One such application is to amplify high-frequency signals that come from sources with relatively low resistances. These include cables, where it is usually necessary for the input

resistance of the amplifier to match the characteristic resistance of the cable. As will be shown in Chapter 9, the CG amplifier has excellent high-frequency response. Thus it can be combined with the CS amplifier in a very beneficial way that takes advantage of the best features of each of the two configurations. A very significant circuit of this kind will be studied in Chapter 7.

EXERCISE

- 5.29** A CG amplifier is required to match a signal source with $R_{\text{sig}} = 100 \Omega$. At what current I_D should the MOSFET be biased if it is operated at an overdrive voltage of 0.20 V? If the total resistance in the drain circuit is 2 k Ω , what overall voltage gain is realized?

Ans. 1 mA; 10 V/V

5.6.6 The Common-Drain Amplifier or Source Follower

The last of the basic MOSFET amplifier configurations is the common-drain amplifier, an important circuit that finds application in the design of both small-signal amplifiers as well as amplifiers that are required to handle large signals and deliver substantial amounts of signal power to a load. This latter variety will be studied in Chapter 11. The common drain amplifier is more commonly known as the *source follower*. The reason behind this name will become apparent shortly.

The Need for Voltage Buffers Before embarking on the analysis of the source follower, it is useful to look at one of its more common applications. Consider the situation depicted in Fig. 5.49(a). A signal source delivering a signal of reasonable strength (1 V)

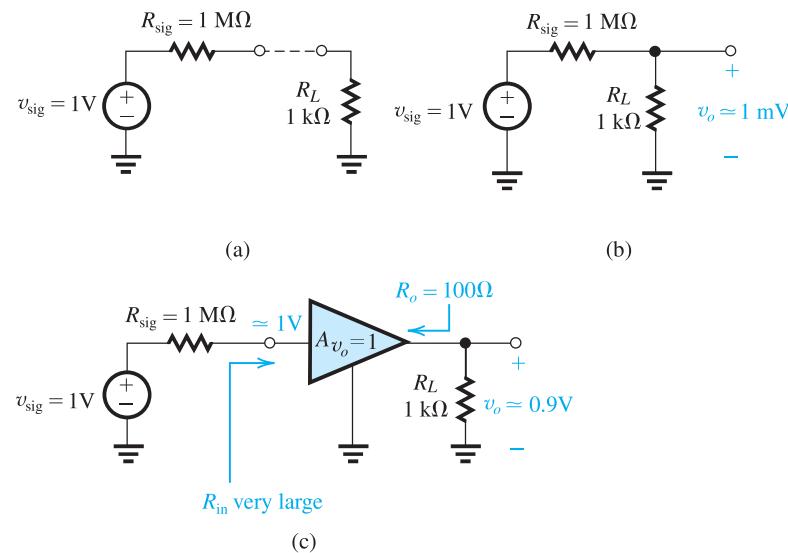


Figure 5.49 Illustrating the need for a unity-gain buffer amplifier.

with an internal resistance of $1 \text{ M}\Omega$ is to be connected to a $1\text{-k}\Omega$ load resistance. Connecting the source to the load directly as in Fig. 5.49(b) would result in severe attenuation of the signal; the signal appearing across the load will be only $1/(1000 + 1)$ of the input signal or about 1 mV . An alternative course of action is suggested in Fig. 5.49(c). Here we have interposed an amplifier between the source and the load. Our amplifier, however, is unlike the amplifiers we have been studying in this chapter thus far; it has a voltage gain of only unity. This is because our signal is already of sufficient strength and we do not need to increase its amplitude. Note, however, that our amplifier has a very large input resistance, thus almost all of v_{sig} (i.e., 1 V) will appear at the input of the amplifier proper. Since the amplifier has a low output resistance (100Ω), 90% of this signal (0.9 V) will appear at the output, obviously a very significant improvement over the situation without the amplifier. As will be seen shortly, the source follower can easily implement the unity-gain buffer amplifier shown in Fig. 5.49(c).

Characteristic Parameters of the Source Follower Figure 5.50(a) shows a source follower with the bias circuit omitted. The source follower is fed with a signal generator ($v_{\text{sig}}, R_{\text{sig}}$) and has a load resistance R_L connected between the source terminal and ground. We shall assume that R_L includes both the actual load and any other resistance that may be present between the source terminal and ground (e.g., for biasing purposes). Normally, the actual load resistance would be much lower in value than such other resistances and thus would dominate.

Since the MOSFET has a resistance R_o connected in its source terminal, it is most convenient to use the T model, as shown in Fig. 5.50(b). Note that we have included r_o , simply because it is very easy to do so. However, since r_o in effect appears in parallel with R_L , and since in discrete circuits $r_o \gg R_L$, we can neglect r_o and obtain the simplified equivalent circuit shown in Fig. 5.50(c). From the latter circuit we can write by inspection

$$R_{\text{in}} = \infty$$

and obtain A_v from the voltage divider formed by $1/g_m$ and R_L as

$$A_v \equiv \frac{v_o}{v_i} = \frac{R_L}{R_L + 1/g_m} \quad (5.89)$$

Setting $R_L = \infty$ we obtain

$$A_{vo} = 1 \quad (5.90)$$

The output resistance R_o is found by setting $v_i = 0$ (i.e., by grounding the gate). Now looking back into the output terminal, excluding R_L , we simply see $1/g_m$, thus

$$R_o = 1/g_m \quad (5.91)$$

The unity open-circuit voltage gain together with R_o in Eq. (5.91) can be used to find A_v when a load resistance R_L is connected. The result is simply the expression in Eq. (5.89). Finally, because of the infinite R_{in} , $v_i = v_{\text{sig}}$, and the overall voltage gain is

$$G_v = A_v = \frac{R_L}{R_L + 1/g_m} \quad (5.92)$$

Thus G_v will be lower than unity. However, because $1/g_m$ is usually low, the voltage gain can be close to unity. The unity open-circuit voltage gain in Eq. (5.90) indicates that the

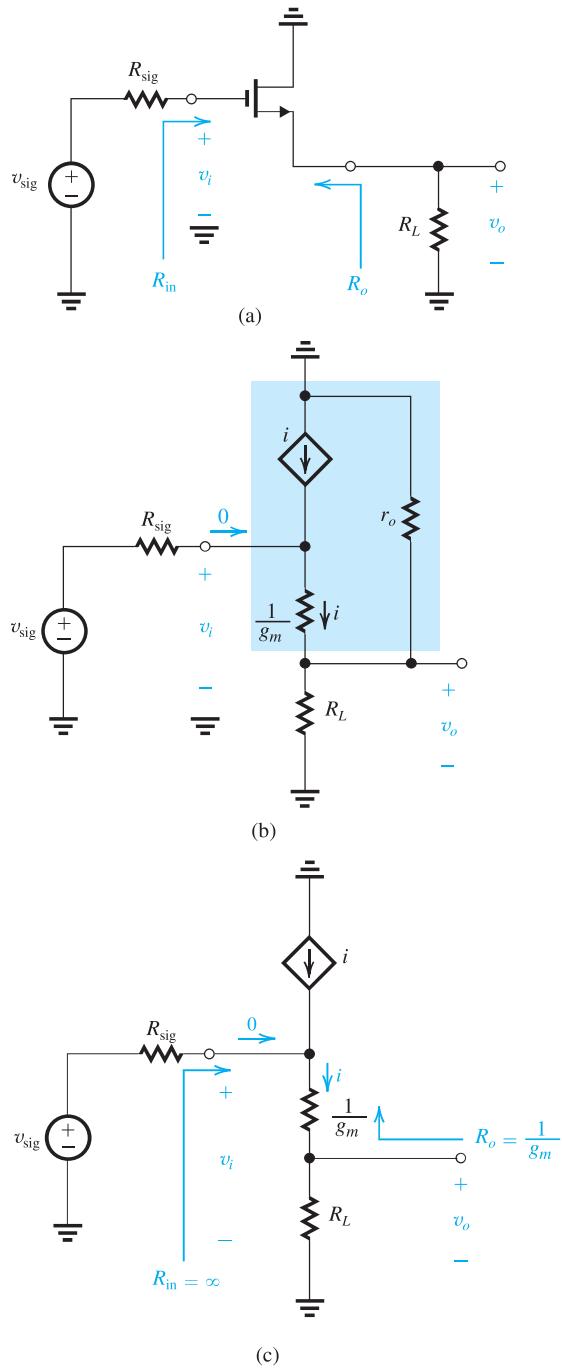


Figure 5.50 (a) Common-drain amplifier or source follower. (b) Equivalent circuit of the source follower obtained by replacing the MOSFET with its T model. Note that r_o appears in parallel with R_L and in discrete circuits, $r_o \gg R_L$. Neglecting r_o , we obtain the simplified equivalent circuit in (c).

voltage at the source terminal will follow that at the input, hence the name *source follower*.

In conclusion, the source follower features a very high input resistance (ideally, infinite), a relatively low output resistance, and an open-circuit voltage gain that is near unity (ideally, unity). Thus the source follower is ideally suited for implementing the unity-gain voltage buffer of Fig. 5.49(c). The source follower is also used as the output (i.e., last) stage in a multistage amplifier, where its function is to equip the overall amplifier with a low output resistance, thus enabling it to supply relatively large load currents without loss of gain (i.e., with little reduction of output signal level). The design of output stages is studied in Chapter 11.

EXERCISES

D5.30 It is required to design a source follower that implements the buffer amplifier shown in Fig. 5.49(c). If the MOSFET is operated with an overdrive voltage $V_{OV} = 0.25$ V, at what drain current should it be biased? Find the output signal amplitude and the signal amplitude between gate and source.

Ans. 1.25 mA; 0.91 V; 91 mV

D5.31 A MOSFET is connected in the source-follower configuration and employed as the output stage of a cascade amplifier. It is required to provide an output resistance of 200Ω . If the MOSFET has $k'_n = 0.4 \text{ mA/V}^2$ and is operated at $V_{OV} = 0.25$ V, find the required W/L ratio. Also specify the dc bias current I_D . If the amplifier load resistance varies over the range $1 \text{ k}\Omega$ to $10 \text{ k}\Omega$, what is the range of G_v of the source follower?

Ans. 50; 0.625 mA; 0.83 V/V to 0.98 V/V

5.32 Refer to Fig. 5.50(b). Show that taking r_o into account results in

$$A_{vo} = \frac{r_o}{r_o + 1/g_m}$$

Now, recalling that $r_o = V_A/I_D$ and $g_m = 2I_D/V_{OV}$, find A_{vo} in terms of V_A and V_{OV} . For a technology for which $V_A = 20$ V, what is the maximum V_{OV} at which the transistor can be operated while obtaining $A_{vo} \geq 0.99$ V/V?

Ans. $A_{vo} = 1/[1 + V_{OV}/2V_A]$; 0.4 V

5.6.7 Summary and Comparisons

For easy reference and to enable comparisons, we present in Table 5.4 the formulas for determining the characteristic parameters of discrete MOS amplifiers. Note that r_o has been neglected throughout. This is because our interest in this chapter is primarily in discrete-circuit amplifiers. As already mentioned, r_o has a relatively small effect on the performance of discrete-circuit amplifiers and can usually be neglected. In some cases, however, it is very easy to take r_o into account, such as in the case of the CS and CD amplifiers, and one is encouraged to do so. For integrated-circuit amplifiers, r_o must always be taken into account.

Table 5.4 Characteristics of MOSFET Amplifiers

Amplifier type	Characteristics ^{a, b}				
	R_{in}	A_{vo}	R_o	A_v	G_v
Common source (Fig. 5.45)	∞	$-g_m R_D$	R_D	$-g_m (R_D \parallel R_L)$	$-g_m (R_D \parallel R_L)$
Common source with R_s (Fig. 5.47)	∞	$\frac{g_m R_D}{1 + g_m R_s}$	R_D	$\frac{-g_m (R_D \parallel R_L)}{1 + g_m R_s}$	$-\frac{g_m (R_D \parallel R_L)}{1 + g_m R_s}$
Common gate (Fig. 5.48)	$\frac{1}{g_m}$	$g_m R_D$	R_D	$g_m (R_D \parallel R_L)$	$\frac{R_D \parallel R_L}{R_{sig} + 1/g_m}$
Source follower (Fig. 5.50)	∞	1	$\frac{1}{g_m}$	$\frac{R_L}{R_L + 1/g_m}$	$\frac{R_L}{R_L + 1/g_m}$

^a For the interpretation of R_{in} , A_{vo} , and R_o , refer to Fig. 5.44(b).

^b The MOSFET output resistance r_o has been neglected, as is permitted in the discrete-circuit amplifiers studied in this chapter. For IC amplifiers, r_o must always be taken into account.

In addition to the remarks already made throughout this section about the characteristics and areas of applicability of the various configurations, we make the following concluding points:

1. The CS configuration is the best suited for realizing the bulk of the gain required in an amplifier. Depending on the magnitude of the gain required, either a single stage or a cascade of two or three stages can be used.
2. Including a resistor R_s in the source lead of the CS stage provides a number of performance improvements at the expense of gain reduction.
3. The low input resistance of the CG amplifier makes it useful only in specific applications. As we shall see in Chapter 9, it has a much better high-frequency response than the CS amplifier. This superiority makes it useful as a high-frequency amplifier, especially when combined with the CS circuit. We shall see one such combination in Chapter 7.
4. The source follower finds application as a voltage buffer for connecting a high-resistance source to a low-resistance load and as the output stage in a multistage amplifier where its purpose is to equip the amplifier with a low output resistance.

5.7 Biasing in MOS Amplifier Circuits

As discussed in Section 5.4, an essential step in the design of a MOSFET amplifier circuit is the establishment of an appropriate dc operating point for the transistor. This is the step known as biasing or bias design. An appropriate dc operating point or bias point is characterized by a stable and predictable dc drain current I_D and by a dc drain-to-source voltage V_{DS} that ensures operation in the saturation region for all expected input-signal levels.

5.7.1 Biasing by Fixing V_{GS}

The most straightforward approach to biasing a MOSFET is to fix its gate-to-source voltage V_{GS} to the value required⁹ to provide the desired I_D . This voltage value can be derived from the power-supply voltage V_{DD} through the use of an appropriate voltage divider. Alternatively, it can be derived from another suitable reference voltage that might be available in the system. Independent of how the voltage V_{GS} may be generated, this is *not* a good approach to biasing a MOSFET. To understand the reason for this statement, recall that

$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_t)^2$$

and note that the values of the threshold voltage V_t , the oxide-capacitance C_{ox} , and (to a lesser extent) the transistor aspect ratio W/L vary widely among devices of supposedly the same size and type. This is certainly the case for discrete devices, in which large spreads in the values of these parameters occur among devices of the same manufacturer's part number. The spread is also large in integrated circuits, especially among devices fabricated on different wafers and certainly between different batches of wafers. Furthermore, both V_t and μ_n depend on temperature, with the result that if we fix the value of V_{GS} , the drain current I_D becomes very much temperature dependent.

To emphasize the point that biasing by fixing V_{GS} is not a good technique, we show in Fig. 5.51 two i_D-v_{GS} characteristic curves representing extreme values in a batch of MOSFETs of the same type. Observe that for the fixed value of V_{GS} , the resultant spread in the values of the drain current can be substantial.

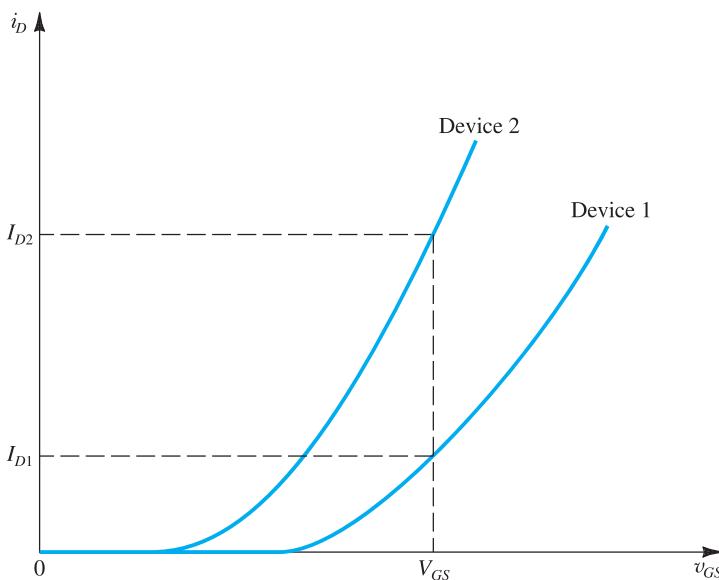


Figure 5.51 The use of fixed bias (constant V_{GS}) can result in a large variability in the value of I_D . Devices 1 and 2 represent extremes among units of the same type.

⁹That is indeed what we were doing in Section 5.4. However, the amplifier circuits studied there were conceptual ones, not actual practical circuits. Our purpose in this section is to study the latter.

5.7.2 Biasing by Fixing V_G and Connecting a Resistance in the Source

An excellent biasing technique for discrete MOSFET circuits consists of fixing the dc voltage at the gate, V_G , and connecting a resistance in the source lead, as shown in Fig. 5.52(a). For this circuit we can write

$$V_G = V_{GS} + R_S I_D \quad (5.93)$$

Now, if V_G is much greater than V_{GS} , I_D will be mostly determined by the values of V_G and R_S . However, even if V_G is not much larger than V_{GS} , resistor R_S provides *negative feedback*, which acts to stabilize the value of the bias current I_D . To see how this comes about, consider what happens when I_D increases for whatever reason. Equation (5.93) indicates that since V_G is constant, V_{GS} will have to decrease. This in turn results in a decrease in I_D , a change that is

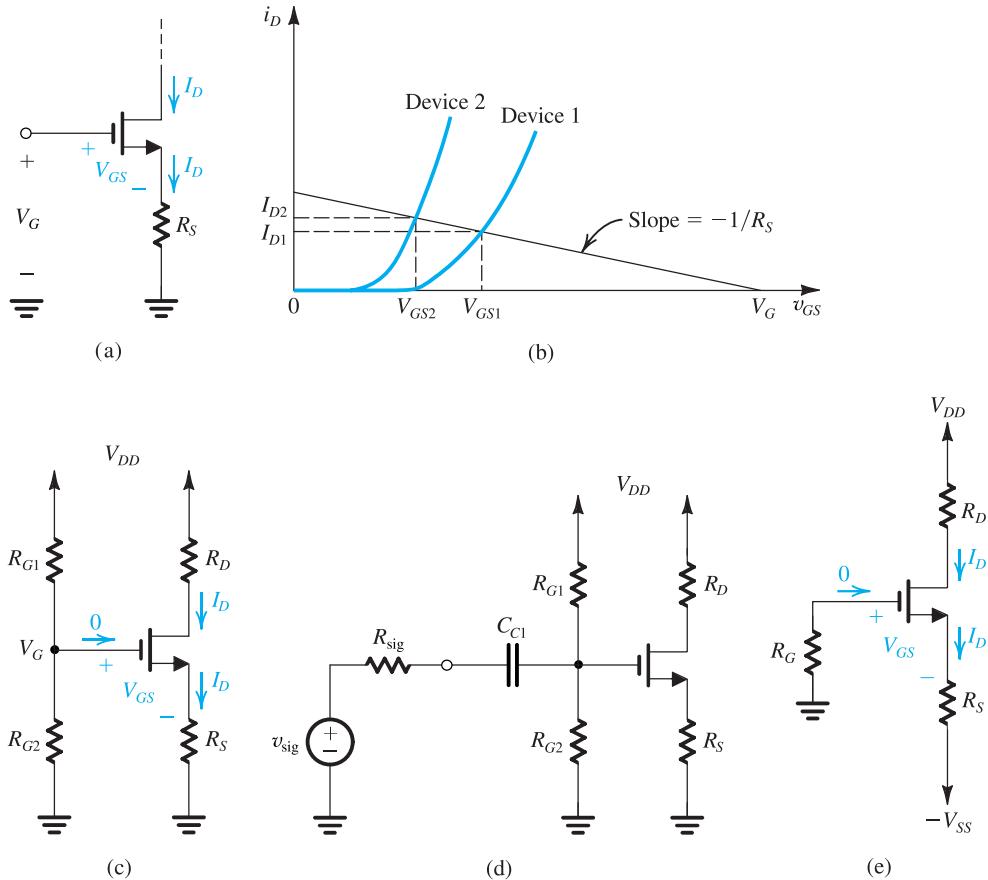


Figure 5.52 Biasing using a fixed voltage at the gate, V_G , and a resistance in the source lead, R_S : (a) basic arrangement; (b) reduced variability in I_D ; (c) practical implementation using a single supply; (d) coupling of a signal source to the gate using a capacitor C_{C1} ; (e) practical implementation using two supplies.

opposite to that initially assumed. Thus the action of R_s works to keep I_D as constant as possible. This negative feedback action of R_s gives it the name **degeneration resistance**, a name that we will appreciate much better at a later point in this text.¹⁰

Figure 5.52(b) provides a graphical illustration of the effectiveness of this biasing scheme. Here too we show the i_D-v_{GS} characteristics for two devices that represent the extremes of a batch of MOSFETs. Superimposed on the device characteristics is a straight line that represents the constraint imposed by the bias circuit—namely, Eq. (5.93). The intersection of this straight line with the i_D-v_{GS} characteristic curve provides the coordinates (I_D and V_{GS}) of the bias point. Observe that compared to the case of fixed V_{GS} , here the variability obtained in I_D is much smaller. Also, note that the variability decreases as V_G and R_s are made larger (thus providing a bias line that is less steep).

Two possible practical discrete implementations of this bias scheme are shown in Fig. 5.52(c) and (e). The circuit in Fig. 5.52(c) utilizes one power-supply V_{DD} and derives V_G through a voltage divider (R_{G1} , R_{G2}). Since $I_G = 0$, R_{G1} and R_{G2} can be selected to be very large (in the megohm range), allowing the MOSFET to present a large input resistance to a signal source that may be connected to the gate through a coupling capacitor, as shown in Fig. 5.52(d). Here capacitor C_{Cl} blocks dc and thus allows us to couple the signal v_{sig} to the amplifier input without disturbing the MOSFET dc bias point. The value of C_{Cl} should be selected large enough to approximate a short circuit at all signal frequencies of interest. We shall study capacitively coupled MOSFET amplifiers, which are suitable only in discrete circuit design, in Section 5.8. Finally, note that in the circuit of Fig. 5.52(c), resistor R_D is selected to be as large as possible to obtain high gain but small enough to allow for the desired signal swing at the drain while keeping the MOSFET in saturation at all times.

When two power supplies are available, as is often the case, the somewhat simpler bias arrangement of Fig. 5.52(e) can be utilized. This circuit is an implementation of Eq. (5.93), with V_G replaced by V_{SS} . Resistor R_G establishes a dc ground at the gate and presents a high input resistance to a signal source that may be connected to the gate through a coupling capacitor.

Example 5.12

It is required to design the circuit of Fig. 5.52(c) to establish a dc drain current $I_D = 0.5$ mA. The MOSFET is specified to have $V_t = 1$ V and $k'_nW/L = 1$ mA/V². For simplicity, neglect the channel-length modulation effect (i.e., assume $\lambda = 0$). Use a power-supply $V_{DD} = 15$ V. Calculate the percentage change in the value of I_D obtained when the MOSFET is replaced with another unit having the same k'_nW/L but $V_t = 1.5$ V.

Solution

As a rule of thumb for designing this classical biasing circuit, we choose R_D and R_s to provide one-third of the power-supply voltage V_{DD} as a drop across each of R_D , the transistor (i.e., V_{DS}) and R_s . For $V_{DD} = 15$ V,

¹⁰The action of R_s in stabilizing the value of the bias current I_D is not unlike that of the resistance R_s , which we included in the source lead of a CS amplifier in Section 5.6.4. In the latter case also, R_s works to reduce the change in i_D with the result that the amplifier gain is reduced.

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Example 5.12 continued

this choice makes $V_D = +10$ V and $V_S = +5$ V. Now, since I_D is required to be 0.5 mA, we can find the values of R_D and R_S as follows:

$$R_D = \frac{V_{DD} - V_D}{I_D} = \frac{15 - 10}{0.5} = 10 \text{ k}\Omega$$

$$R_S = \frac{V_S}{I_D} = \frac{5}{0.5} = 10 \text{ k}\Omega$$

The required value of V_{GS} can be determined by first calculating the overdrive voltage V_{ov} from

$$I_D = \frac{1}{2}k'_n(W/L)V_{ov}^2$$

$$0.5 = \frac{1}{2} \times 1 \times V_{ov}^2$$

which yields $V_{ov} = 1$ V, and thus,

$$V_{GS} = V_t + V_{ov} = 1 + 1 = 2 \text{ V}$$

Now, since $V_S = +5$ V, V_G must be

$$V_G = V_S + V_{GS} = 5 + 2 = 7 \text{ V}$$

To establish this voltage at the gate we may select $R_{G1} = 8 \text{ M}\Omega$ and $R_{G2} = 7 \text{ M}\Omega$. The final circuit is shown in Fig. 5.53. Observe that the dc voltage at the drain (+10 V) allows for a positive signal swing of +5 V (i.e., up to V_{DD}) and a negative signal swing of -4 V [i.e., down to $(V_G - V_t)$].

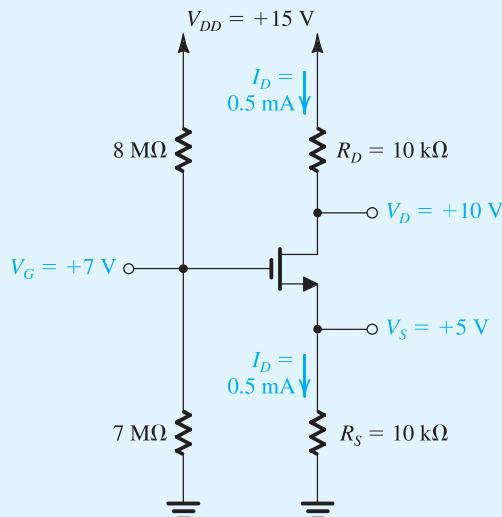


Figure 5.53 Circuit for Example 5.12.

If the NMOS transistor is replaced with another having $V_t = 1.5$ V, the new value of I_D can be found as follows:

$$I_D = \frac{1}{2} \times 1 \times (V_{GS} - 1.5)^2 \quad (5.94)$$

$$\begin{aligned} V_G &= V_{GS} + I_D R_S \\ 7 &= V_{GS} + 10I_D \end{aligned} \quad (5.95)$$

Solving Eqs. (5.94) and (5.95) together yields

$$I_D = 0.455 \text{ mA}$$

Thus the change in I_D is

$$\Delta I_D = 0.455 - 0.5 = -0.045 \text{ mA}$$

which is $\frac{-0.045}{0.5} \times 100 = -9\%$ change.

EXERCISES

- 5.33** Consider the MOSFET in Example 5.12 when fixed- V_{GS} bias is used. Find the required value of V_{GS} to establish a dc bias current $I_D = 0.5$ mA. Recall that the device parameters are $V_t = 1$ V, $k'_n W/L = 1 \text{ mA/V}^2$, and $\lambda = 0$. What is the percentage change in I_D obtained when the transistor is replaced with another having $V_t = 1.5$ V?

Ans. $V_{GS} = 2$ V; -75%

- D5.34** Design the circuit of Fig. 5.52(e) to operate at a dc drain current of 0.5 mA and $V_D = +2$ V. Let $V_t = 1$ V, $k'_n W/L = 1 \text{ mA/V}^2$, $\lambda = 0$, $V_{DD} = V_{SS} = 5$ V. Use standard 5% resistor values (see Appendix G), and give the resulting values of I_D , V_D , and V_S .

Ans. $R_D = R_S = 6.2 \text{ k}\Omega$; $I_D = 0.49$ mA, $V_S = -1.96$ V, and $V_D = +1.96$ V. R_G can be selected in the range of $1 \text{ M}\Omega$ to $10 \text{ M}\Omega$.

5.7.3 Biasing Using a Drain-to-Gate Feedback Resistor

A simple and effective discrete-circuit biasing arrangement utilizing a feedback resistor connected between the drain and the gate is shown in Fig. 5.54. Here the large feedback resistance R_G (usually in the megohm range) forces the dc voltage at the gate to be equal to that at the drain (because $I_G = 0$). Thus we can write

$$V_{GS} = V_{DS} = V_{DD} - R_D I_D$$

which can be rewritten in the form

$$V_{DD} = V_{GS} + R_D I_D \quad (5.96)$$

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which is identical in form to Eq. (5.93), which describes the operation of the bias scheme discussed above [that in Fig. 5.52(a)]. Thus, here too, if I_D for some reason changes, say increases, then Eq. (5.96) indicates that V_{GS} must decrease. The decrease in V_{GS} in turn causes a decrease in I_D , a change that is opposite in direction to the one originally assumed. Thus the negative feedback or degeneration provided by R_G works to keep the value of I_D as constant as possible.

The circuit of Fig. 5.54 can be utilized as an amplifier by applying the input voltage signal to the gate via a coupling capacitor so as not to disturb the dc bias conditions already established. The amplified output signal at the drain can be coupled to another part of the circuit, again via a capacitor. We have considered such an amplifier circuit in Section 5.5 (Example 5.10).

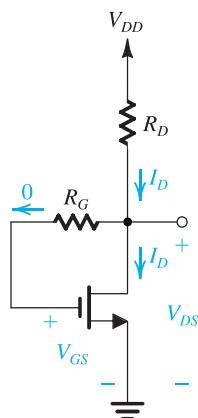


Figure 5.54 Biasing the MOSFET using a large drain-to-gate feedback resistance, R_G .

EXERCISE

D5.35 Design the circuit in Fig. 5.54 to operate at a dc drain current of 0.5 mA. Assume $V_{DD} = +5$ V, $k'_n W/L = 1 \text{ mA/V}^2$, $V_t = 1 \text{ V}$, and $\lambda = 0$. Use a standard 5% resistance value for R_D , and give the actual values obtained for I_D and V_D .

Ans. $R_D = 6.2 \text{ k}\Omega$; $I_D \approx 0.49 \text{ mA}$; $V_D \approx 1.96 \text{ V}$

5.7.4 Biasing Using a Constant-Current Source

The most effective scheme for biasing a MOSFET amplifier is that using a constant-current source. Figure 5.55(a) shows such an arrangement applied to a discrete MOSFET. Here R_G (usually in the megohm range) establishes a dc ground at the gate and presents a large resistance to an input signal source that can be capacitively coupled to the gate. Resistor R_D establishes an appropriate dc voltage at the drain to allow for the required output signal swing while ensuring that the transistor always remains in the saturation region.

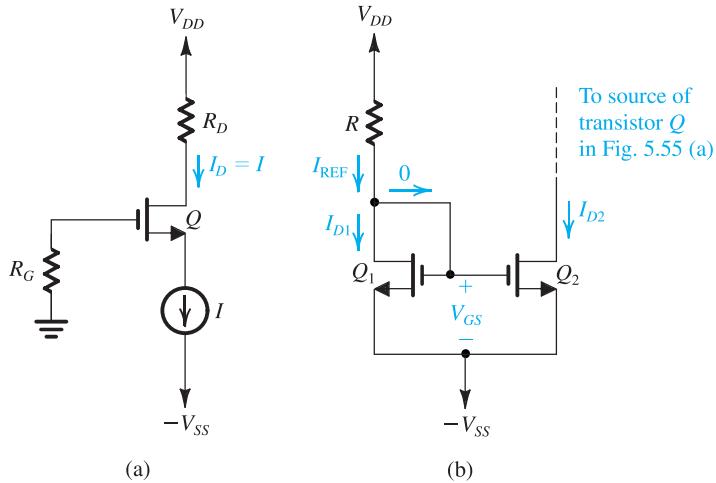


Figure 5.55 (a) Biasing the MOSFET using a constant-current source I . (b) Implementation of the constant-current source I using a current mirror.

A circuit for implementing the constant-current source I is shown in Fig. 5.55(b). The heart of the circuit is transistor Q_1 , whose drain is shorted to its gate, and thus is operating in the saturation region, such that

$$I_{D1} = \frac{1}{2} k'_n \left(\frac{W}{L} \right)_1 (V_{GS} - V_t)^2 \quad (5.97)$$

where we have neglected channel-length modulation (i.e., assumed $\lambda = 0$). The drain current of Q_1 is supplied by V_{DD} through resistor R . Since the gate currents are zero,

$$I_{D1} = I_{\text{REF}} = \frac{V_{DD} + V_{SS} - V_{GS}}{R} \quad (5.98)$$

where the current through R is considered to be the *reference current* of the current source and is denoted I_{REF} . Given the parameter values of Q_1 and a desired value for I_{REF} , Eqs. (5.97) and (5.98) can be used to determine the value of R . Now consider transistor Q_2 : It has the same V_{GS} as Q_1 ; thus if we assume that it is operating in saturation, its drain current, which is the desired current I of the current source, will be

$$I = I_{D2} = \frac{1}{2} k'_n \left(\frac{W}{L} \right)_2 (V_{GS} - V_t)^2 \quad (5.99)$$

where we have neglected channel-length modulation. Equations (5.98) and (5.99) enable us to relate the current I to the reference current I_{REF} ,

$$I = I_{\text{REF}} \frac{(W/L)_2}{(W/L)_1} \quad (5.100)$$

Thus I is related to I_{REF} by the ratio of the aspect ratios of Q_1 and Q_2 . This circuit, known as a **current mirror**, is very popular in the design of IC MOS amplifiers and will be studied in great detail in Chapter 7.

EXERCISE

D5.36 Using two transistors Q_1 and Q_2 having equal lengths but widths related by $W_2/W_1 = 5$, design the circuit of Fig. 5.55(b) to obtain $I = 0.5$ mA. Let $V_{DD} = -V_{SS} = 5$ V, $k'_n(W/L)_1 = 0.8$ mA/V 2 , $V_t = 1$ V, and $\lambda = 0$. Find the required value for R . What is the voltage at the gates of Q_1 and Q_2 ? What is the lowest voltage allowed at the drain of Q_2 while Q_2 remains in the saturation region?

Ans. 85 k Ω ; -3.5 V; -4.5 V

5.7.5 A Final Remark

The bias circuits studied in this section are intended for discrete-circuit applications. The only exception is the current mirror circuit of Fig. 5.55(b) which, as mentioned above, is extensively used in IC design. Bias arrangements for IC MOS amplifiers will be studied in Chapter 7.

5.8 Discrete-Circuit MOS Amplifiers

With our study of MOS amplifier basics complete, we now put everything together by presenting practical circuits for discrete-circuit amplifiers. These circuits, which utilize the amplifier configurations studied in Section 5.6 and one of the biasing methods of Section 5.7, can be assembled using off-the-shelf discrete transistors, resistors, and capacitors. Though practical and carefully selected to illustrate some important points, the circuits presented in this section should be regarded only as examples of discrete-circuit MOS amplifiers. Indeed, there is a great variety of such circuits, a number of which are explored in the end-of-chapter problems. We should, however, caution the reader that MOS transistors are primarily used in integrated circuit design, as we shall see in Chapter 7 and beyond.

In this section we present a series of exercise problems, Exercises 5.37 to 5.41, that are carefully designed to illustrate important aspects of the amplifier circuits studied. These exercises are also intended to enable the reader to see more clearly the differences between the various circuit configurations. We strongly urge the reader to solve these exercises. As usual, the answers are provided.

5.8.1 The Basic Structure

Figure 5.56 shows the basic circuit we shall utilize to implement the various configurations of discrete-circuit MOS amplifiers. Among the various schemes for biasing MOS amplifiers (Section 5.7), we have selected, for both its effectiveness and its simplicity, the one employing constant-current biasing. Figure 5.56 indicates the dc current and the dc voltages resulting at various nodes.

EXERCISE

5.37 Consider the circuit of Fig. 5.56 for the case $V_{DD} = V_{SS} = 10$ V, $I = 0.5$ mA, $R_G = 4.7$ M Ω , $R_D = 15$ k Ω , $V_t = 1.5$ V, and $k'_n(W/L) = 1$ mA/V 2 . Find V_{OV} , V_{GS} , V_G , V_S , and V_D . Also, calculate the values of g_m and r_o , assuming that $V_A = 75$ V. What is the maximum possible signal swing at the drain for which the MOSFET remains in saturation?

Ans. See Fig. E5.37; without taking into account the signal swing at the gate, the drain can swing to -1.5 V, a negative signal swing of 4 V

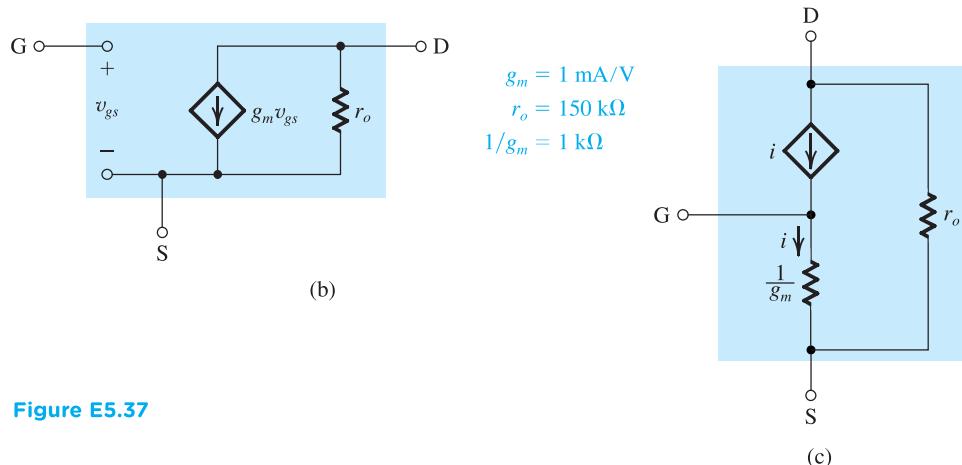
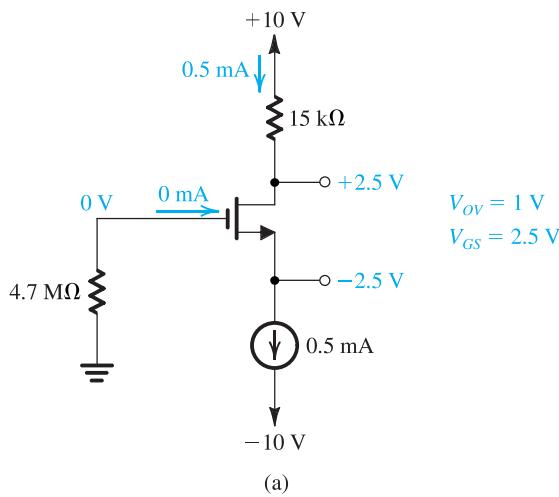


Figure E5.37

5.8.2 The Common-Source (CS) Amplifier

As mentioned in Section 5.6, the common-source (CS) configuration is the most widely used of all MOSFET amplifier circuits. A common-source amplifier realized using the circuit of Fig. 5.56 is shown in Fig. 5.57(a). Observe that to establish a **signal ground**, or an **ac ground** as it is sometimes called, at the source, we have connected a large capacitor, C_s , between the source and ground. This capacitor, usually in the microfarad range, is required to provide a very small impedance (ideally, zero impedance; i.e., in effect, a short circuit) at all signal frequencies of interest. In this way, the signal current passes through C_s to ground and thus *bypasses* the output resistance of current source I (and any other circuit component that might be connected to the MOSFET source); hence, C_s is called a **bypass capacitor**. Obviously, the lower the signal frequency, the less effective the bypass capacitor becomes. This issue will be studied in Section 9.1. For our purposes here we shall assume that C_s is acting as a perfect short circuit and thus is establishing a zero signal voltage at the MOSFET source.

In order not to disturb the dc bias current and voltages, the signal to be amplified, shown as voltage source v_{sig} with an internal resistance R_{sig} , is connected to the gate through a large capacitor C_{c1} . Capacitor C_{c1} , known as a **coupling capacitor**, is required to act as a perfect short circuit at all signal frequencies of interest while blocking dc. Here again, we note that as the signal frequency is lowered, the impedance of C_{c1} (i.e., $1/j\omega C_{c1}$) will increase and its effectiveness as a coupling capacitor will be correspondingly reduced. This problem too will be considered in Section 9.1 when the dependence of the amplifier operation on frequency is studied. For our purposes here we shall assume C_{c1} is acting as a perfect short circuit as far as the signal is concerned. Before leaving C_{c1} , we should point out that when the signal source can provide an appropriate dc path to ground, the gate can be connected directly to the signal source and both R_G and C_{c1} can be dispensed with.

The voltage signal resulting at the drain is coupled to the load resistance R_L via another coupling capacitor C_{c2} . We shall assume that C_{c2} acts as a perfect short circuit at all signal frequencies of interest and thus that the output voltage $v_o = v_d$. Note that R_L can be either an actual load resistor, to which the amplifier is required to provide its output voltage signal, or it can be the input resistance of another amplifier stage in cases where more than one stage of amplification is needed. (We will study multistage amplifiers in Chapter 8.)

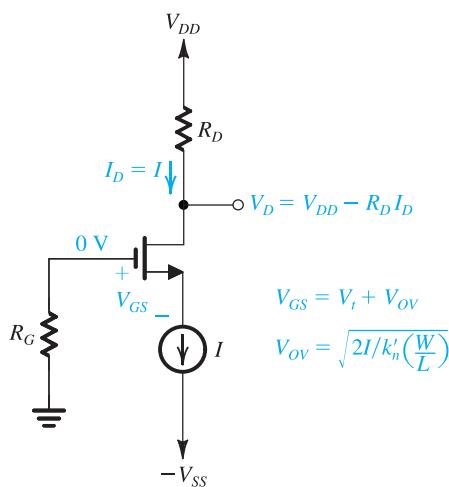


Figure 5.56 Basic structure of the circuit used to realize single-stage, discrete-circuit MOS amplifier configurations.

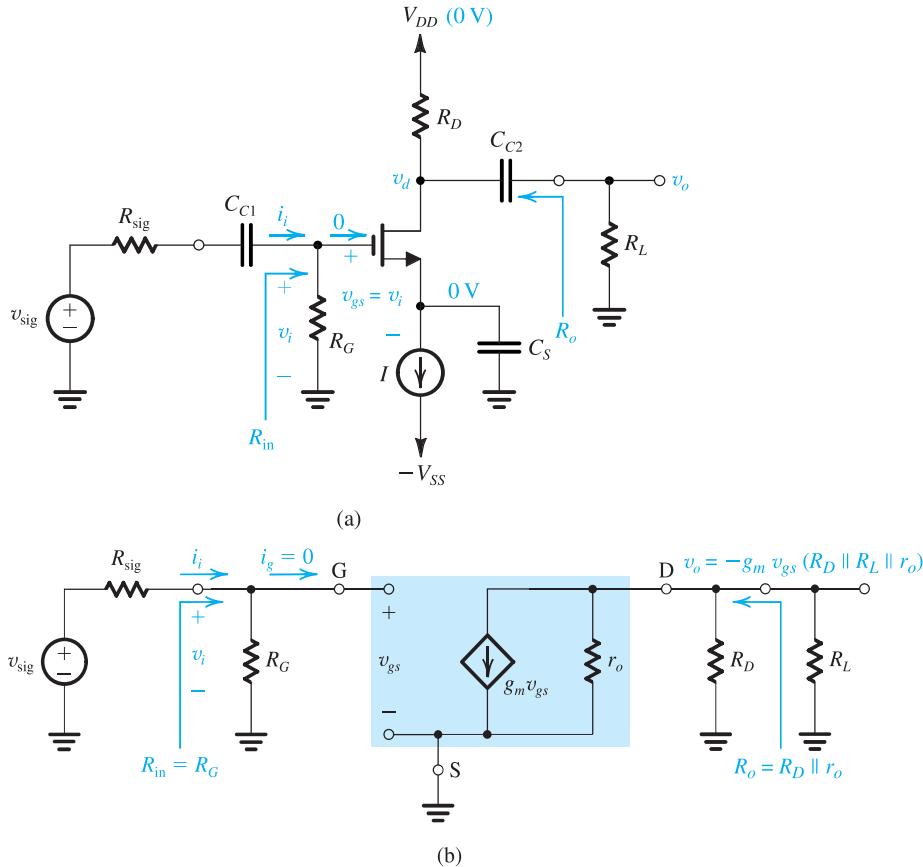


Figure 5.57 (a) Common-source amplifier based on the circuit of Fig. 5.56. (b) Equivalent circuit of the amplifier for small-signal analysis.

To determine the terminal characteristics of the CS amplifier—that is, its input resistance, voltage gain, and output resistance—we replace the MOSFET with its small-signal model. The resulting circuit is shown in Fig. 5.57(b).

We observe that the only difference between this circuit and the stripped-down version studied in Section 5.6.3 (Fig. 5.45) is that here we have the bias resistance R_G . Since R_G appears across the input terminals of the amplifier, the input resistance will no longer be infinite, rather

$$R_{in} = R_G$$

To keep R_{in} high, a large value of R_G (in the megohm range) is usually selected. The finite R_{in} will affect the overall voltage gain G_v , which becomes

$$G_v = -\frac{R_G}{R_G + R_{sig}} g_m (R_D \parallel R_L \parallel r_o) \quad (5.101)$$

Finally, to encourage the reader to do the analysis directly on the circuit diagram, with the MOSFET model used implicitly, we show some of the analysis on the circuit in Fig. 5.57(a).

EXERCISE

- 5.38** Consider a CS amplifier based on the circuit analyzed in Exercise 5.37. Specifically, refer to the results of that exercise shown in Fig. E5.37. Find R_{in} , A_{vo} , and R_o , both without and with r_o taken into account. Then calculate the overall voltage gain G_v , with r_o taken into account, for the case $R_{sig} = 100 \text{ k}\Omega$ and $R_L = 15 \text{ k}\Omega$. If v_{sig} is a 0.4-V peak-to-peak sinusoid, what output signal v_o results?

Ans. Without r_o : $R_{in} = 4.7 \text{ M}\Omega$, $A_{vo} = -15 \text{ V/V}$, and $R_o = 15 \text{ k}\Omega$; with r_o : $R_{in} = 4.7 \text{ M}\Omega$, $A_{vo} = -13.6 \text{ V/V}$, and $R_o = 13.6 \text{ k}\Omega$; $G_v = -7 \text{ V/V}$; v_o is a 2.8-V peak-to-peak sinusoid superimposed on a dc drain voltage of +2.5 V.

5.8.3 The Common-Source Amplifier with a Source Resistance

As demonstrated in Section 5.6.4, a number of beneficial results can be obtained by connecting a resistance R_s in the source lead of the transistor in the CS amplifier. This is shown in Fig. 5.58(a), where R_s is, of course, unbypassed. Figure 5.58(b) shows the small-signal equivalent-circuit model. Observe that the only difference between this circuit and the simplified version studied in Section 5.6.4 is the bias resistance R_G that appears across the input terminals and makes R_{in} finite. This will in turn affect the overall voltage gain G_v , which becomes

$$G_v = -\frac{R_G}{R_G + R_{sig}} \frac{R_D \parallel R_L}{1/g_m + R_s} \quad (5.102)$$

Finally, note that much of the analysis is shown both on the actual circuit in Fig. 5.58(a) and on the equivalent circuit in Fig. 5.58(b).

EXERCISE

- 5.39** In Exercise 5.38 we applied an input signal of 0.4 V peak-to-peak, which resulted in an output signal of the CS amplifier of 2.8 V peak-to-peak. Assume that for some reason we now have an input signal three times as large as before (i.e., 1.2 V p-p) and that we wish to modify the circuit to keep the output signal level unchanged. What value should we use for R_s ?

Ans. 2.15 kΩ

5.8.4 The Common-Gate (CG) Amplifier

Figure 5.59(a) shows a CG amplifier obtained from the circuit of Fig. 5.56. Observe that since both the dc and ac voltages at the gate are to be zero, we have connected the gate directly to ground, thus eliminating resistor R_G altogether. Coupling capacitors C_{C1} and C_{C2} perform similar functions to those in the CS circuit.

The small-signal, equivalent circuit model of the CG amplifier is shown in Fig. 5.59(b). We note that this circuit is identical to the equivalent circuit of the stripped-down version of the CG amplifier, in Fig. 5.48(b). Thus the analysis performed and the results obtained in Section 5.6.5 apply directly here. A substantial portion of the analysis is also shown in Fig. 5.59.