Study of NMOS and CMOS Characteristics

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The Problem Statement

In this experiment, we will do the following:

* Measure NMOS output and transfer characteristics
* Investigate the effect of body bias on the characteristics of a NMOS transistor
* Measure voltage transfer characteristics of CMOS inverter
* Measure transient characteristics of CMOS inverter

Part 1- I_D-V_{DS} Characteristics

1. Write ngspice netlist to plot the I_D-V_{DS} characteristics of NMOS with the voltage V_{GS} varied from 2.5 V to 4 V in steps of 0.5 V. You may vary V_{DS} from 0 V to 5 V(show all 4 curves on a single plot)
2. From these characteristics, obtain r_{DS} (linear region) for each value of V_{GS}. Also, find "Early voltage" and r_0 in saturation region(considering channel length modulation)

Part 2- I_D-V_{GS} Characteristics in different regions

1. Estimate the value of threshold voltage and transconductance g_m in **linear region**:
   - Bias the transistor in linear region by keeping $V_{DS} = 200$ mV
   - Now write ngspice netlist to plot I_D v/s V_{GS} characteristics by varying V_{GS} from 0 to 5 V
   - From this characteristic, obtain V_T and g_m
2. Estimate the value of threshold voltage in **saturation region**:
   - Bias the transistor in saturation region by keeping $V_{DS} = 5$ V
   - Now write ngspice netlist to plot I_D v/s V_{GS} characteristics by varying V_{GS} from 0 to 5 V
   - From this characteristic, obtain V_T
   - Also, plot $\sqrt{I_D}$ v/s V_{GS} to find parameter K(mention its unit)

Part 3- Effect of Body Bias

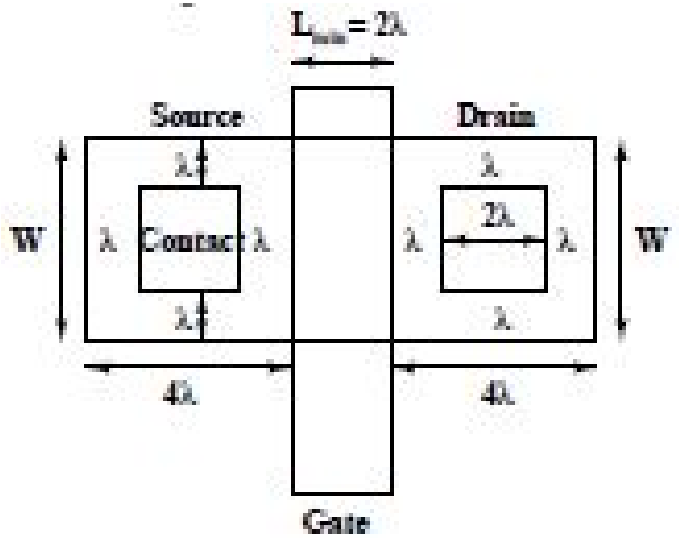
1. Bias the transistor in linear region by keeping $V_{DS} = 200$ mV
2. Now write ngspice netlist to plot I_D v/s V_{GS} characteristics by varying V_{GS} from 0 to 5 V for V_{SB}= 0 V. (which is already asked in part 2)
3. Repeat the above step to get four more sets of I_D v/s V_{GS} characteristics for $V_{SB} = 1$, 2, 3, and 4 V
4. Show all five I_D v/s V_{GS} characteristics on the same plot.
5. Obtain the value of threshold voltage from each plot
6. Plot V_T v/s V_{SB} and Obtain body effect coefficient (γ) using below equation. comment on dependence of V_T on V_{SB}

   $$V_T = V_{T0} + \gamma(\sqrt{\phi_s + V_{SB}} - \sqrt{\phi_s})$$

   where ϕ_s is Surface Potential = 0.9 V for ALD1105N NMOS model, Threshold voltage (V_T) = V_{T0} when $V_{SB} = 0$ V

CMOS Inverter

1. Write ngspice netlist for static CMOS inverter with load capacitance 0.05pF and VDD= 3.3 V. Logic low is 0V, logic High is 3.3V
2. specify source and drain capacitance using below information:
   source/drain area $= 2 * W * L_{min}$
   source/drain perimeter $= 2(W + 2 * L_{min})$



3. use the below template for instantiating nmos:
   mn drain gate source body cmosn L=0.4u W=Wn AS=2*Wn*L PS=2*Wn+4*L AD=2*Wn*L PD=2*Wn+4*L
4. Plot Voltage Transfer Characteristics(VTC) i.e V_{out} vs V_{in} for $W_p/W_n = 60um/30um$, $L = 0.4um(= L_{min})$
5. Find out switching threshold from VTC curve

CMOS Inverter: Voltage Transfer Characteristics

1. Now take $W_p/W_n = 60um/60um$ and $W_p/W_n = 30um/60um$ and plot voltage transfer characteristics on a single plot along with the plot for $W_p/W_n = 60um/30um$. Comment on VTC curves behaviour and switching threshold.
2. Change the supply voltage VDD to 1.5V, 3V for $W_p/W_n = 60um/30um$ and obtain all VTC curves on a single plot. Comment on the plots

CMOS Inverter: Transient Characteristics

1. Input square wave signal of frequency 125MHZ with rise time and fall time of 20ps to CMOS inverter having load capacitance(C_L=0.05pF) and VDD=3.3V
2. **Rise delay(t_r):** t_r is time to rise output from 10% value to 90% value
   Fall delay(t_f): t_f is time to fall output from 90%value to 10% value
   Propagation delay (t_p): Measures speed of output reaction to input change

   $t_p = (t_{pf} + t_{pr})/2$

   • Fall propagation delay, tpf is time for output to fall by 50% with reference to input change by 50%
   • Rise propagation delay, tpr is time for output to rise by 50% with reference to input change by 50%
3. Find rise, fall, propagation delays for $W_p/W_n = 60um/30um, W_p/W_n = 60um/60um, W_p/W_n = 30um/60um$ and comment on each obtained values
4. Vary the supply voltage from 2V to 3.3V and plot propagation delay vs. supply voltage(VDD) for $W_p/W_n = 60um/30um$ and comment on the plot
   Note: While changing supply voltage change input square wave voltage respectively