Indian Institute of Technology, Bombay
Department of Electrical Engineering
Electronic Devices Lab(EE-236)
Quiz 2, Date: March 23rd, 2022

Timing: 3:00 PM to 4:10 PM | Spring 2022 | Max marks: 5

Instructions

- You are allowed to use only those models that have been provided. You can download by clicking the name.
- Read the questions thoroughly.
- You can use previous lab reports and netlist.

Part-2

1. Suppose you are working in a leading processor design company Orange Inc. You have to design logic cells (basic logic gates) with low and high power configuration for a upcoming processor Mx Ultra. Lets assume that you have an dynamic V_{th} CMOS inverter logic cell (Dynamic V_{th} means you have the option to vary the substrate voltage of both the NMOS and the PMOS). Case 3 (See Table 1) is the standard one where substrates of NMOS and PMOS are connected to ground and supply respectively.

   - Make the rise and fall time equal by adjusting width of the PMOS FET. Fill up the table below using simulations.
   - Explain the reason for reduction / increase in peak charging and discharging current and delay (Charging current flows from supply to output capacitor through PMOS and discharging current flows from capacitor to ground through NMOS).
   - Comment on V_{th} for NMOS and PMOS for each of the following cases in the table 1 (increases / decreases and why?) with respect to case 3 (See Table 1) (where bodies of NMOS and PMOS are shorted to their respective sources).
   - What will be the substrate voltages from the following cases in the Table for NMOS and PMOS in the logic cells for low power mode if performance is not the main priority? ***(2 +1 + 1 + 1 = 5 Marks)***
     Here are the specifications:
     - Power supply 3.3 V
     - Output capacitance = 200 fF
     - W_n (Width of NMOS) = 1.2 μm
     - $Length = 0.4\ \mu m$
     - Pulse specs:
       * $V_{peak} = 3.3V$
       * Rise time = Fall time = 500 ps
       * Pulse Width = 4.5 ns
       * Pulse Period = 10 ns

Table 1:

Cases	Body Bias NMOS	Body Bias PMOS	Peak Charging Current	Peak Discharging Current	Delay Time
1	0.3 V	3.0 V			
2	0.1 V	3.2 V			
3	0 V	3.3 V			
4	-0.5 V	3.8 V			
5	-1.0 V	4.3 V			

Note: For both questions use PMOS_NMOS model file, the same as you have used for CMOS inverter experiment in last lab (Click on the name). For your reference regarding the commands you can refer the Appendix on the last page.

1 Appendix

Command for measuring delay, rise and fall time:
.measure tran rise trig v(out) val=0.33 rise=1 targ v(out) val=2.97 rise=1
.measure tran delay trig v(a) val=1.665 rise=2 targ v(out) val=1.665 fall=2
.measure tran fall trig v(out) val=2.97 fall=1 targ v(out) val=0.33 fall=1

Format for pulse:
va a 0 pulse(0 3.3v 0 500p 500p 4500p 10n)