Indian Institute of Technology, Bombay
Department of Electrical Engineering
Electronic Devices Lab (EE-236)
End-Sem Exam, Date: April 13, 2022

Timing: 1:45 PM to 4:15 PM | Spring 2022 | Max marks: 20

Instructions

- You can use previous lab reports, netlists and model files shared with you.
- **For all the questions show the circuit schematic to your TA.**

Problem Statements

1. **BJT vs MOSFET comparison w.r.t temperature coefficient and switching speed.**
   (a) Plot collector current (I_C) vs V_{CE} in NPN-BJT common emitter configuration by setting I_B= 0.1 mA. Extract I_C values at V_{CE}= 3 V for temperature varying from 25 °C to 55 °C in steps of 10 °C. Then plot I_C vs. temperature where temperature varies from 25 °C to 55 °C. Explain the behavior of this plot. (Hint: Recall that I_C=I_S $e^{qV_{BE}/kT}$, where I_S=$\frac{qA_E D_n n_i^2}{N_B W_B}$. Ignore temperature dependence of V_{BE}.)
   (b) Plot drain current (I_D) vs V_{DS} in N-MOSFET common source configuration by setting V_{GS}= 3 V. Extract I_D values at V_{DS}= 3 V for temperatures varying from 25 °C to 55 °C in steps of 10 °C. Then plot I_D vs temperature by varying it from 25 °C to 55 °C. Explain the behavior of this plot and compare it with BJT. (Hint: Recall that I_{DS}=$\frac{\mu C_{ox} W}{L}$(V_{GS}-V_{TH})^2. Ignore temperature dependence of V_{GS}.)
   (c) Find the turn-off times for the NPN-BJT and N-MOSFET for a pulse input with an on-time of 0.25 μs. Which of the two devices turns-off faster? What is the likely reason for this difference in switching speed?

   (2 + 2 + 2 = 6 Marks)

   Model files: BC547a, NMOSFET

2. **Temperature dependence of MOSFET. Use the same NMOS model file.**
   (a) Extract and plot mobility vs. V_{GS} curve for the N-MOSFET for a fixed V_{DS} = 0.3 V. Vary V_{GS} from 0.3 V to 3.3 V. You must take the linear approximation of the MOSFET current equation. What mechanisms are likely to explain the nature of the plot? (W/L = 1.2 μm/0.4 μm, $C_{ox} = 450nF/cm^2$)
   (b) Plot the mobility vs. temperature for the following cases
   - V_{GS}=1.5 V and V_{DS}= 0.3 V.
   - V_{GS}=0.6 V and V_{DS}= 0.3 V.

   Vary the temperature from 20 °C to 80 °C in steps of 10 °C and explain the reason for the nature of the plot based on the temperature dependence of mobility-scattering mechanisms. Can this help to explain the plot in (a)?

(c) Consider an N-channel MOSFET with W=30 μm and L=0.4 μm. Plot $\log_{10}(I_{DS})$ vs. V_{GS} for temperatures 25 °C, 75 °C, 125 °C and find the sub-threshold slope (SS in mV/decade) below V_{TN}, where $SS = (\partial \log_{10} I_{DS}/\partial V_{GS})^{-1}$ in units of mV/decade, and off-current (When V_{GS} = 0V) for these curves. Based on the SS and off-current dependence on temperature, qualitatively comment on the power consumption of the MOSFET with varying temperature.

(2 + 2 + 2 = 6 Marks)

3. **Comparison of long channel (LC) and short channel (SC) MOSFETs. Use the same NMOS model file.**

   - **Short channel NMOS:** $W = 1.2\ \mu m,\ L = 0.2\ \mu m$
   - **Long channel NMOS:** $W = 120\ \mu m,\ L = 20\ \mu m$

   (a) Plot I_{DS} vs. V_{DS} curves for short and long channel N-MOSFETs for a fixed W/L ratio with V_{GS} = 1.5 V and calculate the output impedance in saturation from the curve. Explain the reason behind the difference in the values for the two MOSFETs.

   (b) Plot I_{DS} vs. V_{GS} curves for the short and long channel FETs with V_{DS} =3 V in linear and log scales and determine the V_{TH} (from linear plot), on-current (from log plot the constant portion above V_{th}) sub-threshold slope (from log plot) and off-current (from log plot). What are the likely reason(s) for the difference in values of these parameters between the two transistors and their impact on performance (switching speed) and power consumption for the two?

(2 + 3 = 5 Marks)

4. (a) Design a CMOS inverter by choosing appropriate widths for n and p channel transistors such that it has equal rise and fall times of 250 ps each.The input should be a rail-to-rail square wave with rise and fall times of 20 ps. Measure the rise and fall times of the output by finding the time taken to traverse between 10% to 90% of V_{DD}. (Consider V_{DD}=3.3 V, Ln=Lp=0.4 μm and load capacitance=0.05 pF)

   (b) Plot the static transfer characteristics of this inverter by sweeping the input from 0 to V_{DD} and determine V_{OH}, V_{IL}, V_{OL}, V_{IH} and static noise margins N_{MH} and N_{ML}.

   (c) Plot the current in the CMOS inverter versus the input voltage and explain the nature of the plot.
   Model files: CMOS

(1 + 1 + 1 = 3 Marks)

Appendix

Command for temperature sweeping:
.dc vin 12 30 0.1 temp 20 80 10
Use the below template for instantiating n channel MOSFET:
MN1 drain gate source body NMOSFET L=0.4u W=Wn AS=(2*Wn*L) PS=(2*Wn+4*L) AD=(2*Wn*L) PD=(2*Wn+4*L)

Command for measuring delay, rise and fall time:
.measure tran rise trig v(out) val=0.33 rise=1 targ v(out) val=2.97 rise=1
.measure tran delay trig v(a) val=1.665 rise=2 targ v(out) val=1.665 fall=2
.measure tran fall trig v(out) val=2.97 fall=1 targ v(out) val=0.33 fall=1