Indian Institute of Technology, Bombay
Department of Electrical Engineering
Electronic Devices Lab(EE-236)
Quiz 2, Date: March 23rd, 2022

Timing: 2:00 PM to 2:50 PM | Spring 2022 | Max marks: 5

Instructions

- You are allowed to use only those models that have been provided. You can download by clicking the name.
- Read the questions thoroughly.
- You can use previous lab reports and netlist.

Part-1

1. We want to build a good analog switch i.e. $V_{out} = V_{in}$, on resistance $(R_{ON}) = |V_{DS}/I_{DS}| = 0\ \Omega$ for all V_{in} when control input is enabled. Consider VDD = 3.3 V
   - Write ngspice netlist for below PMOS pass gate having W/L= 4 μm/0.4 μm. Plot and comment on V_{out} vs V_{in}, R_{ON} vs V_{in}.
   - Similary, write ngspice netlist for below NMOS pass gate having W/L= 4 μm/0.4 μm. Plot and comment on V_{out} vs V_{in}, R_{ON} vs V_{in}. Which MOSFET has higher R_{ON} and explain the reason?

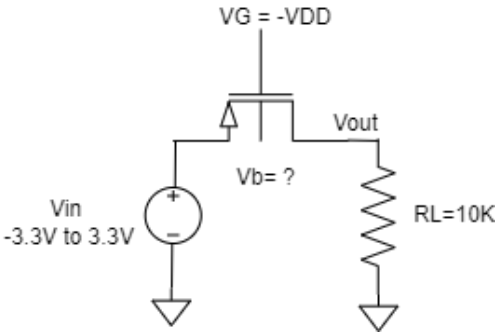

Figure 1: PMOS transistor switch

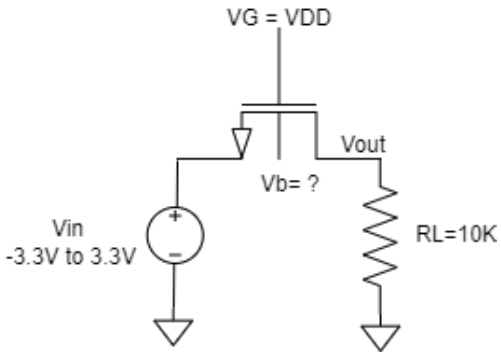

Figure 2: NMOS transistor switch

   - Write ngspice netlist for below transmission gate circuit with each MOSFET having W/L= 4 μm/0.4 μm, plot V_{out} vs V_{in}, R_{ON} vs V_{in}. Explain the reason for small peak in R_{ON} plot and mention the maximum value of R_{ON}. Change device parameters such that on-resistance on either side of the small peak is the same. Show both the plots of R_{ON} vs Vin before and after changing device parameters.
     Note: Ignore the peak value of R_{ON} at V_{in} near 0 V for PMOS, NMOS, transmission gate plots

(1 +1 + 3 Marks)

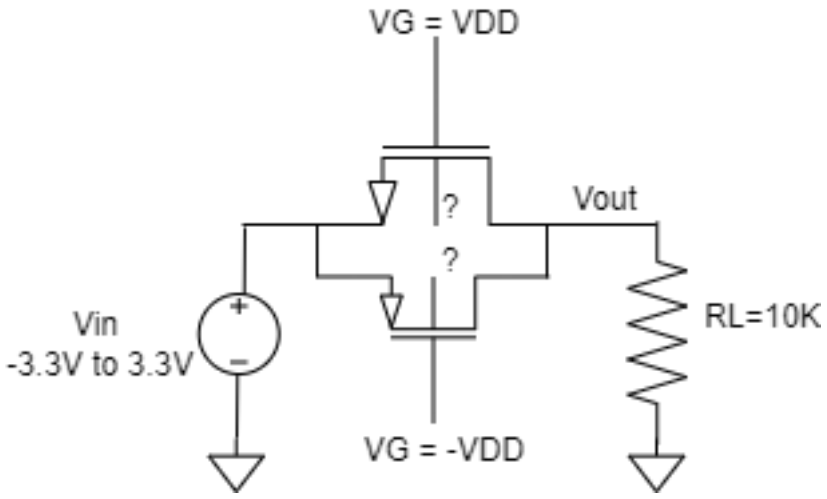

Figure 3: Transmission Gate Circuit

Note: For both part -1&2 questions use PMOS_NMOS model file, the same as you have used for CMOS inverter experiment in last lab (Click on the name)