C–V profiling of solar cells

August 29, 2018

Apart from basic I–V characteristics of a p-n junction, C–V measurement is also important in applications such as switches, where the capacitance sets the bandwidth limitation of a device. The capacitance of a p-n junction is dominated by different physical mechanisms depending on the bias voltage: (a) junction capacitance in depletion region (dominant in reverse bias), and (b) diffusion capacitance (dominant in forward bias).

This C–V measurement experiment describes a simple setup to study how the junction capacitance varies with applied reverse bias and to estimate the doping density and built-in potential. In commercially available diodes, the junction capacitance is designed to be as low as possible to enable fast switching operation. This poses problems in the measurement of capacitance of such devices in the laboratory using educational-grade measurement equipment. To overcome this limitation, we use a solar cell, which is essentially a large-area p-n junction diode, that thereby has larger and hence measurable capacitance.

1 Voltage dependence of p-n junction capacitance

When a p-n junction is reverse biased, uncompensated acceptor ions in the p-side of the junction and an equal number of ionized donors on the n-side of junction form the space charge region. Since there are no mobile carriers in this region, only the free carriers at the edge of the depletion region can respond to externally applied ac field. The junction thus resembles a parallel

plate capacitor, whose capacitance is specified as:

$$C = \left| \frac{dQ}{dV_{dc}} \right| = \frac{\epsilon_0 \epsilon_s A}{x_d} \tag{1}$$

where Q is the charge (free charge carriers) on either side of the junction, V_{dc} is the applied voltage, ϵ_s is the dielectric constant of the semiconductor, ϵ_0 is the permittivity of free space, and A is the area of the p-n junction. The depletion region width, x_d, for a reverse biased junction with constant doping density N_d is given by,

$$x_d = \left[\frac{2\epsilon_0 \epsilon_s (V_{bi} + V_{dc})}{qN_d} \right]^{\frac{1}{2}} \tag{2}$$

V_{bi} is the built-in voltage, q is the charge on an electron (1.6×10^{-19} C), and N_d is the doping density. From Eqs. 1 and 2 it follows that,

$$\frac{1}{C^2} = \left[\frac{x_d}{\epsilon_o \epsilon_s A} \right]^2 = \left[\frac{2(V_{bi} + V_{dc})}{q\epsilon_o \epsilon_s A^2 N_d} \right] \tag{3}$$

A plot of $1/C^2$ v/s V_{dc} is a straight line with slope $d(1/C^2)/dV = 2/(q\epsilon_o \epsilon_s A^2 N_d)$. By obtaining this plot, students can easily find doping density N_d from the slope. The built-in potential V_{bi} can be estimated from either the x-axis intercept ($= -V_{bi}$) or the y-axis intercept $\left(= \frac{2V_{bi}}{q\epsilon_o \epsilon_s A^2 N_d} \right)$. A detailed treatment of C–V profile of a p-n junction is available in semiconductor device textbooks.

2 Capacitance measurement circuit

The primary considerations for the circuit to be used for this experiment are:

- Should be easily implementable on a breadboard and use standard measuring instruments like digital storage oscilloscope (DSO) and function generator to make it cost effective.
- Should not require expensive components or equipment (such as a semiconductor device parameter analyzer and precision LCR meter)

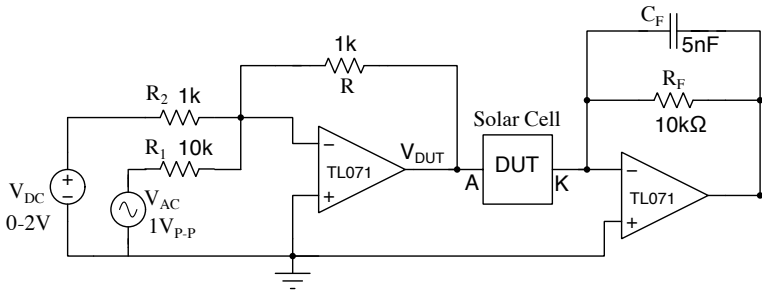

Figure 1: Schematic of the circuit used to apply reverse bias, and extract the capacitance of the device under test (DUT) by measuring small signal ac gain.

- Should use circuit blocks familiar to second-year undergraduate students to understand the principles behind the measurement and analysis.

Since the experiment involves measurement of the C–V profile of the capacitor, the circuit must also be designed to apply an additional dc voltage across the capacitor that can be varied, while measuring the ac current to extract the capacitance. Figure 1 shows a schematic of the circuit used for our measurement. In our setup, we apply a variable dc bias and a small ac signal (small enough not to perturb dc bias) to the DUT (Device Under Test). This is accomplished by using a basic inverting summing amplifier that adds the variable dc voltage (with unity gain = R/R_2) and the small signal ac voltage (with attenuation factor $1/10 = R/R_1$), the output voltage of which is then connected to the DUT. The voltage V_{DUT} in Fig. 1 is thus given by the following equation:

$$V_{DUT} = -R\left(\frac{V_{DC}}{R_2} + \frac{V_{AC}}{R_1}\right) \tag{4}$$

The ac voltage amplitude across the DUT is thus one-tenth of the applied input dc voltage. To measure the capacitance, we utilize the fact that the current through a capacitor is proportional to the applied ac sinusoidal voltage. We use a transimpedance amplifier (I-to-V converter) so that the current flowing through the capacitor is converted into voltage, the ac component of which is measured using a DSO. The transimpedance amplifier generates a voltage output that is proportional to the DUT capacitance C_{DUT} and V_{DUT}. The magnitude of this voltage is given by following equation:

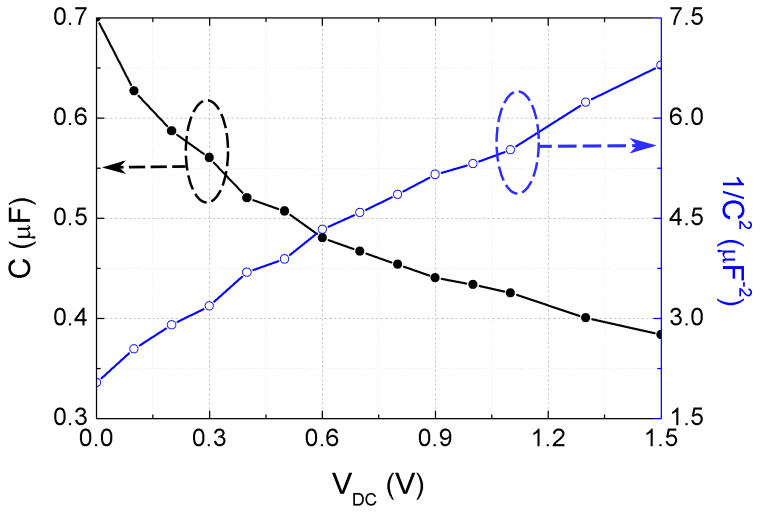

Figure 2: C–V profiling and variation of $1/C^2$ with applied dc voltage for a solar cell

$$V_{out} = V_{DUT}\frac{C_{DUT}}{C_F}\frac{1}{\sqrt{1+(\omega R_F C_F)^{-2}}} \tag{5}$$

By monitoring the amplitude of the ac component of V_{out} at the frequency of the small signal ac voltage applied to the input of the summing amplifier, C_{DUT} could be estimated.

3 Experiment and results

The circuit used to measure the C–V profile of a solar cell (area 4 cm $\times$ 4 cm) is shown in Fig. 1. The small signal ac voltage peak-peak amplitude is set to 1 V, which is further attenuated by a factor of 10. The dc bias is varied in steps from 0–1.5 V. The C–V profile and $1/C^2$ v/s V_{dc} plots obtained from measurements performed by a student from last year's class are shown in Fig. 2. From the slope of a linear least-squares fit to the $1/C^2$ vs. V_{dc} plot, the doping density is estimated to be $N_d = 2\times10^{16}\,\mathrm{cm}^{-3}$ and from the y-axis intercept, the built-in voltage is estimated to be $V_{bi} = 0.75\,\mathrm{V}$.

The characteristics of a solar cell depend on the illumination, so care must be taken to ensure controlled experimental conditions. In our experiment,

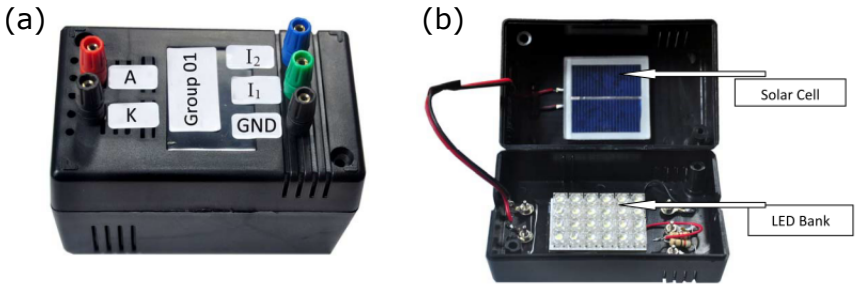

Figure 3: (a) 'Black box' package used for solar cell measurement, (b) inner view, showing LED bank and 4 cm $\times$ 4 cm solar cell

we encase the solar cell (area 4 cm $\times$ 4 cm) in a black colored box, shown in Fig. 3. We have included provision for an LED bank and two resistors to set two different illumination levels (terminals I_1 and I_2), which are used in a separate experiment to study lighted I–V characteristics of a solar cell. For this C–V measurement experiment, we turn off the LED bank and measure the dark characteristics. In next week's lab (solar cell I–V), you will use this box to study lighted and dark characteristics.