

PMOS I/V Characteristics and Applications

Wadhwani Electronics Lab

EE 236 Electronics Devices Lab
Department of Electrical Engineering
Indian Institute of Technology Bombay

The Problem Statement

In this experiment, we will do the following:

- * Measure its output and transfer characteristics
- * Investigate the effect of body bias on the characteristics of a PMOS transistor

Background Information

- * The MOSFET is one of the most commonly used transistor.
- * It has four terminals- Gate (G), Drain (D), Source (S) and Body (B).
- * The device working principle is that the voltage applied between its gate and source terminal controls the current through the source and drain terminals.
- * The body terminal of a PMOS is connected to **the highest voltage** in the circuit i.e, V_{DD} while that of a NMOS is connected to **ground**
- * For the transistor to be ON, the applied gate to source voltage must be **less** than the threshold voltage i.e. $V_{GS} < V_T$. The conditions for different operating regions of a PMOS are

$$\begin{aligned} V_{GS} - V_T &< V_{DS} && \text{(Linear Region)} \\ V_{GS} - V_T &> V_{DS} && \text{(Saturation Region)} \end{aligned} \tag{1}$$

Background Information (cont'd...)

Some information and conventions which we use:

- * The threshold voltage V_{TP} of an PMOS is negative, while that of a NMOS, V_{TN} is positive.
- * The parameter k in current eq. is as k_p and k_n for PMOS and NMOS respectively, and is given as

$$k = \mu C_{ox} \left(\frac{W}{L} \right) \quad (2)$$

Where;

μ - mobility of charge carriers (electrons/holes) in the channel of the MOSFET.

C_{ox} - per unit area capacitance between the gate and body.

W, L - width and length of the channel respectively.

Part 1- I_D - V_{DS} Characteristics

1. Write ngspice netlist to plot the I_D - V_{DS} characteristics of PMOS with the voltage V_{GS} varied from -2.5 V to -4 V in steps of -0.5 V. You may vary V_{DS} from 0 V to -5 V.(show all 4 curves on a single plot)
2. From these characteristics, obtain r_{DS} (linear region) for each value of V_{GS} . Also, find "Early voltage" and r_0 in saturation region(considering channel length modulation).

Part 2- I_D - V_{GS} Characteristics in different regions

1. Estimate the value of threshold voltage and transconductance g_m in **linear region**:
 - Bias the transistor in linear region by keeping $V_{DS} = -200$ mV
 - Now write ngspice netlist to plot I_D v/s V_{GS} characteristics by varying V_{GS} from -5 to 0 V
 - From this characteristic, obtain V_T and g_m
2. Estimate the value of threshold voltage and transconductance g_m in **saturation region**:
 - Bias the transistor in saturation region by keeping $V_{DS} = -5$ V
 - Now write ngspice netlist to plot I_D v/s V_{GS} characteristics by varying V_{GS} from -5 to 0 V
 - From this characteristic, obtain V_T and g_m
 - Also, plot $\sqrt{I_D}$ v/s V_{GS} to find parameter K(mention its unit)

Part 3- Effect of Body Bias

1. Bias the transistor in linear region by keeping $V_{DS} = -200$ mV.
2. Now write ngspice netlist to plot I_D v/s V_{GS} characteristics by varying V_{GS} from -5 to 0 V for $V_{SB} = 0$ V. (which is already asked in part 2)
3. Repeat the above step to get four more sets of I_D v/s V_{GS} characteristics for $V_{SB} = -1, -2, -3, \text{ and } -4$ V.
4. Show all five I_D v/s V_{GS} characteristics on the same plot
5. Obtain the value of threshold voltage from each plot
6. Plot V_T v/s V_{SB} and Obtain body effect coefficient (γ) using below equation. comment on dependence of V_T on V_{SB} .

$$V_T = V_{T0} + \gamma(\sqrt{\phi_s + V_{BS}} - \sqrt{\phi_s})$$

where ϕ_s is Surface Potential = 0.8 V for ALD1107 PMOS model,
Threshold voltage (V_T) = V_{T0} when $V_{BS} = 0$ V