Programming the BASYS3 Board's Non-Volatile Flash Memory through Vivado

Introduction

When the BASYS3 board ships it comes with a diagnostic program stored in its SPI Flash memory. Once the board is turned on, by for example powering it through its USB port, this program is loaded into the FPGA. The BASYS3's HEX display lights up with flashing numbers and the LEDs turn on when the corresponding switches are turned on.

The BASYS3 boards can then be programmed through bitstream files generated by Xilinx's Vivado from either an HDL language, such as Verilog or VHDL, or from a Block Design. Vivado's built in Hardware Manager provides the means to program the boards through its USB-JTAG circuitry.

By default, the bitstream is sent through the USB cable to the (volatile) SRAM-based memory cells within the FPGA where it remains until a) it is overwritten by a new bitstream, b) the board is reset, or, c) turned off. In cases b) and c), the board will revert to the bitstream stored in its SPI Flash memory.

However, it is possible to change the default settings to program the non-volatile SPI Flash memory using Vivado's Hardware manager. In that case, when the board is powered up (or reset) it will always start with the last bitstream stored in its Flash memory. This extremely useful function can be used to build and customize standalone applications on the BASYS3 boards which will start on power up without the aid of a PC.

The instructions provided below explain how to program the non-volatile SPI Flash memory on the BASYS3 board with Vivado's Version 2017.2 Hardware manager. However, keep in mind that programming the SPI Flash memory will erase and overwrite its previously stored bitstream and this data can never be recovered from the FPGA.

In the steps below, we assume that you have already generated, tested and debugged the bitstream file through Vivado's and BASYS3's default setup, using its USB-JTAG interface.

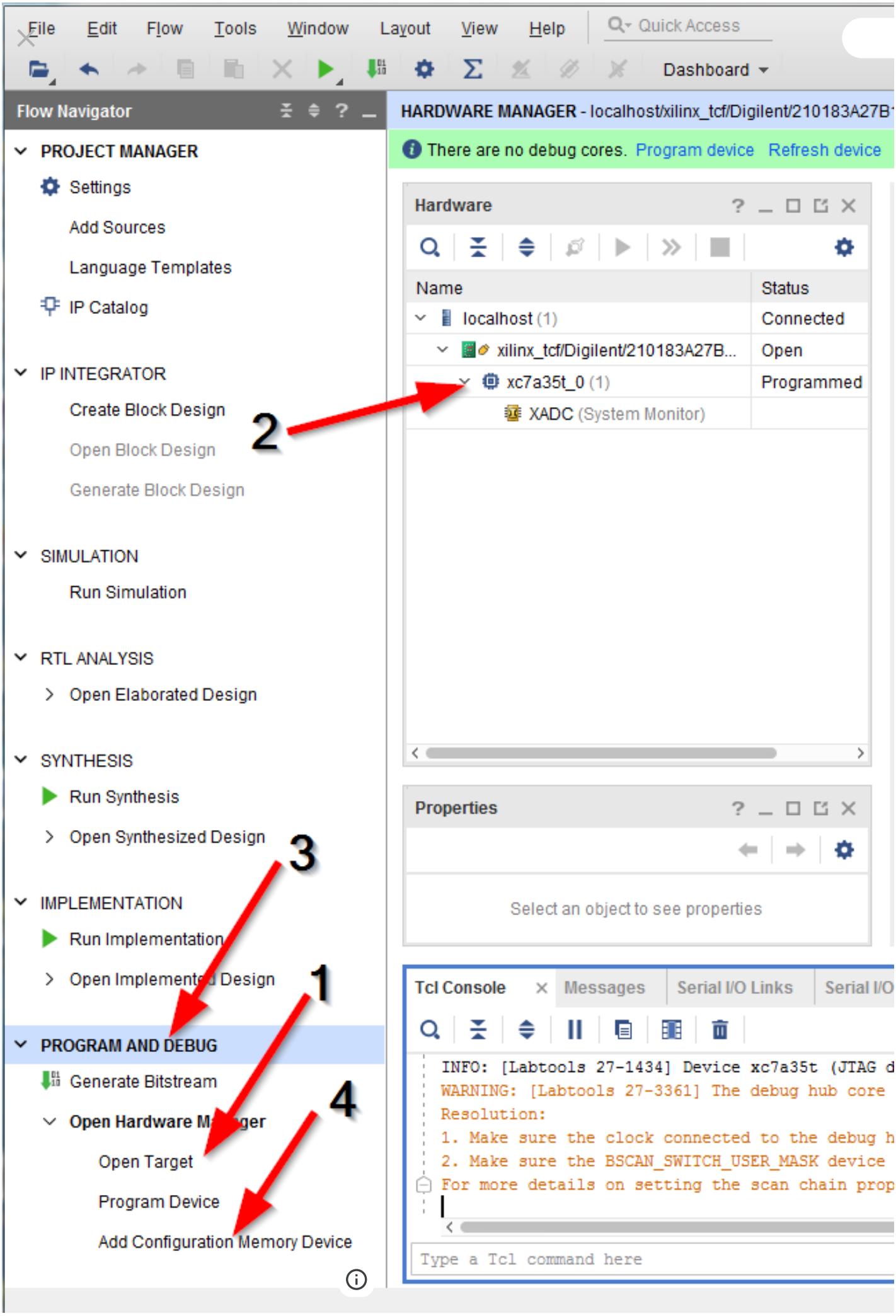
Hardware Setup for Programming the Non-Volatile QSPI Flash

Connect your BASYS3 board to the computer with a USB cable through the Micro-AB USB Connector, (J4.)

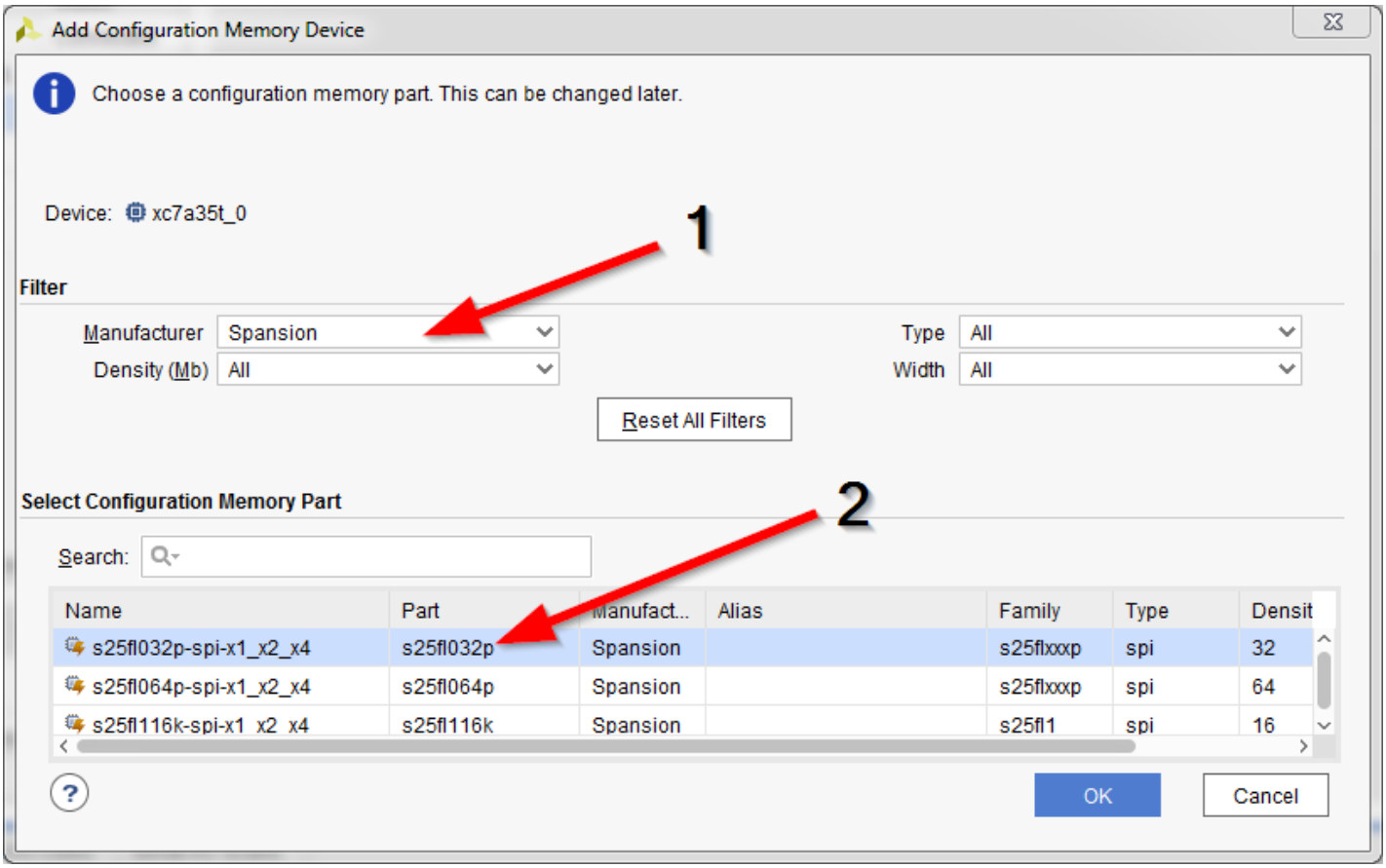
When you are ready to program the BASYS3 SPI Flash, move the blue Programming Mode jumper, JP1, to the SPI Flash mode, QSPI. (It is located in the upper right corner of the BASYS3 board, next to the red RESET button. Its default setting is the JTAG mode where it covers the two middle pins.) In the SPI Flash mode, the blue jumper covers and connects the two uppermost pins of JP1.

Vivado 2017.2 Setup for Programming the Non-Volatile QSPI Flash

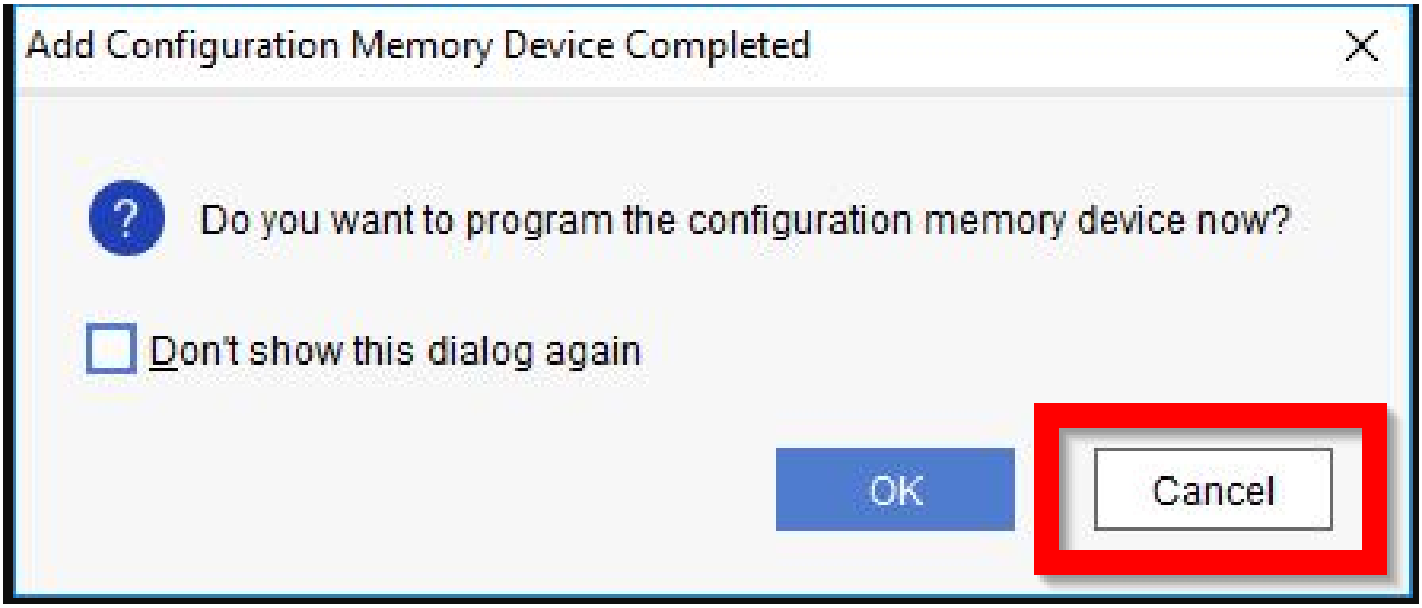
Under "PROGRAM AND DEBUG / Open Hardware Manager / Open Target" (1) click on "Auto Connect" and after a few seconds you should see the BASYS3 board's FPGA xc7a35t_0 in the Hardware Manager as shown in (2) in the screenshot below.


File
Edit
Flow
Tools
Window
Layout
View
Help
Quick Access
Dashboard
Flow Navigator
PROJECT MANAGER
Settings
Add Sources
Language Templates
IP Catalog
IP INTEGRATOR
Create Block Design
Open Block Design
Generate Block Design
SIMULATION
Run Simulation
RTL ANALYSIS
Open Elaborated Design
SYNTHESIS
Run Synthesis
Open Synthesized Design
IMPLEMENTATION
Run Implementation
Open Implemented Design
PROGRAM AND DEBUG
Generate Bitstream
Open Hardware Manager
Open Target
Program Device
Add Configuration Memory Device
HARDWARE MANAGER - localhost/xilinx_tcf/Digilent/210183A27B
There are no debug cores. Program device Refresh device
Hardware
Name
Status
localhost (1)
Connected
xilinx_tcf/Digilent/210183A27B...
Open
xc7a35t_0 (1)
Programmed
XADC (System Monitor)
Properties
Select an object to see properties
Tcl Console
Messages
Serial I/O Links
INFO: [Labtools 27-1434] Device xc7a35t (JTAG d
WARNING: [Labtools 27-3361] The debug hub core
Resolution:
1. Make sure the clock connected to the debug h
2. Make sure the BSCAN_SWITCH_USER_MASK device
For more details on setting the scan chain prop
Type a Tcl command here
1
2
3
4

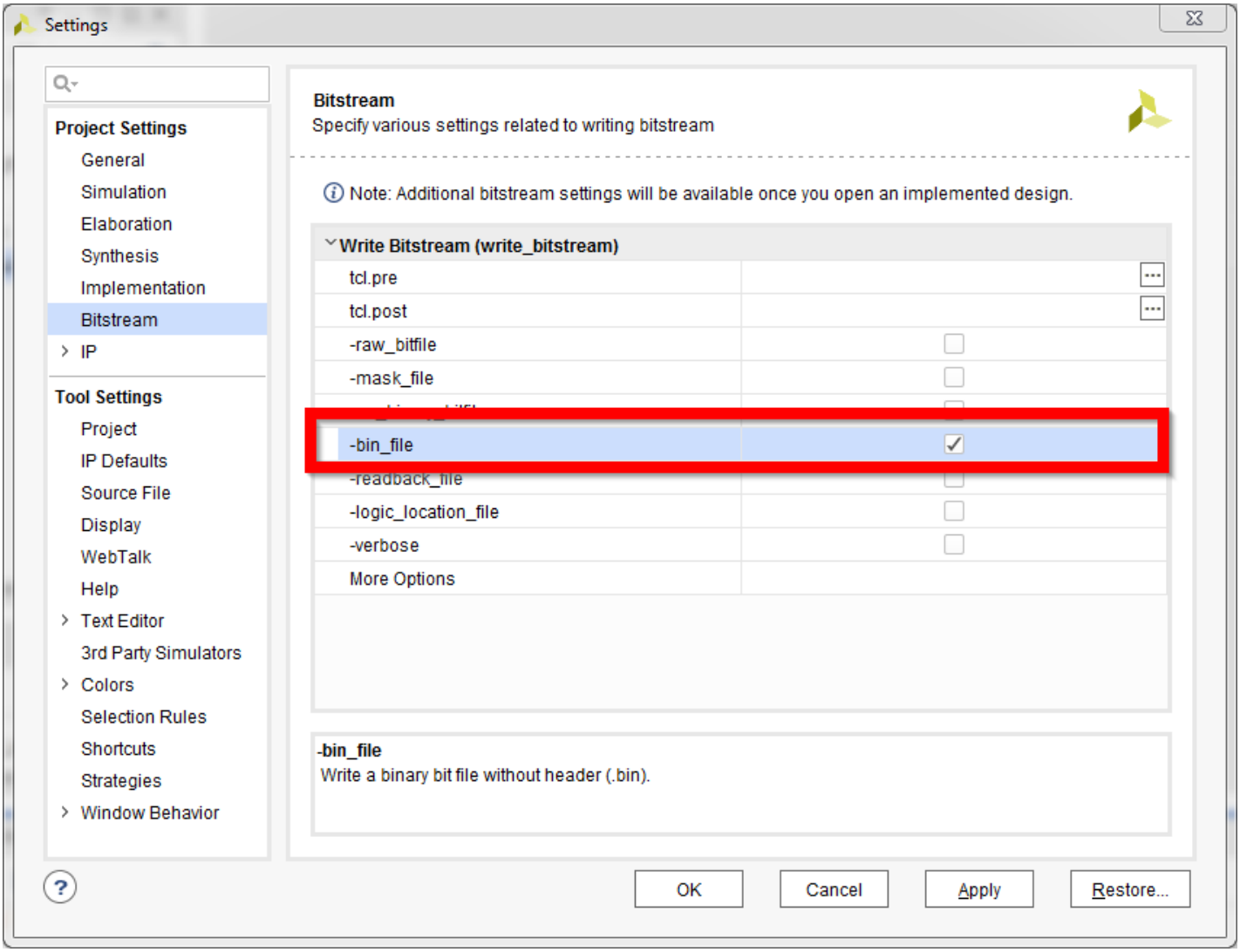
Now add the Configuration Memory Device by clicking on (4) in the screenshot above, under "PROGRAM AND DEBUG / Open Hardware Manager / Add Configuration Memory" and on the "xc7a35t_0" prompt which appears; the window shown below opens. From the Manufacturer (1) select "Spansion" and then select the "s25fl032p" Part as shown in (2) below. Hit OK.

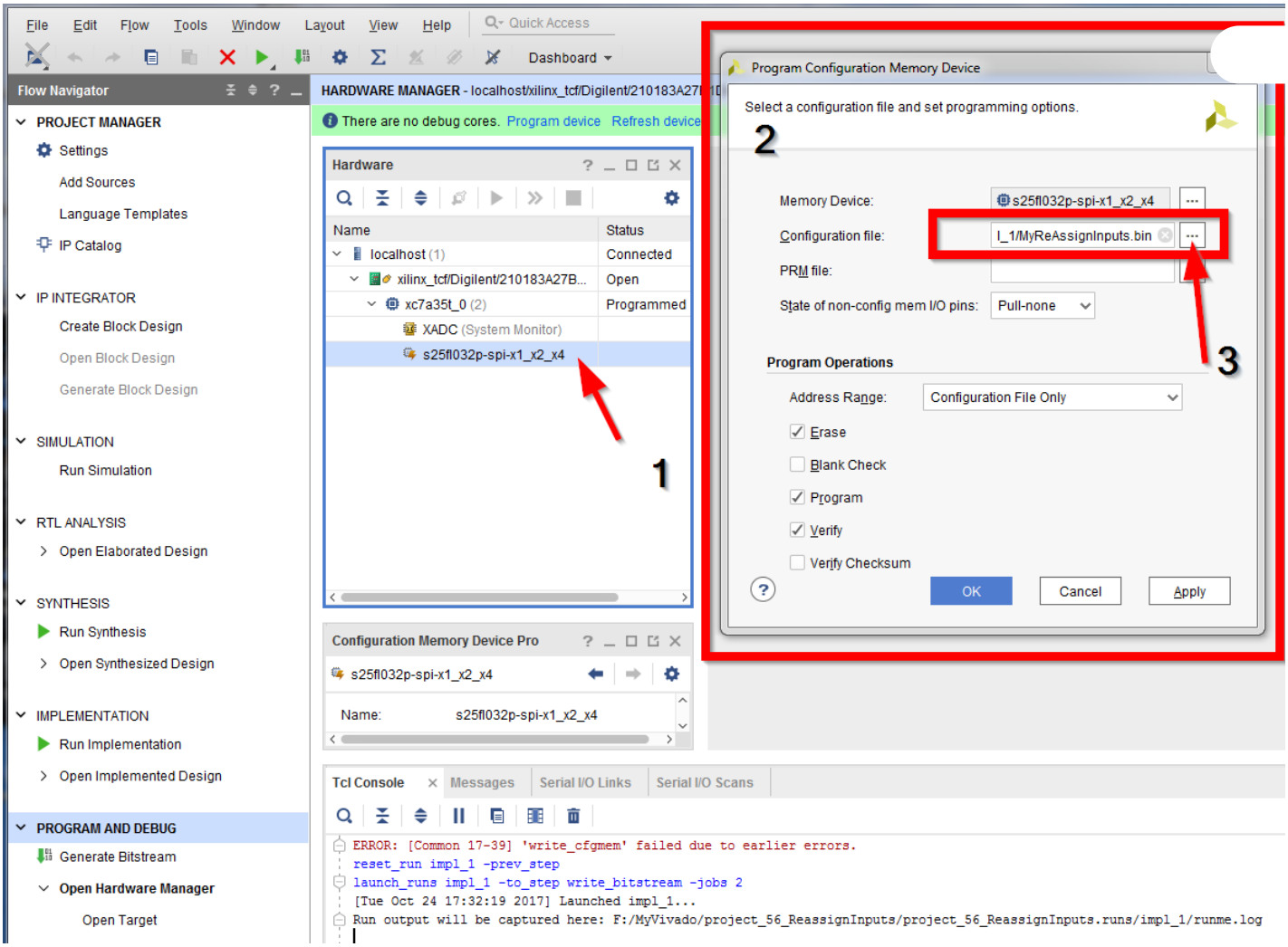


When the text box below opens and asks you to program the configuration memory, select CANCEL.



Right click on "PROGRAM AND DEBUG" (3 in the first screen shot) and select the "Bitstream Settings...". The screen below opens:





Activate the check mark by the "-bin_file" and click on "OK." You have to re-run "PROGRAM AND DEBUG / Generate Bitstream" again.

Under "Hardware," right click on the s25fl032p-spi-x1_x2_x4 configuration memory and select "Program Configuration Memory Device" as shown in (1) below. A new window, shown on the right (2) opens. Add the .bin Configuration file (3) which can be found in the "xxx.runs / impl_1 " folder of your project. ('"xxx" stands for the name of your project.").

Hit "OK" and Vivado will start programming the flash memory. This process will take a few seconds since the flash memory must first be erased.

Press the reset button and wait about 10 seconds for your new program to load from the BASYS3 flash memory into the FPGA.

Restoring the Default Non-Volatile Program

The BASYS3 board comes with a default Non-Volatile program that highlights the Input and Output capabilities of the board. If you want to restore that program, use the .bin and .bit files attached to this page. If you want to view the Verilog code, follow this link to download the code: https://reference.digilentinc.com/learn/programmable-logic/tutorials/basys-3-general-io/start. Once there, follow their instructions f ⓘ ownloading demo projects from Github.

TITLE	LAST MODIFIED
GPIO_demo.bin	11/29/21 Kevin Booth
GPIO_demo.bit	11/29/21 Kevin Booth