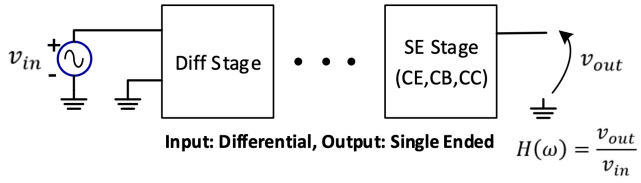
Analog Electronic Circuits Project

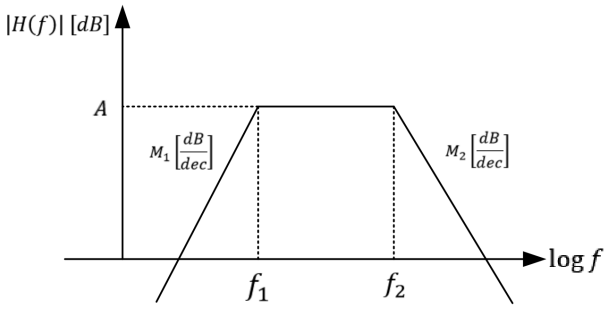
January 2023

	A	B	C	D	E	F	G	H	I
	9	3	2	0	5	6	7	2	4
	9	0	1	7	2	6	5	3	9
1	8	3	3	7	8	3	2	6	3

1 Circuit parameters

We have A and D one is even and the other is odd and thus the following circuit: After substituting the values





of variables, we have

$$\begin{array}{lll} A = 63[dB] & f_1 = 8[kHz] & f_2 = 800[kHz] \\ M_1 = 20[\frac{dB}{dec}] & M_2 = -40[\frac{dB}{dec}] & R_{out} = 103[k\Omega] \\ R_{in} = 103[k\Omega] & & \end{array} \quad (1)$$

All the transistors used had built-in capacitance zero, and $|V_A| \to \infty$, given $r_0 \to \infty$ for all of them.

2 Design process

2.1 Thought Process while designing

This is a general description of how we designed the amplifier. Exact calculations can be found in later parts.

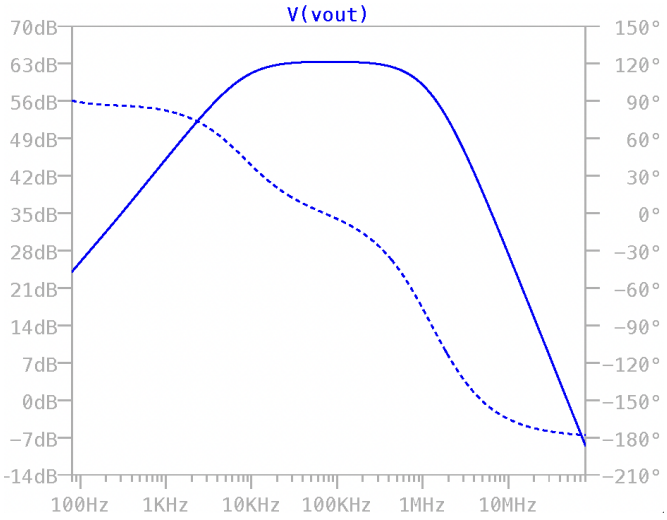


Figure 1: Frequency Response

2.1.1 Step 1

We started with designing the differential stage. We tried to have symmetry with R_{C_1} and R_{C_2}. Then we looked to get the R_{in} we wanted. We set the R_{in} using r_π of the capacitor as per the equations described in detail later. r_π was dependent upon $I_{c_{1,2}}$ and thus on R_r. Thus, we used the equation 16, and relation $r_\pi = \frac{\beta}{g_m}$ to get $g_m \to I_c \to I_{R_R} \to R_R = \frac{5-(-4.3)}{2\times I_{C_1}}$. The required value comes out to be $93[k\Omega]$. Then, we started to manipulate the value of R_{C_1} and R_{C_2} such that we had collector voltage of Q_1 and Q_2 is 0.

2.1.2 Step 2

Once we had our differential stage, we started by adding a single-ended stage. For each stage, we made sure that $\frac{R_{C_i}}{R_{e_i}}$ was $1.2:1$ and that we get $0[V]$ at the base of the next BJT(to reduce free variables and make calculations easier). Then, we calculated the required gain at each stage. At a stage, we would simulate the circuit to cross-check. In case, we realised that this is not enough for the gain we want, we would add another stage and repeat the process. It can be seen the highest gain for stages were obtained for R_c resistances $205.6[k\Omega], 169.62[k\Omega], 30.396[k\Omega]$ as seen in Fig(2).

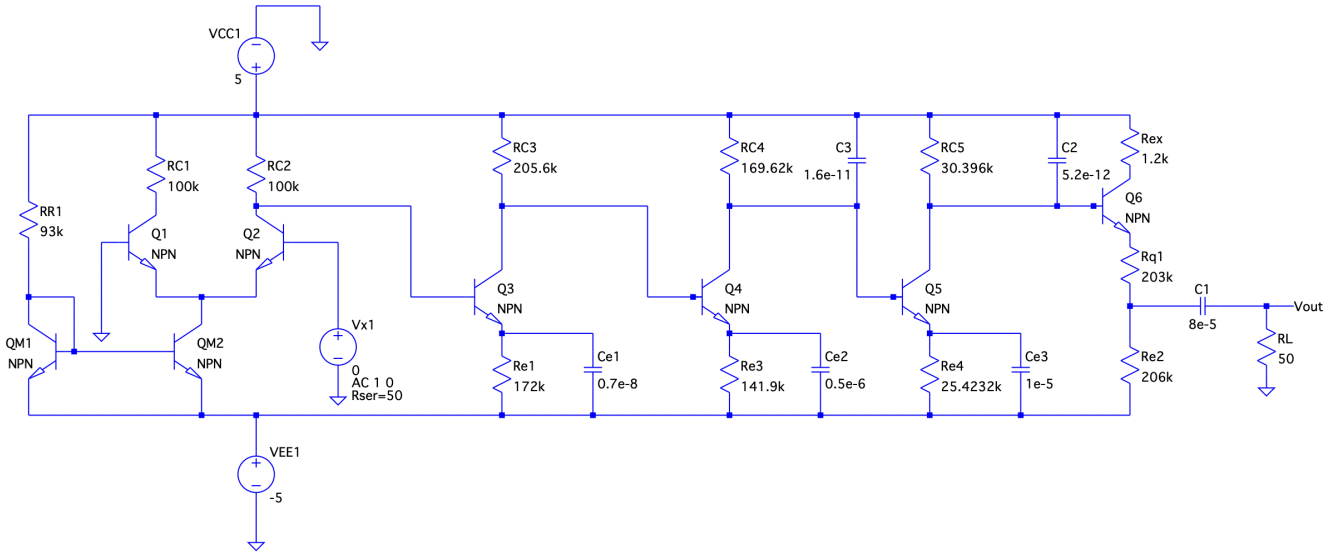


Figure 2: Full Circuit

2.1.3 Step 3

We then realized that we needed a common collector stage at the load so that the low R_L does not kill our gain.

2.1.4 Step 4

However, the amplification of the final stage is not high and our differential output was not capable of producing the full gain within the constraints. Thus, we had to add more stages.

2.1.5 Step 5

The R_{out} had an influence of $r_{\pi_{ce}}$ as can be seen in equations described later, which was in parallel with R_{e_2} (these two can be seen in our final circuit). $r_{\pi_{ce}}$ could not be made high enough under the given constraints to get the needed R_{out}. Thus, we had to add a series resistance R_{q_1} as in the final circuit. However, this had an impact on our gain, and thus we needed another common collector stage.[1]

2.1.6 Step 6

After that, we started to add capacitors that would contribute high and low poles at places easy to calculate. We choose positions where it is simple to calculate R_{net} using the test source method, of course ensuring positions of the capacitor contributed in the frequency range we wanted them to. After calculating the values, they were tested in the simulations and were altered by tiny amounts in order to get exactly $-3[dB]$ at the poles.[2]

[1] In Fig(2), the function of the R_{ex} is only for the good result of OP analysis. We got $r_{o_6} = 0$ in the OP analysis instead of infinity. It also helped us reduce excess gain and hence more accurate result

[2] If the pole was at a higher frequency, we increased the value of C slightly and vv.

2.2 Final Circuit

The circuit is as described in Fig(2) and the frequency response is as follows in Fig(1)

3 Large Signal Analysis

The values of resistances were chosen such that the BJTs will be in forward active mode. We will calculate the bias points for every BJT.

3.1 Q_{M_1}

In DC analysis we have $V_{E_{Q_1}} = -5$, and a node connection of collector and base, so $V_{B_{Q_1}} = V_{C_{Q_1}} = -4.3$, because we assumed the BJT is in the forward active, there has to be a -0.7 voltage drop between base and emitter. So we get the current of $I_{CE_{QM_1}} = \frac{5-(-4.3)}{93k} = 0.1[mA]$ then we obtain

$$\begin{cases} I_{C_{M_1}} = 0.1[mA] \\ V_{B_{M_1}} = -4.3[V] \\ V_{C_{M_1}} = -4.3[V] \\ V_{E_{M_1}} = -5[V] \end{cases} \tag{2}$$

This gives us the following small signal parameters

$$\begin{cases} g_{m_{M_1}} = 4[\frac{mA}{V}] \\ r_{\pi_{M_1}} = 25[k\Omega] \end{cases} \tag{3}$$

3.2 Q_{M_2}

The Q_{M_1} is the current mirror of Q_{M_2}, so we have the same bias current $I_{Q_{M_1}} = I_{Q_{M_2}} = 0.1[mA]$. And the $V_{B_{M_2}} = V_{B_{M_1}}[V] = -4.3[V], V_{E_{M_2}} = -5[V]$, plus because of the $V_{B_1} = 0[V]$, with the -0.7 voltage drop, we obtain the $V_{C_{M_2}} = -0.7[V]$. As a result, we obtain the following.

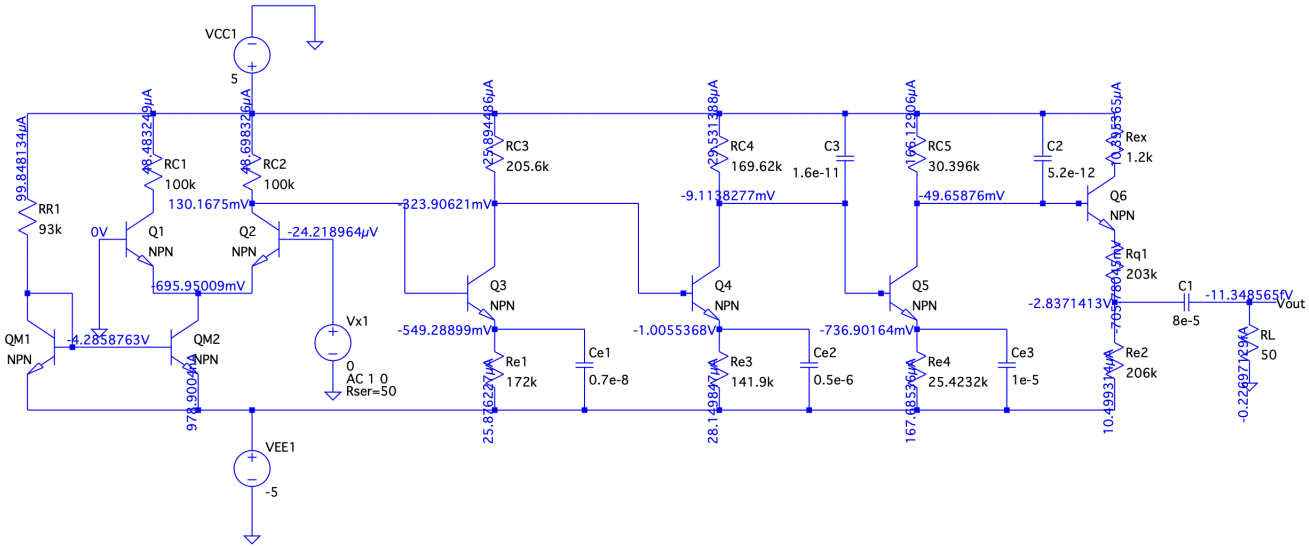


Figure 3: Voltage and Currents

$$\begin{cases} I_{C_{M_2}} = 0.1[mA] \\ V_{B_{M_2}} = -4.3[V] \\ V_{C_{M_2}} = -0.7[V] \\ V_{E_{M_2}} = -5[V] \end{cases} \tag{4}$$

This gives us the following small signal parameters

$$\begin{cases} g_{m_M 2} = 4[\frac{mA}{V}] \\ r_{\pi_M 2} = 25[k\Omega] \end{cases} \tag{5}$$

3.3 Q_1 and Q_2

We discuss the differential pair together,$V_{B_1} = V_{B_2} = 0[V], V_{E_1} = V_{E_2} = -0.7[V]$, and because the $I_{Q_{M_2}} = 0.1[mA]$, by the symmetry we get $I_{Q_1} = I_{Q_2} = 0.05[mA]$, then we obtain $V_{C_1} = V_{C_2} = 5 - I_{Q_1} R_{C_1} = 0[V]$, then we obtain the following.

$$\begin{cases} I_{C_1} = I_{Q_2} = 0.05[mA] \\ V_{B_1} = V_{B_2} = 0[V] \\ V_{C_1} = V_{C_2} = 0[V] \\ V_{E_1} = V_{E_2} = -0.7[V] \end{cases} \tag{6}$$

This gives us the following small signal parameters

$$\begin{cases} g_{m_1} = g_{m_2} = 2[\frac{mA}{V}] \\ r_{\pi_1} = r_{\pi_2} = 50[k\Omega] \end{cases} \tag{7}$$

3.4 Q_3

We have $V_{B_{Q_3}} = V_{C_{Q_2}} = 0$. Then, we have a $0.7[V]$ drop across BC of Q_3, which gives us $V_{C_{Q_3}} = -0.7[V]$.
The current is $I_{Q_3} = \frac{-0.7-(-5)}{172k} = 0.025[mA]$. The same current flows from R_{C_3}. Then we calculate the voltage drop across R_{C_3} to get $V_{C_{Q_3}} = -0.14[V]$

$$\begin{cases} I_{C_3} = 0.025[mA] \\ V_{B_3} = 0[V] \\ V_{C_3} = -0.14[V] \\ V_{E_3} = -0.7[V] \end{cases} \tag{8}$$

This gives us the following small signal parameters

$$\begin{cases} g_{m_3} = 1[\frac{mA}{V}] \\ r_{\pi_3} = 100[k\Omega] \end{cases} \tag{9}$$

3.5 Q_4

We perform similar calculations for Q_4 and obtain

$$\begin{cases} I_{C_4} = 0.03[mA] \\ V_{B_4} = -0.14[V] \\ V_{C_4} = -0.84[V] \\ V_{E_4} = -0.0886[V] \end{cases} \tag{10}$$

This gives us the following small signal parameters

$$\begin{cases} g_{m_4} = 1.1728[\frac{mA}{V}] \\ r_{\pi_4} = 85.266[k\Omega] \end{cases} \tag{11}$$

3.6 Q_5

We perform similar calculations for Q_5 and obtain

$$\begin{cases} I_{C_5} = 0.17018[mA] \\ V_{B_5} = 0.026[V] \\ V_{C_5} = -0.05[V] \\ V_{E_5} = -0.6733[V] \end{cases} \tag{12}$$

This gives us the following small signal parameters

$$\begin{cases} g_{m_5} = 6.807[\frac{mA}{V}] \\ r_{\pi_5} = 14.69[k\Omega] \end{cases} \tag{13}$$

3.7 Q_6

We perform similar calculations for Q_6 and obtain

$$\begin{cases} I_{C_6} = 1.05 \times 10^{-2}[mA] \\ V_{B_6} = 0.05[V] \\ V_{C_6} = 5[V] \\ V_{E_6} = -0.7[V] \end{cases} \tag{14}$$

This gives us the following small signal parameters

$$\begin{cases} g_{m_6} = 0.403[\frac{mA}{V}] \\ r_{\pi_6} = 232.56[k\Omega] \end{cases} \tag{15}$$

Indeed, all the BJTs are in forward active mode ($V_{CE} > 0.2$). The DC output can be seen in Fig(4)

We verified all the above calculations and small signal

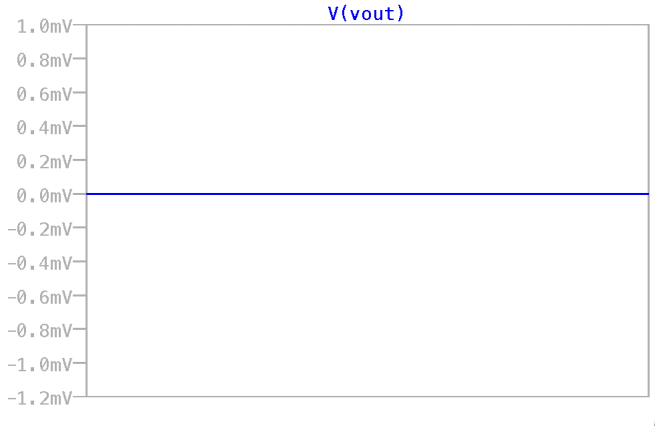


Figure 4: DC V_{out}

parameters in LTSpice as can be seen in Fig(5) and in Fig(3)

4 R_{in}

Before trying to set the gain, we set the required R_{in}. We add a test source at V_{in} and look into Q_2. We see the following resistance[3]

$$R_{in} = r_{\pi_1} + (\beta + 1)\frac{r_{\pi_2}}{1 + \beta} \tag{16}$$

We get $R_{in} \approx 103[k\Omega]$. The test can be seen in Fig(6). A test source of $1[V]$ was added and current across it was measured. Thus, in log scale, $R_{in}[dB] = -I[dB]$. We get values close to 100.24, which corresponds with the required R_{in}.

5 R_{out}

We now start to look at R_{out}. In the given circuit, we have

$$R_{out} = R_{e_2} || \left(R_{q_1} + \frac{r_{\pi_6} + R_{C_5}}{\beta + 1} \right) \tag{17}$$

We get $R_{out} \approx 103[k\Omega]$

[3]In all small signal, $V_A \to \infty$ and thus $r_o \to \infty$

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Semiconductor Device Operating Points:
                        --- Bipolar Transistors ---
Name:       q6          q5          q4          q2          qm1
Model:      npn         npn         npn         npn         npn
Ib:      1.04e-07    1.66e-06    2.79e-07    4.84e-07    9.79e-07
Ic:      1.04e-05    1.66e-04    2.79e-05    4.84e-05    9.79e-05
Vbe:     6.56e-01    7.28e-01    6.82e-01    6.96e-01    7.14e-01
Vbc:    -5.04e+00    4.05e-02   -3.15e-01   -1.30e-01    0.00e+00
Vce:     5.69e+00    6.87e-01    9.96e-01    8.26e-01    7.14e-01
BetaDC:  1.00e+02    1.00e+02    1.00e+02    1.00e+02    1.00e+02
Gm:      4.02e-04    6.42e-03    1.08e-03    1.87e-03    3.78e-03
Rpi:     2.49e+05    1.56e+04    9.28e+04    5.34e+04    2.64e+04
Rx:      0.00e+00    0.00e+00    0.00e+00    0.00e+00    0.00e+00
Ro:      9.80e+98    5.39e+13    4.99e+19    3.97e+16    2.59e+14
Cbe:     0.00e+00    0.00e+00    0.00e+00    0.00e+00    0.00e+00
Cbc:     0.00e+00    0.00e+00    0.00e+00    0.00e+00    0.00e+00
Cjs:     0.00e+00    0.00e+00    0.00e+00    0.00e+00    0.00e+00
BetaAC:  1.00e+02    1.00e+02    1.00e+02    1.00e+02    1.00e+02
Cbx:     0.00e+00    0.00e+00    0.00e+00    0.00e+00    0.00e+00
Ft:      0.00e+00    0.00e+00    0.00e+00    0.00e+00    0.00e+00

Name:       qm2         q3          q1
Model:      npn         npn         npn
Ib:      9.79e-07    2.60e-07    4.85e-07
Ic:      9.79e-05    2.56e-05    4.85e-05
Vbe:     7.14e-01    6.79e-01    6.96e-01
Vbc:    -3.59e+00    4.54e-01   -1.52e-01
Vce:     4.30e+00    2.25e-01    8.48e-01
BetaDC:  1.00e+02    9.84e+01    1.00e+02
Gm:      3.78e-03    9.91e-04    1.87e-03
Rpi:     2.64e+04    1.01e+05    5.33e+04
Rx:      0.00e+00    0.00e+00    0.00e+00
Ro:      4.90e+74    6.14e+06    9.11e+16
Cbe:     0.00e+00    0.00e+00    0.00e+00
Cbc:     0.00e+00    0.00e+00    0.00e+00
Cjs:     0.00e+00    0.00e+00    0.00e+00
BetaAC:  1.00e+02    1.00e+02    1.00e+02
Cbx:     0.00e+00    0.00e+00    0.00e+00
Ft:      0.00e+00    0.00e+00    0.00e+00
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Figure 5: Operating Point Analysis for Small Signal Parameters

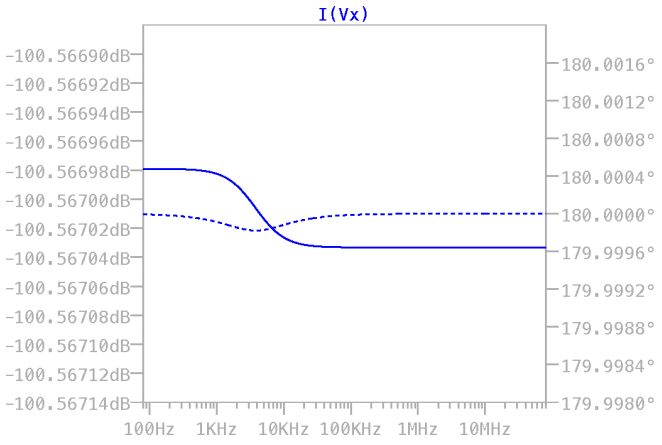

Figure 6: R_{in}

6 DC Power Consumption

To calculate the DC power consumption, we measured the current across V_{cc} and V_{ee} as can be seen in Fig(8). Then we just use $P = VI$ for both sources and obtain $P = 4.295 \times 10^{-3}[W] << 0.1[W]$

7 Gain

After setting R_{in} and R_{out}, we moved on to calculate the gain

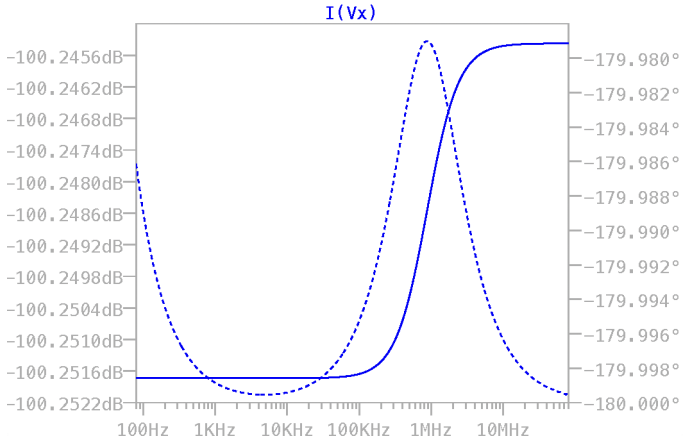

Figure 7: R_{out}

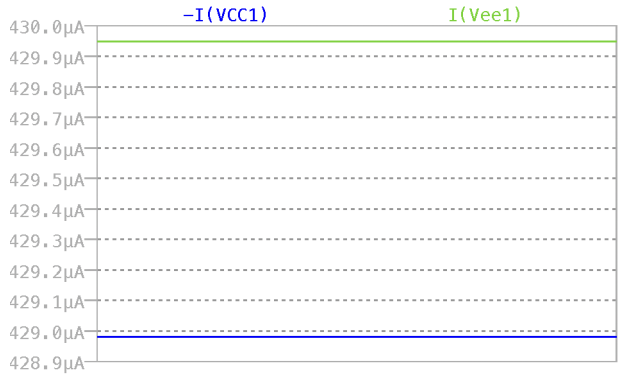

Figure 8: Current across V_{cc} and V_{ee}

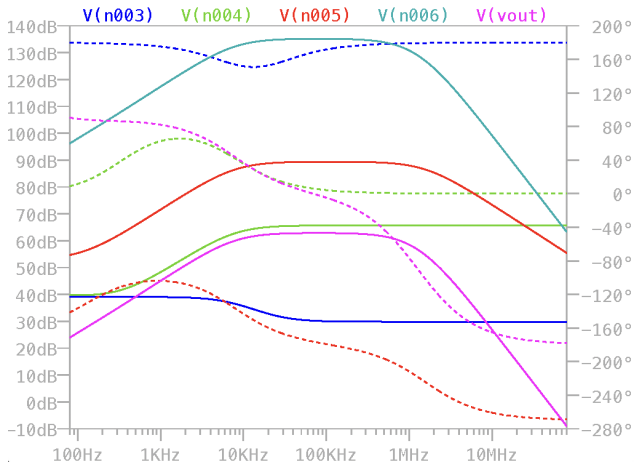

Figure 9: Gain at each stage in Final Circuit

7.1 Differential Gain

The differential gain is given by[4]

$$A_{diff} = \frac{1}{2} g_{m_2}(R_{C_2} || r_{\pi_3}) \approx 50(34[dB]) \tag{18}$$

[4]No Common Gain here (insignificant)

7.2 Common Emitter Stage Gain

The next three stages have the following gain

$$\begin{aligned} A_{cs_3} &= -g_{m_3}(R_{C_3} || r_{\pi_4}) \approx -60.27(35.3[dB]) \\ A_{cs_4} &= -g_{m_4}(R_{C_4} || r_{\pi_5}) \approx -15.84(23.3[dB]) \\ A_{cs_5} &= -g_{m_5}(R_{C_5} || (r_{\pi_6} + (1+\beta)R_{q_1} + R_{e_2} || R_L)) \\ &\approx -211(45.5[dB]) \end{aligned} \tag{19}$$

7.3 Common Collector Gain

$$A_{ce} = \frac{g_{m_6}(R_{q_1} + R_{e_2} || R_L)}{1 + g_{m_6}(R_{q_1} + R_{e_2} || R_L)} \frac{R_L || R_{e_2}}{(R_L || R_{e_2}) + R_{q_1}} \tag{20}$$

$\approx 2.4 \times 10^{-4}(-73.7[dB])$.
Thus, we get our total gain $A \approx 63[dB]$

8 Calculating Capacitor that contribute to ω_L

The only capacitor that is influencing the slope near $8[kHz]$ is C_{e_1}. C_{e_2} helps to nullify the effects of zeros near $8[Hz]$, and C_{e_3} only serves to remove degeneration. These capacitors were given bigger values so that they help us remove generation without affecting the frequency response in the interested intervals.

8.1 Calculating C_{e_1}

We replace C_{e_1} with a test source. The resistance seen by this test source is

$$R^{eff}_{C_{e_1}} = R_{e_1} || \left[\frac{r_{\pi_3} + R_{C_2}}{\beta + 1} \right] \tag{21}$$

Then, we have that $\omega = 2\pi(8[kHz]) = \frac{1}{R^{eff}_{C_{e_1}} C_{e_1}}$.
Solving for C_{e_1} gives us $C_{e_1} = 0.85 \times 10^{-8}[F]$

9 Calculating Capacitor that contribute to ω_H

We now look at the frequency-dependent elements

9.1 Calculating C_3

We replace C_3 by a test source. The resistance seen by this test source is

$$R^{eff}_{C_3} = r_{\pi_5} || R_{C_4} \tag{22}$$

Then, we have that $\omega = 2\pi(800[kHz]) = \frac{1}{R^{eff}_{C_3} C_3}$.
Solving for C_3 gives us $C_3 = 1.56 \times 10^{-11}[F]$

9.2 Calculating C_2

We replace C_2 with a test source. The resistance seen by this test source is

$$R_{C_2}^{eff} = R_{C_5}||[r_{\pi_6} + (\beta + 1)(R_{q_1} + R_L||R_{e_2})] \qquad (23)$$

Then, we have that $\omega = 2\pi(800[kHz]) = \dfrac{1}{R_{C_2}^{eff} C_2}$.
Solving for C_2 gives us $C_2 = 5.2 \times 10^{-12}[F]$ [5]

9.3 Bode Plot at $8[kHz]$ and $800[kHz]$

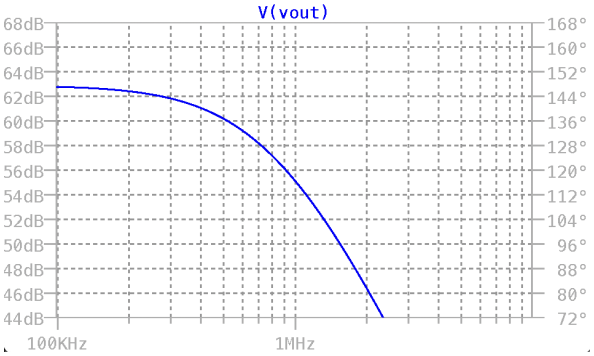

Figure 10: Plot around $800[kHz]$

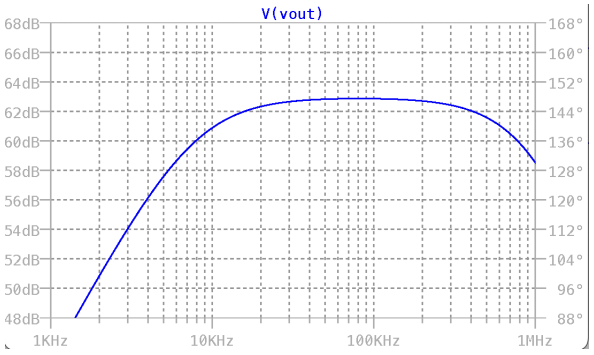

Figure 11: Plot around $8[kHz]$

We can easily see -3dB at f_L and -6dB at f_H drop as expected.

[5] The values of the capacitors were slightly altered in the final circuit in order to get more accurate results and solve the inaccuracy caused by rough calculations and assumptions