The Iby and Aladar Fleischman
Faculty of Engineering
Tel Aviv University

Designing Oscillator for an Antenna at $\sim$3.5 GHz

2896

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Edoh Shaulov

Tel Aviv University

Milestones completed so far

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- Created test schematic for oscillator using an ideal transistor
- Ran LTSpice Simulations for the ideal version
- Selected an RF transistor with a required performance at the interested frequency
- Ran PSpice Simulations for the same schematic but with non-ideal transistor
- Collected useful data like S-parameters, Z-parameters, Z_{in} and Z_{out} in order to build matching network
- Built matching network for Z_{out} and $Z_{load} = 50[\Omega]$ at $\sim 3.5[GHz]$
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Choosing the BJT

Reqired characteristics

- The transistor needs high-frequency performance, including f_{max} and f_t, well above $3.5[GHz]$.
- Low parasitic capacitance at collector, base, and emitter terminals is crucial.
- Low noise figure is essential.
- High gain, especially at the operating frequency, is necessary for stable oscillation.
- Ensure appropriate biasing for Colpitts oscillator operation, including DC voltages and currents.

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BFP520 from Infenion[1]

- Surface mount low voltage silicon NPN RF bipolar transistor
- Transition frequency f_T of $45[GHz]$
- High Gain, with $|S_{12}|, G_{ma}, G_{ms} > 16[dB]$ at $3.5[GHz]$ under $V_{ce} = 2[V]$
- Low Noise Figure, $NF < 1.2[dB]$ at $3.5[GHz], 2[V], 2[mA]$

[1] https://www.infineon.com/dgdl/Infineon-BFP520-DS-v02_00-EN.pdf?fileId=5546d462689a790c01690f035fe2391a

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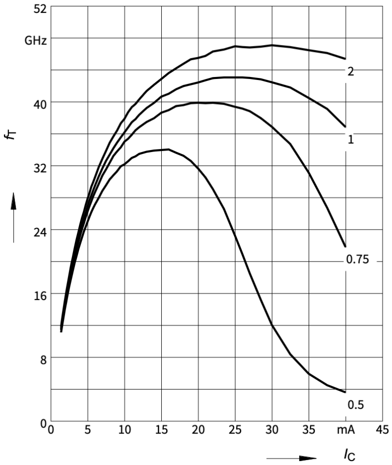
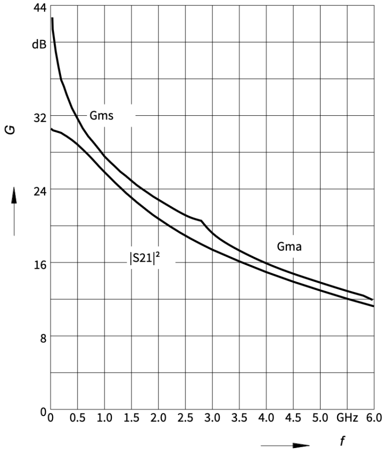
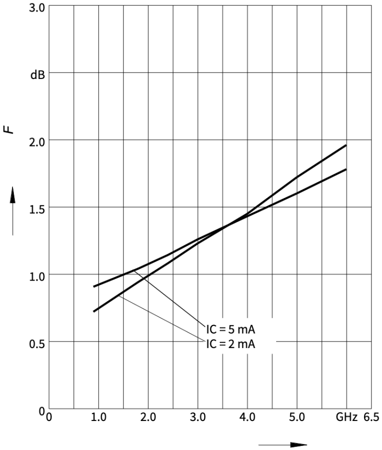
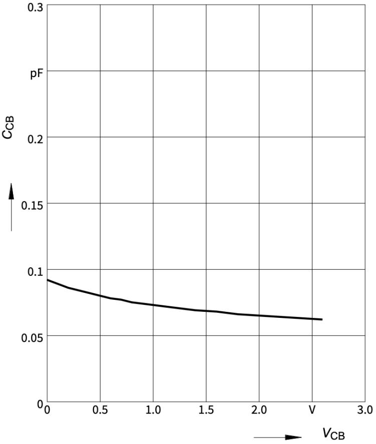
Data from Infenion - 1





Data from Infenion - 2





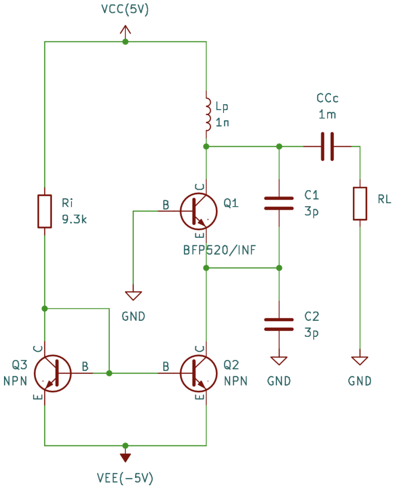
Oscillator Circuit

Collpit's Oscillator

- The circuit was tested with some high impedance load attached
- Values of L_p, C_1 and C_2 were computed using the operating frequency formula

$$f_c \approx \frac{1}{2\pi\sqrt{L_p \frac{C_1 C_2}{C_1 + C_2}}}$$

- $C_1 = C_2$ was chosen since it gave the highest oscillation frequency



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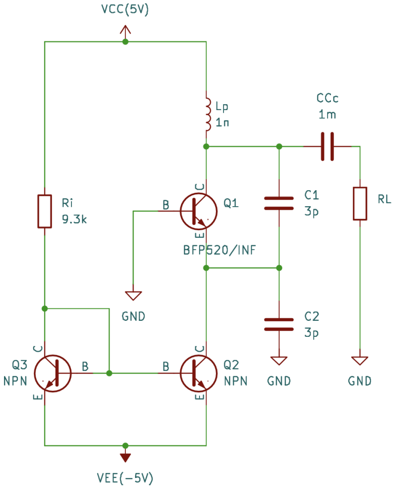

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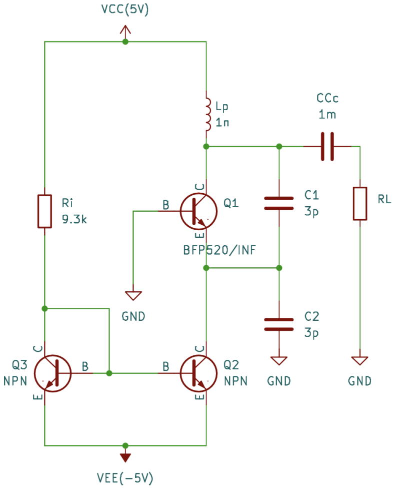

Ouput Waveform

Choosing a Matching Network

Why Matching Network

- The oscillator we have works for high R_L. Having low R_L, such as $50[\Omega]$ fails to satisfy $g_m R_L^{eff} >> 4$
- We need to design a matching network that converts $R_L = 50[\Omega]$ to the R_L we have in the schematic
- We used a T-Matching network. T-matching is better for matching a load to a source impedance when there's a large disparity because it provides efficient power transfer, minimizes losses, and offers impedance transformation with stability.

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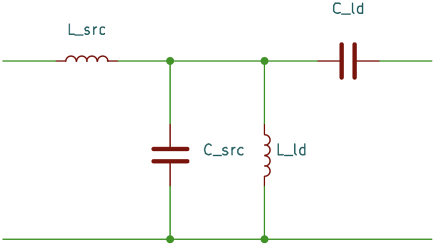
Matching Network

The following is the matching network used[2]

$$\begin{cases} L_{src} = \\ C_{src} = \\ L_{ld} = \\ C_{ld} = \end{cases}$$



[2] Design method in Appendix

S-parameters of the Matching Network

Tested with $R_S = 1000[\Omega]$ and $R_L = 50[\Omega]$

Ouput of Oscillator using Matching Network as $50[\Omega]$ load

Efficiency η

Defining η

- **Input:** $P_{DC} = V_{CC} I_C$
- **Output:** $P_{ac} = \frac{V_{rms}^2}{R_L}$ where $V_{rms} = \frac{V_{max}}{\sqrt{2}}$ for the output waveform
- **Efficiency:** $\eta = \frac{P_{ac}}{P_{CD}}$ [3]

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Calculation of η

Next Steps

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- Create an antenna at $3.5[GHz]$
- Measure S-parameters of the antenna and of the whole system
- Layout the PCB
- Fabrication and Testing

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Appendix

Proof of operating frequency

BFP520 Spice File

```
*$
.SUBCKT BFP520/INF 200 100 300
L1    1    10    0.47nH
L2    2    20    0.56nH
L3    3    30    0.23nH
C1   10    20    6.9fF
C2   20    30    134fF
C3   30    10    136fF
L4   10   100    0.53nH
L5   20   200    0.58nH
L6   30   300    0.05nH
Q1   2 1 3 BFP520
.ENDS
.MODEL BFP520 NPN(
+ IS =1.5E-17        NF =1            NR =1
+ ISE=2.5E-14        NE =2            ISC=2E-14
+ NC =2              BF =235          BR =1.5
+ VAF=25             VAR=2            IKF=0.4
+ IKR=0.01           RB =11           RBM=7.5
+ RE =0.6            RC =7.6          CJE=2.35E-13
+ VJE=0.958          MJE=0.335        CJC=9.3E-14
+ VJC=0.661          MJC=0.236        CJS=0
+ VJS=0.75           MJS=0.333        FC=0.5
+ XCJC=1             TF=1.7E-12       TR=5E-08
+ XTF=10             ITF=0.7          VTF=5
+ PTF=50             XTB=-0.25        XTI=0.035
+ EG=1.11)
****************************************************************
*$
```

Calculation of matching network