Designing Oscillator for an Antenna at $\sim 3.5[GHz]$

2896

Mazz Shaikh(932056724), Nir Finch Cohen(230336612)

Edoh Shaulov

Tel Aviv University

Milestones completed so far

List of Milestones completed

- Selected the transistor we will use
- Simulated the oscillator we designed in PSpice
- Designed Matching network for the load(antenna)
- Optimised matching network for efficiency

List of Milestones completed

- Selected the transistor we will use
- Simulated the oscillator we designed in PSpice
- Designed Matching network for the load(antenna)
- Optimised matching network for efficiency

List of Milestones completed

- Selected the transistor we will use
- Simulated the oscillator we designed in PSpice
- Designed Matching network for the load(antenna)
- Optimised matching network for efficiency

List of Milestones completed

- Selected the transistor we will use
- Simulated the oscillator we designed in PSpice
- Designed Matching network for the load(antenna)
- Optimised matching network for efficiency

Choosing the BJT

Reqired characteristics

- The transistor needs high-frequency performance, including $f_{\max}$ and f_t, well above $3.5[GHz]$.

- Low parasitic capacitance at collector, base, and emitter terminals is crucial.

- Low noise figure is essential.

- High gain, especially at the operating frequency, is necessary for stable oscillation.

- Ensure appropriate biasing for Colpitts oscillator operation, including DC voltages and currents.

Reqired characteristics

- The transistor needs high-frequency performance, including $f_{\max}$ and f_t, well above $3.5[GHz]$.

- Low parasitic capacitance at collector, base, and emitter terminals is crucial.

- Low noise figure is essential.

- High gain, especially at the operating frequency, is necessary for stable oscillation.

- Ensure appropriate biasing for Colpitts oscillator operation, including DC voltages and currents.

Reqired characteristics

- The transistor needs high-frequency performance, including $f_{\max}$ and f_t, well above $3.5[GHz]$.

- Low parasitic capacitance at collector, base, and emitter terminals is crucial.

- Low noise figure is essential.

- High gain, especially at the operating frequency, is necessary for stable oscillation.

- Ensure appropriate biasing for Colpitts oscillator operation, including DC voltages and currents.

Reqired characteristics

- The transistor needs high-frequency performance, including $f_{\max}$ and f_t, well above $3.5[GHz]$.

- Low parasitic capacitance at collector, base, and emitter terminals is crucial.

- Low noise figure is essential.

- High gain, especially at the operating frequency, is necessary for stable oscillation.

- Ensure appropriate biasing for Colpitts oscillator operation, including DC voltages and currents.

Reqired characteristics

- The transistor needs high-frequency performance, including $f_{\max}$ and f_t, well above $3.5[GHz]$.

- Low parasitic capacitance at collector, base, and emitter terminals is crucial.

- Low noise figure is essential.

- High gain, especially at the operating frequency, is necessary for stable oscillation.

- Ensure appropriate biasing for Colpitts oscillator operation, including DC voltages and currents.

Transistor Details

BFP520 from Infenion[1]

- Surface mount low voltage silicon NPN RF bipolar transistor

- Transition frequency f_T of $45[GHz]$

- High Gain, with $|S_{12}|$, G_{ma}, $G_{ms} > 16[dB]$ at $3.5[GHz]$ under $V_{ce} = 2[V]$

- Low Noise Figure, $NF < 1.2[dB]$ at $3.5[GHz], 2[V], 2[mA]$

---

[1] https://www.infineon.com/dgdl/Infineon-BFP520-DS-v02_00-EN.pdf? fileId=5546d462689a790c01690f035fe2391a

Transistor Details

BFP520 from Infenion[1]

- Surface mount low voltage silicon NPN RF bipolar transistor

- Transition frequency f_T of 45[GHz]

- High Gain, with $|S_{12}|$, G_{ma}, $G_{ms} > 16[dB]$ at 3.5[GHz] under $V_{ce} = 2[V]$

- Low Noise Figure, $NF < 1.2[dB]$ at 3.5[GHz], 2[V], 2[mA]

---

[1]https://www.infineon.com/dgdl/Infineon-BFP520-DS-v02_00-EN.pdf?
fileId=5546d462689a790c01690f035fe2391a

Transistor Details

BFP520 from Infenion[1]

- Surface mount low voltage silicon NPN RF bipolar transistor
- Transition frequency f_T of $45[GHz]$
- High Gain, with $|S_{12}|$, G_{ma}, $G_{ms} > 16[dB]$ at $3.5[GHz]$ under $V_{ce} = 2[V]$
- Low Noise Figure, $NF < 1.2[dB]$ at $3.5[GHz], 2[V], 2[mA]$

---

[1] https://www.infineon.com/dgdl/Infineon-BFP520-DS-v02_00-EN.pdf? fileId=5546d462689a790c01690f035fe2391a

Transistor Details

BFP520 from Infenion[1]

- Surface mount low voltage silicon NPN RF bipolar transistor
- Transition frequency f_T of $45[GHz]$
- High Gain, with $|S_{12}|$, G_{ma}, $G_{ms} > 16[dB]$ at $3.5[GHz]$ under $V_{ce} = 2[V]$
- Low Noise Figure, $NF < 1.2[dB]$ at $3.5[GHz], 2[V], 2[mA]$

---

[1]https://www.infineon.com/dgdl/Infineon-BFP520-DS-v02_00-EN.pdf?
fileId=5546d462689a790c01690f035fe2391a

Transistor Details

<div style="text-align:center">

BFP520 from Infenion[1]

</div>

- Surface mount low voltage silicon NPN RF bipolar transistor
- Transition frequency f_T of $45[GHz]$
- High Gain, with $|S_{12}|, G_{ma}, G_{ms} > 16[dB]$ at $3.5[GHz]$ under $V_{ce} = 2[V]$
- Low Noise Figure, $NF < 1.2[dB]$ at $3.5[GHz], 2[V], 2[mA]$

---

[1] https://www.infineon.com/dgdl/Infineon-BFP520-DS-v02_00-EN.pdf?fileId=5546d462689a790c01690f035fe2391a
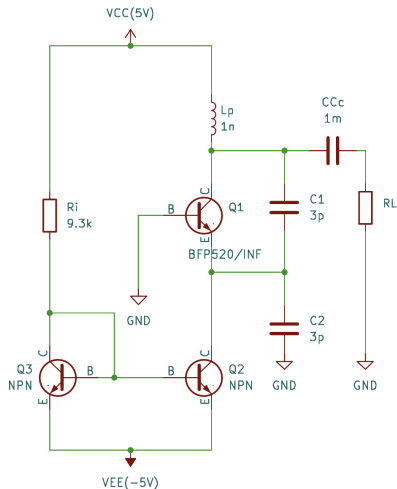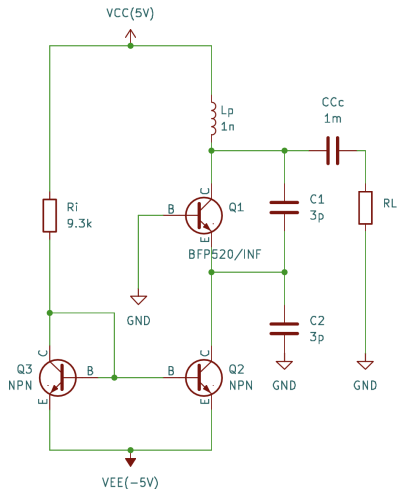
Oscillator Circuit

Collpit's Oscillator

- The circuit was tested with some high impedance load attached

- Values of L_p, C_1 and C_2 were computed using the operating frequency formula

$$f_c \approx \frac{1}{2\pi\sqrt{L_p\frac{C_1 C_2}{C_1+C_2}}}$$

[a]

- $C_1 = C_2$ was chosen since it gave the highest oscillation frequency

---

[a]In-depth analysis in Appendix

Collpit's Oscillator

- The circuit was tested with some high impedance load attached

- Values of L_p, C_1 and C_2 were computed using the operating frequency formula

$$f_c \approx \frac{1}{2\pi\sqrt{L_p \frac{C_1 C_2}{C_1 + C_2}}}$$

a

- $C_1 = C_2$ was chosen since it gave the highest oscillation frequency

---

[a]In-depth analysis in Appendix

Collpit's Oscillator

- The circuit was tested with some high impedance load attached

- Values of L_p, C_1 and C_2 were computed using the operating frequency formula

$$f_c \approx \frac{1}{2\pi\sqrt{L_p \frac{C_1 C_2}{C_1 + C_2}}}$$

a

- $C_1 = C_2$ was chosen since it gave the highest oscillation frequency

---

[a] In-depth analysis in Appendix

Ouput Waveform

Choosing a Matching Network

Matching Network

T-matching is better for matching a load to a source impedance when there's a large disparity because it provides efficient power transfer, minimizes losses, and offers impedance transformation with stability.[2]

- $L_{src} = 2.03361[nH]$
- $C_{src} = 2.02955[fF]$
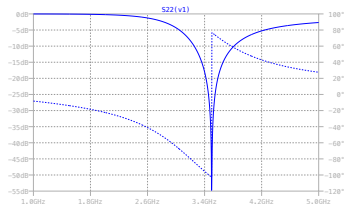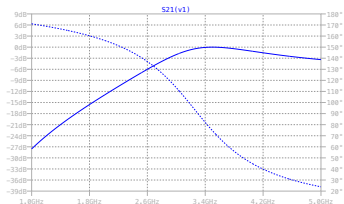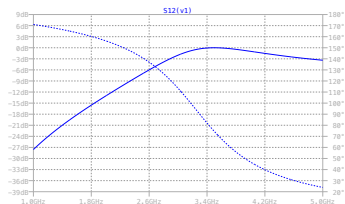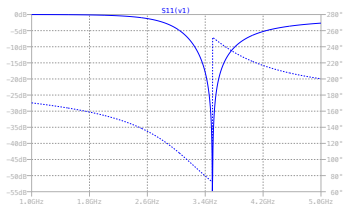- $L_{ld} = 10.4421[nH]$
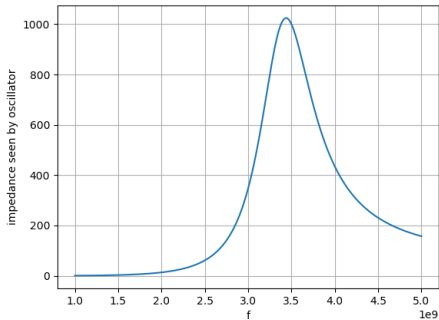- $C_{ld} = 0.208424[pF]$

---
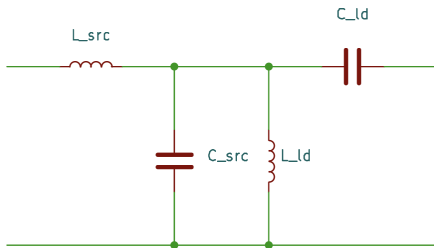
[2]Design method in Appendix

S-parameters of the Matching Network[3]

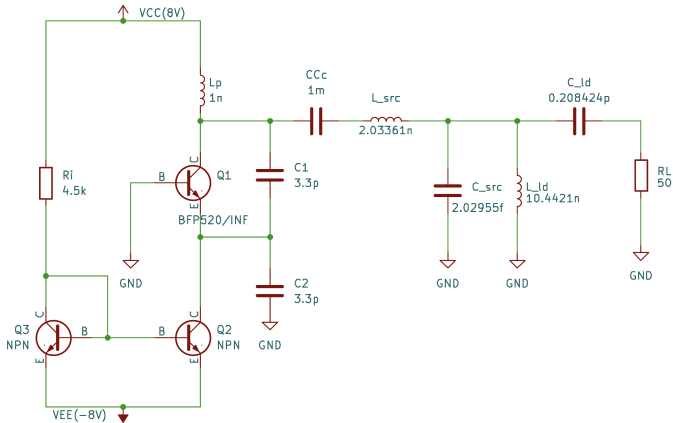[3]Simulated using .net parameter in LTSpice

Input impedance through the Matching Network

- Attains max value of $\approx 1000[\Omega]$ at $3.5[GHz]$
- Tapers quickly for the non-central frequencies

Oscillator using Matching Network as 50[Ω] load

After making adjustments to supply and current to maximize efficiency, we have the following system[4]

---

[4]Efficiency η is defined in the next section

Output of Oscillator using Matching Network as 50[Ω] load

Efficiency

Calculation of η

- **Input:** $P_{DC} = V_{CC}I_C$
- **Output:** $P_{ac} = \frac{V_{rms}^2}{R_L}$ where $V_{rms} = \frac{V_{max}}{\sqrt{2}}$ for the output waveform
- **Efficiency:** $\eta = \frac{P_{ac}}{P_{CD}}$

---

[5]It has been shown (Krauss, et al., 1980) that the maximum theoretical efficiency for this oscillator configuration is 25%, implying we have a decent efficiency

Calculation of η

- **Input:** $P_{DC} = V_{CC} I_C$
- **Output:** $P_{ac} = \frac{V_{rms}^2}{R_L}$ where $V_{rms} = \frac{V_{max}}{\sqrt{2}}$ for the output waveform
- **Efficiency:** $\eta = \frac{P_{ac}}{P_{CD}}$

---

[5]It has been shown (Krauss, et al., 1980) that the maximum theoretical efficiency for this oscillator configuration is 25%, implying we have a decent efficiency

Calculation of η

- **Input:** $P_{DC} = V_{CC} I_C$
- **Output:** $P_{ac} = \frac{V_{rms}^2}{R_L}$ where $V_{rms} = \frac{V_{max}}{\sqrt{2}}$ for the output waveform
- **Efficiency:** $\eta = \frac{P_{ac}}{P_{CD}}$

---

[5]It has been shown (Krauss, et al., 1980) that the maximum theoretical efficiency for this oscillator configuration is 25%, implying we have a decent efficiency

Calculation of η

- **Input:** $P_{DC} = V_{CC}I_C$
- **Output:** $P_{ac} = \frac{V_{rms}^2}{R_L}$ where $V_{rms} = \frac{V_{max}}{\sqrt{2}}$ for the output waveform
- **Efficiency:** $\eta = \frac{P_{ac}}{P_{CD}}$

For $V_{cc} = -V_{ee} = 8[V]$, and current mirror set to give $3.36[mA]$, we have $v_p = 1.6[V]$, giving us

$$\eta \approx 20\%[5]$$

---

[5]It has been shown (Krauss, et al., 1980) that the maximum theoretical efficiency for this oscillator configuration is 25%, implying we have a decent efficiency

Antenna Design

Patch Microstrip Antenna

- Directional Antenna with good efficiency and high gain when used in an antenna array
- Input impedance of 50[Ω]

Patch Microstrip Antenna

- Directional Antenna with good efficiency and high gain when used in an antenna array
- Input impedance of 50[Ω]

Next Steps

Next Steps
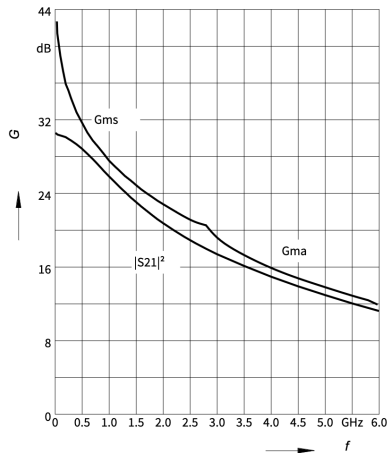
- Layout the PCB
- Fabrication and Testing

Next Steps

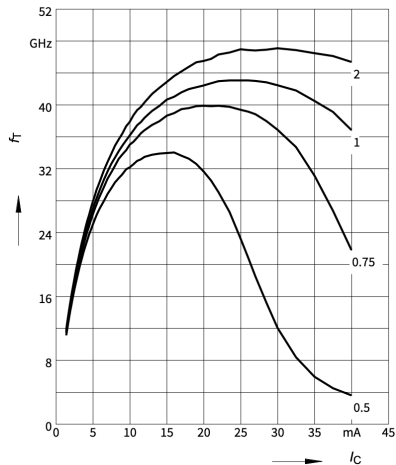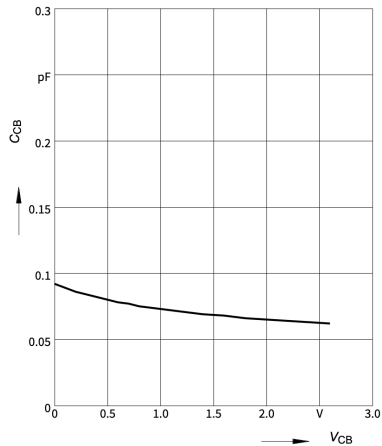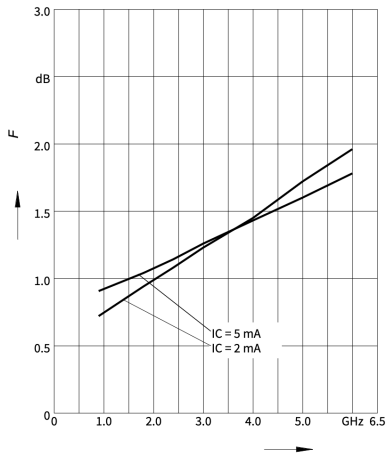- Layout the PCB
- Fabrication and Testing

Appendix

Data from Infenion - 1

BFP520 Spice File

```
.SUBCKT BFP520/INF 200 100 300
L1    1    10    0.47nH
L2    2    20    0.56nH
L3    3    30    0.23nH
C1    10   20    6.9fF
C2    20   30    134fF
C3    30   10    136fF
L4    10   100   0.53nH
L5    20   200   0.58nH
L6    30   300   0.05nH
Q1    2  1  3  BFP520
.ENDS
.MODEL BFP520 NPN(
+ IS =1.5E-17        NF =1              NR =1
+ ISE=2.5E-14        NE =2              ISC=2E-14
+ NC =2              BF =235            BR =1.5
+ VAF=25             VAR=2              IKF=0.4
+ IKR=0.01           RB =11             RBM=7.5
+ RE =0.6            RC =7.6            CJE=2.35E-13
+ VJE=0.958          MJE=0.335          CJC=9.3E-14
+ VJC=0.661          MJC=0.236          CJS=0
+ VJS=0.75           MJS=0.333          FC=0.5
+ XCJC=1             TF=1.7E-12         TR=5E-08
+ XTF=10             ITF=0.7            VTF=5
+ PTF=50             XTB=-0.25          XTI=0.035
+ EG=1.11)
```

Proof of operating frequency - 1

We have the following small signal model of Collpit's oscillator, with $C_1 = C_2 = C$[6]

---
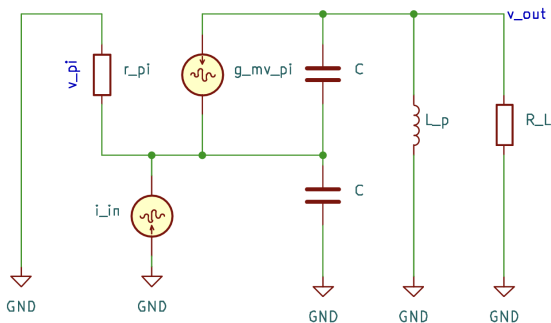
[6]In all the results, we try to ignore effects of r_π and then adjust the values accordingly to get required response

Proof of operating frequency - 2

$$i_{in} = -\frac{v_\pi}{r_\pi} - sC(v_{out} + 2v_\pi)$$

$$g_m v_\pi + sC(v_{out} + v_\pi) + \frac{v_{out}}{sL_p} + \frac{v_{out}}{R_L} = 0$$

This gives us the following frequency response

$$\frac{v_{out}}{i_{in}} = \frac{r_\pi L_p R_L(s^2 C + sg_m)}{r_\pi C^2 L_p R_L s^3 + (-r\pi C L_p R_L g_m + 2r_\pi C L_p + C L_p R_L)s^2 + (2r_\pi C R_L + L_p)s + R_L}$$

Put $s = j\omega$ and let *Im* of denominator $\to 0$

$$\omega_0 = \sqrt{\frac{2r_\pi C R_L + L_p}{r_\pi C^2 L_p R_L}}$$

Assuming $r_\pi \to \infty$, as is the case is MOS, we reach the well-known expression $\omega_0 = \sqrt{\frac{1}{L\frac{C.C}{C+C}}}$

Proof of operating frequency - 3

For sustained oscillations, we need

$$-(-r_\pi C L_p R_L g_m + 2 r_\pi C L_p + C L_p R_L)\omega_0^2 + R_L > 0$$

This gives us

$$^7 R_L g_m - \frac{R_L}{r_\pi} - 2 > 0$$

Thus, we need to set R_L accordingly at the oscillating frequency, giving us a lower bound for load and thus a need for a matching network

----

[7]This is similar to the condition found in Razavi, but for NMOS in place of NPN BJT

Calculation of matching network - 1

We have a source impedance Z_s, a load impedance Z_L, and operating frequency f_0 and we need to match Z_L to Z_s at f_0 using a T-Matching Network. We assume a central impedance Z_c such that $Z_c > \max(Z_s, Z_L)$, and then calculate the series and parallel reactive components on both sides.[8]

Source:

$$Q_{src} = \sqrt{\frac{Z_c}{Z_s} - 1}$$

$$X_{src}^{patallel} = \frac{Z_c}{Q_{src}}$$

$$X_{src}^{series} = Q_{src} Z_s$$

Load:

$$Q_{ld} = \sqrt{\frac{Z_c}{Z_L} - 1}$$

$$X_{ld}^{patallel} = \frac{Z_c}{Q_{ld}}$$

$$X_{ls}^{series} = Q_{ls} Z_L$$

Then, $L = \frac{X}{2\pi f_0}$ and $C = \frac{1}{2\pi f_0 X}$ for chosen X series/parallel

---

[8] In our case, all impedances are real

20

Calculation of matching network - 2^9

After this, the values of V_{cc}, V_{ee}, and I_c were changed so as to get the maximum efficiency. R_L was matched to $1[K\Omega]$.

Variable	Value
f_0	3.5×10^9
$Z_{\text{out\_osc}}$	1000
Z_{load}	50
Z_{center}	1002
Q_{src}	0.0447214
$X_{\text{paralle\_src}}$	22405.4
$X_{\text{series\_src}}$	44.7214
L_{src}	2.03361×10^{-9}

Variable	Value
C_{src}	2.02955×10^{-15}
Q_{ld}	4.36348
$X_{\text{paralle\_ld}}$	229.633
$X_{\text{series\_ld}}$	218.174
L_{ld}	1.04421×10^{-8}
C_{ld}	2.08424×10^{-13}
C_{com}	2.10454×10^{-13}
L_{com}	1.70212×10^{-9}

---

[9]Values generated using .py script that we made

Calculation of parameters of Patch Antenna

1. $W = \frac{1}{2f\sqrt{\mu_0\epsilon_0}}\sqrt{\frac{2}{\epsilon_r+1}}$

2. $\epsilon_{eff} = \frac{\epsilon_r+1}{2} + \frac{\epsilon_r-1}{2\sqrt{1+\frac{12h}{W}}}$

3. $\frac{\Delta L}{h} = 0.412\frac{(\epsilon_{eff}+0.3)(\frac{W}{h}+0.264)}{(\epsilon_{eff}-0.258)(\frac{W}{h}+0.8)}$

Calculation of parameters of Patch Antenna

1. $W = \frac{1}{2f\sqrt{\mu_0\epsilon_0}}\sqrt{\frac{2}{\epsilon_r+1}}$

2. $\epsilon_{eff} = \frac{\epsilon_r+1}{2} + \frac{\epsilon_r-1}{2\sqrt{1+\frac{12h}{W}}}$

3. $\frac{\Delta L}{h} = 0.412\frac{(\epsilon_{eff}+0.3)\left(\frac{W}{h}+0.264\right)}{(\epsilon_{eff}-0.258)\left(\frac{W}{h}+0.8\right)}$

Calculation of parameters of Patch Antenna

1. $W = \frac{1}{2f\sqrt{\mu_0 \epsilon_0}}\sqrt{\frac{2}{\epsilon_r+1}}$

2. $\epsilon_{eff} = \frac{\epsilon_r+1}{2} + \frac{\epsilon_r-1}{2\sqrt{1+\frac{12h}{W}}}$

3. $\frac{\Delta L}{h} = 0.412\frac{(\epsilon_{eff}+0.3)\left(\frac{W}{h}+0.264\right)}{(\epsilon_{eff}-0.258)\left(\frac{W}{h}+0.8\right)}$

📄 T. K. Johnson, "A colpitts oscillator design technique using s-parameters," 1986.

📄 X. Li, S. Shekhar, and D. Allstot, "G/sub m/-boosted common-gate lna and differential colpitts vco/qvco in 0.18-/spl mu/m cmos," *Solid-State Circuits, IEEE Journal of*, vol. 40, pp. 2609 – 2619, 01 2006.

📄 D. M. Pozar, *Microwave engineering; 3rd ed.* **Hoboken, NJ: Wiley, 2005.**

📄 B. Razavi, *Design of Analog CMOS Integrated Circuits.* **McGraw-Hill, first ed., 2001.**

📄 F. Ullah, Y. Liu, Z. Li, X. Wang, M. Sarfraz, and H. Zhang, "A bandwidth-enhanced differential lc-voltage controlled oscillator (lc-vco) and superharmonic coupled quadrature vco for k-band applications," *Electronics*, vol. 7, p. 127, 07 2018.

📄 M. Giuseppe, *Comparison of Voltage-Controlled-Oscillator Architectures for Implementation in 180 nm SiGe Technology.*
PhD thesis, 12 2016.