Session: ML Compilers & Runtime

Moderator: **Gennady Pekhimenko**

Talk Order:

Oral: The CoRa Tensor Compiler: Compilation for Ragged Tensors with Minimal Padding
Oral: Apollo: Automatic Partition-based Operator Fusion through Layer by Layer Optimizatior
Oral: DietCode: Automatic Optimization for Dynamic Tensor Programs
Oral: Bit-serial Weight Pools: Compression and Arbitrary Precision Execution of Neural Netw

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MLSys 2022
Exhibit Hall A

The CoRa Tensor Compiler: Compilation for Ragged Tensors with Minimal Padding

- Pratik Fegade *
- Tianqi Chen
- Phillip Gibbons
- Todd Mowry

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The CoRa Tensor Compiler: Compilation for Ragged Tensors With Minimal Padding

Pratik Fegade[1],
Tianqi Chen[1,2], Phillip B. Gibbons[1], Todd C. Mowry[1]

[1]Carnegie Mellon University [2]OctoML

Carnegie Mellon University
Computer Science Department

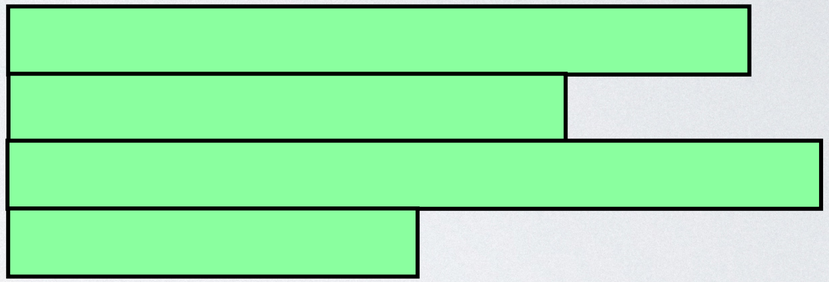
catalyst

Ragged Tensors in Deep Learning

- Natural language processing

```
input_batch = [
  [Dogs,  bark, .],
  [Maine, is,   a,     state, .],
  [The,   song, rocks, !],
  [Hello]
]
```

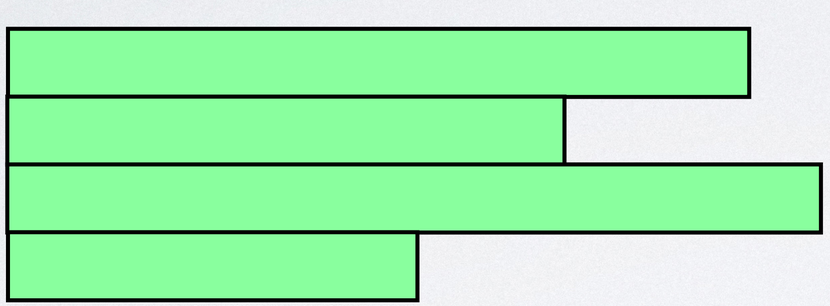
- Image processing



Ragged Tensor

Ragged Tensors

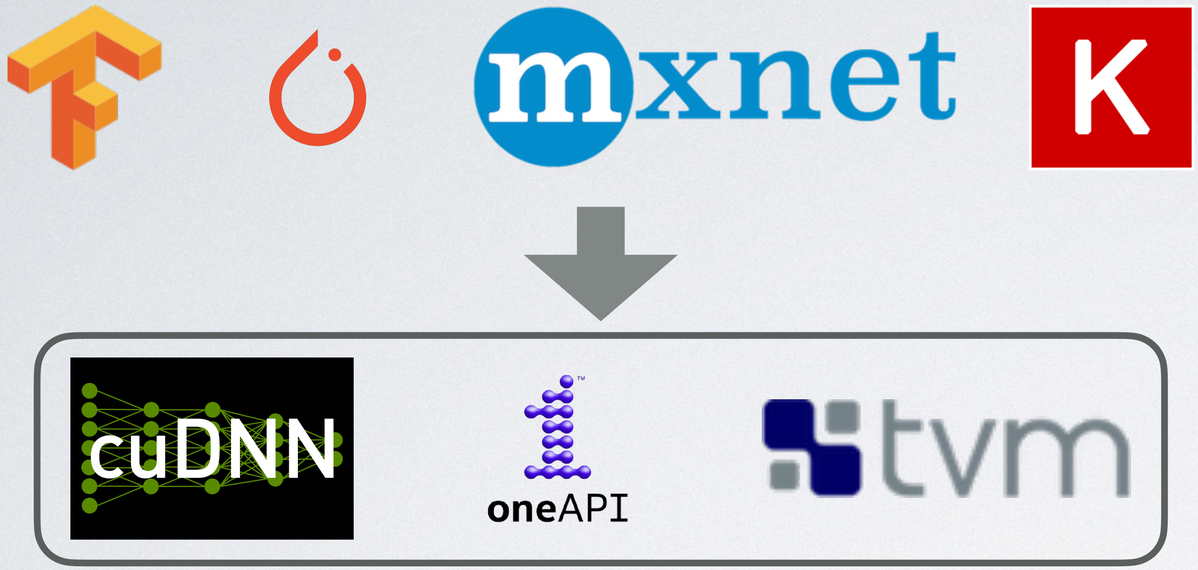
- Ragged tensor is a tensor where the slices corresponding to one or more dimensions have varying lengths

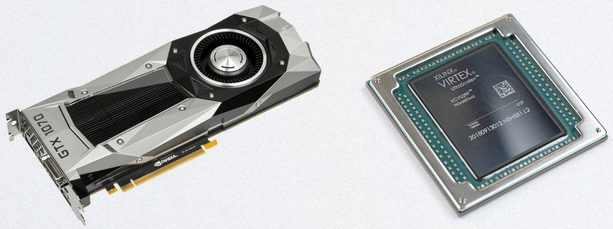


Dimensions: `[4, ?]`

Rows (slices of the inner dimension) have varying lengths

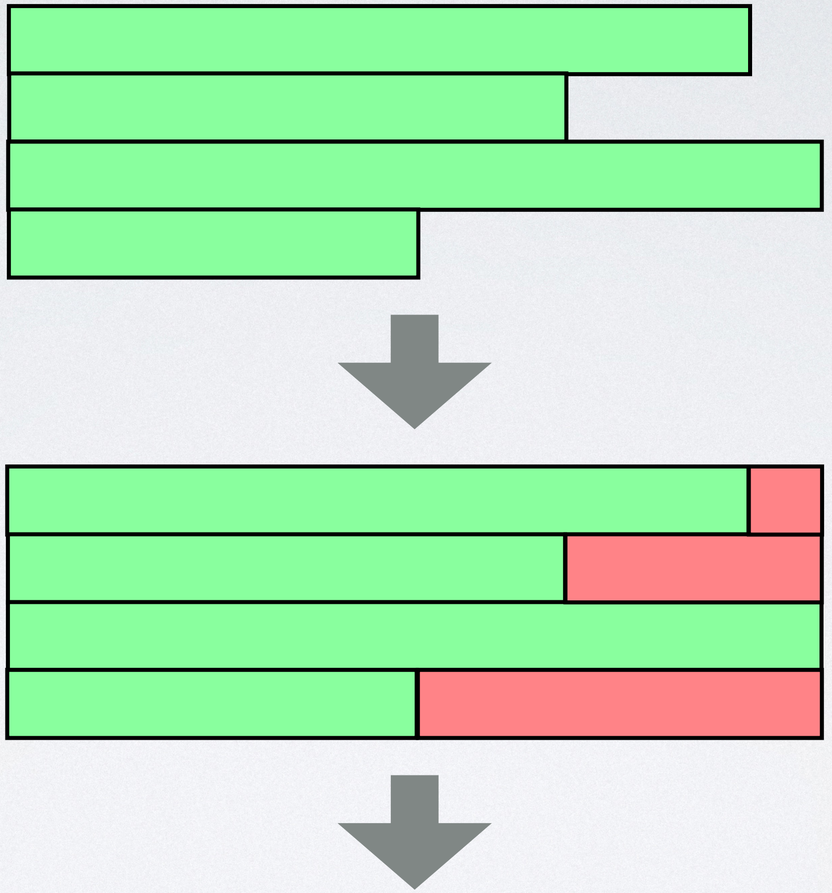
Limited Support for Ragged Tensor Operators





- Limited support for operations on ragged tensors
- Extensive support for dense tensors

And Padding Leads to Wasted Computation



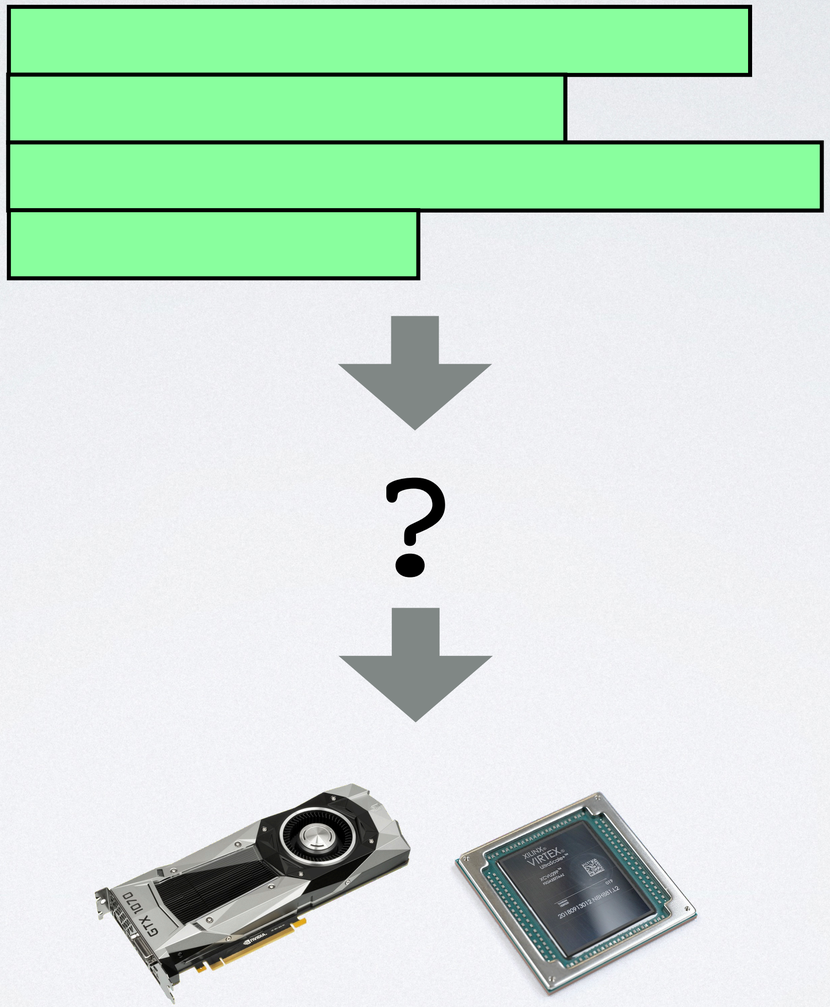
1.07 - 2.41X wasted computation!

cuDNN

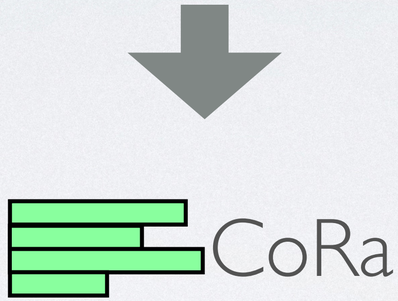
oneAPI

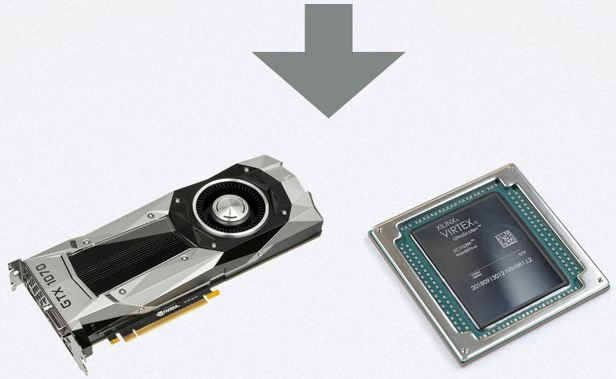
tvm

Ideal Execution: Compilation Without Padding

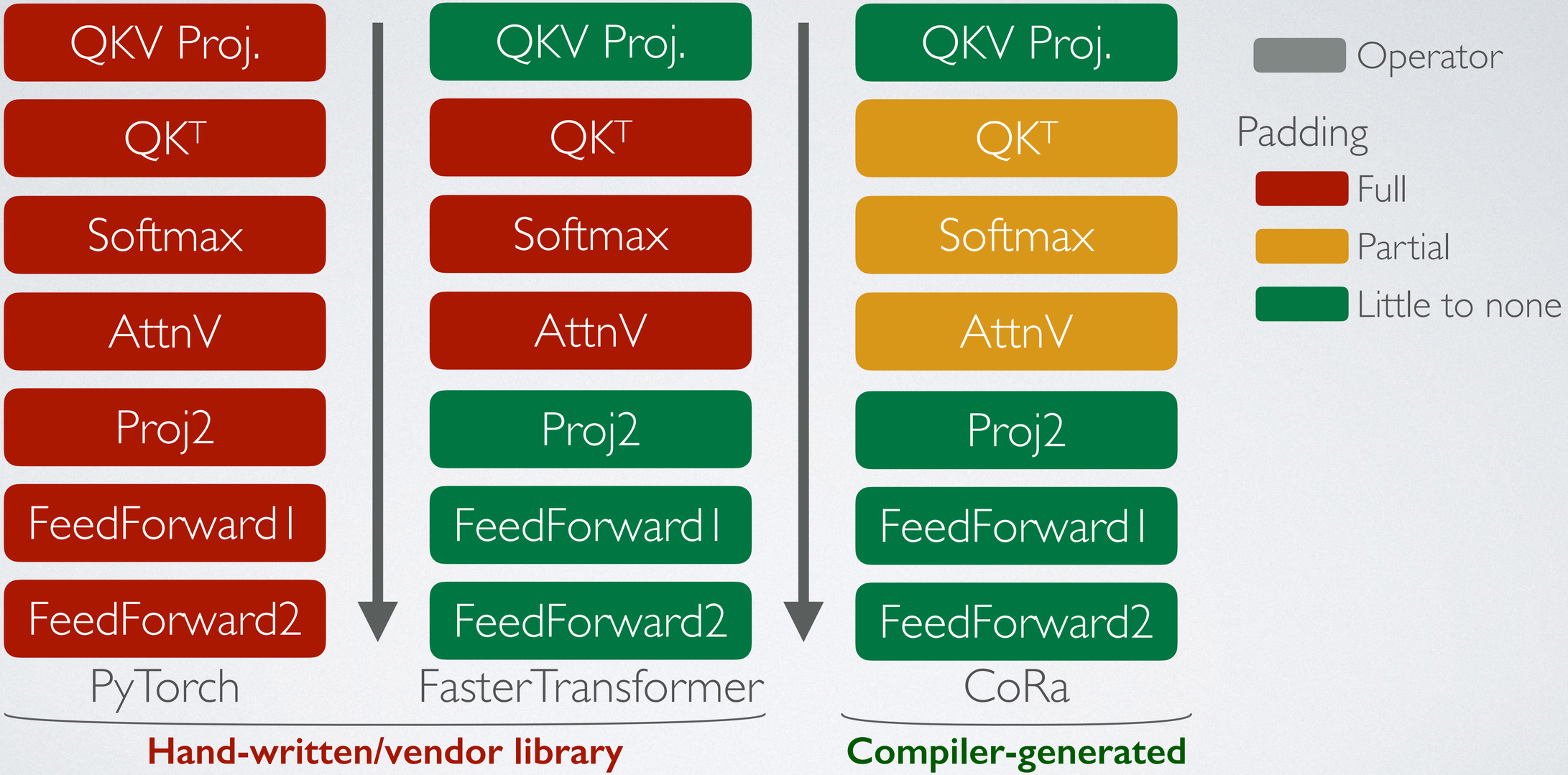


CoRa Enables Ragged Tensor Execution for Higher Frameworks





CoRa Enables Transformer Implementation Without Padding



Outline

- Motivation: Inefficient Support for Ragged Tensors
- CoRa: Our Compiler Based Solution
  - Scheduling and lowering
  - API and overview
- Evaluation
- Wrapping up

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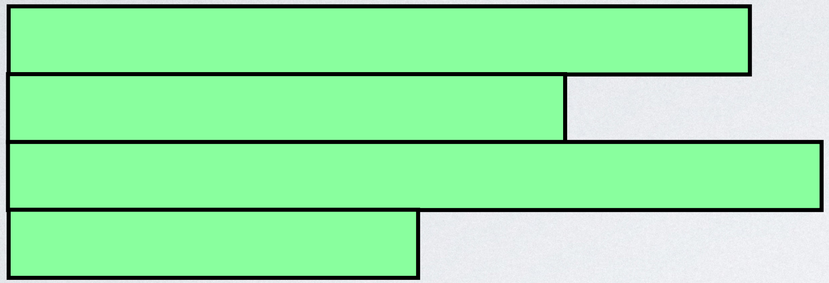
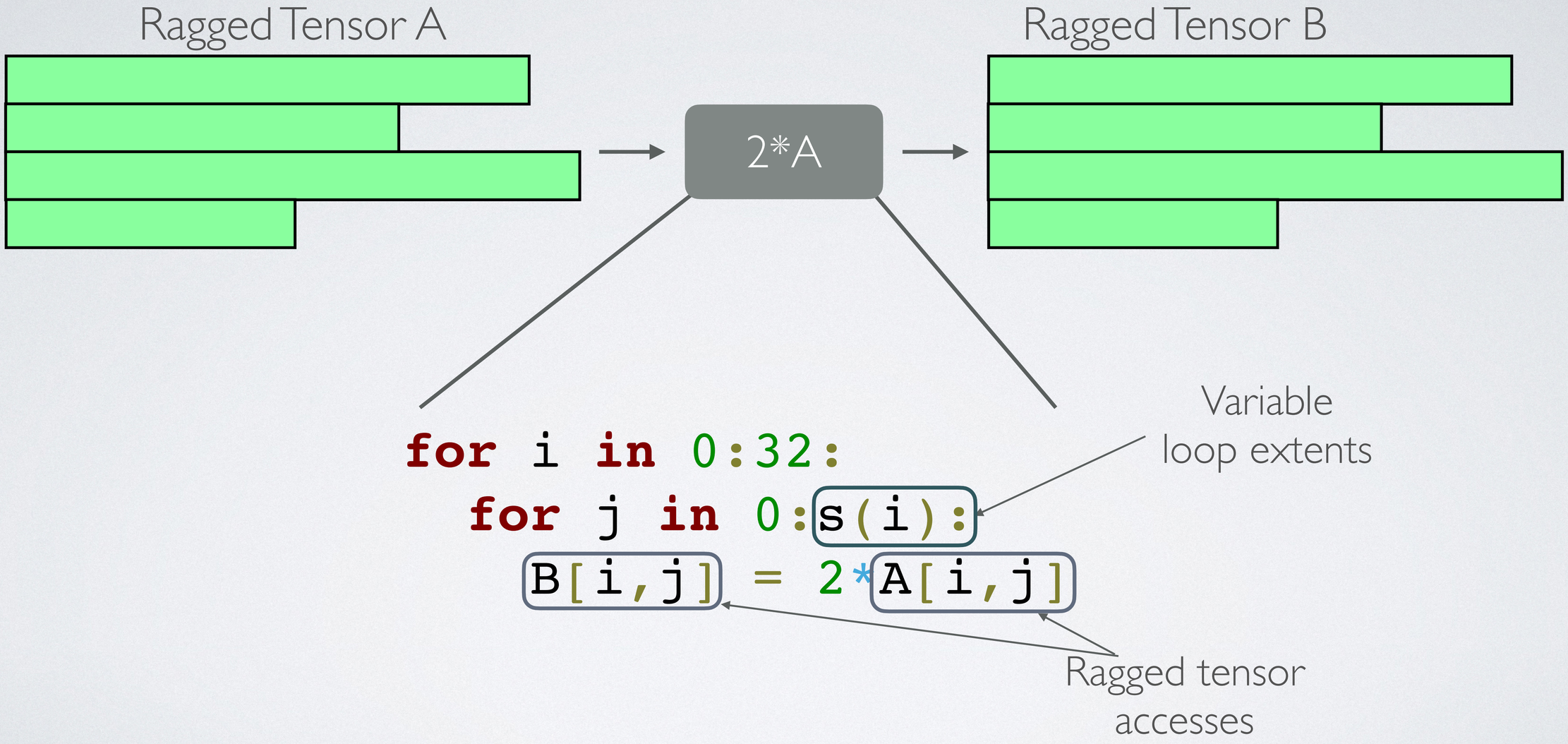
Ragged Computations Are Similar to Dense Computations



Densely packed data with no holes, like dense tensors

Ragged Computations Are Similar to Dense Computations



Ragged Computations Are Similar to Dense Computations

- Densely packed data with no holes, like dense tensors
- Ragged computations are similar to dense tensor computations

Reuse abstractions and techniques from dense tensor compilers

```
for i in 0:32:
  for j in 0:s(i):
    B[i,j] = 2*A[i,j]
```

Variable loop extents → Generalize
- Compiler's loop representations
- Scheduling primitives and their impl.

Ragged tensor accesses → Generalize
- Tensor storage scheme
- Tensor access lowering

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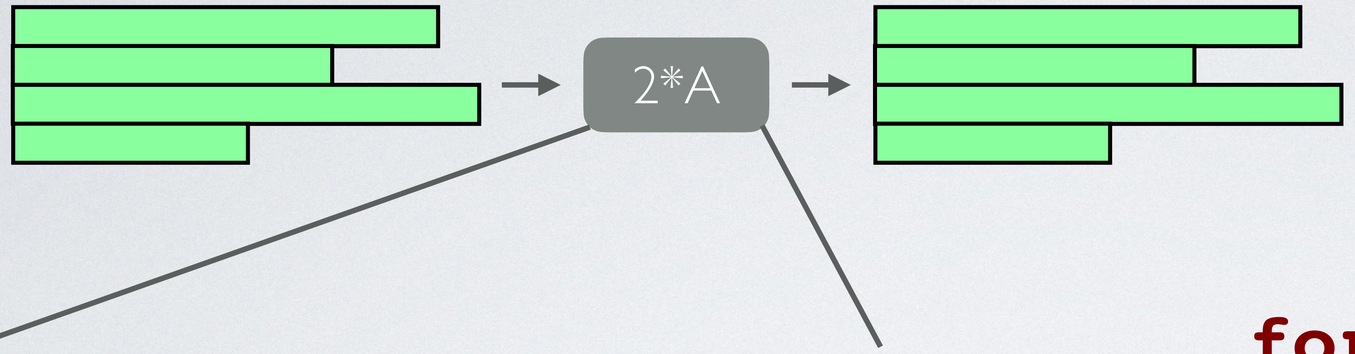
Loop Fusion in Ragged Operators




```
for i in 0:32:
  for j in 0:s(i):
    B[i,j] = 2*A[i,j]
```

Fuse(i,j)

$$\sum_{i=0}^{31} s(i)$$

```
for f in 0:?:
  i = ?
  j = ?
  B[i,j] = 2*A[i,j]
```

Pre-compute mappings from `f` to `i` and `j`

Once precomputed, we can schedule ragged ops like dense ops!

Ragged Computations Are Similar to Dense Computations

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Reuse abstractions and techniques from dense tensor compilers

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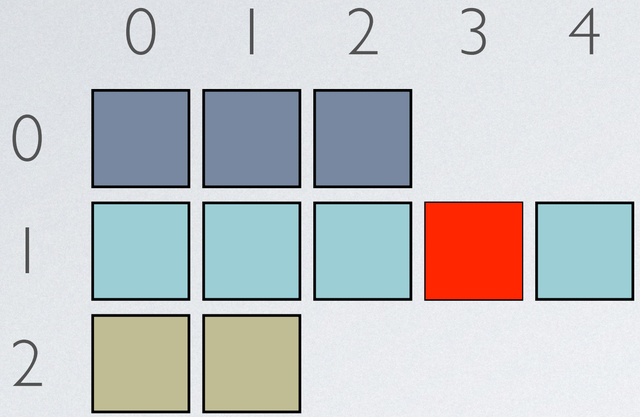
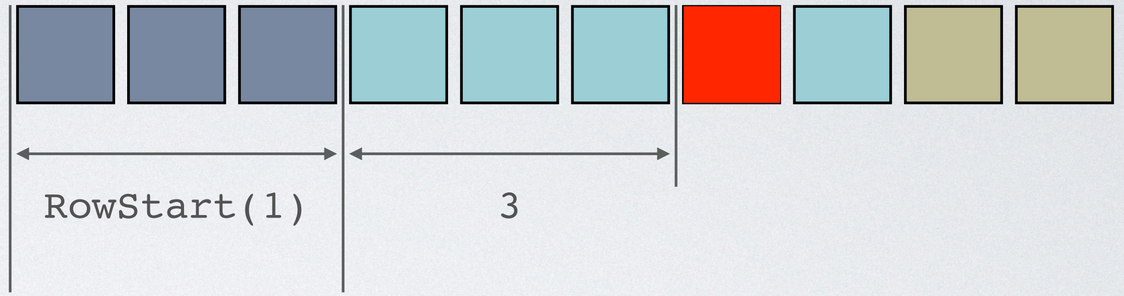
Ragged Tensor Storage Without Padding





Offset(1, 3) = RowStart(1) + 3

Need to precompute dimension offsets before kernel execution

Once precomputed, we have cheap random accesses, similar to dense tensors!

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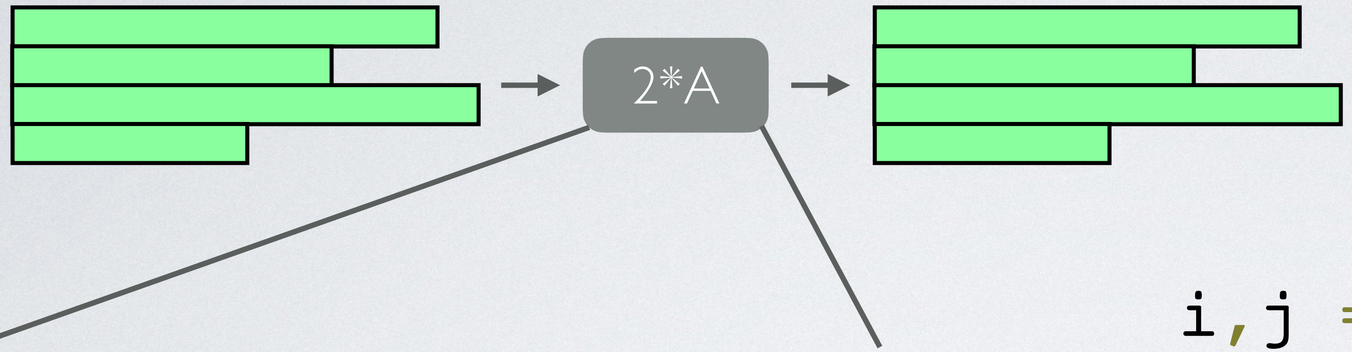
CoRa's API Is Similar to That of Dense Compilers

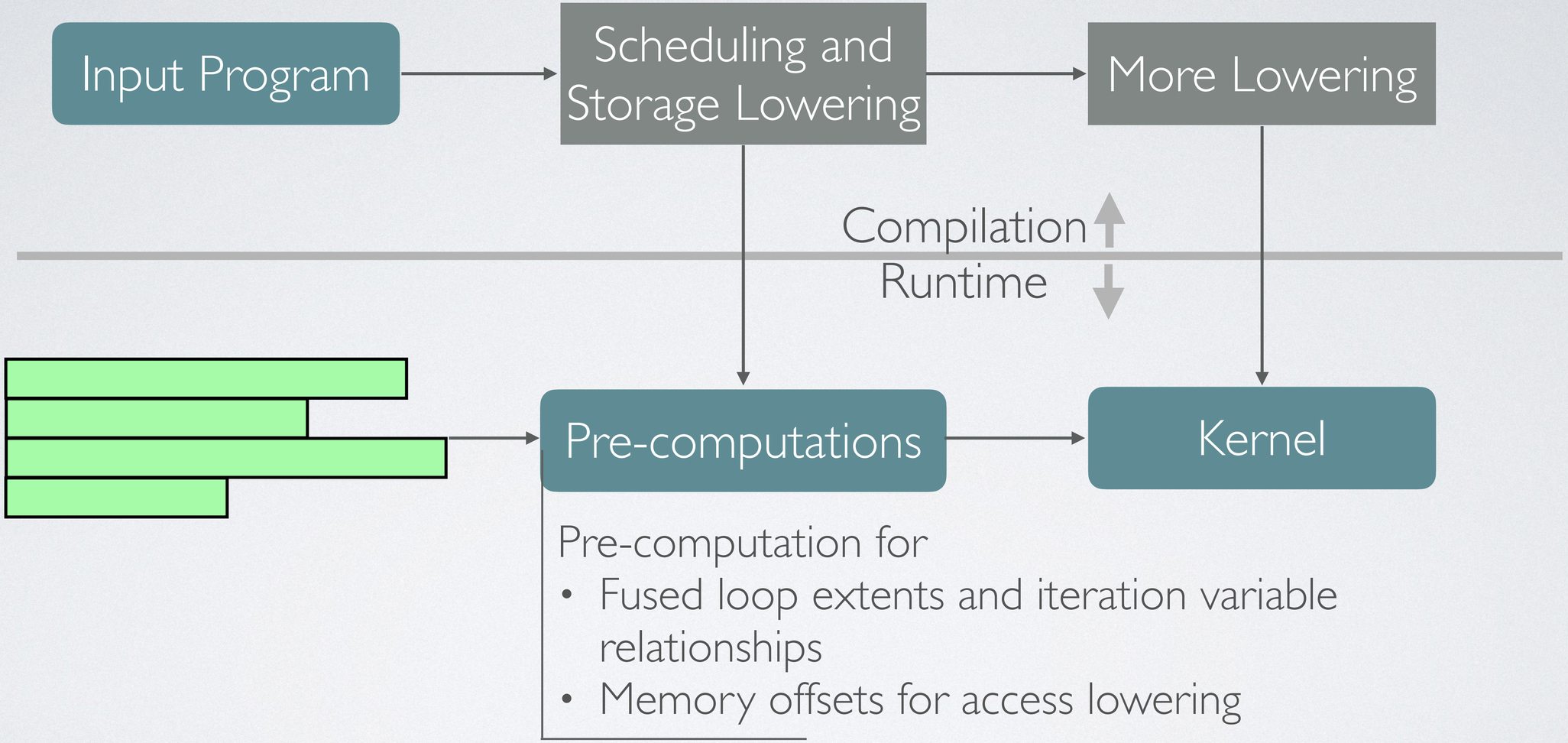



```
for i in 0:32:
  for j in 0:s(i):
    B[i,j] = 2*A[i,j]
```

```
i,j = B.axis
f = fuse(i,j)
fo, fi = split(f,64)
bind(fo, 'blockIdx.x')
bind(fi, 'threadIdx.x')
```

Other scheduling primitives for load balancing, operation splitting, tensor dimension scheduling are available

CoRa's Compilation and Runtime Pipeline



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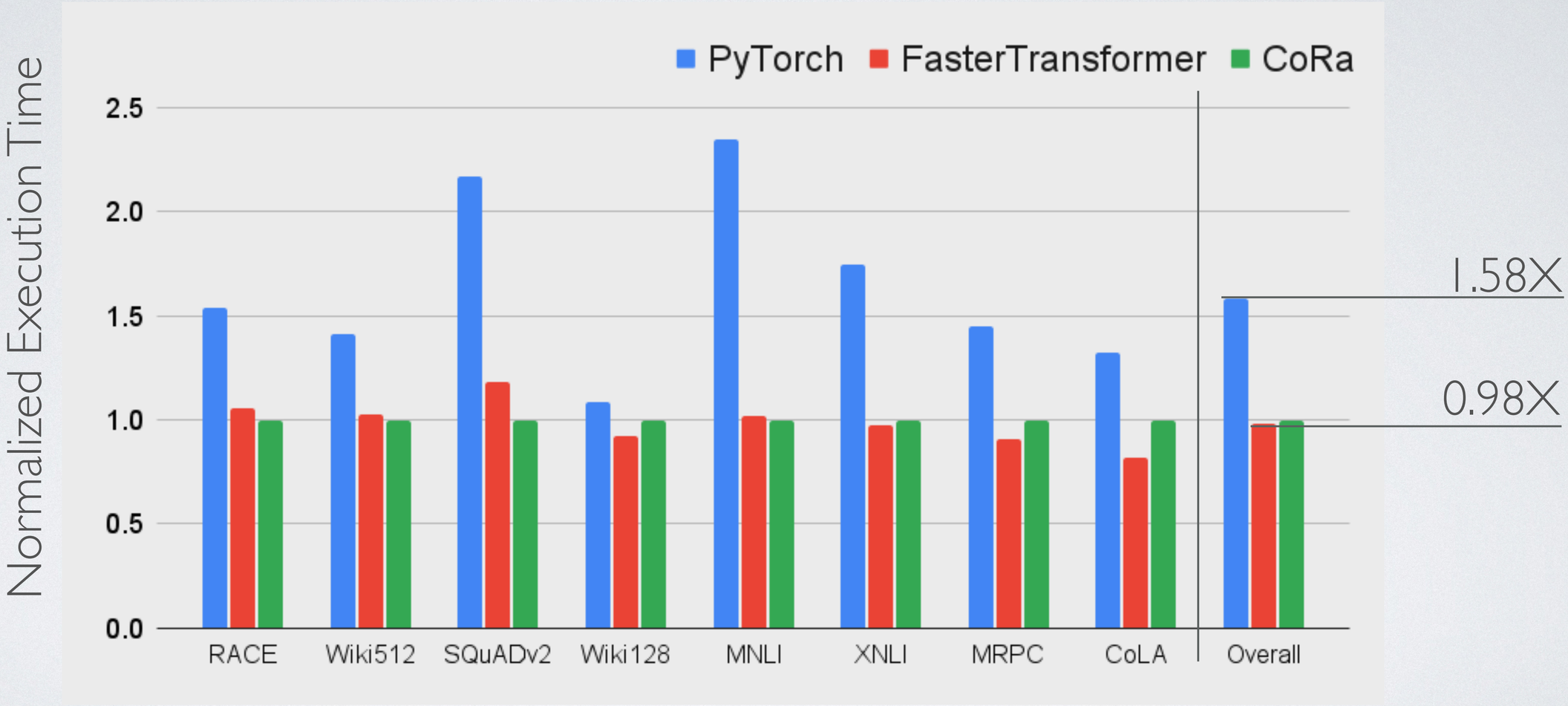
Layer Forward Pass Latencies on Nvidia V100 GPU

Lower is better



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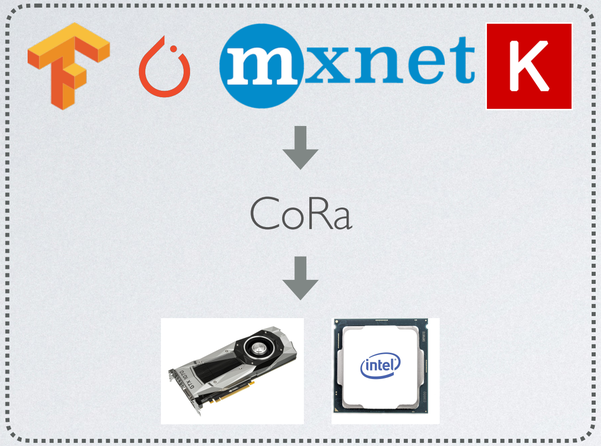
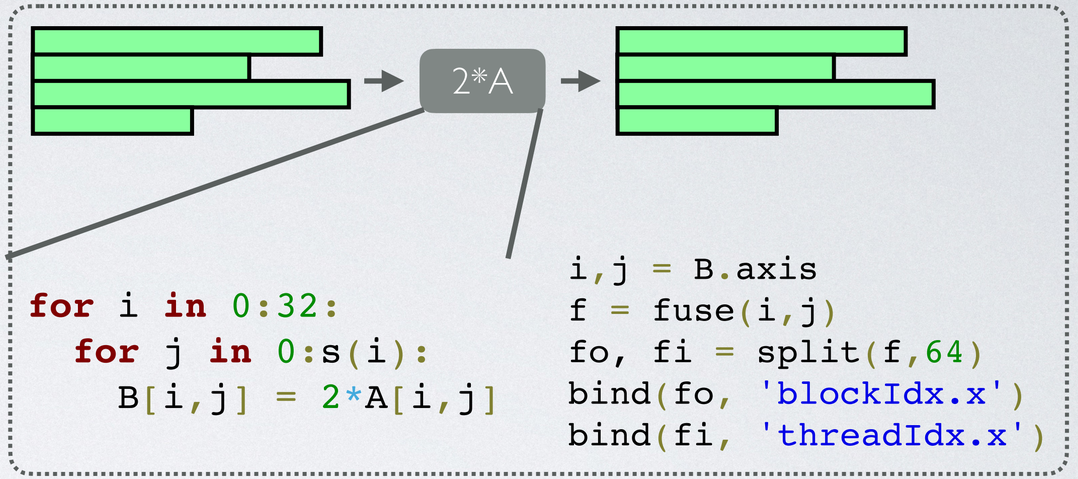
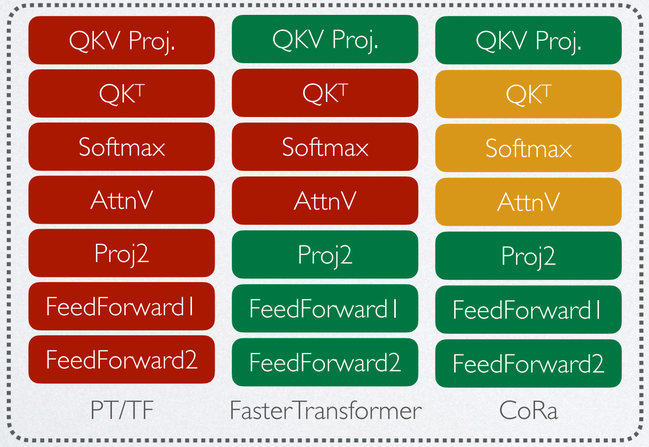
Wrapping Up CoRa



CoRa is a tensor compiler for operations on ragged tensors



CoRa provides a familiar API similar to that of dense tensor compilers



CoRa generates code as performant as hand-written code for transformer models

Apollo: Automatic Partition-based Operator Fusion through Layer by Layer Optimization

- Jie Zhao *
- Xiong Gao
- Ruijie Xia
- Zhaochuang Zhang
- Deshi Chen
- Lei Chen
- Renwei Zhang
- Zhen Geng
- Bin Cheng
- Xuefeng Jin

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APOLLO: Automatic Partition-based Operator Fusion through Layer by Layer Optimization

Presenter: Bojian Zheng

EcoSystem Research Group, University of Toronto, Toronto

presenting on behalf of

Jie Zhao[1] Xiong Gao[2] Ruijie Xia[2]
Zhaochuang Zhang[2] Deshi Chen[2] Lei Chen[3]
Renwei Zhang[2] Zhen Geng[2†] Bin Cheng[2] Xuefeng Jin[2]

[1]State Key Laboratory of Mathematical Engineering and Advanced Computing, Zhengzhou
[2]Huawei Technologies Co. Ltd., Hangzhou, Beijing and Shenzhen
[3]Hong Kong University of Science and Technology, Hong Kong
[†]Now is with the Parallel Computing Software Team at Alibaba, Hangzhou

Fifth Conference on Machine Learning and Systems **(MLSys'22)**

2022.08.29, Santa Clara, CA, USA

Outline

Fusion in Deep Learning Compilers

- *fusion* is an important transformation for making use of faster local memory, but it was **NOT** exploited by deep learning frameworks like TensorFlow [1] and Pytorch [10].

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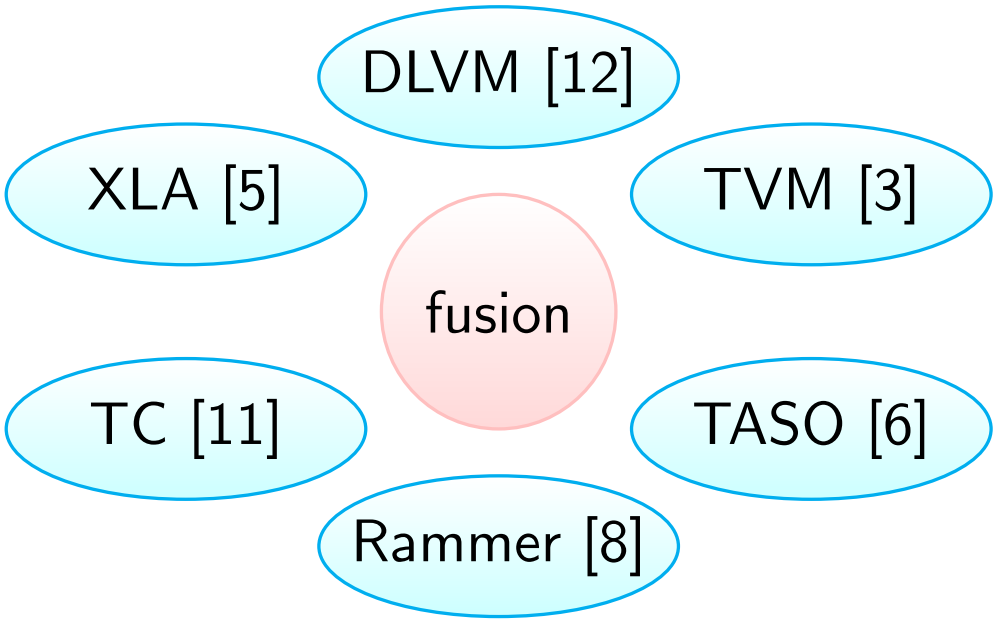
- In recent years, fusion has fascinated massive attentions in deep learning compilers.



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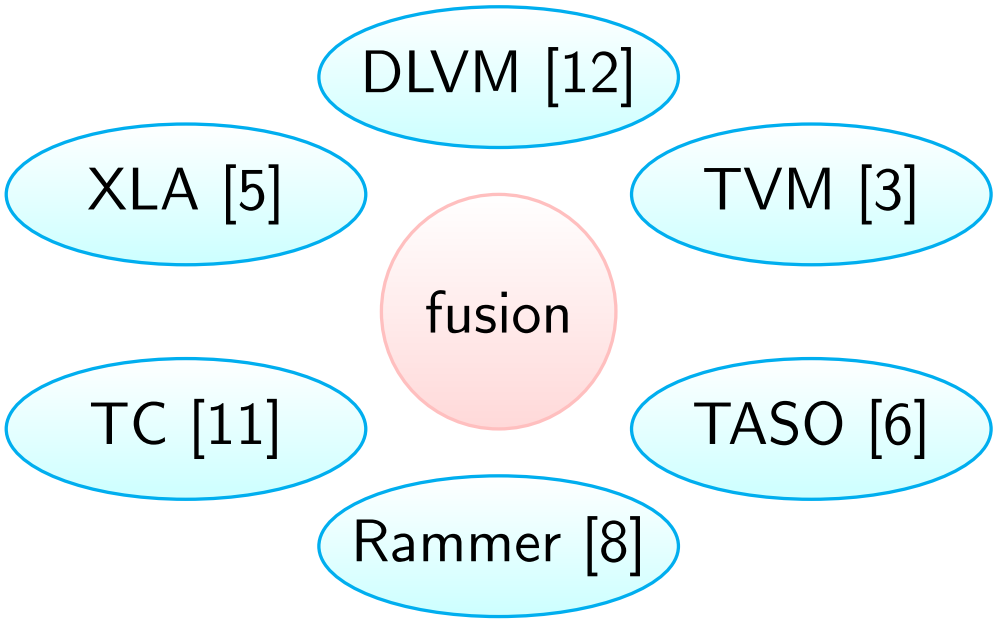
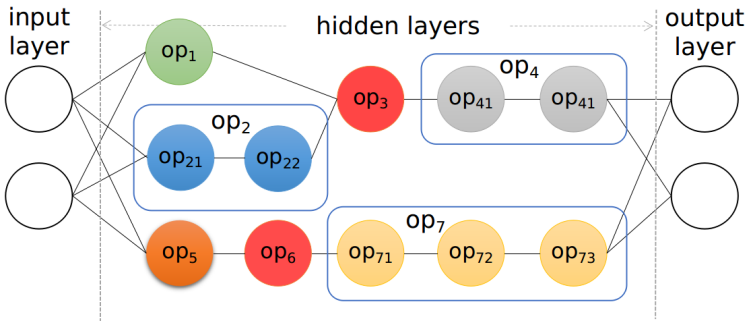


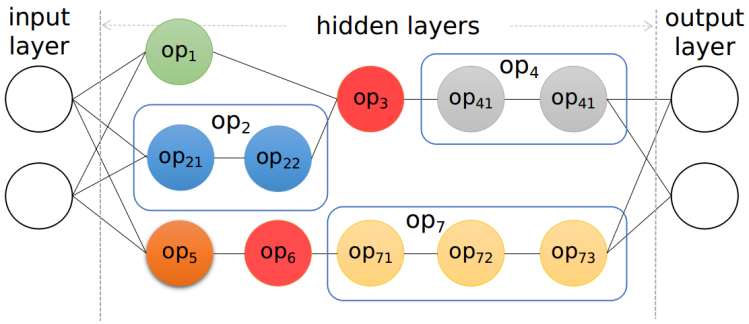
- While extensively investigated, fusion in these deep learning compilers can be inspected in different ways.

Limitations of Prior Fusion Compilers



A primitive/compound operator is denoted using a circle or a box. A compond operator is composed of multiple primitive operators. These operators consititute two sub-graphs.

Limitations of Prior Fusion Compilers



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- Graph compilers like XLA [5] and DLVM [12] did not consider compute-intensive operators (op_3 or op_5), isolating each of the two sub-graphs into multiple components.

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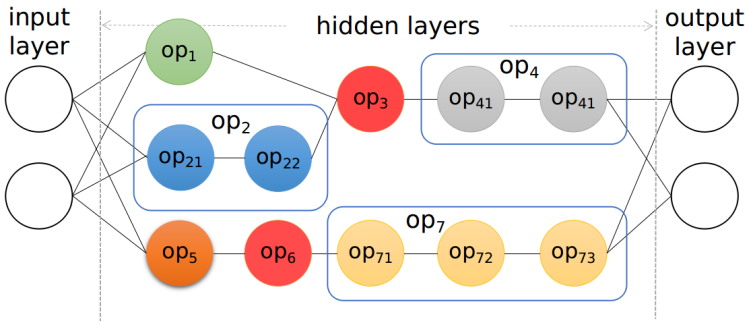

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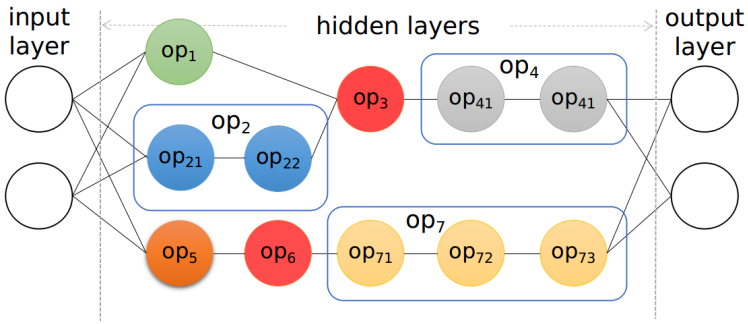

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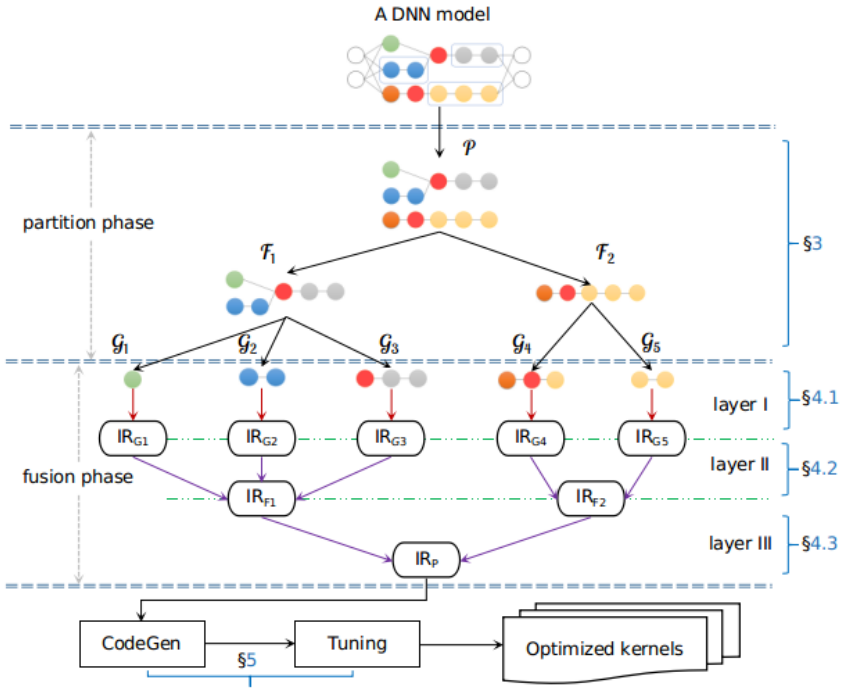
- Tensor compilers including TVM [3], TC [11] and Tiramisu [2] execute a routine transformation orchestration (first node grouping and next loop fusion), subject to the scalability issue [15, 9] caused by the constraints from the upstream graph engine.
- More recent works [6, 8, 17] investigated horizontal fusion between independent operators, e.g., (op_1 and op_2), but training workloads and dedicated chips were rarely considered.

Architecture of Apollo



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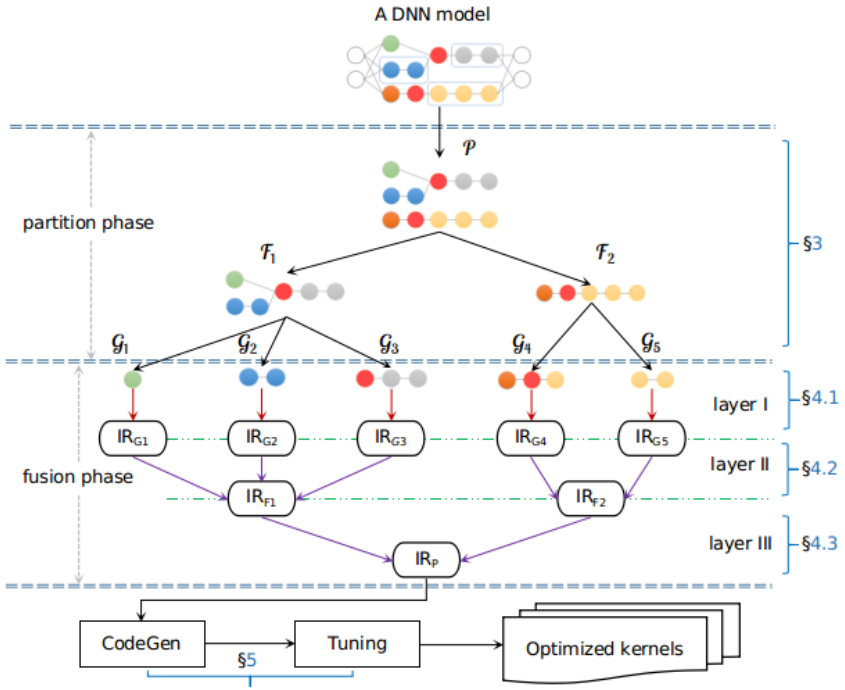
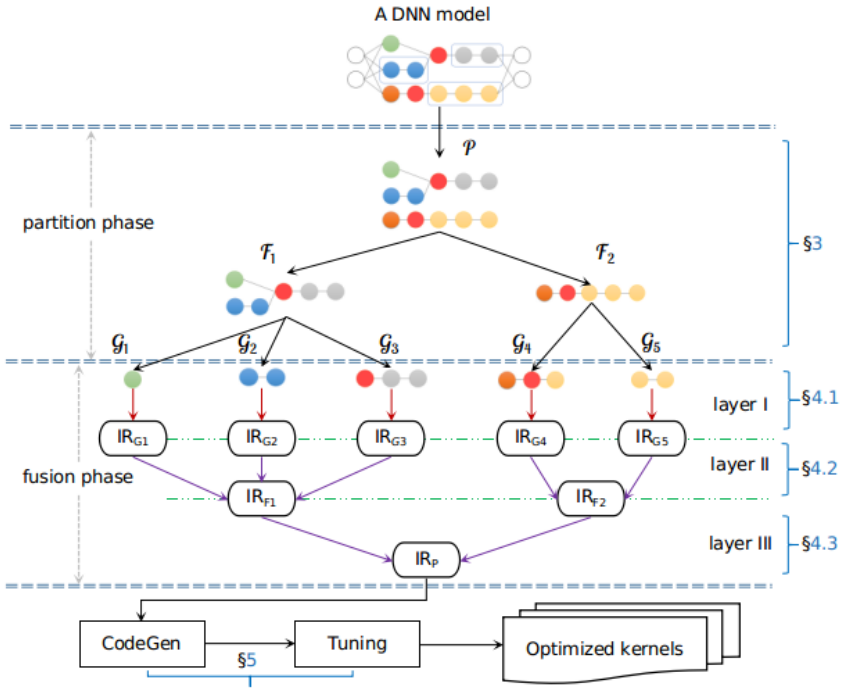


- The partition phase
- The fusion phase

Architecture of APOLLO



- The partition phase
  - considers compute-intensive operators (missed by XLA [5]);
- The fusion phase

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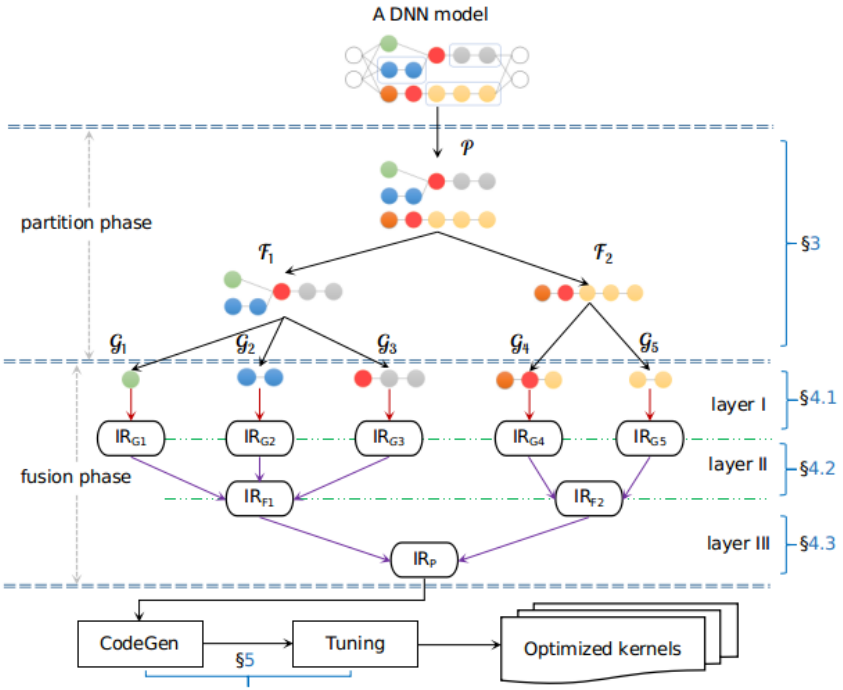

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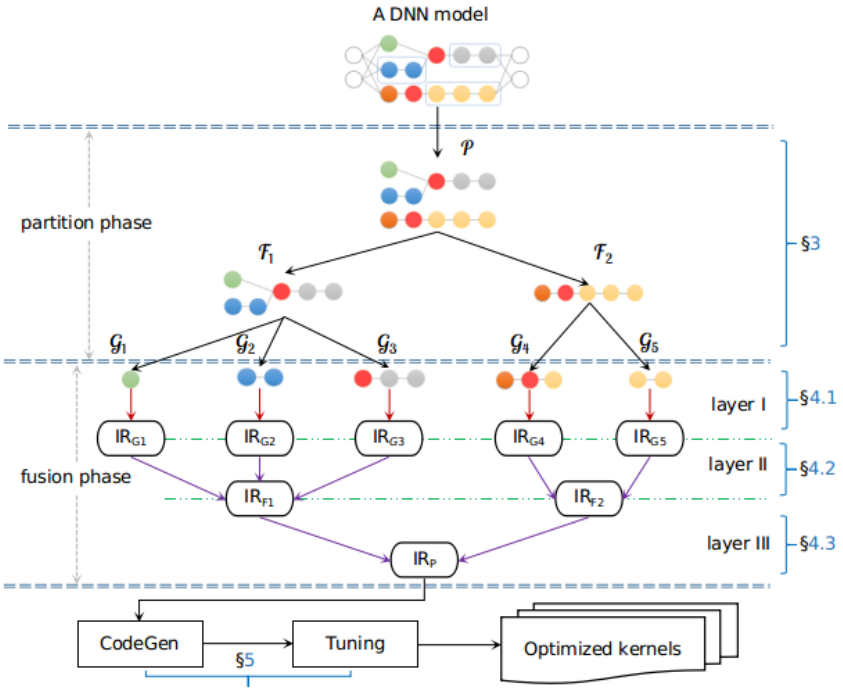

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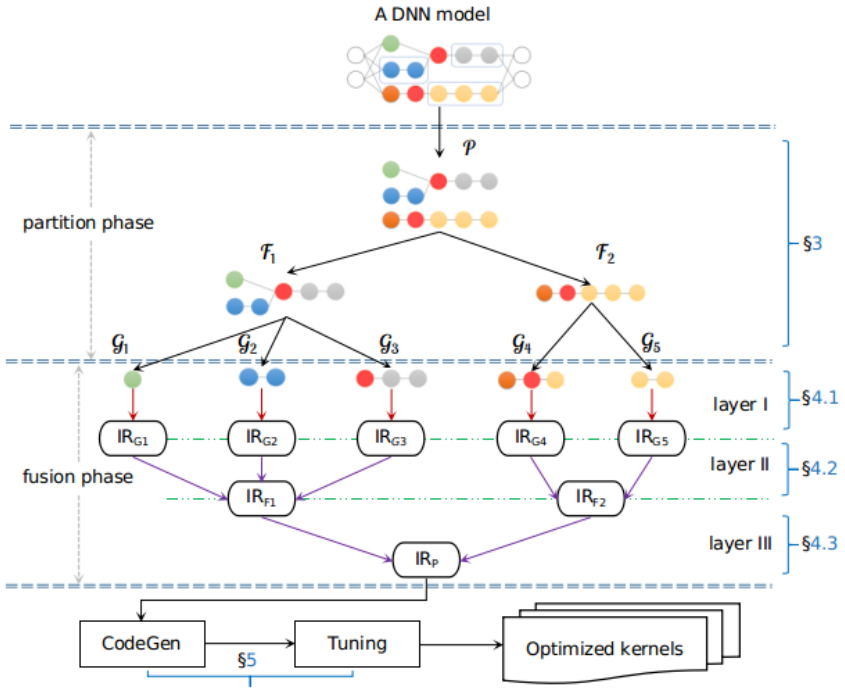

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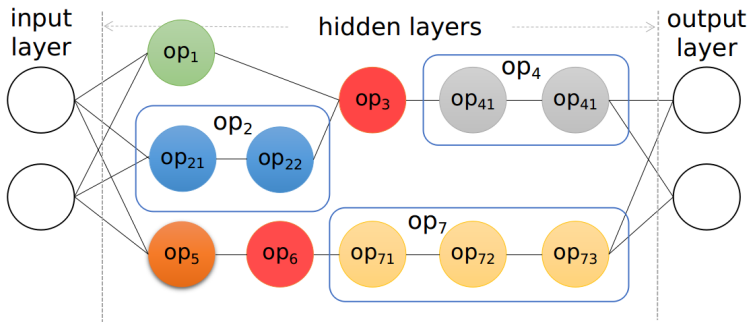
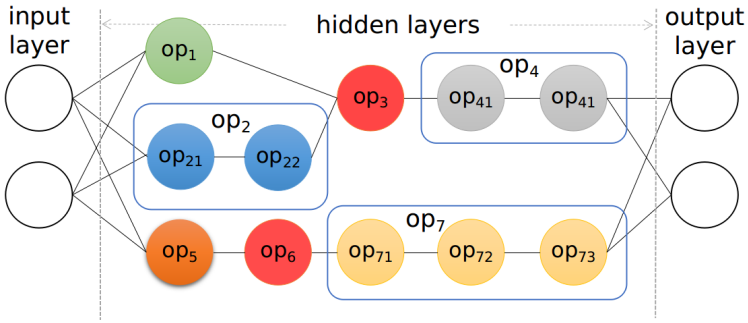
- The fusion phase
  - addresses the scalability issue of existing polyhedral compilers [16, 11];
  - goes beyond the recent works [8, 17] by enabling memory and parallelism stitching for training workloads on a dedicated accelerator.

Graph Simplification and Extracting Sub-graph Cluster $\mathcal{P}$



Graph Simplification and Extracting Sub-graph Cluster $\mathcal{P}$



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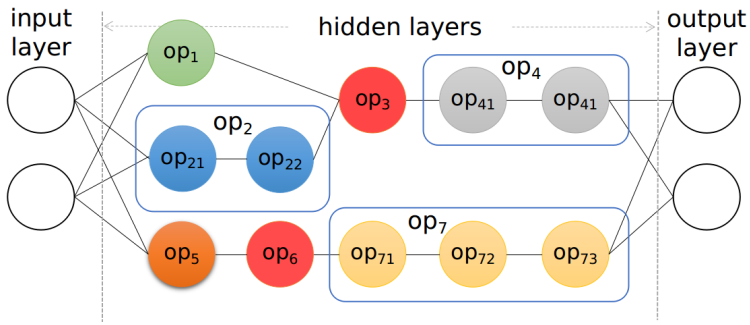

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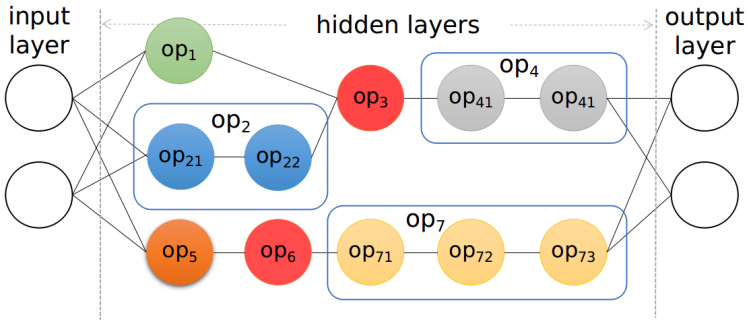

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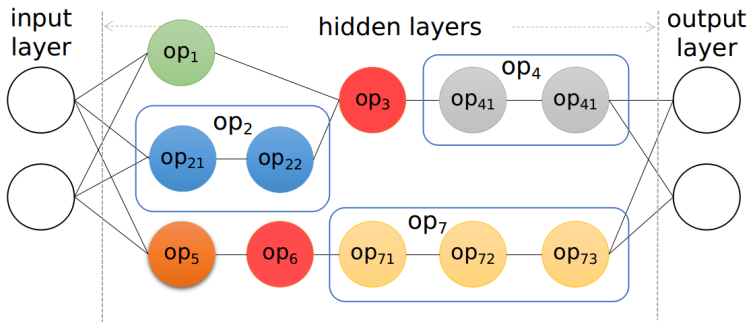

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  - user-defined and/or extraordinary operators with complex computational logic, e.g., `all-reduce` used in training speech recognition.
  - control flow operators like TensorFlow's `RefSwitch`.

Opening Compound Operators within each Sub-graph $\mathcal{F}_x$

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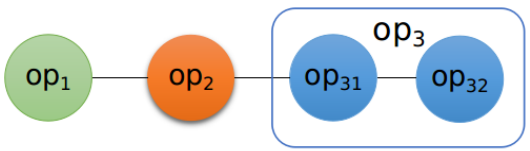

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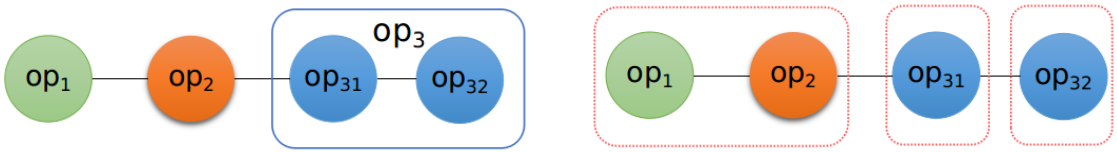

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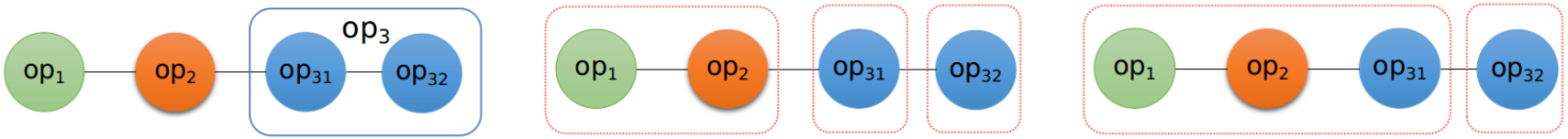

Merging Primitive Operators within each Micro-graph $\mathcal{G}_y$

- A micro-graph $\mathcal{G}_y$ is built by merging primitive operators using rules.

Rules	$\mathcal{G}_p$	$\mathcal{G}_c$	$\mathcal{G}_a$
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❻-matmul	matmul	element-wise	matmul
❻-matmul	element-wise	matmul	matmul
❻-conv	conv	element-wise	conv
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- These rules do not need to cover all composition patterns of operators, since some pair of operators should not be fused.

Polyhedral Loop Fusion and its Scalability within a $\mathcal{G}_y$

- A $\mathcal{G}_y$ is converted into a sequence of loop nests and used to produce a single kernel through our prior polyhedral loop optimizer AKG [16].

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    a(i,j)=a(i,j)+bias; //$S_1$
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- We design and implement a framework called PANAMERA [14] to optimize a reduction not fused with its follow-up elementwise operators.

Memory Stitching between multiple $\mathcal{G}_y$'s

- Micro-graphs often end with reductions. We define complementary rules to exploit the stitching possibilities between them.

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- Canonicalizing reductions guarantees the matching between the loop dimensions of two $\mathcal{G}_y$'s that are to be stitched in faster memory.

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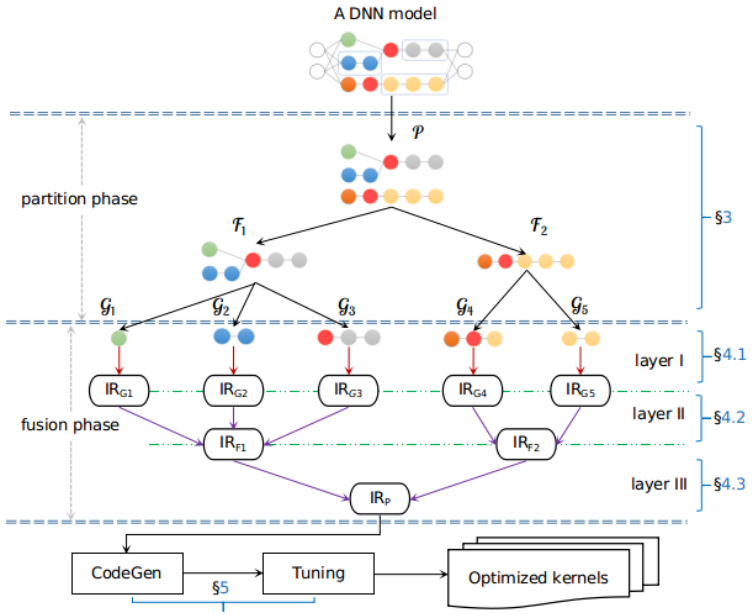
- A compute-intensive operator is excluded in such a traverse, since its huge amount of data usually consumes up the hardware resources.

Putting It All Together



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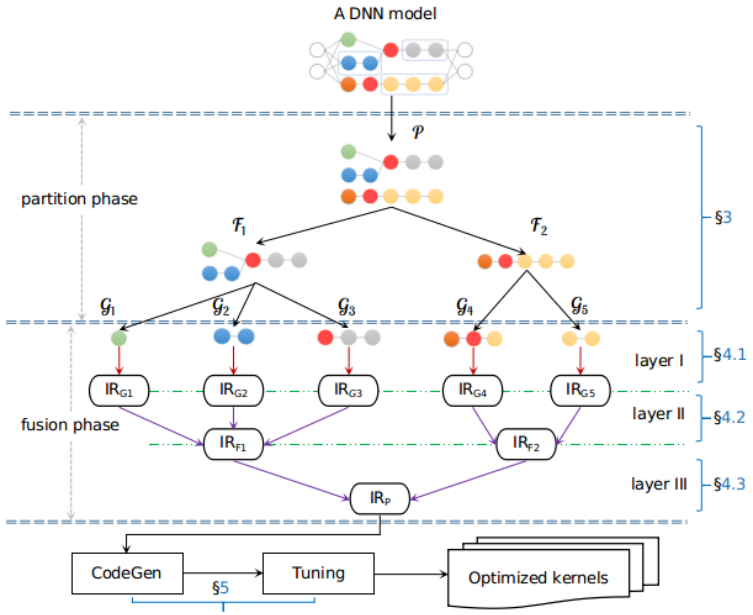

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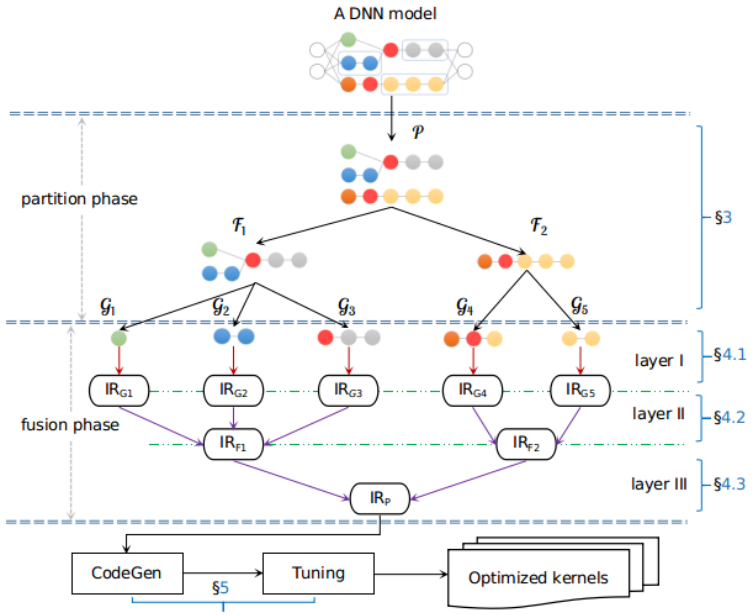

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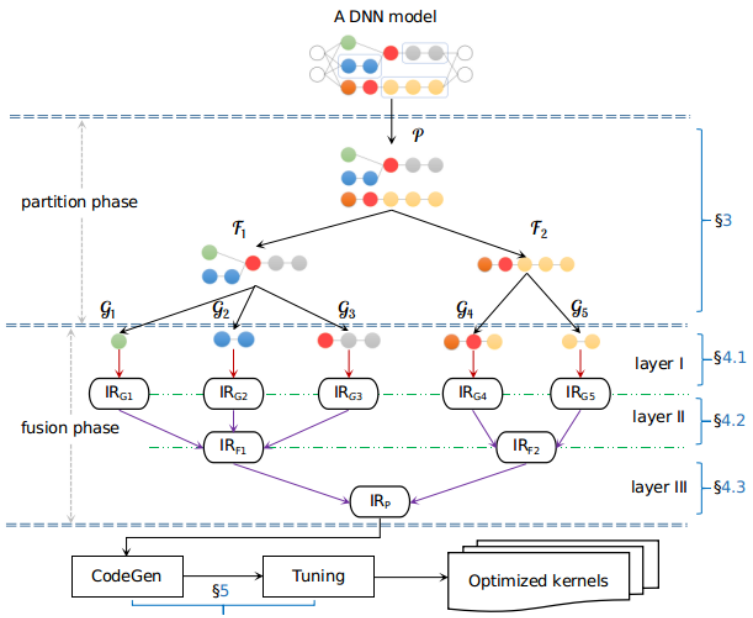

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- **Auto-tuning**: APOLLO captures the loop composition of a $\mathcal{G}_x$ that are prevented from parallelization by Cost Model (3) of the paper.
- **Piecewise compilation** is performed alongthe red/violet arrows, further reducing compilation overhead.
- **Code generation** supports both GPUs and Huawei Ascend 910 chips [7].

Results on Single GPU

- Experiments are conducted using five training workloads.
- Generated CUDA code on GPUs is executed using CUDA Toolkit 10.1 with -O3 enabled.
- Generated CCE code on Ascend 910 is executed using the later's native compiler.
- The geometric mean of 10 executions is reported.
- Case study on sub-graphs, results of inference workloads and compilation overhead are reported in the paper.

Results on Single GPU

BT: BERT; TR: Transformer; WD: Wide&Deep; YO: Yolo-v3; FM: DeepFM; b.s.: batch sizes; TF: TensorFlow; MS: MindSpore; imp.: improvements

models	b.s.	TF	XLA/TF	MS	APOLLO/MS	imp.
BT-base	32	167	**105%**	135	**252%**	**39%**
	64	200.8	**129%**	183.6	**212%**	**23%**
TR	8	6750	**16%**	5122	**84%**	**20%**
	16	9500	**11%**	10868	**59%**	**64%**
WD	16000	1133696	**15%**	762086	**123%**	**48%**
	32000	1470221	**5%**	836820	**121%**	**20%**
YO	4	33.11	**15%**	39.48	**46%**	**51%**
	8	56.00	**12%**	75.01	**10%**	**31%**
FM	8192	26117	**-1%**	479744	**151%**	-
	16384	30279	**-2%**	543024	**167%**	-

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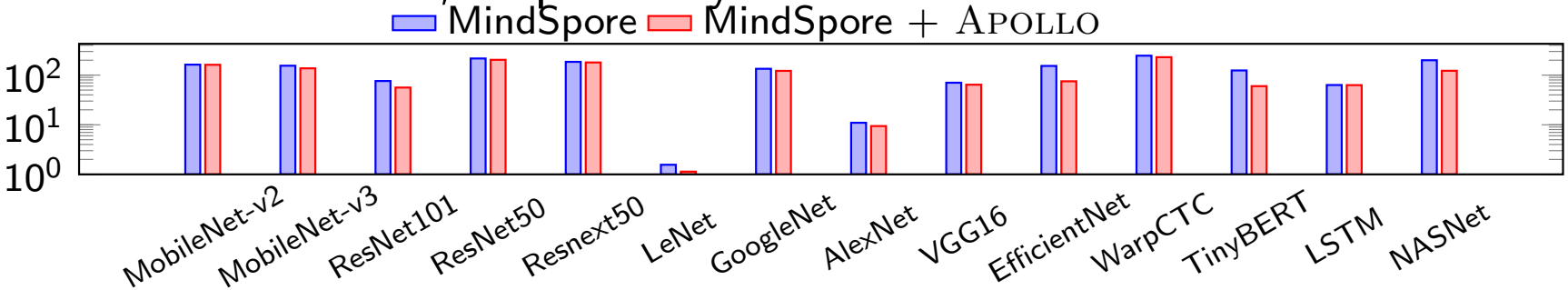

Execution times of MindSpore's model zoo (y axis: log scaled time in ms; lower is better). On average, APOLLO improves MindSpore by 29.6%.

Results on Multiple GPUs

BT: BERT; WD: Wide&Deep; FM: DeepFM; batch sizes in parenthesis; TF: TensorFlow; MS: MindSpore; imp.: improvements

models	GPUs	TF	XLA/TF	MS	APOLLO/MS	*imp.*
BT-base(32)	8	1244.9	**96%**	944.4	**247%**	**34%**
BT-base(64)	8	1555.4	**117%**	1333.1	**222%**	**27%**
BT-large(4)	4	66.94	**33%**	37.62	**133%**	**-2%**
WD(16000)	8	8086178	**1%**	4964319	**87%**	**13%**
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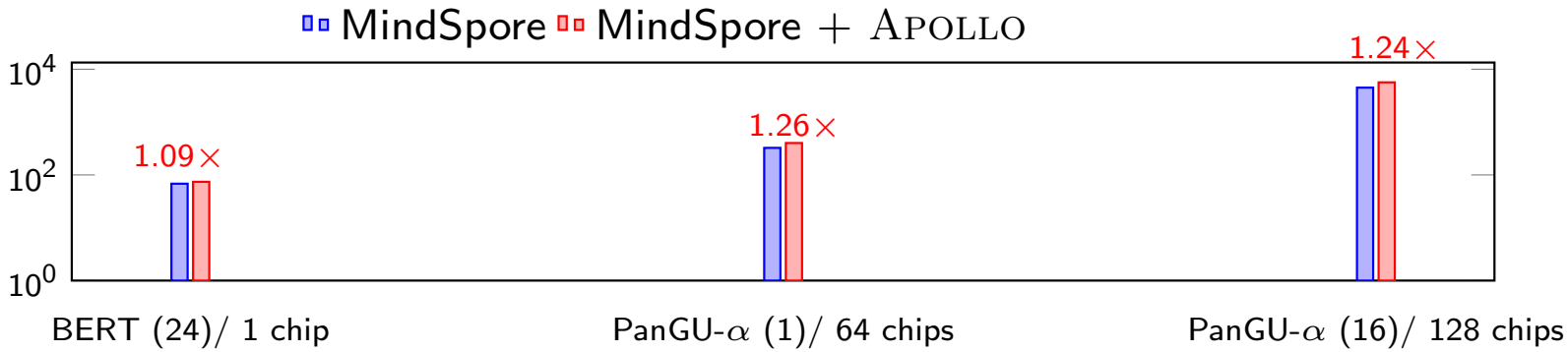
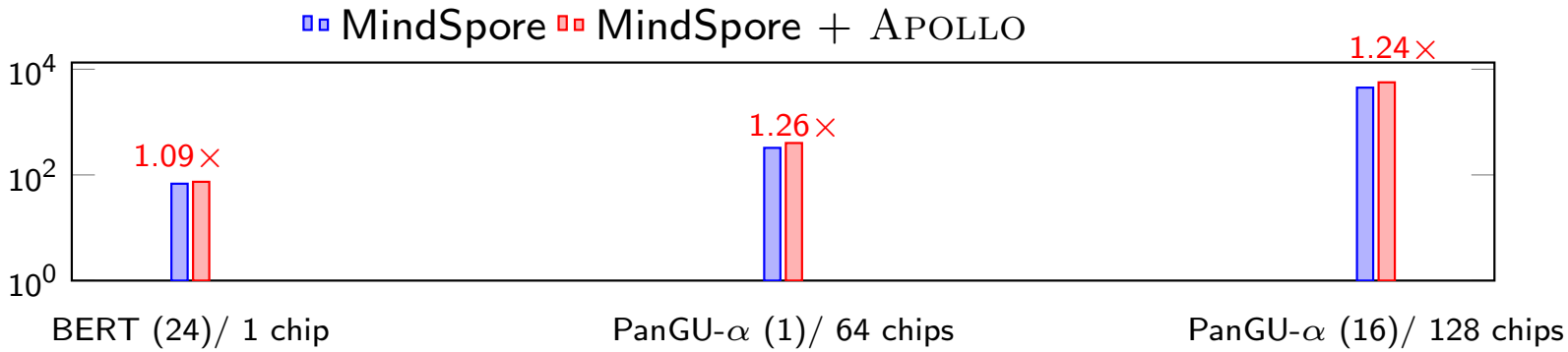
- The throughput of MindSpore falls behind, sometimes significantly, than those of TensorFlow and XLA, but it outperforms the latter two by 1.96× and 1.18×, respectively.

Results on Ascend 910 chips



Throughput of BERT and PanGu-α [13] (examples/s) on Ascend. Batch sizes are in parentheses. Higher is better.

Results on Ascend 910 chips



Throughput of BERT and PanGu-α [13] (examples/s) on Ascend. Batch sizes are in parentheses. Higher is better.

- APOLLO brings about a mean improvement of 19.7% over MindSpore when targeting Ascend 910 chips.

Summary of the Contributions

- APOLLO extends the search space of fusion by considering more operator types, generating more profitable across-layer schedules originally hindered by operator boundaries;

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- APOLLO extends the search space of fusion by considering more operator types, generating more profitable across-layer schedules originally hindered by operator boundaries;
- APOLLO addresses the scalability issue of fusion by allowing reverse feedback from the operator-level optimizer, achieving a fully automatic fusion framework;
- APOLLO enhances the performance of deep learning workloads by modeling both data locality and parallelism, producing more efficient code than the state of the art;
- APOLLO exhibits reasonable JIT compilation overhead, demonstrating its effectiveness using rather difficult real-life training workloads.

References

[1] Abadi, M., Barham, P., Chen, J., Chen, Z., Davis, A., Dean, J., Devin, M., Ghemawat, S., Irving, G., Isard, M., Kudlur, M., Levenberg, J., Monga, R., Moore, S., Murray, D. G., Steiner, B., Tucker, P., Vasudevan, V., Warden, P., Wicke, M., Yu, Y., and Zheng, X.
Tensorflow: A system for large-scale machine learning.
In *Proceedings of the 12th USENIX Conference on Operating Systems Design and Implementation* (Berkeley, CA, USA, 2016), OSDI'16, USENIX Association, pp. 265–283.

[2] Baghdadi, R., Ray, J., Romdhane, M. B., Del Sozzo, E., Akkas, A., Zhang, Y., Suriana, P., Kamil, S., and Amarasinghe, S.
Tiramisu: A polyhedral compiler for expressing fast and portable code.
In *Proceedings of the 2019 IEEE/ACM International Symposium on Code Generation and Optimization* (Piscataway, NJ, USA, 2019), CGO 2019, IEEE Press, pp. 193–205.

[3] Chen, T., Moreau, T., Jiang, Z., Zheng, L., Yan, E., Cowan, M., Shen, H., Wang, L., Hu, Y., Ceze, L., Guestrin, C., and Krishnamurthy, A.
Tvm: An automated end-to-end optimizing compiler for deep learning.
In *Proceedings of the 12th USENIX Conference on Operating Systems Design and Implementation* (Berkeley, CA, USA, 2018), OSDI'18, USENIX Association, pp. 579–594.

[4] Cyphers, S., Bansal, A. K., Bhiwandiwalla, A., Bobba, J., Brookhart, M., Chakraborty, A., Constable, W., Convey, C., Cook, L., Kanawi, O., Kimball, R., Knight, J., Korovaiko, N., Kumar, V., Lao, Y., Lishka, C. R., Menon, J., Myers, J., Narayana, S. A., Procter, A., and Webb, T. J.
Intel ngraph: An intermediate representation, compiler, and executor for deep learning, 2018.

[5] Google.
Xla: Optimizing compiler for machine learning, 2017.

[6] Jia, Z., Padon, O., Thomas, J., Warszawski, T., Zaharia, M., and Aiken, A.
Taso: Optimizing deep learning computation with automatic generation of graph substitutions.
In *Proceedings of the 27th ACM Symposium on Operating Systems Principles* (New York, NY, USA, 2019), SOSP'19, ACM, pp. 47–62.

References

[7] Liao, H., Tu, J., Xia, J., Liu, H., Zhou, X., Yuan, H., and Hu, Y.
Ascend: a scalable and unified architecture for ubiquitous deep neural network computing : Industry track paper.
In *2021 IEEE International Symposium on High-Performance Computer Architecture (HPCA)* (2021), pp. 789–801.

[8] Ma, L., Xie, Z., Yang, Z., Xue, J., Miao, Y., Cui, W., Hu, W., Yang, F., Zhang, L., and Zhou, L.
Rammer: Enabling holistic deep learning compiler optimizations with rtasks.
In *14th USENIX Symposium on Operating Systems Design and Implementation (OSDI 20)* (Nov. 2020), USENIX Association, pp. 881–897.

[9] Mehta, S., Lin, P.-H., and Yew, P.-C.
Revisiting loop fusion in the polyhedral framework.
In *Proceedings of the 19th ACM SIGPLAN Symposium on Principles and Practice of Parallel Programming* (New York, NY, USA, 2014), PPoPP'14, ACM, pp. 233–246.

[10] Paszke, A., Gross, S., Massa, F., Lerer, A., Bradbury, J., Chanan, G., Killeen, T., Lin, Z., Gimelshein, N., Antiga, L., Desmaison, A., Kopf, A., Yang, E., DeVito, Z., Raison, M., Tejani, A., Chilamkurthy, S., Steiner, B., Fang, L., Bai, J., and Chintala, S.
Pytorch: An imperative style, high-performance deep learning library.
In *Advances in neural information processing systems* (2019), pp. 8026–8037.

[11] Vasilache, N., Zinenko, O., Theodoridis, T., Goyal, P., Devito, Z., Moses, W. S., Verdoolaege, S., Adams, A., and Cohen, A.
The next 700 accelerated layers: From mathematical expressions of network computation graphs to accelerated gpu kernels, automatically.
ACM Trans. Archit. Code Optim. 16, 4 (Oct. 2019).

[12] Wei, R., Schwartz, L., and Adve, V.
Dlvm: A modern compiler infrastructure for deep learning systems, 2018.

References

[13] Zeng, W., Ren, X., Su, T., Wang, H., Liao, Y., Wang, Z., Jiang, X., Yang, Z., Wang, K., Zhang, X., Li, C., Gong, Z., Yao, Y., Huang, X., Wang, J., Yu, J., Guo, Q., Yu, Y., Zhang, Y., Wang, J., Tao, H., Yan, D., Yi, Z., Peng, F., Jiang, F., Zhang, H., Deng, L., Zhang, Y., Lin, Z., Zhang, C., Zhang, S., Guo, M., Gu, S., Fan, G., Wang, Y., Jin, X., Liu, Q., and Tian, Y.
Pangu-α: Large-scale autoregressive pretrained chinese language models with auto-parallel computation, 2021.

[14] Zhao, J., Bastoul, C., Yi, Y., Hu, J., Nie, W., Zhang, R., Geng, Z., Li, C., Tachon, T., and Gan, Z.
Parallelizing neural network models effectively on gpu by implementing reductions atomically.
In *Proceedings of the 31st International Conference on Parallel Architectures and Compilation Techniques* (2022), PACT'22, ACM.

[15] Zhao, J., and Di, P.
Optimizing the memory hierarchy by compositing automatic transformations on computations and data.
In *Proceedings of the 53rd IEEE/ACM International Symposium on Microarchitecture* (Piscataway, NJ, USA, 2020), MICRO-53, IEEE Press, pp. 427–441.

[16] Zhao, J., Li, B., Nie, W., Geng, Z., Zhang, R., Gao, X., Cheng, B., Wu, C., Cheng, Y., Li, Z., Di, P., Zhang, K., and Jin, X.
Akg: Automatic kernel generation for neural processing units using polyhedral transformations.
In *Proceedings of the 42nd ACM SIGPLAN International Conference on Programming Language Design and Implementation* (New York, NY, USA, 2021), PLDI 2021, Association for Computing Machinery, pp. 1233–1248.

[17] Zheng, Z., Zhao, P., Long, G., Zhu, F., Zhu, K., Zhao, W., Diao, L., Yang, J., and Lin, W.
Fusionstitching: Boosting memory intensive computations for deep learning workloads, 2020.

Questions & Answers

Scan the QR code to obtain the paper/code repository/artifact.

Thank you!

Any Questions?

DietCode: Automatic Optimization for Dynamic Tensor Programs

- Bojian Zheng *
- Ziheng Jiang
- Cody Hao Yu
- Haichen Shen
- Joshua Fromm
- Yizhi Liu
- Yida Wang
- Luis Ceze
- Tianqi Chen
- Gennady Pekhimenko

MLSys 2022

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DietCode: Automatic Code Generation for Dynamic Tensor Programs

Bojian Zheng[1, 2, 3 *], Ziheng Jiang[4 *], Cody Yu[2], Haichen Shen[2],
Josh Fromm[5], Yizhi Liu[2], Yida Wang[2],
Luis Ceze[5, 6], Tianqi Chen[5, 7], Gennady Pekhimenko[1, 2, 3]

[*] Equal Contributions

1 

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7 

Executive Summary

- Challenges posed by dynamic-shape workloads:
  - Vendor Libraries: Hard to be Engineered for Efficiency
  - Existing Auto-Schedulers: Long Compilation Time (**days** for a single operator)
- *DietCode* addresses the challenges with
  ① shape-generic search space
  ② micro-kernel-based cost model.
- Key Results:
  - Compilation Time: $\mathbf{5.88}\times$ saving vs. Ansor.
  - Performance: Up to $\mathbf{1.70}\times$ better vs. Ansor and $\mathbf{1.19}\times$ vs. the vendor library on modern GPUs.

Background: ML Framework Stack

Application

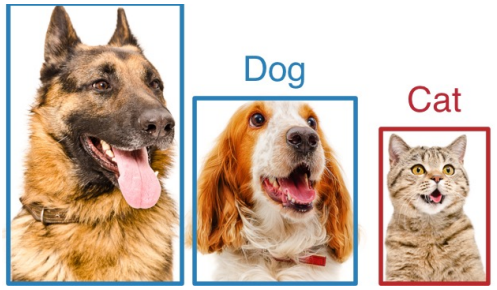
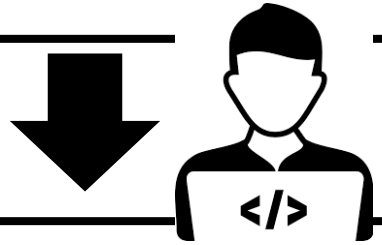


Image Classification[1]

Machine Translation[2]

Speech Recognition[3]



Framework

TensorFlow [4]

PyTorch [5]

[6]

[1] J. Guo et al. *GluonCV and GluonNLP*. JMLR 2020
[2] https://translate.google.com/
[3] https://github.com/NVIDIA/NeMo
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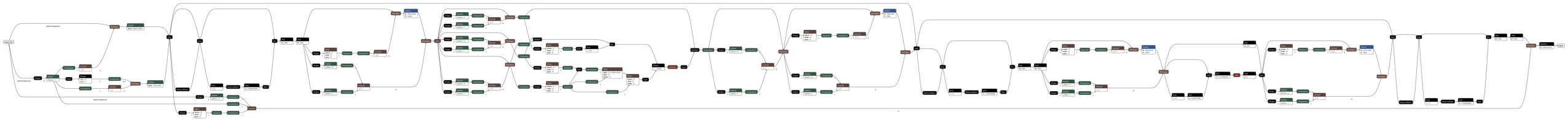
TensorFlow [4] PyTorch [5] [6]

Interpretation: Graph of Operators[7]



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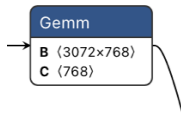
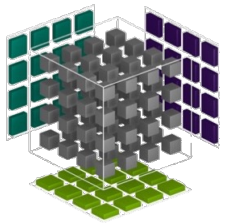


Operator
(Matrix Multiply)

Invoke

Vendor Libraries



cuBLAS[1]

[2]

Dispatcher

Built-in Kernel 2

Built-in Kernel 1

Hardware

NVIDIA GPU[3]

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[2] https://developer.nvidia.com/cudnn
[3] https://www.nvidia.com/en-us/data-center/tesla-t4/

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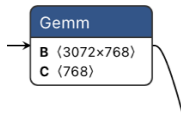

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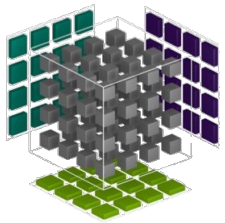

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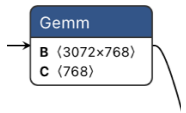

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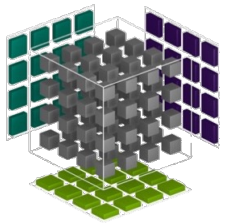

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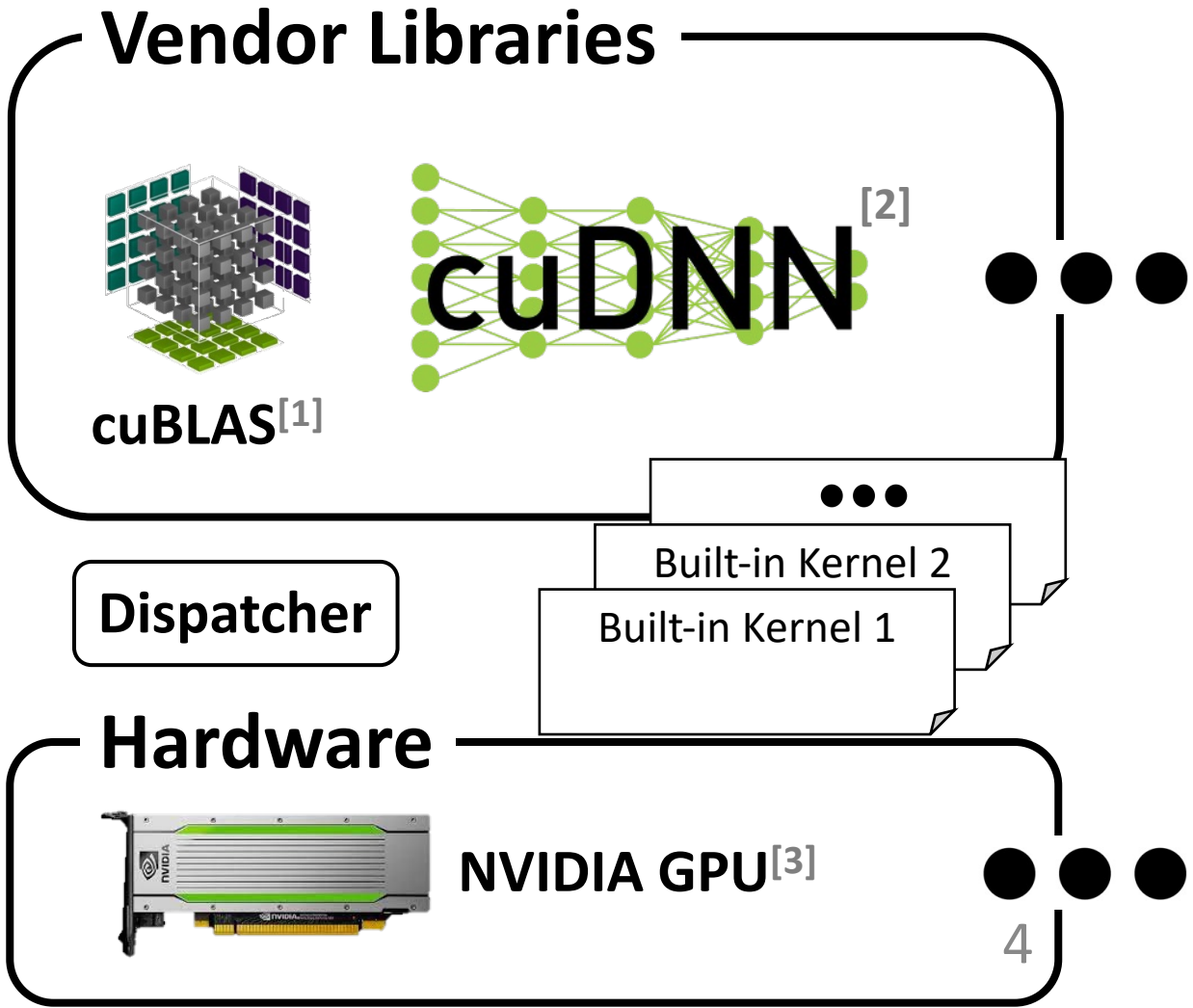
[3] https://www.nvidia.com/en-us/data-center/tesla-t4/

Background: Vendor Libraries

- Challenges
  - Performance of built-in kernels can be **suboptimal** on the given shapes or hardware[4, 5, 6, 7, 8, 9, …].
  - **Huge** engineering efforts and expertise required to tune for specific use cases.



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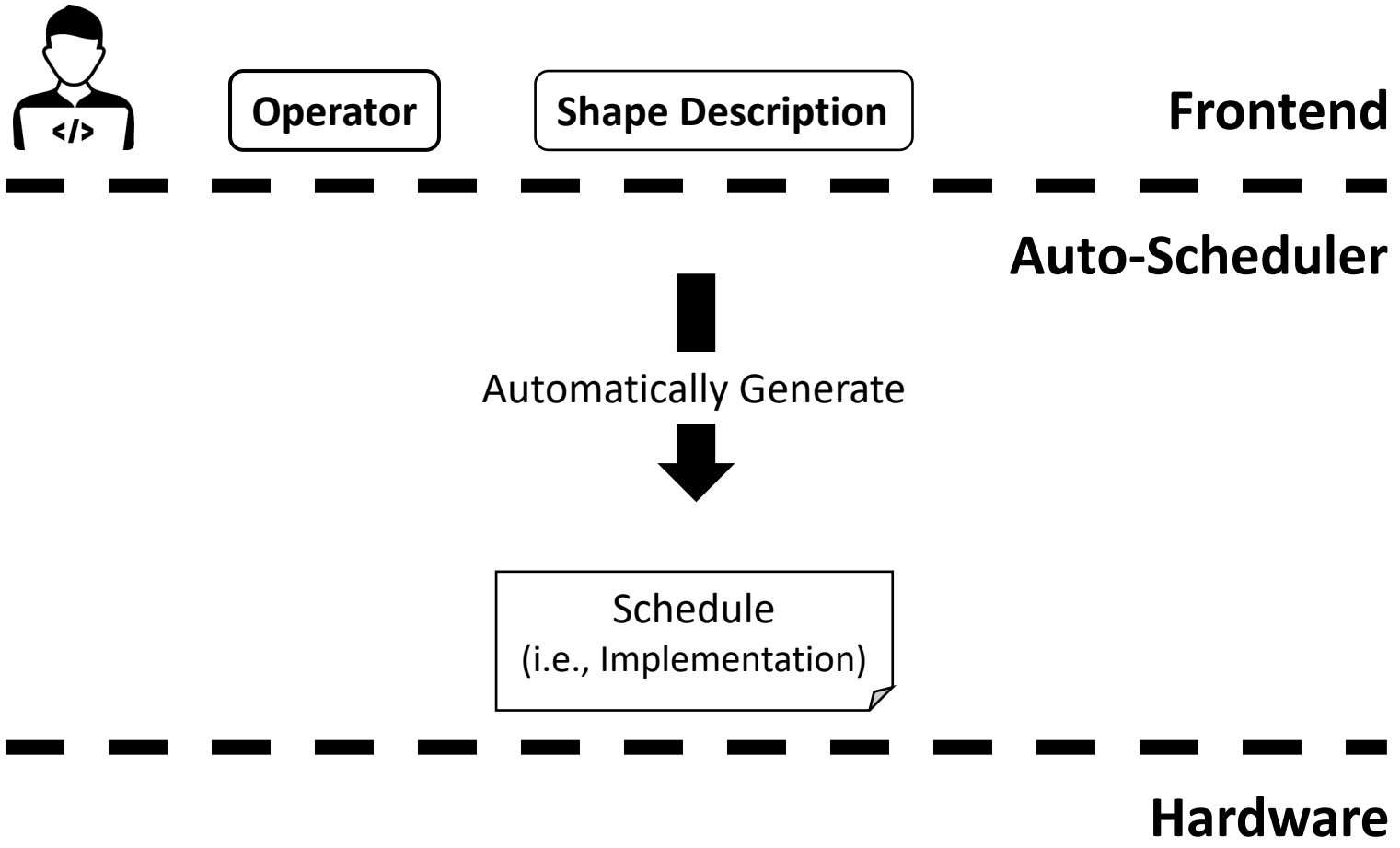
[5] N. Vasilache et al. *Tensor Comprehensions*. TACO 2019
[6] L. Zheng et al. *Ansor*. OSDI 2020
[7] F. Yu et al. *Towards Latency-aware DNN Optimization with GPU Runtime Analysis and Tail Effect Elimination*. arXiv 2020
[8] S. Feng, B. Hou et al. *TensorIR*. arXiv 2022
[9] https://tvm.apache.org/2018/03/23/nmt-transformer-optimize

Background: Auto-Scheduler [1, 2, 3, 4]

- **Objective**:



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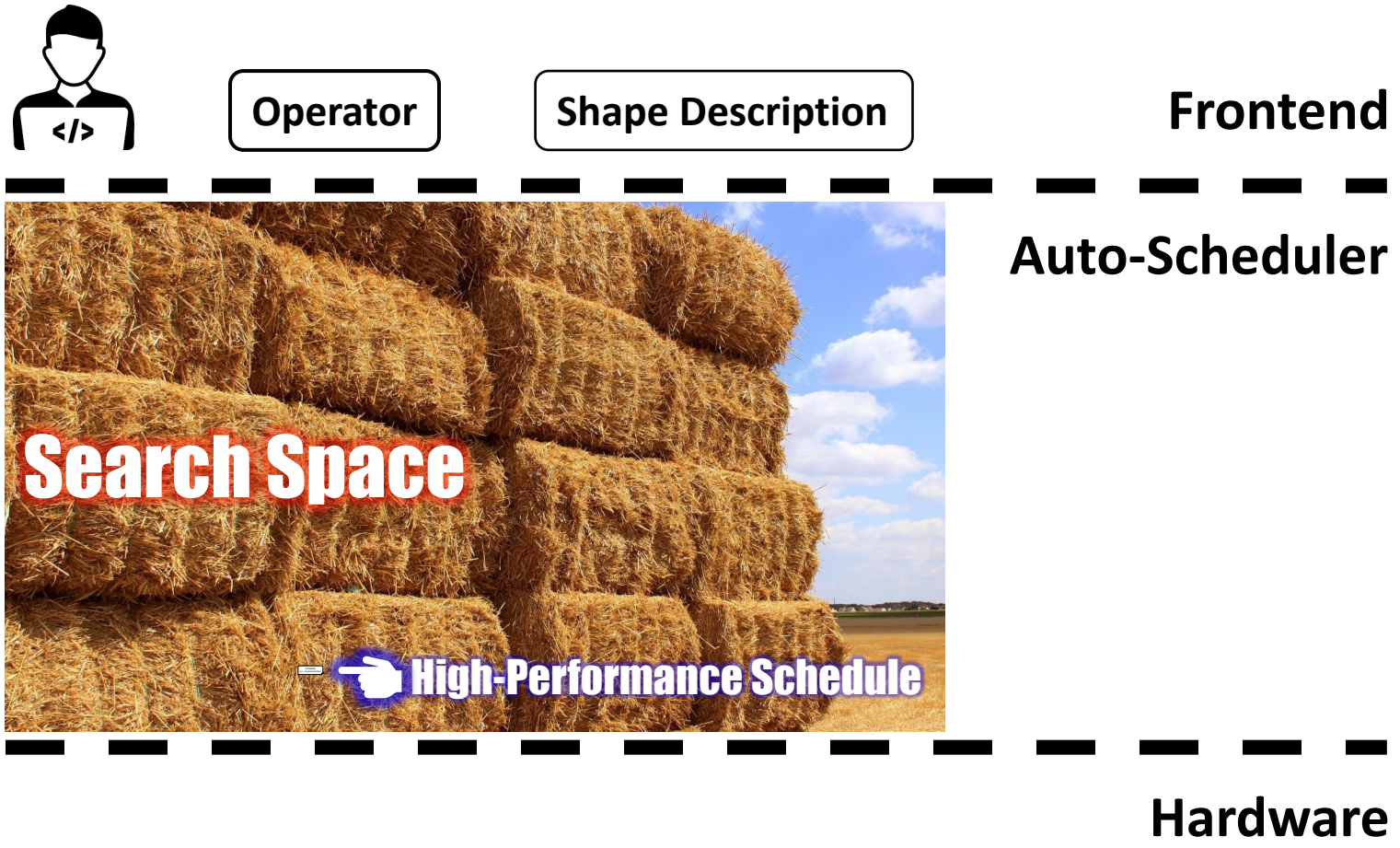

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[2] N. Vasilache et al. *Tensor Comprehensions*. TACO 2019
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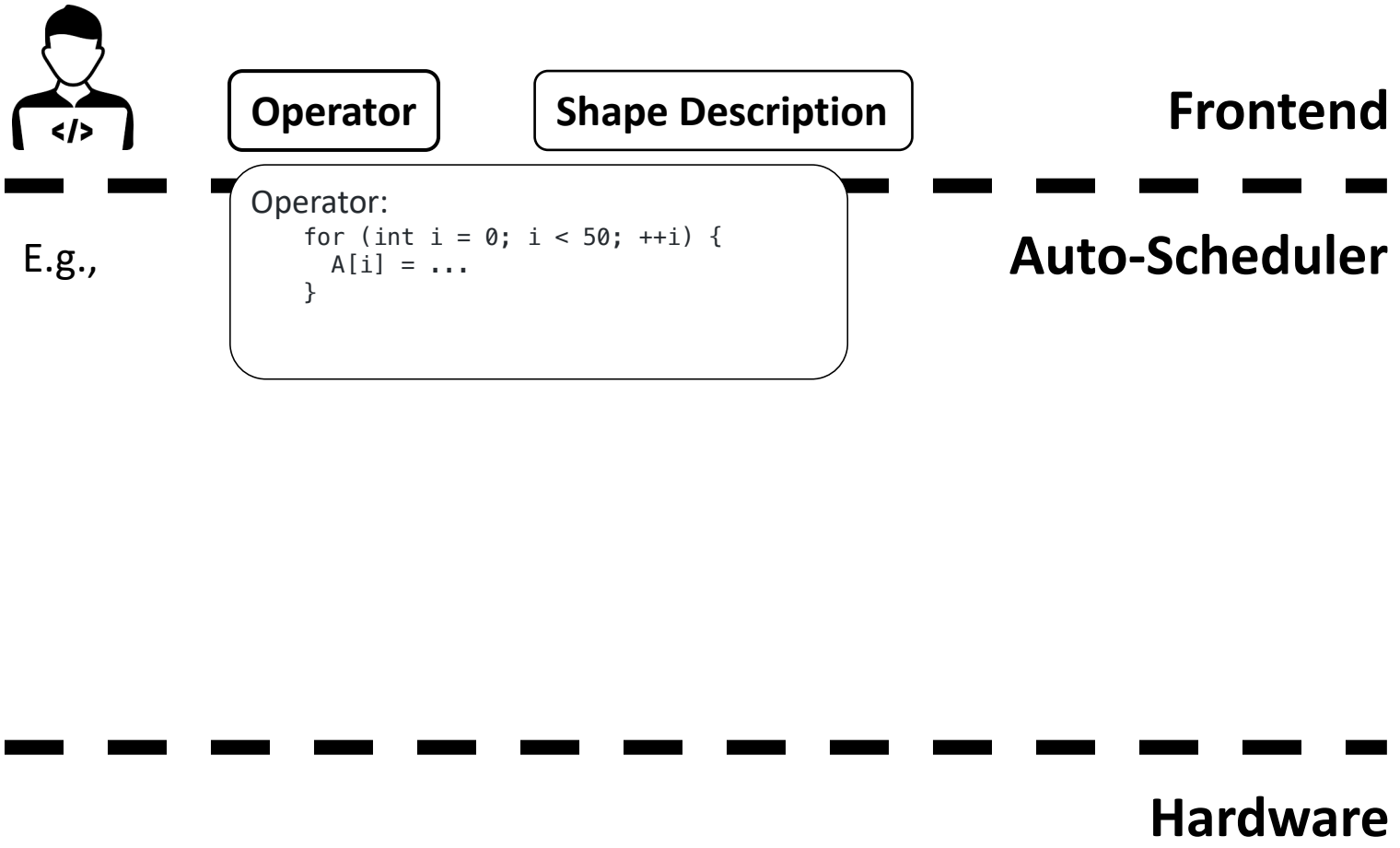
[4] S. Feng, B. Hou et al. *TensorIR*. arXiv 2022

Background: Auto-Scheduler [1, 2, 3, 4]



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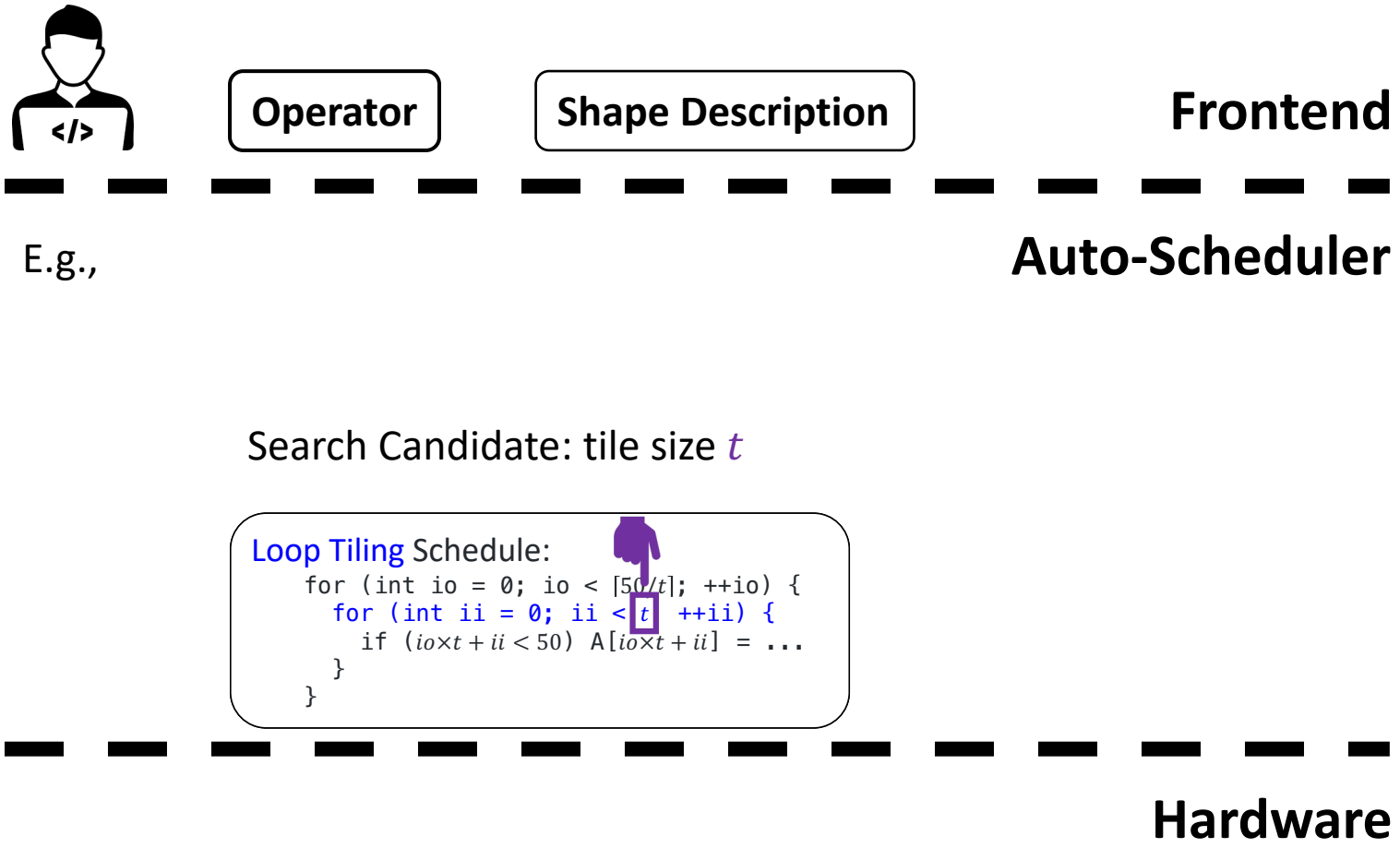

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Background: Auto-Scheduler [1, 2, 3, 4]

Operator **Shape Description** **Frontend**

E.g., **Auto-Scheduler**

Search Candidate: tile size $t \in [2, \infty)$

Search Techniques:
1. Shape-Dependent Search Space
2. Complete Program Cost Model

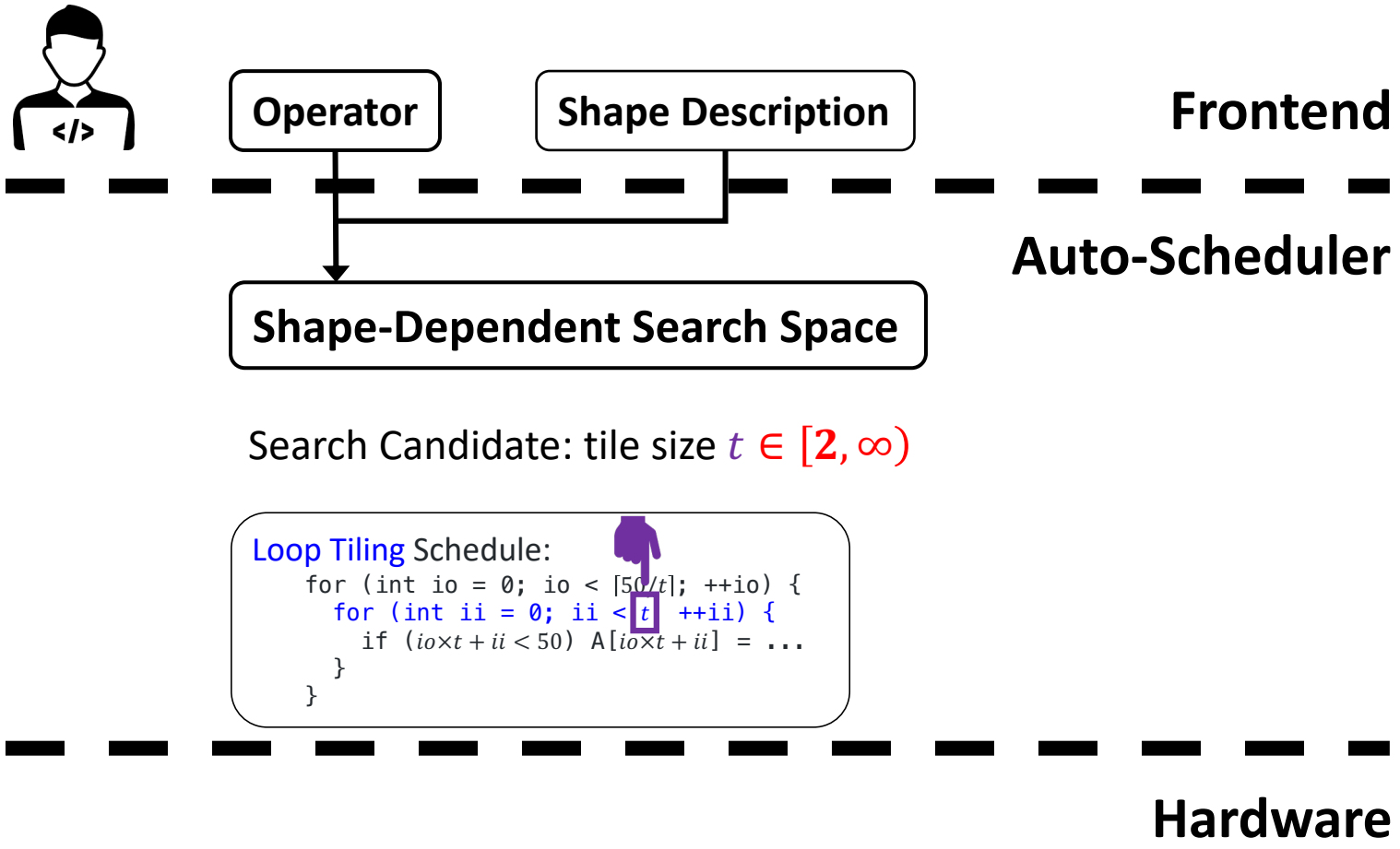
Loop Tiling Schedule:

```
for (int io = 0; io < [50/t]; ++io) {
  for (int ii = 0; ii < t; ++ii) {
    if (io×t + ii < 50) A[io×t + ii] = ...
  }
}
```

Hardware

[1] A. Adams et al. *Halide Auto-Scheduler*. SIGGRAPH 2019
[2] N. Vasilache et al. *Tensor Comprehensions*. TACO 2019
[3] L. Zheng et al. *Ansor*. OSDI 2020
[4] S. Feng, B. Hou et al. *TensorIR*. arXiv 2022

1. Shape-Dependent Search Space



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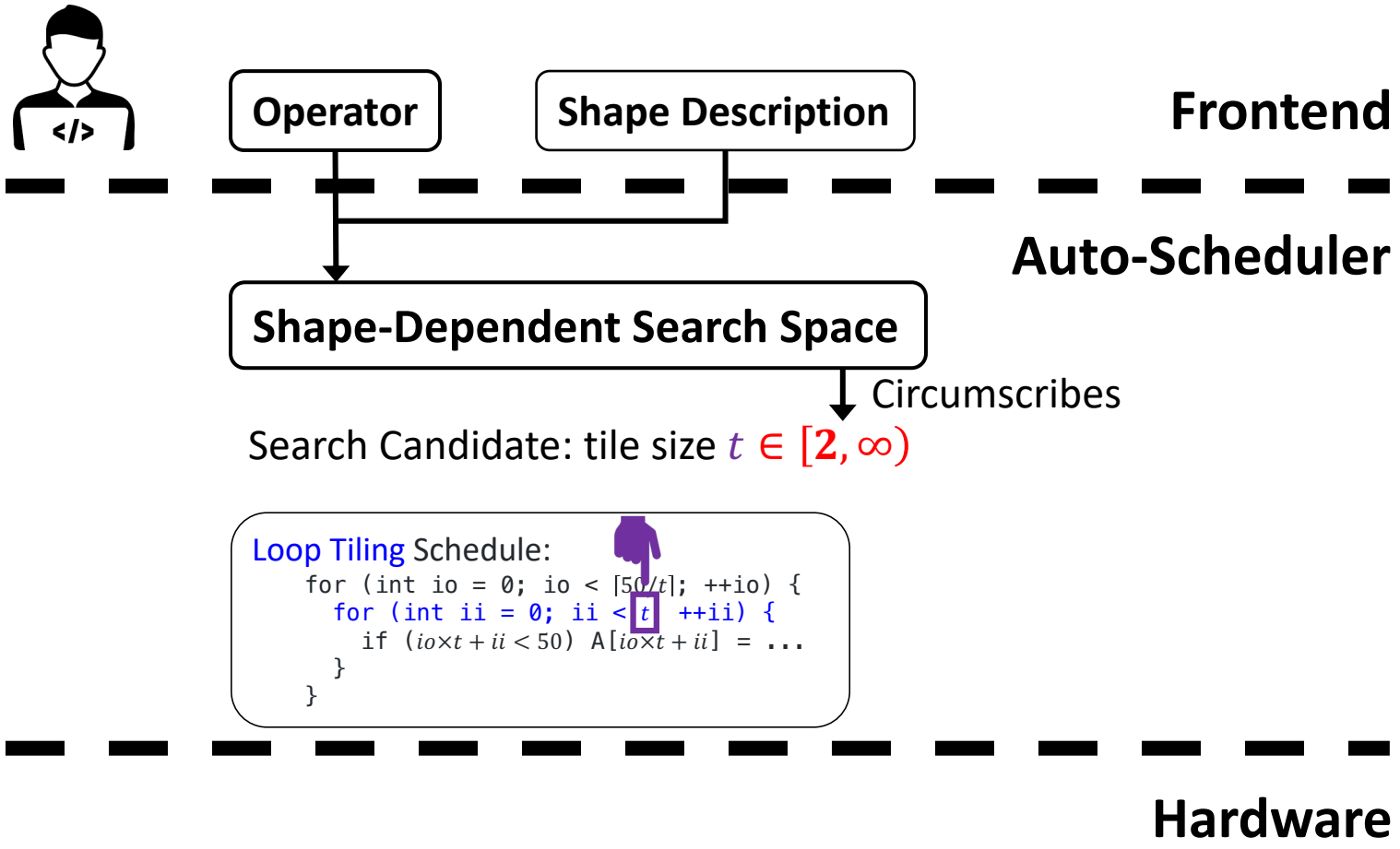

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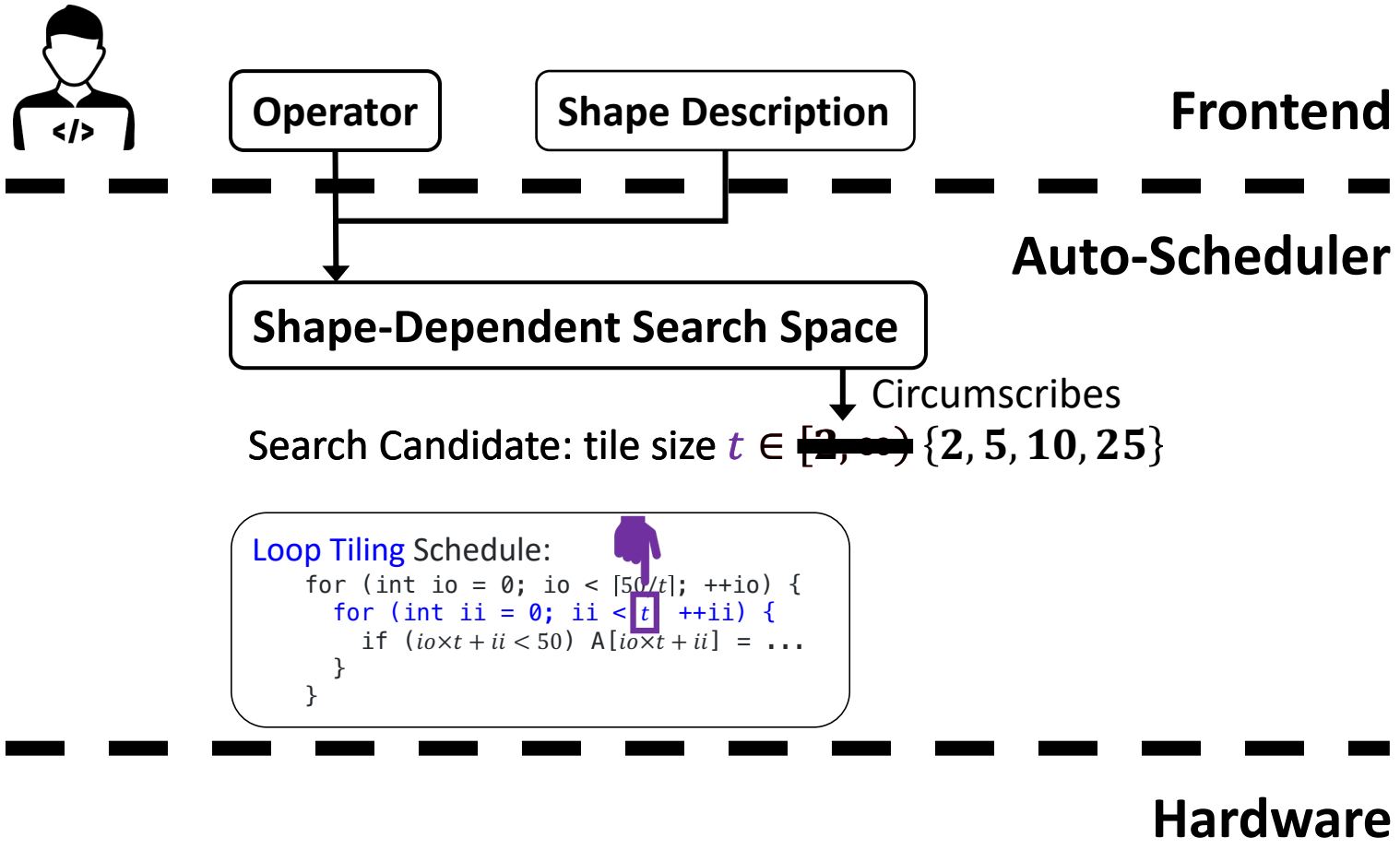
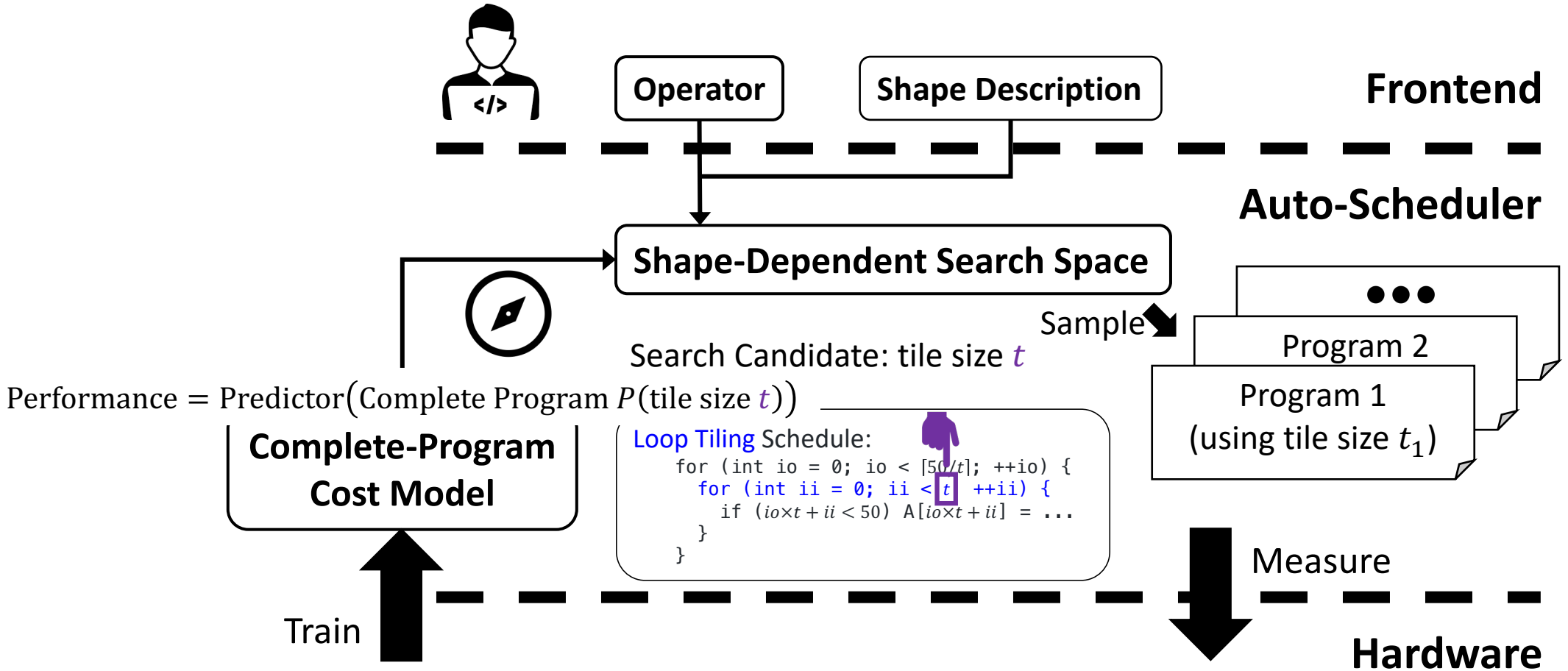
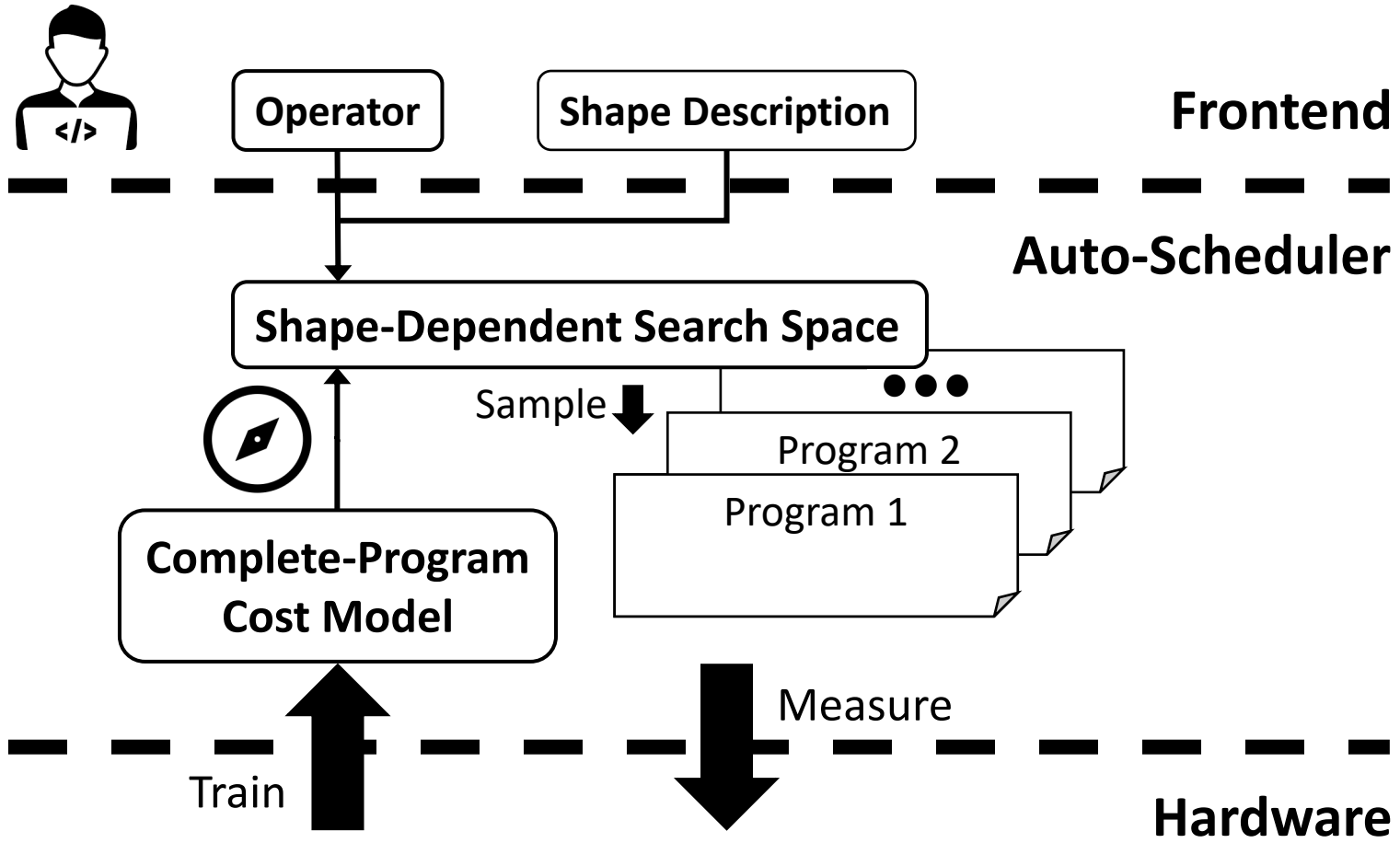


2. Complete Program Cost Model

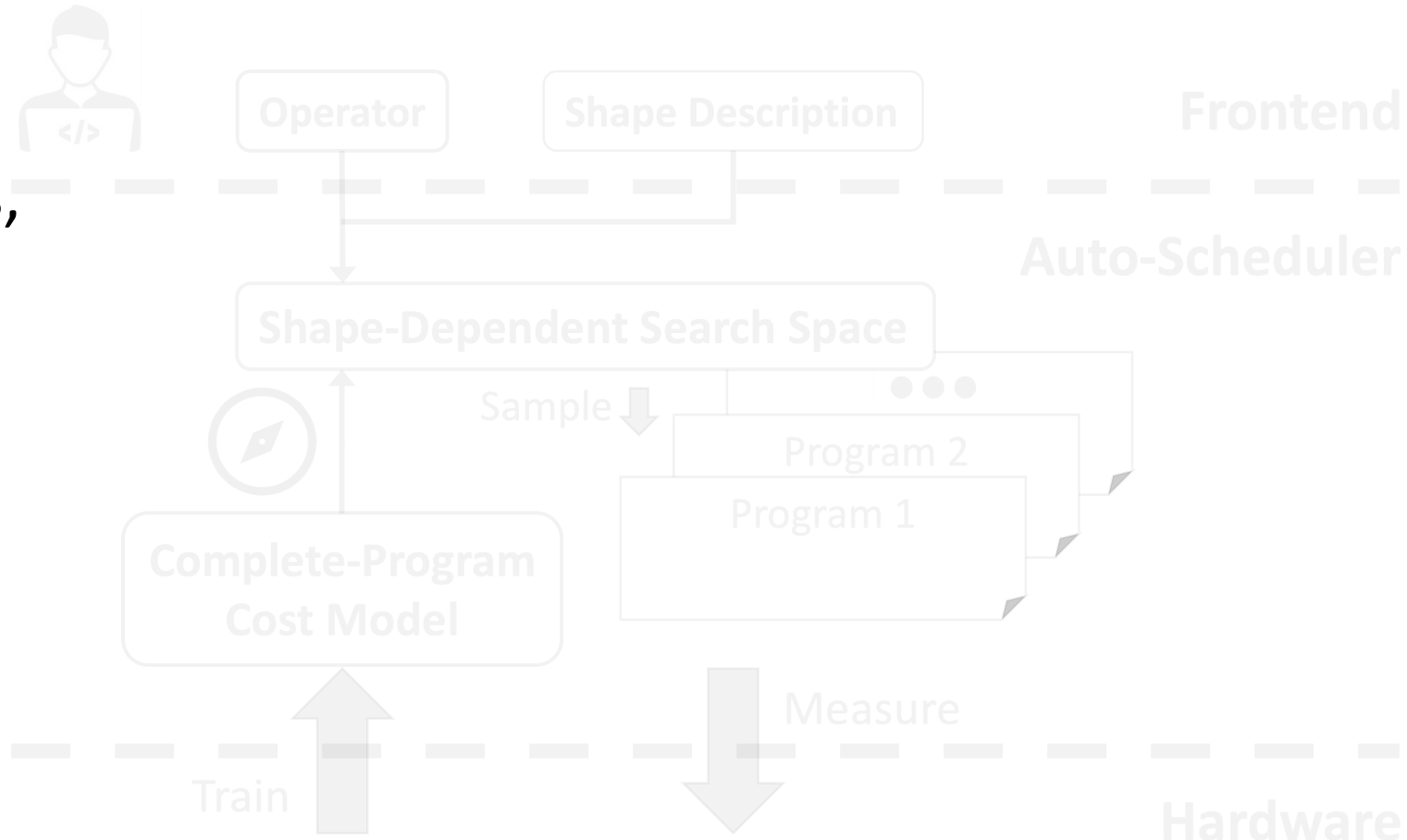


Challenges from Dynamic-Shape Workloads



Challenges from Dynamic-Shape Workloads

- **Cannot** efficiently handle **dynamic-shape** operators, common in

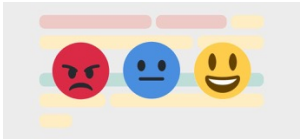


Challenges from Dynamic-Shape Workloads

- **Cannot** efficiently handle **dynamic-shape** operators, common in

Translation[1]

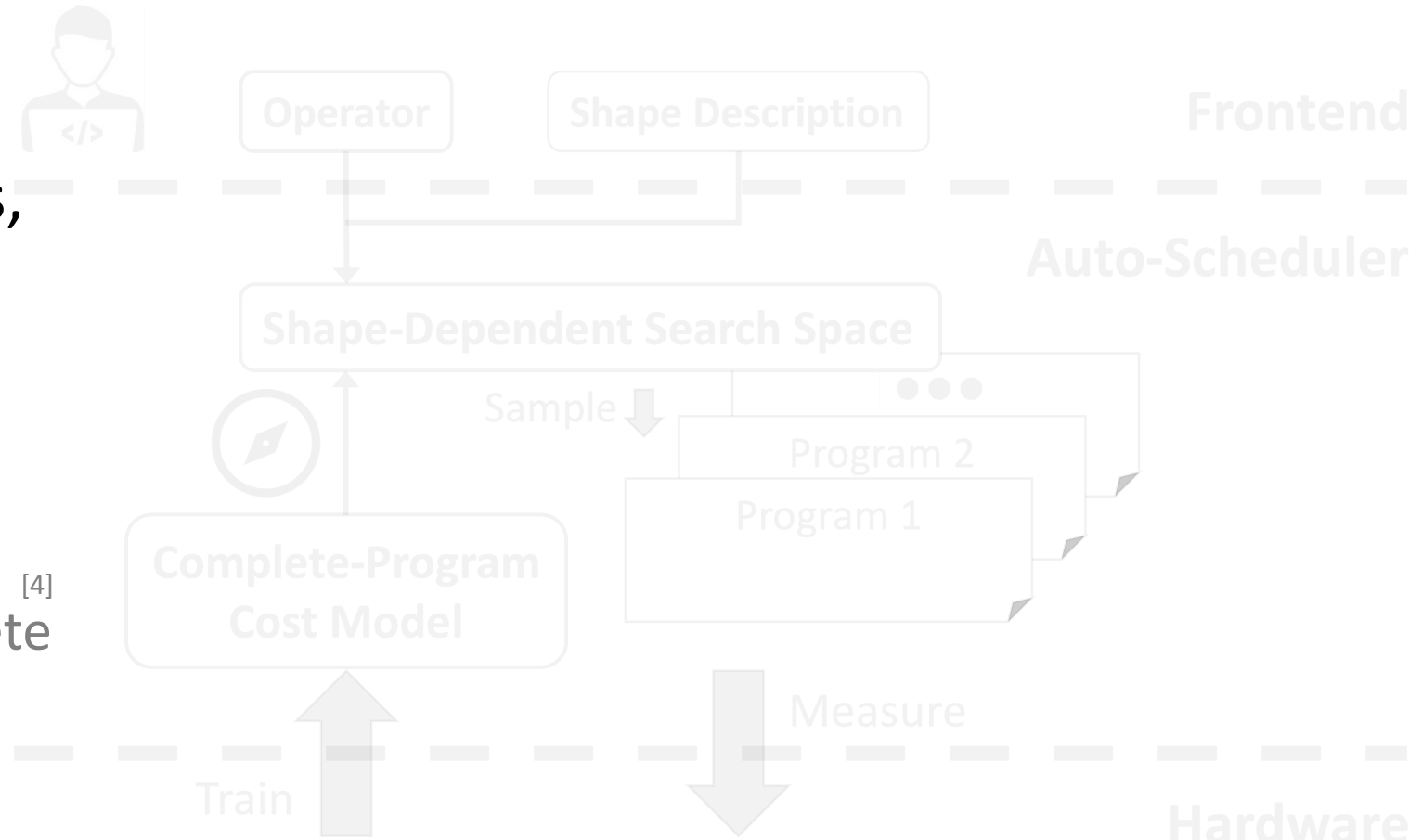
Speech Recognition[2]



Sentiment Analysis[3]

Text Auto-Complete[4]

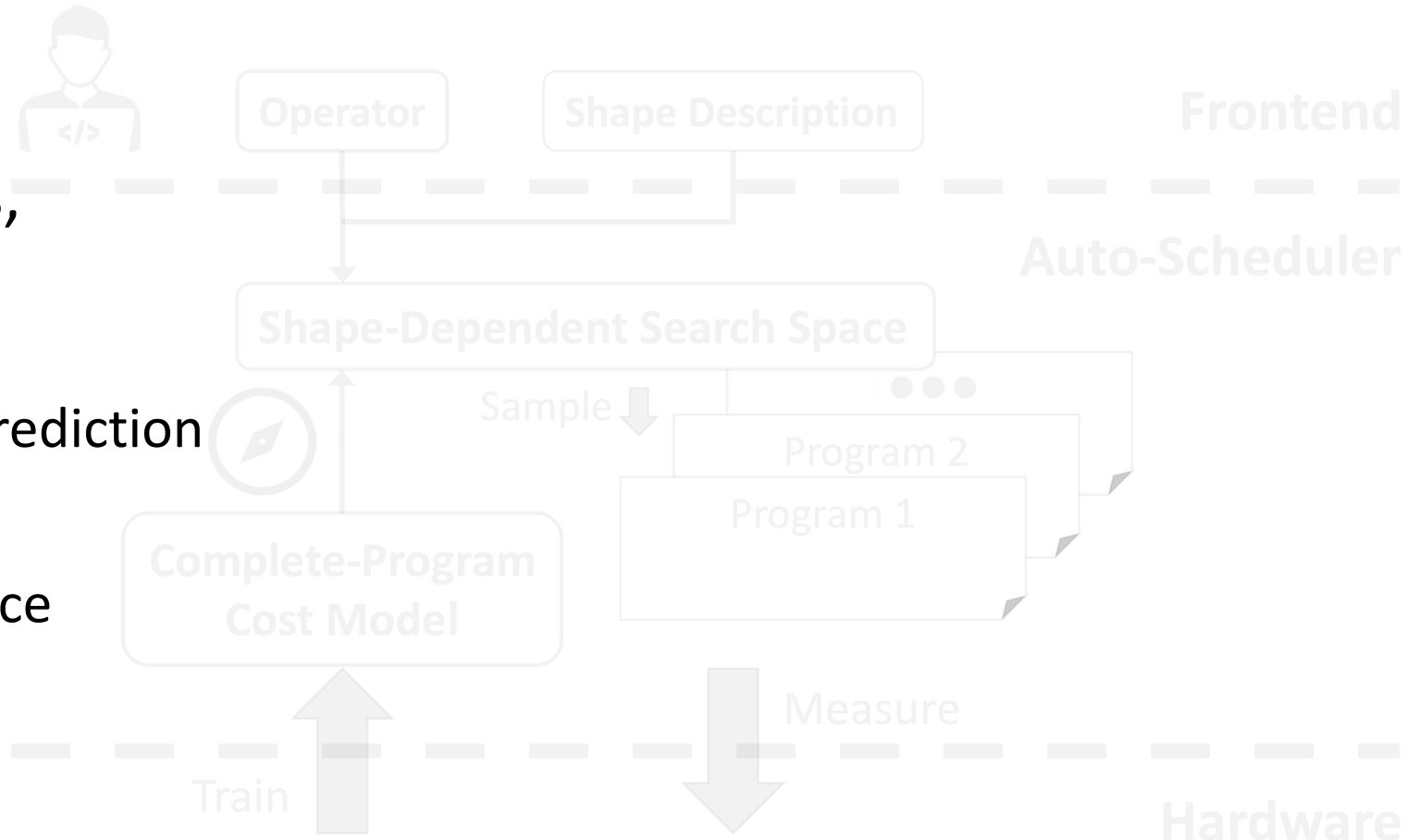
whose input sentences/audios have dynamic lengths.



[1] https://translate.google.com/
[2] https://github.com/NVIDIA/NeMo
[3] J. Devlin et al. *BERT*. NAACL-HTL 2019
[4] A. Radford et al. *GPT-2*. 2019

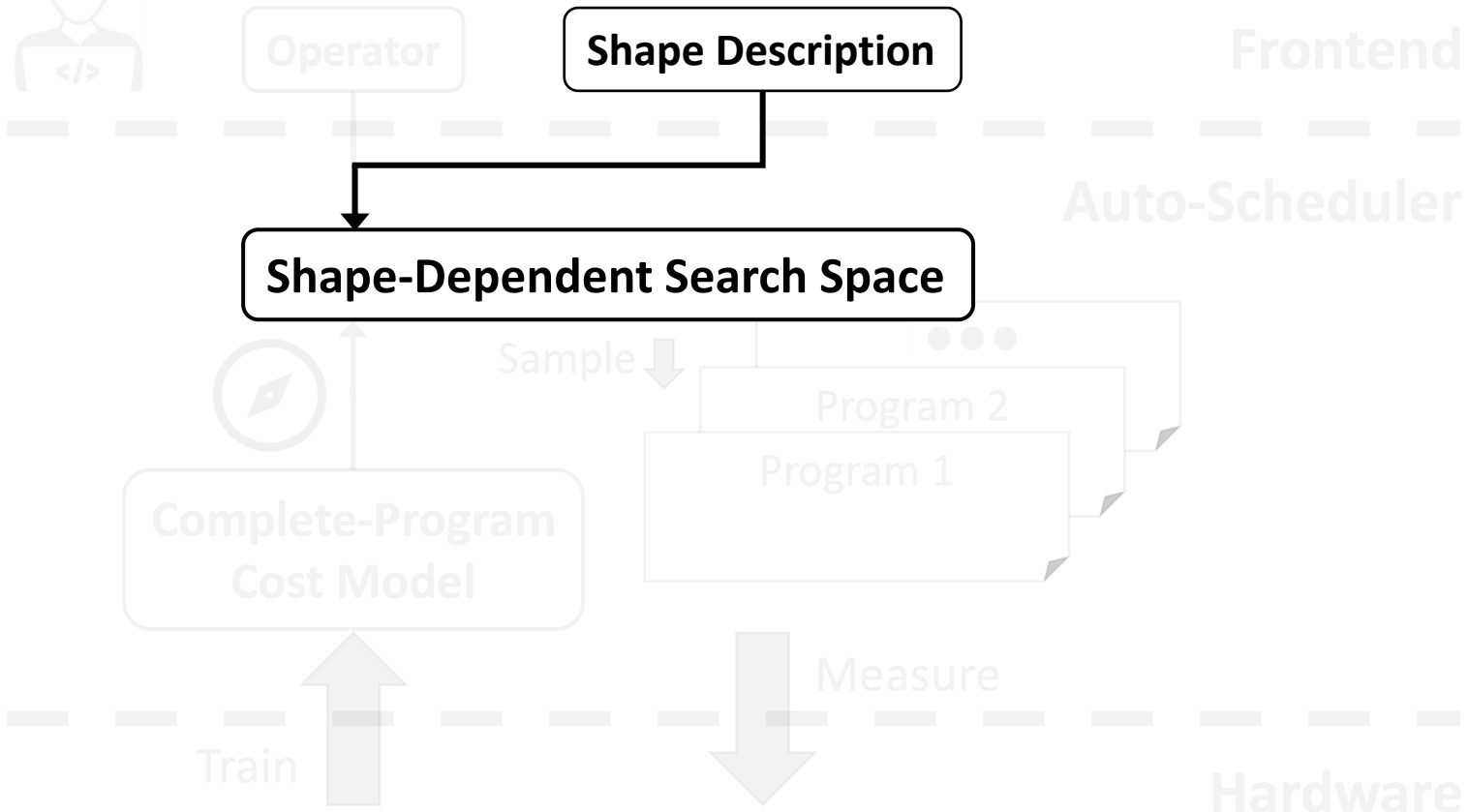
Challenges from Dynamic-Shape Workloads

- **Cannot** efficiently handle **dynamic-shape** operators, due to
  - Humongous Search Space
  - Inaccurate Performance Prediction
- *DietCode*'s Key Ideas:
  - Shape-Generic Search Space
  - Micro-Kernel-based Cost Model



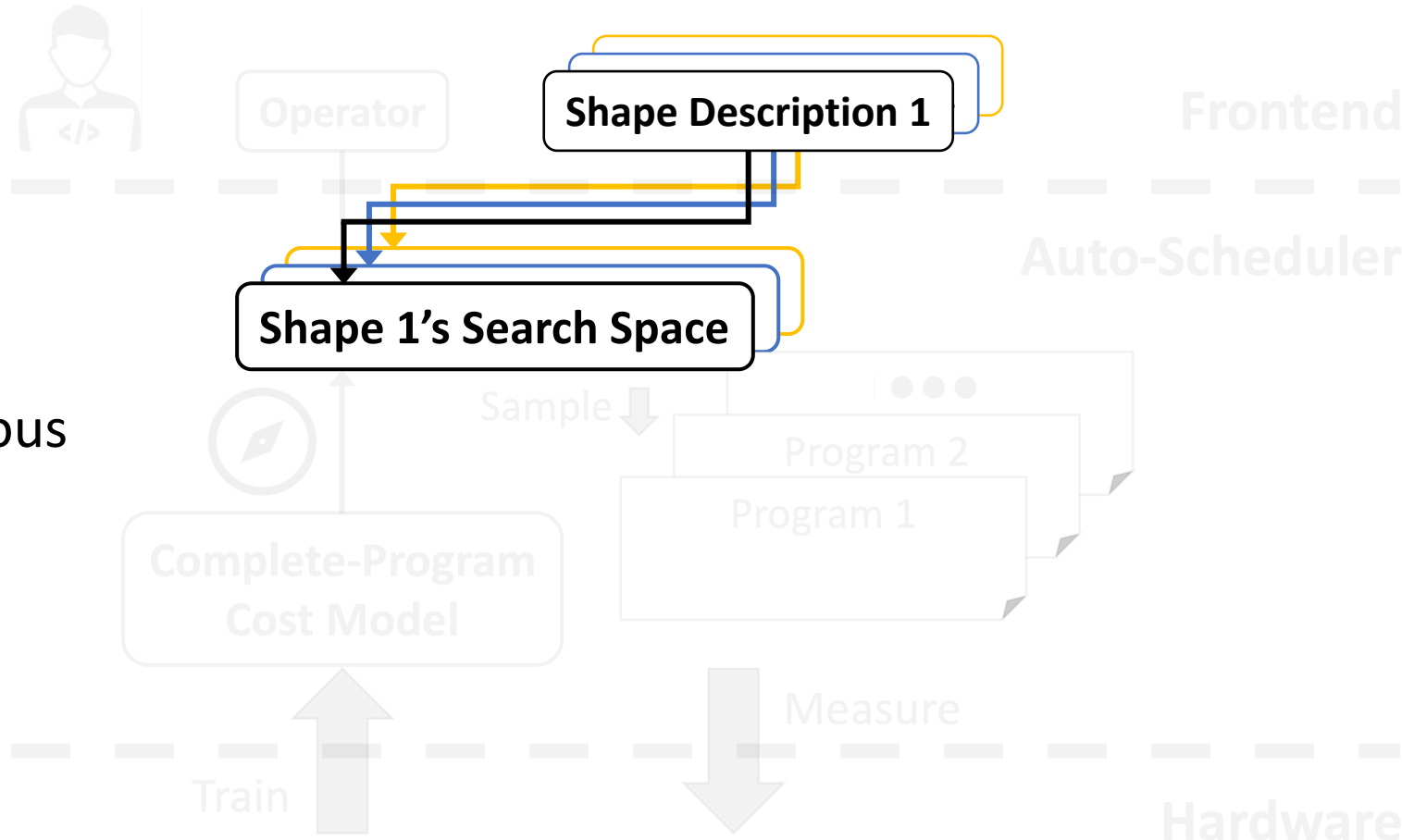
Challenge #1. Humongous Search Space

- **Hard** to share search space between operators of different shapes.



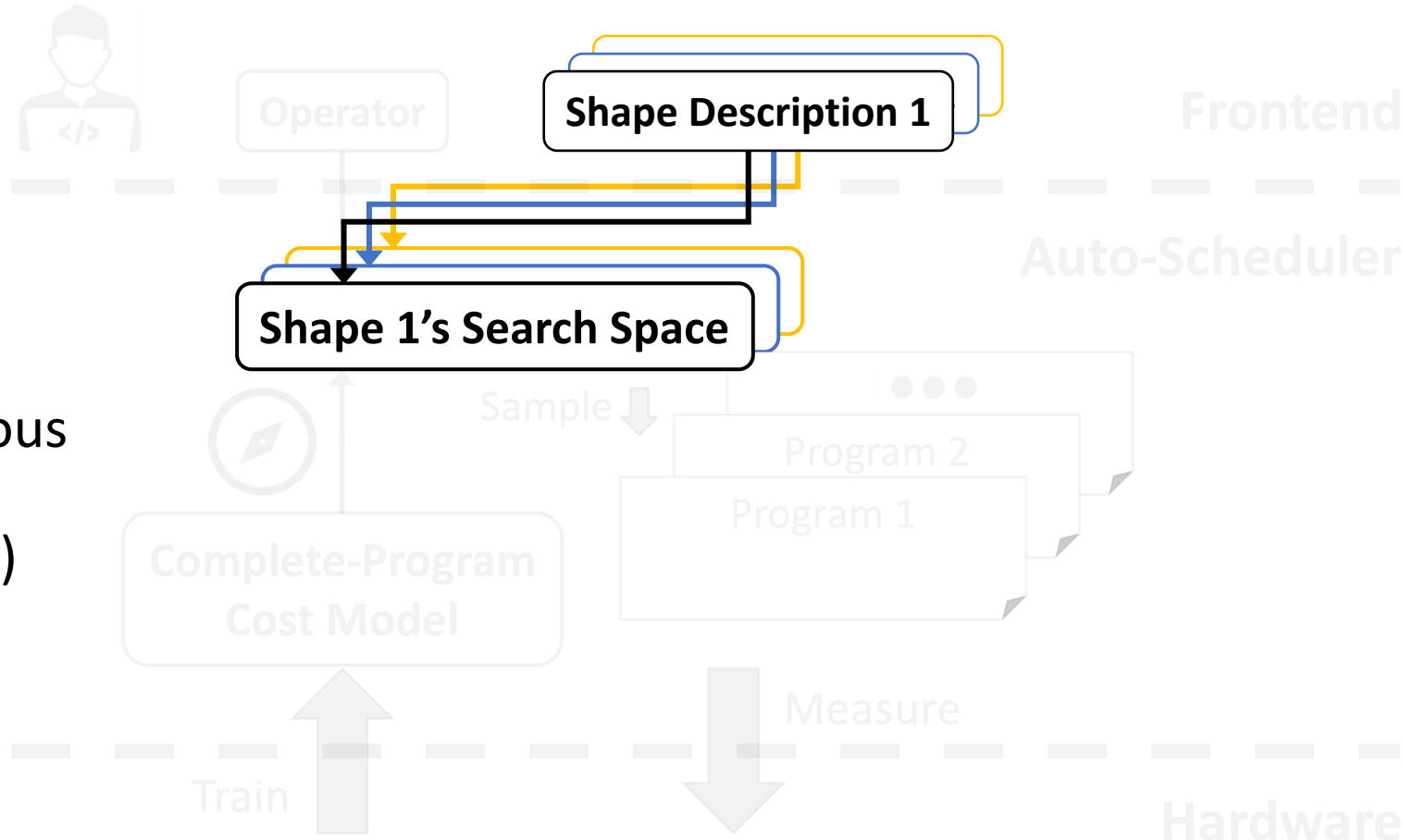
Challenge #1. Humongous Search Space

- **Hard** to share search space between operators of different shapes.
  - ⋂ search space: Tiny
  - ⋃ search space: Humongous



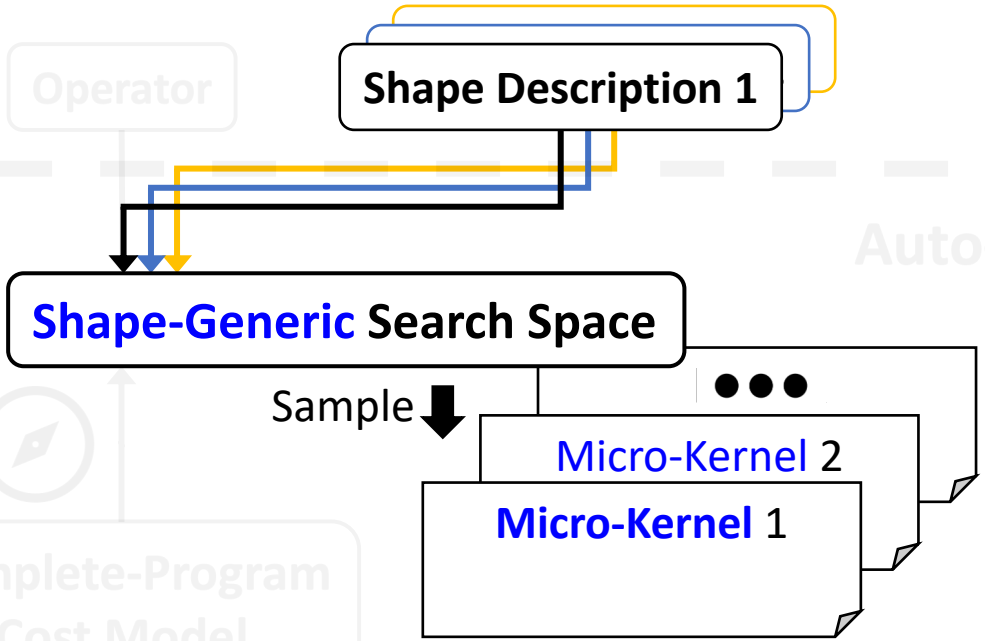
Challenge #1. Humongous Search Space

- **Hard** to share search space between operators of different shapes.
  - ⋂ search space: Tiny
  - ⋃ search space: Humongous
    ⇒ Huge Compilation Time
    (**days** for a single operator)



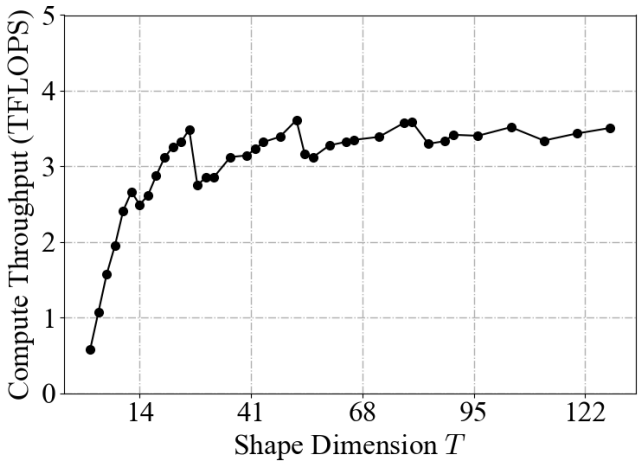
Key Idea #1. Shape-Generic Search Space

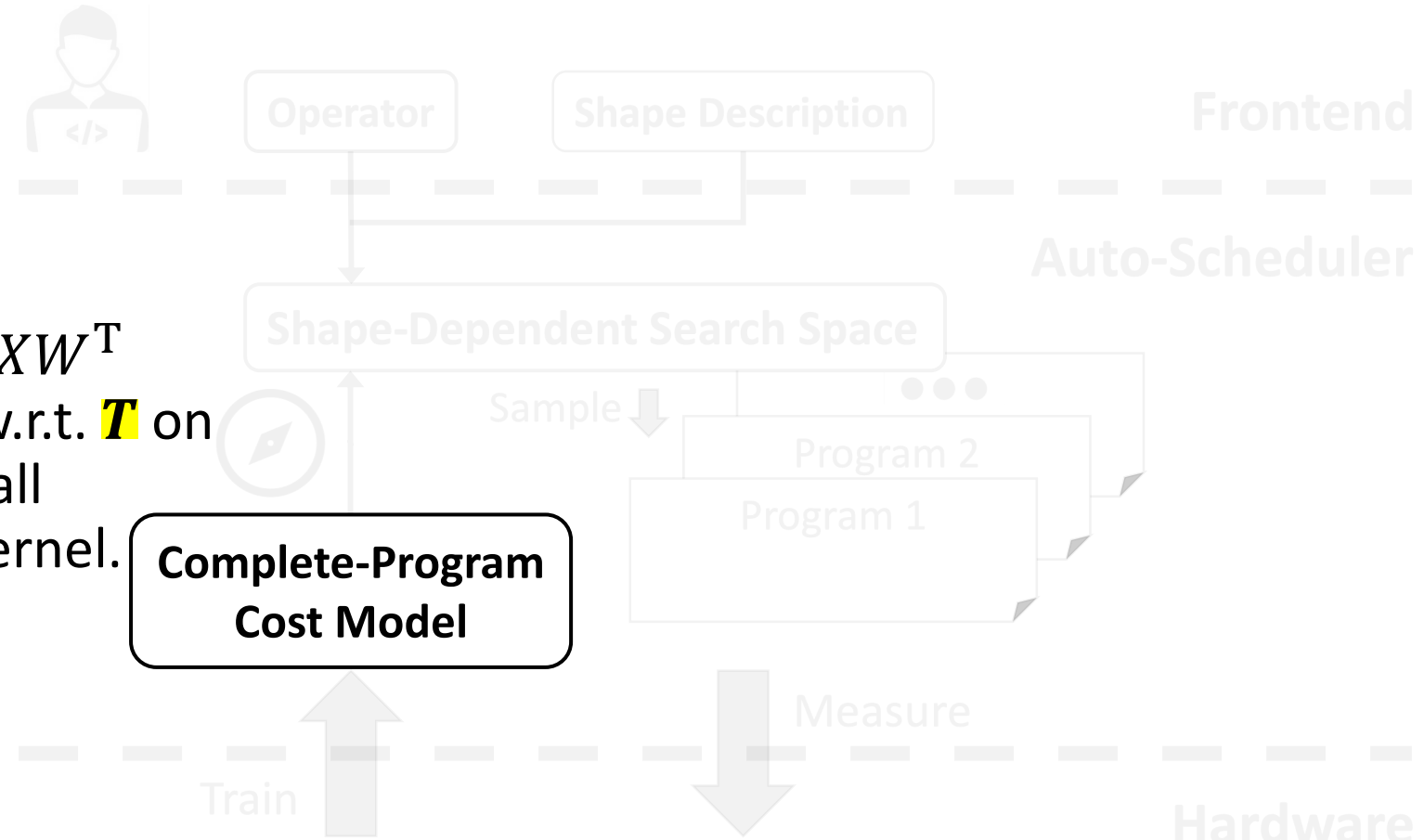
- Composed of **micro-kernels**, each
  - Does a tile of the entire compute.
  - Sampled uniformly from maximum shapes and constrained by hardware parameters.
  - Can be ported to **all** shapes of the same operator.



Challenge #2. Inaccurate Performance Prediction

- Cost model trained on one shape can be **inaccurate** on others.
  - E.g., Performance of $Y = XW^{\mathrm{T}}$ X: $[16\times\boldsymbol{T}, 768]$, W: $[2304, 768]$ w.r.t. $\boldsymbol{T}$ on a NVIDIA Tesla T4 GPU[1], all sharing the same micro-kernel.





[1] https://www.nvidia.com/en-us/data-center/tesla-t4/

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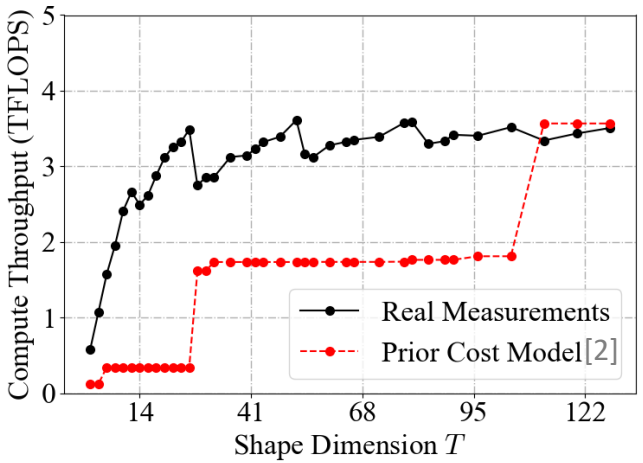


Complete-Program Cost Model

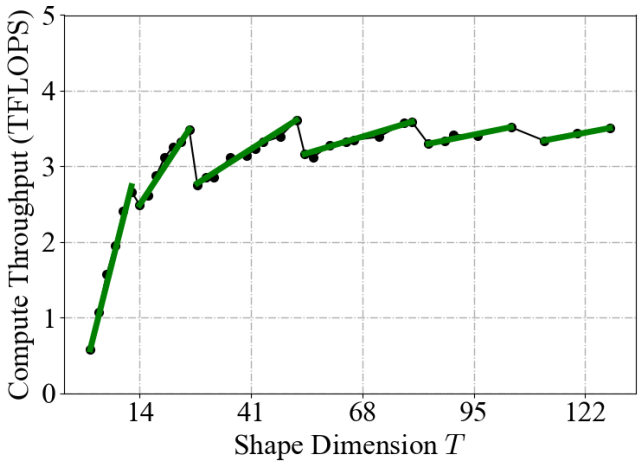
😕 Predictions are **inaccurate** on other shapes.

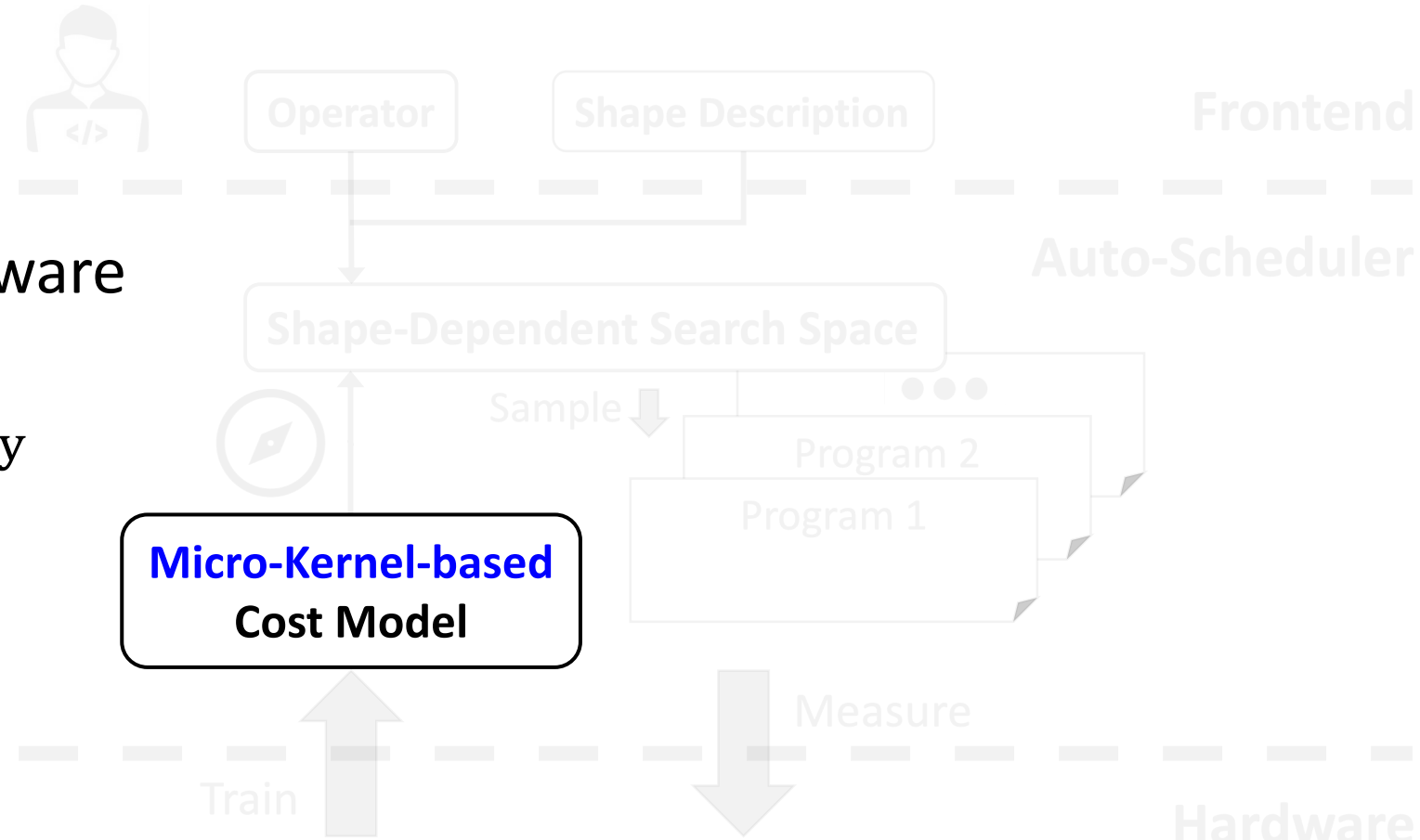
[1] https://www.nvidia.com/en-us/data-center/tesla-t4/
[2] L. Zheng et al. *Ansor*. OSDI 2020

Key Idea #2. Micro-Kernel-based Cost Model

- Key Observation: Performance scales **proportionally** with hardware core occupancy.

$$f_{\text{MicroKernel}} \cdot f_{\text{Penalty}}$$





Key Idea #2. Micro-Kernel-based Cost Model

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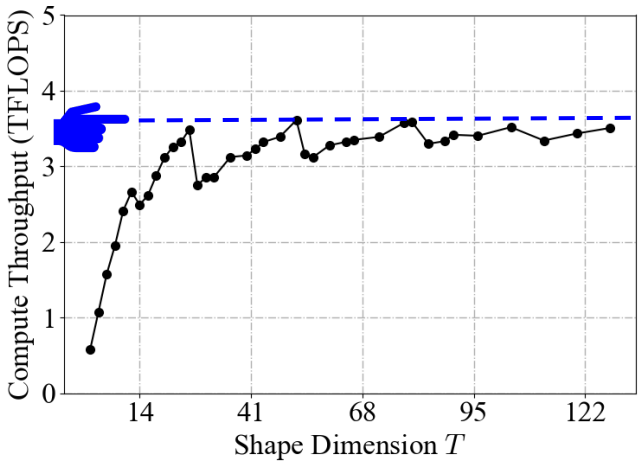
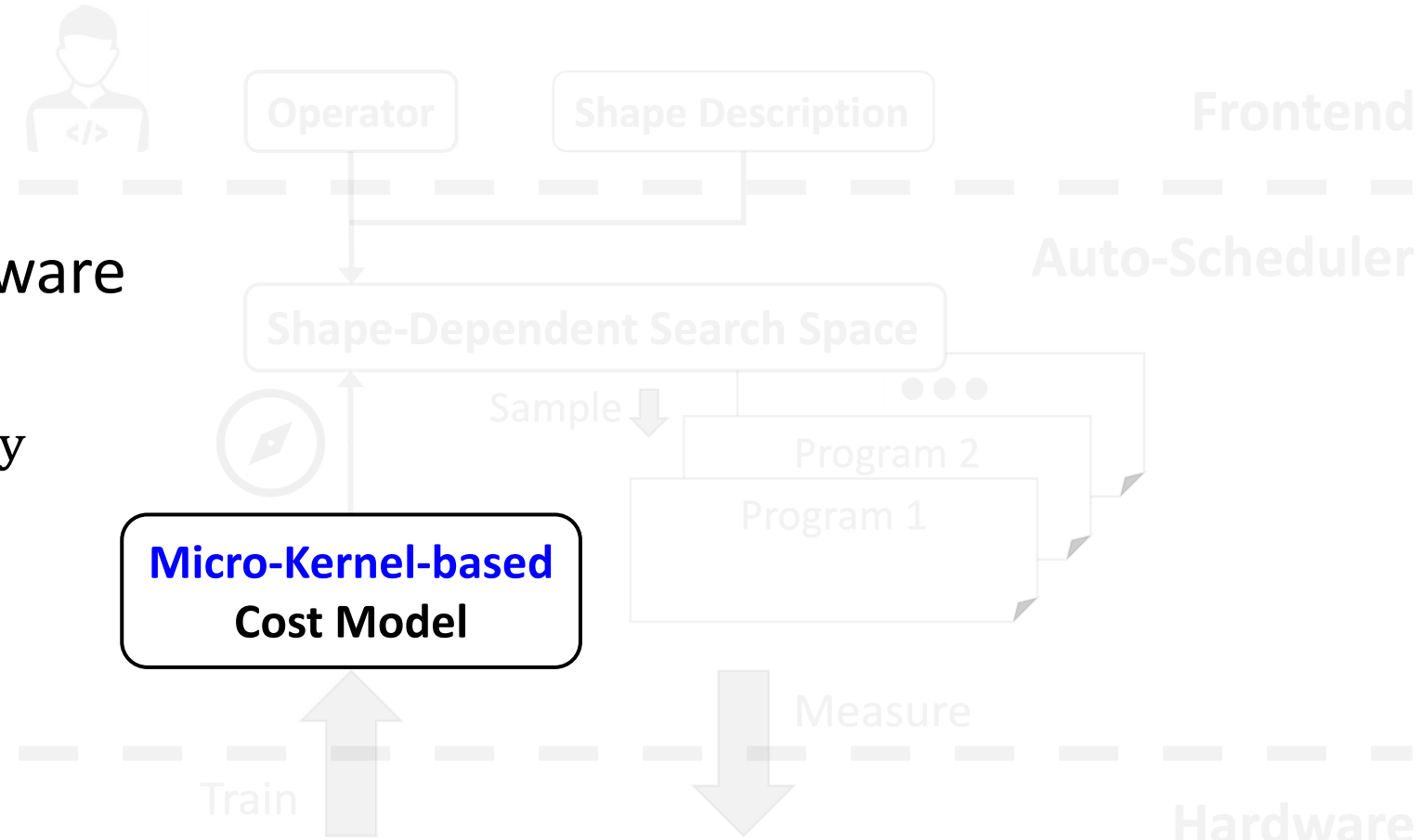
Trainable function for peak prediction





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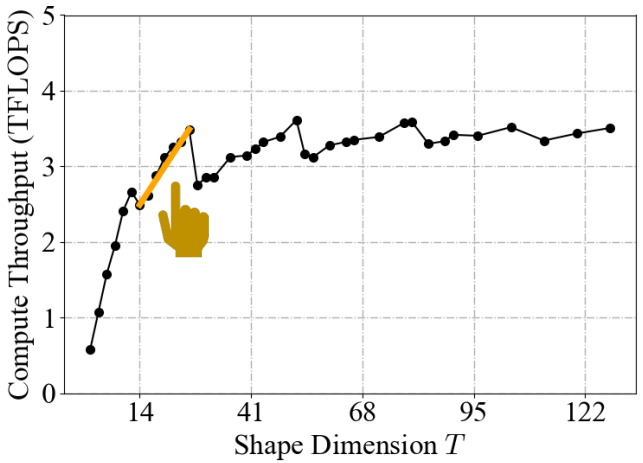
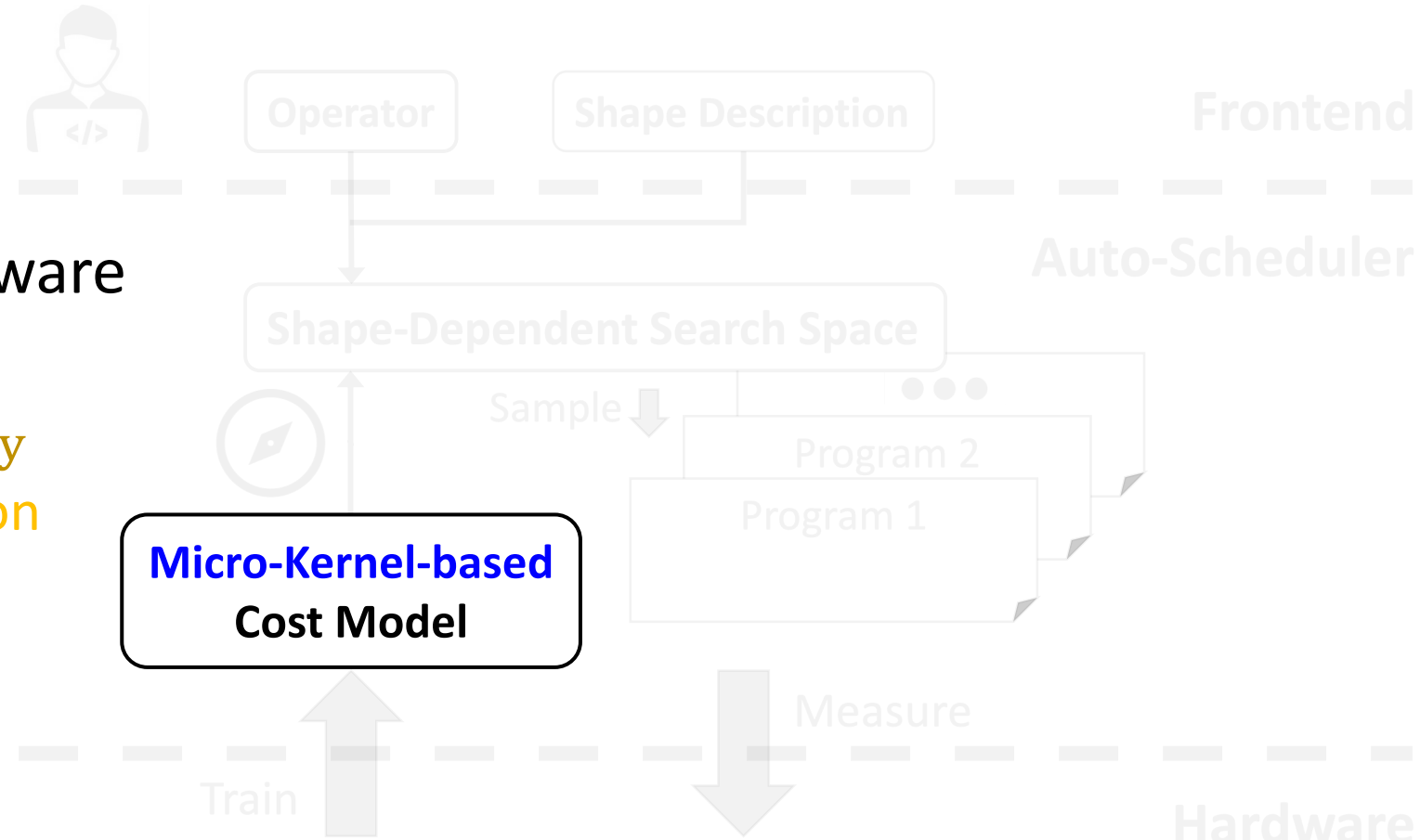
Analytical **linear** function of the core occupancy





Key Idea #2. Micro-Kernel-based Cost Model

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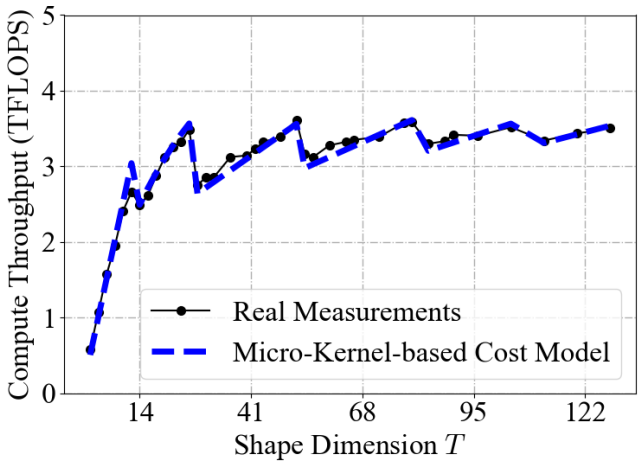
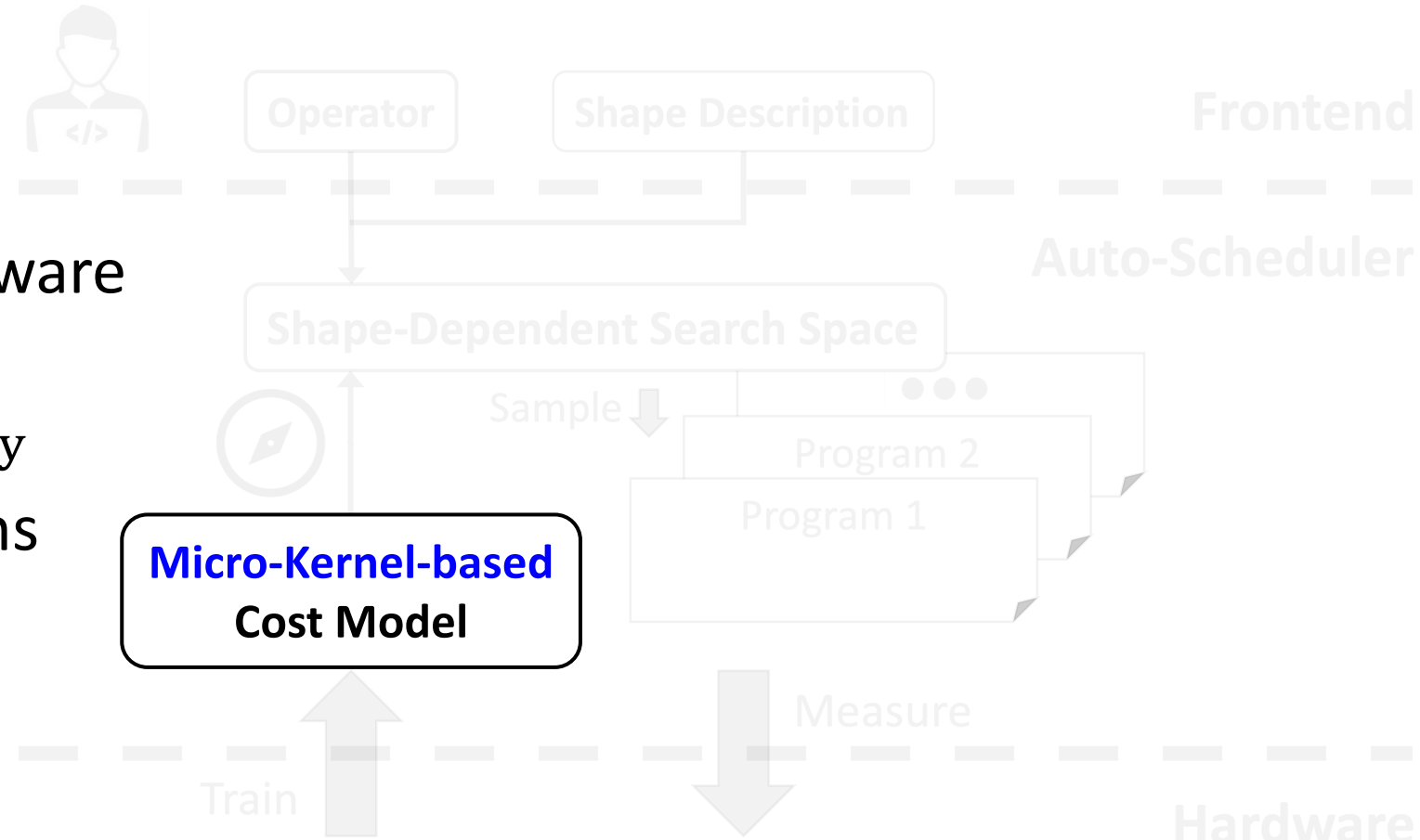
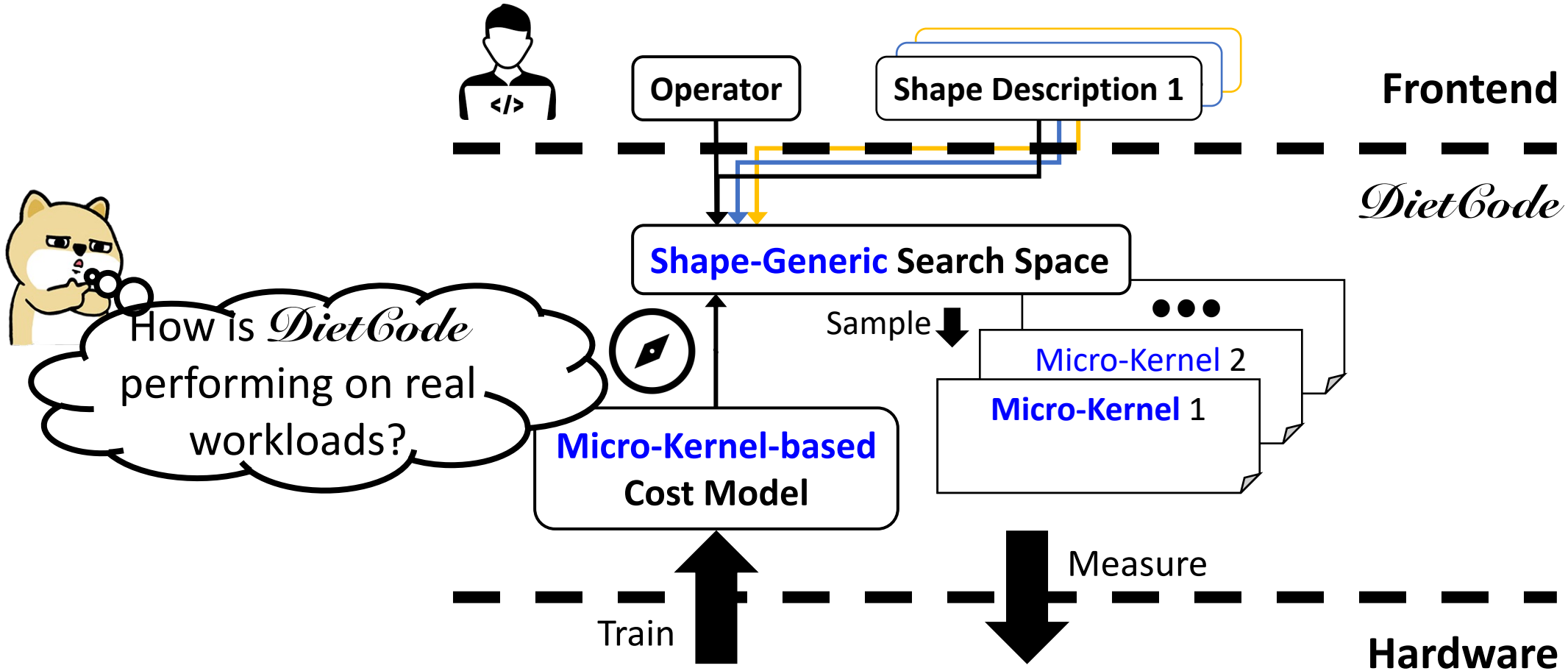
- More **Accurate** Predictions





DietCode System Overview



Evaluation

[1] https://www.nvidia.com/en-us/data-center/tesla-t4/
[2] https://www.nvidia.com/en-us/geforce/graphics-cards/30-series/rtx-3090-3090ti/

Hardware

NVIDIA Tesla T4 GPU[1]

NVIDIA RTX 3090 GPU[2]

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[5] https://docs.nvidia.com/deeplearning/cudnn/developer-guide/index.html

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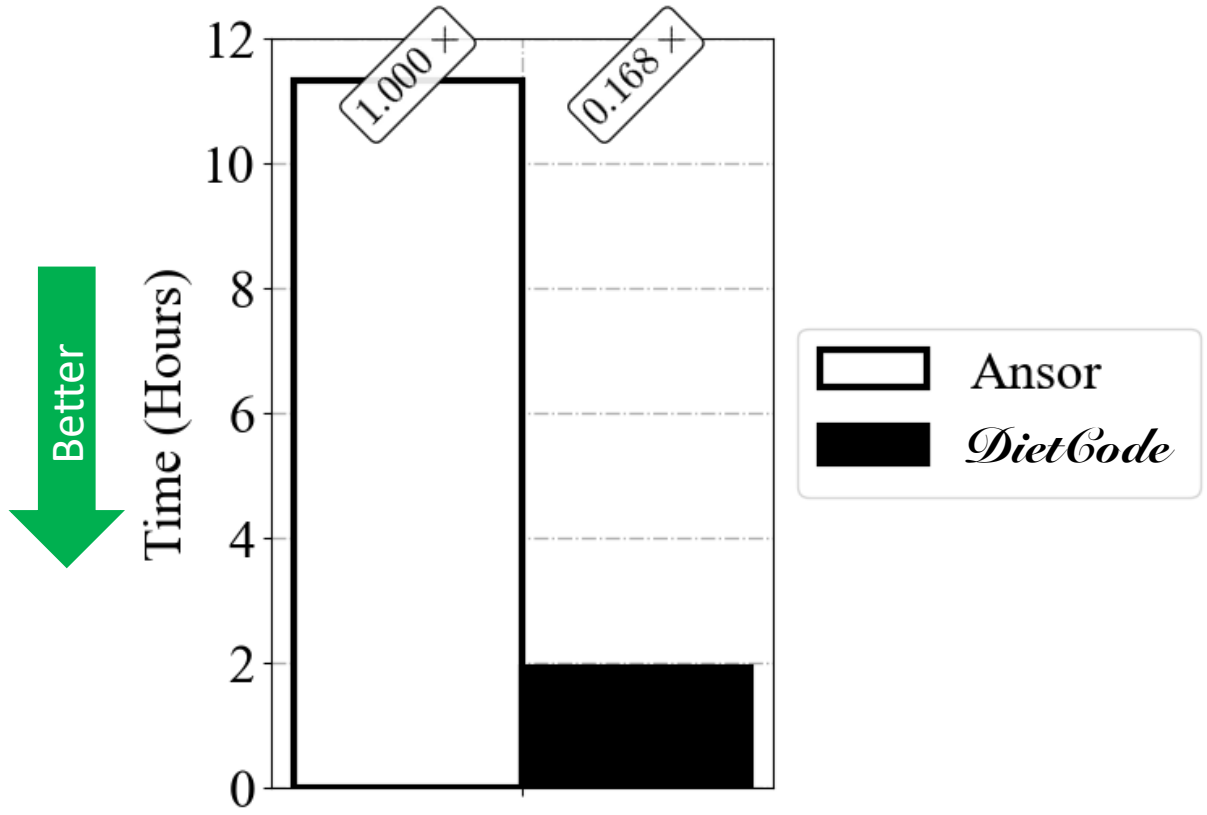
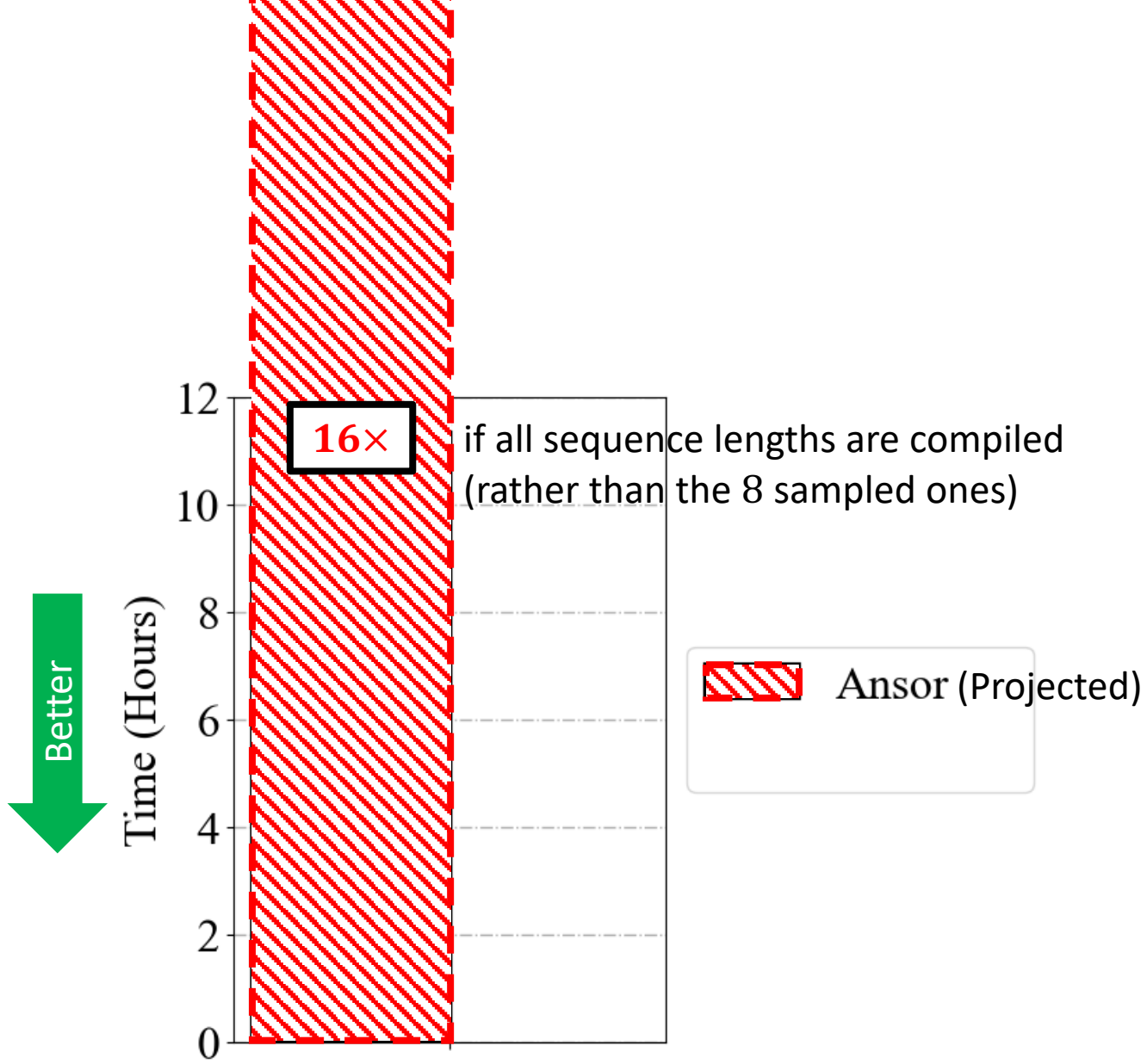
Compilation Time vs. Ansor



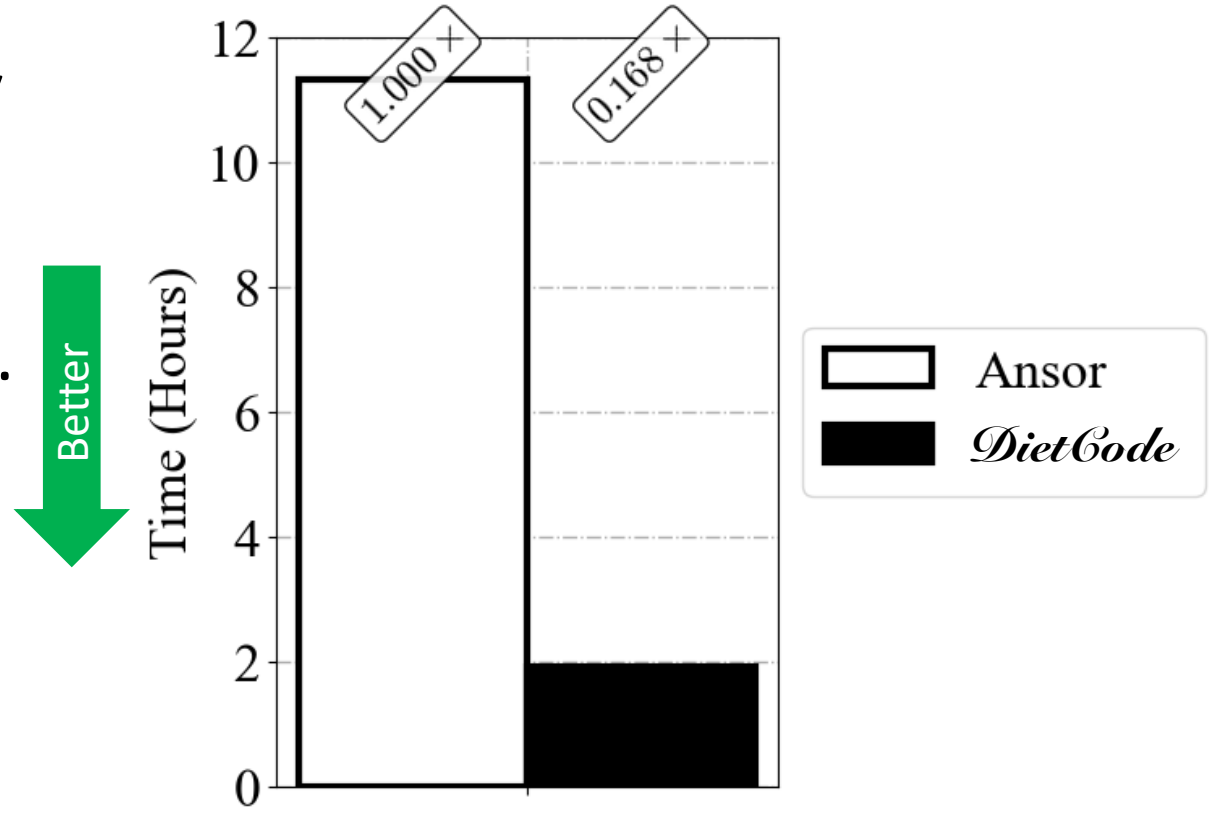
Compilation Time

- Ansor: Time estimated to be more than **1 week** for only key operators.



Compilation Time vs. Ansor

- Ansor: Time estimated to be more than **1 week** for only key operators.
- *DietCode* reduces the compilation time by **5.88×** vs. Ansor



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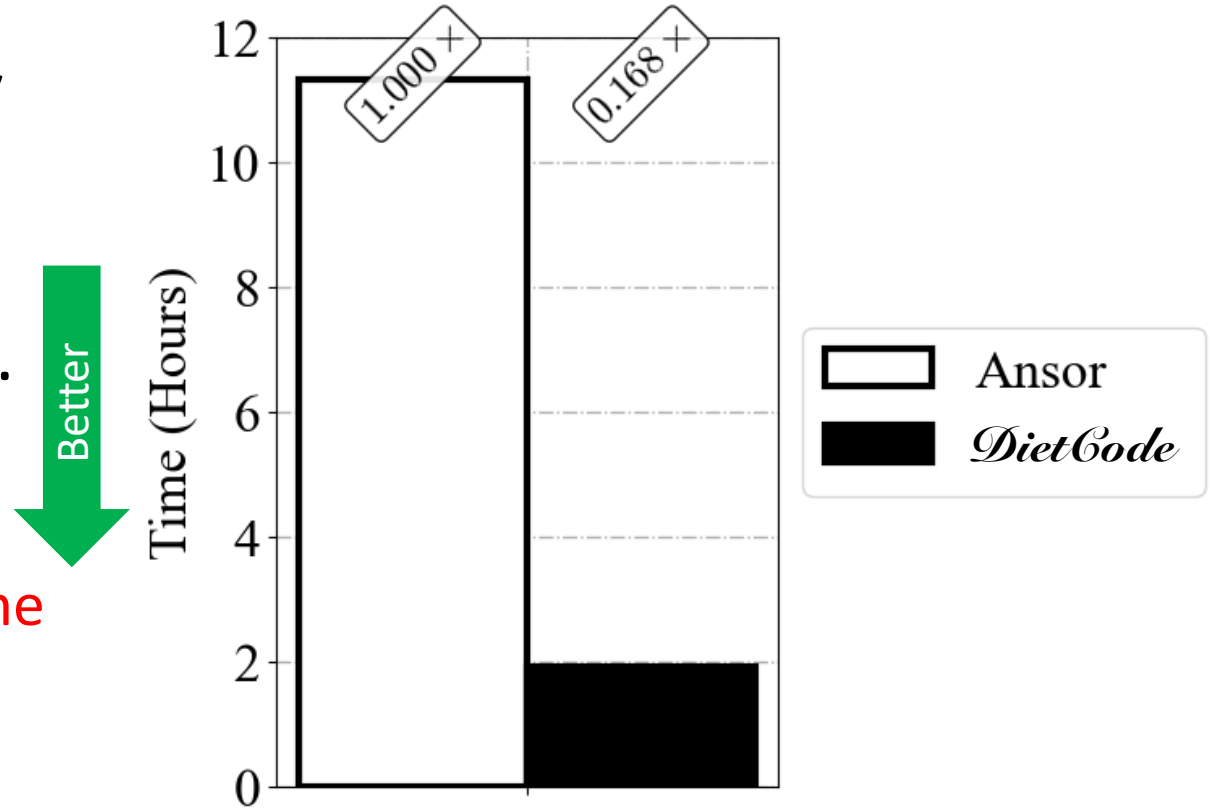
  - 16× increase in compilation time



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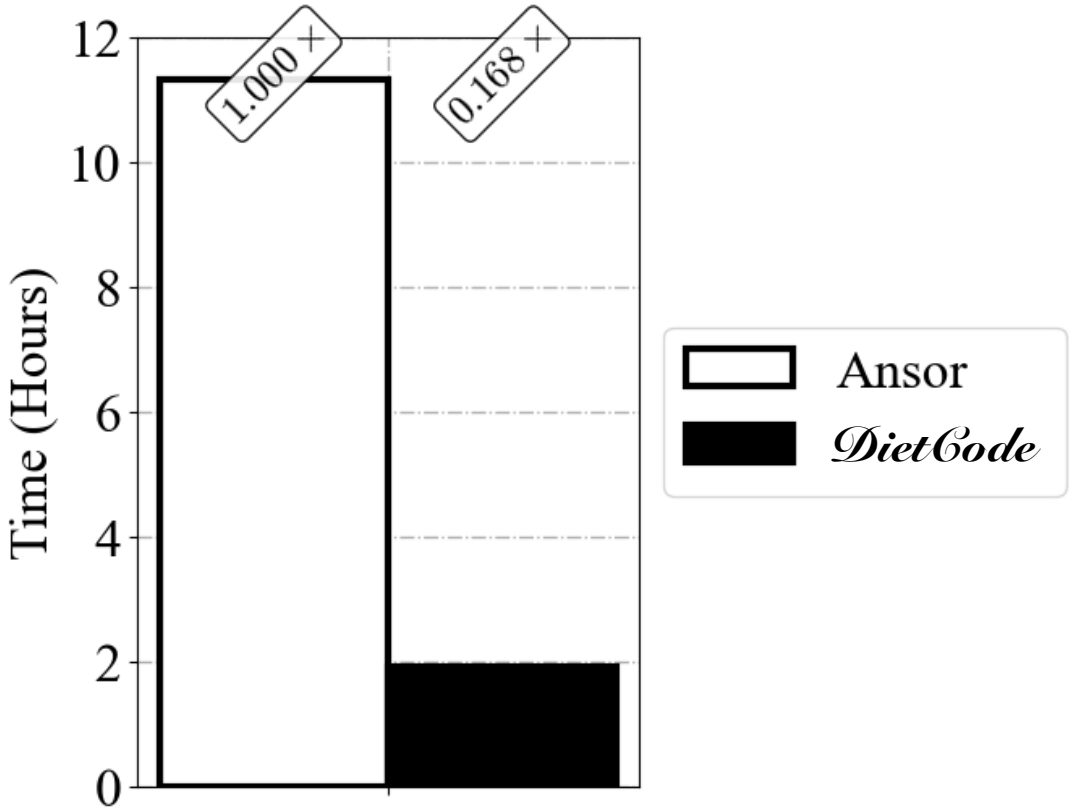
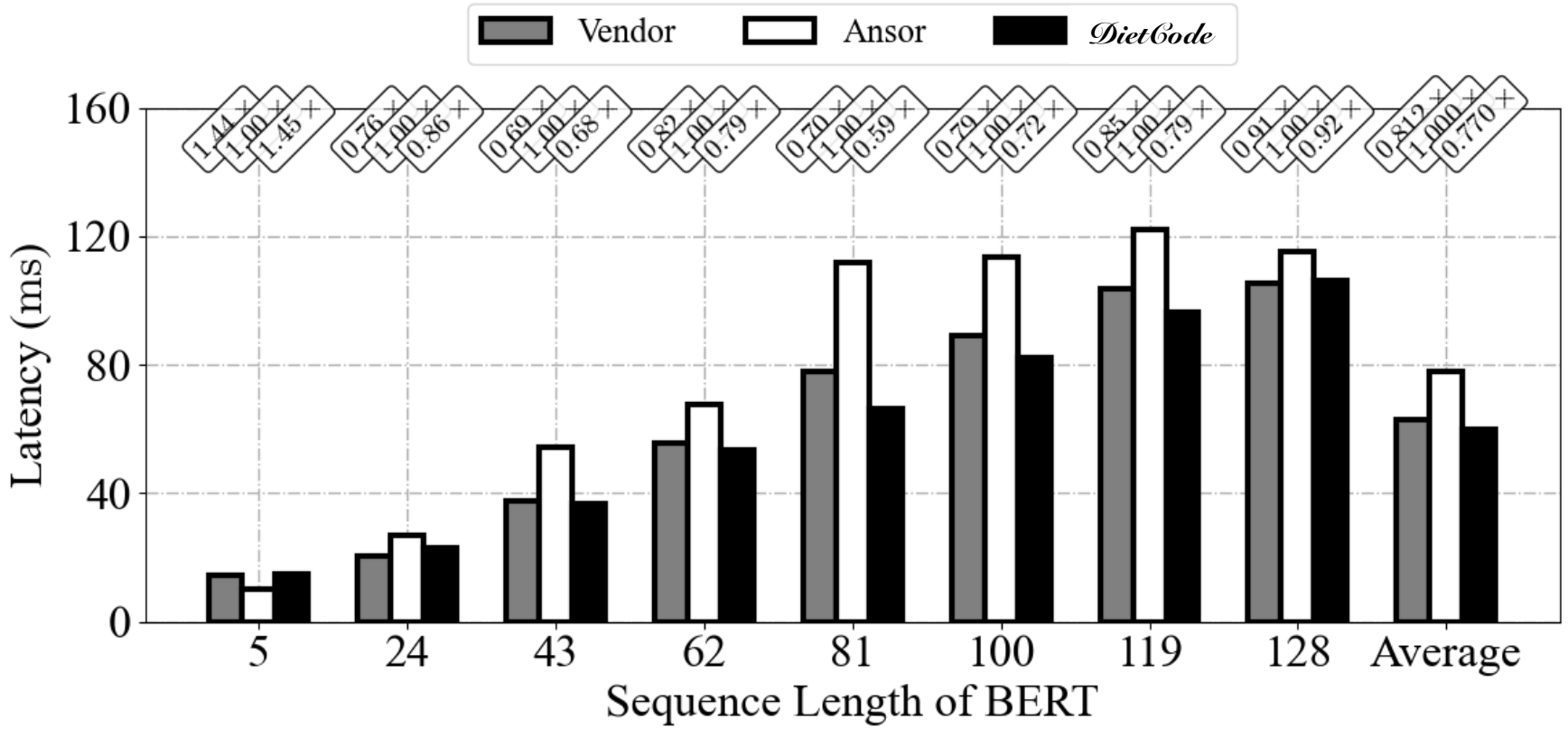
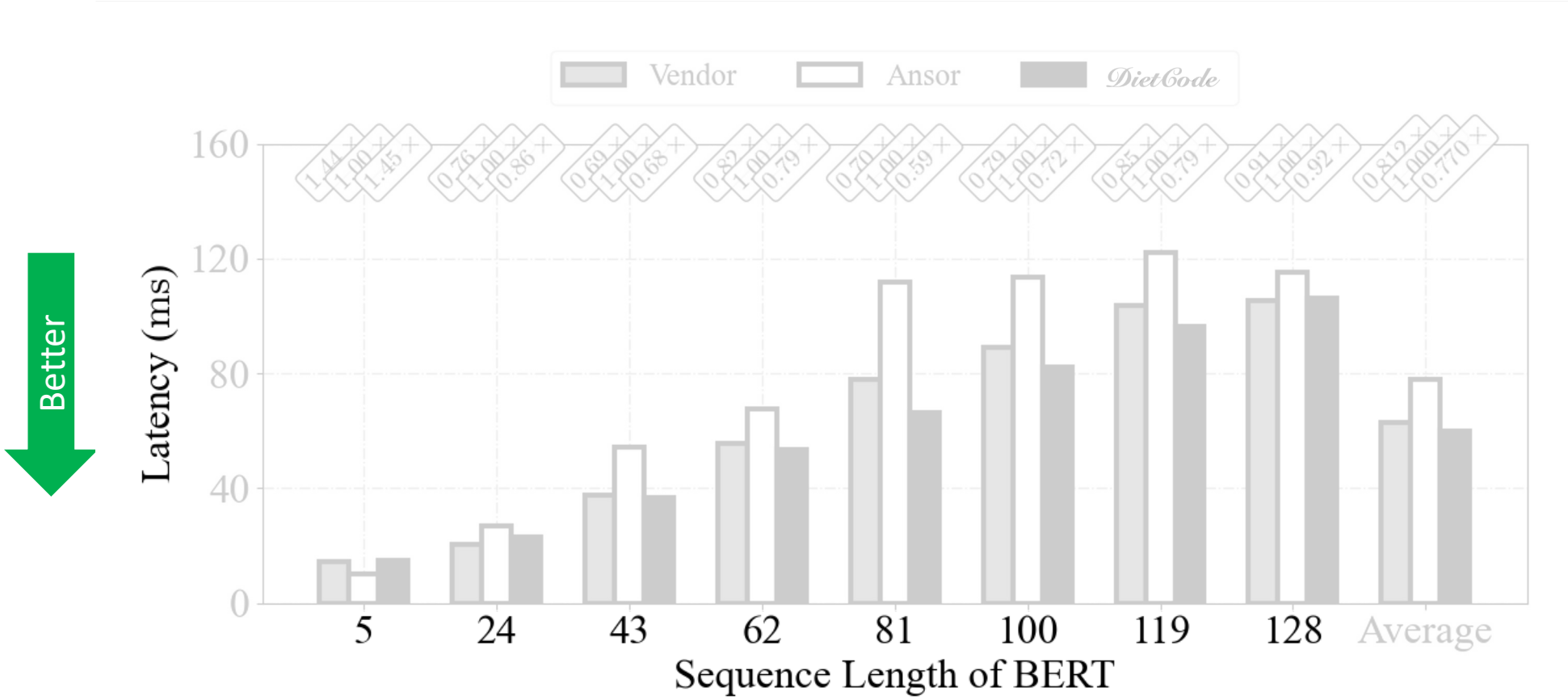


Latency vs. Vendor/Ansor

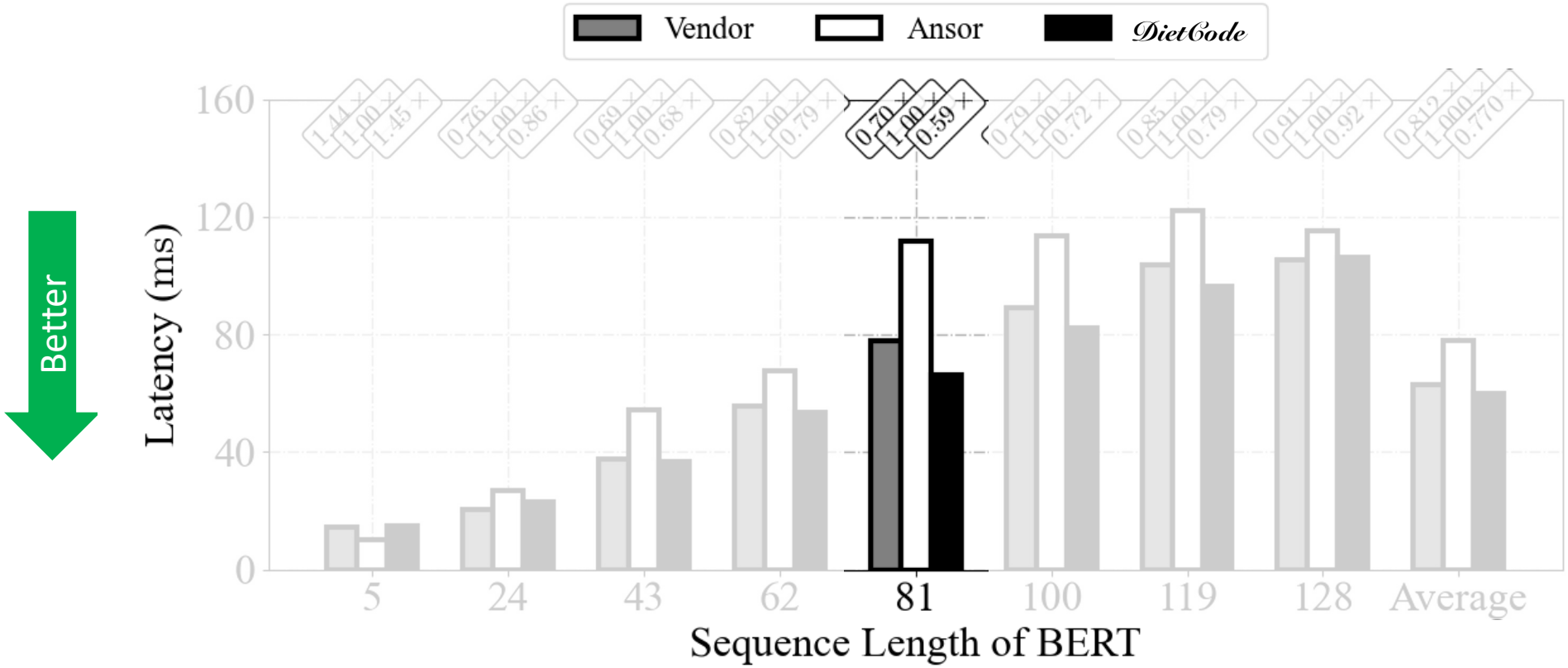


Latency vs. Vendor/Ansor



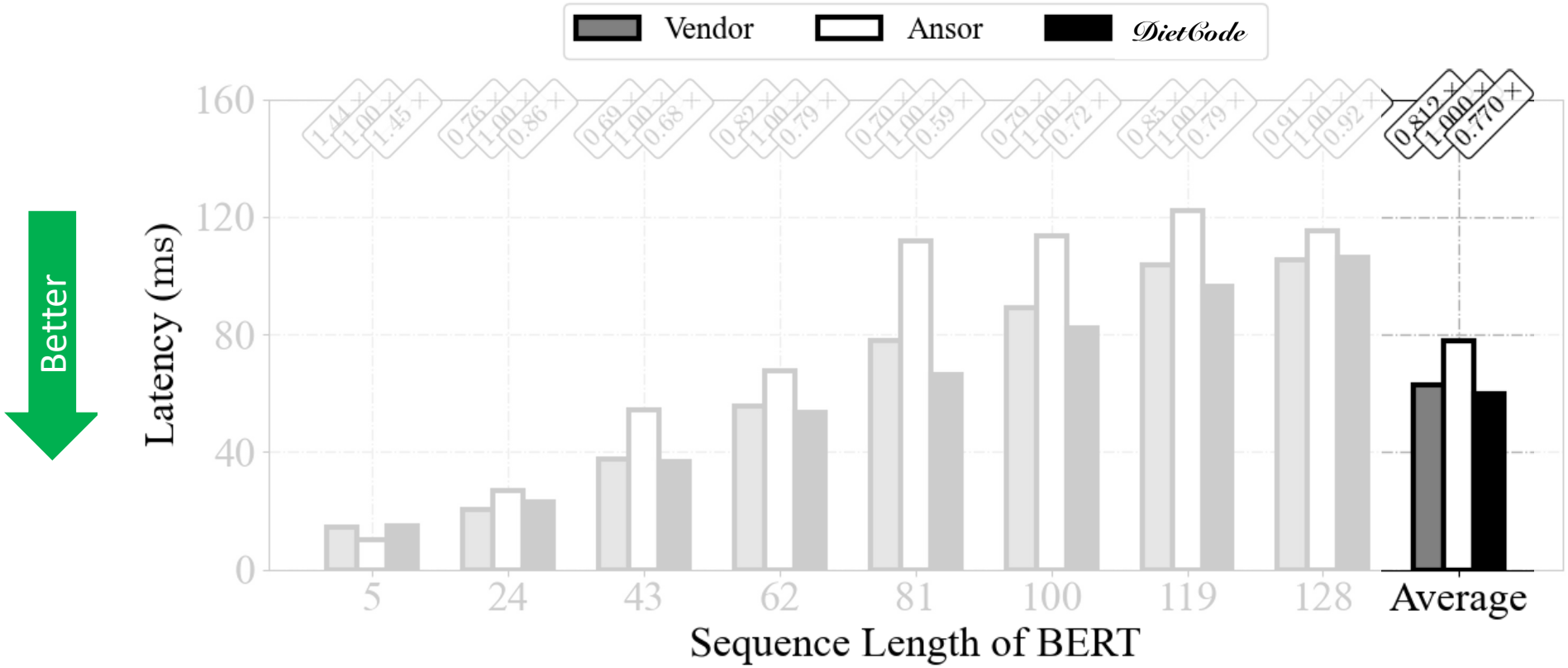
Uniformly sampled and includes composite and **prime** numbers.

Latency vs. Vendor/Ansor



√ Up to $\mathbf{1.70}\times/\mathbf{1.19}\times$ better than Ansor/Vendor.

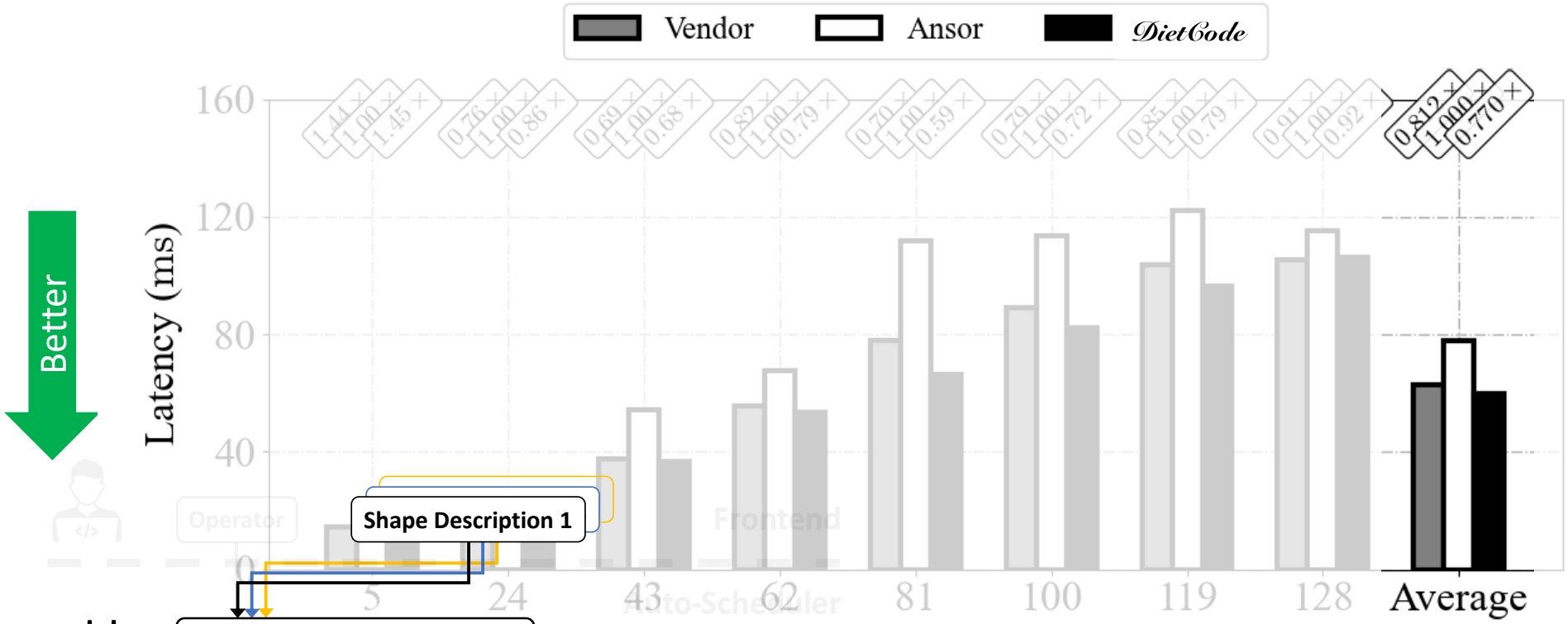
Latency vs. Vendor/Ansor



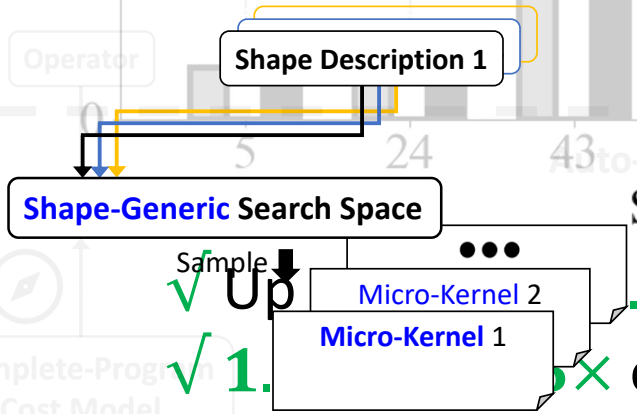
√ Up to $\mathbf{1.70\times}$/$\mathbf{1.19\times}$ better than Ansor/Vendor.

√ $\mathbf{1.30\times}$/$\mathbf{1.05\times}$ on average.

Latency vs. Vendor/Ansor



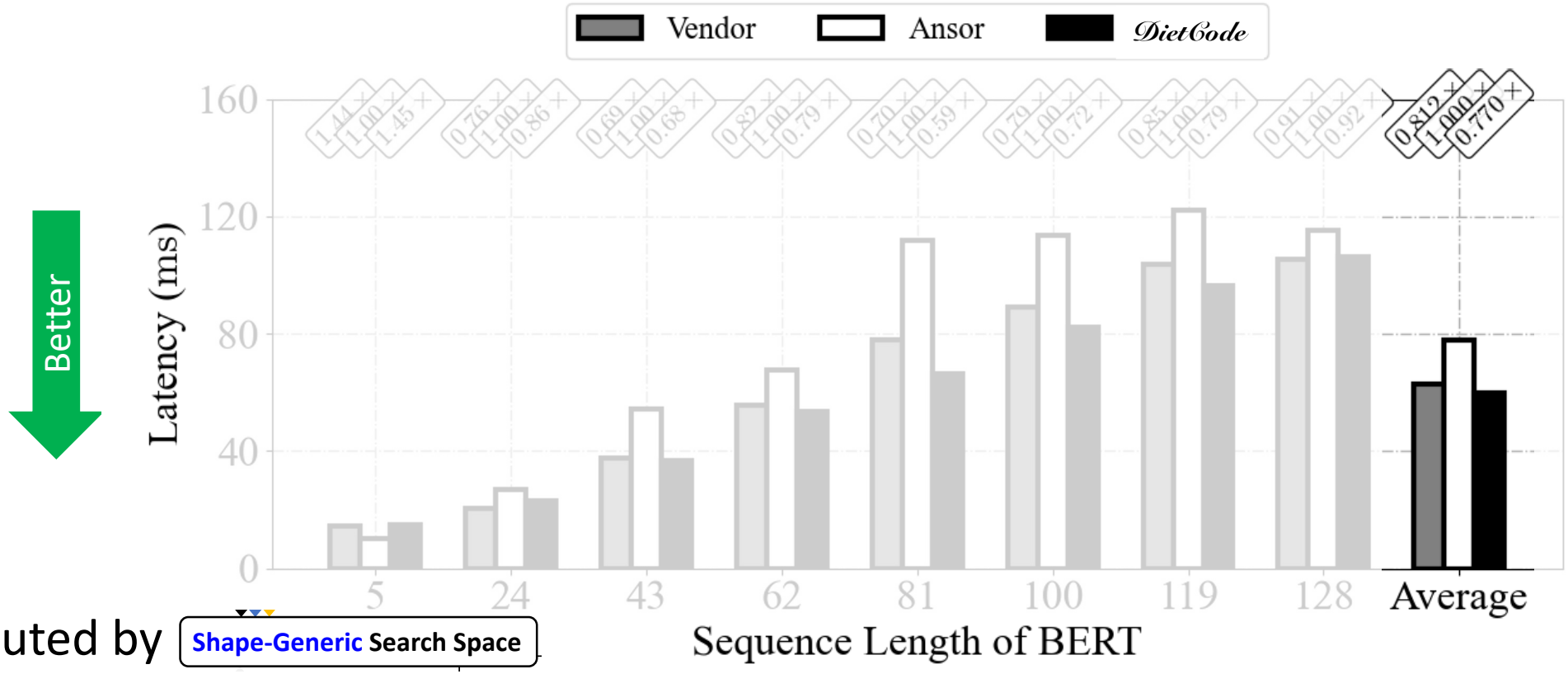
Contributed by



√ Up to **1.19×** better than Ansor/Vendor.

√ **1.**[illegible]**×** on average.

Latency vs. Vendor/Ansor



Contributed by Shape-Generic Search Space

√ Up to $\mathbf{1.70\times}$/$\mathbf{1.19\times}$ better than Ansor/Vendor.

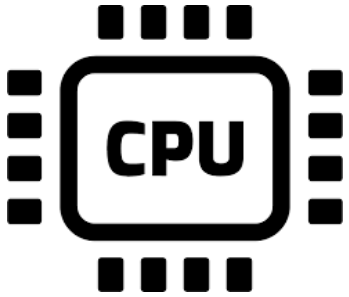
√ $\mathbf{1.30\times}$/$\mathbf{1.05\times}$ on average.

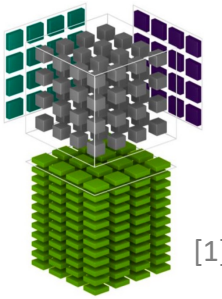
Future Directions

- We are working on upstreaming *DietCode* to the TVM main branch: https://github.com/apache/tvm-rfcs/pull/72, together with improvement of the tuning algorithms.

  Many thanks to the  community!

- Evaluations on more hardware platforms (CPUs and NVIDIA GPUs using tensor core operations)





[1]

[1] https://www.nvidia.com/en-us/data-center/tensor-cores/

Future Directions

- We are working on upstreaming *DietCode* to the TVM main branch: https://github.com/apache/tvm-rfcs/pull/72, together with improvement of the tuning algorithms.

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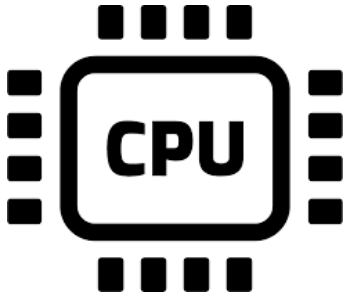
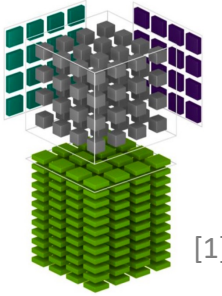
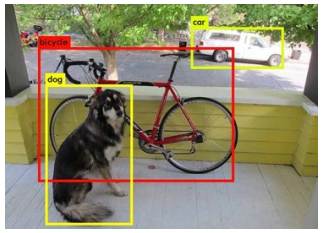
- Evaluations on more hardware platforms (CPUs and NVIDIA GPUs using tensor core operations) and workloads.





[1]

Speech Recognition[2]



Object Detection[3]

[1] https://www.nvidia.com/en-us/data-center/tensor-cores/
[2] https://github.com/NVIDIA/NeMo
[3] K. He et al. Mask R-CNN. ICCV 2017

Conclusion

- Challenges posed by dynamic-shape workloads:
  - Vendor Libraries: Hard to be Engineered for Efficiency
  - Existing Auto-Schedulers: Long Compilation Time
- *DietCode* addresses the challenges with
  ① shape-generic search space
  ② micro-kernel-based cost model.
- Key Results:
  - Compilation Time: $\mathbf{5.88}\times$ saving vs. Ansor.
  - Performance: Up to $\mathbf{1.70}\times$ better vs. Ansor and $\mathbf{1.19}\times$ vs. the vendor library on modern GPUs.

DietCode: Automatic Code Generation for Dynamic Tensor Programs

Bojian Zheng[1, 2, 3 *], Ziheng Jiang[4 *], Cody Yu[2], Haichen Shen[2],
Josh Fromm[5], Yizhi Liu[2], Yida Wang[2],
Luis Ceze[5, 6], Tianqi Chen[5, 7], Gennady Pekhimenko[1, 2, 3]

[*] Equal Contributions

1 

2 

3 

4 

5 

6 

7 

Optimization Strategy

- **Objective**: End-to-End Latency

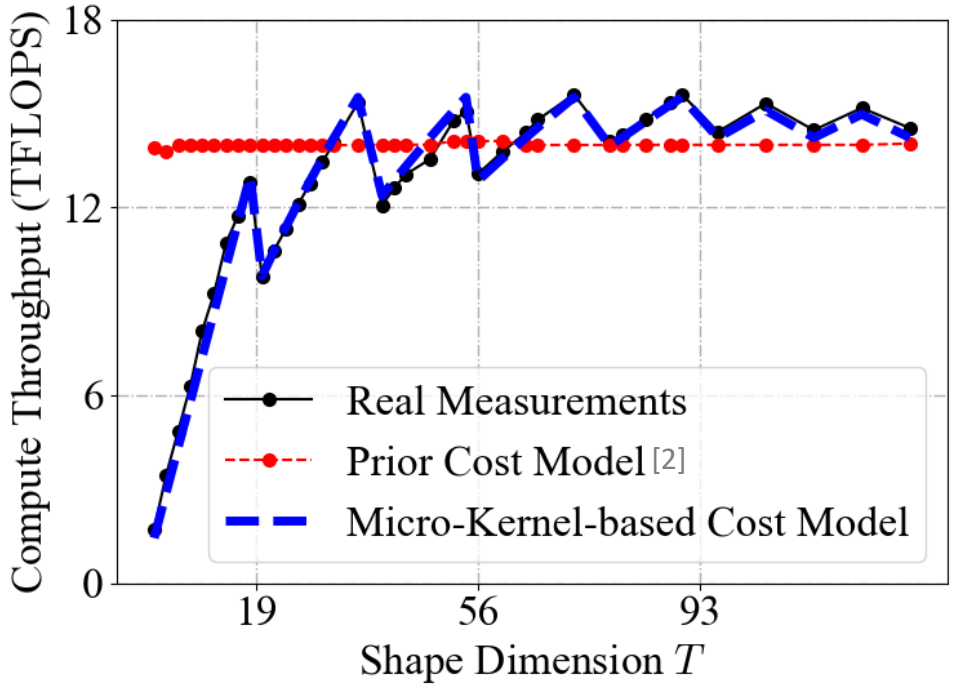
- All workloads have “optimization priority” as

$$\text{FLOPs} \times \text{weight (user-defined, 1 by default)}$$

- Consequently, workloads with higher FLOPs will be given more attention compared with smaller ones.

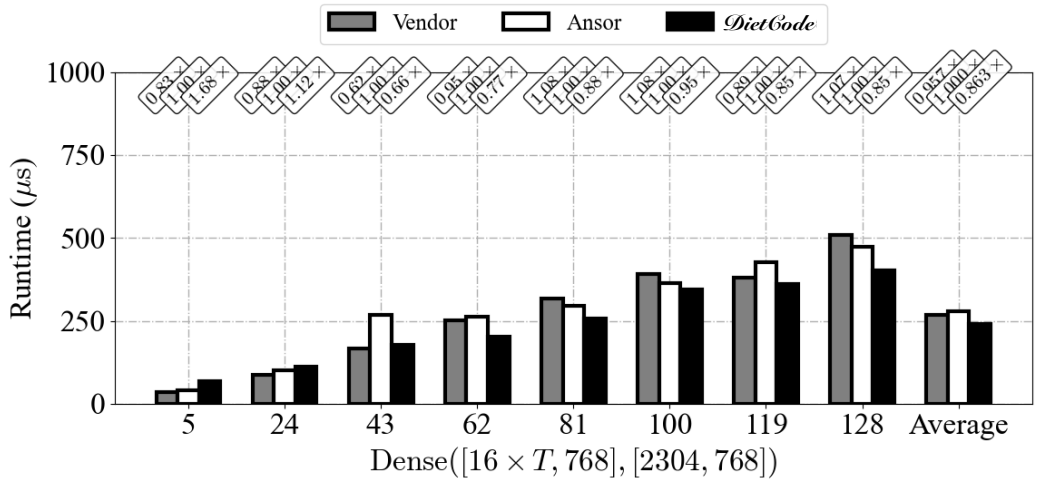
NVIDIA RTX 3090[1] Preliminary Results

Micro-Kernel-based Cost Model



Performance

Better

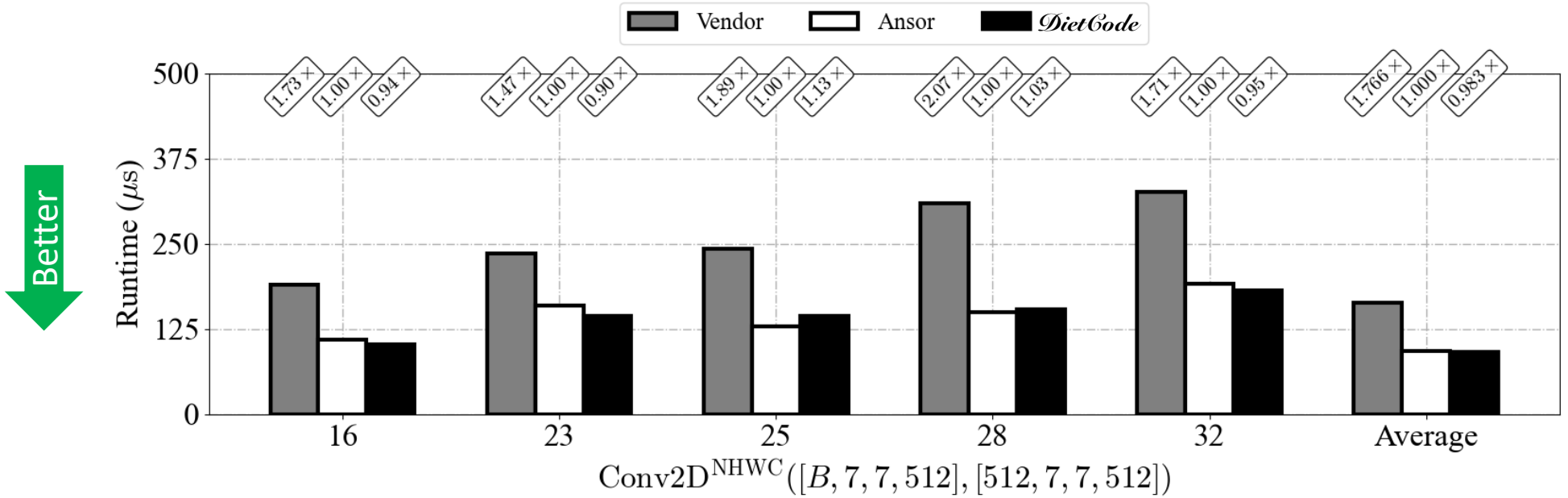


Up to $\mathbf{1.52\times}$/$\mathbf{1.26\times}$ better than Ansor/Vendor ($\mathbf{1.16\times}$/$\mathbf{1.11\times}$ on average).

[1] https://www.nvidia.com/en-us/geforce/graphics-cards/30-series/rtx-3090-3090ti/
[2] L. Zheng et al. *Ansor*. OSDI 2020

Conv2D

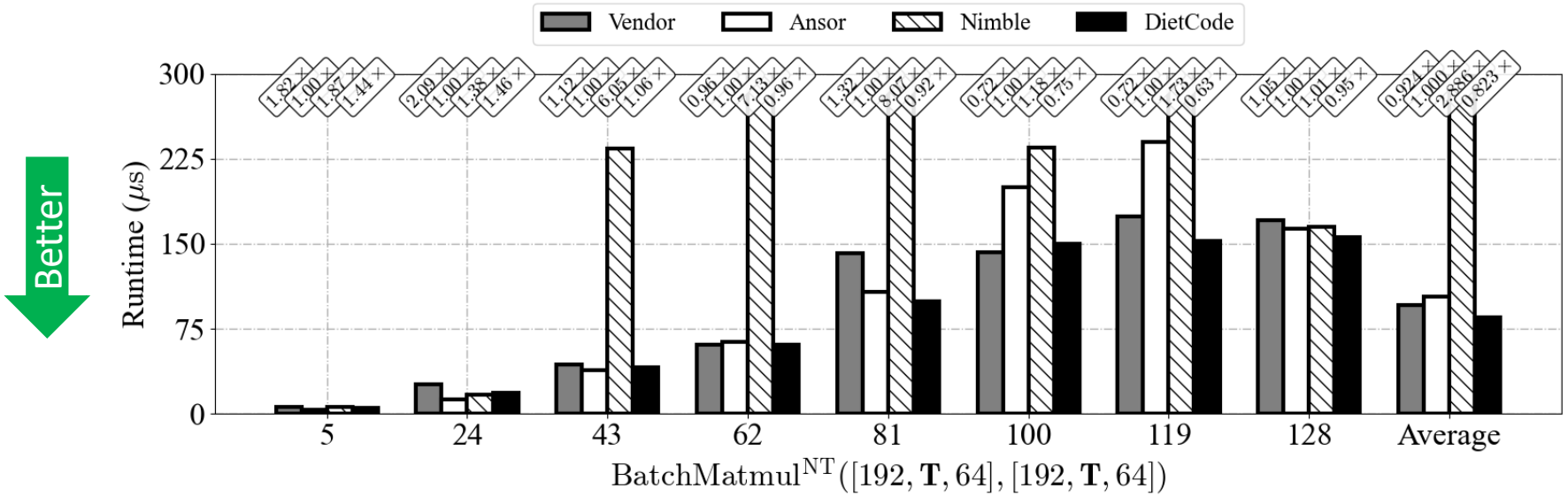
- NCHW is usually implemented using the Winograd algorithm, which is in essence batched matrix multiplies.
- NHWC:



Up to $\mathbf{1.11}\times/\mathbf{2.01}\times$ better than Ansor/Vendor ($\mathbf{1.02}\times/\mathbf{1.80}\times$ on average).

vs. Nimble [1]

- Focuses on the **runtime system** for dynamic-shape workloads, with one section (i.e., Section 3.5) discussing about the code generation.



Nimble cannot cover all shapes efficiently.

[1] H. Shen, J. Roesch et al. *Nimble*. MLSys 2021

Local Padding vs. Loop Partitioning

- Common:
  - Key Observation: Out-of-boundary checks in the **compute** stage are what negatively affect performance the most.
  - Performance difference is usually less than 5%.

Local Padding vs. Loop Partitioning

Local Padding

- Key Idea: Pads tensors by the size of the local workspace when loading from the off-chip device memory.

(-) Redundant computations

Loop Partitioning

- Key Idea: Partition the regions that have predicates and regions that do not.

(-) Cannot remove overheads in some pathological cases.

(-) Cannot support compute intrinsics such as the tensor core operations.

Bit-serial Weight Pools: Compression and Arbitrary Precision Execution of Neural Networks on Resource Constrained Processors

- Shurui Li
- Puneet Gupta

View on https://mlsys.org

MLSys 2022