Points	Grade

Team: XX

MatNr. First SECOND #1
MatNr. First SECOND #2
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Digital Integrated Circuits Lab (LDIS)

384.088, Summer Term 2019

Supervisors:
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Task 1: Digital Waterscale

1 Problem statement

Your goal is to design a system that reads data from an accelerometer, performs simple digital signal processing on captured data, and outputs the processed signal via light emitting diode (LED) bar (Figure 1).

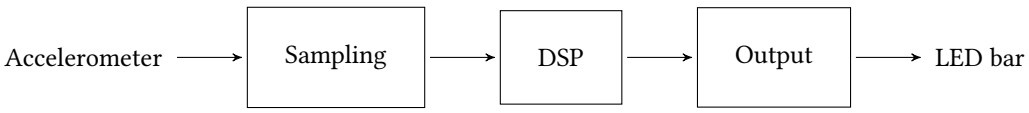

Figure 1: Block diagram of the system

You have to design three intellectual property (IP) cores:

1. Data sampling: This IP core controls and reads the output of the accelerometer, and provides the sampled data of a pre-defined sample rate at its output. The sample rate should be adjustable pre-synthesis. The accelerometer signal's resolution should be 12-bit.
2. The digital signal processor (DSP) core should implement an algorithm that calculates the angle of the board relative to the horizon in the axis of the LED bar.
3. The output stage takes the calculated angle, and transforms it into a thermometer-encoded signal that is provided to the LED bar. If the LED bar is parallel to the horizon, all LEDs should be turned off. If the led bar is tilted perpendicular both to the horizon and the ground, the entire upper portion of the LED bar should be turned on. If the angle of the board is between 0 and 90 degrees, the corresponding share of the LEDs should be turned on.

Design the system using either VHDL or Verilog. You can use third-party intellectual property (3PIP), but you have to fully understand what you are doing, and you have to cite the original source.

2 Team management

You can solve the problem on your own, or you can team up with others in order to share work and knowledge. If you team up, it is essential that you understand every aspect of the solution, rather that just the part that was implemented by you. In any case, use *git* to organize collaboration, even in case you work alone. We will assess your activity in the project based on your commits.

3 Proposed solution

Model the system in any hardware description language (HDL) of your choice. Design a testbench with reasonable test cases, and verify the design's functional correctness by simulating your design. Use any simulator you prefer, however, support is only provided for *ghdl*, *Verilator*, *Icarus Verilog*, and *xsim*. You can use free and open-source tools for modeling, simulation and synthesis. However, for technology mapping and bitstream generation (i.e., *implementing* the design), you will need *Vivado*. Implement the design on the Nexys 4 DDR board.