The VSC8486: A 10 GbE, Low-Power PHY for Synchronous Ethernet Applications

Application Note

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1 Introduction

The VSC8486 10G Transceiver is a low power (700 mW LAN mode) PHY device that is being used by network vendors to develop high port density network equipment for time sensitive synchronous communication in the transmission of voice, video, and data services over a single converged Ethernet link, referred to as “Synchronous Ethernet”. This application note explains the basic implementation scheme and operation of the VSC8486 running in both a conventional mode and enhanced mode of operation in Synchronous Ethernet applications. It is seen that the feature set of the VSC8486 is well suited to a straight forward implementation of Synchronous Ethernet at the PHY layer.

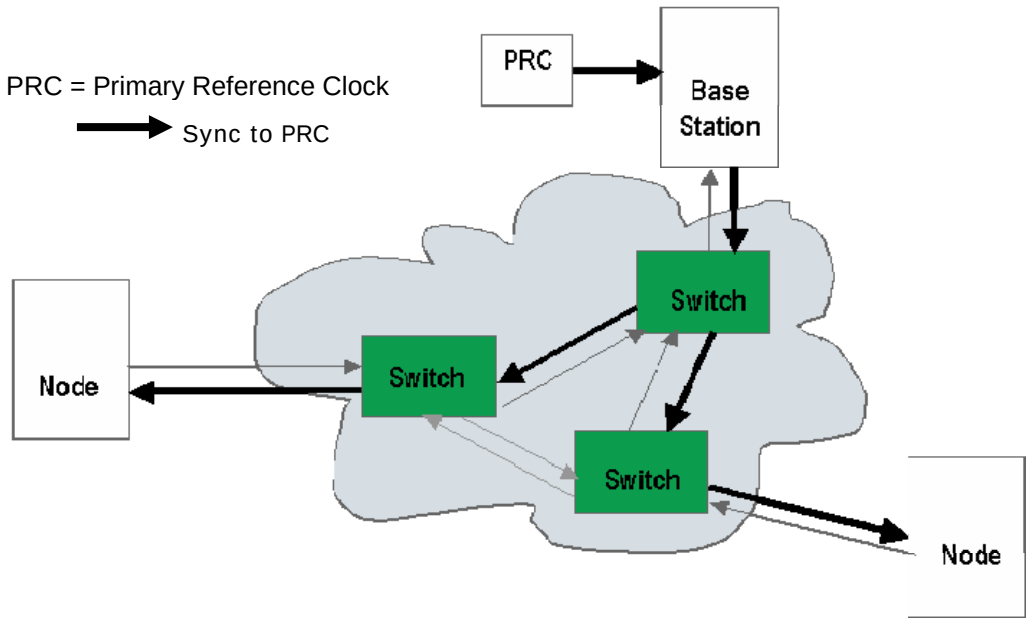
2 Synchronous Ethernet

When traditional TDM-based telecommunication applications are ported over to Ethernet, there are certain applications that require the transport of accurate and synchronous frequencies. These include networks for cellular communication, circuit emulation services (CES), streaming video, and VoIP. As an example, a cellular phone application requires base-stations with a highly accurate frequency reference at the PHY layer to derive the transmission frequencies. If adjacent cellular sites have different frequency references, mutual interference could occur.

In other applications involving the use of wall clock timing, a Synchronous Ethernet approach may also be employed to provide a highly accurate frequency reference that can be used by a higher layer protocol, such as IEEE-1588, to distribute message frames containing a master clock timestamp for network synchronization. Here again distribution of a highly accurate reference frequency at the PHY layer becomes an important element for supporting higher layer synchronization schemes.

The basic clock distribution scheme for implementing Synchronous Ethernet is illustrated below in Fig 1. A Primary Reference Clock (PRC) is used at the base station for distribution to the various nodes of the network over the data links. In order to implement such a distribution scheme at the PHY layer, the receiver needs to extract the clock from the input data and reuse it to transmit the data to other switches and nodes in the network. In this way, the whole network can be synchronized to a single PRC clock.

Figure 1. Propagation of Data Synchronized to a Primary Reference Clock



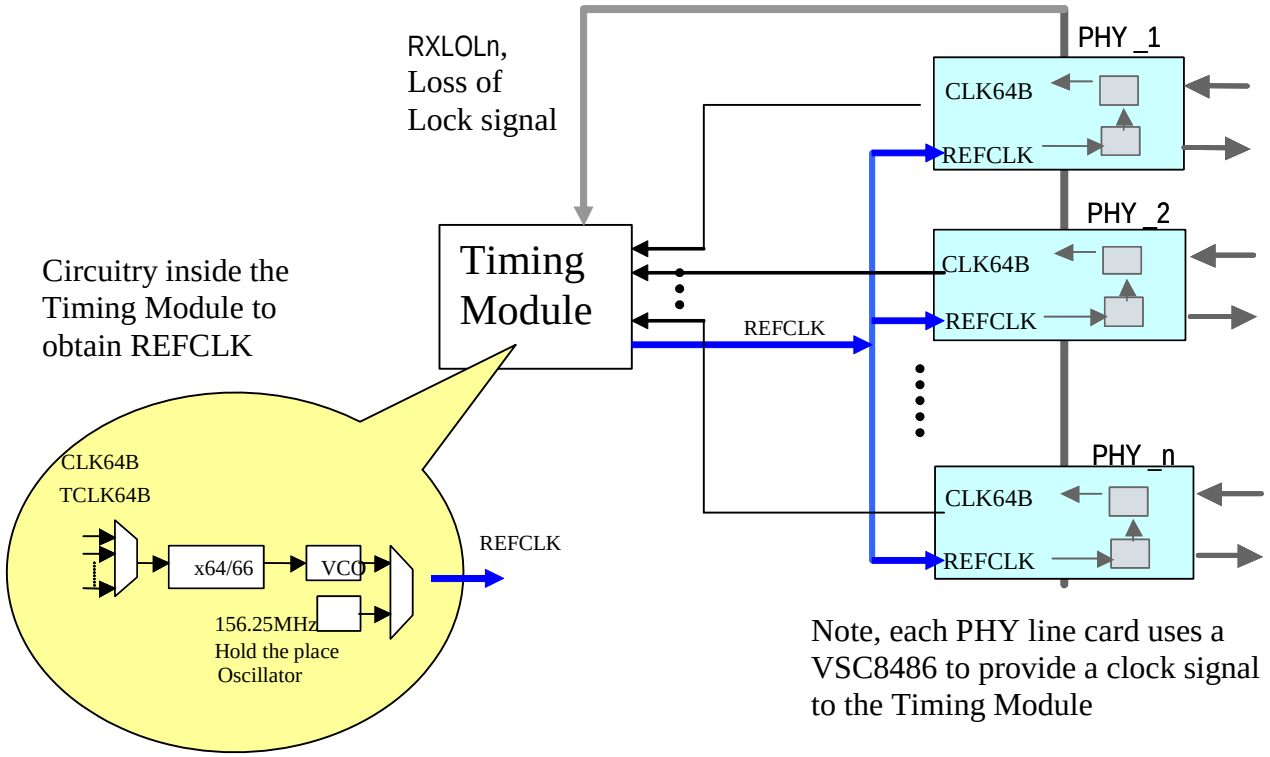
3 Synchronous Ethernet Design using the VSC8486 in Conventional Mode

The distribution of clock signals within a Synchronous Ethernet network employing the VSC8486 running in conventional mode is shown in Fig 2. The VSC8486 facilitates the implementation of Synchronous Ethernet by taking the recovered clock from the XFI input data and making it available for transmission to the other nodes through the Ethernet physical layer.

The tasks involved in synchronizing the CMU transmit clock to the CRU received clock consist of the following:

1. Recover the clock from XFI input in each line card
2. Indicate the recovered clock is stabilized
3. Select the recovered clock from the different line cards
4. Translate the recovered clock frequency to the reference clock frequency.
5. Clean up the jitter of the recovered clock
6. Distribute the recovered clock as the transmit clock to all other PHYs

Figure 2. Clock Path Distribution with the VSC8486 in Conventional Mode



The operation of the VSC8486 in each of the PHY line cards involves the following:

1. The CLK64B output from the VSC8486 can be programmed to be a divided by 64 recovered clock from the rate of the XFI input data. The register bit 1xE602.5 is set to high to enable the CLK64B output and the register bits 1xE602.4:3 are set to 00 to select the CLK64B to be divided by 64 from the input data rate.

2. Before the recovered clock of a particular line card is selected to be the system REFCLK, and hence the transmit clock for all the line cards, the timing module needs to know if the particular recovered clock is stabilized and good to use. The signal, Receiver Loss of Lock (RXLOL), can be used and it can be read from register bit 2xEF03.12 in the VSC8486. Alternatively, the WIS_INTA/B pins can be configured to indicate such a LOL. The register bits at 2xEF05.12 (WIS_INTA) or 2xEF06.12 (WIS_INTB), are used to configure the WIS_INTA/B as the LOL indicator.

3. When the RXLOL of the VSC8486 indicates a good signal, the corresponding CLK64B becomes a candidate for selection as the system reference clock.

4. REFCLK is used for the transmit clock for the CMU and the hint clock for the CRU inside the VSC8486. Its frequency is 156.25MHz in LAN mode. However, the recovered CLK64B is 161MHz. As a result, the CLK64B has to be multiplied by 64 and then divided by 66 to obtain the required 156.25MHz clock.

5. The recovered clock in general will contain too much jitter to meet the XFI jitter generation specs if used directly as the REFCLK to the VSC8486. Hence, an external PLL is needed to clean up the jitter and provide a clean clock to the VSC8486.

6. All the line cards then use the clean output clock from the PLL as the REFCLK, which will in turn be the Tx clock of the CMU on each PHY. Therefore, the clock that is synchronized to the input data of the selected line card, will be distributed and propagated to the other systems.

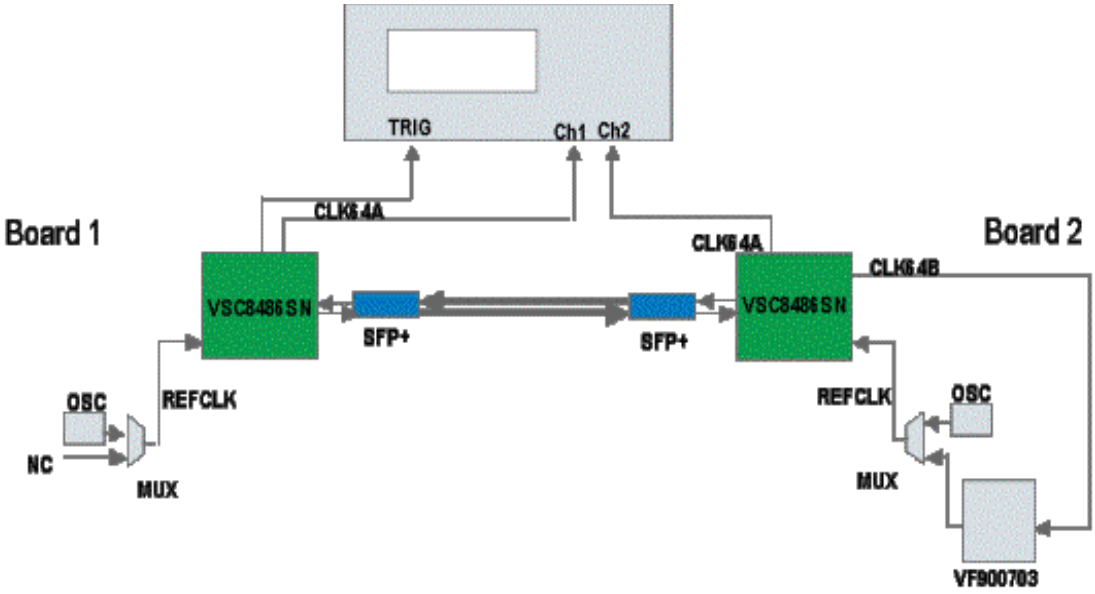
7. There is an issue in the conventional approach regarding the need for the REFCLK as the hint clock for the CRU of the PHY, since the recovered clock from the CRU is also used for the REFCLK for all the line cards including the same local PHY. This presents a "chicken and egg" issue in terms of how to initiate the synchronization process. In order to resolve this in the conventional mode, a "hold the place" clock source (usually an oscillator) must be used at start up as the initial REFCLK to allow the CRU to recover the clock from the XFI input data. Once the recovered clock is available, the external PLL will lock to it and clean up its jitter in order to provide the REFCLK. The clock source is then switched from the "hold the place" oscillator to this PLL output. The output of the PLL and the oscillator should be within 100ppm to provide an acceptable transient environment.

8. There are commercially available narrow band PLLs that can output 156.25MHz +/- 100ppm even when there is no input to lock on. Once an input clock signal is applied, the output of the PLL will be frequency locked to the input. A PLL that was found to successfully provide this feature is the VF900703 from Valpey Fisher. The VF900703 can also accept an input of either 161MHz or 156.25MHz to generate the required 156.25MHz REFCLK, thereby taking care of the frequency matching issue between the CLK64B and the REFCLK. (More on this in the next section)

4 Synchronous Ethernet Operation of the VSC8486 in Conventional Mode

A lab system was set up at Vitesse to demonstrate and evaluate the capability of the VSC8486 device in a Synchronous Ethernet application. The system consists of two VSC8486 line cards, connected together as illustrated in Fig 3. The REFCLK to the VSC8486 of Board #1 is from a local oscillator. The SFI output is connected to the SFI input of the VSC8486 of Board #2. The REFCLK of Board #2 is from the output of a Valpey Fisher VF900703 PLL. The CLK64A is programmed on both boards to be the CMU clock divided by 64.

Figure 3. Demo Setup with the VSC8486 Connected to a Narrow Band PLL



The CLK64A+ of Board #1 is connected to the scope through Channel 1 while the CLK64A- of Board #1 is connected to the scope as the trigger. The CLK64A+ of Board #2 is connected to the scope through channel 2. The optical link between Board #1 and Board #2 is not connected when powering up the system.

Upon power up, channel 1 is displayed on the scope as a steady signal since the scope is triggered by the same signal essentially. However, channel 2 appears unlocked and jumping around because the frequency source for board #1 is from a local oscillator; while the frequency source for board #2, is from the VF900703 PLL. These two sources are not locked until the optical link is inserted.

Once the optical connection is made, the recovered clock on Board #2 is derived from the data generated from Board #1, The recovered clock is used as the input to the VF900703, which then locks to this input. As a result, the VF900703 output and the REFCLK become locked to the input for synchronized use by the VSC8486 on Board #2. As a result, the CLK64A+ signal from Board #2 locks to the REFCLK of the Board #1 and its CLKA64+/- derivative. As expected, once the optical link is connected between the two boards, the channel 2 display is observed to be synchronized to channel 1 and not jumping anymore.

5 Synchronous Ethernet Design using the VSC8486 in Enhanced Mode

The Enhanced mode of the VSC8486 is designed to simplify the start up synchronization process by eliminating the transient REFCLK requirement and the resulting need for a narrow band PLL These enhancements include:

1. Separate reference clock source signals are provided for the PMA's CMU and CRU as well as for operation of XAUI:

a) CRU of PMA – can use REFCLK, WREFCLK, and VREFCLK; (Note, the REFCLK is recommended for SyncE applications).

b) CMU of PMA – can use REFCLK, WREFCLK, VREFCLK, and internal recovered clock; (Note, VREFCLK. is recommended for SyncE applications)

c) XAUI Block – can only use REFCLK

2. New MUXs and register bits added for more flexibility in controlling the clock sources to the different blocks of the VSC8486, thereby facilitating implementation of synchronous Ethernet:

a) Register 1xE602.2 – Clock Mode Override. When this bit is enabled, the 1xE604 can be used to program the clock sources used by the CMU and CRU.

0 = Disable the mode override (default)

1 = Enable the mode override

b) Register 1xE604.15.0

Bit 8:0 - Reserved.

Bit 7- Clock source for CMU in Linetime mode when 1xE602.2=1 and Linetime=1

0 = Reserved

1 = CMU clock is from the CRU recovered clock (div-by-64)

Bit 6:5 – Clock source to CRU when 1xE602.2=1

00 = Reserved

01 = Clock source to CRU is from WREFCLK input (div-by-64 clock)

1X = Clock source to CRU is from WREFCLK input (div-by-16 clock)

Bit 4:3 – Clock source to CMU when 1xE602.2=1

00 = Reserved

01 = Clock source to CMU is from REFCLK input

10 = Clock source to CMU is from CRU recovered clock (see bit 7)

11 = Clock source to CMU is from VREFCLK input

Bit 2:1 – selection of clock ratio for CMU when 1xE602.2=1

00 = div-by-64

01 = div-by-16

1X = divi-by-66

Bit 0 – selection of clock ratio for CRU when 1xE602.2=1

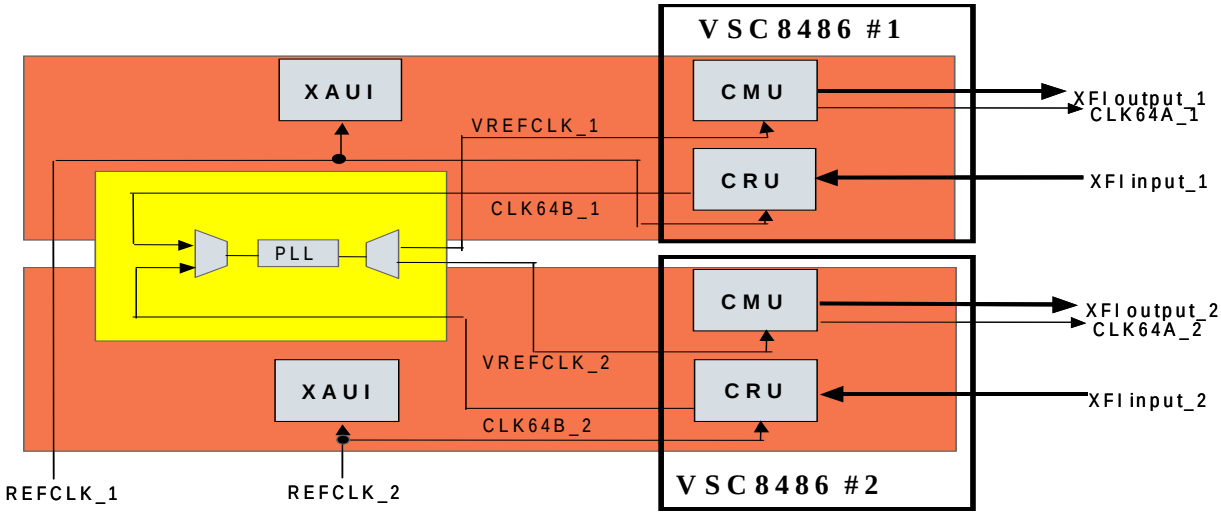
0 = div-by-64

1 = div-by-66

A major benefit of Enhanced mode is elimination of the transient period that occurs in the Conventional mode because the REFCLK must be used to recover the clock from the input data. Note, WREFCLK and VREFCLK can be /16, /64, or /66, while the REFCLK can only be /66. For better jitter performance, the /16 VREFCLK is preferred. The recovered CLK64B could be set to a PLL that takes in the CLK64B to provide a 4x CLK64B. A narrow band PLL would no longer be required and there would be no need to adjust a /66 REFCLK from a /64 recovered clock. The REFCLK and WREFCLK could be free running clocks from oscillators all the time. These new features should lead to a more cost effective implementation using a common PLL, as illustrated in Fig 4.

An even more cost effective solution can be provided by using the REFCLK for both the XAUI block and the clock source for the PMA's CRU, while leaving the WREFCLK unused. The VREFCLK can be selected to be at the same frequency as the CLK64B, i.e. 161MHz. A 1:1 or 1:4 PLL is still required to clean up the jitter from CLK64B to the VREFCLK input block. A free running clock source is needed for the PMA's CRU and the WREFCLK can be left unused.

Figure 4. Two Enhanced Mode VSC8486s in a Synchronous Ethernet Application

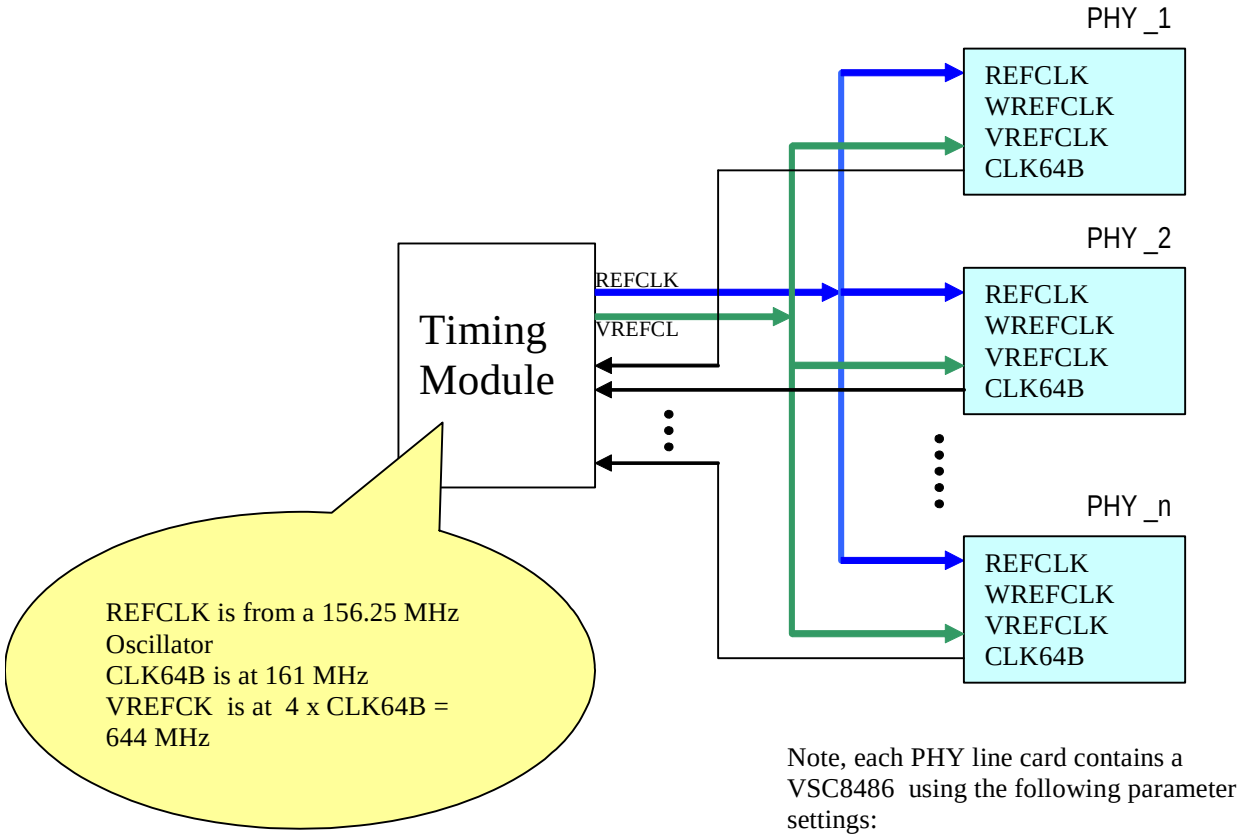


Note: REFCLK_1 and REFCLK_2 as well as WREFCLK_1 and WREFCLK_2 could be from the same clock source.

6 Synchronous Ethernet Operation of the VSC8486 in Enhanced Mode

The separate clocks to be provided in the Enhanced mode of the VSC8486 lead to the distribution of clock paths diagrammed below in Fig 5 for Synchronous Ethernet operation.

Figure 5. Clock Path Distribution with the VSC8486 in Enhanced Mode



The separate clocks and added MUX bits to be provided in the enhanced mode of the VSC8486 will simplify operation in SyncE applications. The expected operational procedure is as follows:

1. A free running oscillator based clock (156.25MHz) is used for the REFCLK that is used for the XAUI block and the hint clock of the CRU to recover the CLK64B from the XFI input data. This will be configured by setting the 1xE602.2 = 1, 1xE604.6:5 = 00, and 1xE604.0=1.

2. The CLK64B output is programmed to be a divided by 64 recovered clock from the rate of the XFI input data. The register bit 1xE602.5 is set to high to

enable the CLK64B output and the register bits 1xE602.4:3 are set to 00 to select the CLK64B to be divided by 64 from the input data rate.

3. The Receiver Loss of Lock, RXLOL, can be read from register bit 2xEF03.12 or program the WIS_INTA/B to indicate a LOL through register bit 2xEF05.12 (WIS_INTA) or 2xEF06.12 (WIS_INTB).

4. When the RXLOL of the VSC8486SN indicates a good signal, the corresponding CLK64B could be selected to be the reference clock.

5. For better jitter performance, a 644MHz VREFCLK input is used for the transmit clock for the CMU. The CLK64B is 161MHz and so it needs to be multiplied by 4 and the jitter is cleaned by an external PLL to achieve a 644MHz VREFCLK. The register bits, 1xE604.4:3 are set to 11 and 1xE604.2:1 are set to 01.

6. The PLL output which is phase locked to the CLK64B, will be distributed to the chip of all line cards, which will in turn be the VREFCLK that is the transmit clock of the CMU on each PHY. Therefore, the clock that is synchronized to the input data of the selected line card will be distributed and propagated to the other systems.

7. The REFCLK will be provided locally on the individual line card or fanned out from a timing module in the system.

Note, the above serves merely as a general guideline, realizing that a given application may have a specific and unique set of constraints in the actual operating environment.