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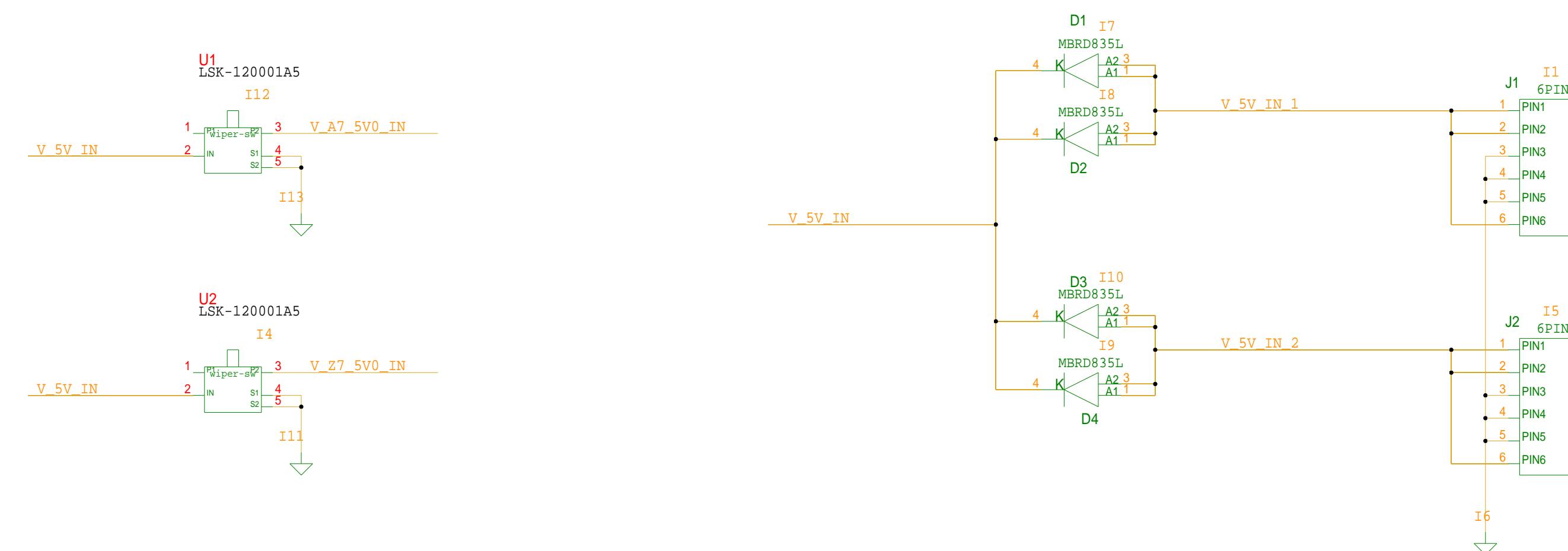
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MAIN POWER

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ARTIX-7 INDEX

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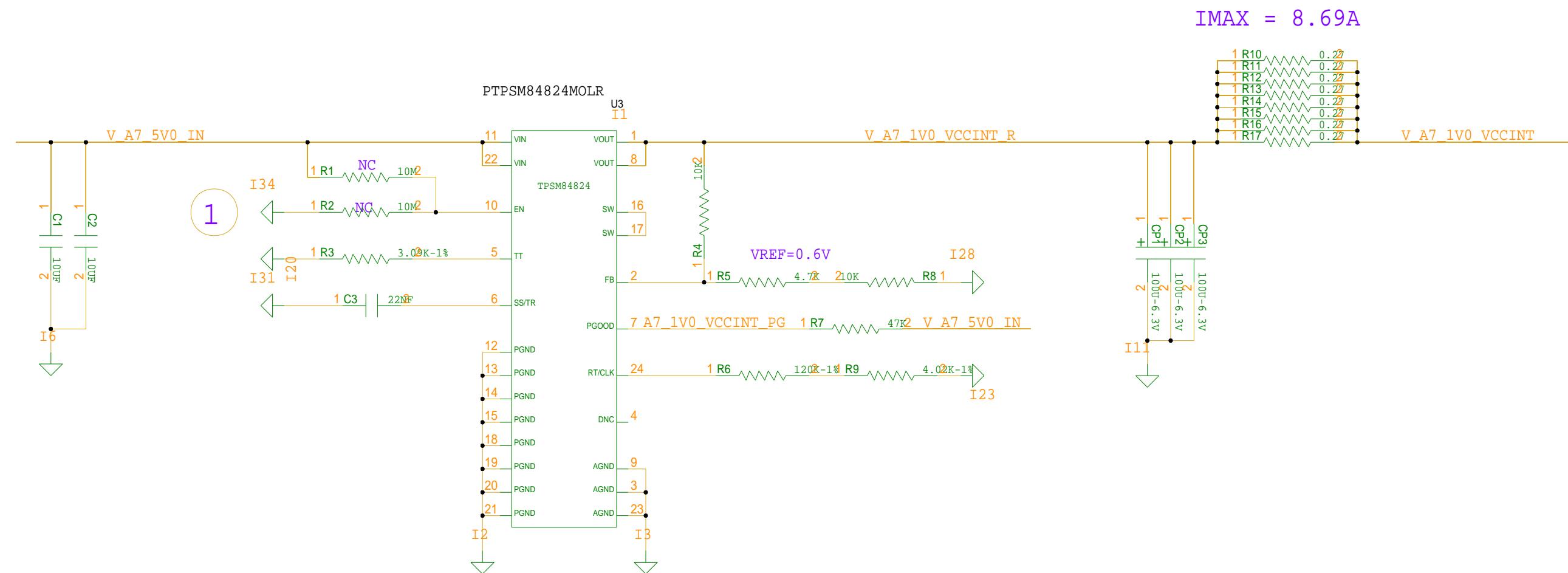
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ARTIX-7 POWER (1)



SS/TR	6	I	Soft-start and tracking pin. Connecting an external capacitor to this pin adjusts the output voltage soft-start ramp slower than its 1.2 ms default setting. A voltage applied to this pin allows for tracking and sequencing control.
-------	---	---	--

Table 9. Soft-Start Capacitor Values and Soft-Start Time

C _{ss} (nF)	open	10	15	22	47
SS Time (ms)	1.2	2.4	3	3.8	6.8

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ARTIX-7 POWER (2)

$$V_{OUT} = V_{REF} \times (1 + (R_{TOP}/R_{BOT}))$$

$$R_{RT} (\text{k}\Omega) = [14,822/f_{SW} (\text{kHz})]^{1.081}$$

$$V_{IN_STARTUP} = (0.8 \text{ nA} + (0.8 \text{ V}/R_{BOT_EN})) \times \left(R_{TOP_EN} + \frac{R_{BOT_EN} \times 1 \text{ M}\Omega}{R_{BOT_EN} + 1 \text{ M}\Omega} \right)$$

where:

R_{TOP_EN} is the resistor from V_{IN} to EN.

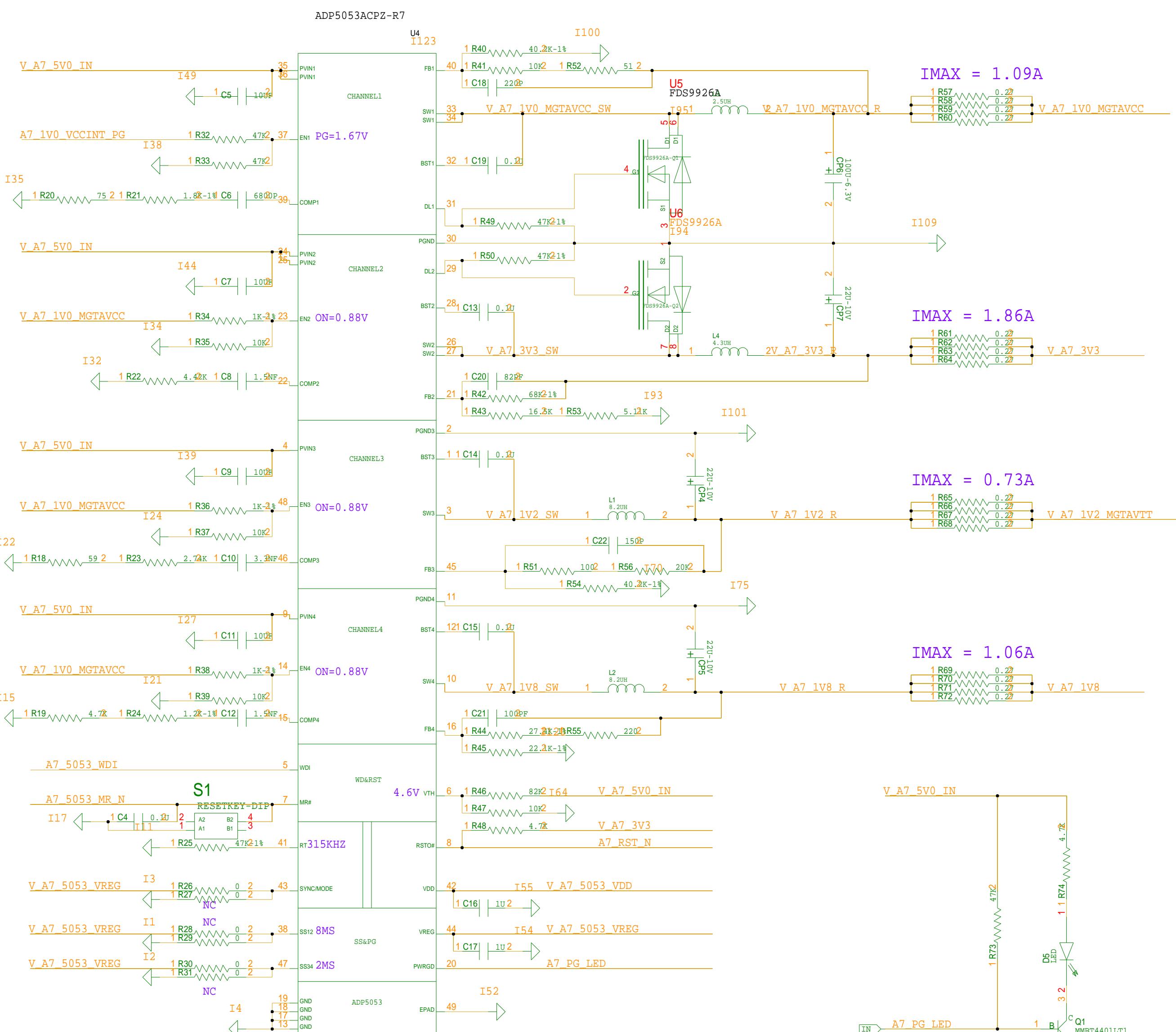
R_{BOT_EN} is the resistor from EN to ground.

Table 9. Soft Start Time Set by the SS12 and SS34 Pins

R_{TOP} (k Ω)	R_{BOT} (k Ω)	Soft Start Time			
		Channel 1	Channel 2	Channel 3	Channel 4
0	N/A ¹	2 ms	2 ms	2 ms	2 ms
100	600	2 ms	Parallel	2 ms	4 ms
200	500	2 ms	8 ms	2 ms	8 ms
300	400	4 ms	2 ms	4 ms	2 ms
400	300	4 ms	4 ms	4 ms	4 ms
500	200	8 ms	2 ms	4 ms	8 ms
600	100	8 ms	Parallel	8 ms	2 ms
N/A ¹	0	8 ms	8 ms	8 ms	8 ms

Table 16. Factory Default Options

Option	Default Value
Channel 1 Output Voltage	0.8V adjustable output
Channel 2 Output Voltage	0.8V adjustable output
Channel 3 Output Voltage	0.8V adjustable output
Channel 4 Output Voltage	0.8V adjustable output
PWRGD Pin (Pin 20) Output	Monitor Channel 1 output
Output Discharge Function	Enabled for all four buck regulators
Switching Frequency on Channel 1	1x switching frequency set by the RT pin
Switching Frequency on Channel 3	1x switching frequency set by the RT pin
SYNC/MODE Pin (Pin 43) Function	Forced PWM/automatic PWM/PSM mode setting with the ability to synchronize to an external clock
Hiccup Protection	Enabled for overcurrent events
Short-Circuit Latch-Off Function	Disabled for output short-circuit events
Oversupply Latch-Off Function	Disabled for output oversupply events
Reset Timeout Period	200 ms
Watchdog Timeout Period	1.6 sec
Manual Reset Input Mode	Processor manual reset mode



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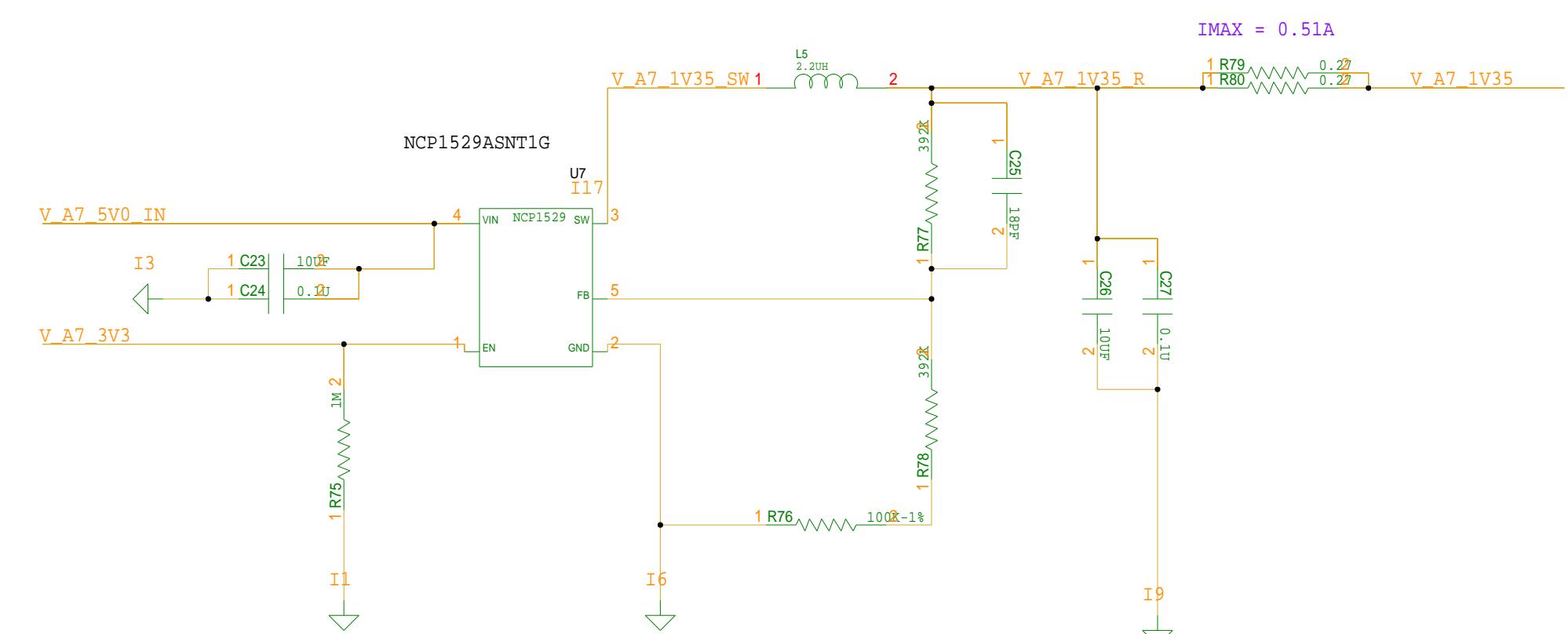
ARTIX-7 POWER (3)

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$$V_{out} = V_{FB} \times (1 + R1/R2)$$

- V_{OUT} : Output Voltage (V)
- V_{FB} : Feedback Voltage = 0.6 V
- $R1$: Feedback Resistor from V_{OUT} to FB
- $R2$: Feedback Resistor from FB to GND

4



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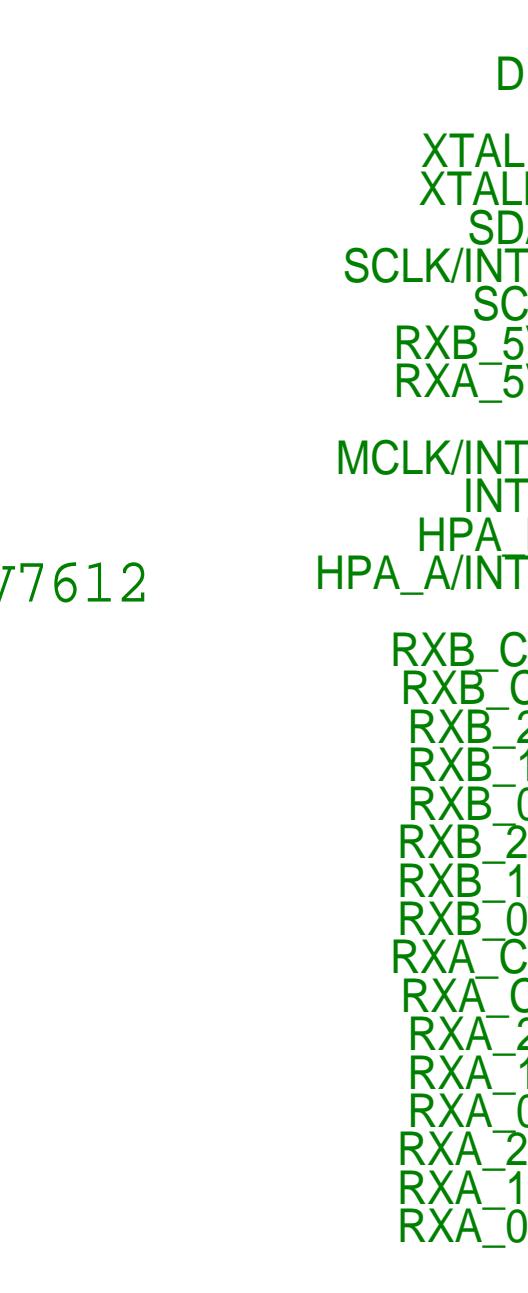
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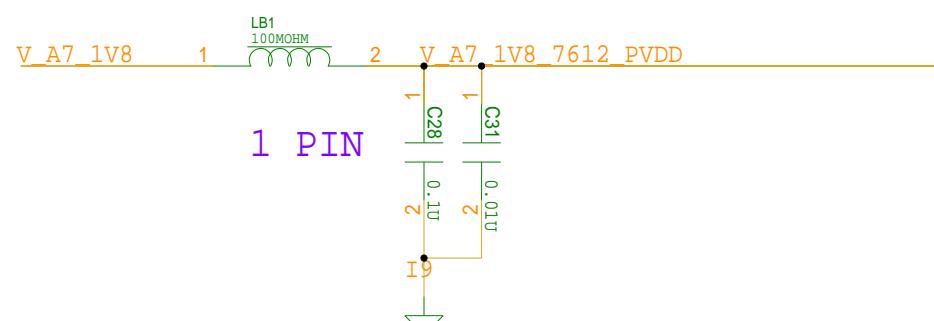
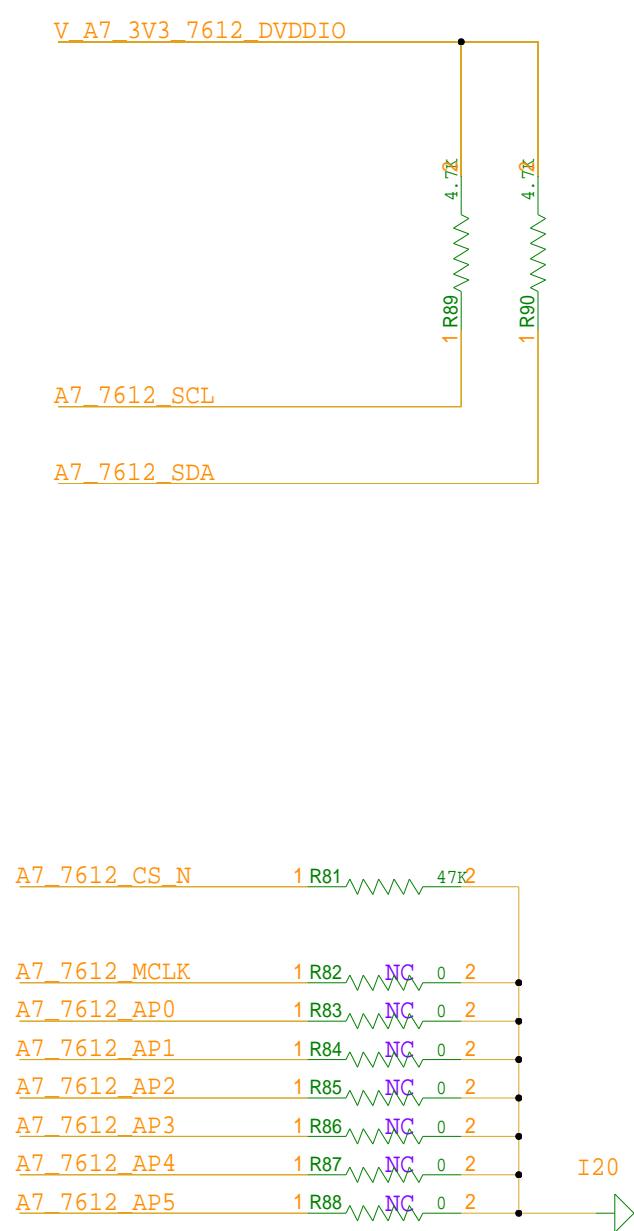
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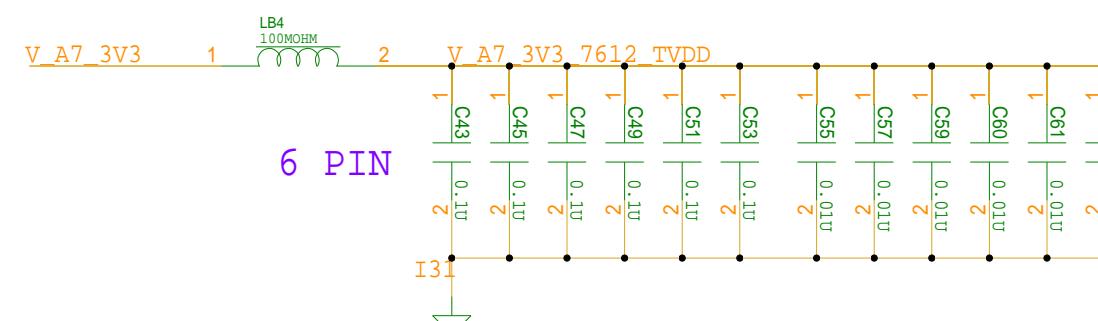
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U8



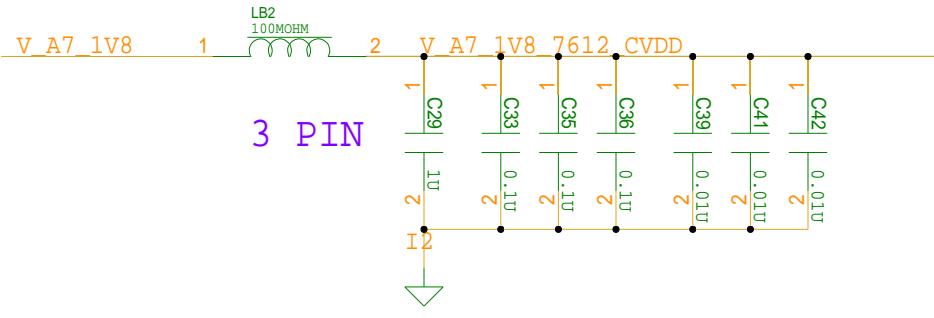
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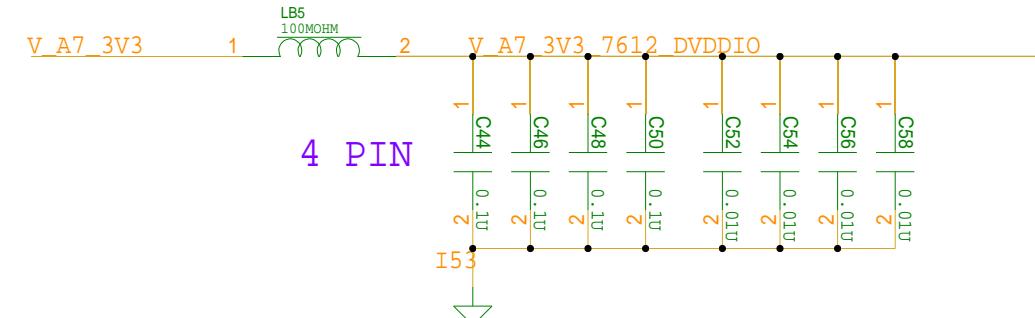
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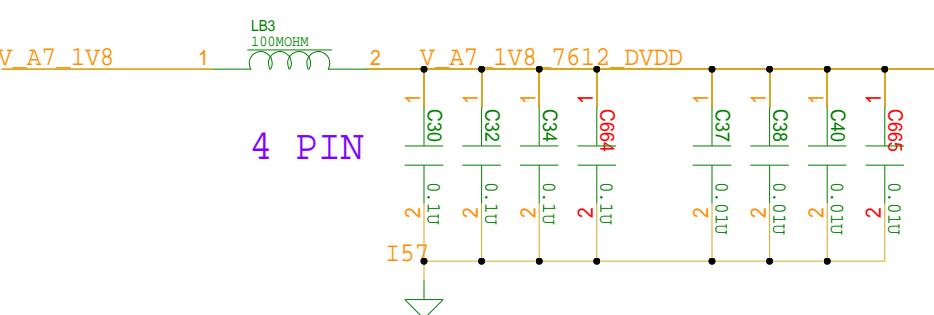
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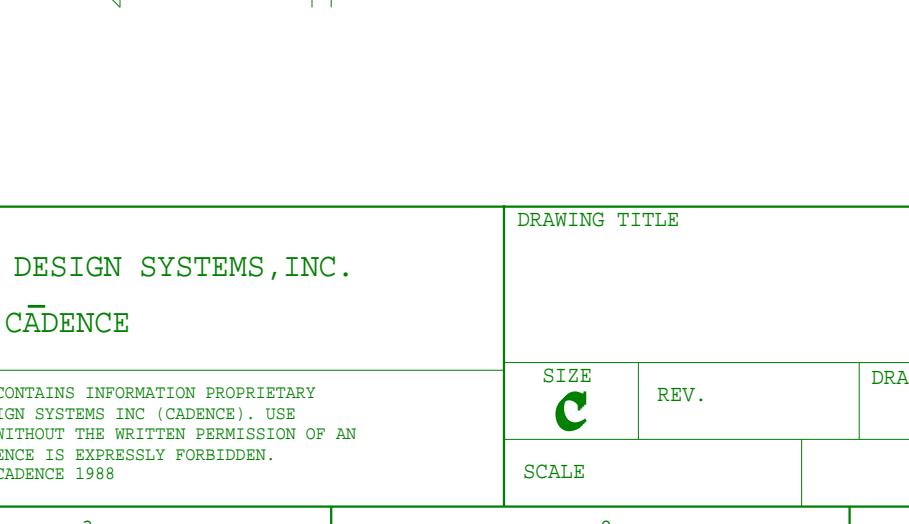
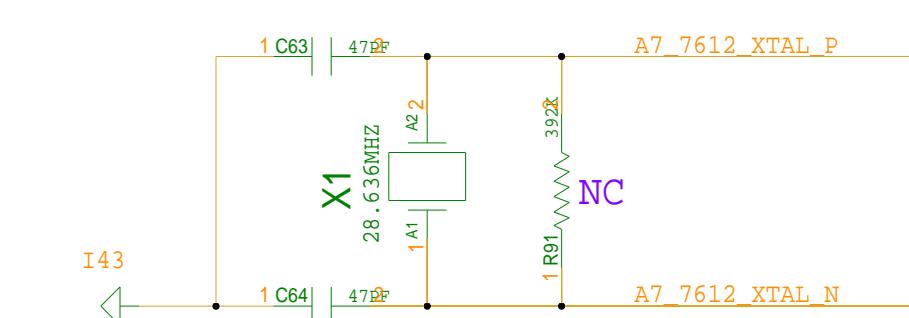
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4 PIN



4 PIN



ARTIX-7 HDMI RECEIVER (2)

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A7_7612_P3	66	P3
A7_7612_P4	65	P4
A7_7612_P5	64	P5
A7_7612_P6	63	P6
A7_7612_P7	61	P7
A7_7612_P8	60	P8
A7_7612_P9	59	P9
A7_7612_P10	58	P10
A7_7612_P11	57	P11
A7_7612_P12	56	P12
A7_7612_P13	55	P13
A7_7612_P14	53	P14
A7_7612_P15	52	P15
A7_7612_P16	51	P16
A7_7612_P17	49	P17
A7_7612_P18	48	P18
A7_7612_P19	47	P19
A7_7612_P20	46	P20
A7_7612_P21	45	P21
A7_7612_P22	44	P22
A7_7612_P23	43	P23
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A7_7612_P27	36	P27
A7_7612_P28	35	P28
A7_7612_P29	34	P29
A7_7612_P30	33	P30
A7_7612_P31	32	P31
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A7_7612_P34	28	P34
A7_7612_P35	27	P35



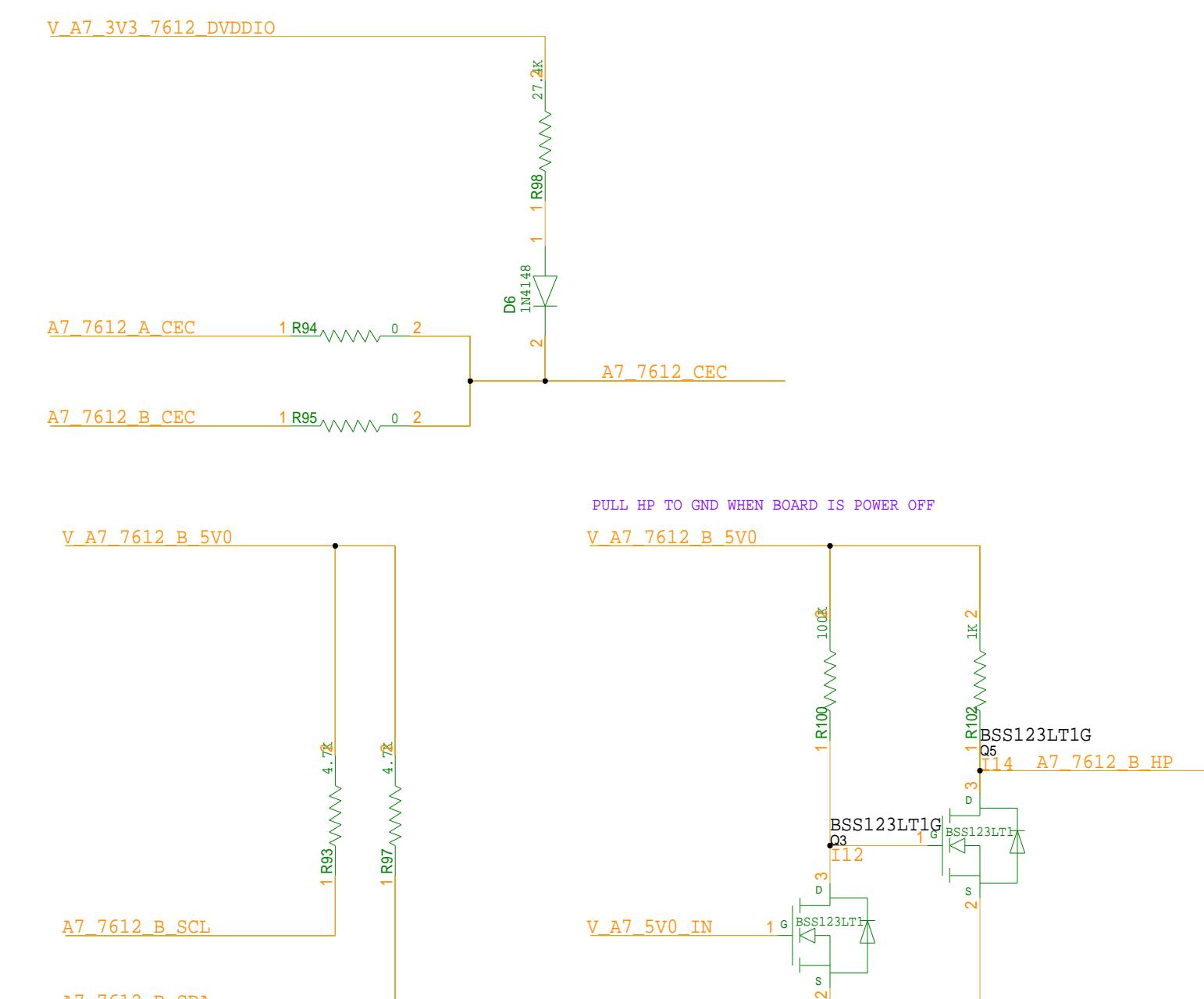
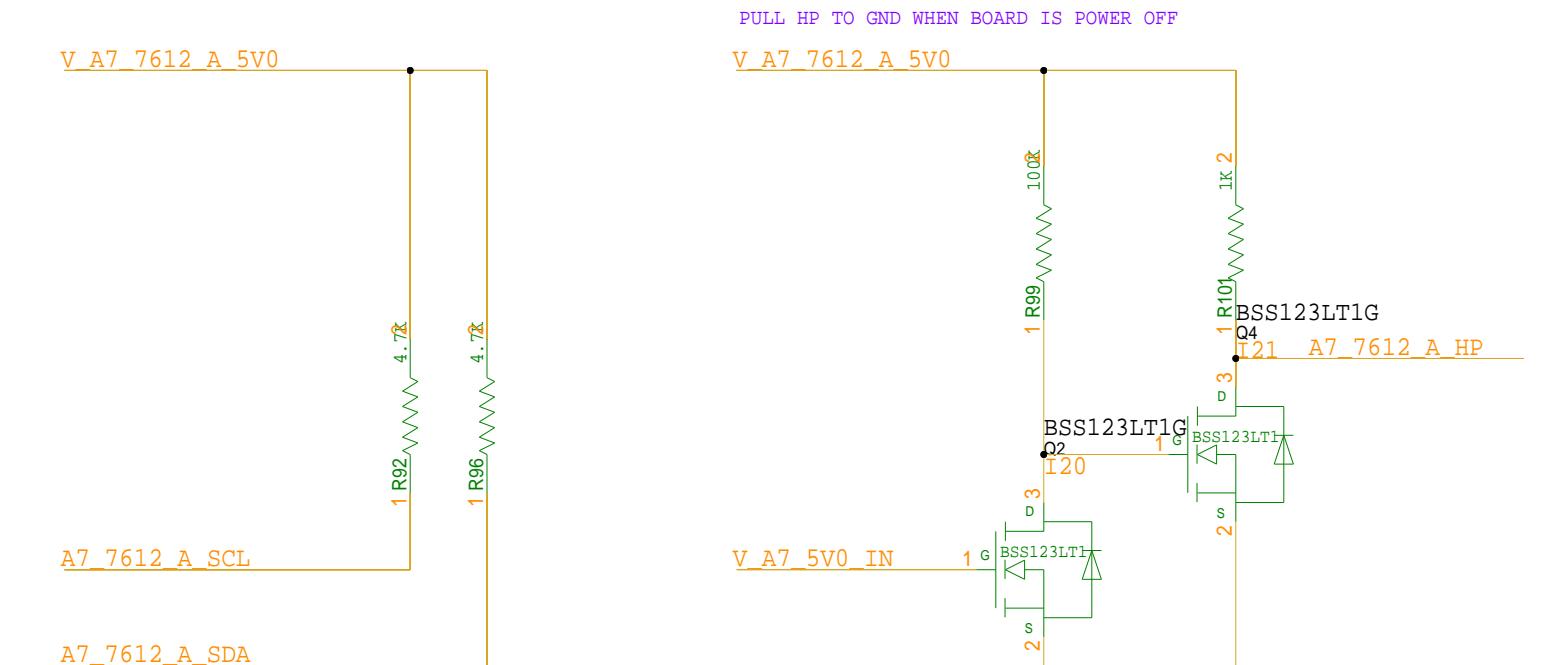
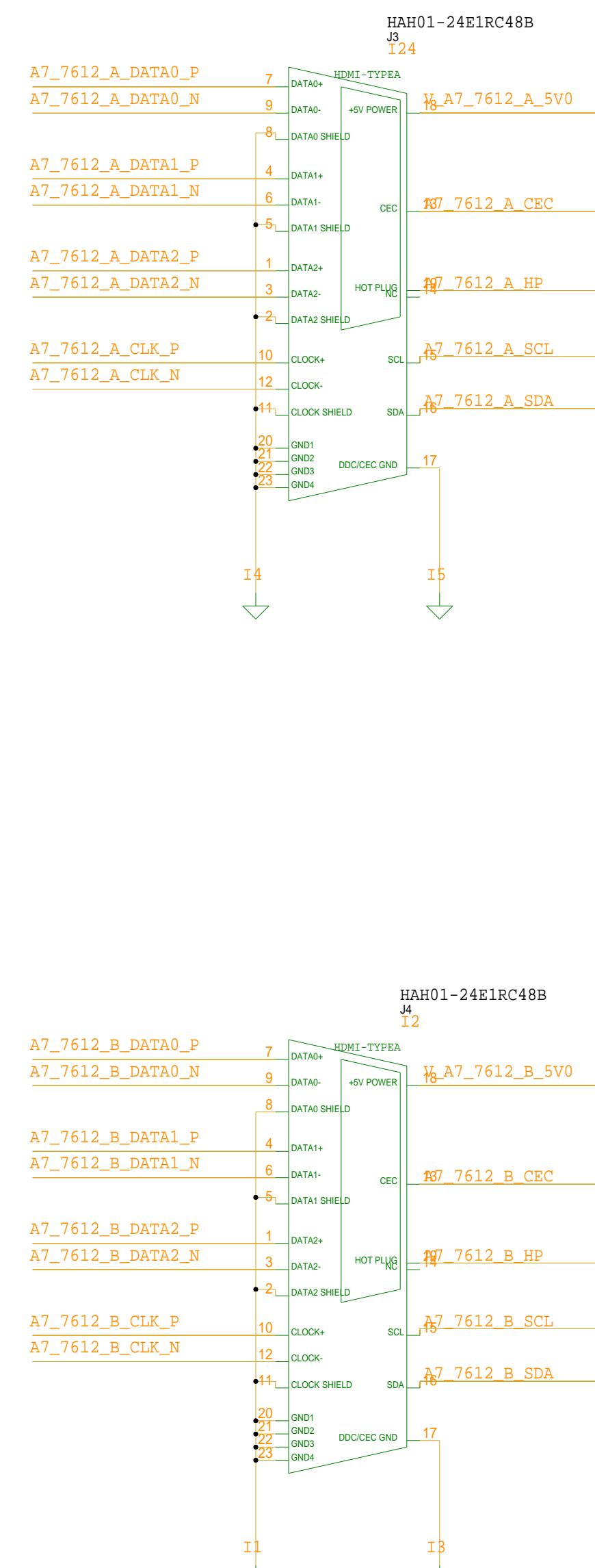
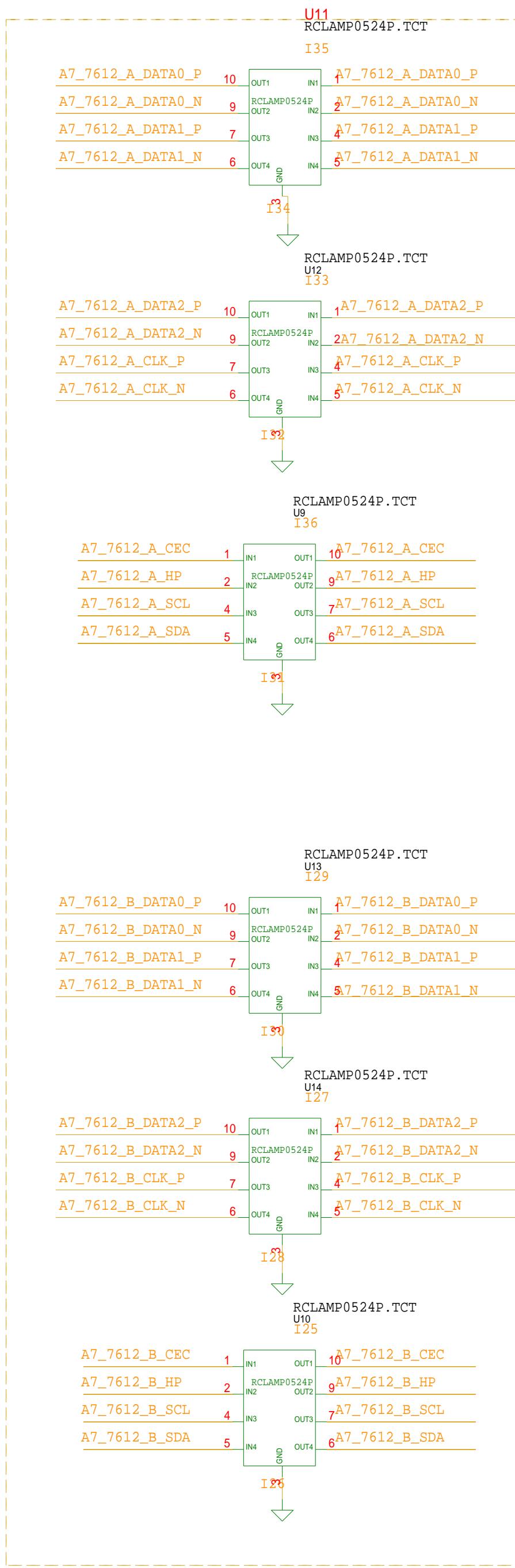
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ARTIX-7 HDMI RECEIVER (3)

CHANGE CONNECTION DUE TO LAYOUT

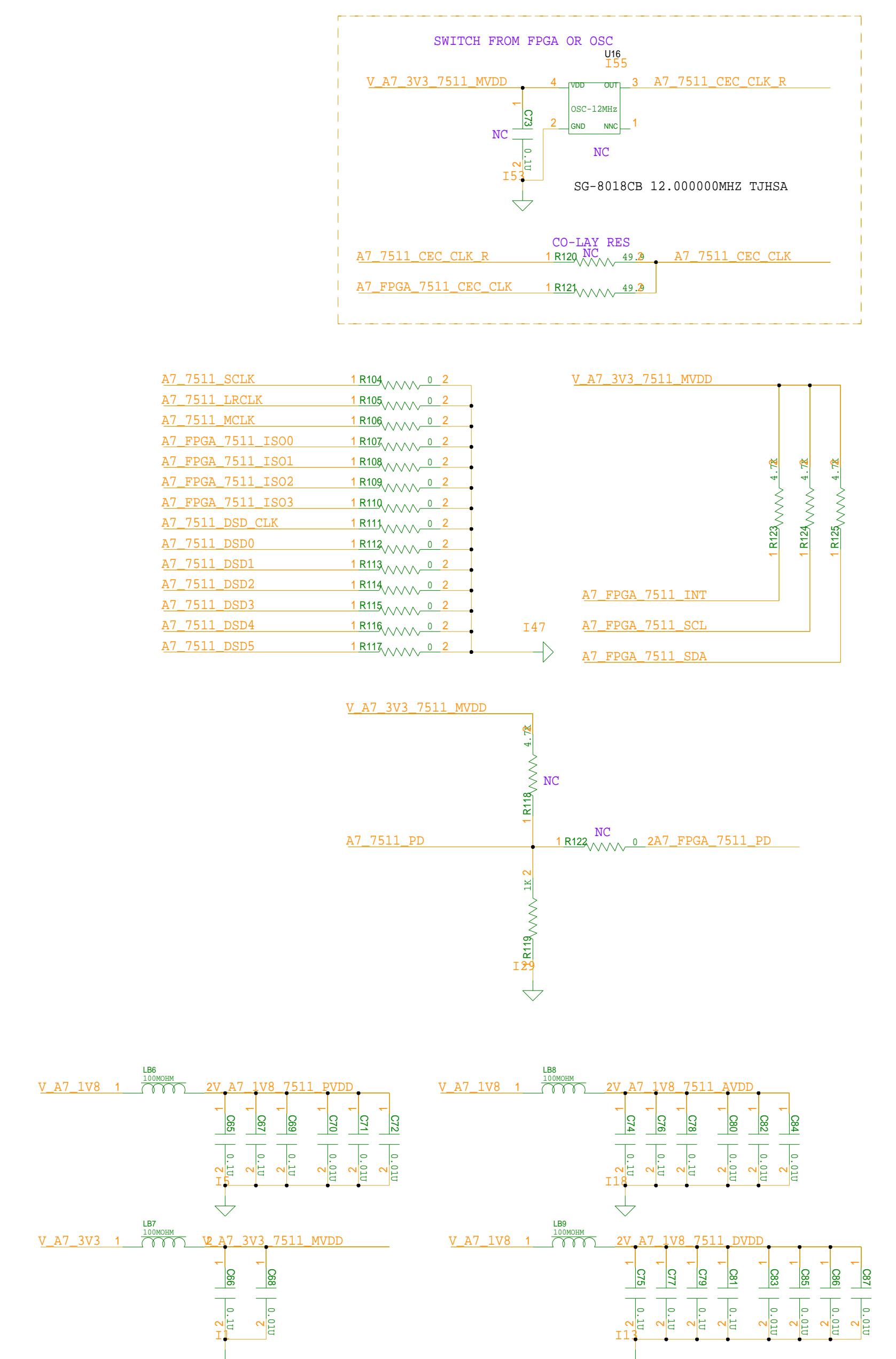
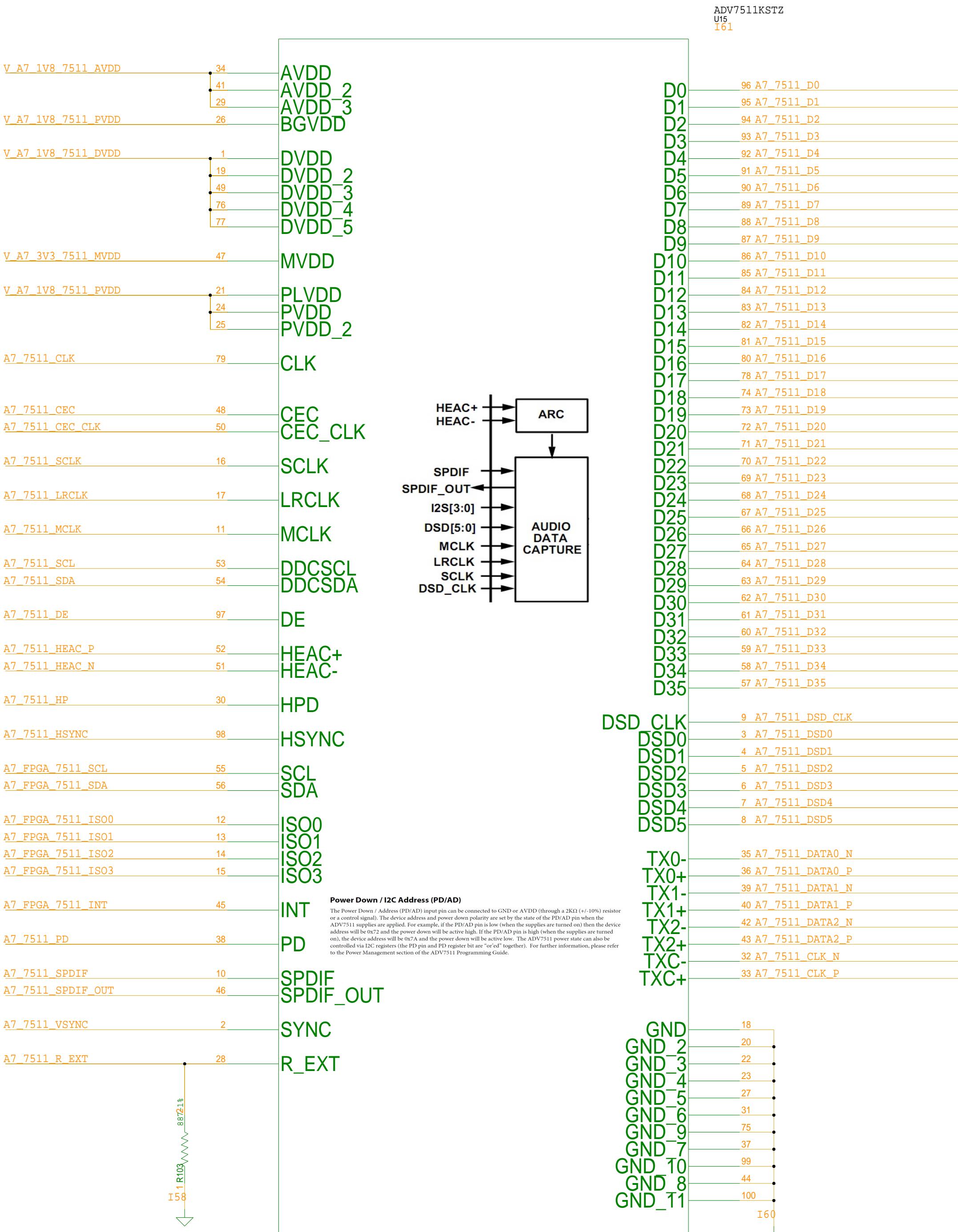


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ARTIX-7 HDMI TRANSMITTER(1)



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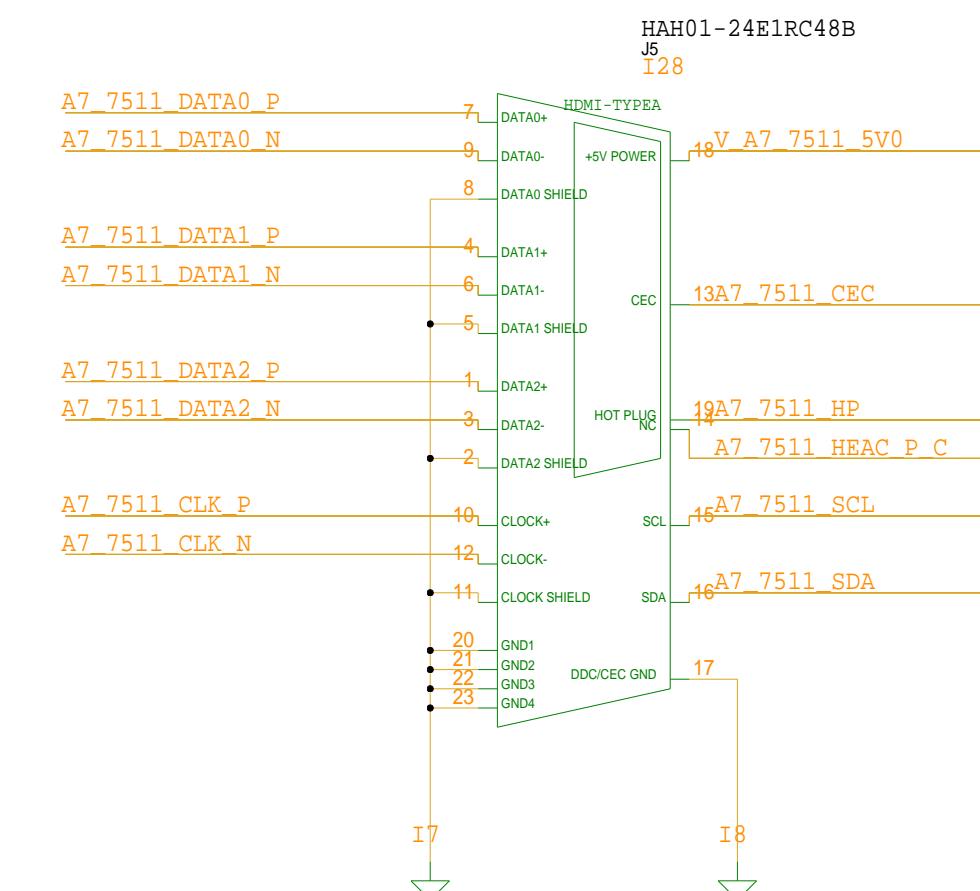
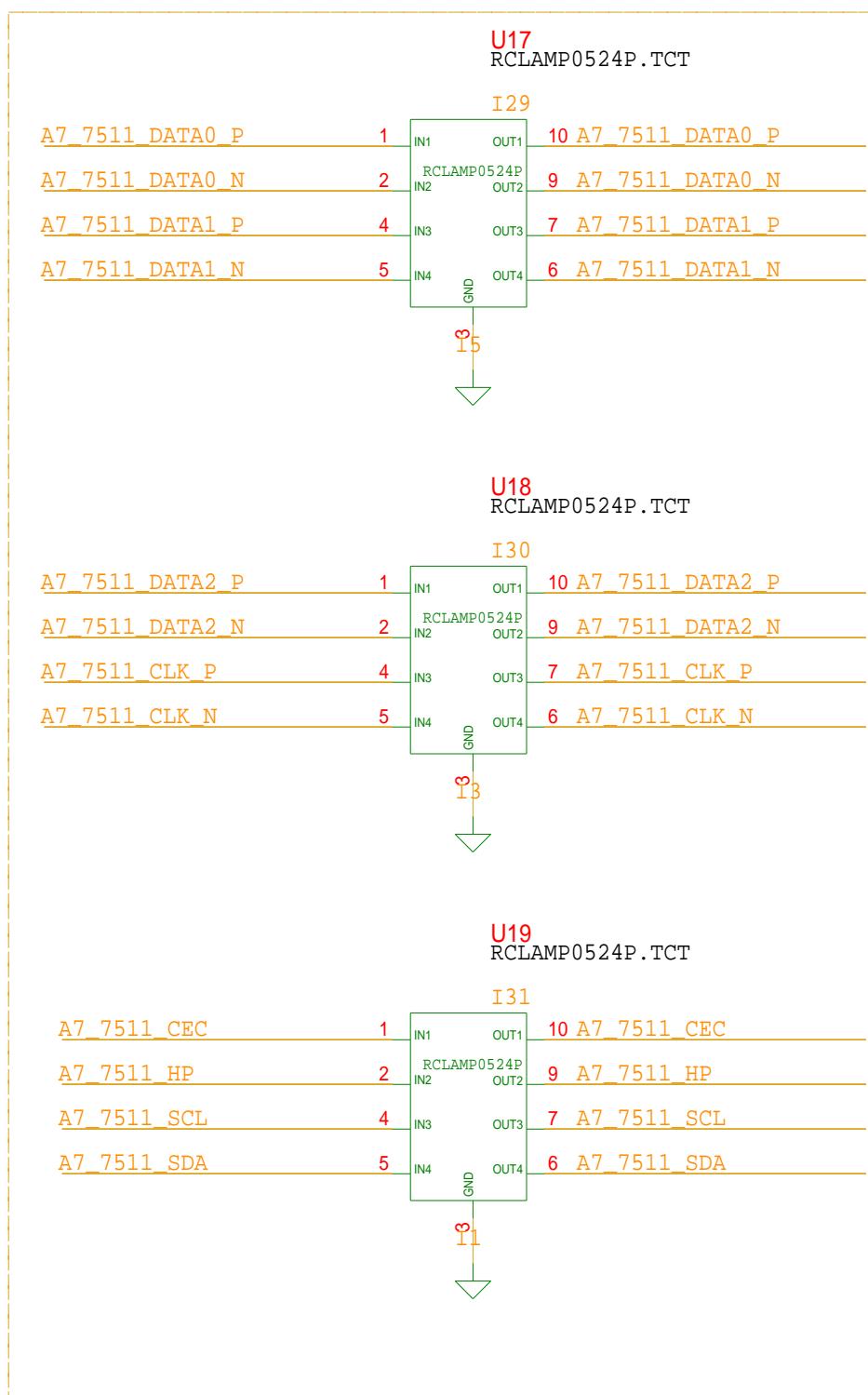
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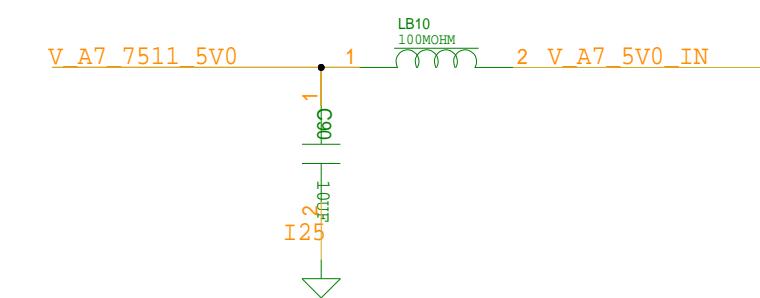
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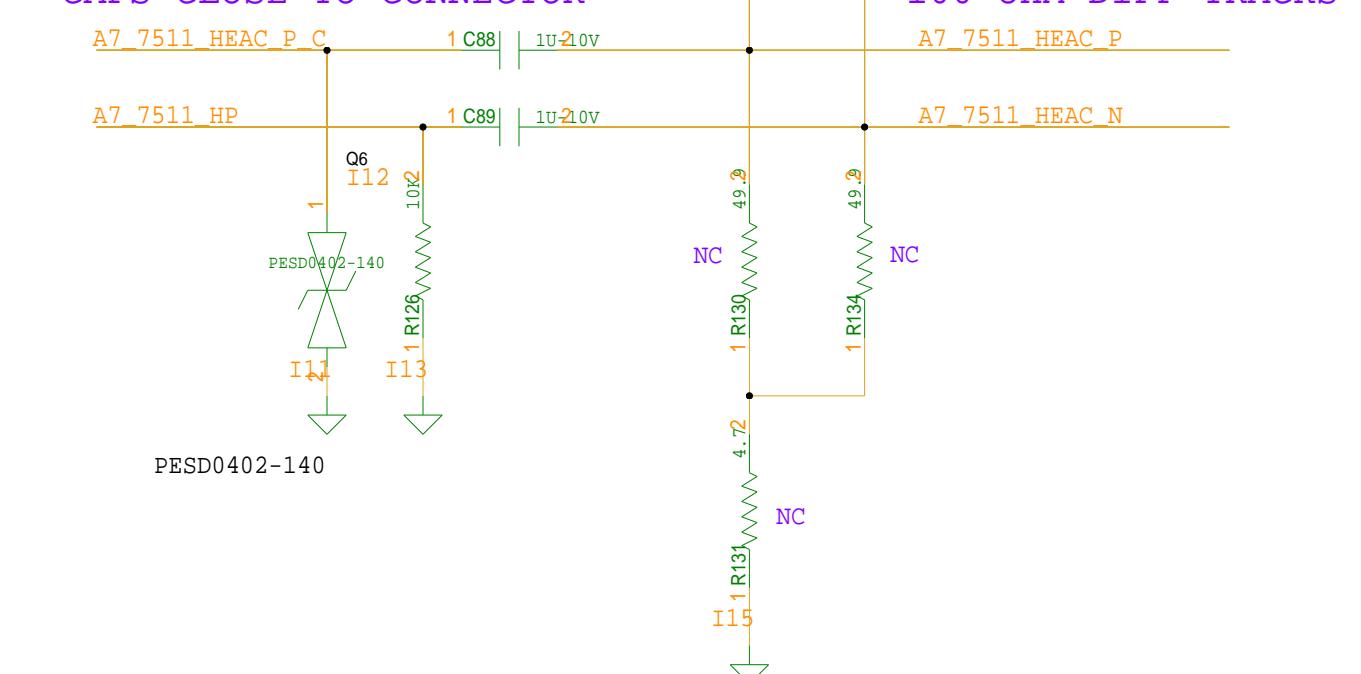
CHANGE CONNECTION DUE TO LAYOUT



CLOSE TO HDMI CONNECTOR



CAPS CLOSE TO CONNECTOR



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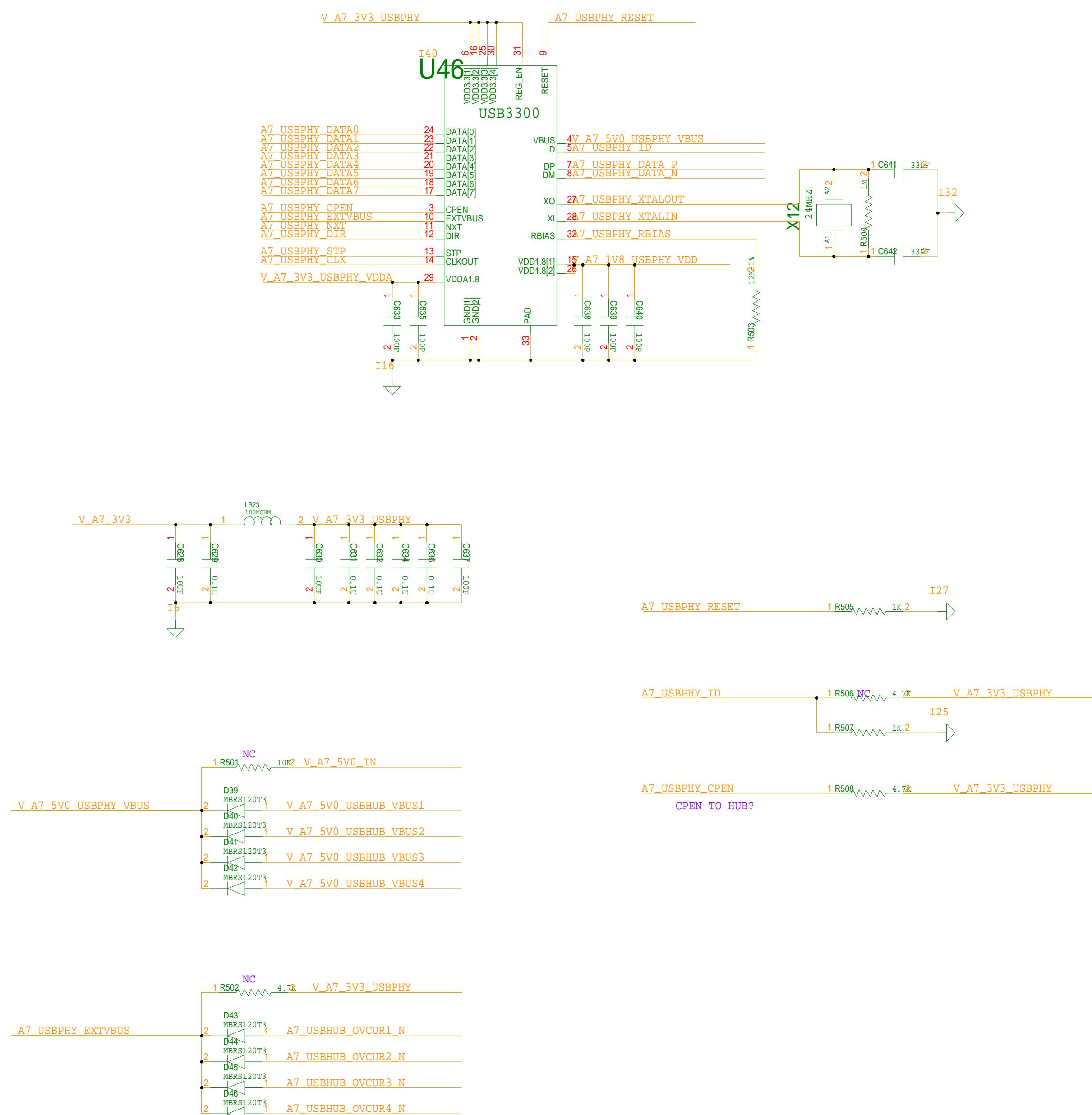
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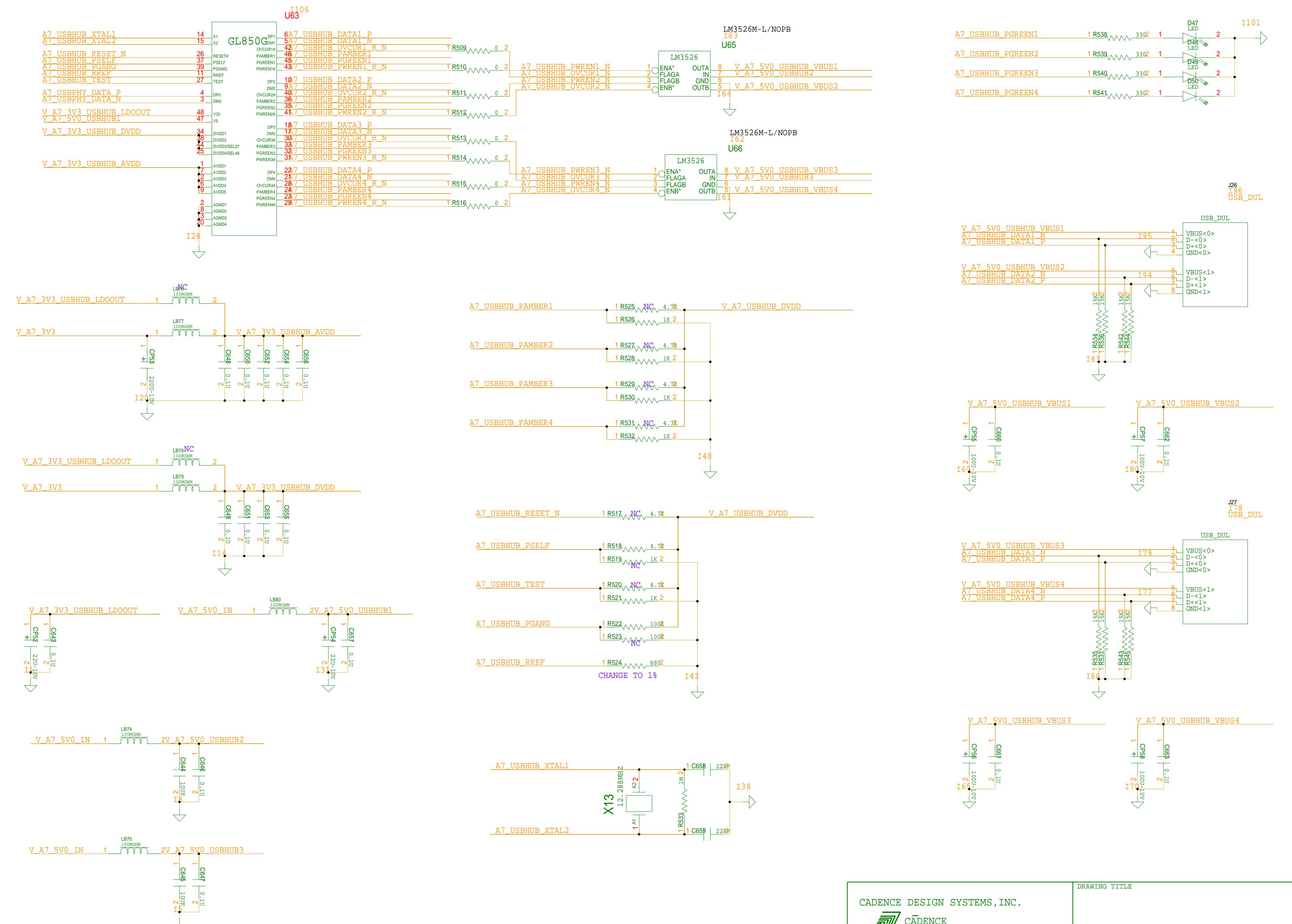
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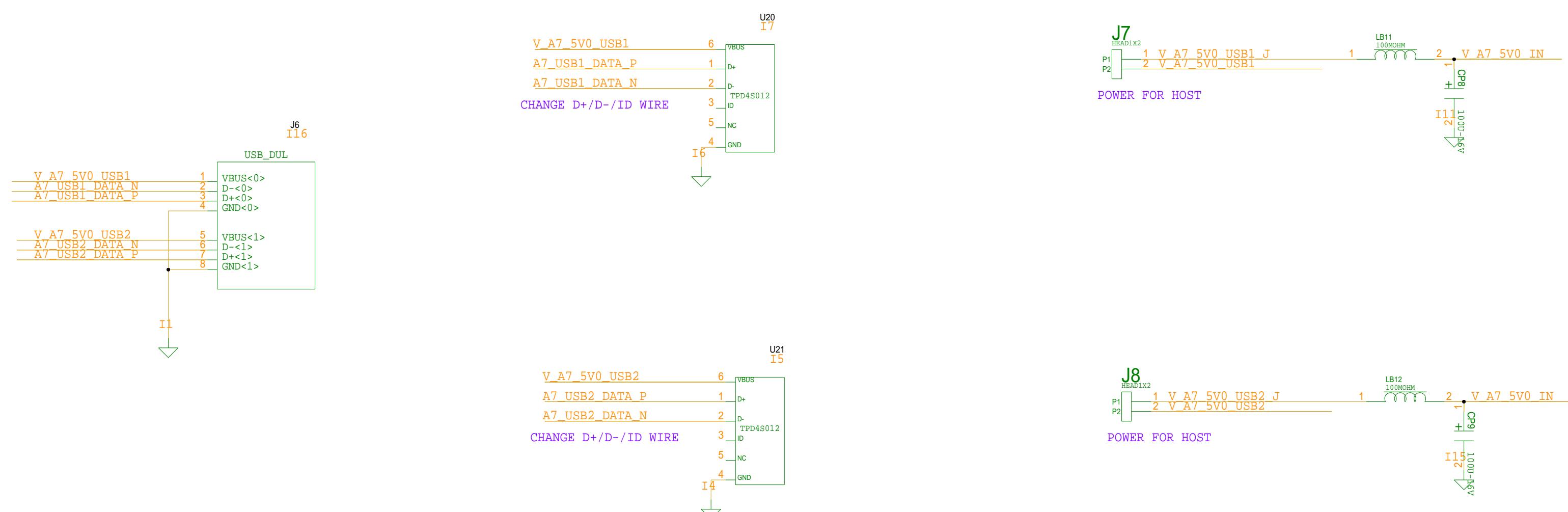
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ARTIX-7 USB INOUT

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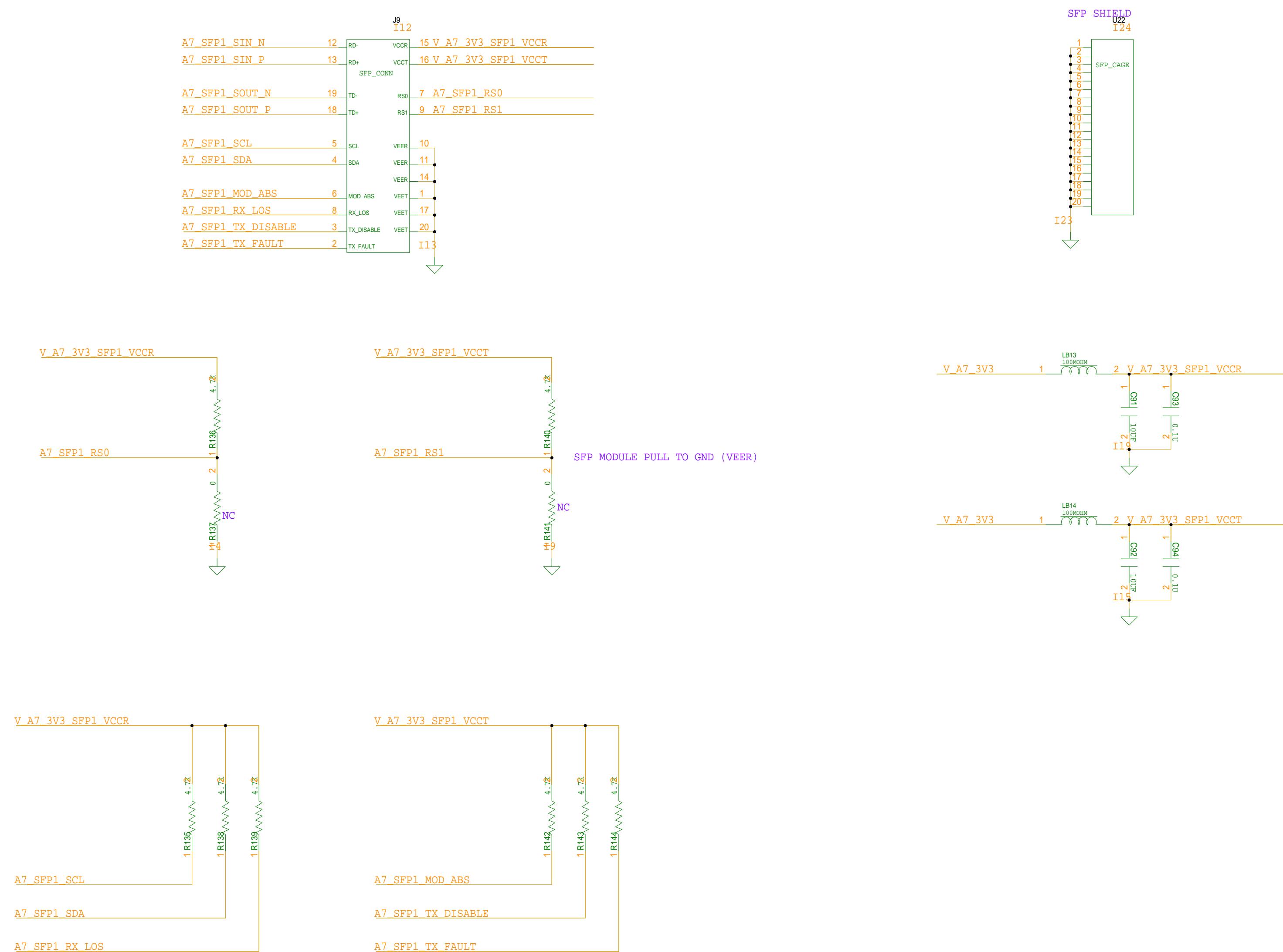
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ARTIX-7 SFP+/SFP INOUT (1)



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ARTIX-7 SFP+/SFP INOUT (2)



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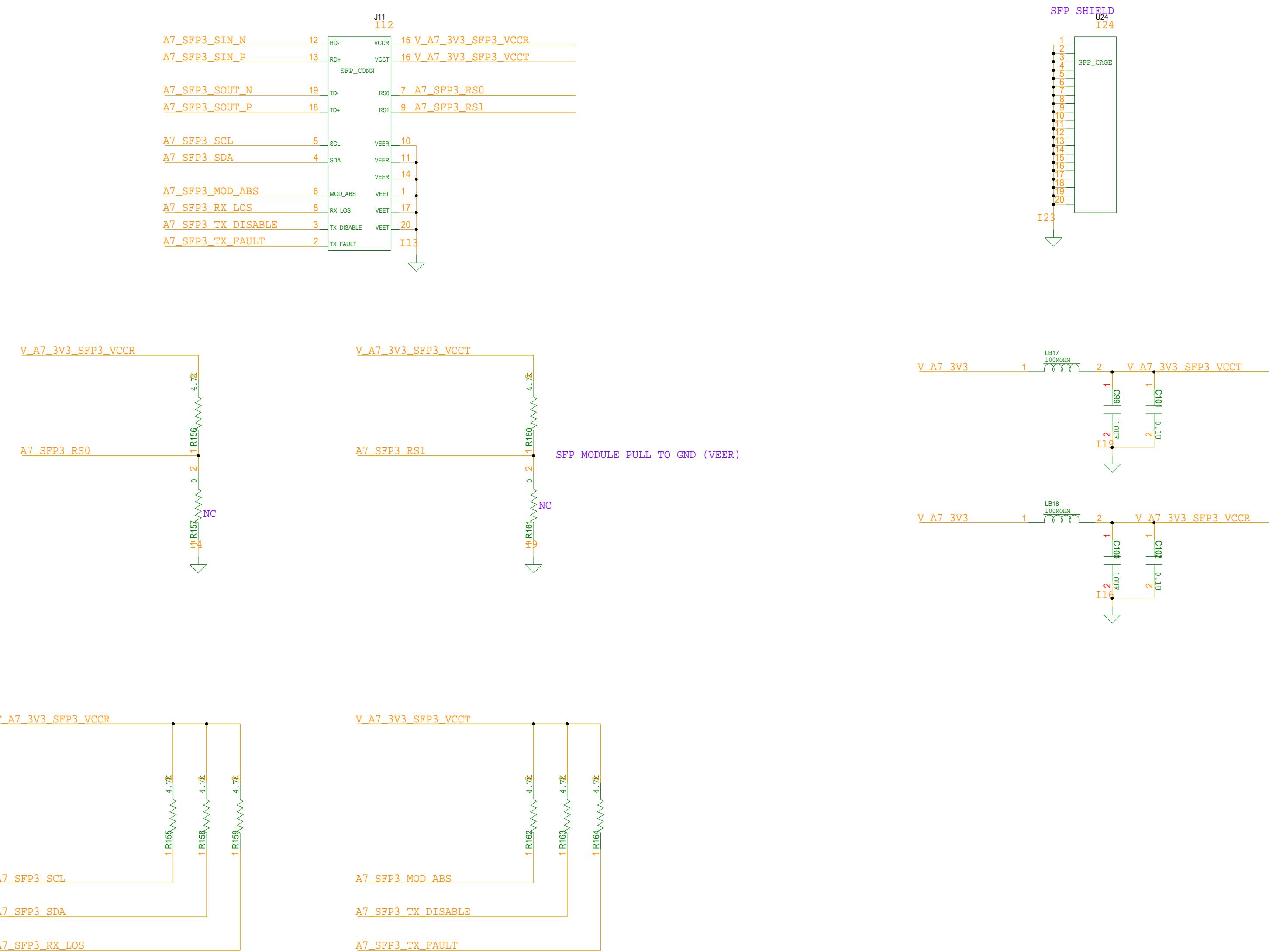
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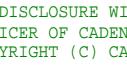
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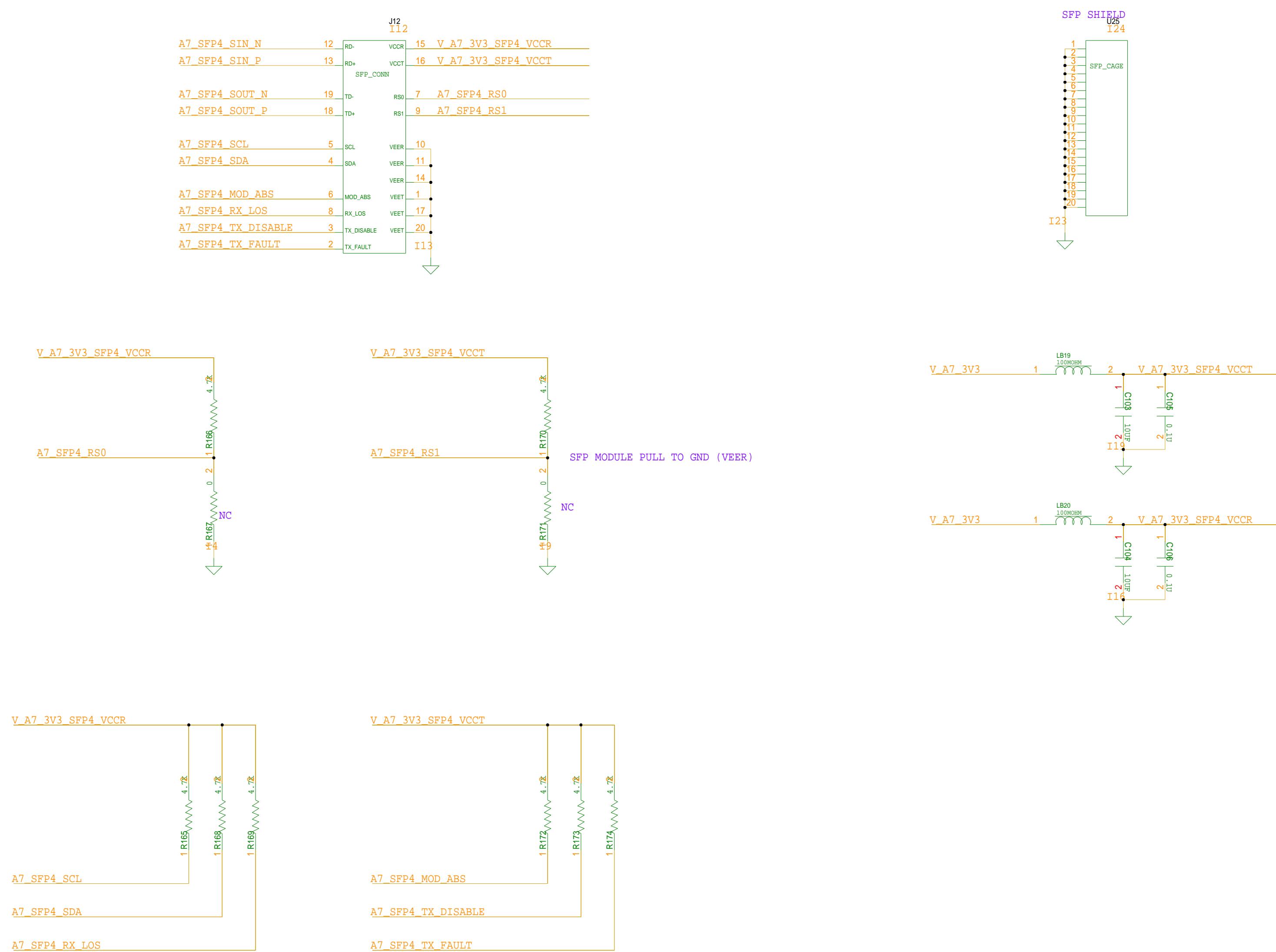


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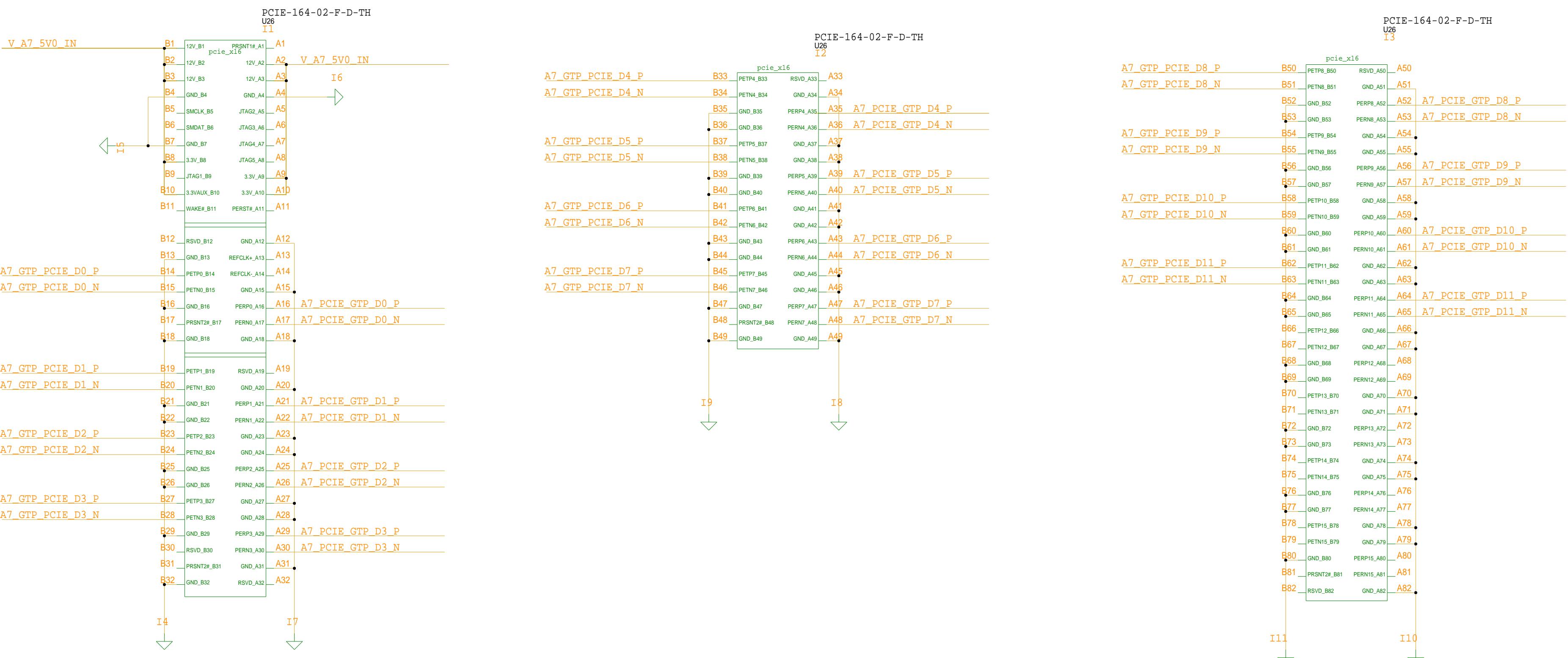
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ARTIX-7 PCIE X16 CONN

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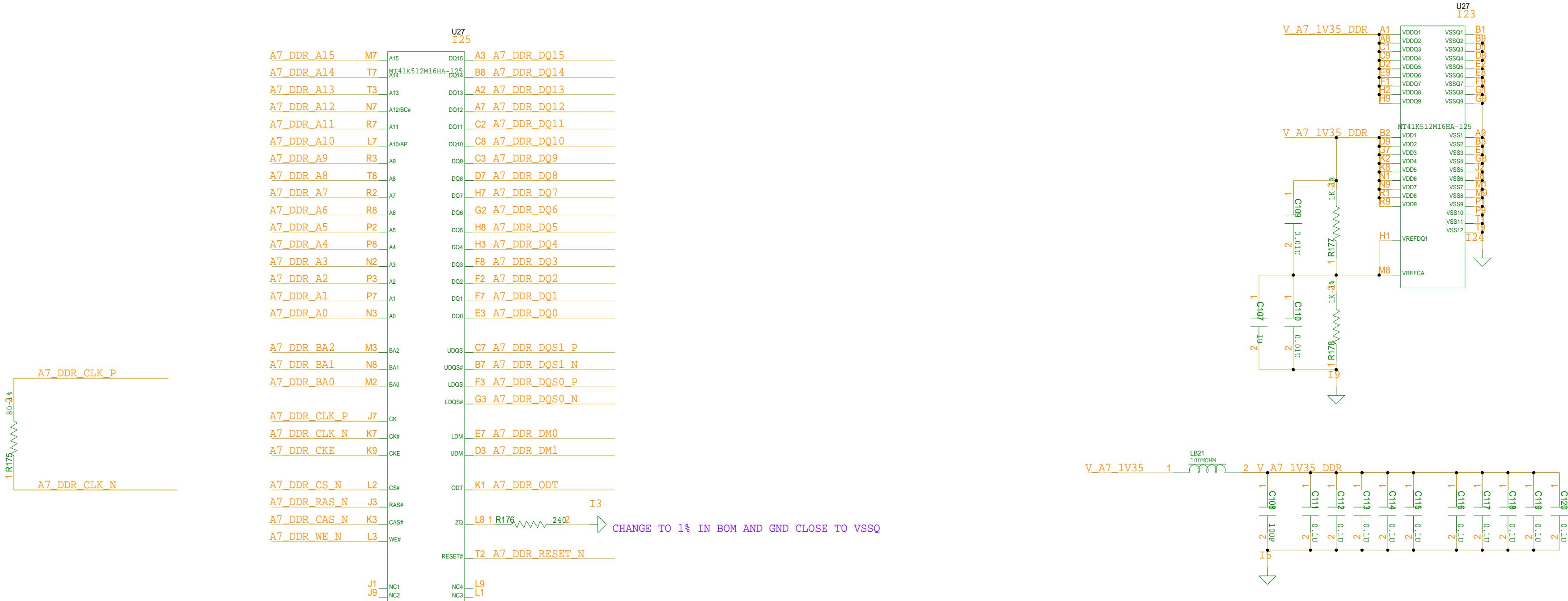
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ARTIX-7 DDR3

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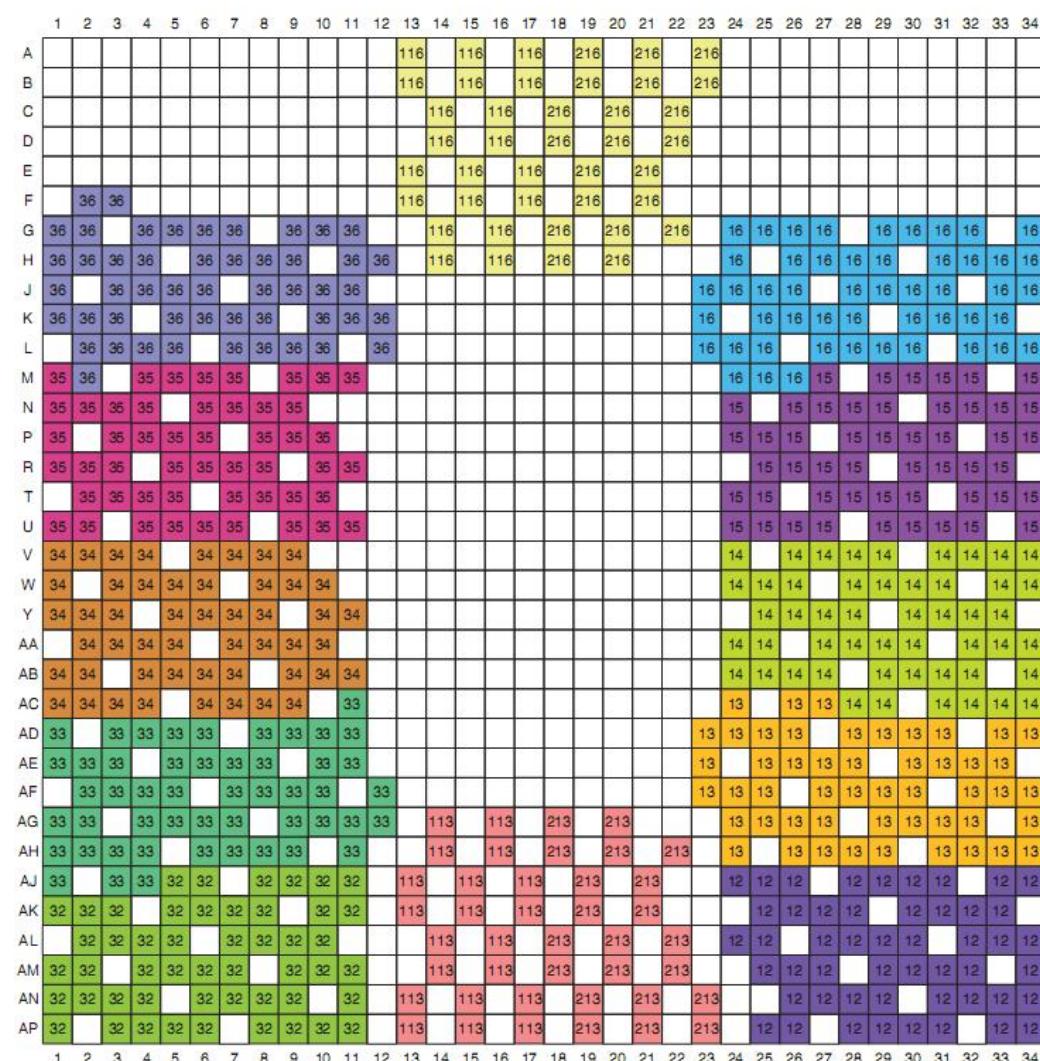
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ARTIX-7 PINOUT MAP



BANK0 : 3.3V CONFIG

BANK36 : 3.3V USB INOUT 1/2 SFP+ MUX

BANK35 : 3.3V NC

BANK34 : 1.35V DDR3

BANK33 : 3.3V USB PHY

BANK32 : 3.3V NC

BANK16 : 3.3V NC

BANK15 : 3.3V HDMI RECEIVER

BANK14 : 3.3V SPI FLASH

BANK13 : 3.3V HDMI INOUT 1/2

BANK12 : 3.3V HDMI TRANSMITTER

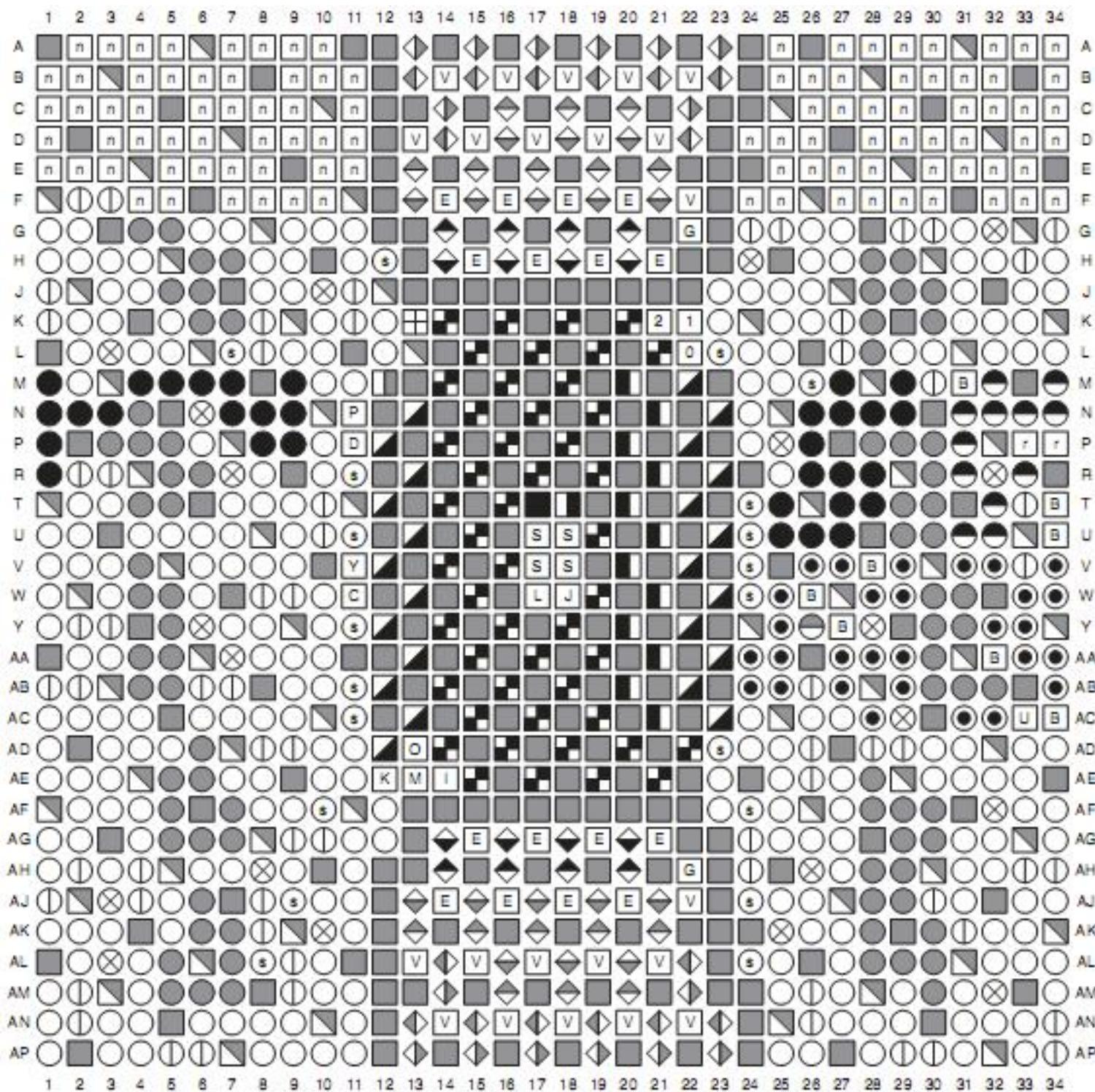
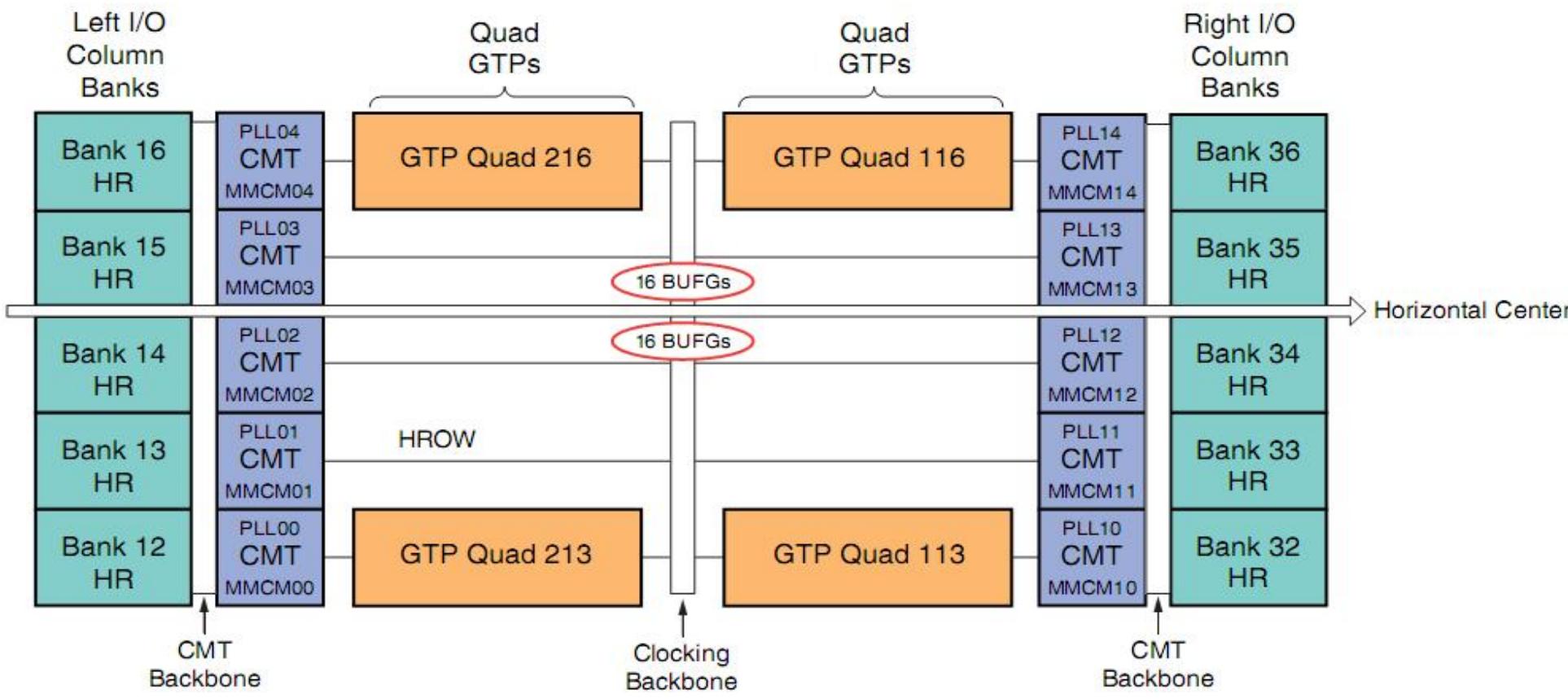
BANK116 : 3.3V PCIE X4

BANK216 : 3.3V SFP+ *4

BANK113 : 3.3V PCIE X4

BANK213 : 3.3V PCIE X4

All HR I/O banks and the GTP Quads are fully bonded out in this package.



User I/O Pins	Transceiver Pins	Dedicated Pins	Other Pins
○ IO_LXXY_# ● IO_XX_#	E MGTAVCC_G# V MGTAVTT_G# A MGTVCVCAUX_G# ◀ MGTAVTTRCAL G MGTREFREF B ADV_B B FCS_B B FOE_B B MOSI B FWE_B B DOUT_CSO_B B CSI_B B PUDC_B U RDWR_B r RSD-RS1 ● ADDP/ADON-AD15P/AD15N ● EMCCLK	C CCLK_0 V CFGBVS_0 A DONE_0 ◀ MGTAVTTRCAL J DXP_0 L DXN_0 ■ GNDADC_0 Y INIT_B_0 O M0_0 1 M1_0 2 M2_0 P PROGRAM_B_0 K TCK_0 I TDI_0 O TDO_0 M TMS_0 ■ VCCADC_0 ■ VCCBATT_0	GND VCCAUX_IO_G# VCCAUX VCCINT VCCO_# VCCBRAM NC
Multi-Function Pins			
	B PLL04 CMT MMCM04 PLL03 CMT MMCM03 PLL02 CMT MMCM02 PLL01 CMT MMCM01 PLL00 CMT MMCM00 B GTP Quad 216 B GTP Quad 116 B GTP Quad 213 B GTP Quad 113 B PLL14 CMT MMCM14 PLL13 CMT MMCM13 PLL12 CMT MMCM12 PLL11 CMT MMCM11 PLL10 CMT MMCM10 B Bank 36 HR B Bank 35 HR B Bank 34 HR B Bank 33 HR B Bank 32 HR B 16 BUFGs B 16 BUFGs B HROW B CMT Backbone B Clocking Backbone B CMT Backbone		

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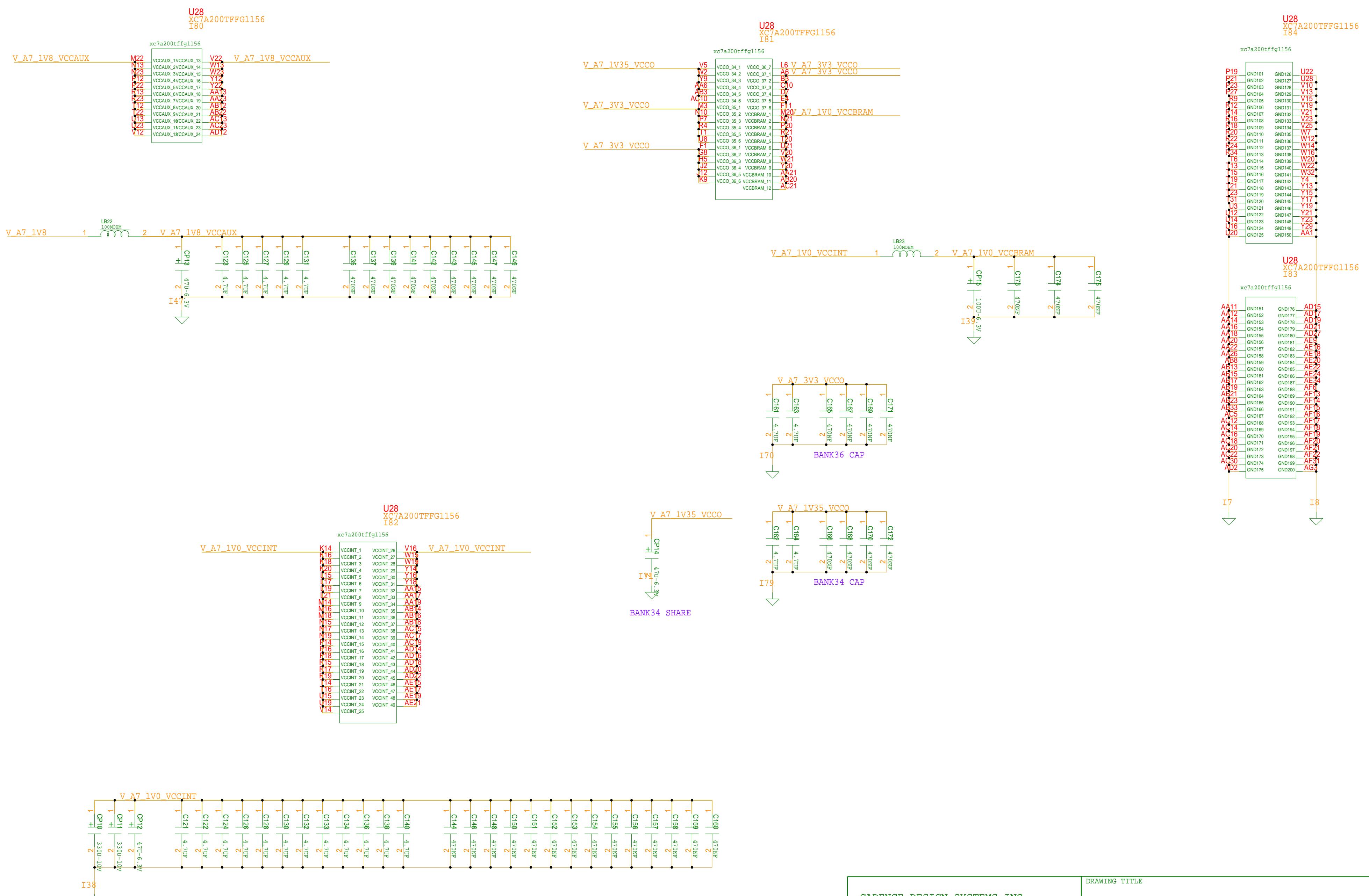
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ARTIX-7 BANK POWER (1)

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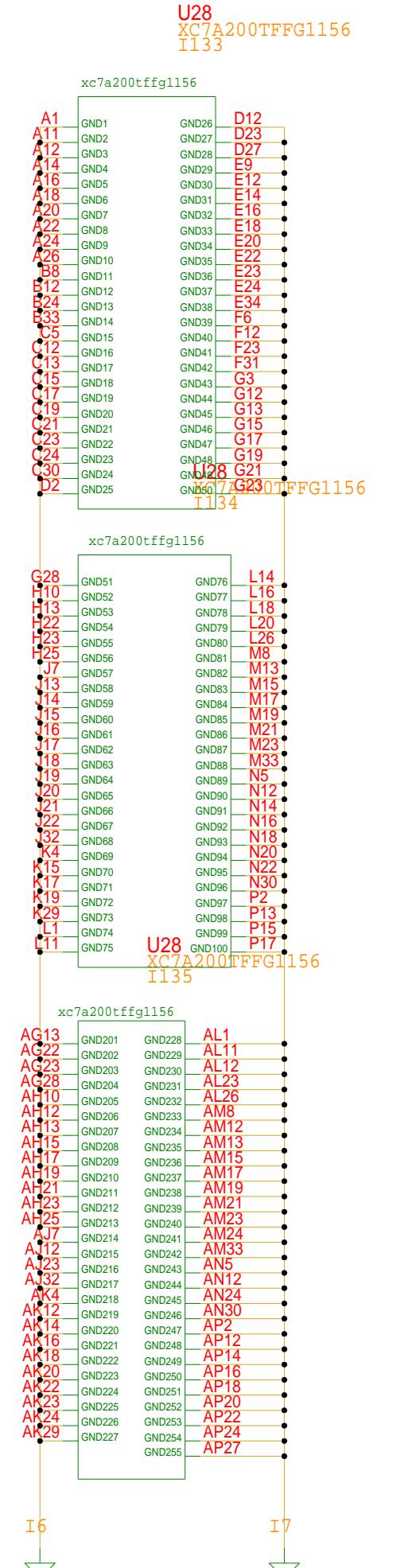
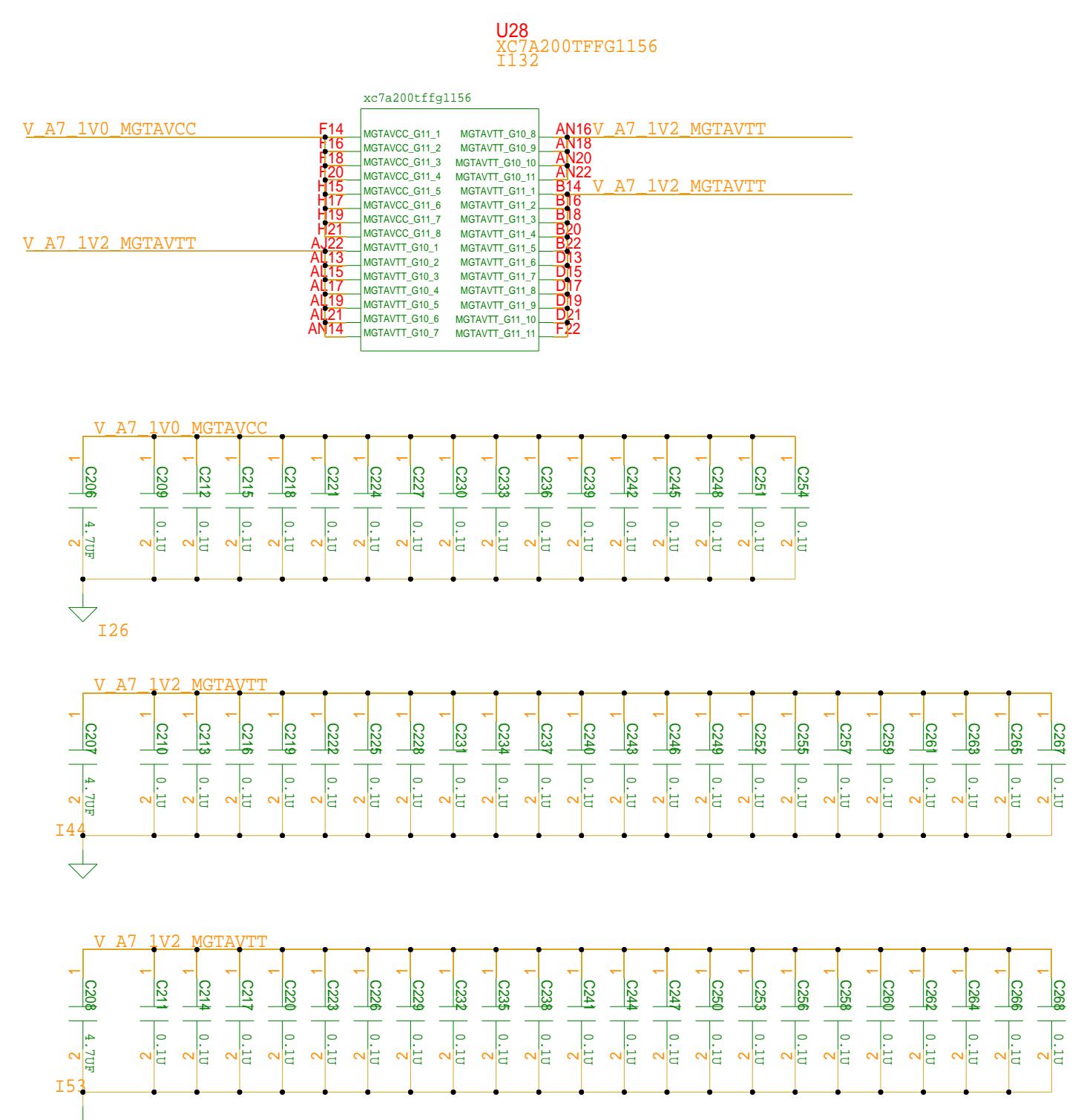
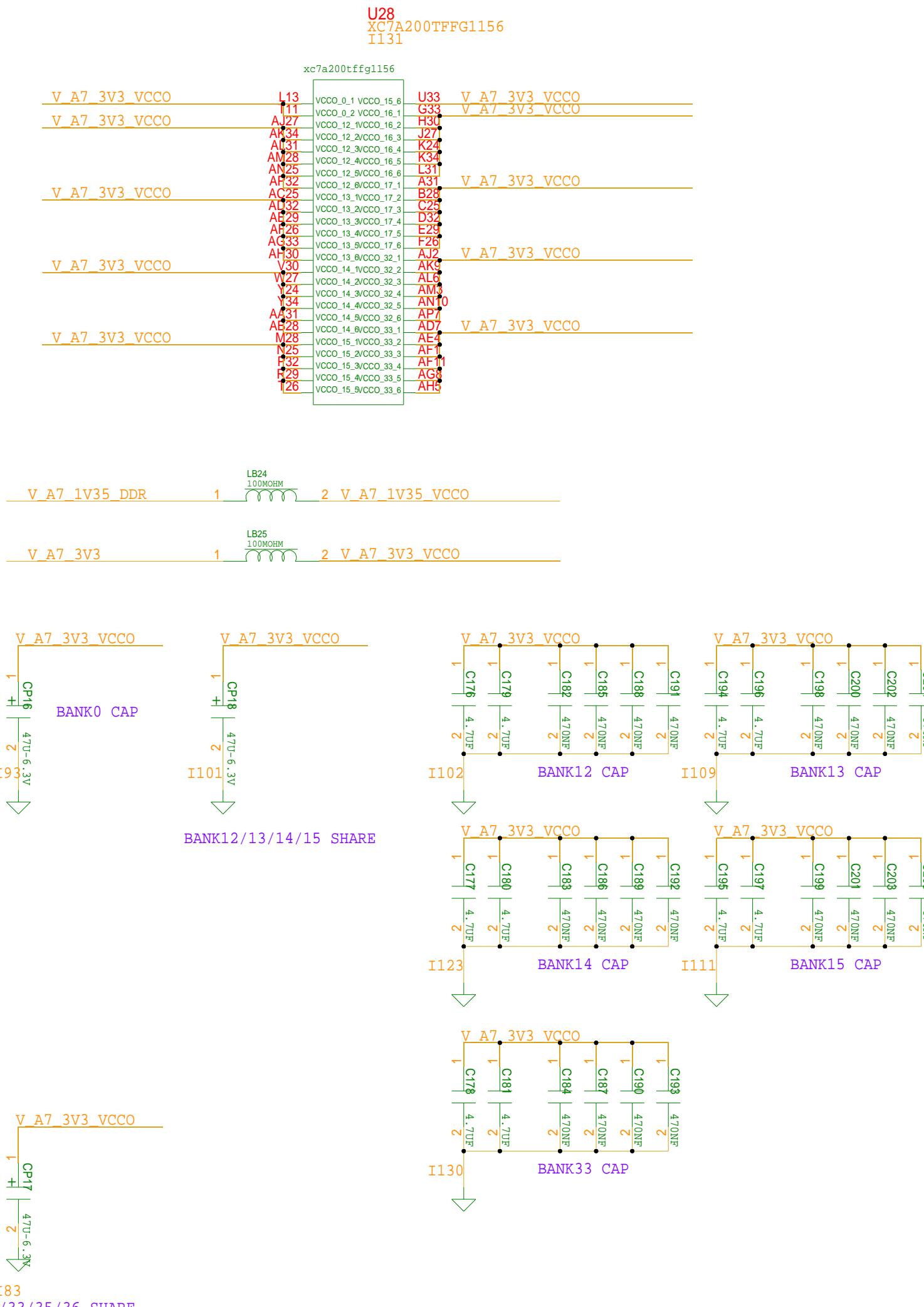
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ARTIX-7 BANK POWER (2)

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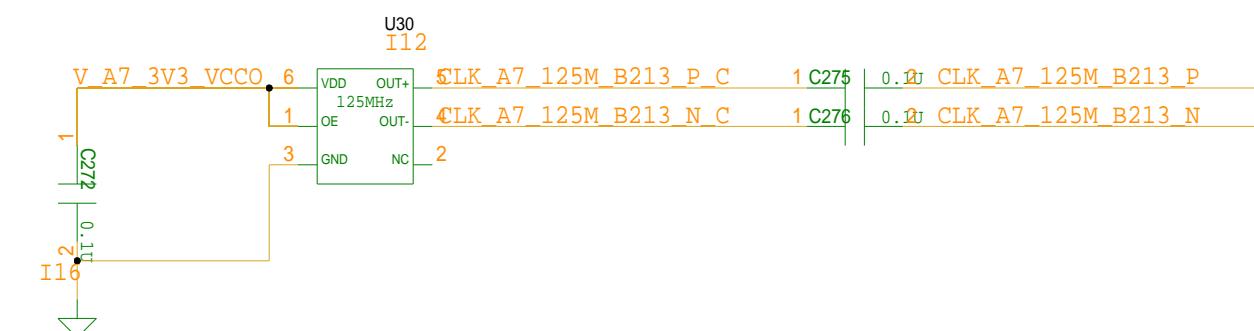
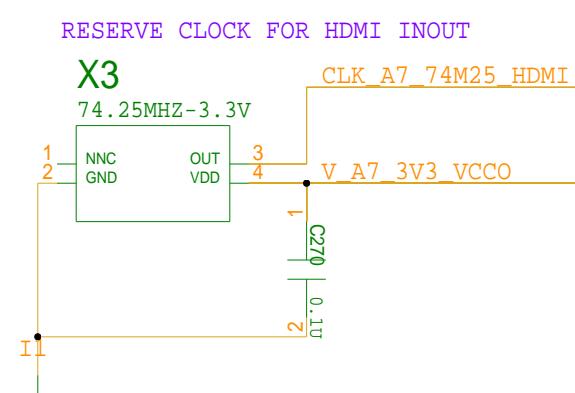
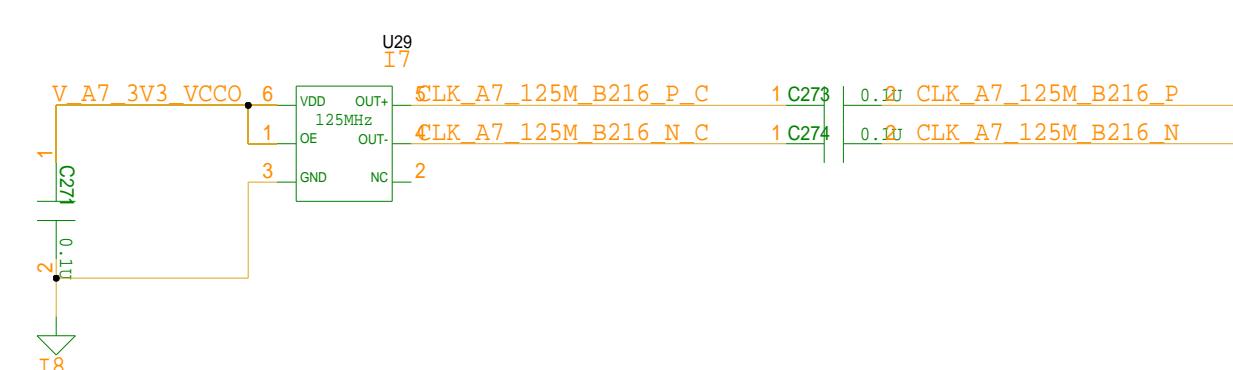
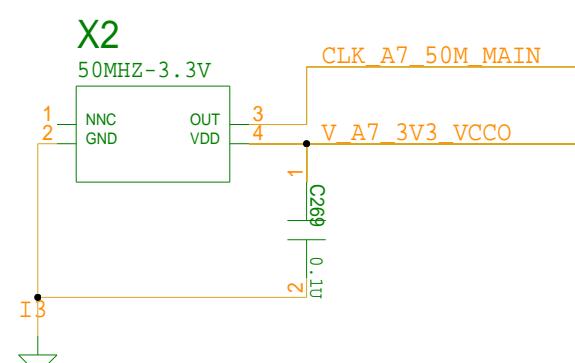
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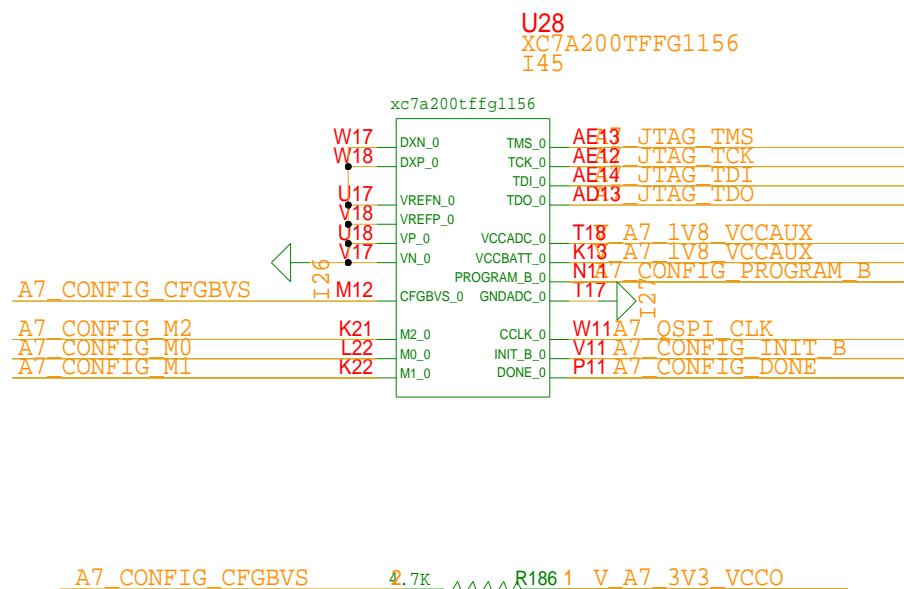
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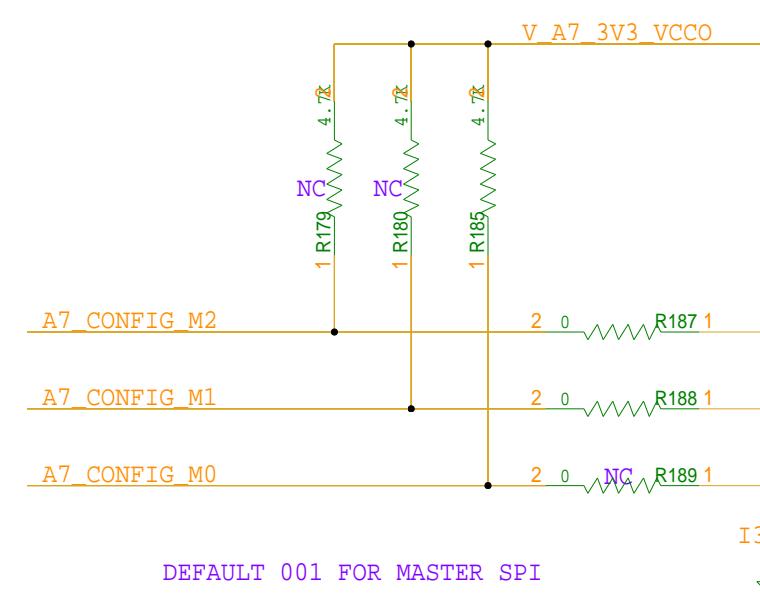
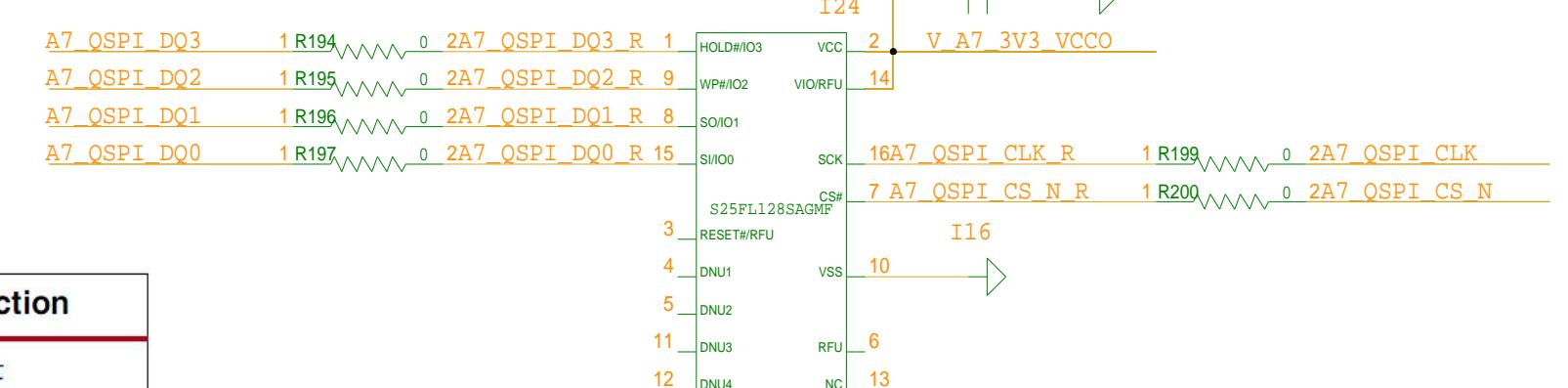
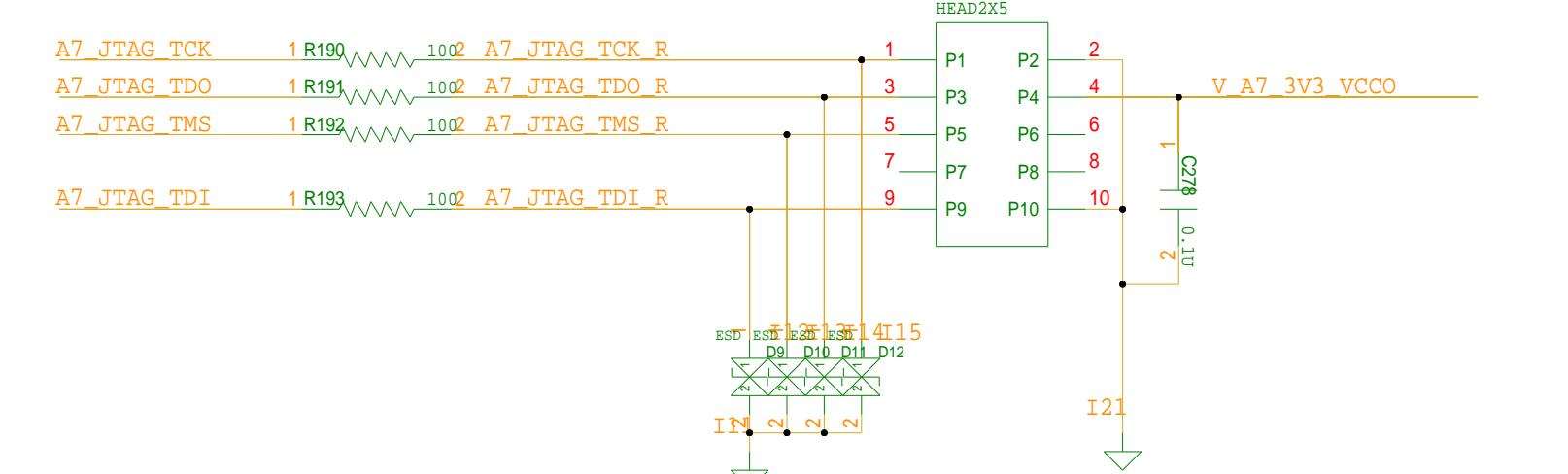
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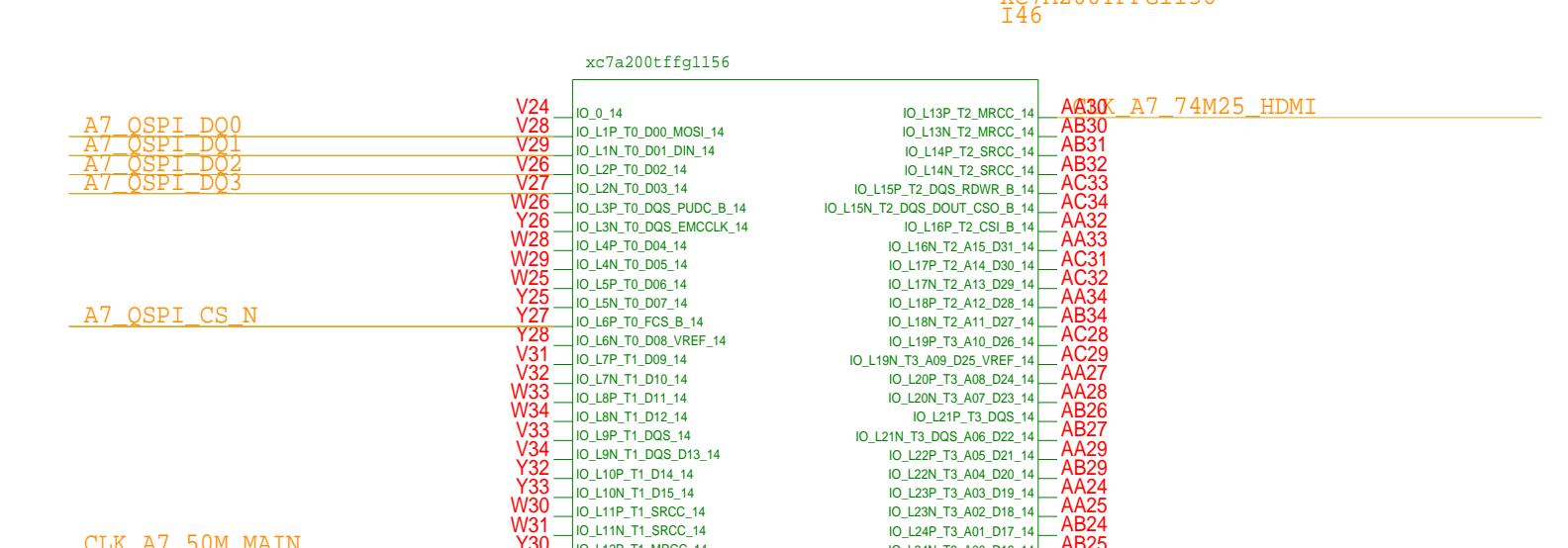
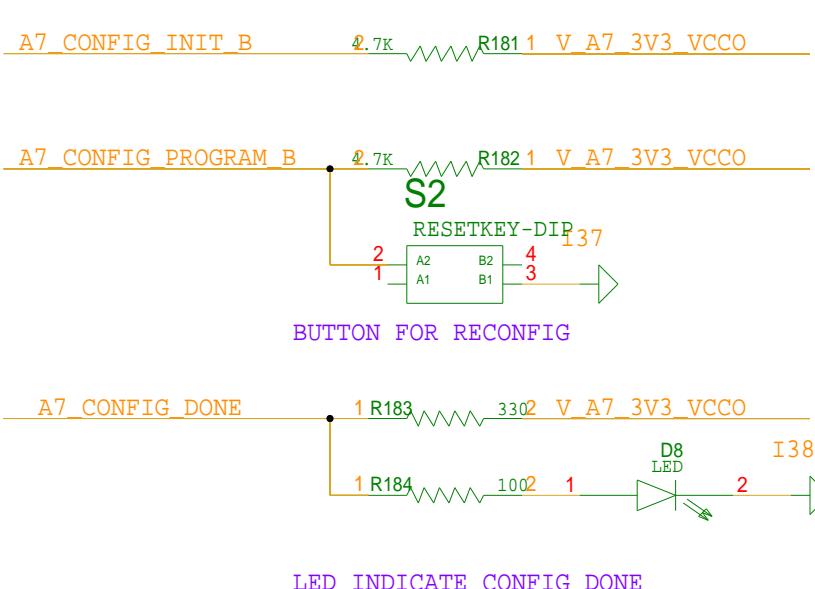
ARTIX-7 BANK0/14 CONFIG



CFGBVS Pin Connection	Supported Configuration Banks 0/14/15 V _{CCO} Supply and I/O Signal Voltages		
	Spartan-7, Artix-7, Kintex-7	Virtex-7 T, XT	Virtex-7 HT
Banks Affected	0, 14, 15	0	none
V _{CCO} _0 (3.3V or 2.5V)	3.3V or 2.5V	3.3V or 2.5V	1.8V (no CFGBVS)
GND	1.8V or 1.5V	1.8V or 1.5V	



Configuration Mode	M[2:0]	Bus Width	CCLK Direction
Master Serial	000	x1	Output
Master SPI	001	x1, x2, x4	Output
Master BPI	010	x8, x16	Output
Master SelectMAP	100	x8, x16	Output
JTAG	101	x1	Not Applicable
Slave SelectMAP	110	x8, x16, x32 ⁽¹⁾	Input
Slave Serial ⁽²⁾	111	x1	Input



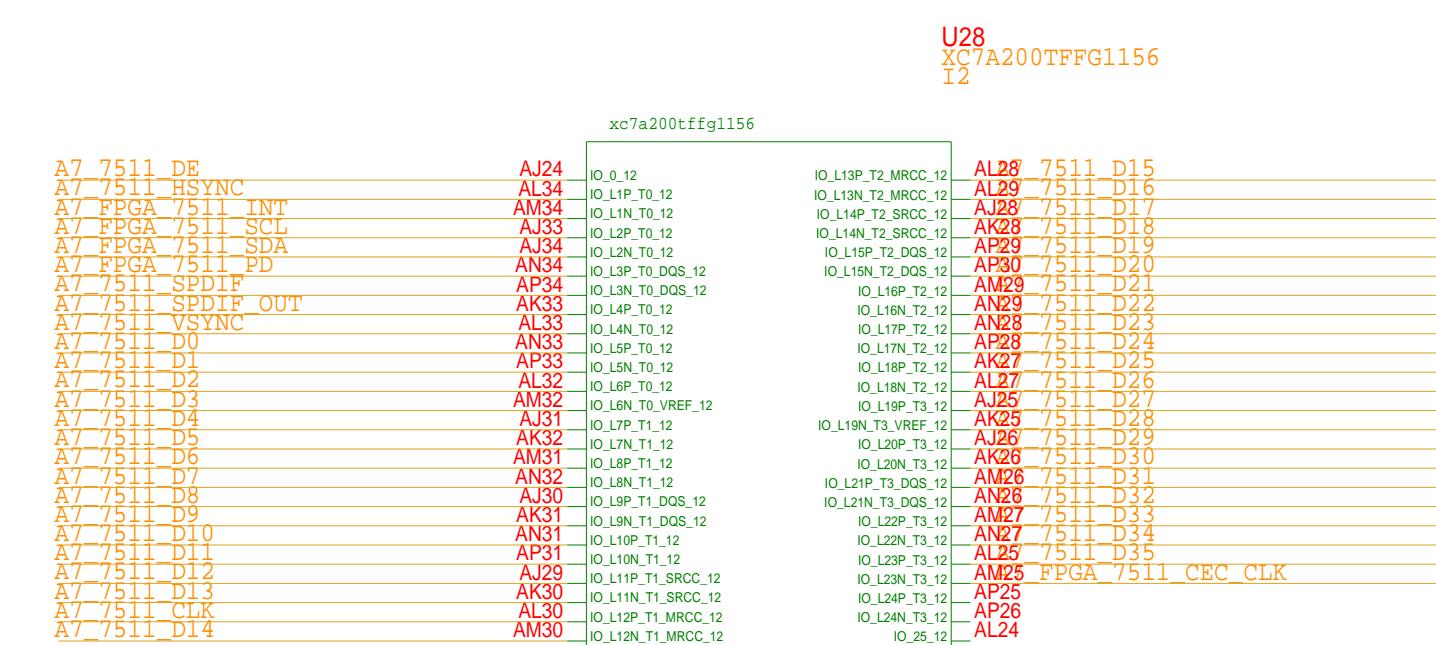
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ARTIX-7 BANK12

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OD CONFIG AS BELOW:
A7_FPGA_7511_SCL
A7_FPGA_7511_SDA

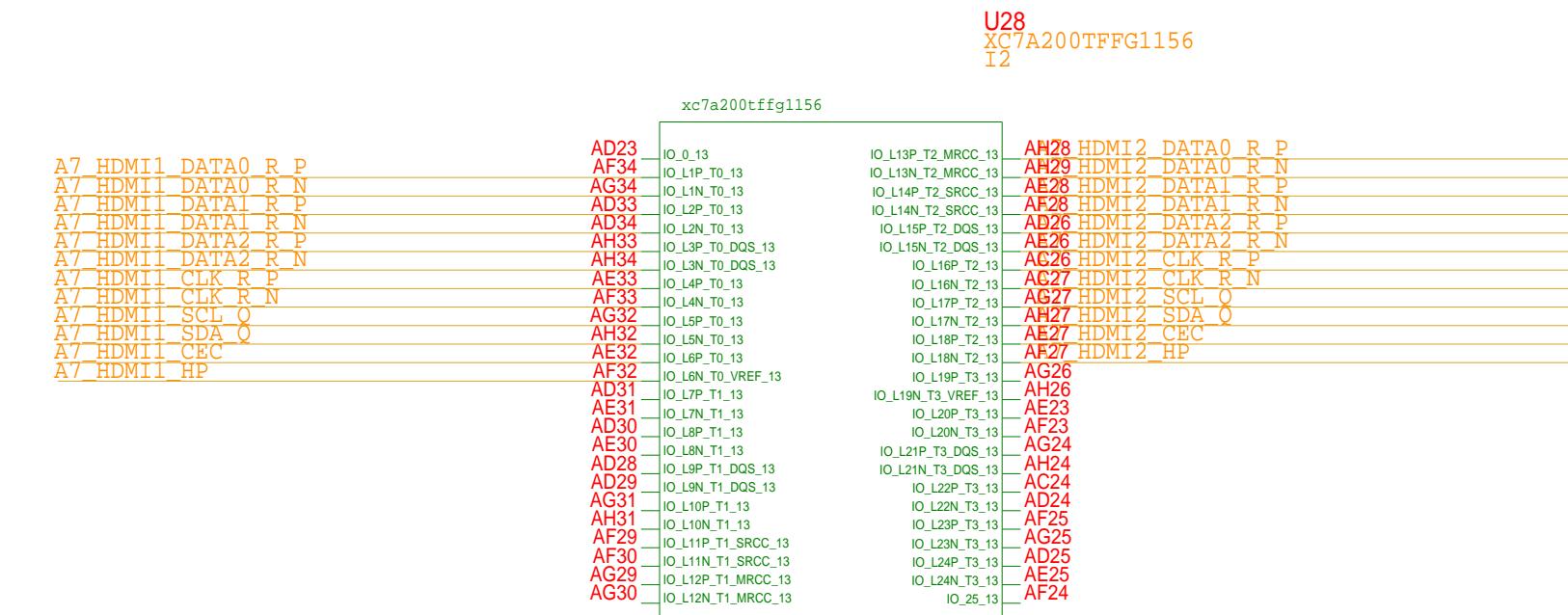
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ARTIX-7 BANK13

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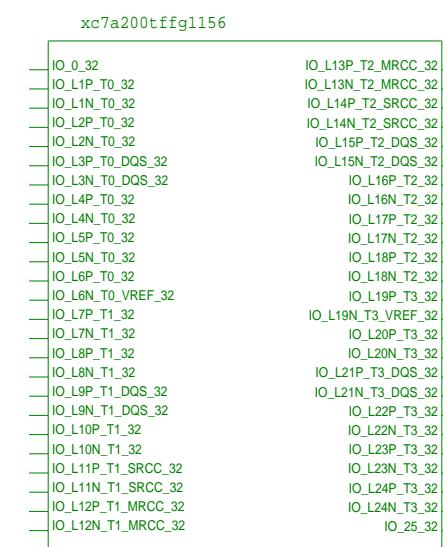


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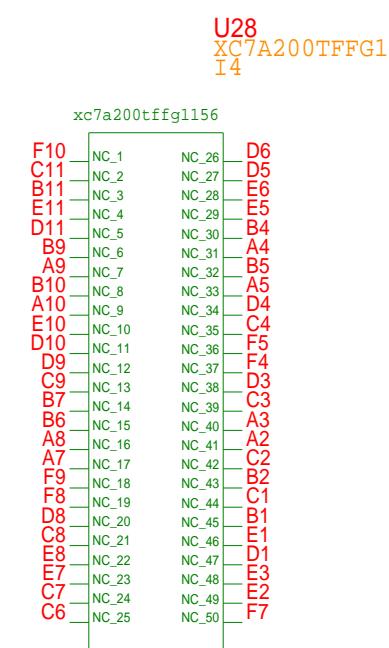
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ARTIX-7 BANK NC

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ARTIX-7 BANK16

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L23	IO_0_16	J29
M24	IO_L1P_T0_16	H29
L24	IO_L1N_T0_16	K30
K23	IO_L2P_T0_16	J30
J23	IO_L2N_T0_16	G29
G24	IO_L3P_T0_DQS_16	J30
G25	IO_L3N_T0_DQS_16	K31
K25	IO_L4P_T0_16	J31
J25	IO_L4N_T0_16	H31
M25	IO_L5P_T0_16	G31
L25	IO_L5N_T0_16	L29
J24	IO_L6P_T0_16	L30
H24	IO_L6N_TO_VREF_16	H32
H27	IO_L7P_T1_16	G32
G27	IO_L7N_T1_16	K33
H26	IO_L8P_T1_16	J34
G26	IO_L8N_T1_16	H33
L27	IO_L9P_T1_DQS_16	G34
K27	IO_L9N_T1_DQS_16	L32
K26	IO_L10P_T1_16	G32
J26	IO_L10N_T1_16	J33
L28	IO_L11P_T1_SRCC_16	H34
K28	IO_L11N_T1_SRCC_16	I33
J28	IO_L12P_T1_MRCC_16	L34
H28	IO_L12N_T1_MRCC_16	I26
	IO_25_16	M26

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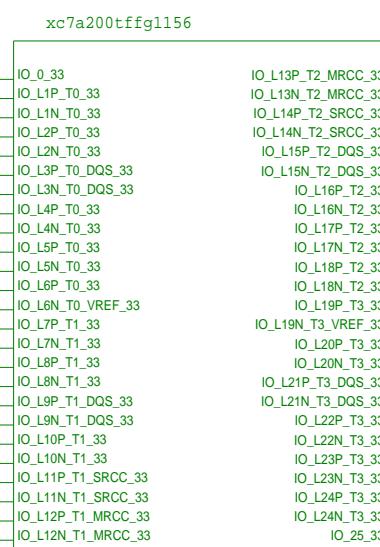
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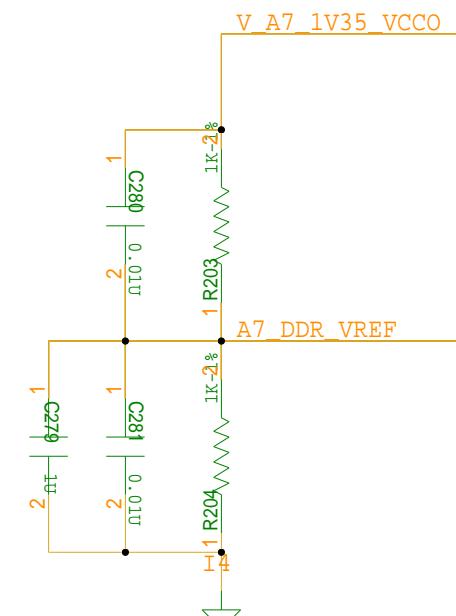
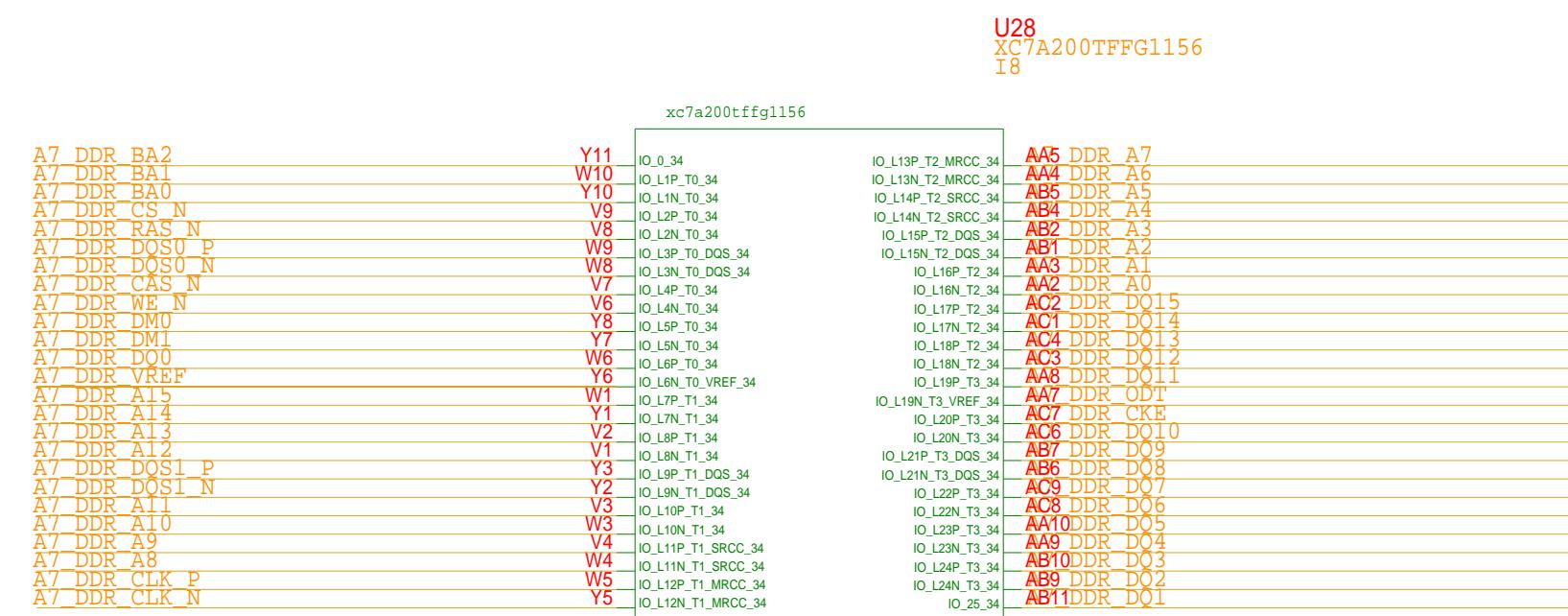


A7_USBPHY_CLK

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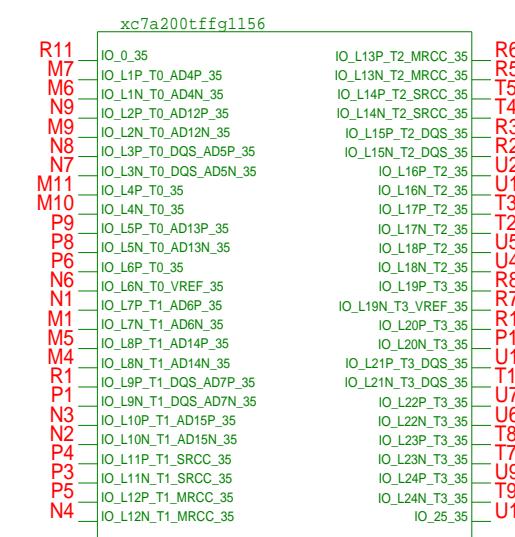
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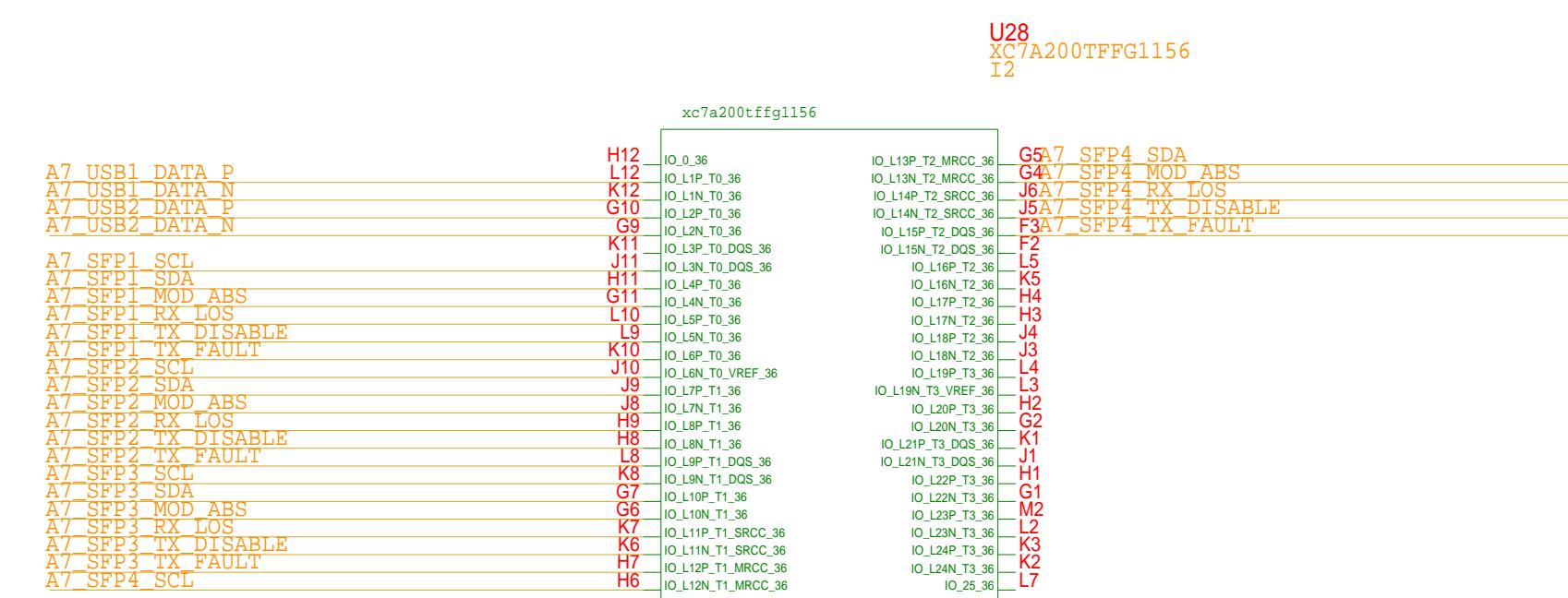


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ARTIX-7 BANK36

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ARTIX-7 GTP (1)

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A7_PCIE_GTP_D0_P	AP13	MGTPTXP2_113	A167	PCIE_GTP_D5_N	
A7_PCIE_GTP_D0_N	AK13	MGTPTXN2_113	C167	PCIE_GTP_D5_N	
A7_PCIE_GTP_D0_N	AL13	MGTPTXN2_113	H16		
A7_GTP_PCIE_D1_P	AM14	MGTPTXP2_113	G14		
A7_PCIE_GTP_D1_P	AK15	MGTPTXP2_113	H14		
A7_GTP_PCIE_D1_N	AG14	MGTREFCLK0P_113	D147	PCIE_GTP_D6_P	
A7_PCIE_GTP_D1_N	AH14	MGTREFCLK0N_113	F167	PCIE_GTP_D6_N	
A7_GTP_PCIE_D2_P	AM16	MGTREFCLK0N_113	C147	PCIE_GTP_D6_N	
A7_PCIE_GTP_D2_P	AK16	MGTPTXP1_113	E167	PCIE_GTP_D6_N	
A7_GTP_PCIE_D2_N	AP15	MGTPTXN1_113	B167	PCIE_GTP_D7_P	
A7_PCIE_GTP_D2_N	AM16	MGTPTXN1_113	F187	PCIE_GTP_D7_P	
A7_GTP_PCIE_D3_P	AN17	MGTPTXP0_113	A167	PCIE_GTP_D7_N	
A7_PCIE_GTP_D3_P	AJ17	MGTPTXP0_113	E187	PCIE_GTP_D7_N	
A7_GTP_PCIE_D3_N	AP17	MGTPTXN0_113	B187	PCIE_GTP_D8_P	
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A7_GTP_PCIE_D4_P	B17	MGTPTXP1_113	F23	PCIE_GTP_D8_P	
A7_PCIE_GTP_D4_P	F17	MGTPTXP2_113	A23	PCIE_GTP_D8_N	
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A7_PCIE_GTP_D4_N	E17	MGTPTXN2_116	MGTREFCLK0N_213	AH20K	A7_I25M_B2I3_P
A7_GTP_PCIE_D5_P	B15	MGTPTXN2_116	MGTREFCLK0P_213	AG20K	A7_I25M_B2I3_N

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ARTIX-7 GTP (2)

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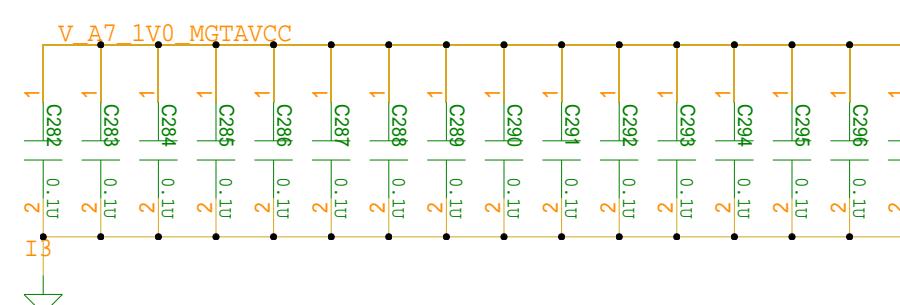
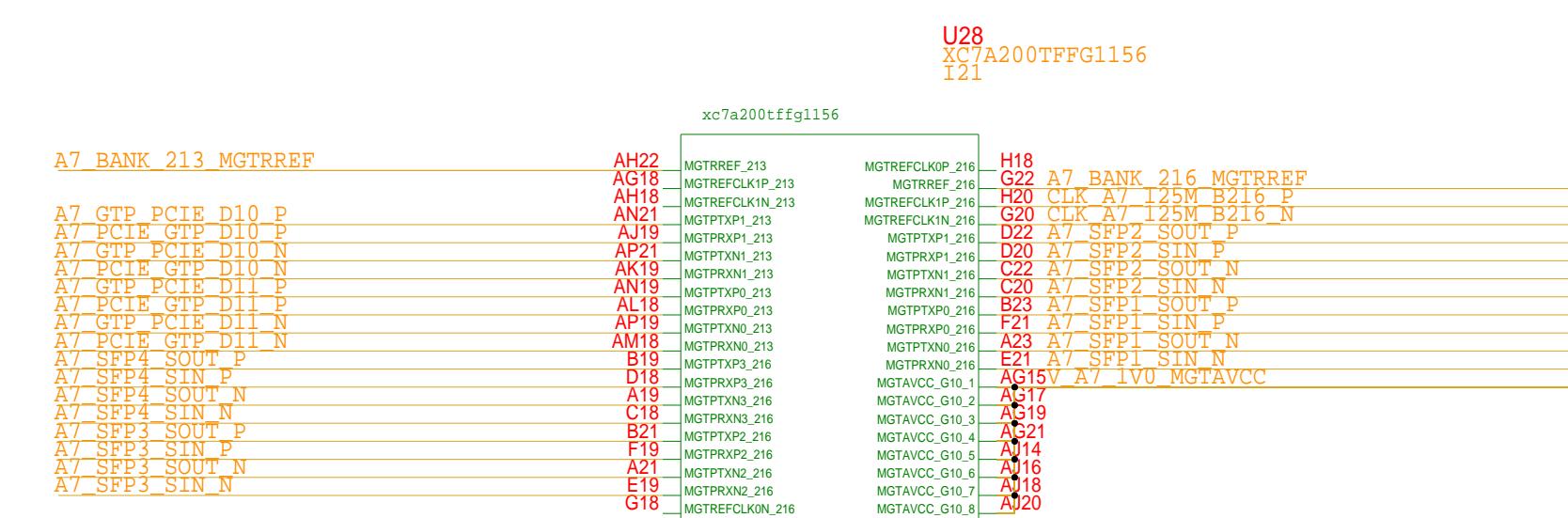
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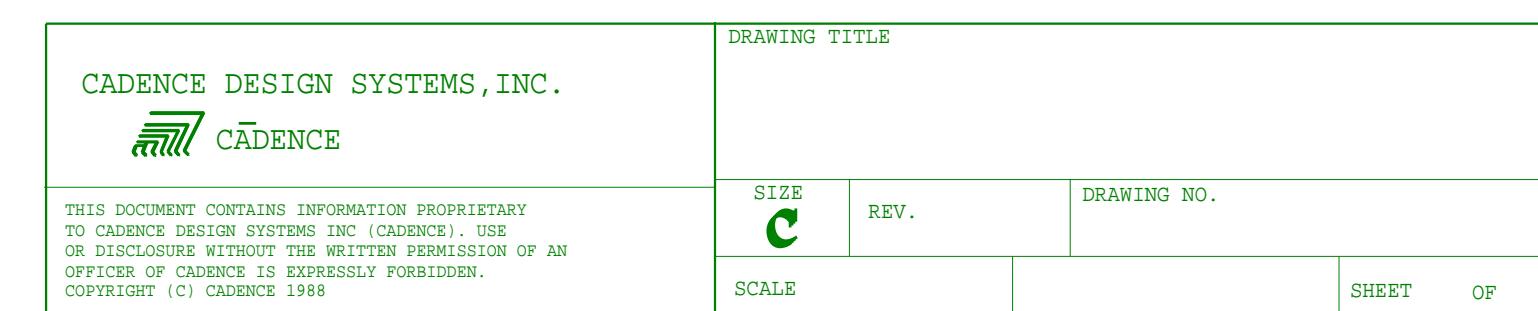
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A7 BANK 216 MGTRREF 1 R205 ~~~~~ 1002 V A7 1V2 MGTAVTT

A7 BANK 213 MGTRREF 1 R206 ^ ^ ^ 1002 V A7 1V2 MGTAVTT



ZYNQ-7 INDEX

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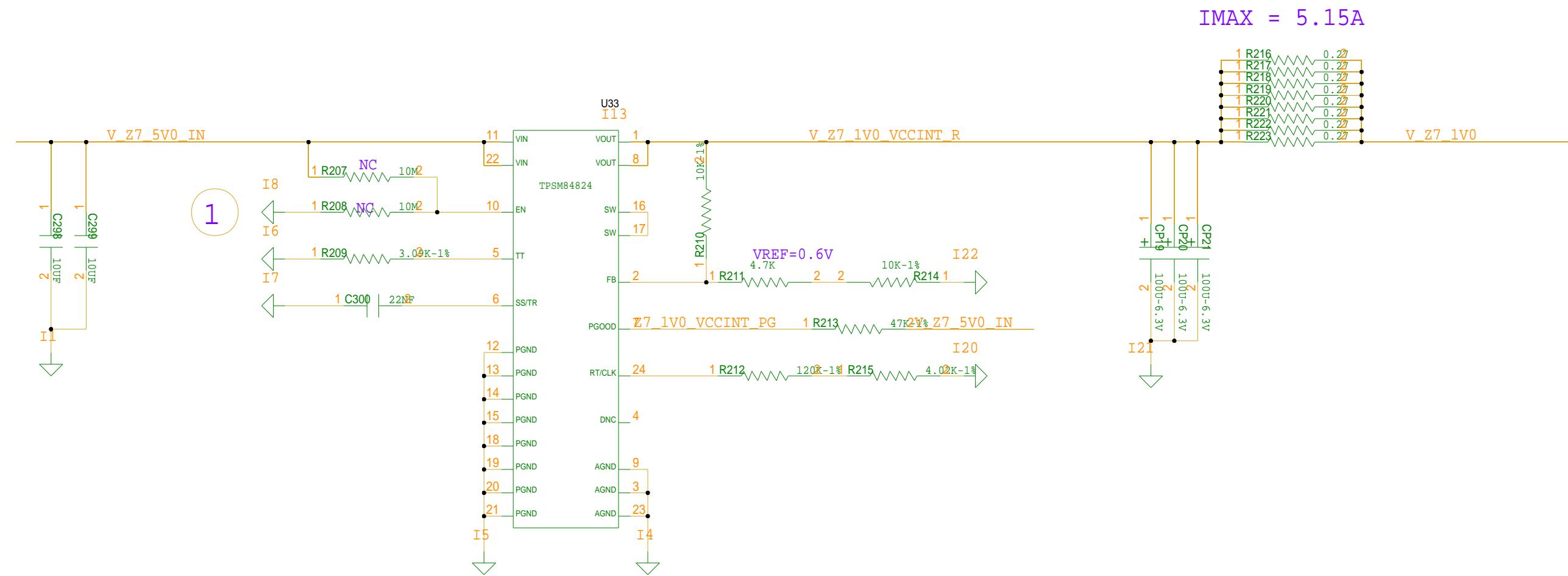
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ZYNQ-7 POWER (1)



SS/TR	6	I	Soft-start and tracking pin. Connecting an external capacitor to this pin adjusts the output voltage soft-start ramp slower than its 1.2 ms default setting. A voltage applied to this pin allows for tracking and sequencing control.
-------	---	---	--

Table 9. Soft-Start Capacitor Values and Soft-Start Time

C _{ss} (nF)	open	10	15	22	47
SS Time (ms)	1.2	2.4	3	3.8	6.8

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ZYNQ-7 POWER (2)

$$V_{OUT} = V_{REF} \times (1 + (R_{TOP}/R_{BOT}))$$

$$R_{RT} (\text{k}\Omega) = [14,822/f_{SW} (\text{kHz})]^{1.081}$$

$$V_{IN_STARTUP} = (0.8 \text{ nA} + (0.8 \text{ V}/R_{BOT_EN})) \times \left(R_{TOP_EN} + \frac{R_{BOT_EN} \times 1 \text{ M}\Omega}{R_{BOT_EN} + 1 \text{ M}\Omega} \right)$$

where:

R_{TOP_EN} is the resistor from V_{IN} to EN

R_{BOT_EN} is the resistor from EN to ground.

Table 9. Soft Start Time Set by the SS12 and SS34 Pins

R _{TOP} (kΩ)	R _{BOT} (kΩ)	Soft Start Time			
		Channel 1	Channel 2	Channel 3	Channel 4
0	N/A ¹	2 ms	2 ms	2 ms	2 ms
100	600	2 ms	Parallel	2 ms	4 ms
200	500	2 ms	8 ms	2 ms	8 ms
300	400	4 ms	2 ms	4 ms	2 ms
400	300	4 ms	4 ms	4 ms	4 ms
500	200	8 ms	2 ms	4 ms	8 ms
600	100	8 ms	Parallel	8 ms	2 ms
N/A ¹	0	8 ms	8 ms	8 ms	8 ms

Table 16. Factory Default Options

Option	Default Value
Channel 1 Output Voltage	0.8 V adjustable output
Channel 2 Output Voltage	0.8 V adjustable output
Channel 3 Output Voltage	0.8 V adjustable output
Channel 4 Output Voltage	0.8 V adjustable output
PWRGD Pin (Pin 20) Output	Monitor Channel 1 output
Output Discharge Function	Enabled for all four buck regulators
Switching Frequency on Channel 1	1 x switching frequency set by the RT pin
Switching Frequency on Channel 3	1 x switching frequency set by the RT pin
SYNC/MODE Pin (Pin 43) Function	Forced PWM/automatic PWM/PSM mode setting with the ability to synchronize to an external clock
Hiccup Protection	Enabled for overcurrent events
Short-Circuit Latch-Off Function	Disabled for output short-circuit events
Oversupply Latch-Off Function	Disabled for output oversupply events
Reset Timeout Period	200 ms
Watchdog Timeout Period	1.6 sec
Manual Reset Input Mode	Processor manual reset mode



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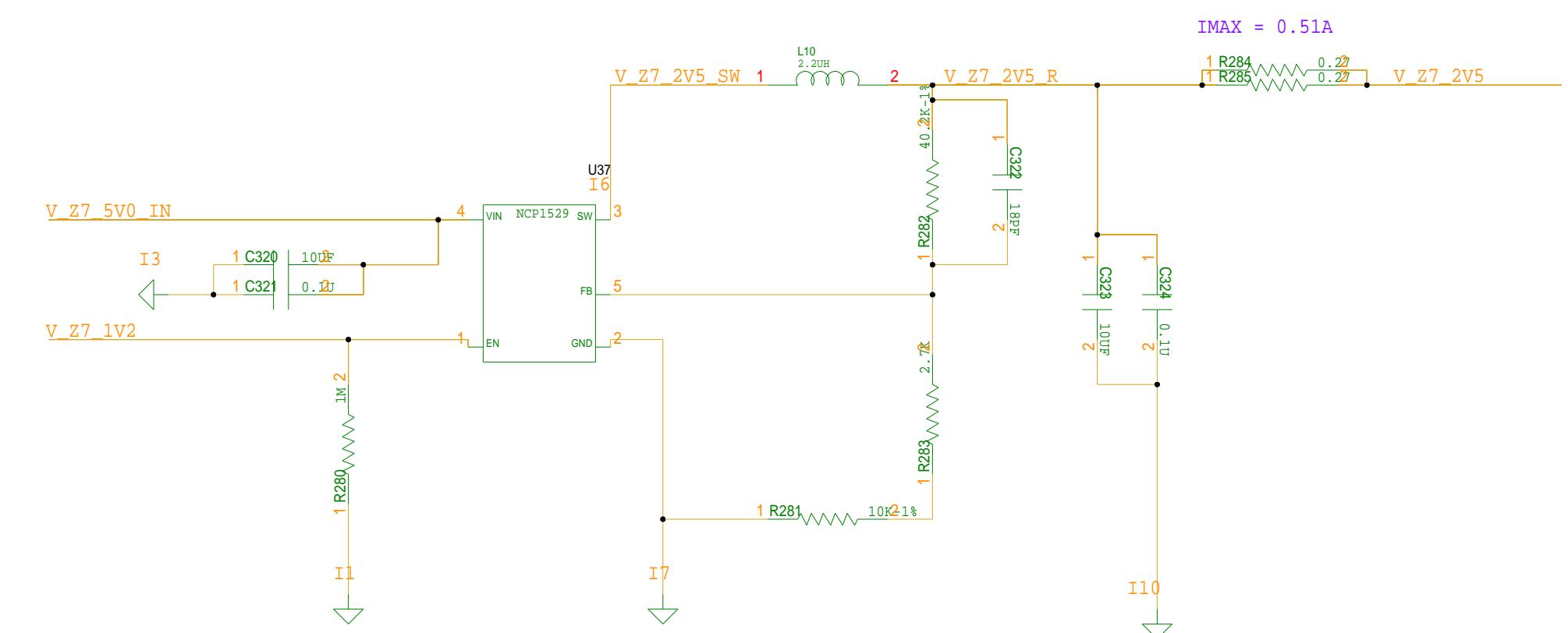
QUESTION

ZYNQ-7 POWER (3)

REVISIONS		
ZONE	LTR	DESCRIPTION
		DATE APPR.

- $V_{out} = V_{FB} \times (1 + R1/R2)$
- V_{OUT} : Output Voltage (V)
 - V_{FB} : Feedback Voltage = 0.6 V
 - $R1$: Feedback Resistor from V_{OUT} to FB
 - $R2$: Feedback Resistor from FB to GND

3



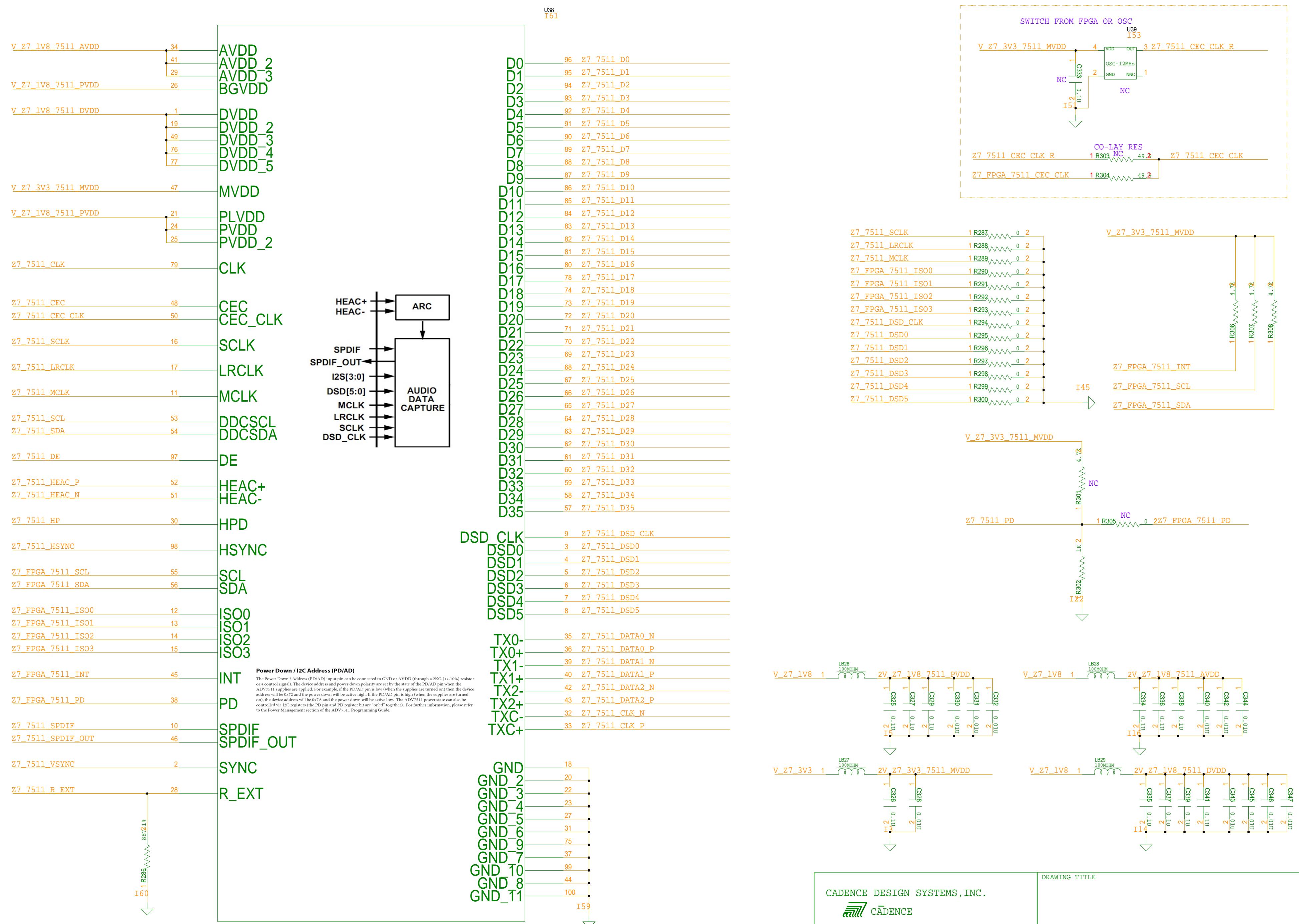
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ZYNQ-7 PL HDMI TRANSMITTER (1)

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ZYNQ-7 PL HDMI TRANSMITTER (2)

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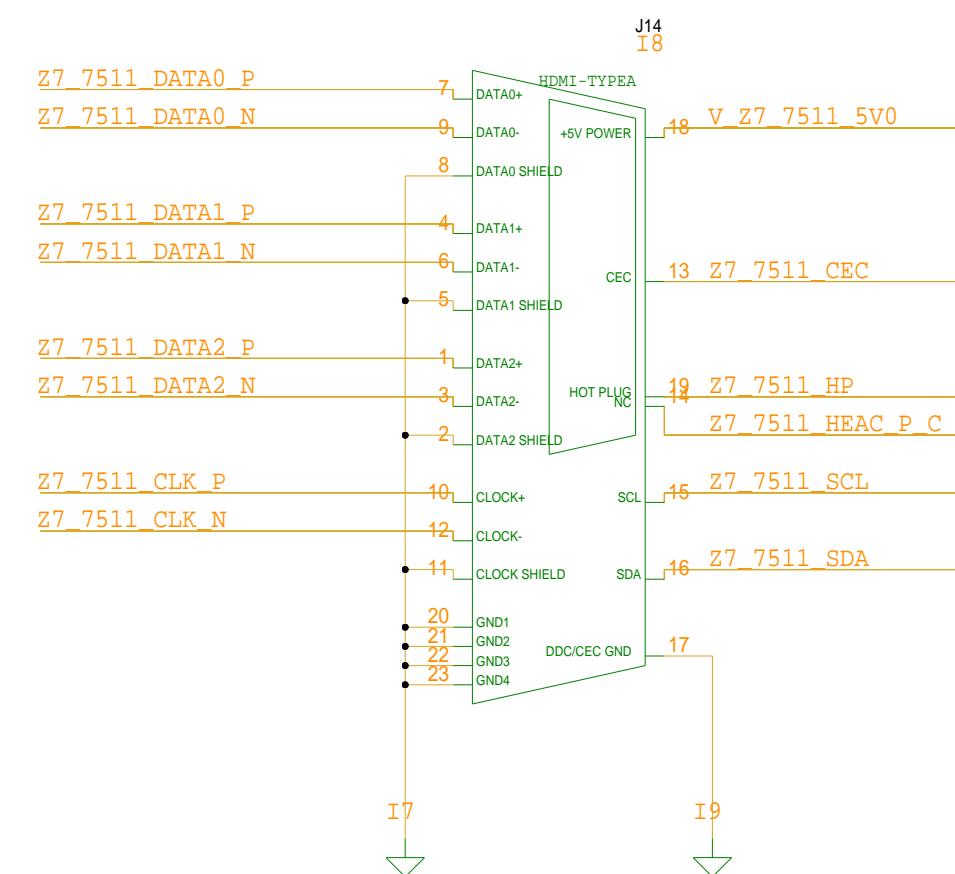
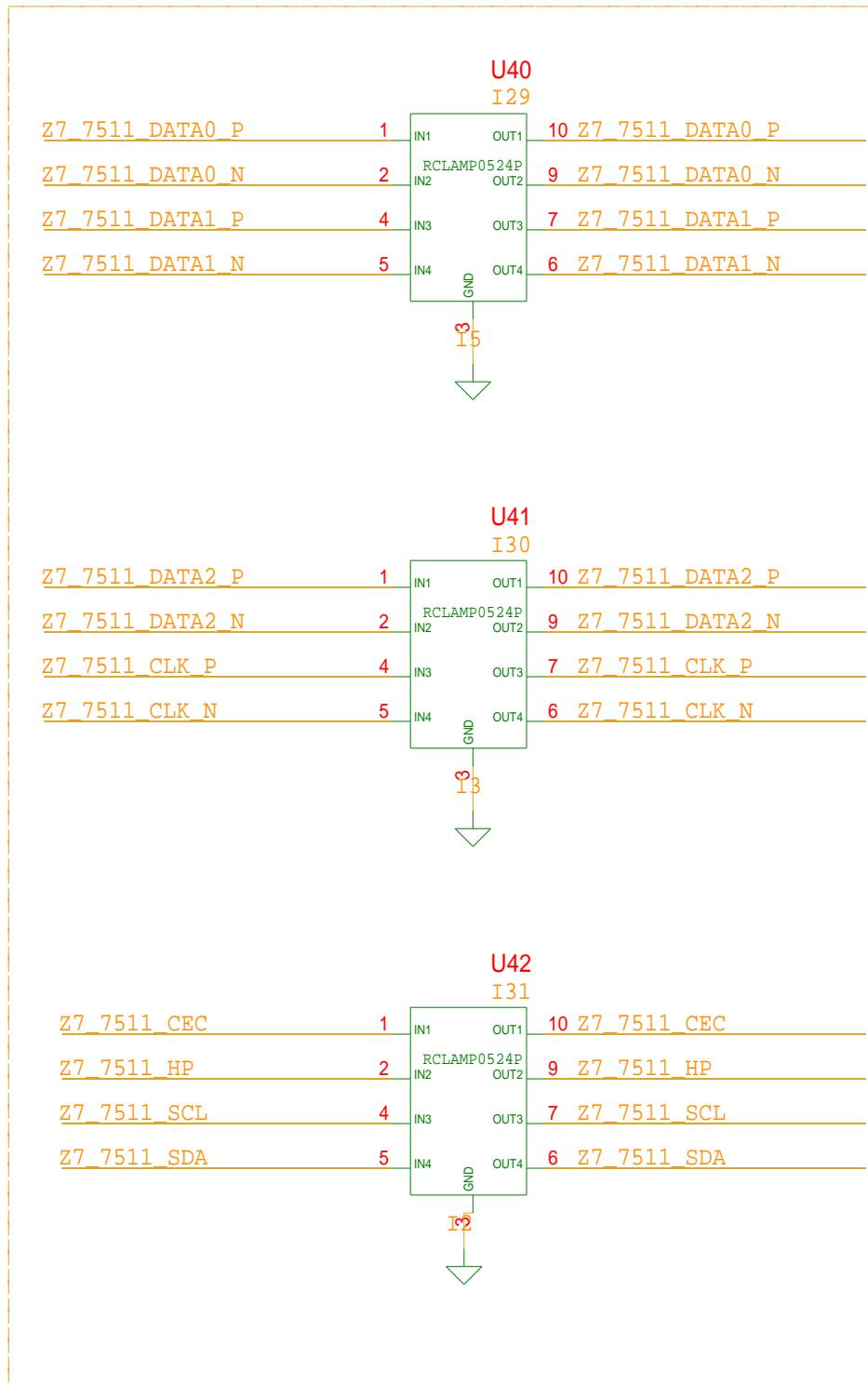
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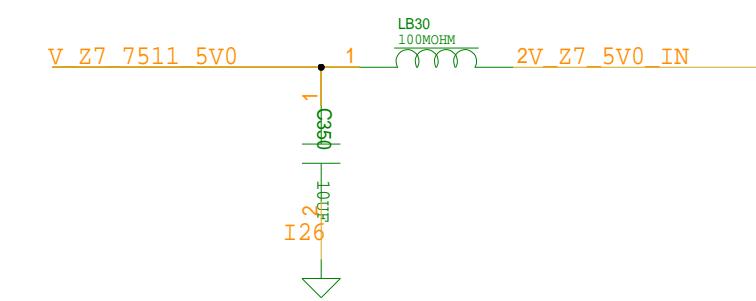
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DATE APPR.

CHANGE CONNECTION DUE TO LAYOUT

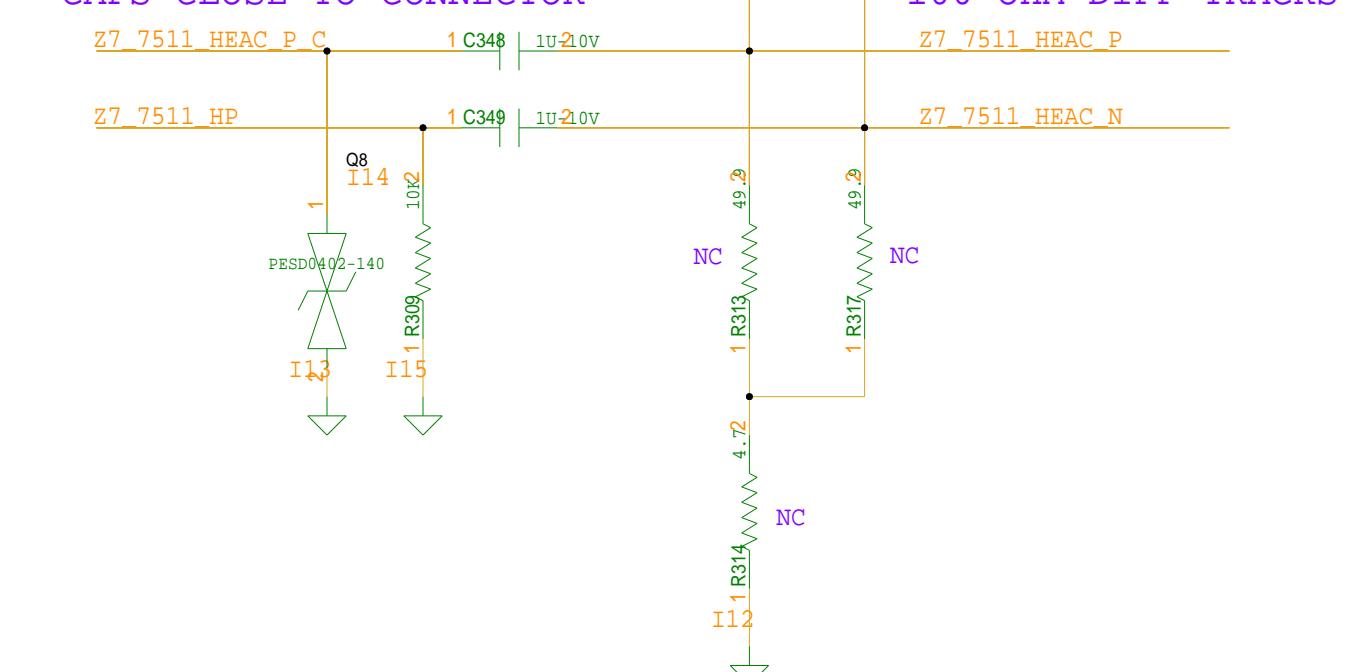


CLOSE TO HDMI CONNECTOR



Z7_7511_CEC (2) → D14 1N4148 (1) → R315 (1) → Z7_3V3_7511_MVDD (1)

CAPS CLOSE TO CONNECTOR



Z7_7511_SCL (1) → R310 (1) → 1.8Ω 1% → Z7_7511_5V0 (1)

Z7_7511_SDA (1) → R311 (1) → 1.8Ω 1% → Z7_7511_5V0 (1)

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ZYNQ-7 PL HDMI INOUT

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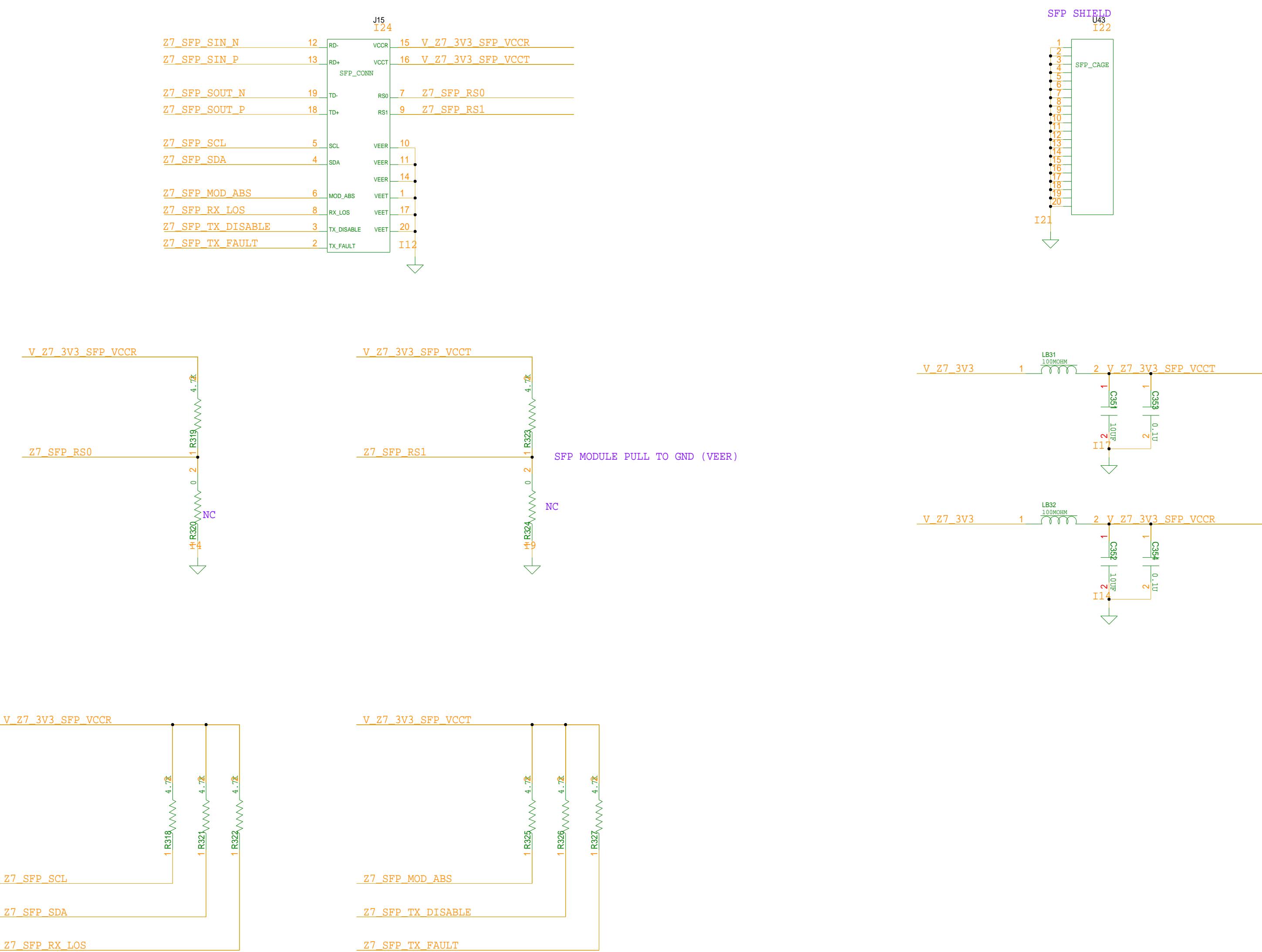
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ZYNQ-7 PL SFP+/SFP INOUT

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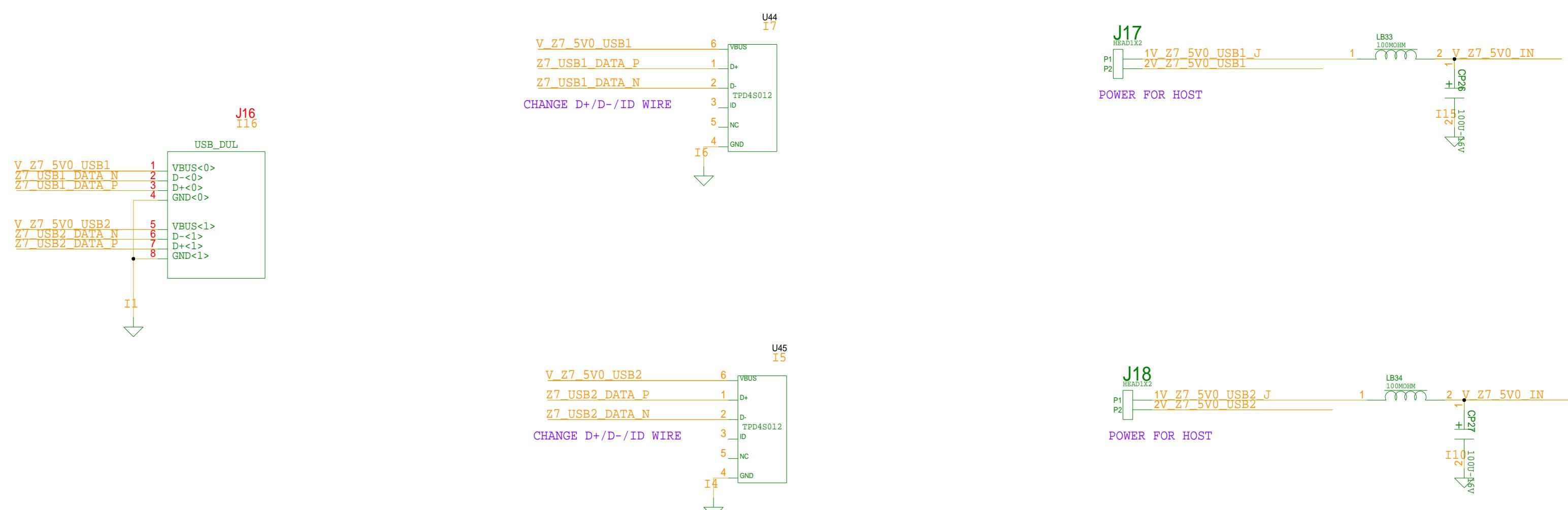
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ZYNQ-7 PL USB INOUT

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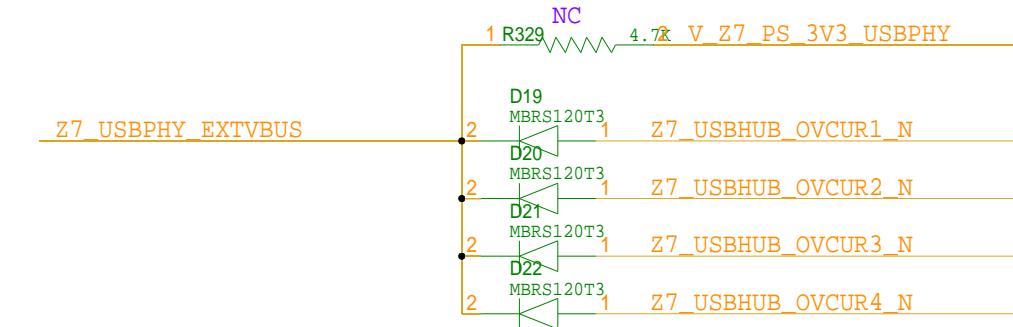
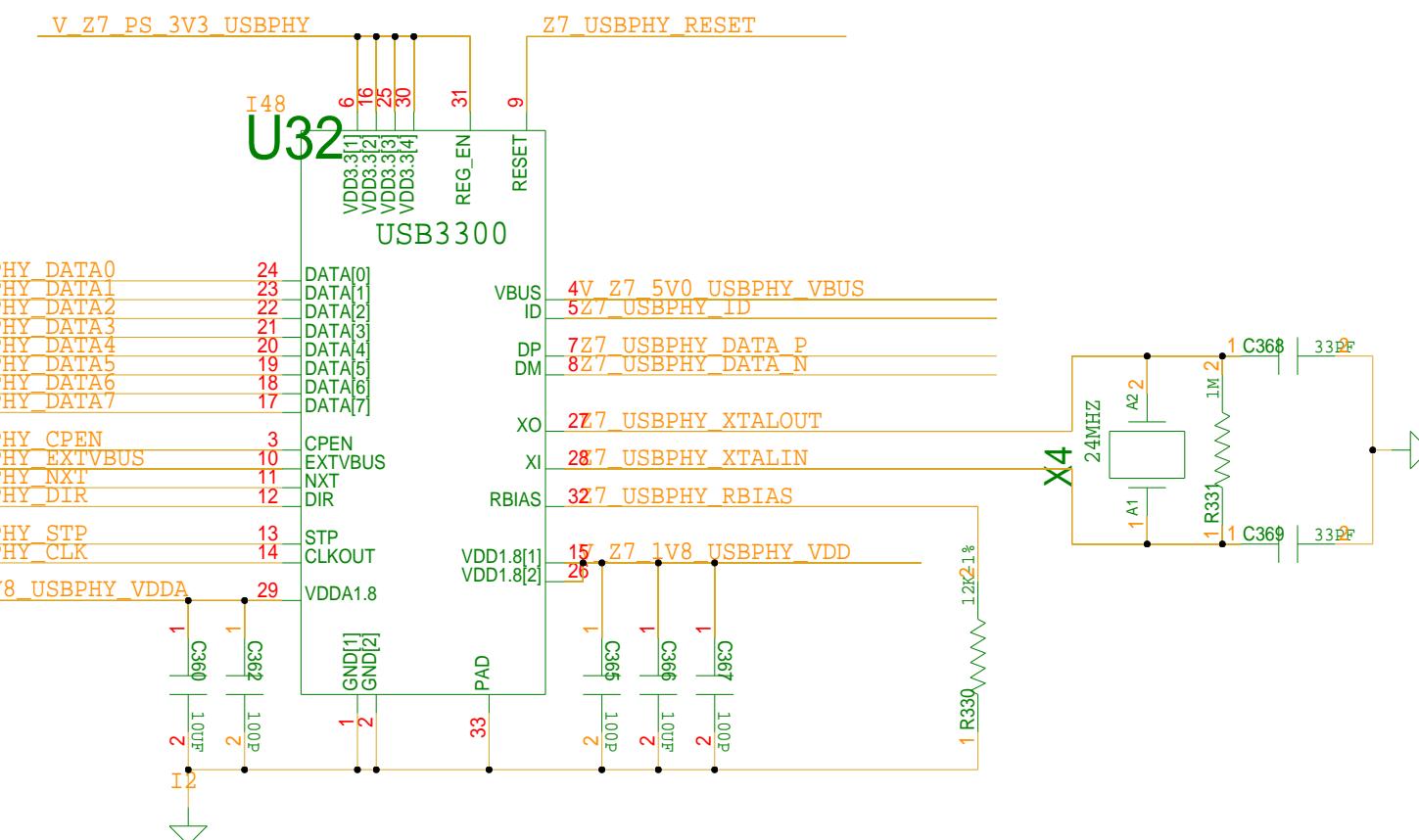
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SCALE SHEET OF

ZYNQ-7 PL USB PHY (1)

REVOLUTIONS

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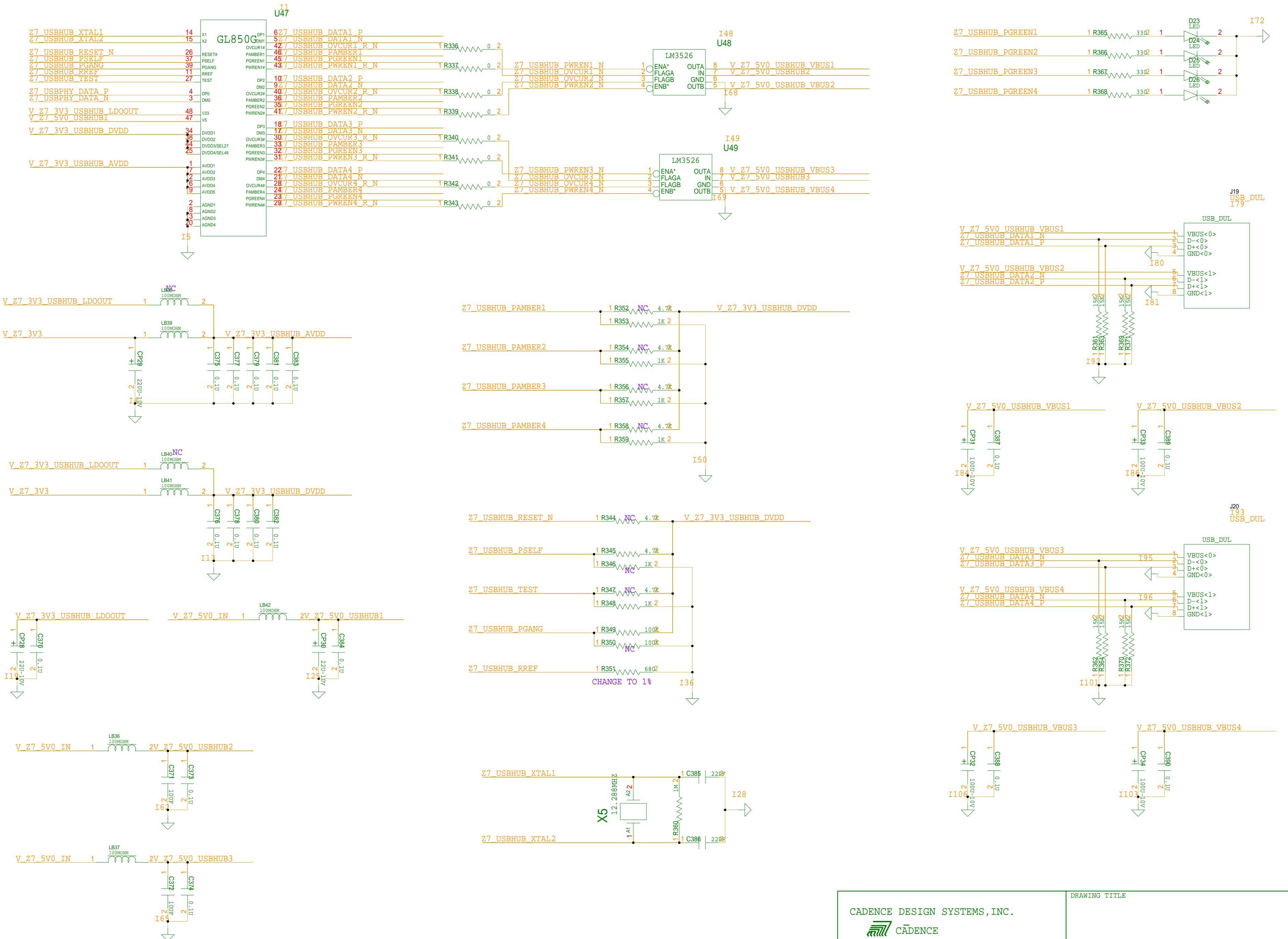
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ZYNQ-7 PL USB PHY (2)

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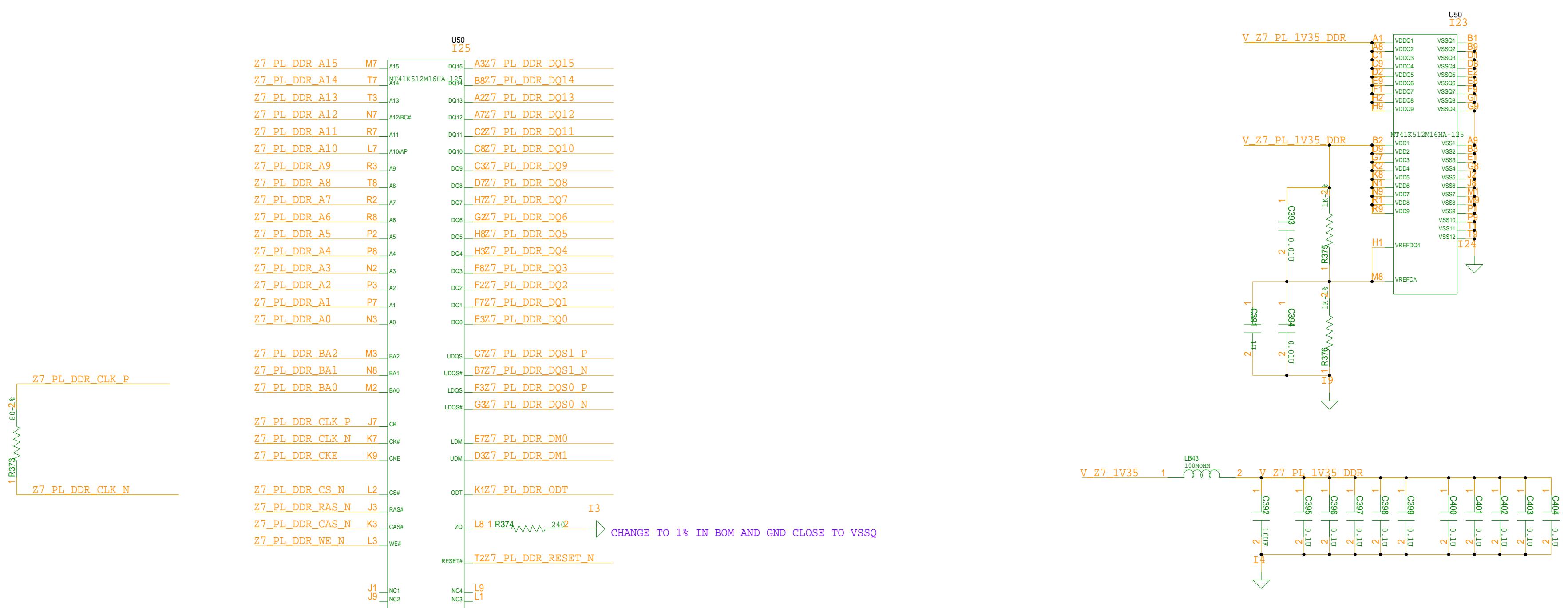
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ZYNQ-7 PL DDR3

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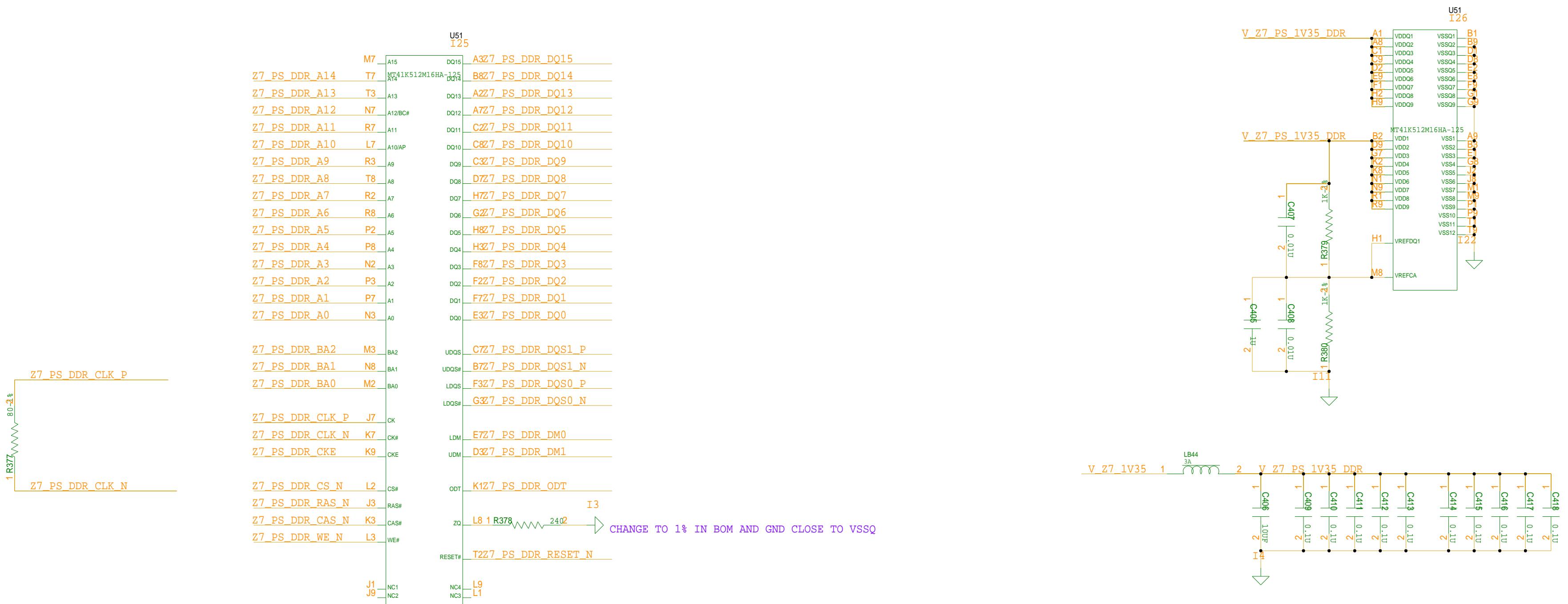
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ZYNQ-7 PS DDR3 (1)

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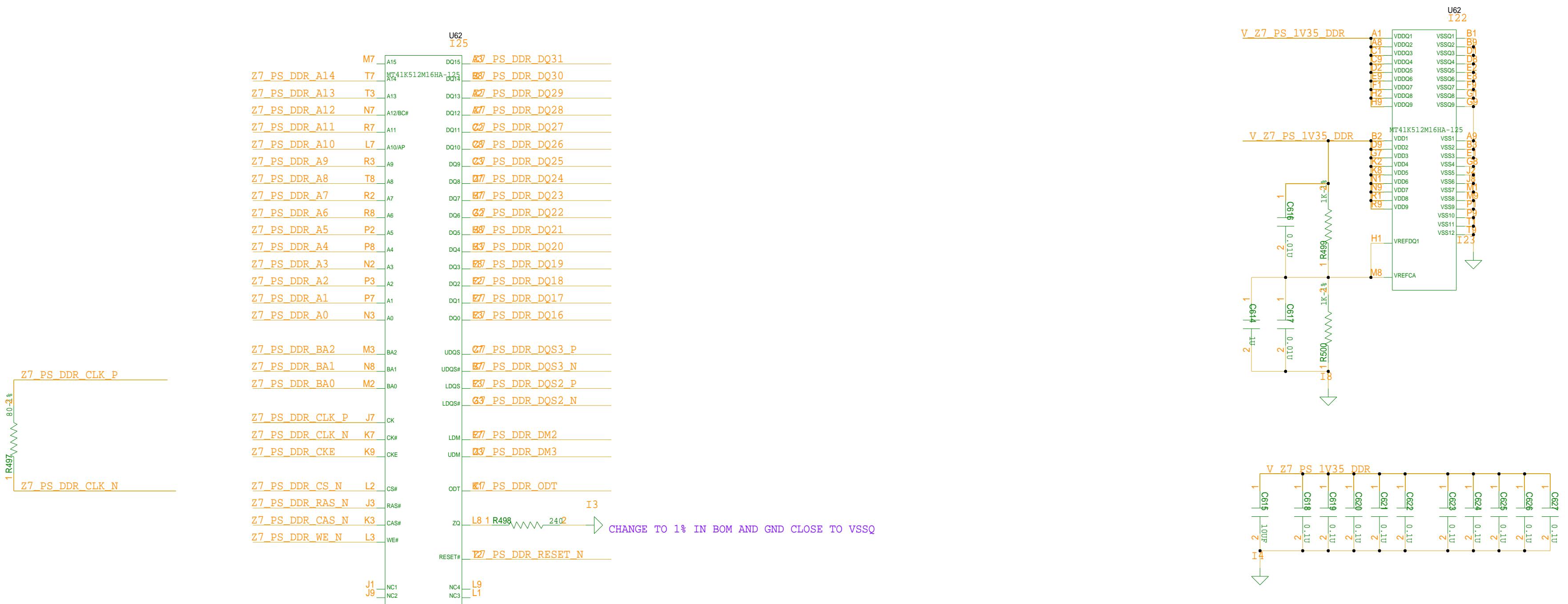
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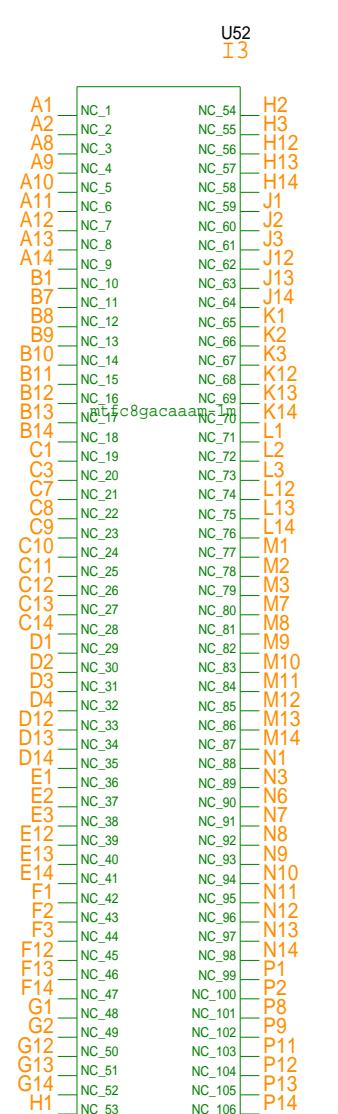
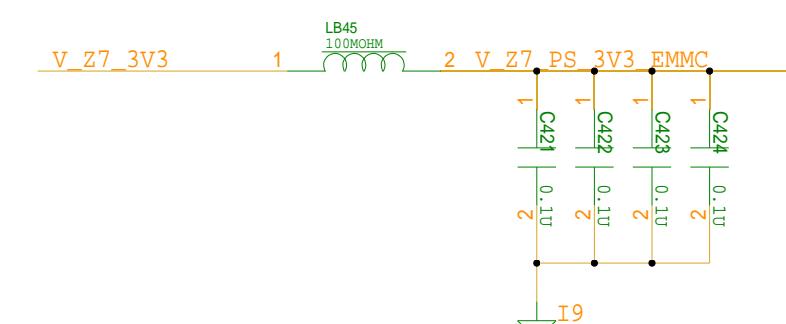
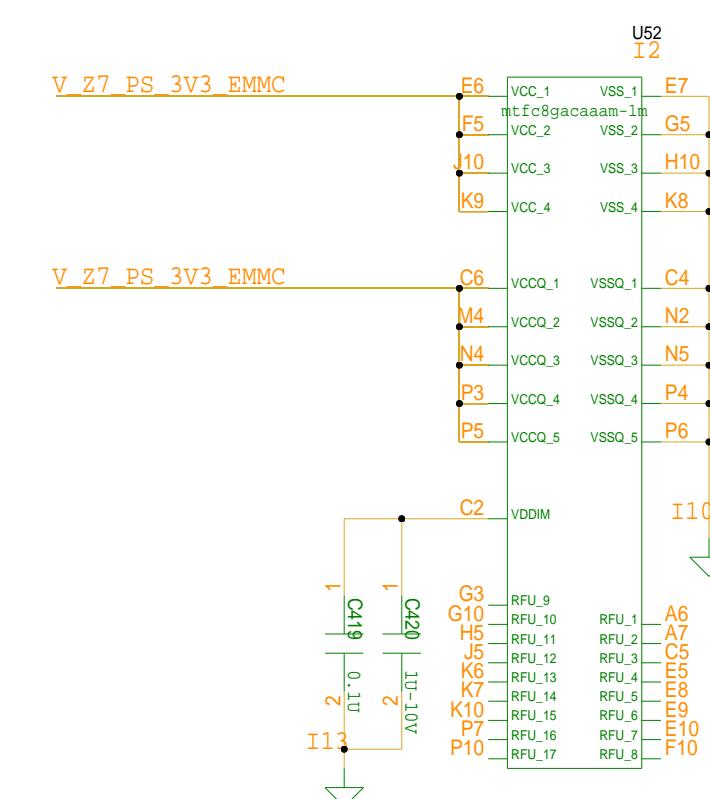
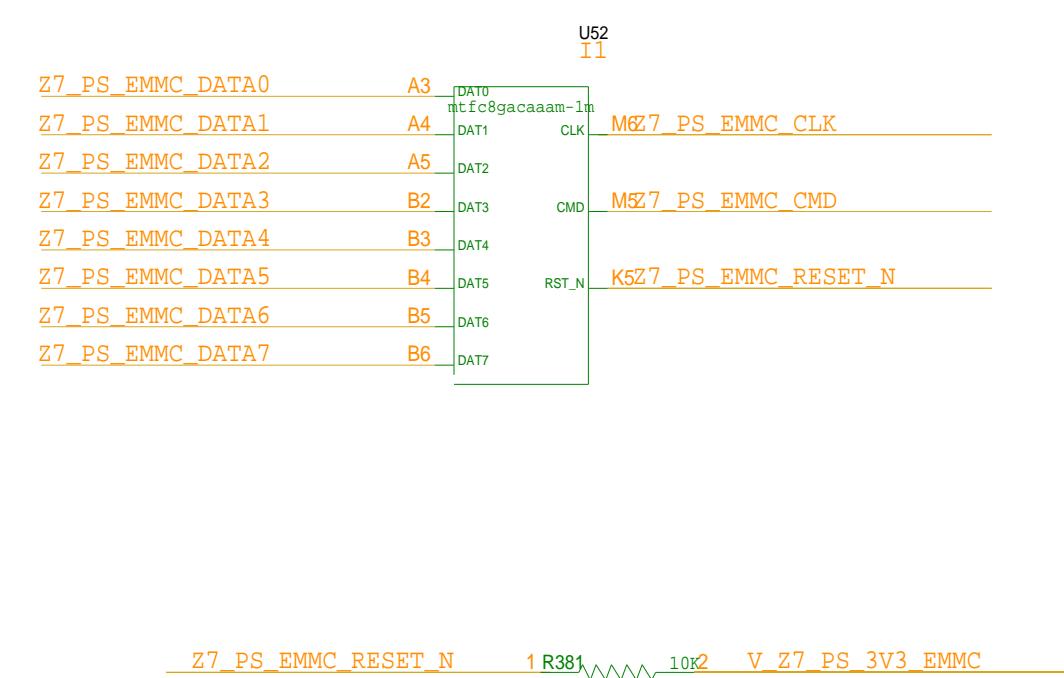
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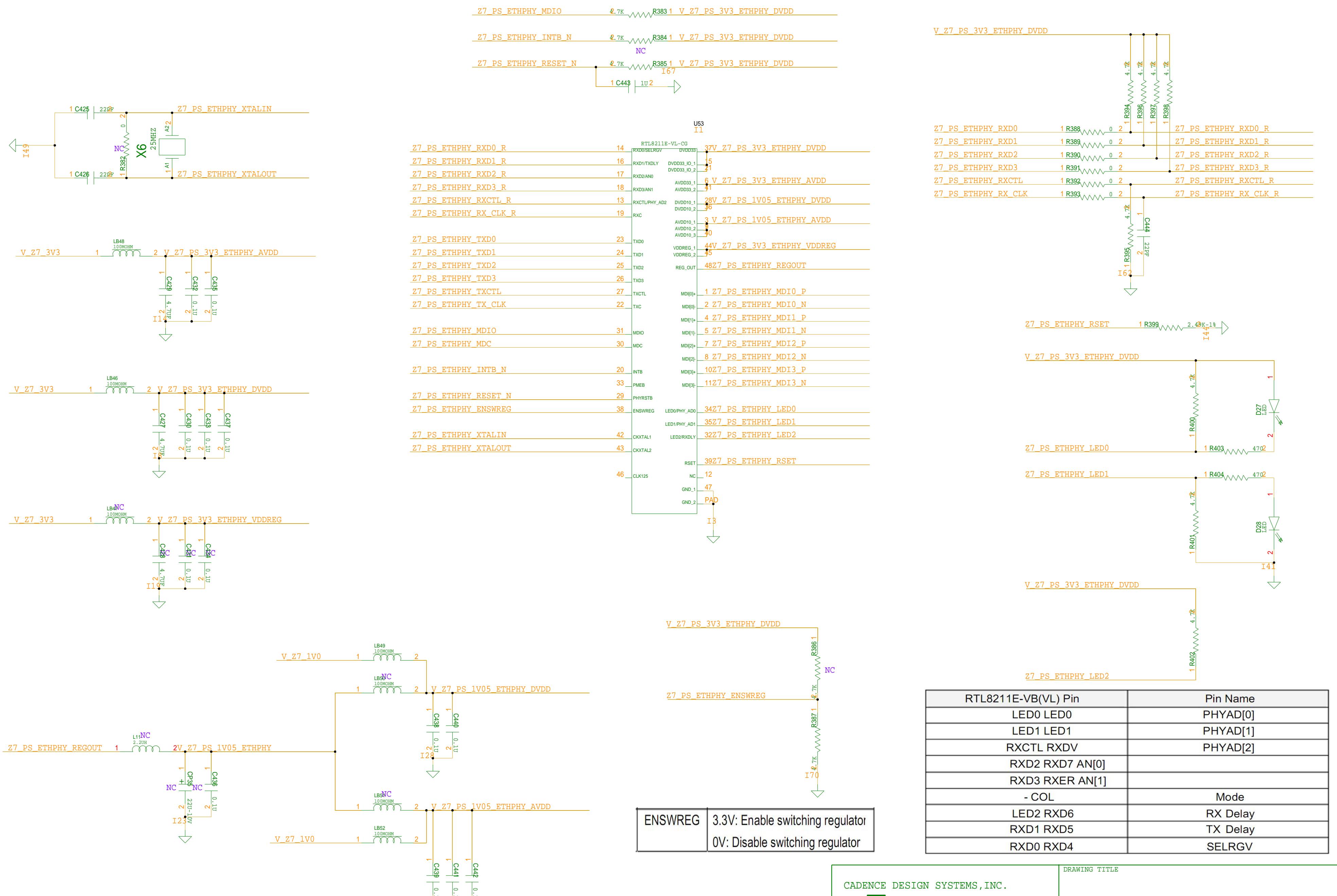
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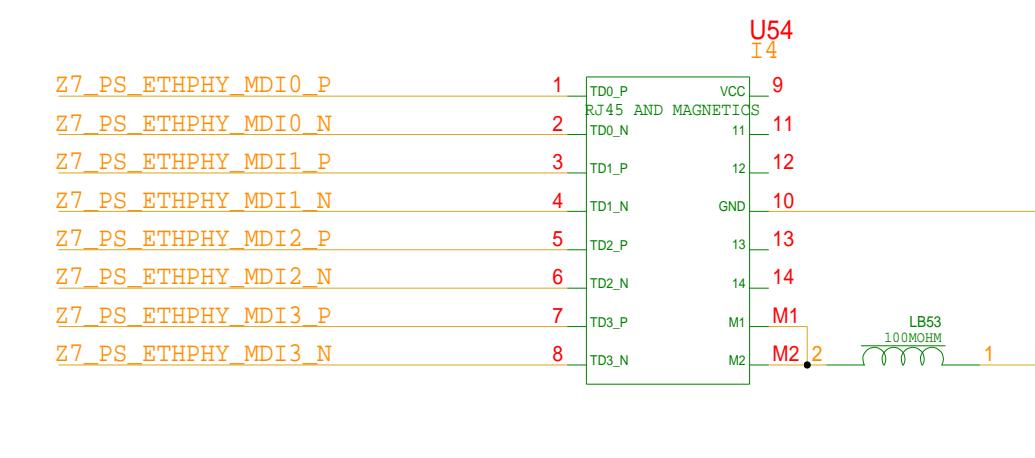
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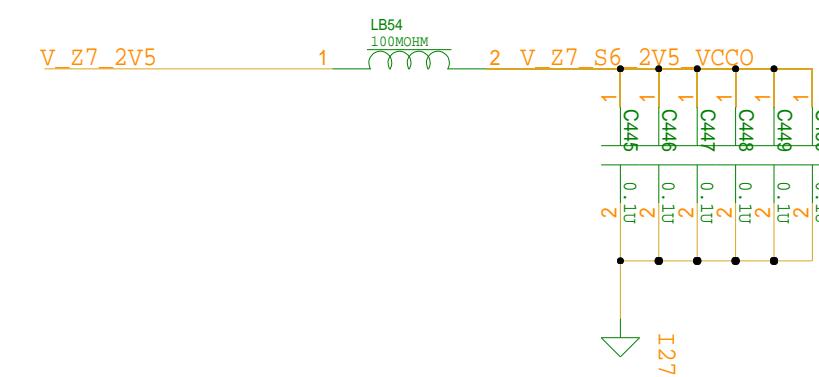
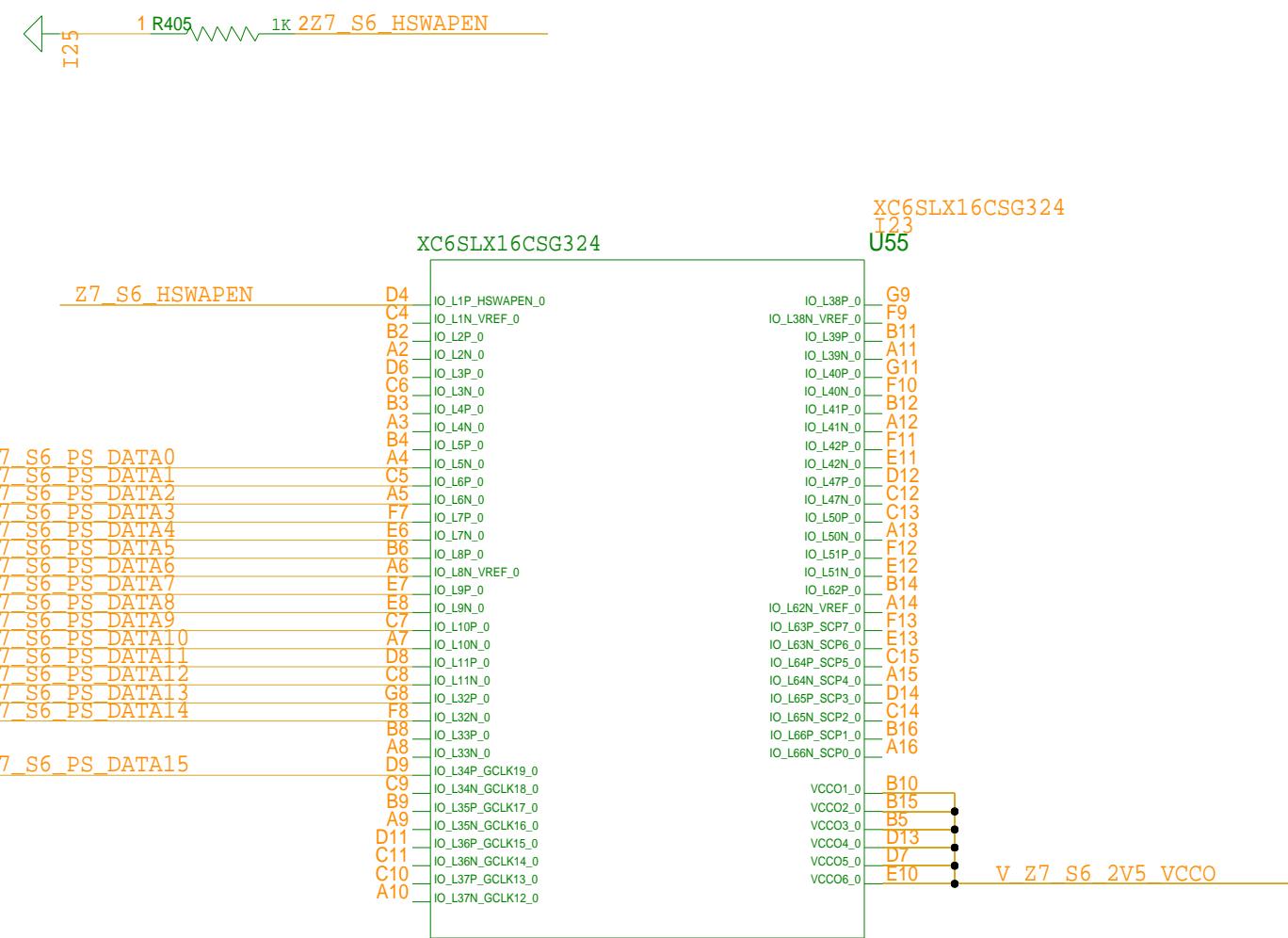
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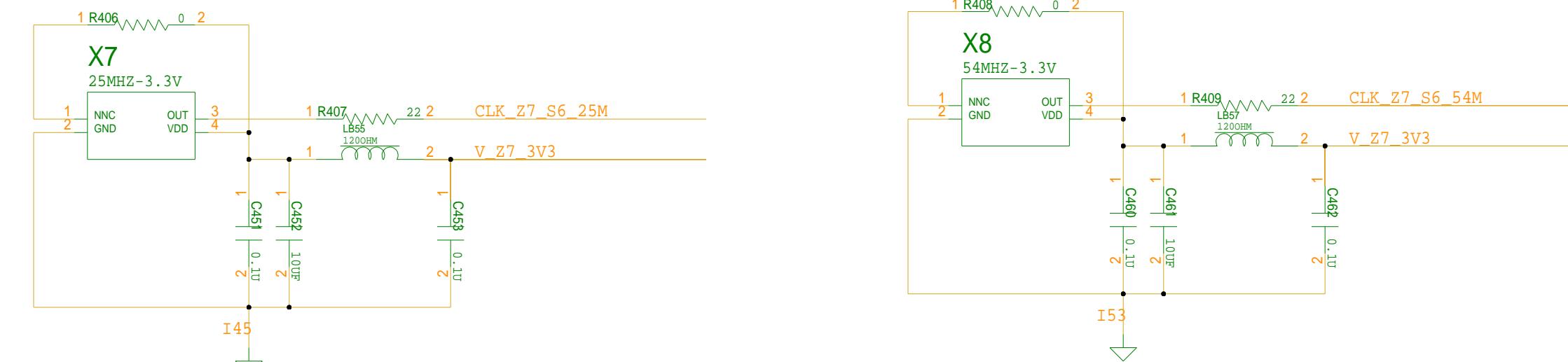
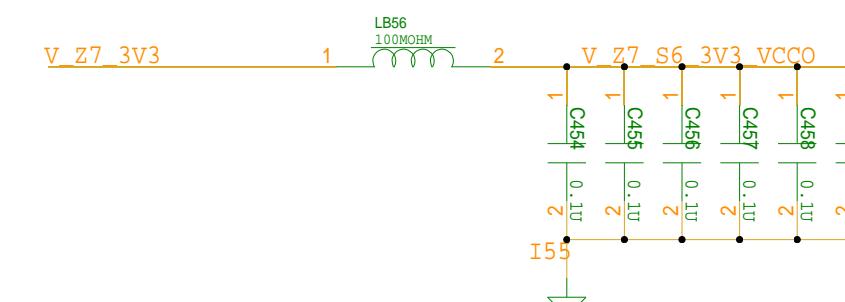
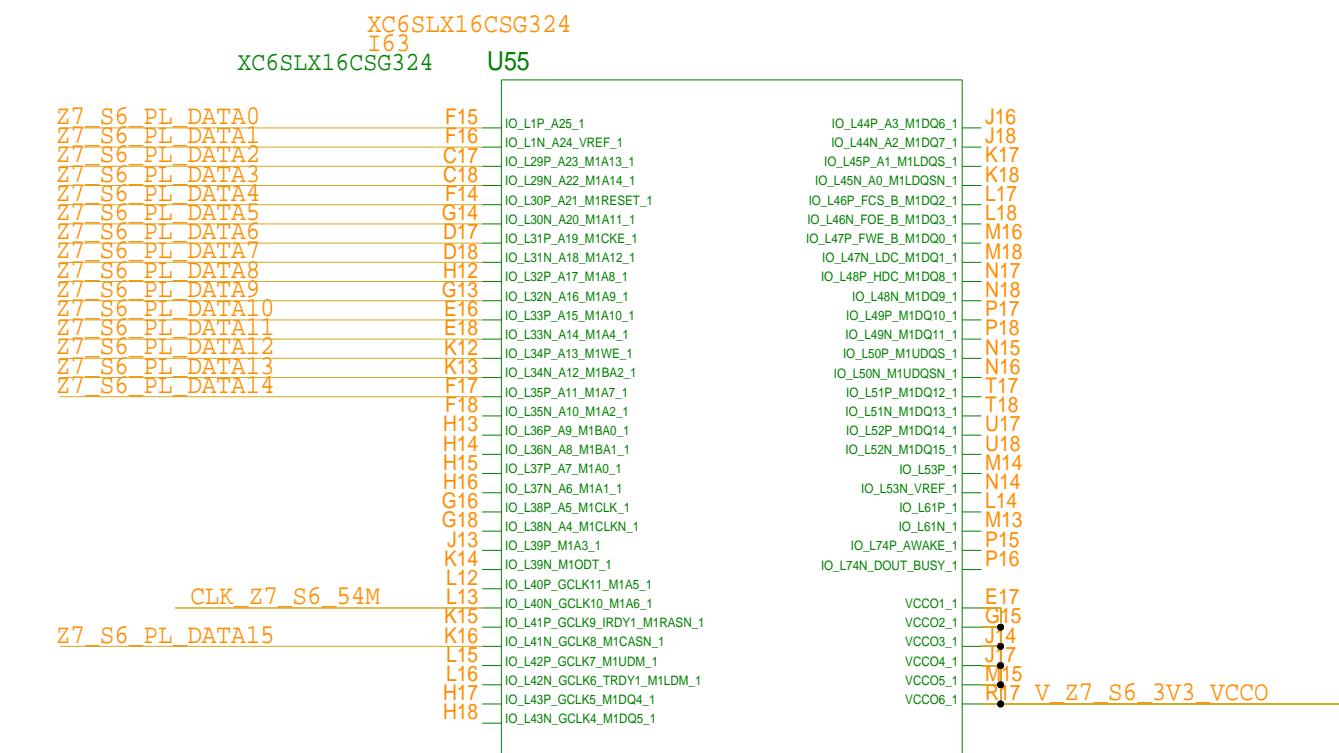
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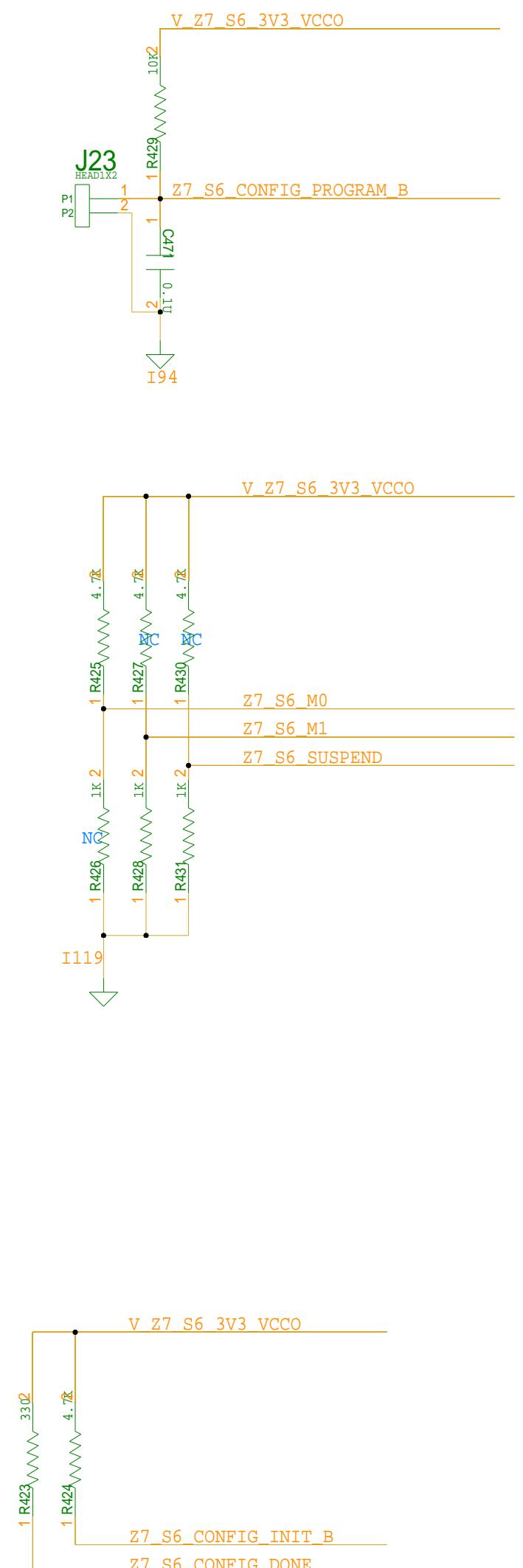
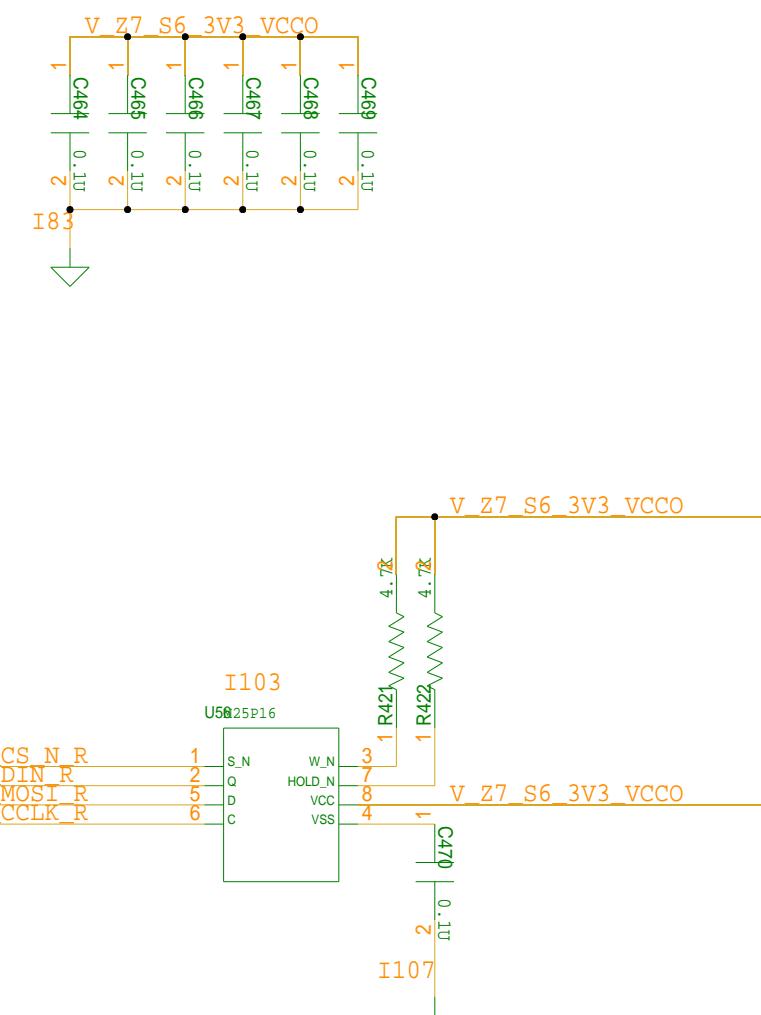
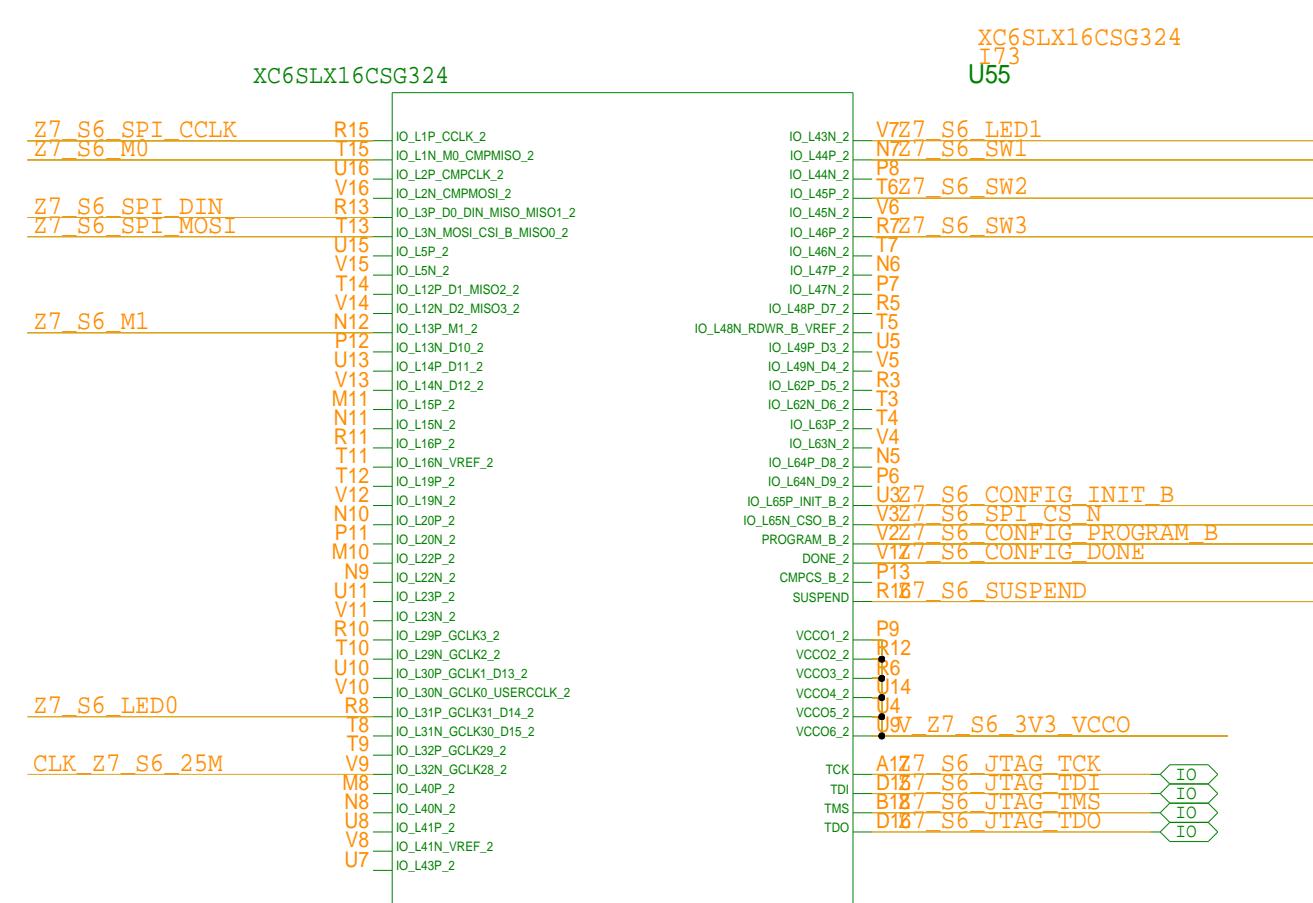
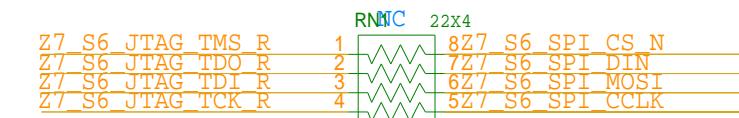
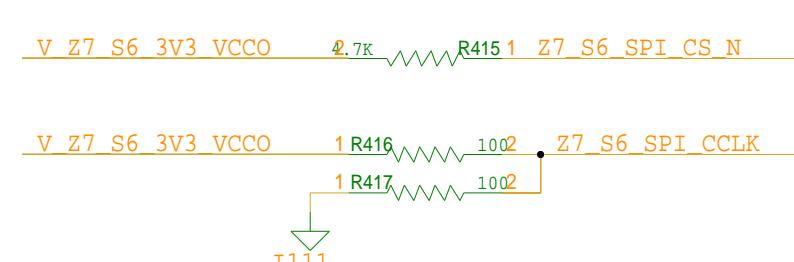
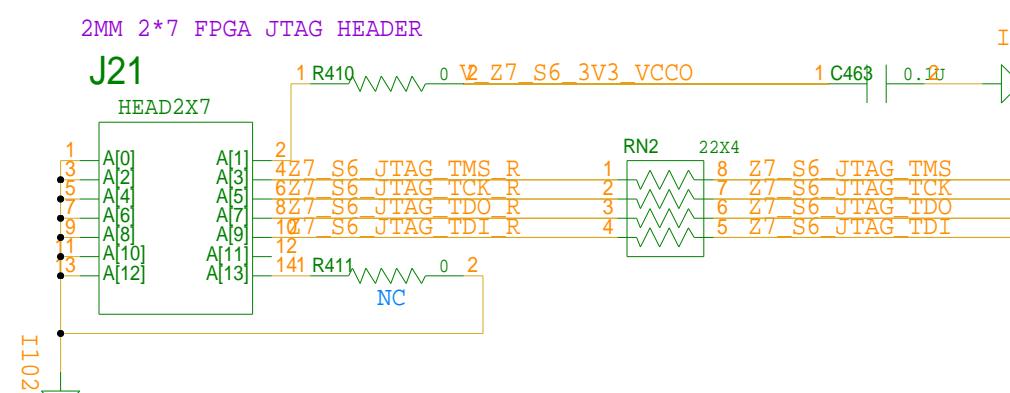
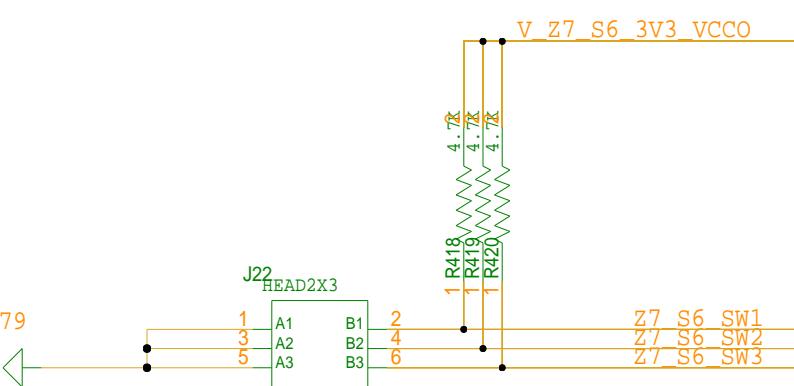
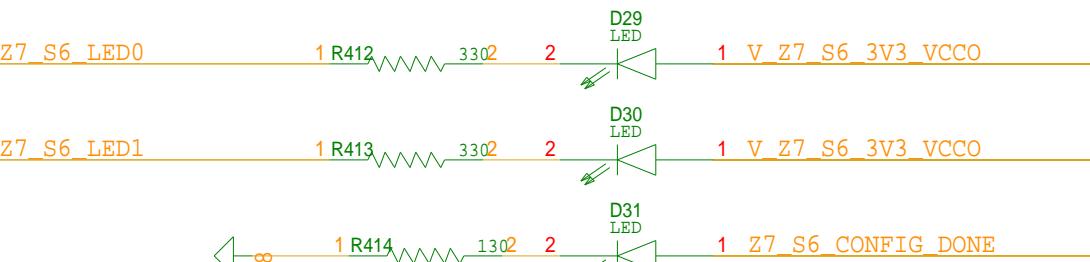
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ZYNQ-7 SPARTAN6 (3)

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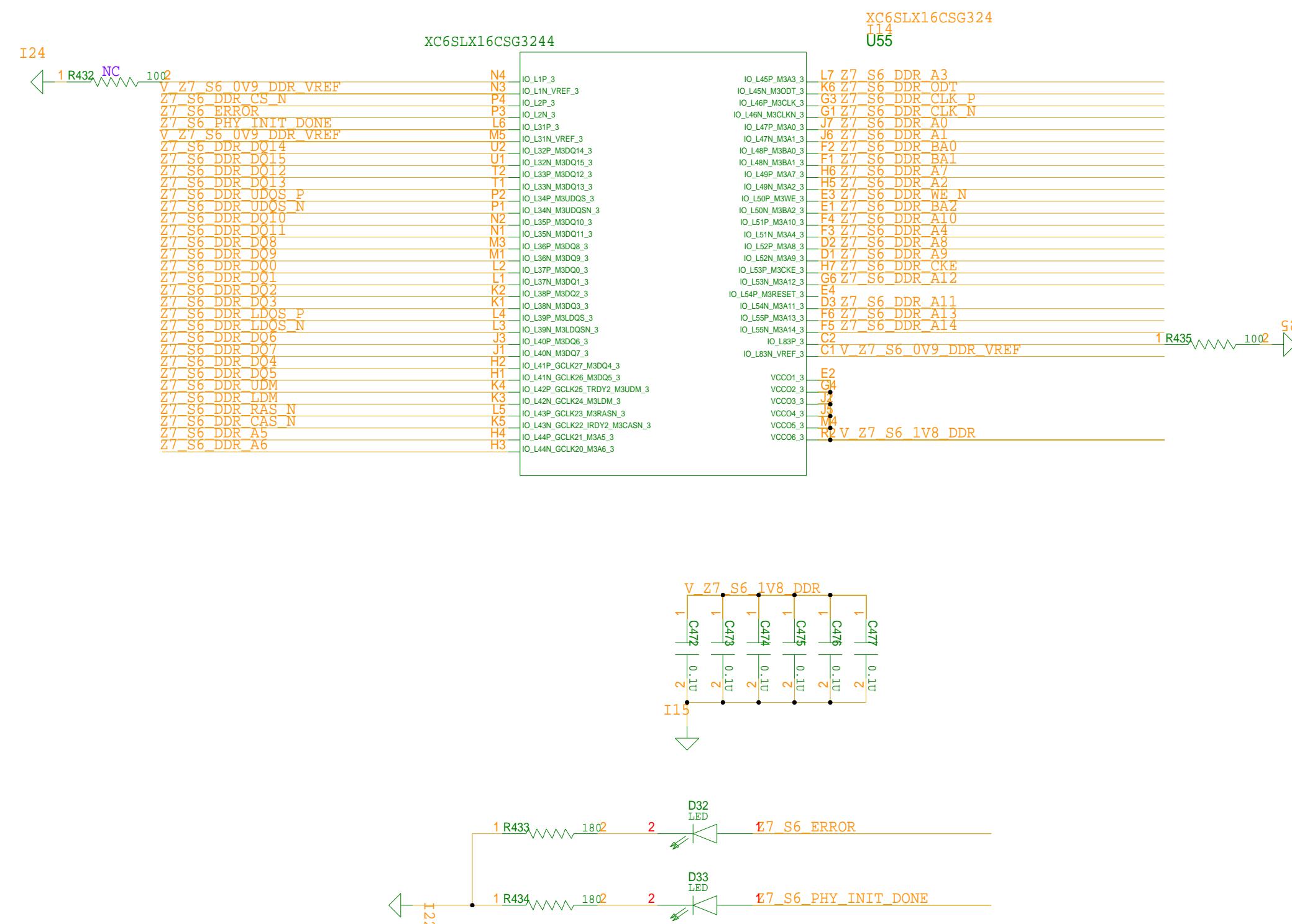
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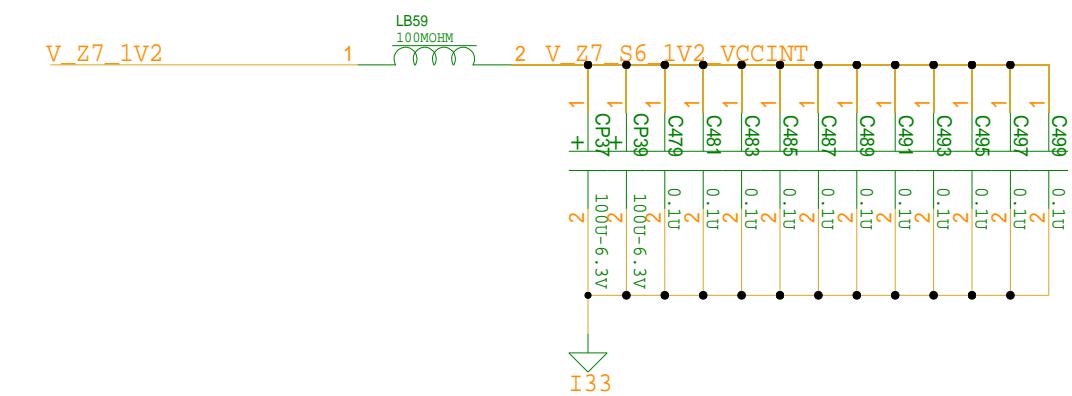
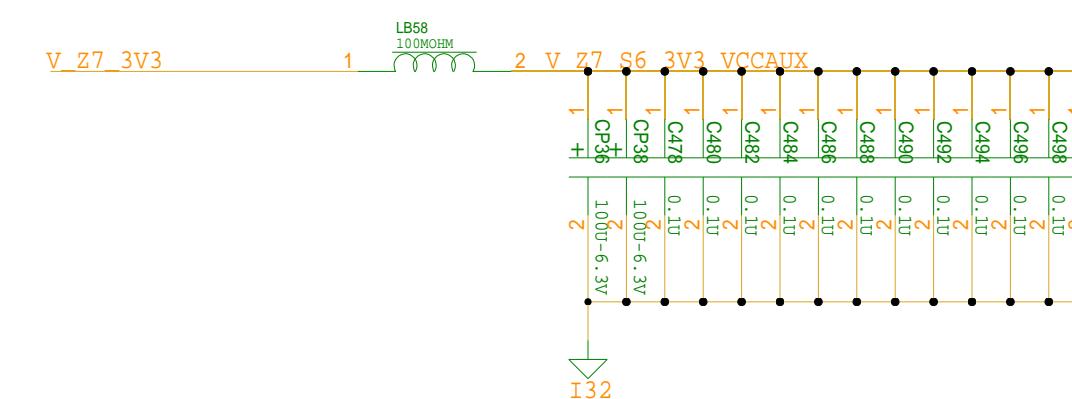
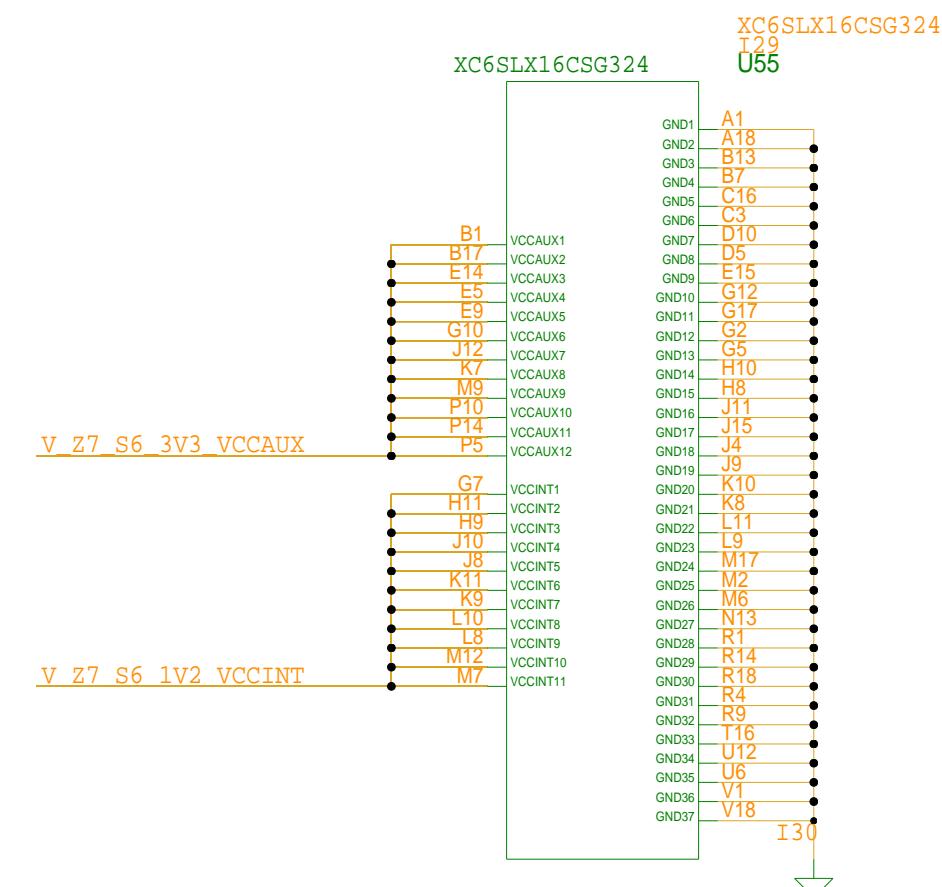
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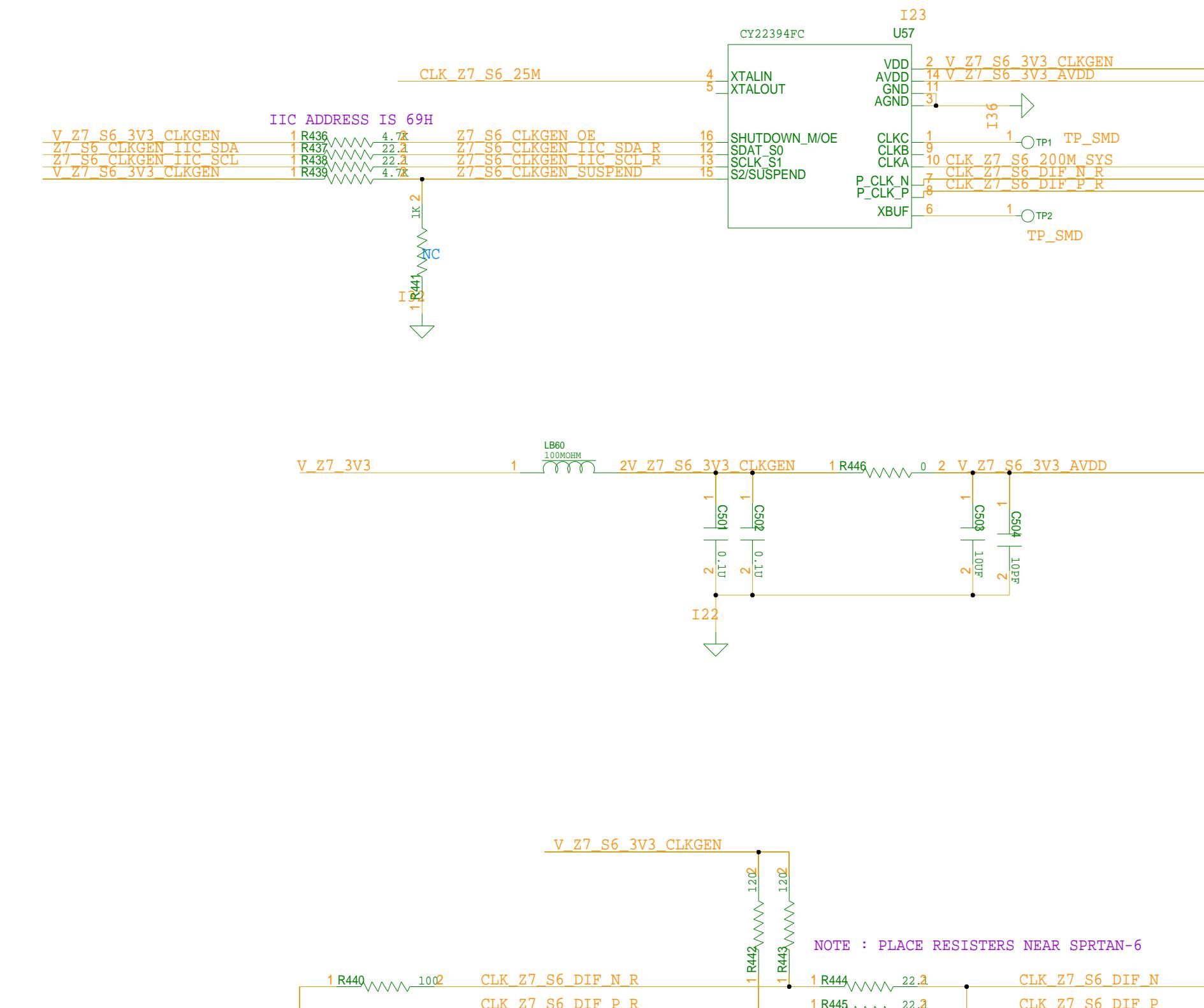
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FPGA DDR2 200M-CLOCK



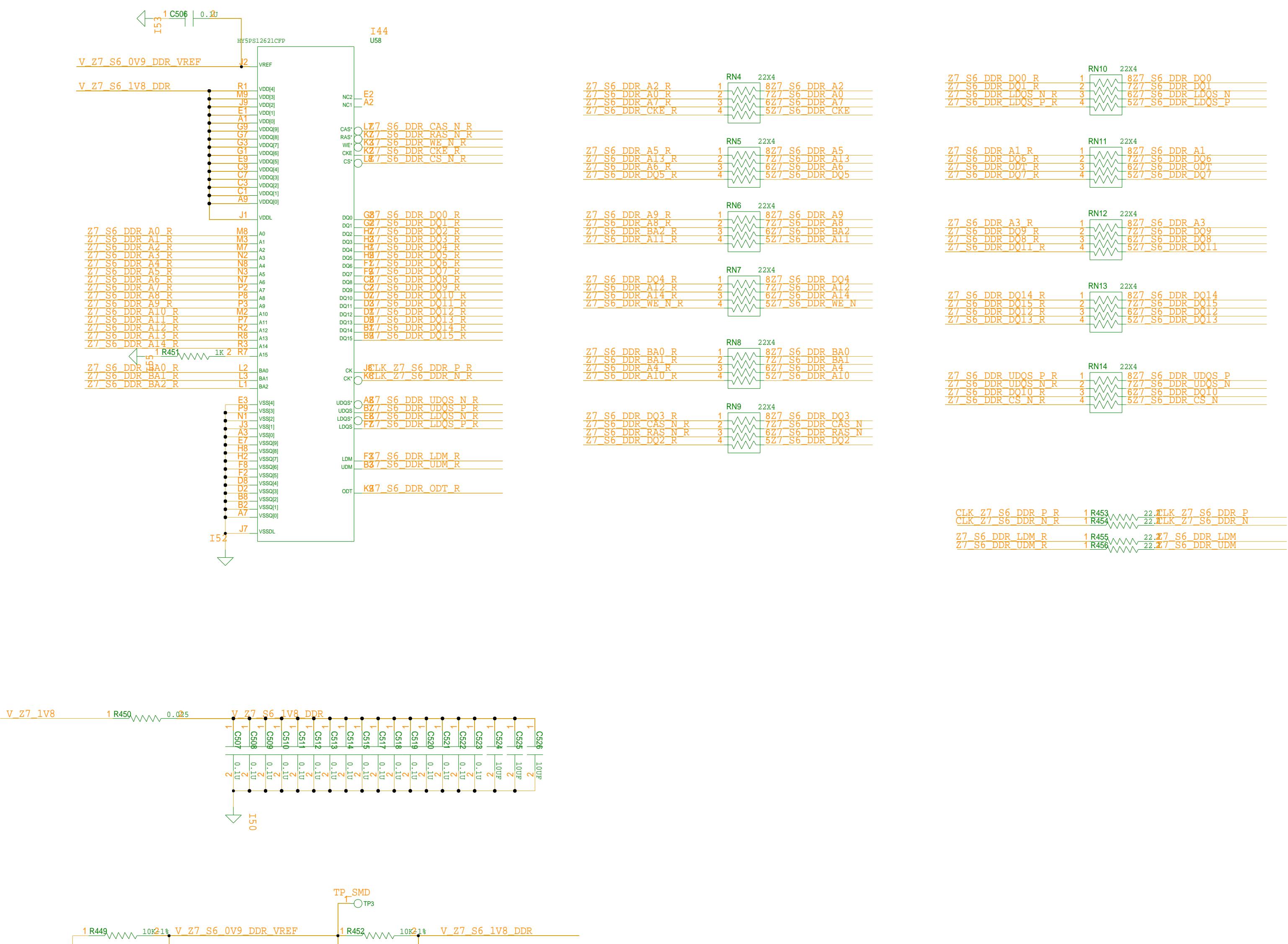
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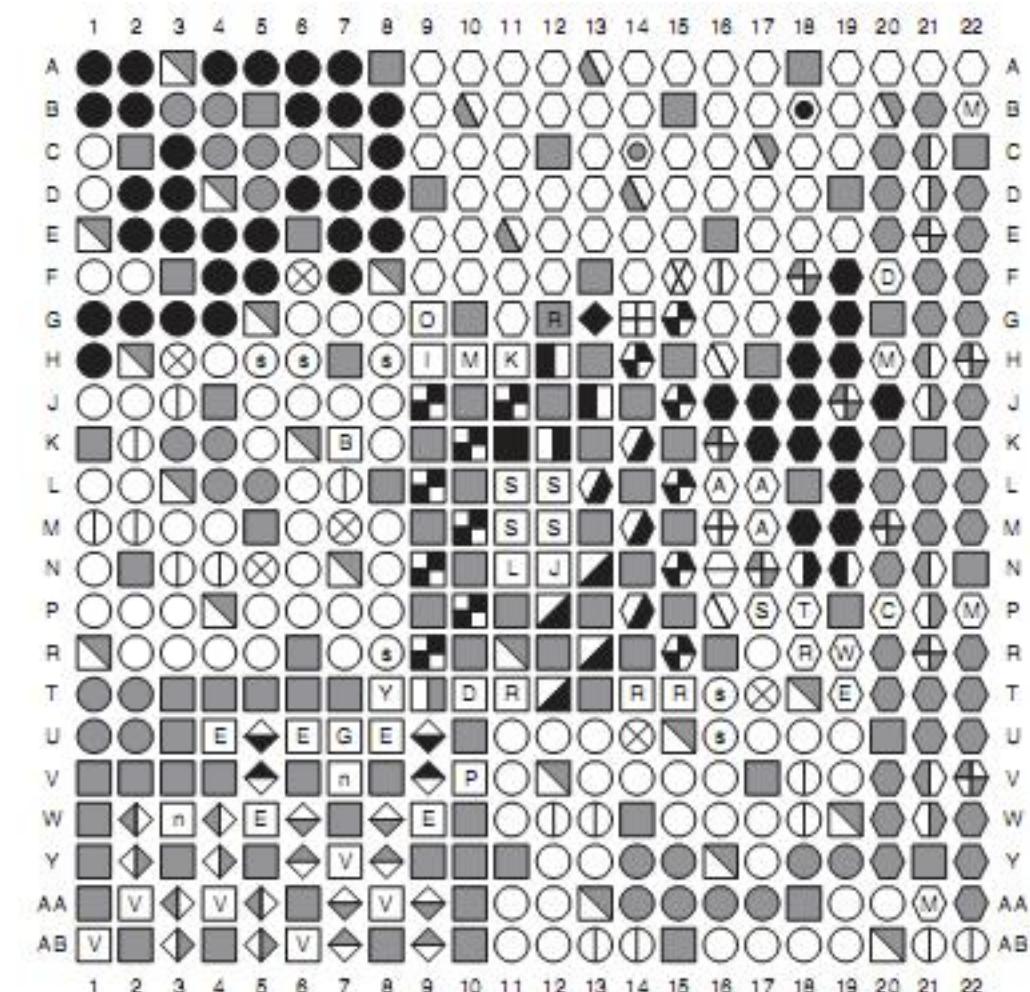
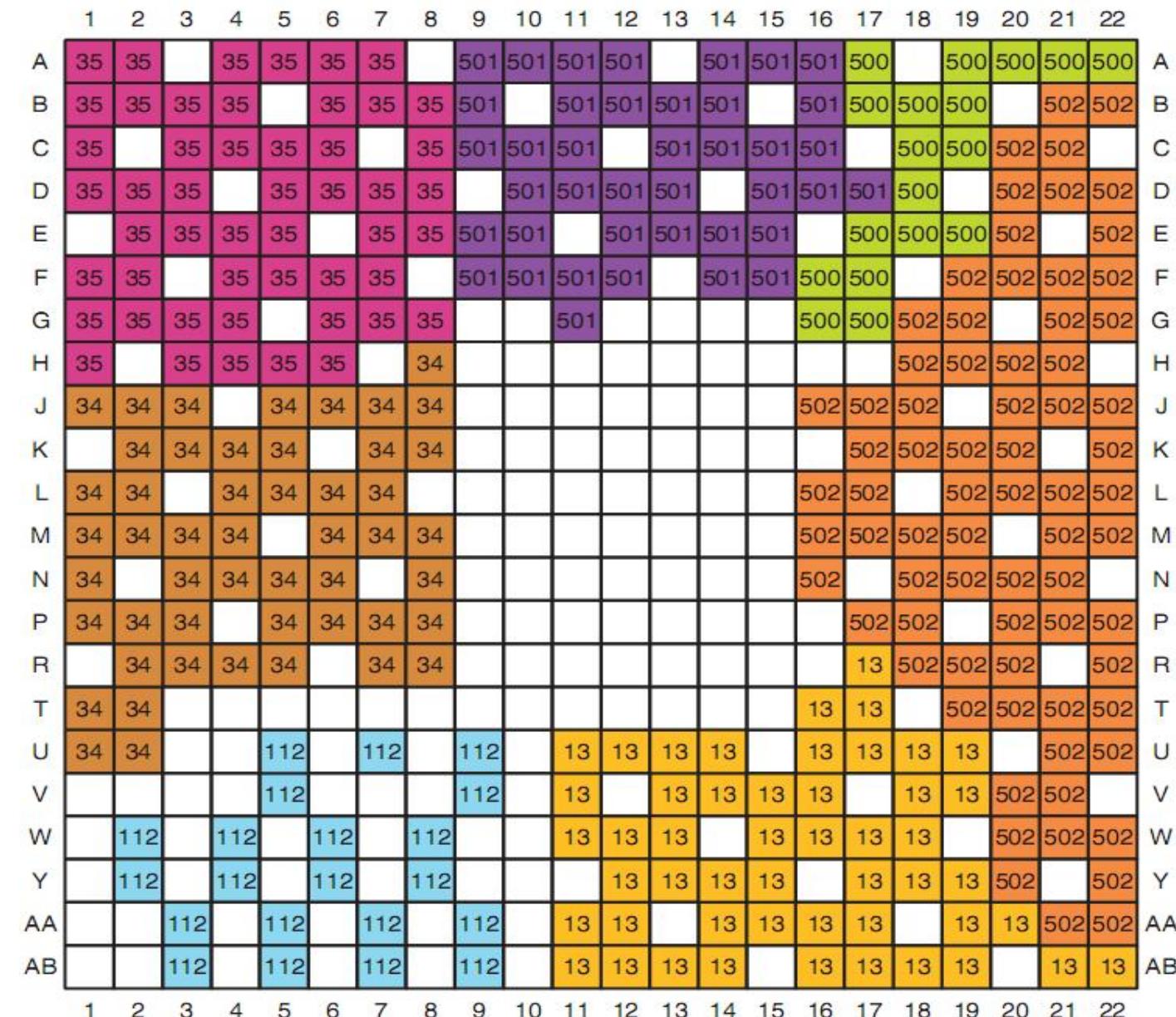
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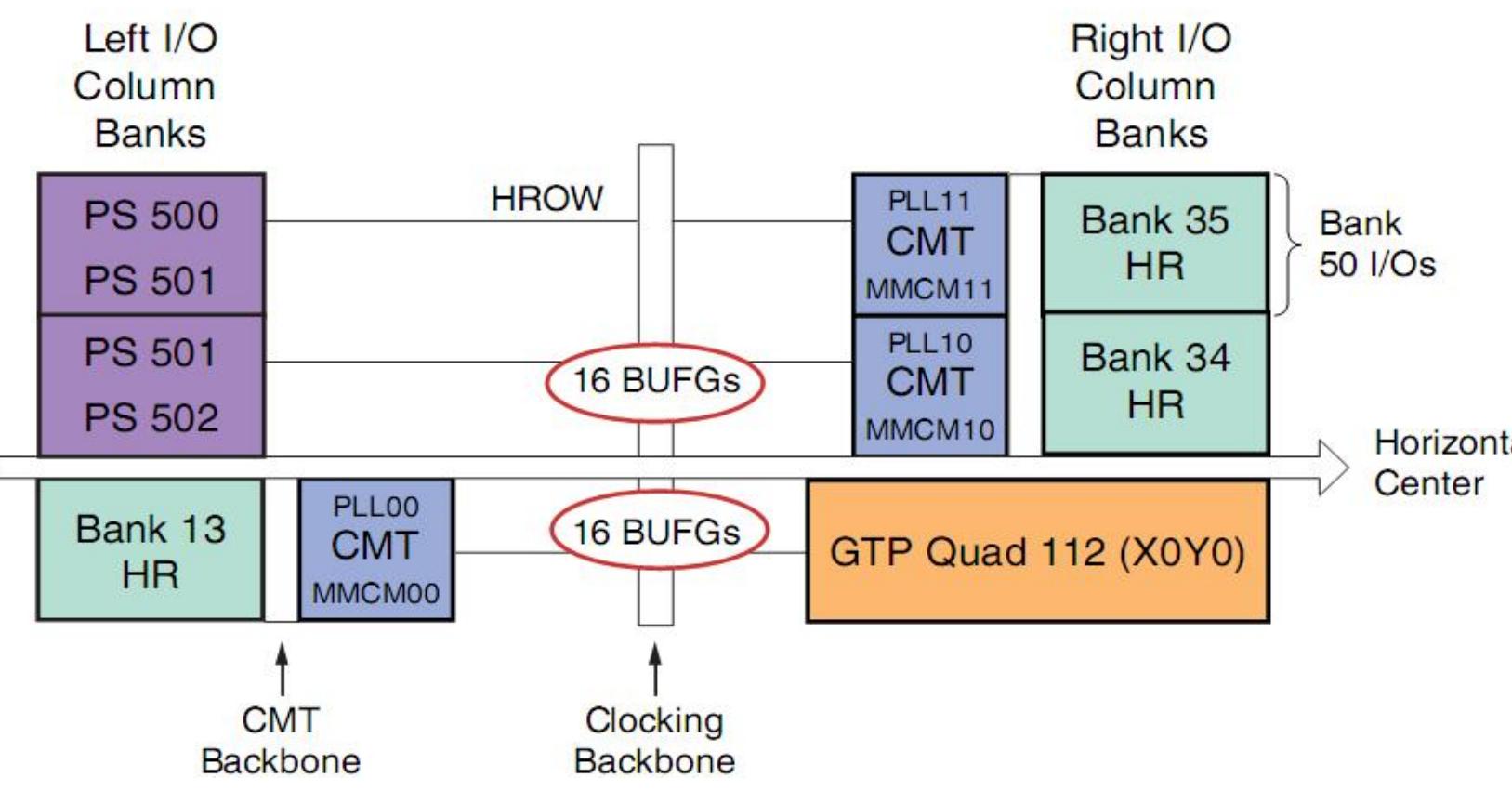
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BANK35 : 3.3V SPARTAN6/ USB/HDMI INOUT
BANK34 : 1.35V DDR3
BANK13 : 3.3V HDMI TRANSMITER
BANK112 : SFP

BANK502 : 1.35V DDR3*2
BANK501 : 2.5V SPARTAN6/ 88E1111
BANK500 : 3.3V SPI FLASH



User I/O Pins	Transceiver Pins	Dedicated Pins	Other Pins	PS MIO Pins	PS DDR Pins
<ul style="list-style-type: none"> ○ IO_LXXY_# ● IO_XX_# 	<ul style="list-style-type: none"> E MGTAVCC_G# V MGTAVTT_G# A MGTVCVAUX_G# < MGTAVTTRCAL G MGTRREF ◆ MGTRFCLK1OP ◆ MGTRFCLK1ON ◆ MGTPRXP ◆ MGTPRXN ◆ MGTPTXP ◆ MGPTXN B PUDC_B ● ADOP/ADON- AD15P/AD15N ⊕ VRN ⊖ VRP ⊗ VREF ⊖ DOS ● MRCC ● SRCC 	<ul style="list-style-type: none"> ■ CFGBVS_0 □ DONE_0 ■ DXP_0 ■ DXN_0 ■ GNDADC_0 ■ INIT_B_0 ■ PROGRAM_B_0 ■ TCK_0 ■ TD_L0 ■ TDO_0 ■ TMS_0 ■ VCCADC_0 ■ VCCBATT_0 ■ VP_0 ■ VN_0 ■ VREFP_0 ■ VREFN_0 	<ul style="list-style-type: none"> ■ GND ■ VCCAUX_IO_G# ■ VCCAUX ■ VCCINT ■ VCCO_# ■ VCCBRAM ■ VCCPINT ■ VCCPAUX ■ VCCO_MIO0 ■ VCCO_MIO1 ■ VCCO_DDR ■ VCCPLL ■ RSVDVCC[3:1] ■ RSVDGND n NC 	<ul style="list-style-type: none"> ● PS_POP_B ○ PS_CLK ○ PS_SRST_B ⊗ PS_MIO_VREF ○ PS_MIO 	<ul style="list-style-type: none"> ○ PS_DDR_CKP ○ PS_DDR_CKN ● PS_DDR_CKE ● PS_DDR_CS_B ○ PS_DDR_RAS_B ○ PS_DDR_CAS_B ● PS_DDR_WE_B ● PS_DDR_BA ● PS_DDR_A ○ PS_DDR_ODT ○ PS_DDR_DRST_B ● PS_DDR_DO ● PS_DDR_DM ● PS_DDR_DOS_P ● PS_DDR_DOS_N ○ PS_DDR_VRP ● PS_DDR_VRN ○ PS_DDR_VREF
<ul style="list-style-type: none"> ○ IO_LXXY_# ● IO_XX_# 	<ul style="list-style-type: none"> E MGTAVCC_G# V MGTAVTT_G# A MGTVCVAUX_G# < MGTAVTTRCAL G MGTRREF ◆ MGTRFCLK1OP ◆ MGTRFCLK1ON ◆ MGTPRXP ◆ MGTPRXN ◆ MGTPTXP ◆ MGPTXN B PUDC_B ● ADOP/ADON- AD15P/AD15N ⊕ VRN ⊖ VRP ⊗ VREF ⊖ DOS ● MRCC ● SRCC 	<ul style="list-style-type: none"> ■ CFGBVS_0 □ DONE_0 ■ DXP_0 ■ DXN_0 ■ GNDADC_0 ■ INIT_B_0 ■ PROGRAM_B_0 ■ TCK_0 ■ TD_L0 ■ TDO_0 ■ TMS_0 ■ VCCADC_0 ■ VCCBATT_0 ■ VP_0 ■ VN_0 ■ VREFP_0 ■ VREFN_0 	<ul style="list-style-type: none"> ■ GND ■ VCCAUX_IO_G# ■ VCCAUX ■ VCCINT ■ VCCO_# ■ VCCBRAM ■ VCCPINT ■ VCCPAUX ■ VCCO_MIO0 ■ VCCO_MIO1 ■ VCCO_DDR ■ VCCPLL ■ RSVDVCC[3:1] ■ RSVDGND n NC 	<ul style="list-style-type: none"> ● PS_POP_B ○ PS_CLK ○ PS_SRST_B ⊗ PS_MIO_VREF ○ PS_MIO 	<ul style="list-style-type: none"> ○ PS_DDR_CKP ○ PS_DDR_CKN ● PS_DDR_CKE ● PS_DDR_CS_B ○ PS_DDR_RAS_B ○ PS_DDR_CAS_B ● PS_DDR_WE_B ● PS_DDR_BA ● PS_DDR_A ○ PS_DDR_ODT ○ PS_DDR_DRST_B ● PS_DDR_DO ● PS_DDR_DM ● PS_DDR_DOS_P ● PS_DDR_DOS_N ○ PS_DDR_VRP ● PS_DDR_VRN ○ PS_DDR_VREF

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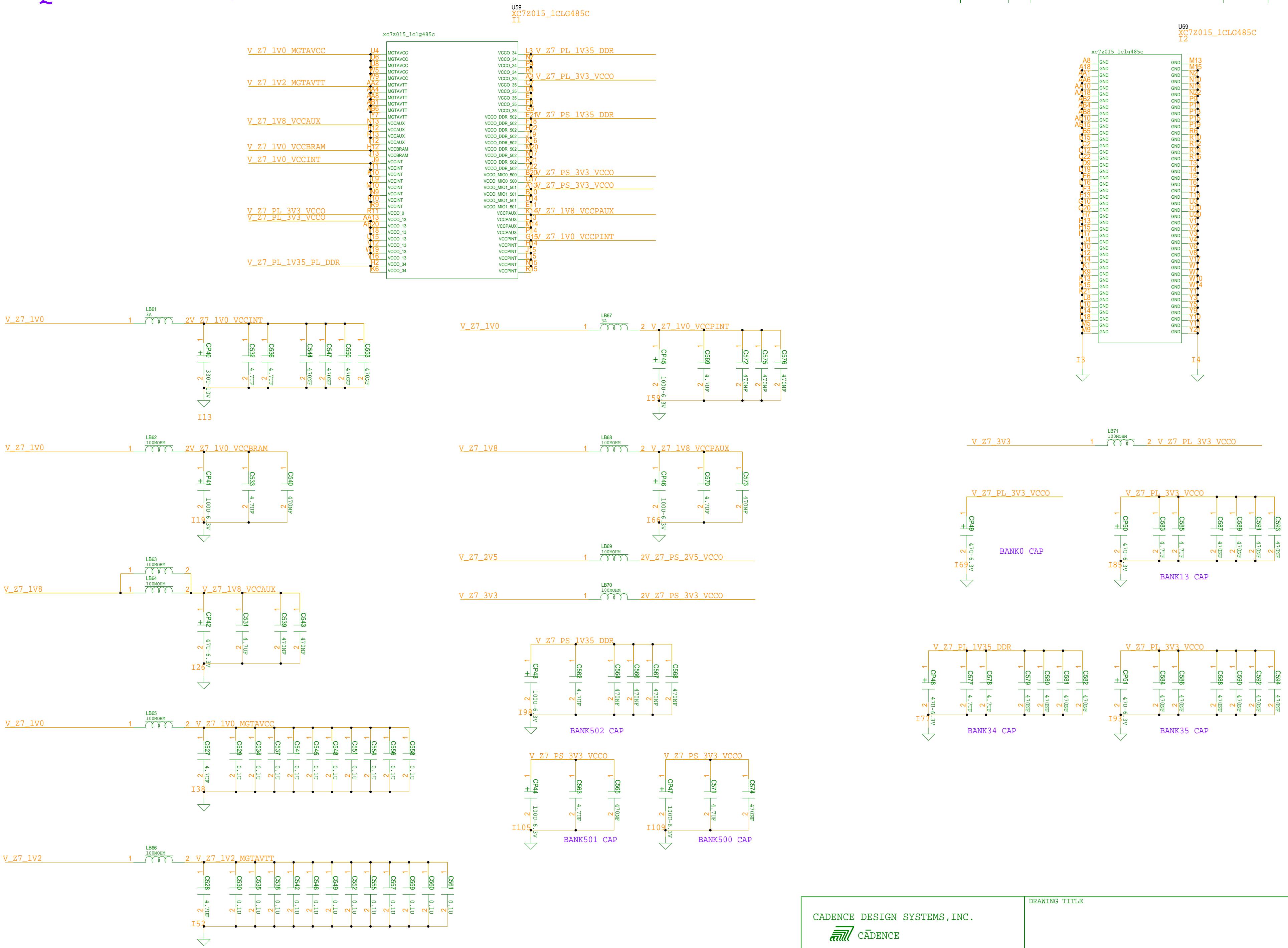
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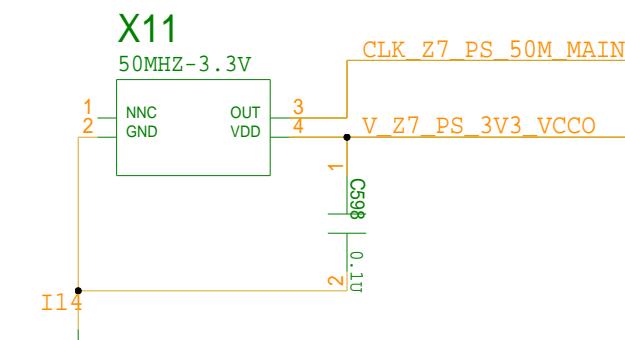
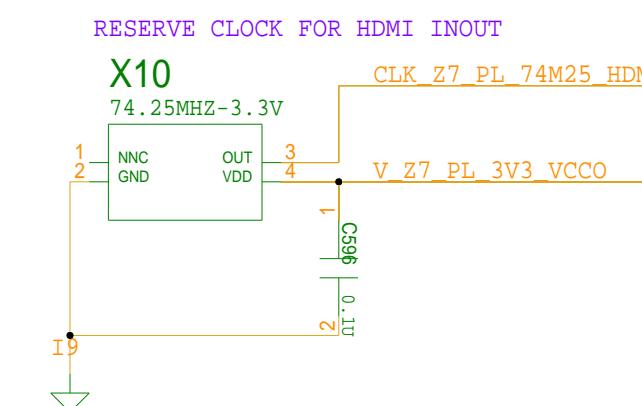
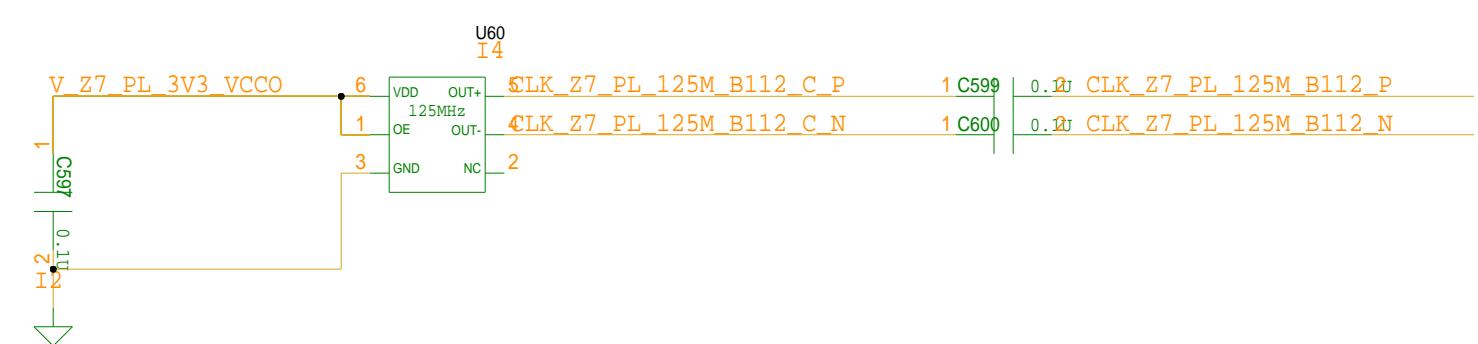
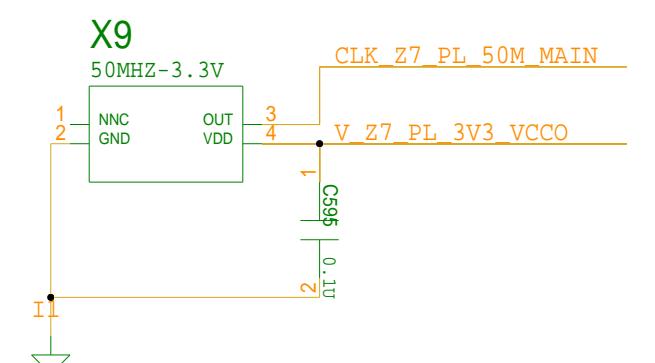
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Z7_CONFIG_CFBVS 2.7K R457 1 V_Z7_3V3_VCCO

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Z7_CONFIG_PROGRAM_B 2.7K R461 1 V_Z7_3V3_VCCO

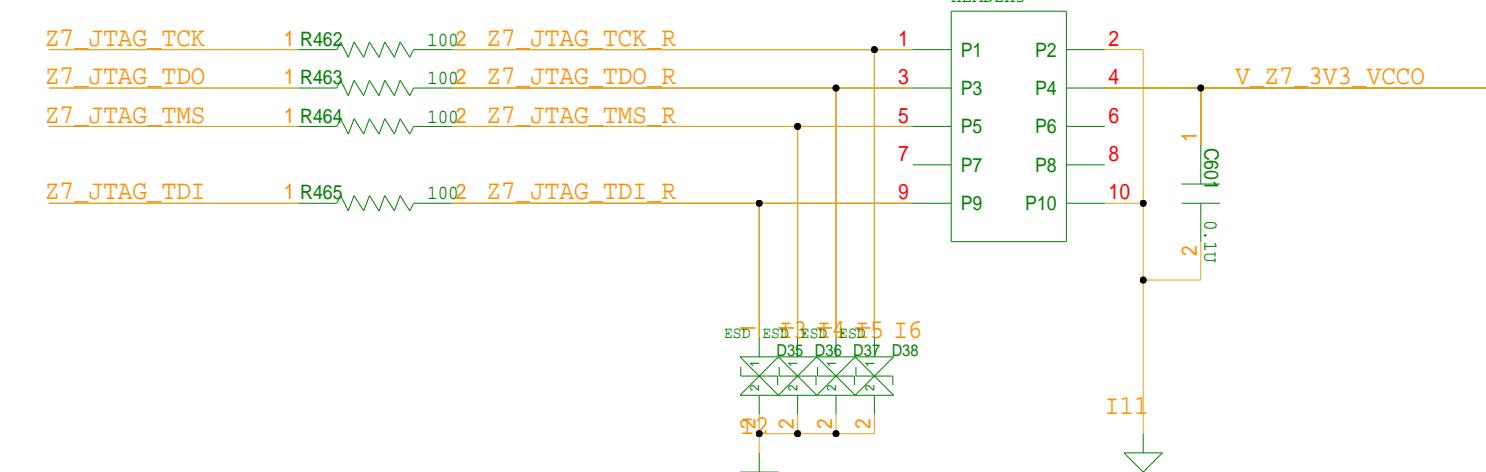
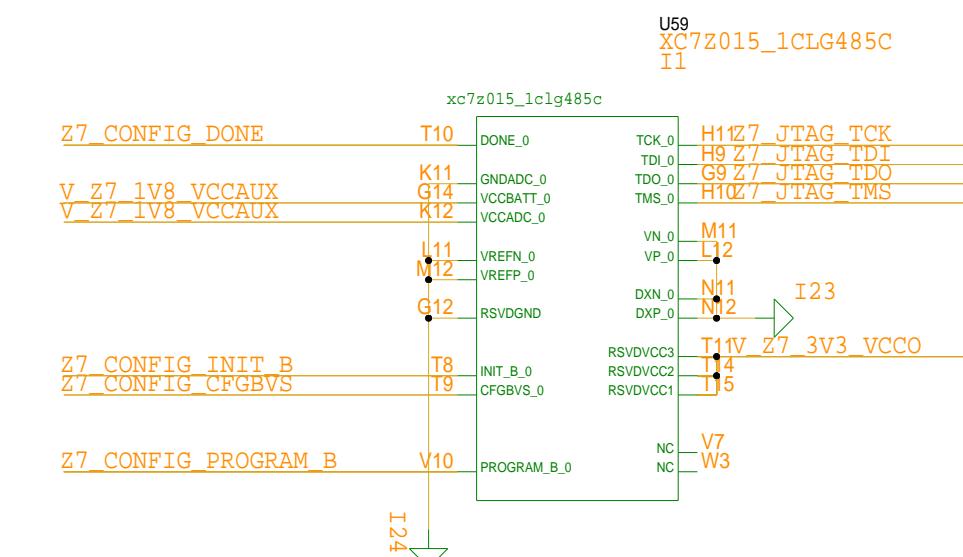


BUTTON FOR RECONFIG

Z7_CONFIG_DONE 1 R459 330 2 V_Z7_3V3_VCCO

1 R460 100 2 1 D34 LED 2 I16

LED INDICATE CONFIG DONE



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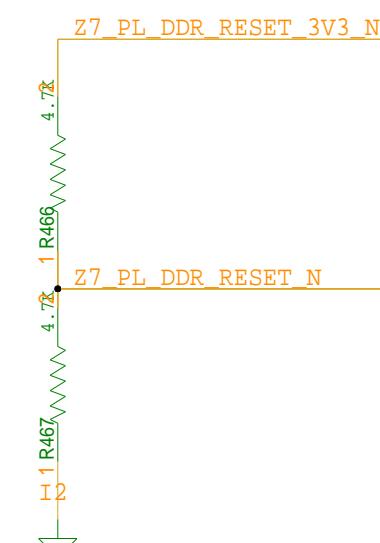
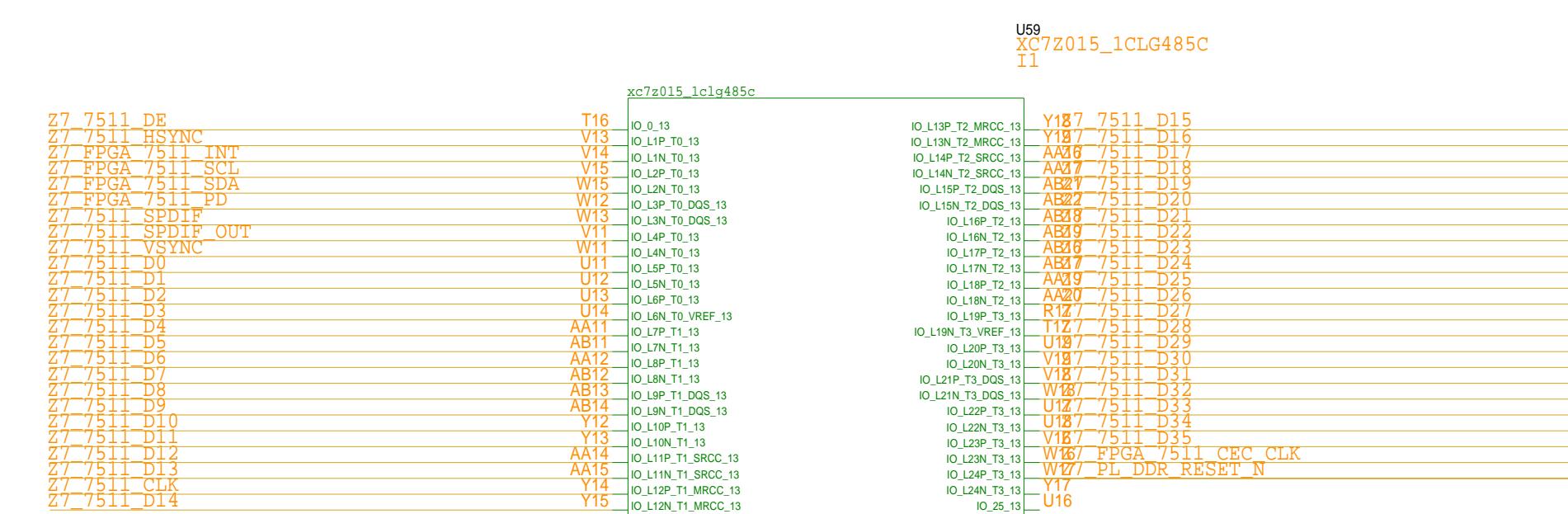
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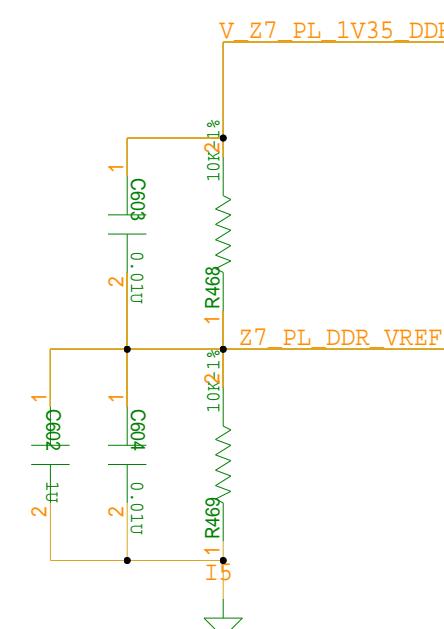
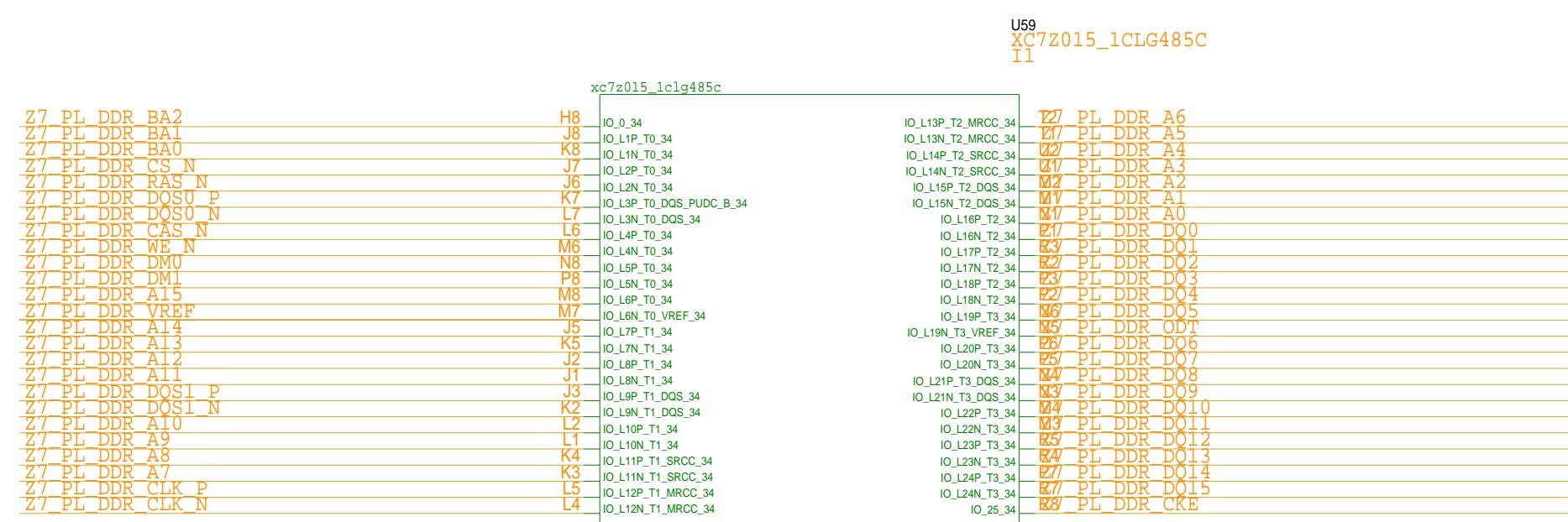
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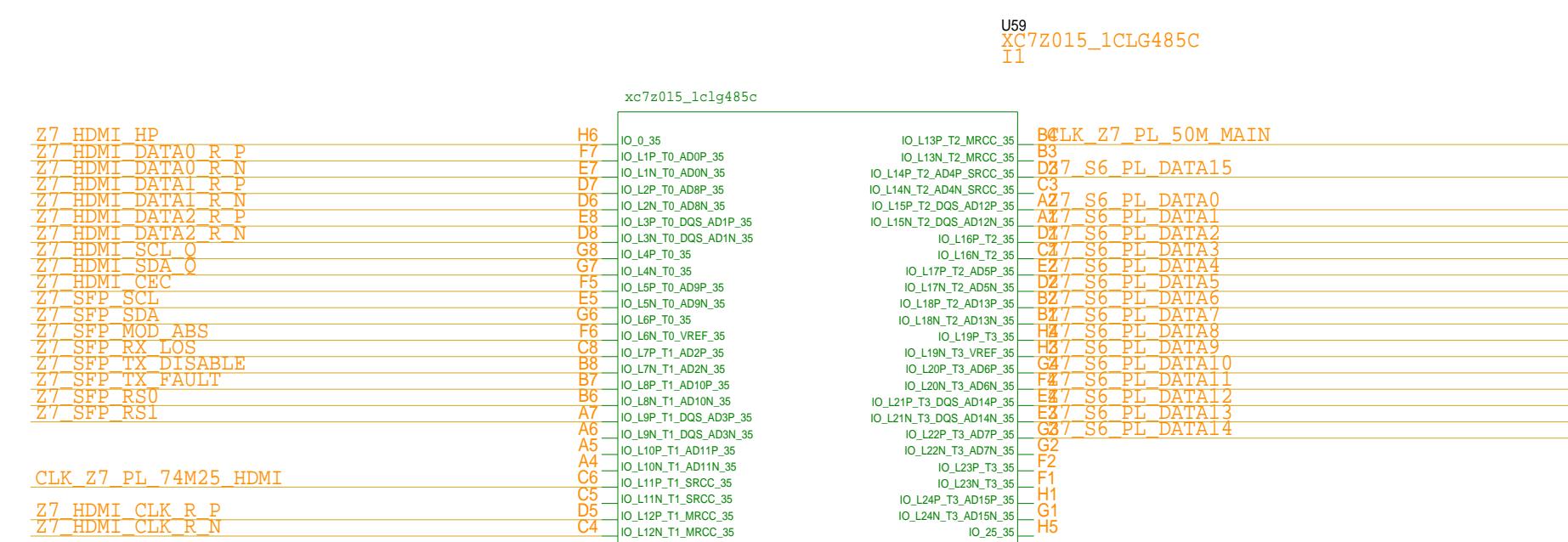
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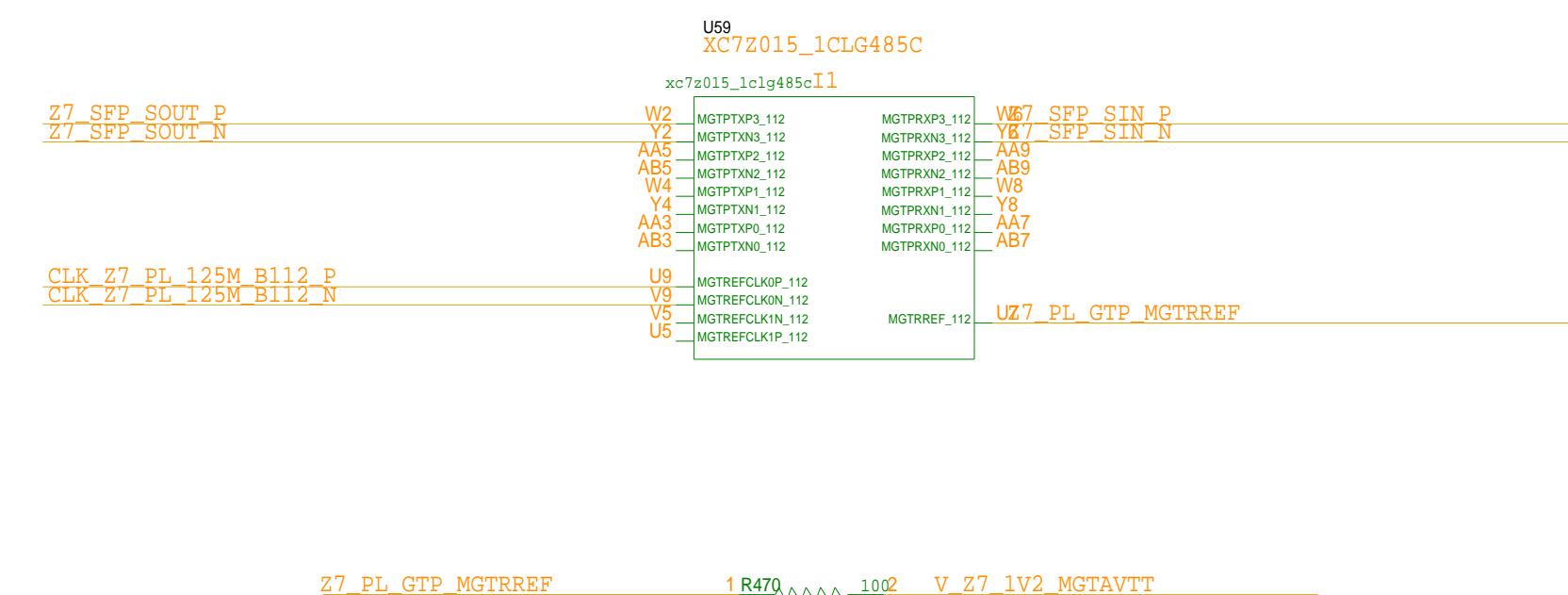
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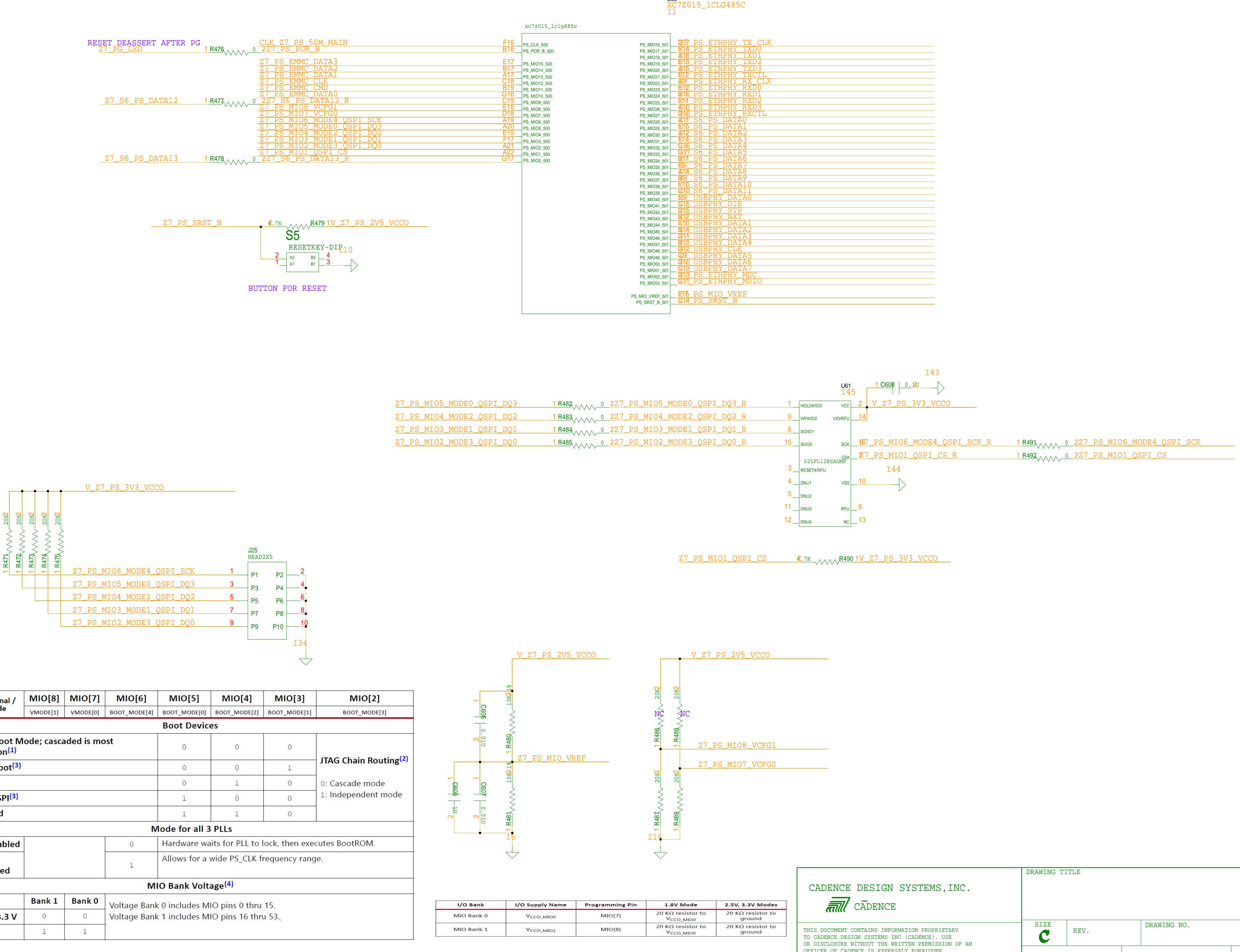
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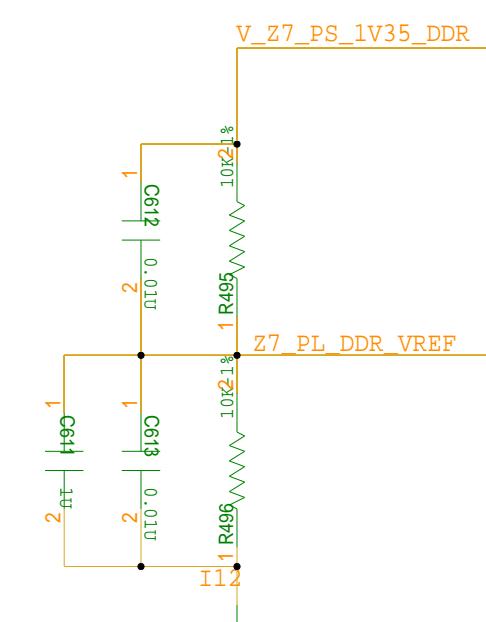
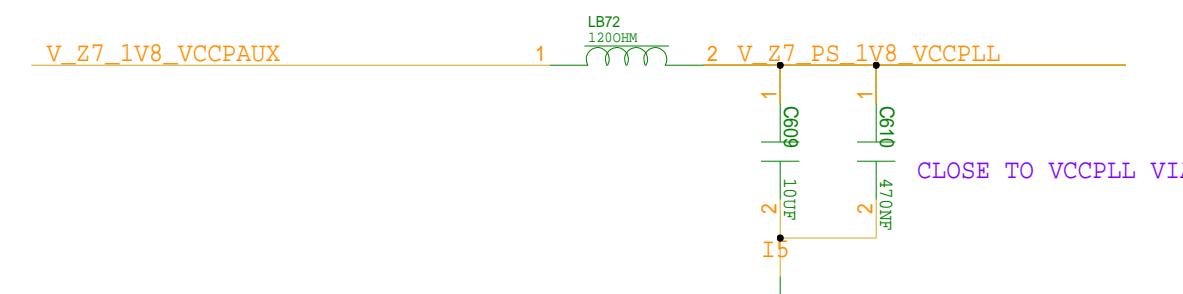
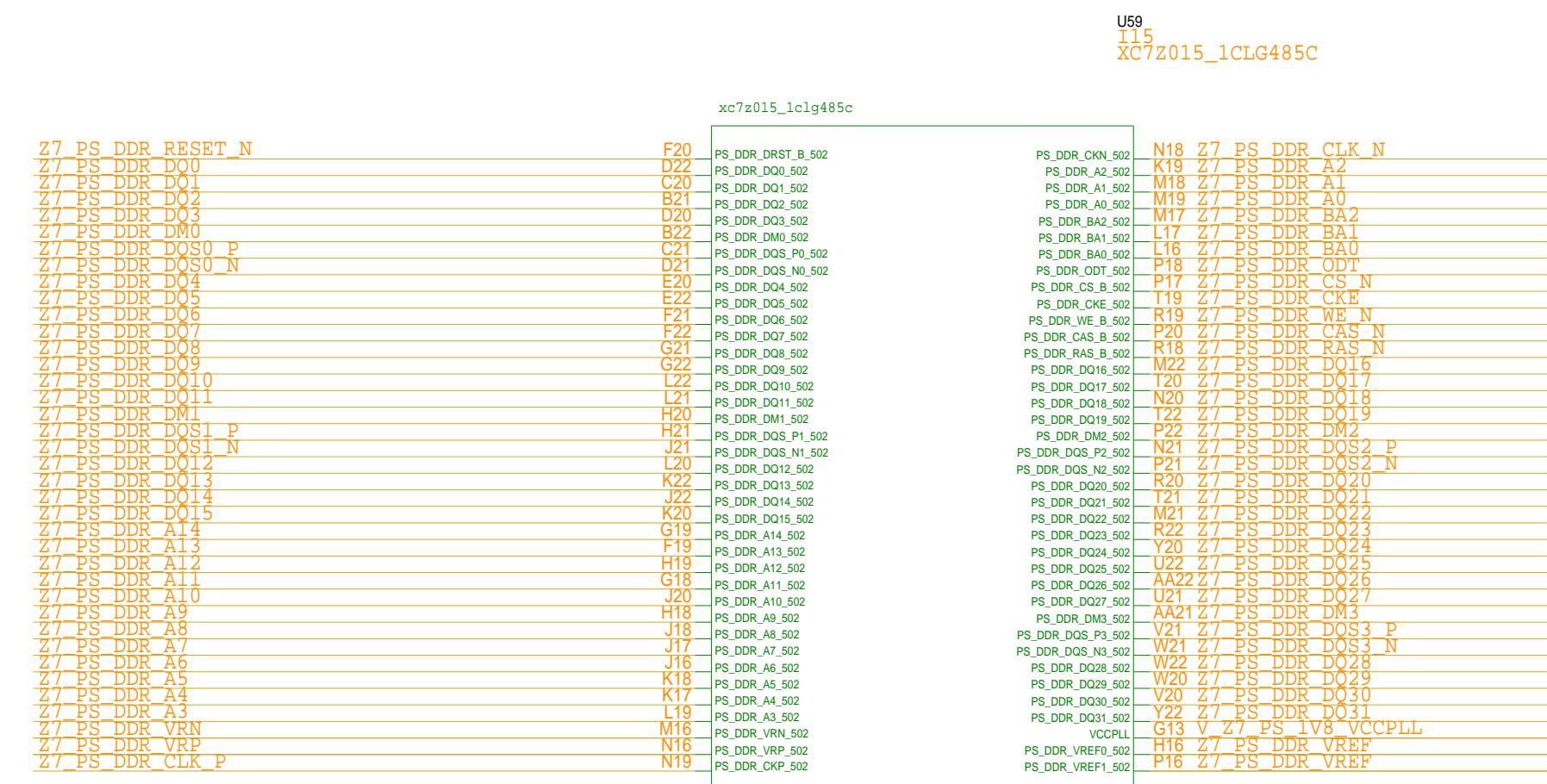
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