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> AR# 53561: Design Advisory for Artix-7 FPGA GTP Transceivers: RX Reset Sequence Requirement for Production Silicon

## AR# 53561

### Design Advisory for Artix-7 FPGA GTP Transceivers: RX Reset Sequence Requirement for Production Silicon

#### Description

This answer record covers the RX reset sequence requirements for the Artix-7 GTP Transceiver Production Silicon.

#### Solution

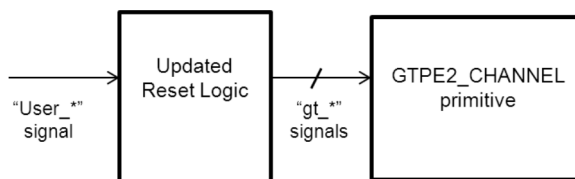
The required sequences to follow for issuing GTRXRESET, RXPMARESET, or RXRATE in the Artix-7 GTP Production Transceivers are documented below. These reset sequences can be also used on General ES silicon but are not required.

These sequences are implemented in the wrapper generated by 7 Series FPGAs Transceivers Wizard v2.5 in the "ISE 14.4.1 Device Pack" or ISE 14.5/Vivado 2013.1 tool version. The reset sequences are added to v1.4 of the *7 Series FPGA GTP Transceiver User Guide* (UG482). Note, special care is needed in simulation. Please see the "Additional Requirements for Simulation" section below.

In these sequences, "user\_\*" denotes user input. This signal was previously connected directly to the GT primitive. It will now trigger an alternative reset sequence as described below.

"gt\_\*" denotes connection to GT primitive. The following diagram indicates where this new sequence fits in.

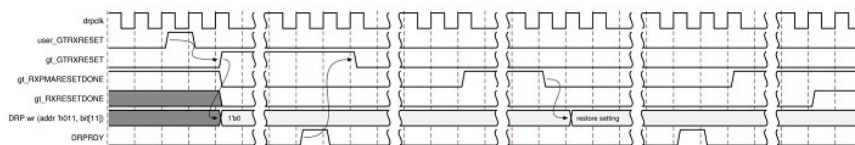
"DRP wr" denotes the function of performing a DRP write to address 9'h011. The exact DRP transaction is not shown.



#### 1) GTRXRESET:

The following reset sequence must be followed when the user wants to perform GTRXRESET.

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### Steps:

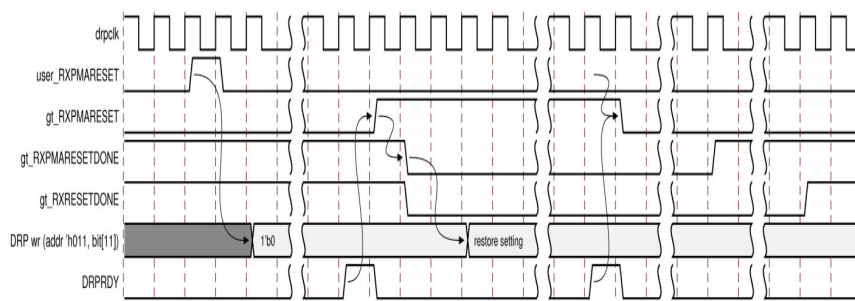
1. User triggers a reset request by asserting `user_GTRXRESET`.
2. Set and hold `gt_GTRXRESET` High. This will cause `gt_RXPMARESETDONE` to go Low.
3. Issue DRP write to the `GTPE2_CHANNEL` primitive, DRP address `9'h011`, and set bit[11] to `1'b0`.
4. In order to ensure only bit[11] of DRP address `9'h011` is modified, it is best to perform a read-modify-write function.
5. Upon DRP write completion and `user_GTRXRESET` detected as Low, set and hold `gt_GTRXRESET` Low. If `user_GTRXRESET` remains asserted upon completion of the DRP write, continue to assert `gt_GTRXRESET` until `user_GTRXRESET` is Low.
6. Wait for falling edge of `gt_RXPMARESETDONE`.
7. Issue DRP write to the `GTPE2_CHANNEL` primitive, DRP address `9'h011`, restoring the original setting for bit[11]. The completion of this DRP write must occur before `gt_RXPMARESETDONE` switches from Low to High. `gt_RXPMARESETDONE` will stay Low for a minimum of 0.66 us.

### Notes:

1. Make sure `gt_GTRXRESET` is output of a register.
2. Make sure `RXPMARESET_TIME` is set to `5'h3`. This should be the default setting.
3. The sequence above will only simulate properly if `SIM_GTRESET_SPEEDUP` is set to `FALSE`. If `SIM_GTRESET_SPEEDUP` is set to `TRUE`, the above sequence must be bypassed.

## 2) RXPMARESET:

The following reset sequence must be followed when the user wants to perform `RXPMARESET`.



### Steps:

1. User triggers a `RXPMARESET` request by asserting `user_RXPMARESET`.
2. Issue DRP write to the `GTPE2_CHANNEL` primitive, `DRPADDR`

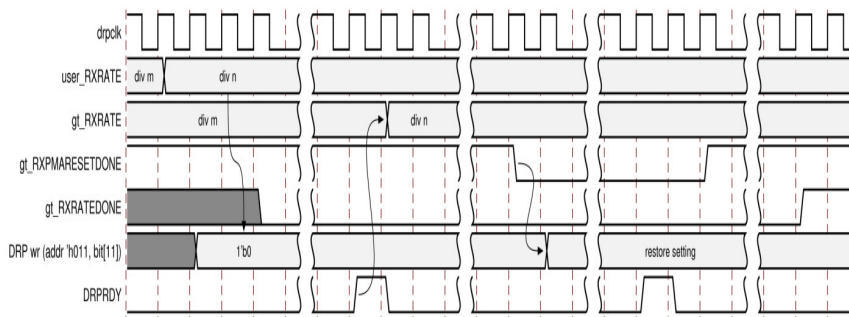
9h011, and set bit[11] to 1b0.

3. In order to ensure only bit[11] of DRPADDR 9h011 is modified, it is best to perform a read-modify-write function.
4. Upon DRP write completion, set and hold gt\_RXPMARESET High.
5. Wait for RXPMARESETDONE to go Low.
6. Issue DRP write to the GTPE2\_CHANNEL primitive, DRPADDR 9h011, restoring the original setting for bit[11].
7. Upon DRP write completion and user\_RXPMARESET detected as Low, set and hold gt\_RXPMARESET Low. If user\_RXPMARESET remains asserted upon completion of the DRP write, continue to assert gt\_RXPMARESET until user\_RXPMARESET is Low.

**Note:** Make sure gt\_RXPMARESET is output of a register.

### 3) RXRATE:

The following sequence must be followed when the user wants to trigger RX rate change via RXRATE.



#### Steps:

1. User triggers a RX rate change request by changing user\_RXRATE.
2. Issue DRP write to the GTPE2\_CHANNEL primitive, DRPADDR 9h011, set bit[11] to 1b0.
3. In order to ensure only bit[11] of DRPADDR 9h011 is modified, it is best to perform a read-modify-write function.
4. Upon DRP write completion, set gt\_RXRATE to the value of user\_RXRATE.
5. Wait for RXPMARESETDONE to go Low
6. Issue DRP write to the GTPE2\_CHANNEL primitive, DRPADDR 9h011, restoring the original setting for bit[11]. The completion of this DRP write must occur before RXPMARESETDONE switches from Low to High. RXPMARESETDONE will stay Low for a minimum of 0.66 us.

**Note:** The sequence above will only simulate properly if SIM\_GTRESET\_SPEEDUP is set to FALSE. If SIM\_GTRESET\_SPEEDUP is set to TRUE, the above sequence must be bypassed. See the "Additional Requirements for Simulation" below.

#### GTP Attribute:

In addition to the required sequences above, the following attribute must be set correctly:

PMA\_RSV2 = 32h'00002040.

### Additional Requirements for Simulation

While these sequences are implemented in the wrapper generated by the 7 Series FPGAs Transceivers Wizard for proper hardware operation, users might see in simulation that the RXOUTCLK, RXUSRCLK, and RXUSRCLK2 run at the incorrect clock rates.

For example, the clock rates are the GT rate divided by 16 instead of the correct divide rate of 20 for a configuration with 8b10b decoder enabled and an internal data width of 20.

To work around/bypass this behavior in simulation and generate the correct clock rates, step through the following:

1. Set the DRP address (drpaddr\_o) within the core\_name\_gtxreset\_seq.v/.vhd to 2C. This DRP address is set to 11 by default which is the appropriate setting for hardware. A setting of 2C can be used as a work-around for simulation. For Verilog, see lines 251 and 324 in core\_name\_gtxreset\_seq.v. For VHDL, see line 244 in core\_name\_gtxreset\_seq.vhd. Note: this needs to be defined for simulation only and not for hardware operation. For example, in Verilog define the 2C address within an `ifdef SIMULATION.
2. Ensure that the EXAMPLE\_SIM\_GTRESET\_SPEEDUP parameter is being pulled through the rtl hierarchy to the gt\_channel level. This step is required in the GT Wizard example design.
3. Ensure that the EXAMPLE\_SIMULATION parameter is set to 1.

After these changes, the proper clock rates will be seen in simulation within ~20us of reset.

### Revision History

02/14/2017	Added Additional Requirements for Simulation
04/12/2013	Updated the user guide version with the reset sequence
01/31/2013	Initial release

Was this Answer Record helpful?

Yes 

No 

### Linked Answer Records

### Master Answer Records

↑ Answer Number	↑ Answer Title	↑ Version Found	↑
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↓ Answer Number	↓ Answer Title	↓ Version Found	↓ 'N/A'
51456	Design Advisory Master Answer Record for Artix-7 FPGA	N/A	N/A
47852	7 Series FPGAs GTP Transceivers - Known Issues and Answer Record List	N/A	N/A
54473	LogiCORE IP CPRI Core - Release Notes and Known Issues for Vivado 2013.1 and newer tool versions	N/A	N/A

#### Associated Answer Records

↓ Answer Number	↓ Answer Title	↓ Version Found	↓ 'N/A'
54232	7 Series Integrated Block Wrapper for PCI Express v1.8 (ISE 14.4/2012.4) - How to generate the core for Artix-7 Production Silicon	N/A	N/A
55445	RXAUI v2.4, 7 Series - Required GTP/GTX and GTH transceiver updates	N/A	N/A
55446	XAUI v10.4 - 7 Series - Required GTP/GTX and GTH transceiver updates	N/A	N/A

↓ Answer Number	↓ Answer Title	↓ Version Found	↓ '
62770	Design Advisory for 7-Series Integrated Block for PCI Express / AXI Bridge for PCI Express (Vivado 2013.3 - Vivado 2014.3) - Link training issue with GTP devices	N/A	N/
54249	IP Release Notes and Known Issues for LogiCORE RXAUI for Vivado 2013.1 and newer tool versions	N/A	N/

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