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REVISIONS

ZONE	LTR	DESCRIPTION	DATE	APPR.

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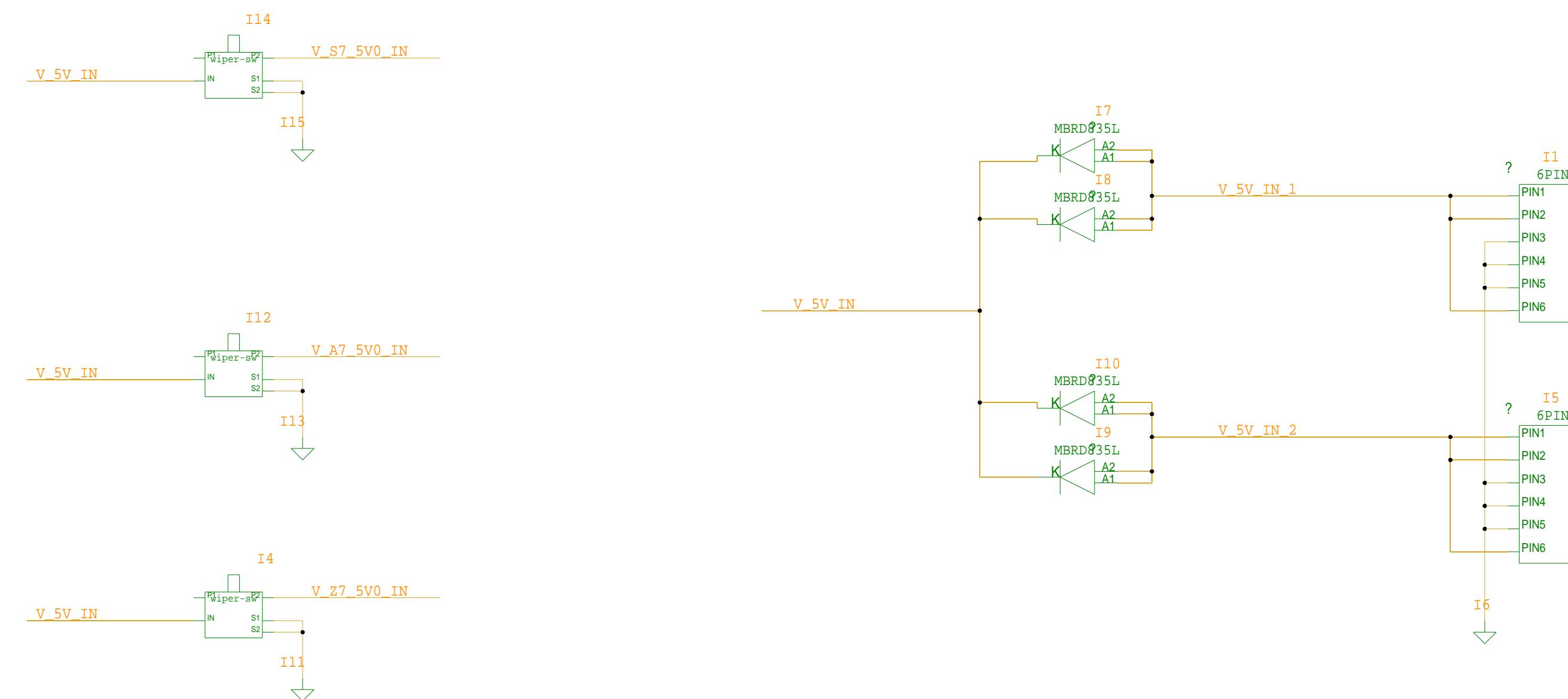
2

1

MAIN POWER

REVISIONS

ZONE	LTR	DESCRIPTION	DATE	APPR.



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SPARTAN-7 INDEX

REVISIONS				
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HDMI RECEVIER	PAGE 6-8
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SFP PHY	PAGE 12-13
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SPARTAN-7 POWER (1)

$$V_{OUT} = V_{REF} \times (1 + (R_{TOP}/R_{BOT}))$$

$$R_{RT} (\text{k}\Omega) = [14,822/f_{SW} (\text{kHz})]^{1.081}$$

$$V_{IN_STARTUP} = (0.8 \text{ nA} + (0.8 \text{ V}/R_{BOT_EN})) \times \left(R_{TOP_EN} + \frac{R_{BOT_EN} \times 1 \text{ M}\Omega}{R_{BOT_EN} + 1 \text{ M}\Omega} \right)$$

where:

R_{TOP_EN} is the resistor from V_{IN} to EN.

R_{BOT_EN} is the resistor from EN to ground.

Table 9. Soft Start Time Set by the SS12 and SS34 Pins

R_{TOP} ($\text{k}\Omega$)	R_{BOT} ($\text{k}\Omega$)	Soft Start Time			
		Channel 1	Channel 2	Channel 3	Channel 4
0	N/A ¹	2 ms	2 ms	2 ms	2 ms
100	600	2 ms	Parallel	2 ms	4 ms
200	500	2 ms	8 ms	2 ms	8 ms
300	400	4 ms	2 ms	4 ms	2 ms
400	300	4 ms	4 ms	4 ms	4 ms
500	200	8 ms	2 ms	4 ms	8 ms
600	100	8 ms	Parallel	8 ms	2 ms
N/A ¹	0	8 ms	8 ms	8 ms	8 ms

Table 16. Factory Default Options

Option	Default Value
Channel 1 Output Voltage	0.8V adjustable output
Channel 2 Output Voltage	0.8V adjustable output
Channel 3 Output Voltage	0.8V adjustable output
Channel 4 Output Voltage	0.8V adjustable output
PWRGD Pin (Pin 20) Output	Monitor Channel 1 output
Output Discharge Function	Enabled for all four buck regulators
Switching Frequency on Channel 1	1 x switching frequency set by the RT pin
Switching Frequency on Channel 3	1 x switching frequency set by the RT pin
SYNC/MODE Pin (Pin 43) Function	Forced PWM/automatic PWM/PSM mode setting with the ability to synchronize to an external clock
Hiccup Protection	Enabled for overcurrent events
Short-Circuit Latch-Off Function	Disabled for output short-circuit events
Oversupply Latch-Off Function	Disabled for output oversupply events
Reset Timeout Period	200 ms
Watchdog Timeout Period	1.6 sec
Manual Reset Input Mode	Processor manual reset mode

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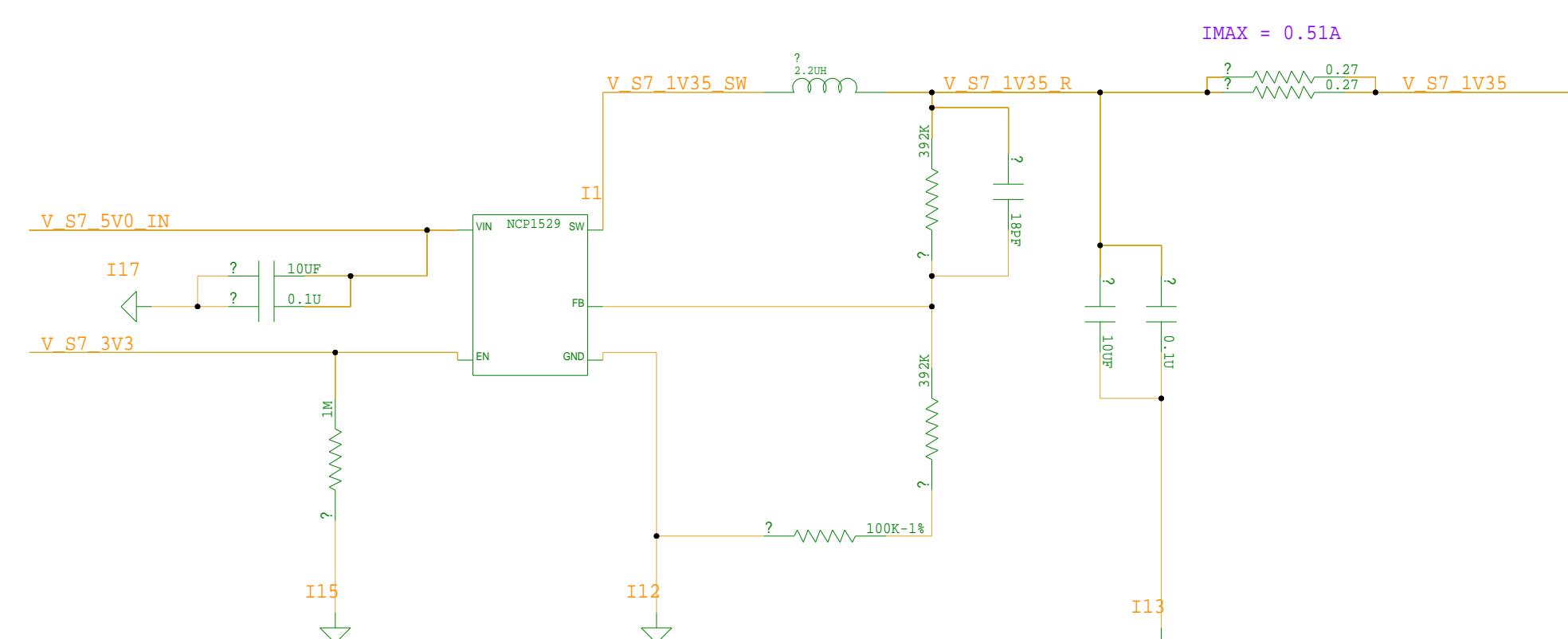
SPARTAN-7 POWER (2)

REVOLUTIONS		DESCRIPTION		DATE	APPR.
ZONE	LTR				

$$V_{out} = V_{FB} \times (1 + R1/R2)$$

- V_{OUT} : Output Voltage (V)
- V_{FB} : Feedback Voltage = 0.6 V
- $R1$: Feedback Resistor from V_{OUT} to FB
- $R2$: Feedback Resistor from FB to GND

3



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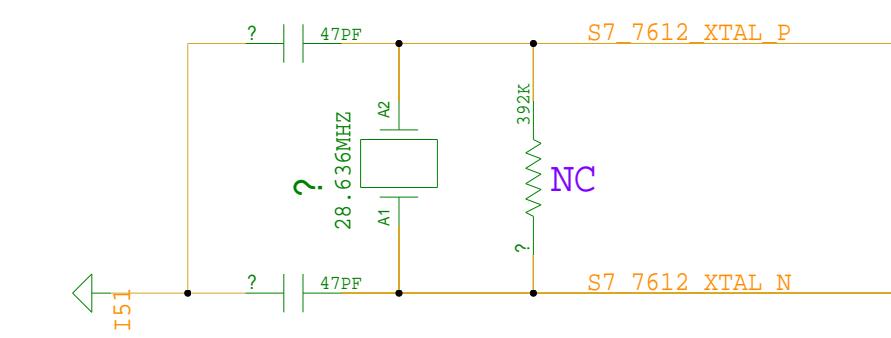
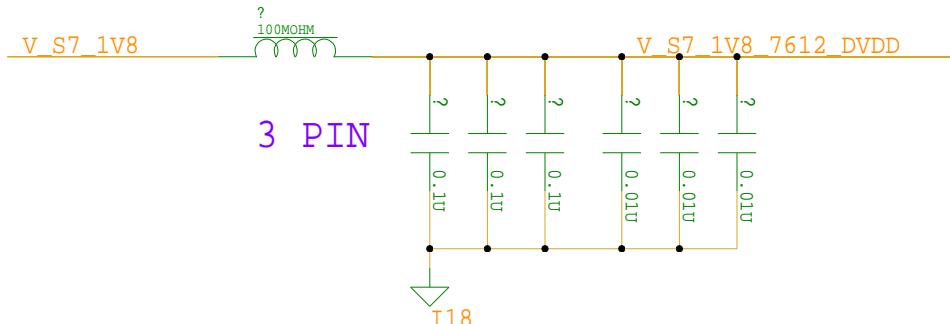
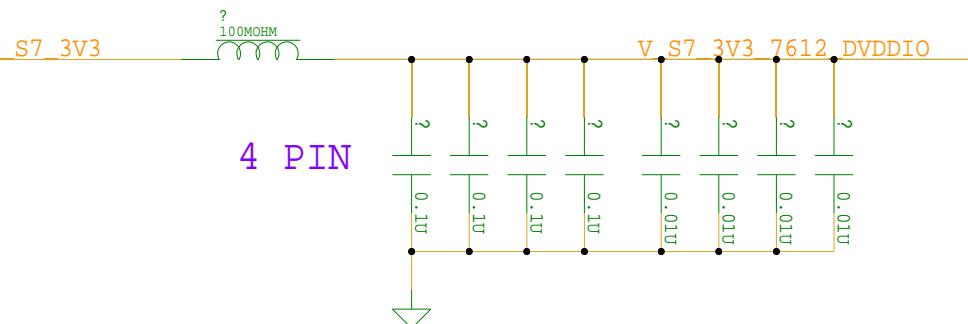
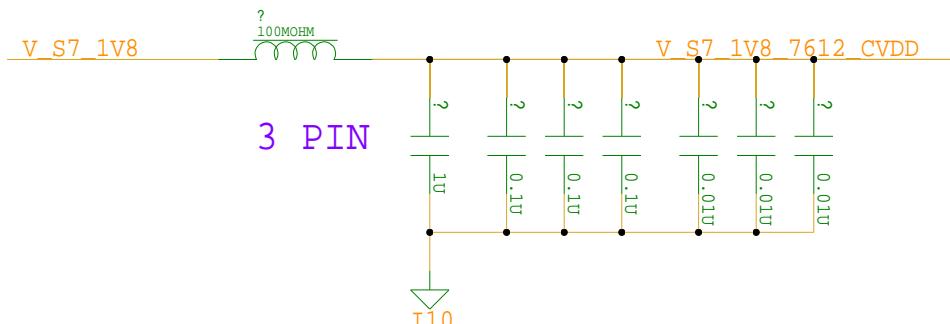
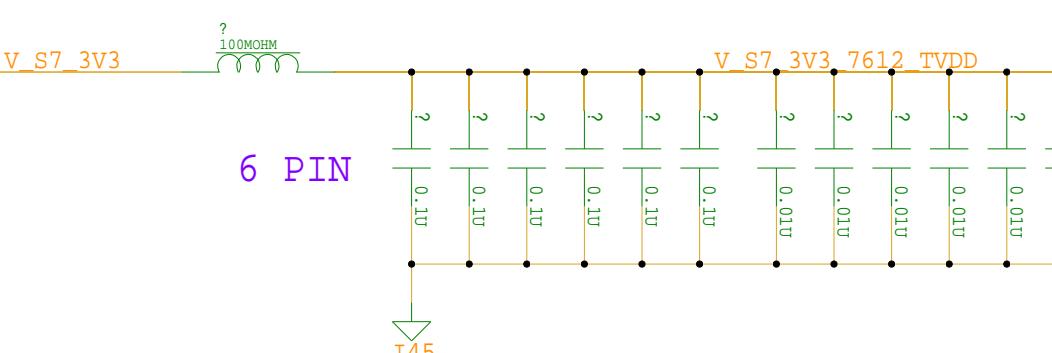
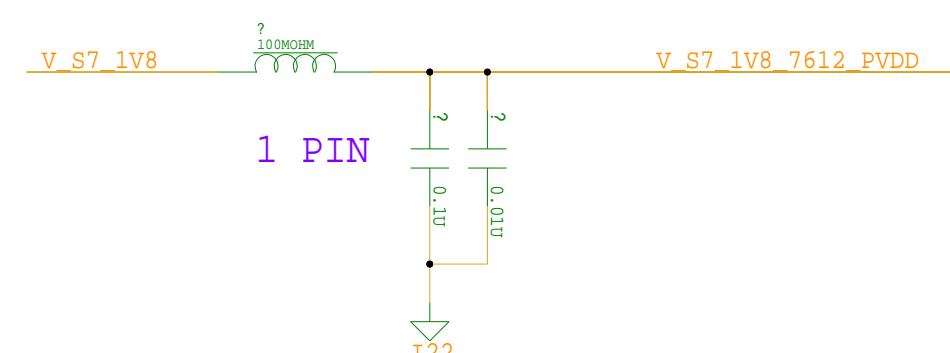
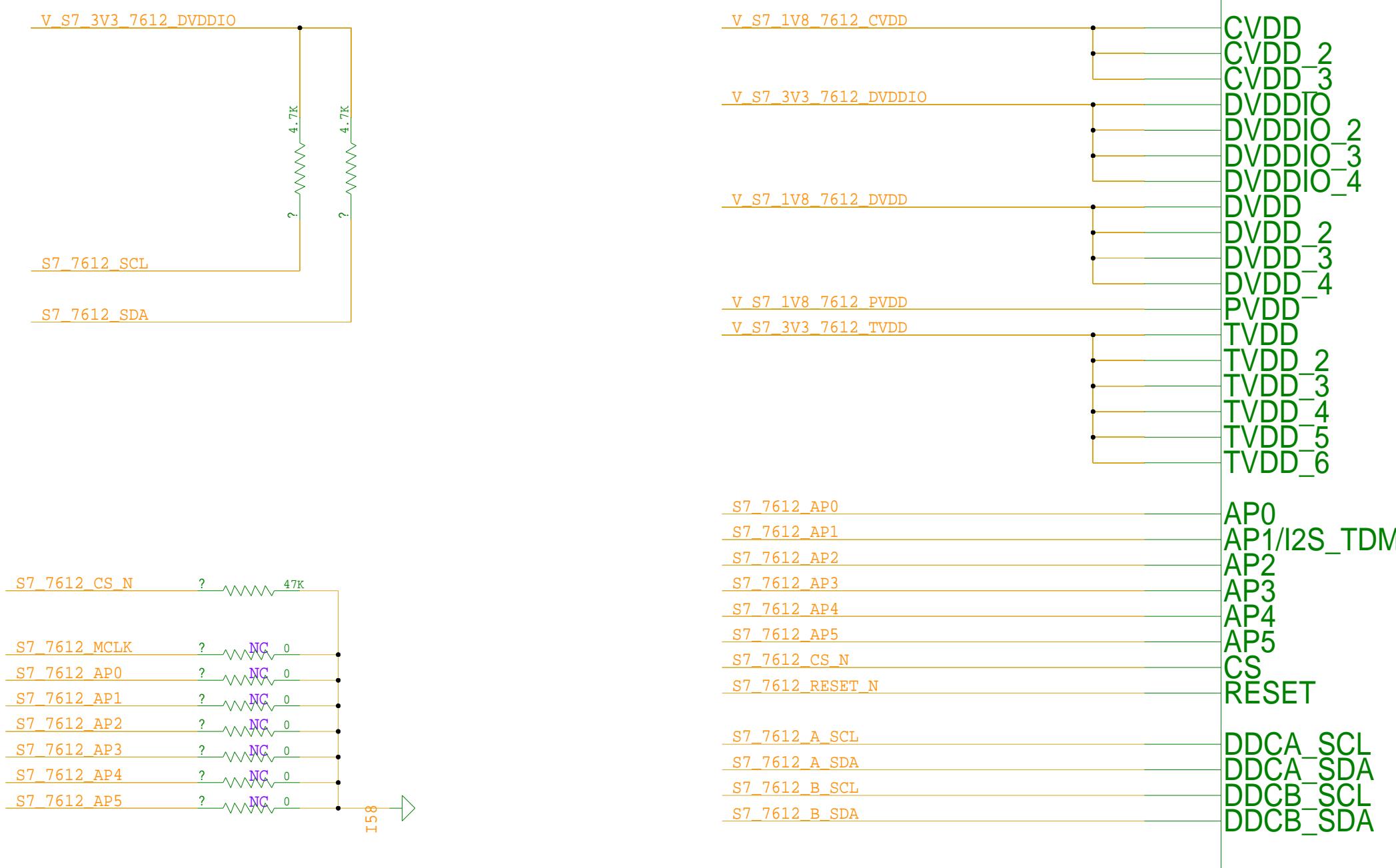
SPARTAN-7 HDMI RECEIVER (1)

REVISIONS

ZONE	LTR	DESCRIPTION	DATE	APPR.

?

DE	S7_7612_DE
XTALP	S7_7612_XTAL_P
XTALN	S7_7612_XTAL_N
SDA	S7_7612_SDA
SCLK/INT2	S7_7612_INT2
SCL	S7_7612_SCL
RXB_5V	V_S7_7612_B_5V0
RXA_5V	V_S7_7612_A_5V0
MCLK/INT2	S7_7612_MCLK
INT1	S7_7612_INT1
HPA_B	S7_7612_B_HP
HPA_A/INT2	S7_7612_A_HP
RXB_C+	S7_7612_B_CLK_P
RXB_C-	S7_7612_B_CLK_N
RXB_2-	S7_7612_B_DATA2_N
RXB_1-	S7_7612_B_DATA1_N
RXB_0-	S7_7612_B_DATA0_N
RXB_2+	S7_7612_B_DATA2_P
RXB_1+	S7_7612_B_DATA1_P
RXB_0+	S7_7612_B_DATA0_P
RXA_C+	S7_7612_A_CLK_P
RXA_C-	S7_7612_A_CLK_N
RXA_2-	S7_7612_A_DATA2_N
RXA_1-	S7_7612_A_DATA1_N
RXA_0-	S7_7612_A_DATA0_N
RXA_2+	S7_7612_A_DATA2_P
RXA_1+	S7_7612_A_DATA1_P
RXA_0+	S7_7612_A_DATA0_P



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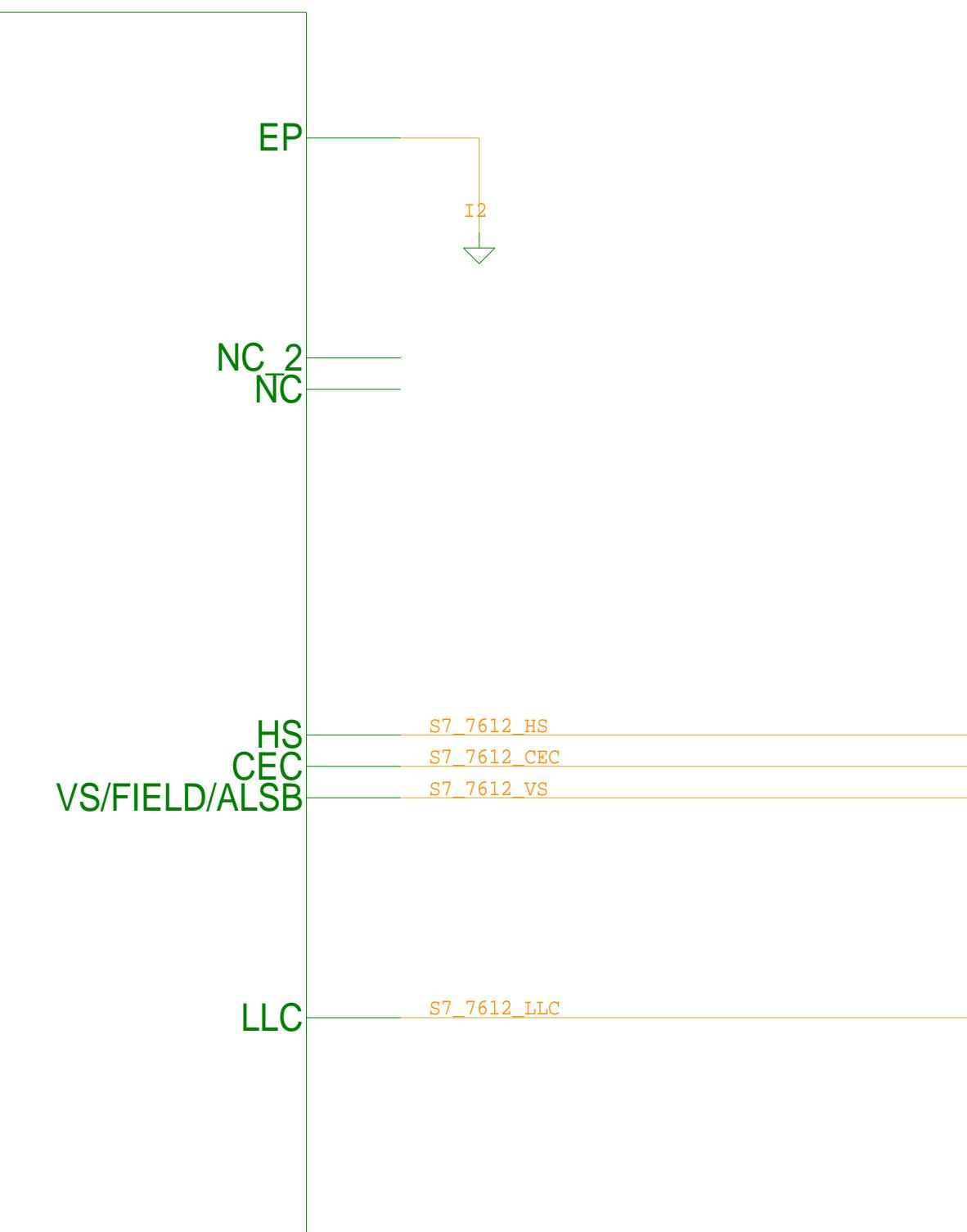
SPARTAN-7 HDMI RECEIVER (2)

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPR.

S7_7612_P0
S7_7612_P1
S7_7612_P2
S7_7612_P3
S7_7612_P4
S7_7612_P5
S7_7612_P6
S7_7612_P7
S7_7612_P8
S7_7612_P9
S7_7612_P10
S7_7612_P11
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S7_7612_P28
S7_7612_P29
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S7_7612_P33
S7_7612_P34
S7_7612_P35

P0
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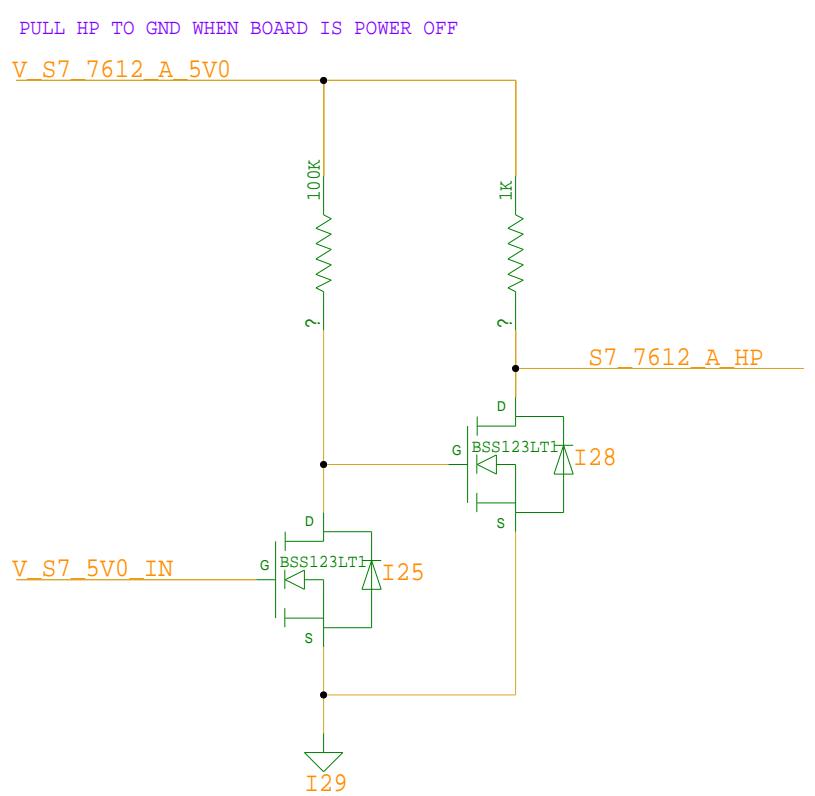
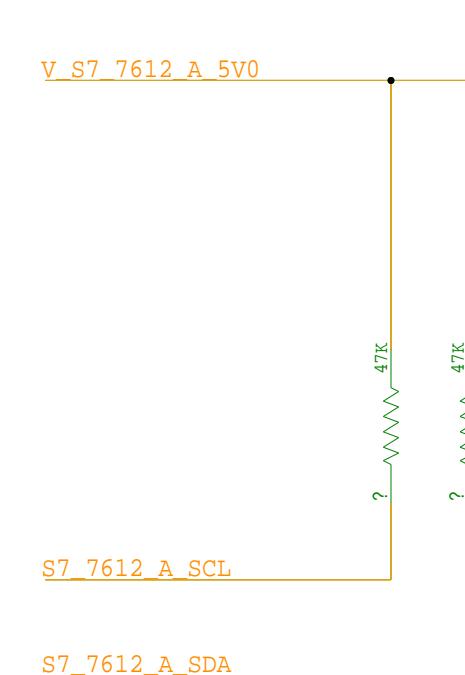
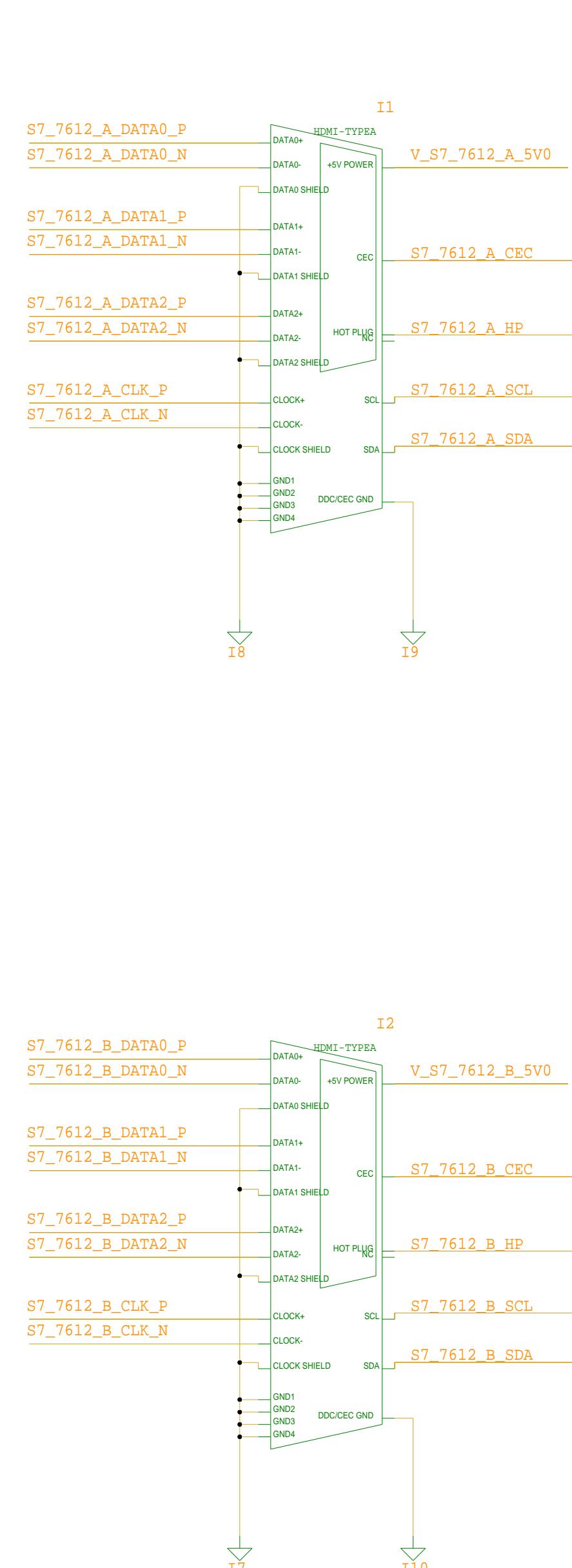
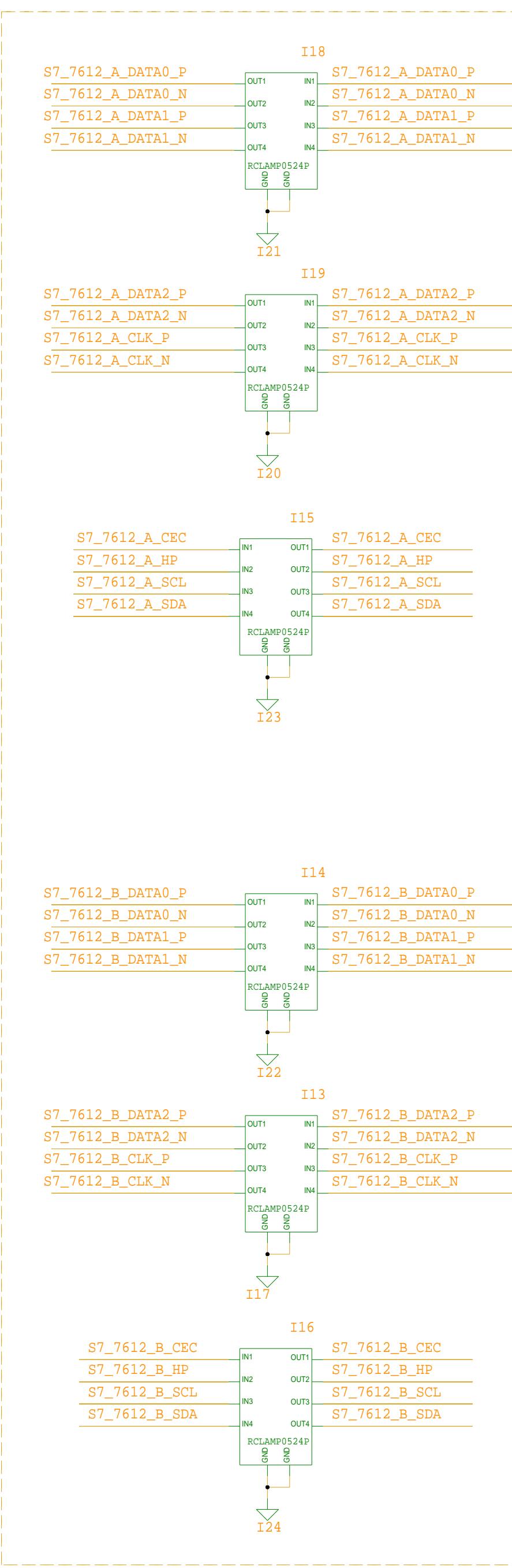
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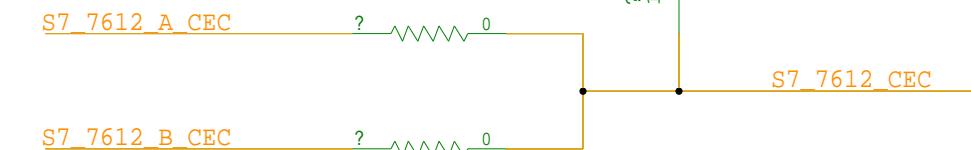
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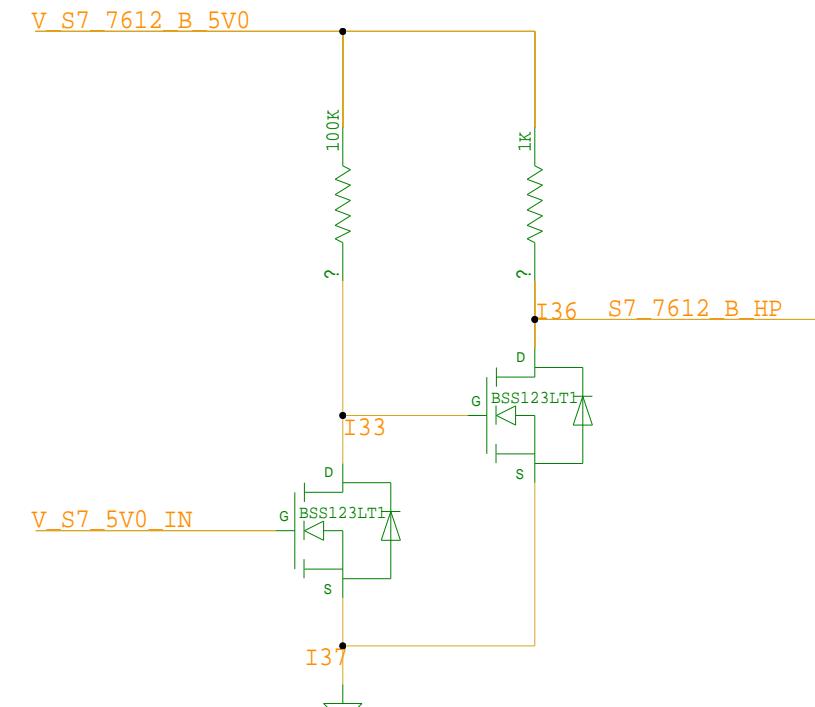
CHANGE CONNECTION DUE TO LAYOUT



V_S7_3V3_7612_DVDDIO



PULL HP TO GND WHEN BOARD IS POWER OFF



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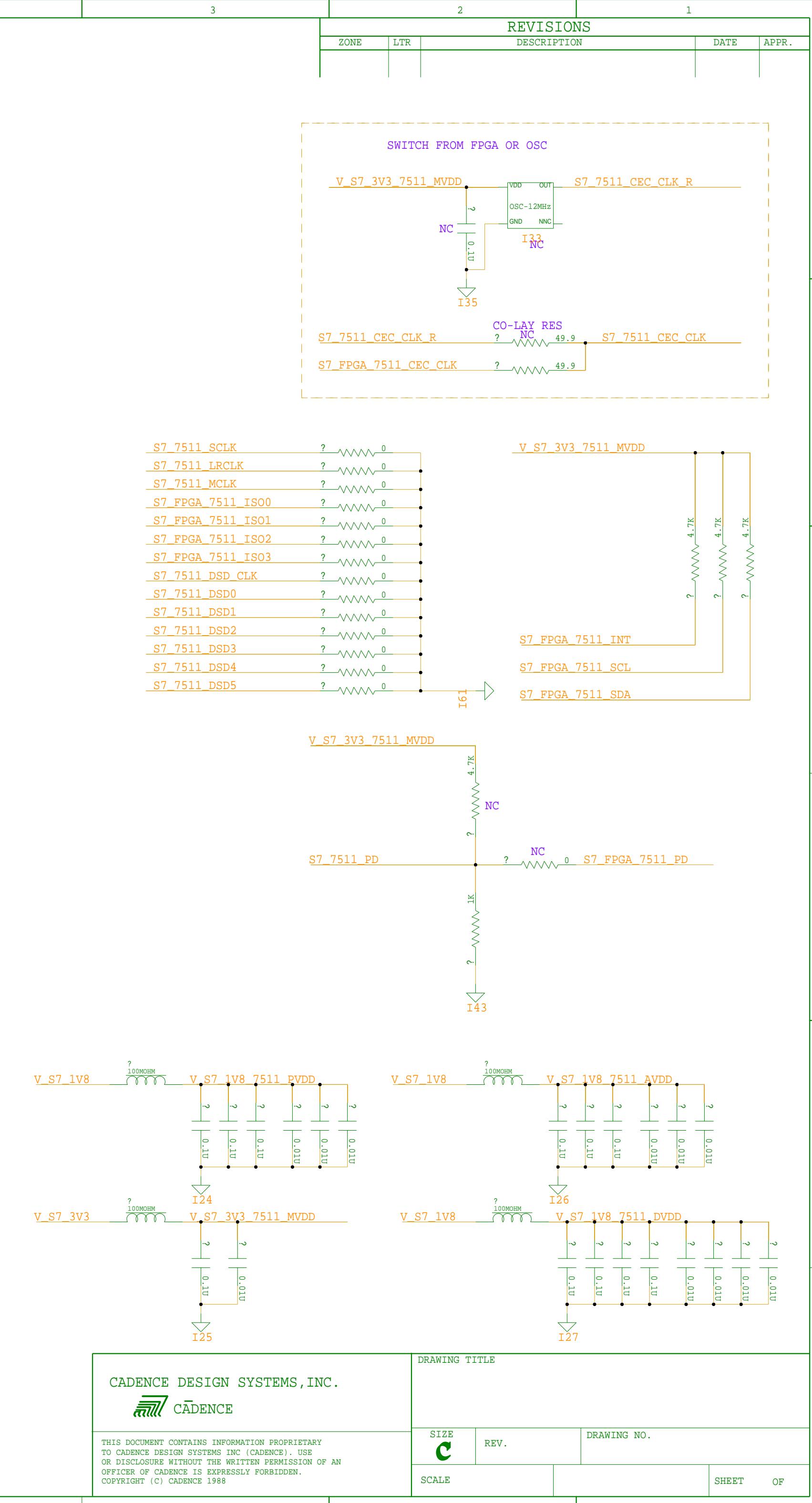
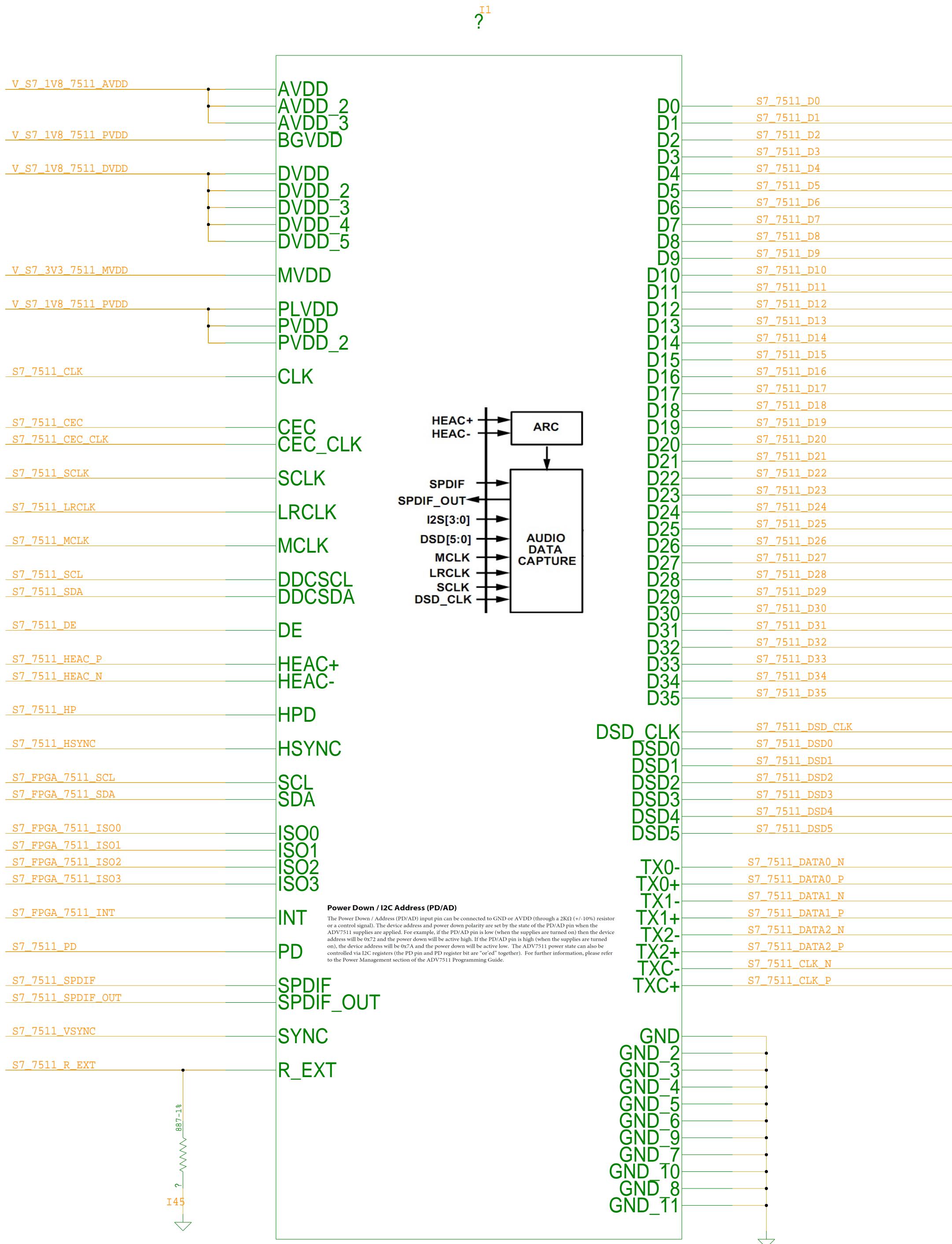
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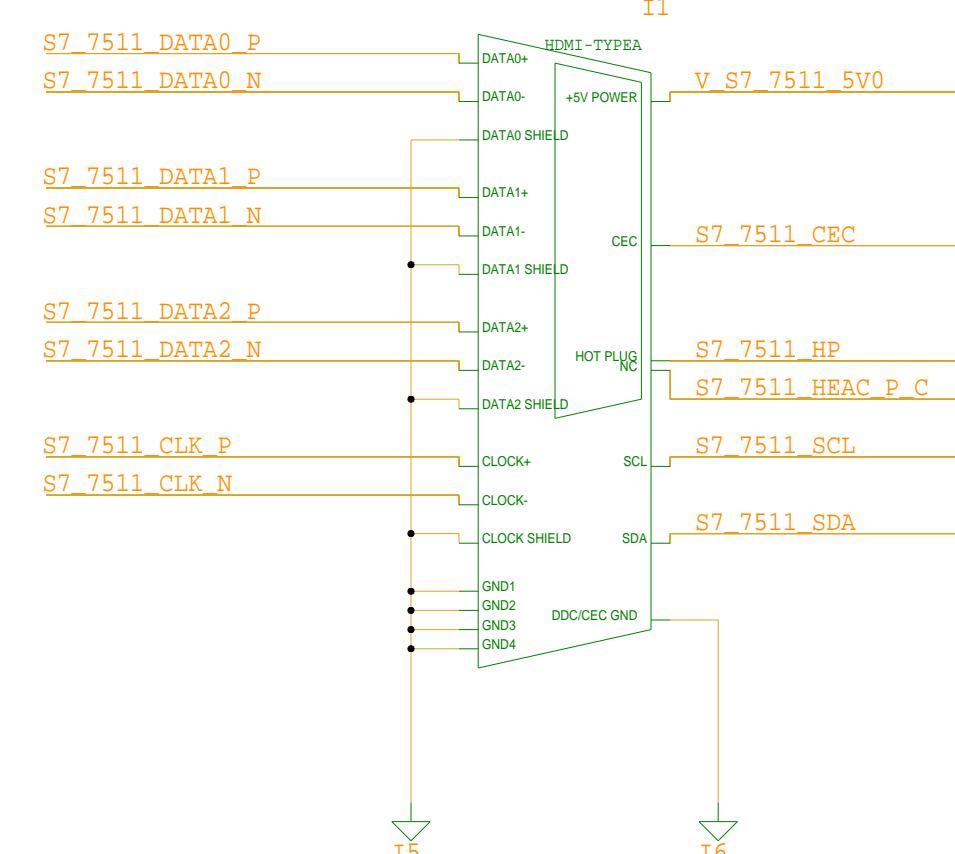
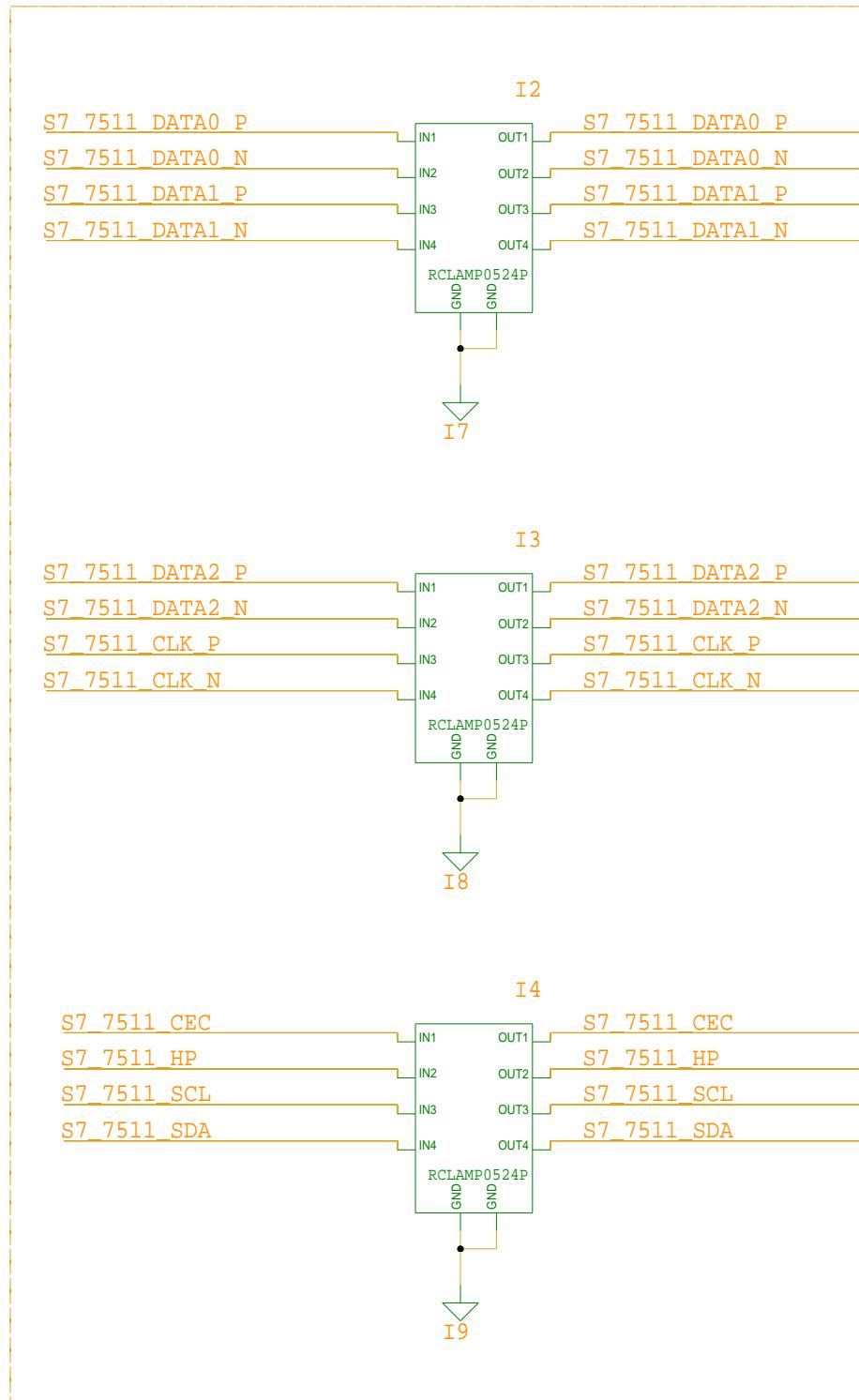


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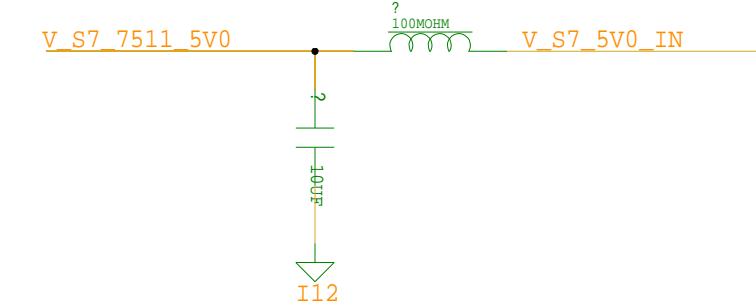
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CHANGE CONNECTION DUE TO LAYOUT

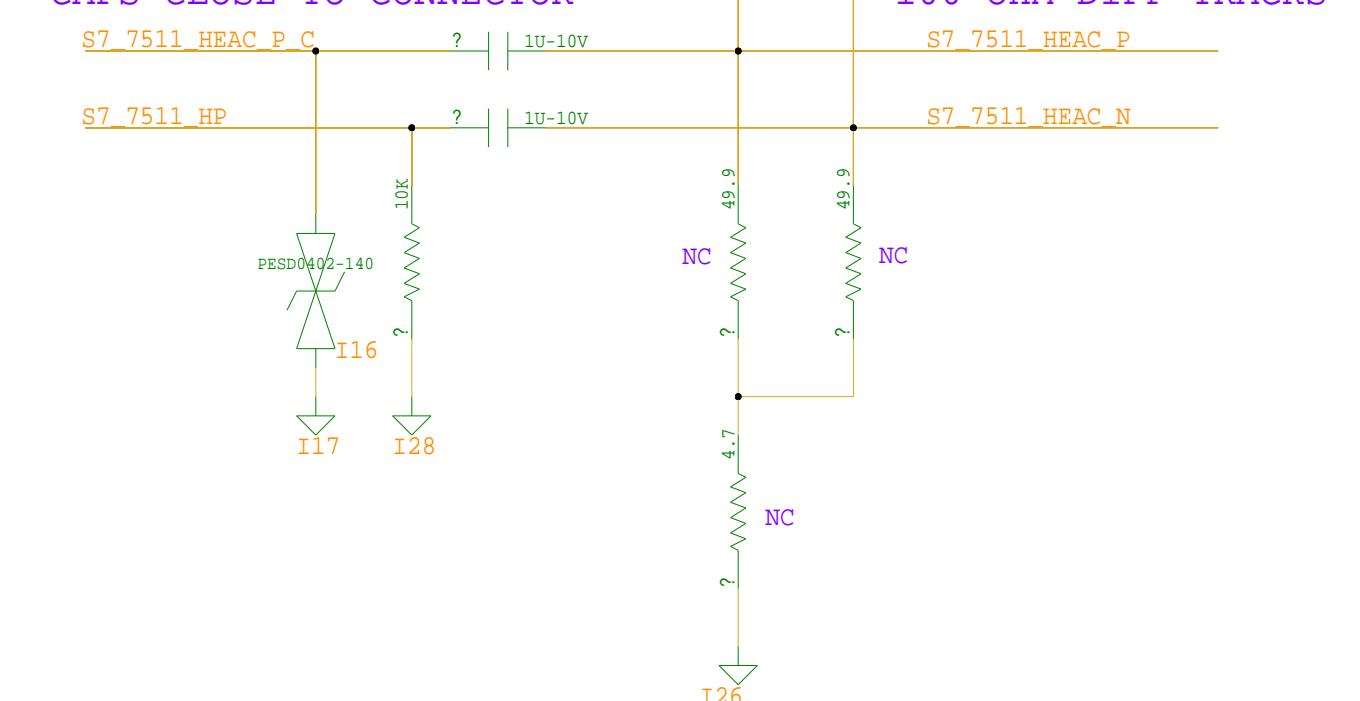


CLOSE TO HDMI CONNECTOR



S7_7511_CEC → 1N4148 → ? → 27.4K V_S7_3V3_7511_MVDD

CAPS CLOSE TO CONNECTOR



S7_7511_SCL → 1.8K-1% → S7_7511_5V0
S7_7511_SDA → 1.8K-1% → S7_7511_5V0

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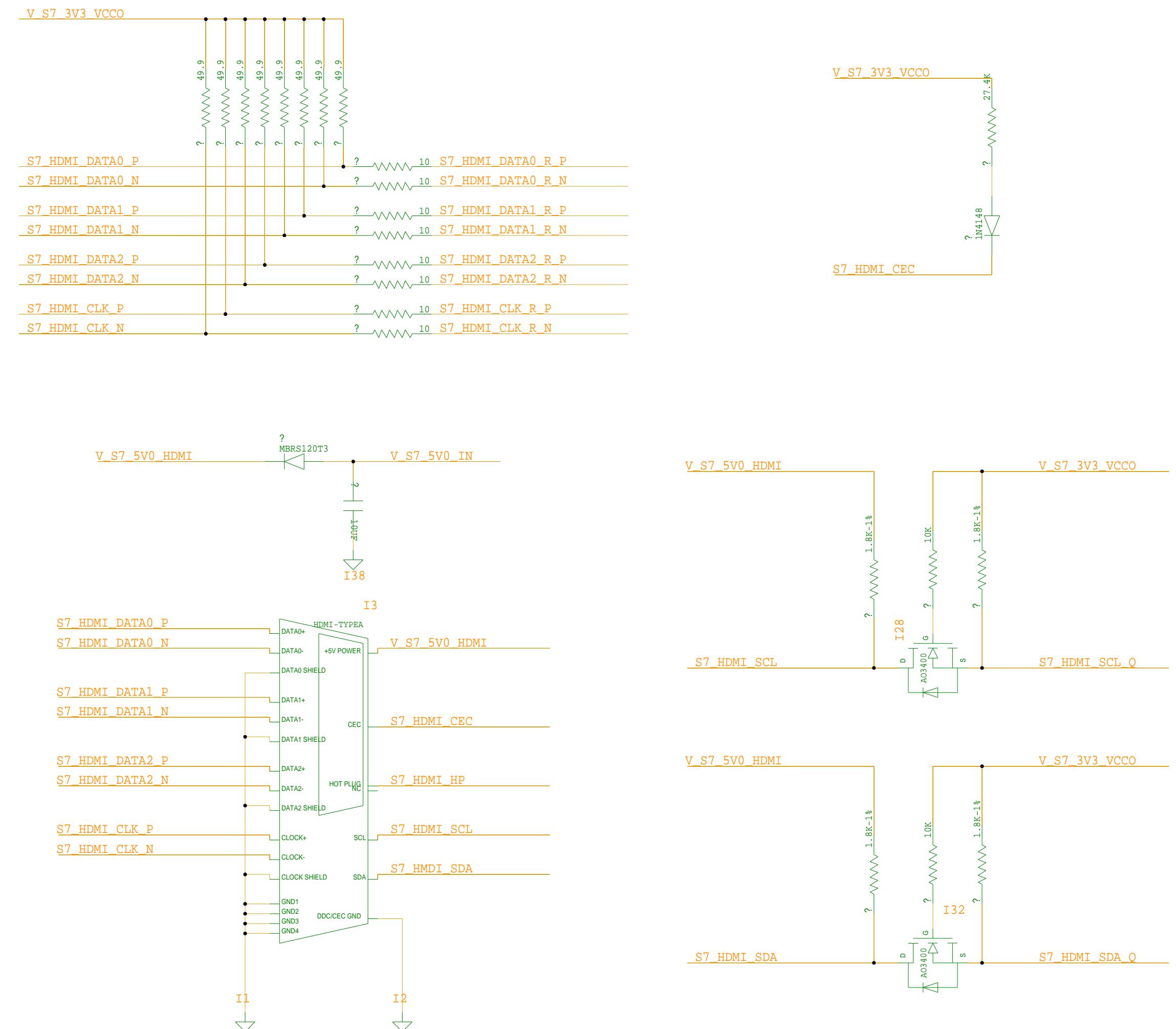
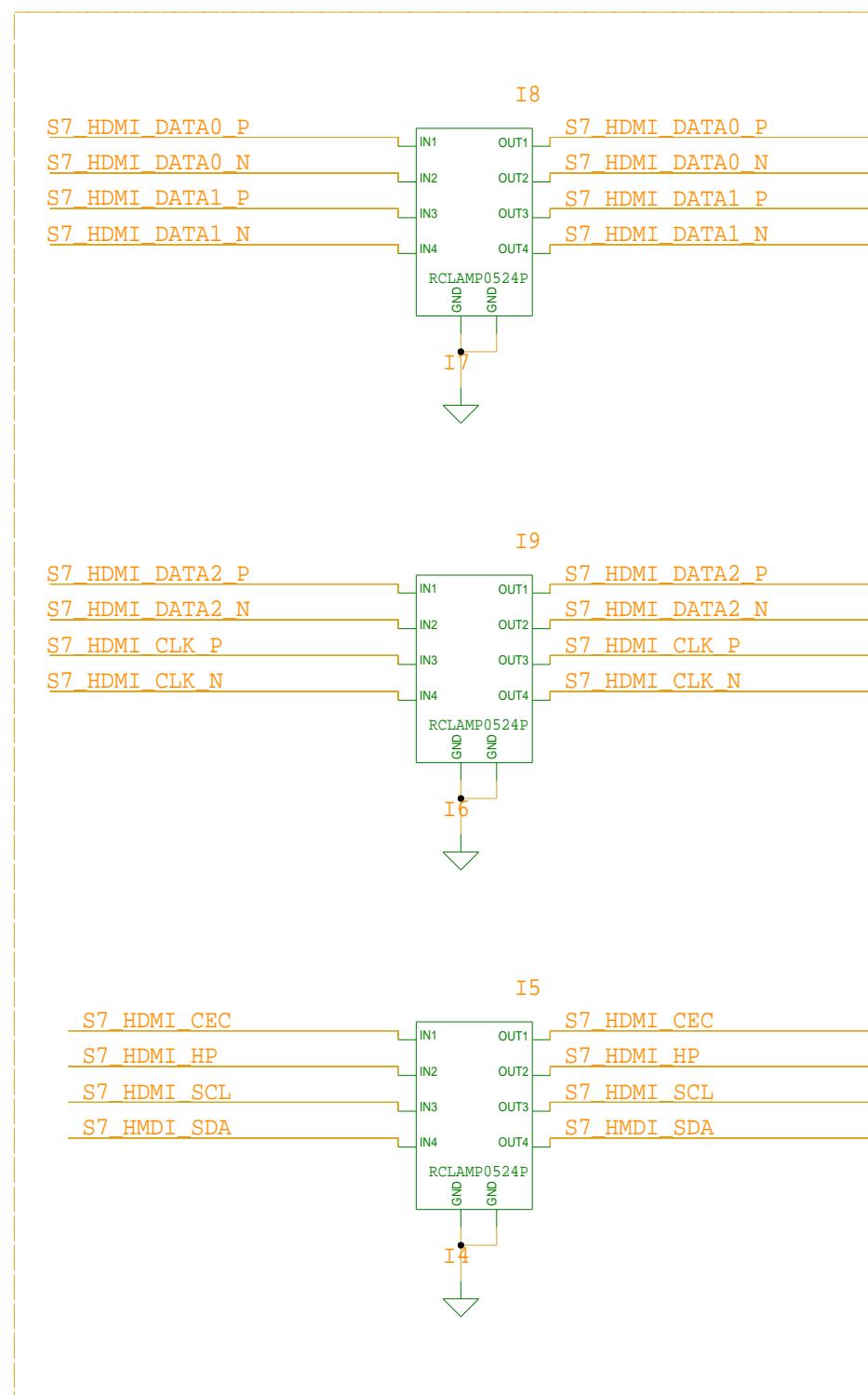
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SPARTAN-7 HDMI INOUT

CHANGE CONNECTION DUE TO LAYOUT



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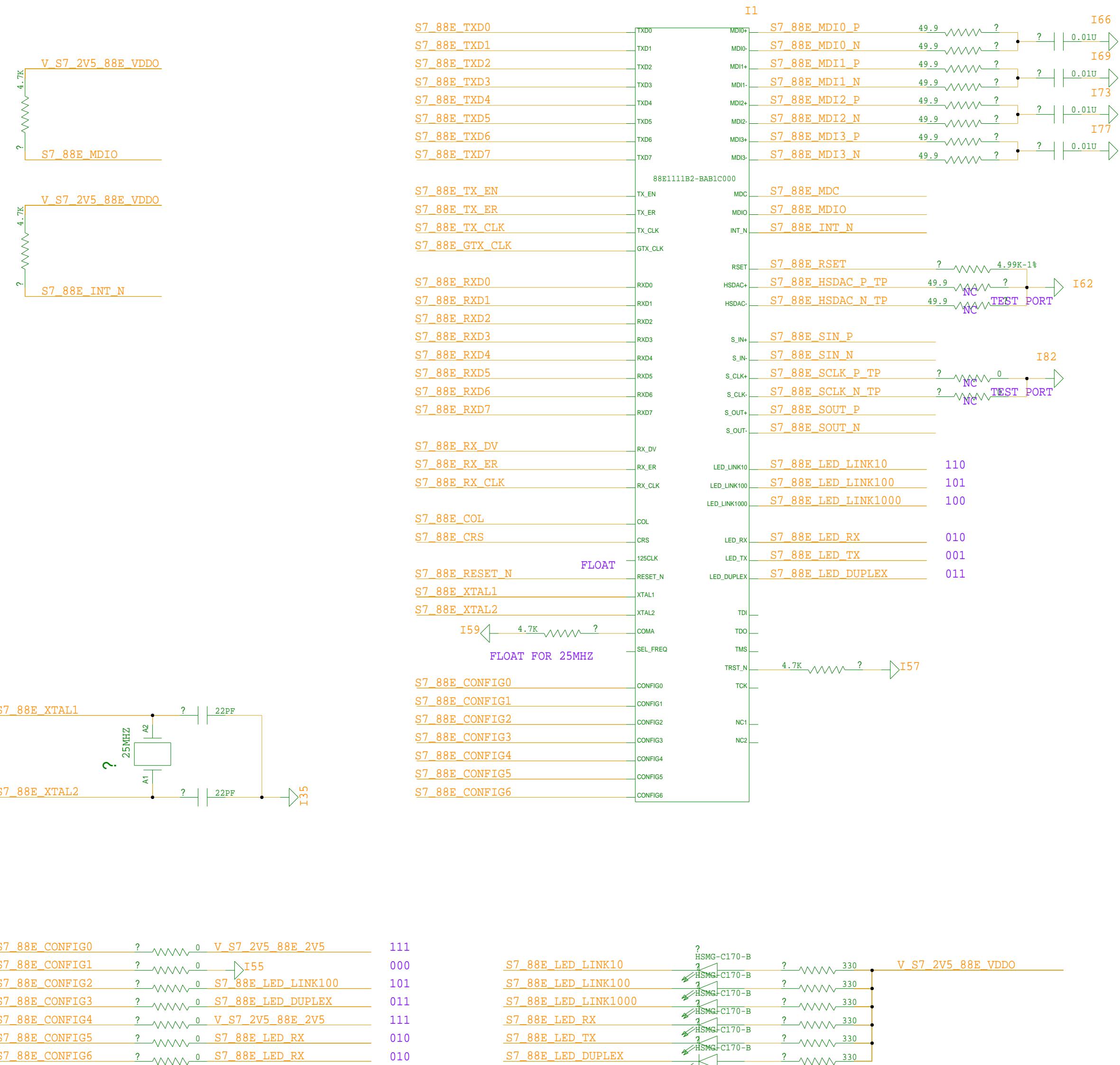
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SPARTAN-7 SFP PHY (1)

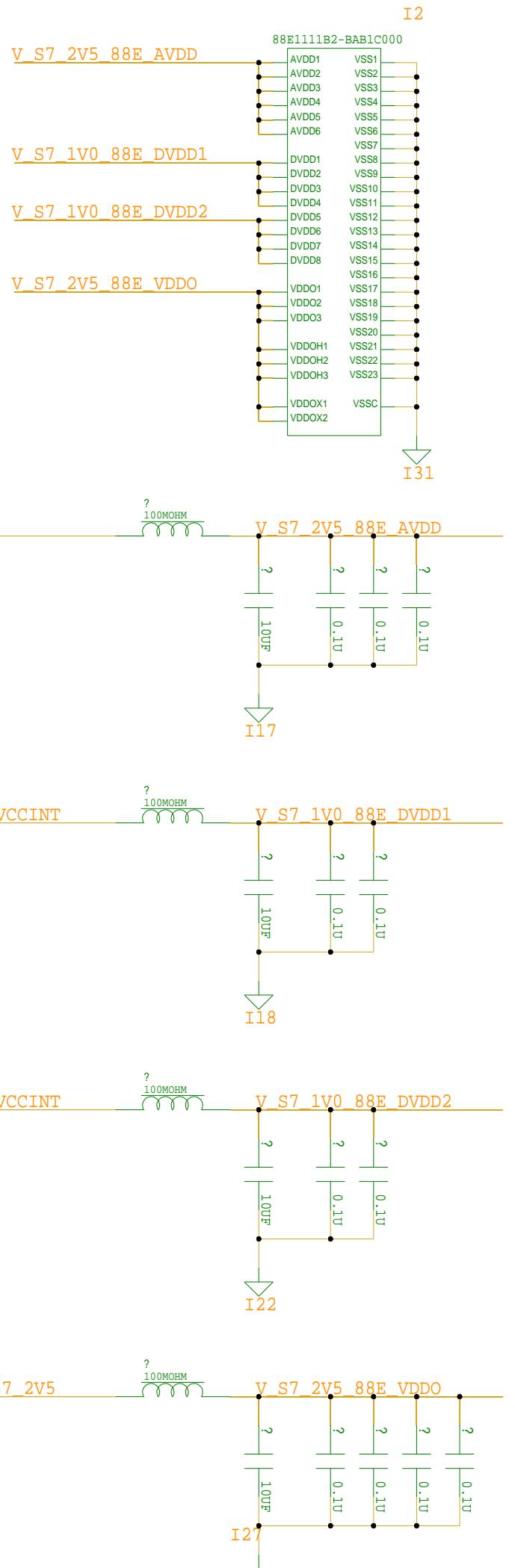
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PIN	CONNECTION	BACKUP	REG	VALUE	BACKUP	CONFIGURATION
CONFIG0	VDD	GND	PHYADR[2:0]	111	000	PHYADR=111
CONFIG1	GND	LED_LINK1000	ENA_PAUSE/PHYADR[4:3]	000	100	Disable PAUSE frame, PHYADR=00
CONFIG2	VDD		ANEG[3:1]	101	111	Fiber, force 1000BASE-X full-duplex
CONFIG3	LED_DUPLEX		ANEG[0]/ENA_XC/DIS_125	011		Crossover Enable, Disable 125MHz
CONFIG4	VDD	LED_DUPLEX	HWCFG_MODE[2:0]	111	011	GMII to Fiber 0111
CONFIG5	LED_RX	LED_LINK10	DIS_FC/DIS_SLEEP/HWCFG_MODE[3]	010	110	Enable FC/Copper, Disable Sleep
CONFIG6	LED_RX	LED_LINK10	SEL_TWSI/INT_POL/75_500OHM	010	110	MDI/MDC, INT low, 50 ohm serdes

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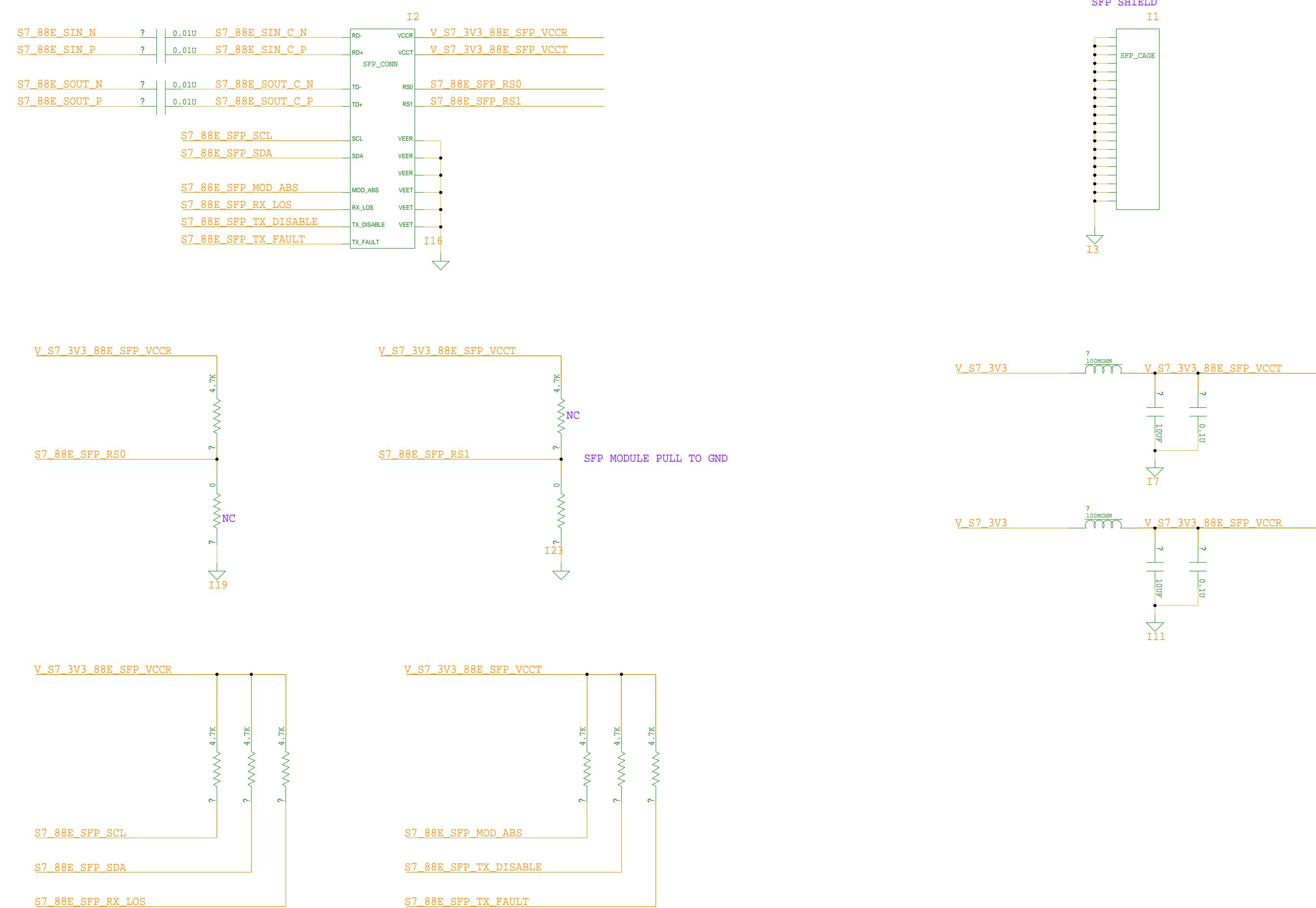


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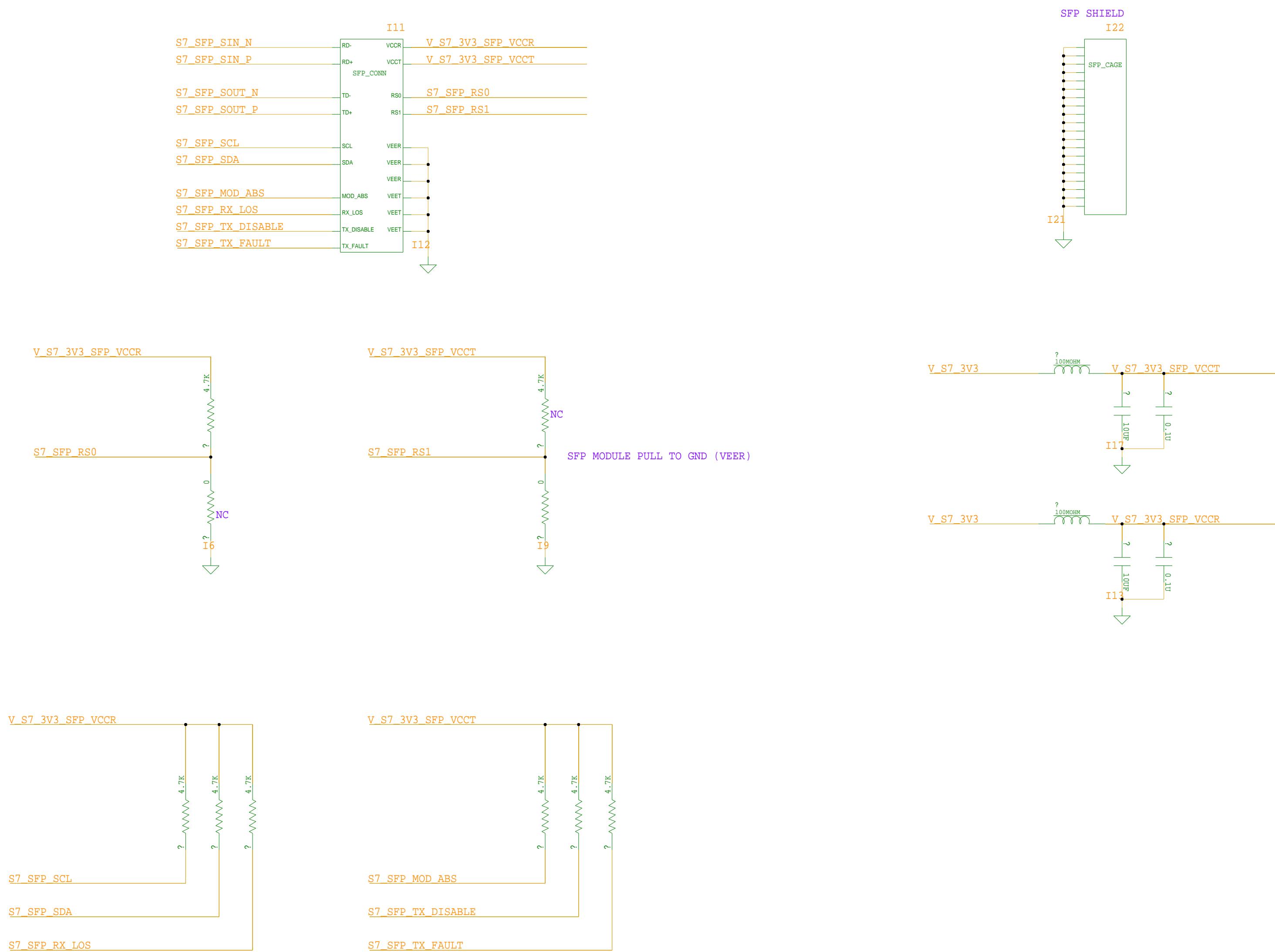
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SPARTAN-7 SFP INOUT

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SPARTAN-7 USB CONTROLLER (1)

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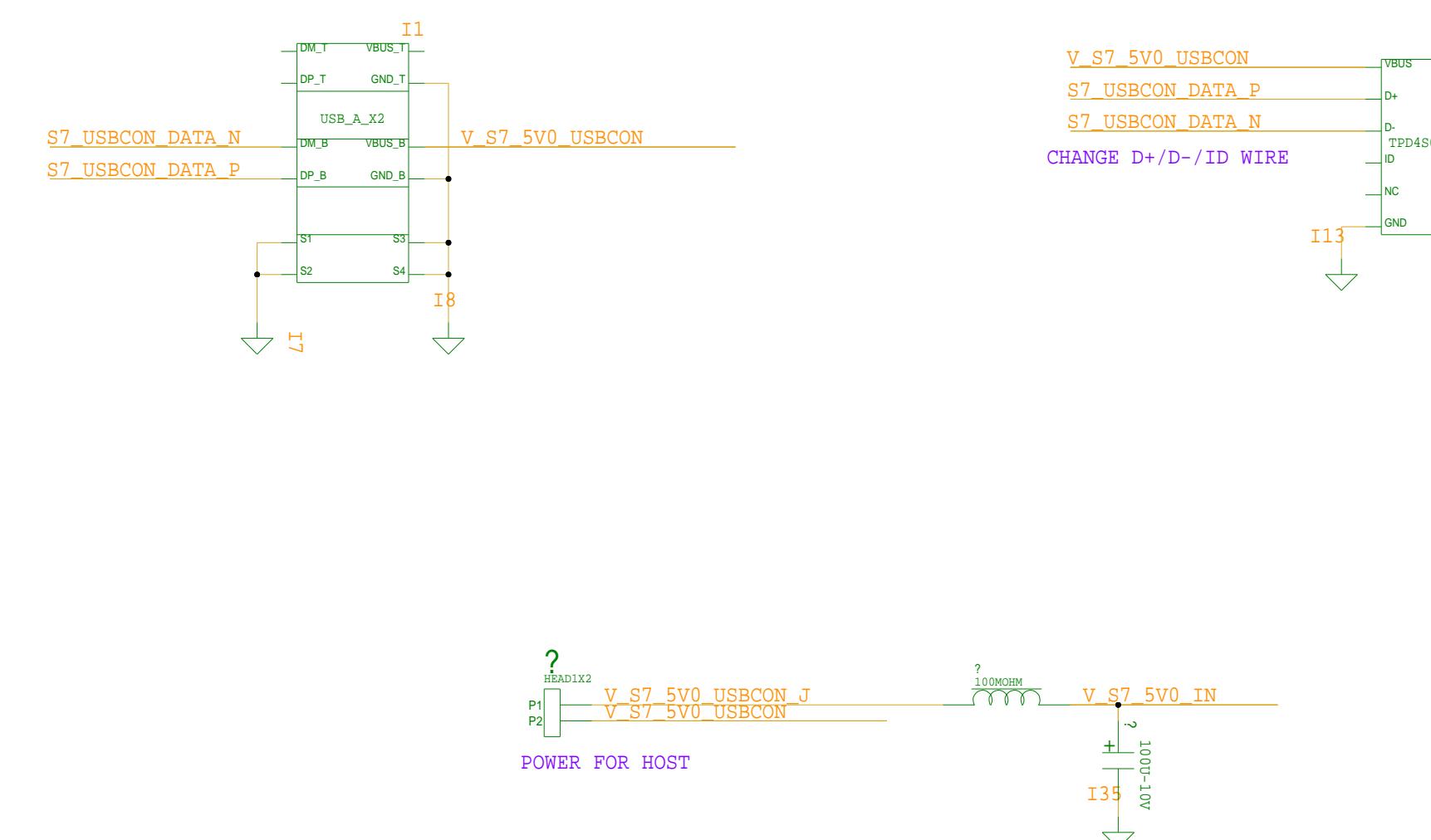
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SPARTAN-7 USB CONTROLLER (2)

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USB IP CORE DOSEN'T SUPPORT SPARTAN-7

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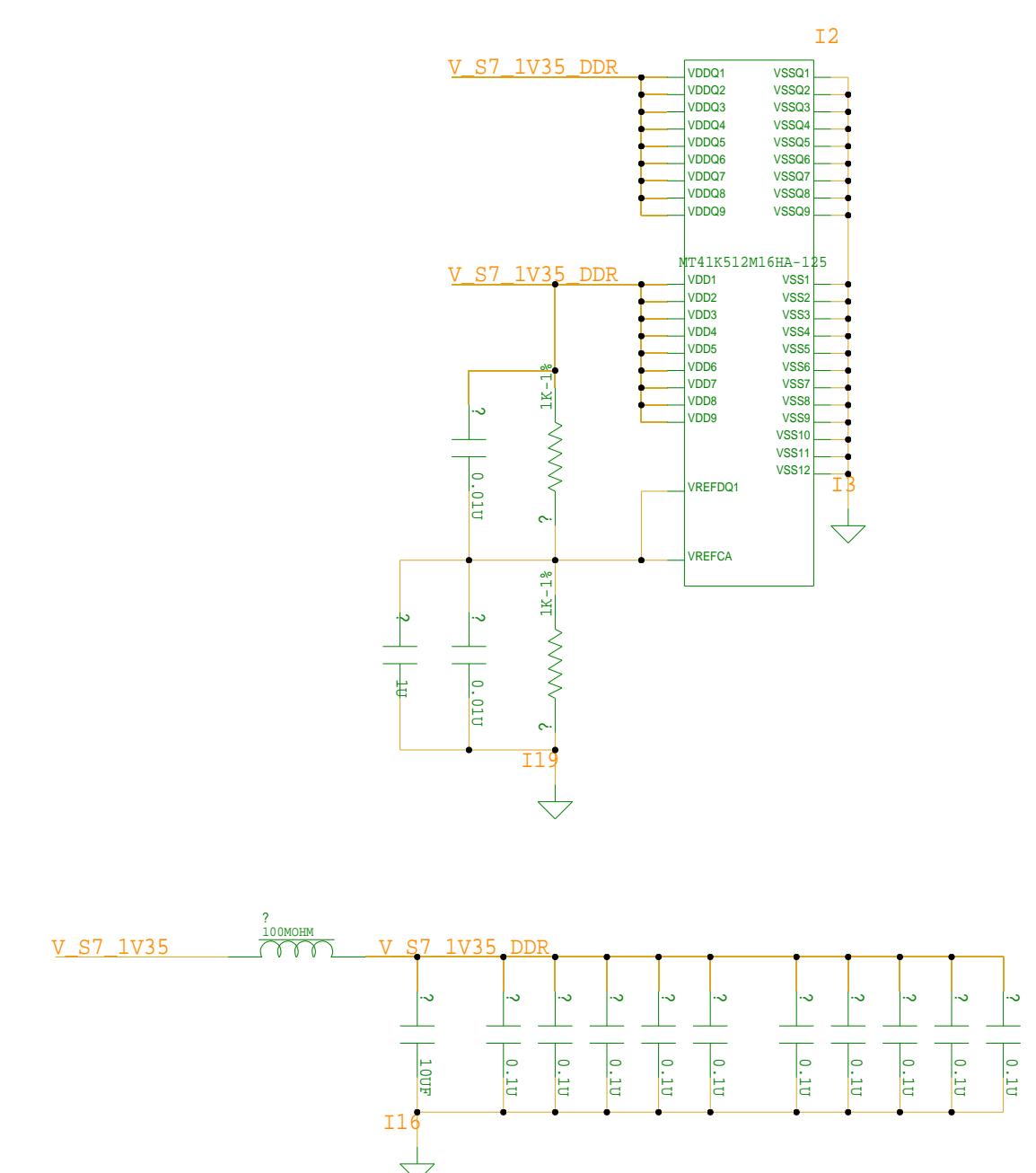
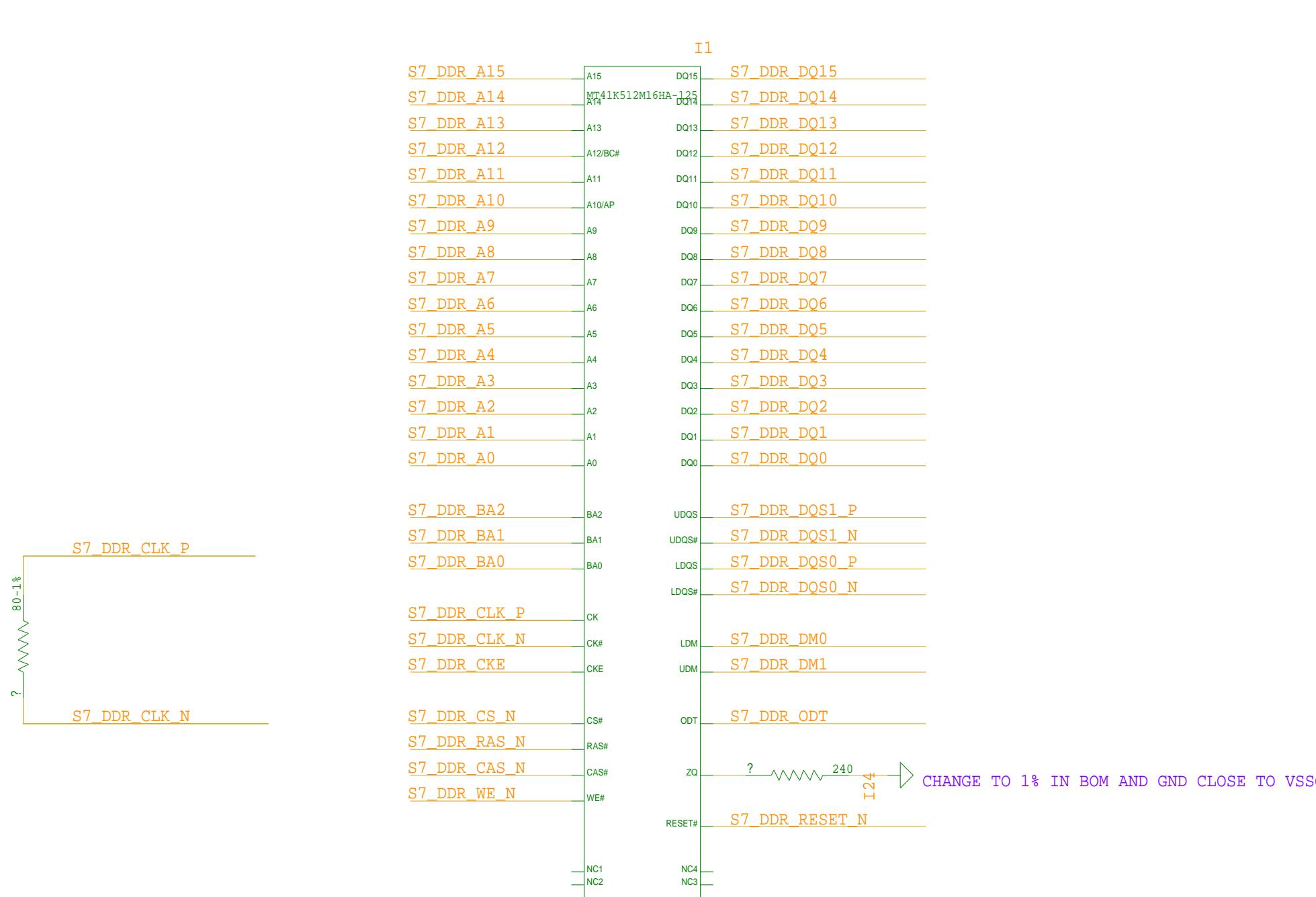
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SPARTAN-7 DDR3

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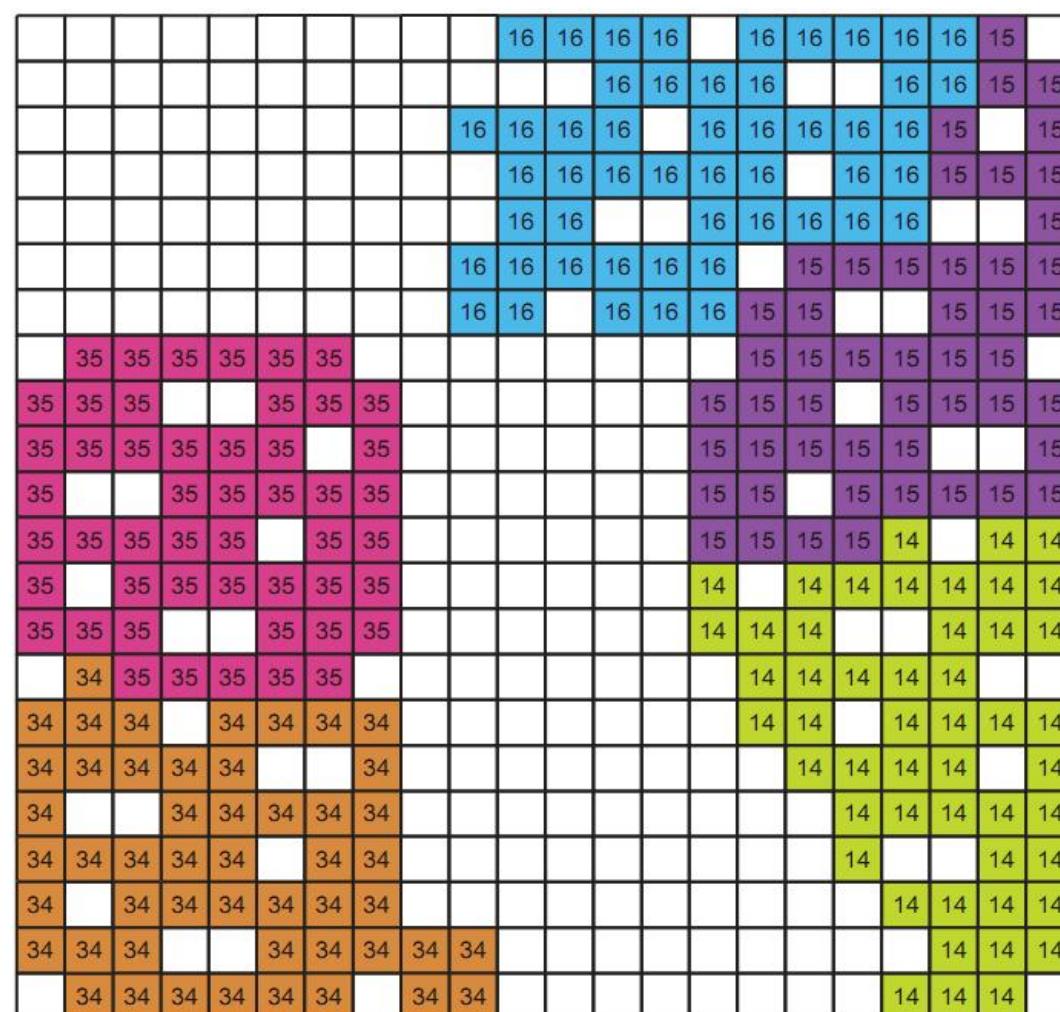


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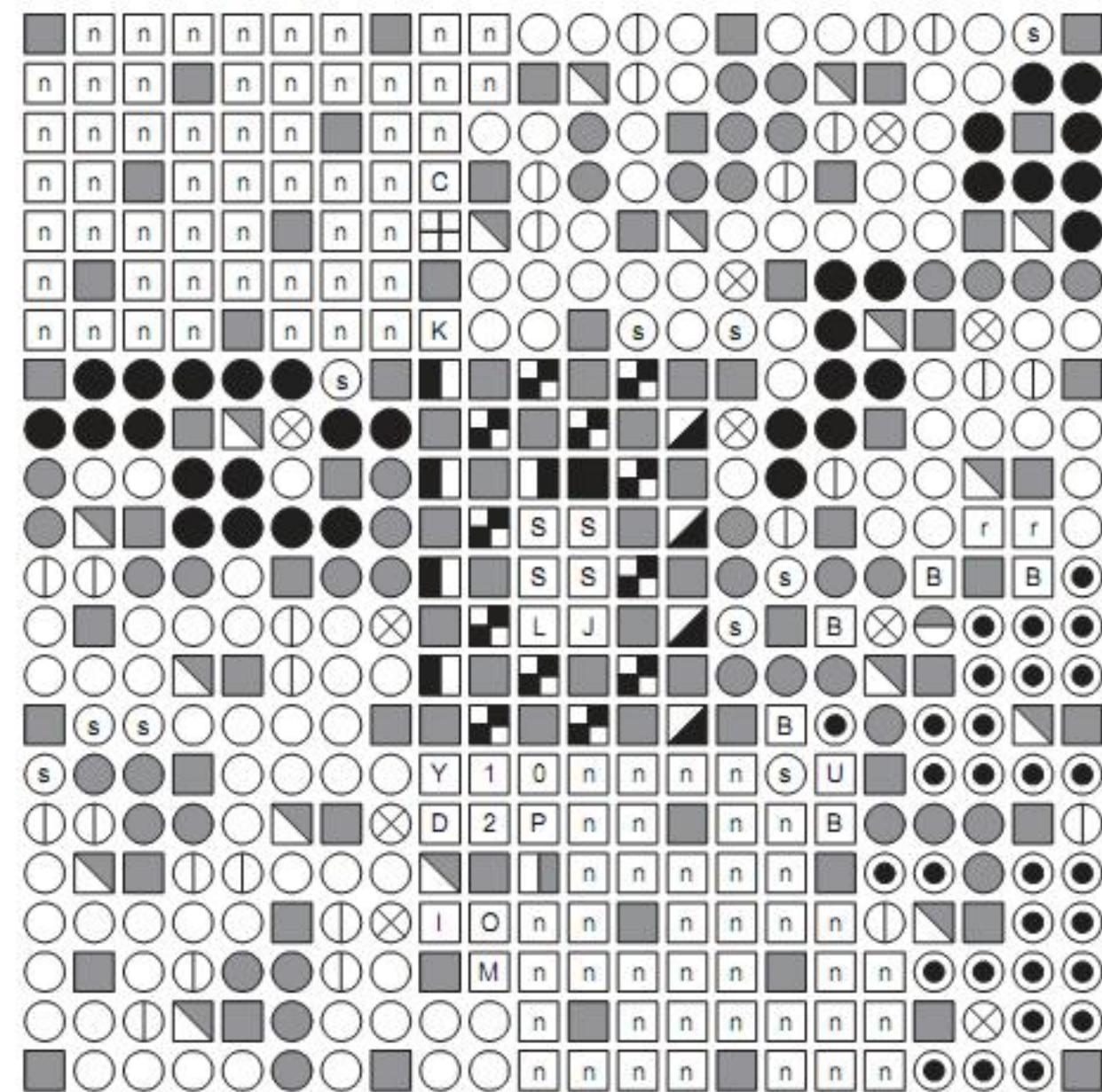
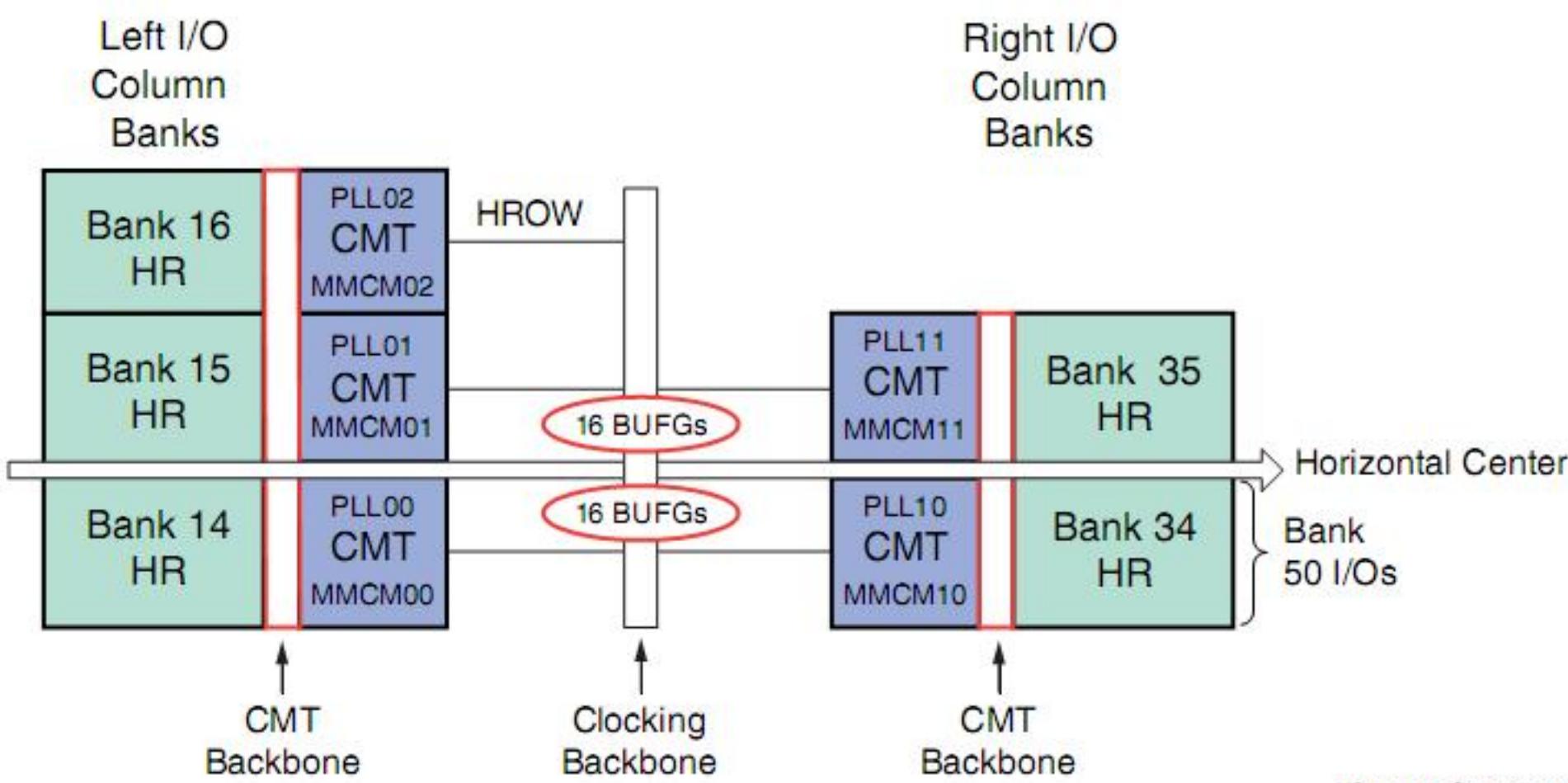
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SPARTAN-7 PINOUT MAP



BANK0 : 3.3V CONFIG
BANK14 : 3.3V HDMI RECEIVER/ HDMI INOUT/ USB
BANK15 : 3.3V HDMI TRANSMITTER/ RECEIVER
BANK16 : 3.3V SFP INOUT/ HDMI TRANSMITTER
BANK34 : 1.35V DDR3
BANK35 : 2.5V GE PHY/ SFP INOUT

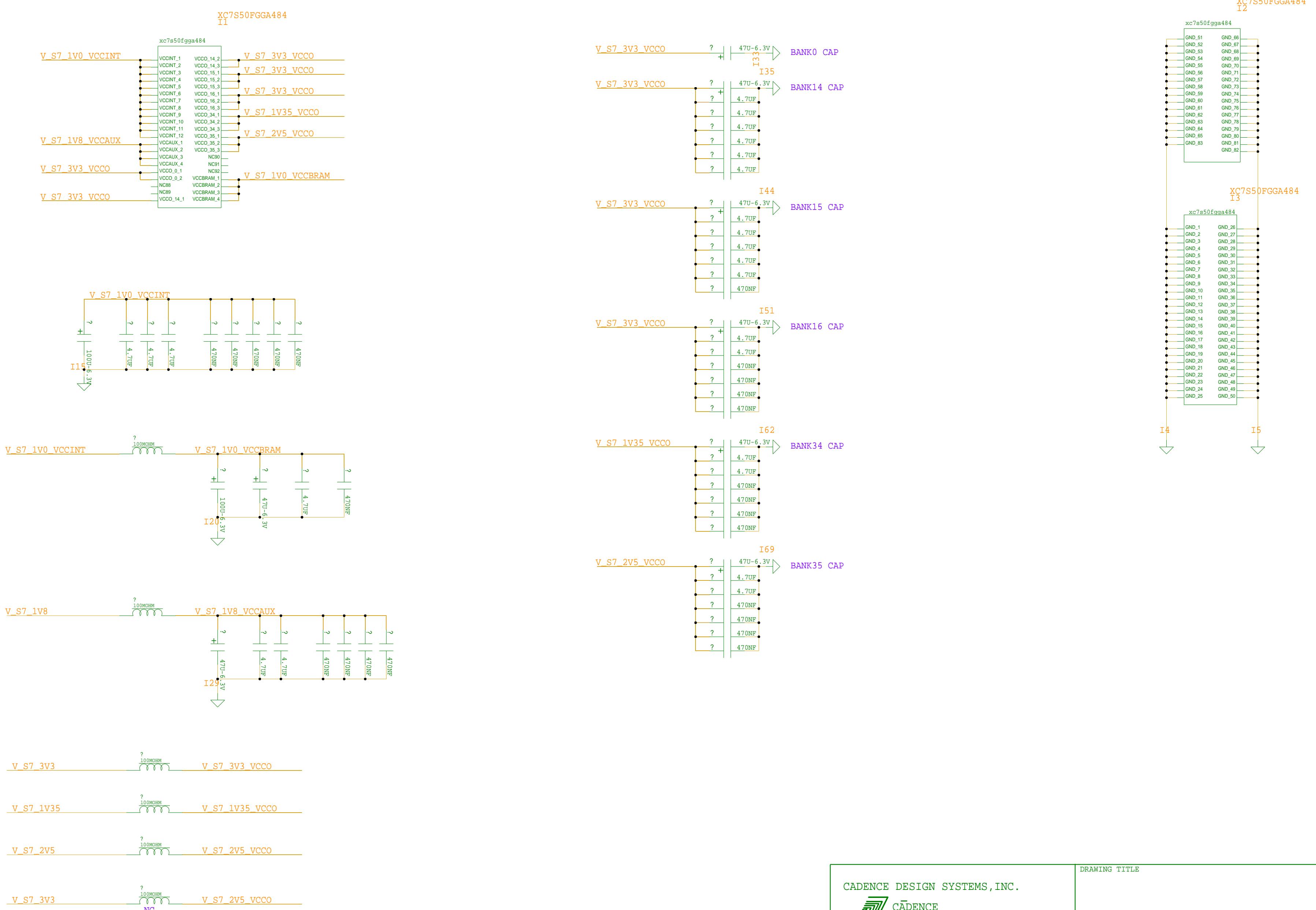


User I/O Pins	Dedicated Pins	Other Pins
○ IO_LXXY_#	C CCLK_0	S VP_0
(s) IO_XX_#	T CFGBVS_0	S VN_0
Multi-Function Pins		
B ADV_B	⊕ VRN	█ GND
B FCS_B	⊖ VRP	▀ VCCAUX_IO_G#
B FOE_B	⊗ VREF	△ VCCAUX
B MOSI	● D00-D31	□ VCCINT
B FWE_B	● A00-A28	▨ VCCO_#
B DOUT_CS0_B	○ DQS	■ VCCBRAM
B CSI_B	● MRCC	n NC
B PUDC_B	● SRCC	
U RDWR_B		
r RS0-RS1		
● AD0P/AD0N-AD15P/AD15N		
● EMCCLK		
	C DONE_0	S VREFP_0
	J DXP_0	S VREFN_0
	L DXN_0	
	█ GNDADC_0	
	Y INIT_B_0	
	0 M0_0	
	1 M1_0	
	2 M2_0	
	P PROGRAM_B_0	
	K TCK_0	
	I TDI_0	
	O TDO_0	
	M TMS_0	
	█ VCCADC_0	
	▀ VCCBATT_0	

SPARTAN-7 BANK POWER

REVISIONS

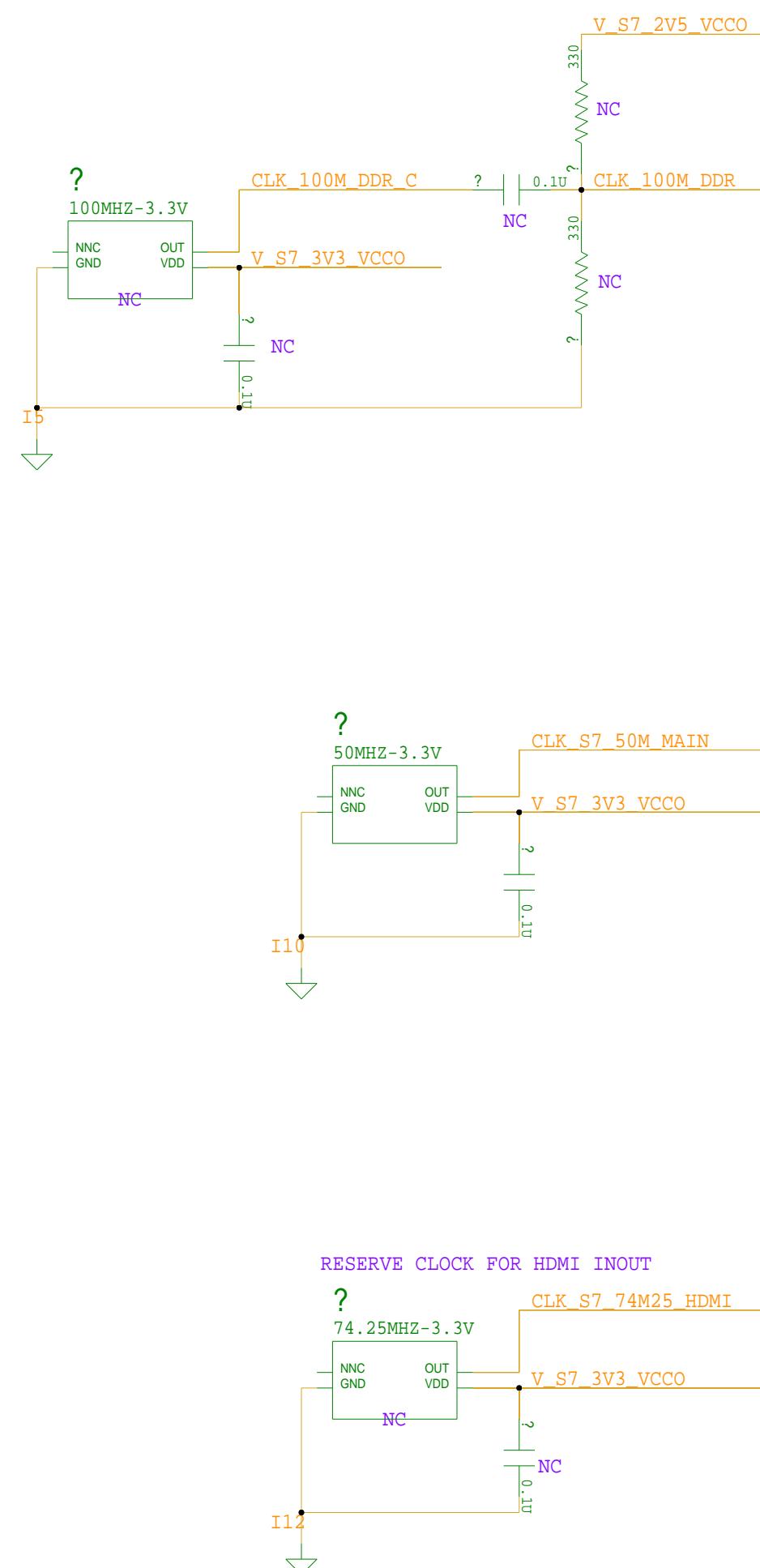
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SPARTAN-7 CLOCK



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SPARTAN-7 BANK15

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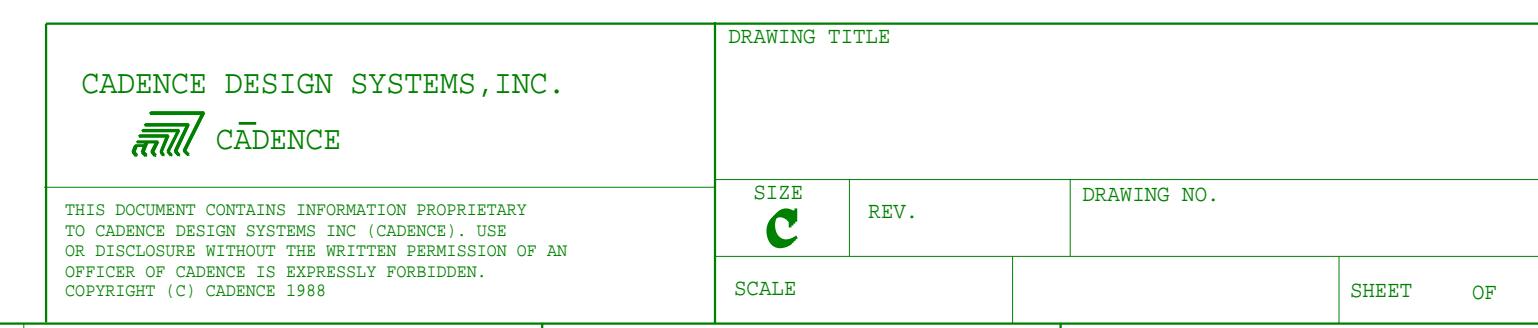
xc7s50fsgga484		XC7S50FGGA484 I1
S7_7612_CS_N	IO_L1P_T0_AD0P_15	S7_7612_P14
S7_7612_RESET_N	IO_L1N_T0_AD0N_15	S7_7612_LUC
S7_7612_DE	IO_L2P_T0_AD0P_15	S7_7612_P15
S7_7612_SCL	IO_L2N_T0_AD0N_15	S7_7612_P16
S7_7612_SDA	IO_L3P_T0_DQS_AD1P_15	S7_7612_P17
S7_7612_INT1	IO_L3N_T0_DQS_AD1N_15	S7_7612_P18
S7_7612_INT2	IO_L4P_T0_15	S7_7612_P19
S7_7612_HS	IO_L4N_T0_15	S7_7612_P20
S7_7612_VS	IO_L5P_T0_AD0P_15	S7_7612_P21
S7_7612_P0	IO_L5N_T0_AD0N_15	S7_7612_P22
S7_7612_P1	IO_L6P_T0_15	S7_7612_P23
S7_7612_P2	IO_L6N_T0_VREF_15	S7_7612_P24
S7_7612_P3	IO_L7P_T1_AD2P_15	S7_7612_P25
S7_7612_P4	IO_L7N_T1_AD2N_15	S7_7612_P26
S7_7612_P5	IO_L8P_T1_AD1P_15	S7_7612_P27
S7_7612_P6	IO_L8N_T1_AD10N_15	S7_7612_P28
S7_7612_P7	IO_L9P_T1_DQS_AD3P_15	S7_7612_P29
S7_7612_P8	IO_L9N_T1_DQS_AD3N_15	S7_7612_P30
S7_7612_P9	IO_L10P_T1_AD11P_15	S7_7612_P31
S7_7612_P10	IO_L10N_T1_AD11N_15	S7_7612_P32
S7_7612_P11	IO_L11P_T1_SRCC_15	S7_7612_P33
S7_7612_P12	IO_L11N_T1_SRCC_15	S7_7612_P34
CLK_S7_50M_MAIN	IO_L12P_T1_MRCC_15	S7_7612_P35
S7_7612_P13	IO_L12N_T1_MRCC_15	S7_7612_P35
CLK_S7_74M25_HDMI	IO_L13P_T2_MRCC_15	IO_25_15 S7_HDMI_SCL_Q S7_HDMI_SDA_Q IO_0_15

DO NOT CHANGE WIRES AS BELOW:

CLK_50M_MAIN
CLK_74M25_HDMI

OD CONFIG AS BELOW:

S7_7612_SCL
S7_7612_SDA
S7_HDMI_SCL_Q
S7_HDMI_SDA_Q



SPARTAN-7 BANK16

REVISIONS

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xc7s50fgga484
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xc7s50fgga484

S7_SFP_SIN_P	IO_L1P_T0_16	IO_L19N_T2_MRCC_16	S7_7511_D8
S7_SFP_SIN_N	IO_L1N_T0_16	IO_L14P_T2_SRCC_16	S7_7511_D9
S7_SFP_SOUT_P	IO_L2P_T0_16	IO_L14N_T2_SRCC_16	S7_7511_D10
S7_SFP_SOUT_N	IO_L2N_T0_16	IO_L15P_T2_DOS_16	S7_7511_D11
S7_FPGA_7511_SCL	IO_L3P_T0_DQS_16	IO_L15N_T2_DOS_16	S7_7511_D12
S7_FPGA_7511_SDA	IO_L3N_T0_DQS_16	IO_L16P_T2_16	S7_7511_D13
S7_7511_DE	IO_L4P_T0_16	IO_L16N_T2_16	S7_7511_D14
S7_7511_HSYNC	IO_L4N_T0_16	IO_L17P_T2_16	S7_7511_D15
S7_FPGA_7511_INT	IO_L5P_T0_16	IO_L17N_T2_16	S7_7511_D19
S7_7511_SDPFF_OUT	IO_L5N_T0_16	IO_L18P_T2_16	S7_7511_D20
S7_7511_VSYNC	IO_L6P_T0_16	IO_L18N_T2_16	S7_7511_D21
S7_7511_D0	IO_L7P_T0_VREF_16	IO_L19P_T3_16	S7_7511_D22
S7_7511_D1	IO_L7N_T0_VREF_16	IO_L19N_T3_16	S7_7511_D23
S7_7511_D2	IO_L7N_T1_16	IO_L20P_T3_16	S7_7511_D24
S7_7511_D3	IO_L8P_T1_16	IO_L20N_T3_16	S7_7511_D25
S7_7511_D4	IO_L8N_T1_16	IO_L21P_T3_DQS_16	S7_7511_D26
S7_7511_D5	IO_L9P_T1_DQS_16	IO_L21N_T3_DQS_16	S7_7511_D27
S7_7511_D6	IO_L9N_T1_DQS_16	IO_L22P_T3_16	S7_7511_D28
S7_7511_D7	IO_L10P_T1_16	IO_L22N_T3_16	S7_7511_D29
S7_7511_CLK	IO_L10N_T1_16	IO_L23P_T3_16	S7_7511_D30
S7_7511_D16	IO_L11P_T1_SRCC_16	IO_L23N_T3_16	S7_7511_D31
S7_7511_D17	IO_L11N_T1_SRCC_16	IO_L24P_T3_16	S7_7511_D32
S7_7511_D18	IO_L12P_T1_MRCC_16	IO_L24N_T3_16	S7_7511_D33
S7_FPGA_7511_CEC_CLK	IO_L12N_T1_MRCC_16	IO_25_16	S7_7511_D34
	IO_L13P_T2_MRCC_16	IO_0_16	S7_7511_D35

OD CONFIG AS BELOW:

S7_FPGA_7511_SCL
S7_FPGA_7511_SDA

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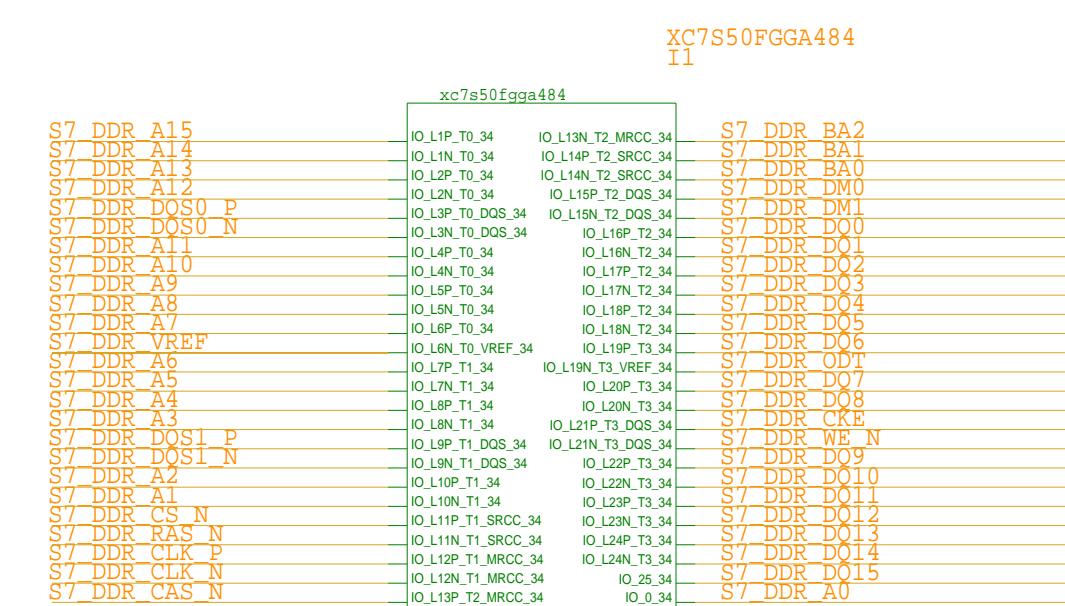
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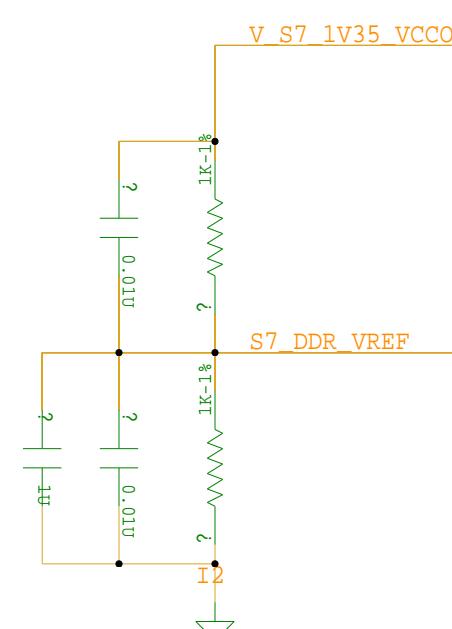
SPARTAN-7 BANK34

REVISED		DESCRIPTION		DATE	APPR.



DO NOT CHANGE WIRES AS BELOW:

S7_DDR_DQS0/1_P/N
S7_DDR_CLK_P/N
S7_DDR_VREF



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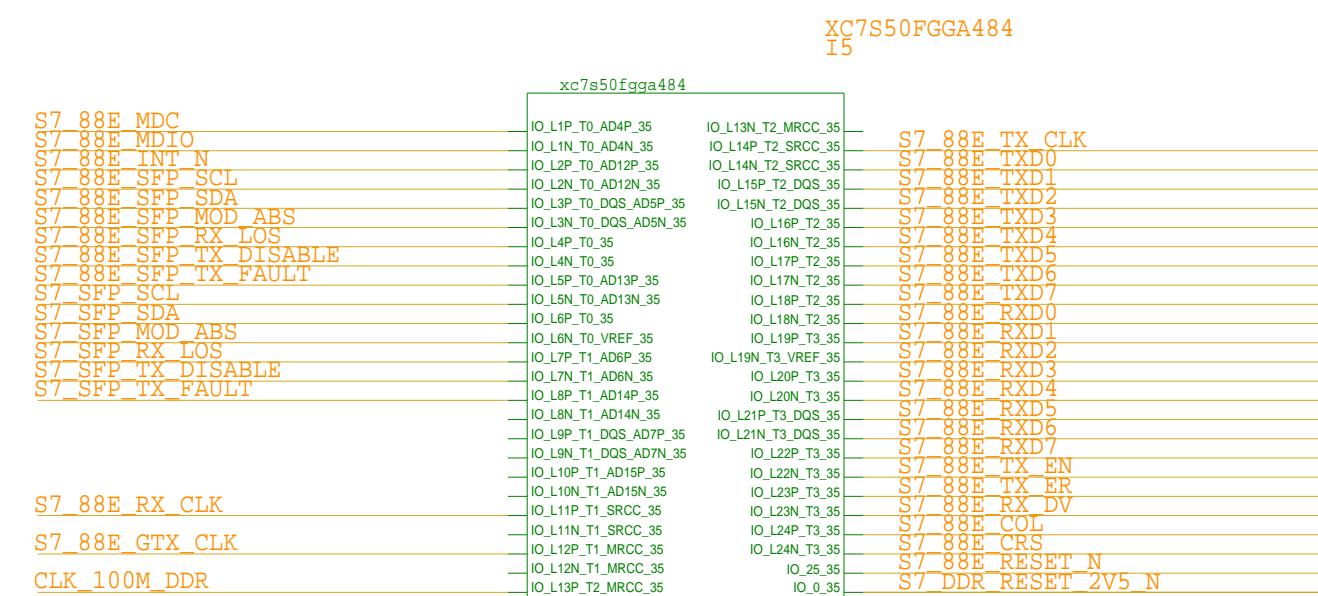
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SPARTAN-7 BANK35

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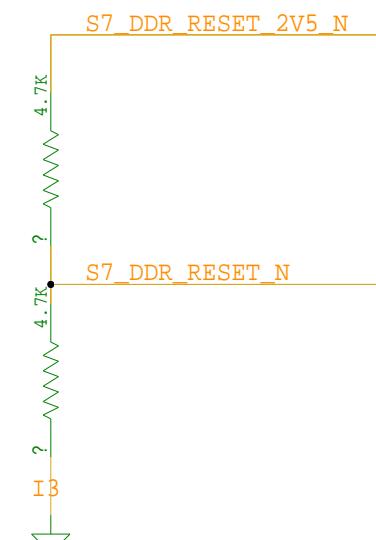
DO NOT CHANGE WIRES AS BELOW:

CLK_100M_DDR
S7_88E_CTX_CLK
S7_88E_RX_CLK

OD CONFIG AS BELOW:

S7_88E_SFP_SCL
S7_88E_SFP_SDA
S7_88E_SFP_MOD_ABS
S7_88E_SFP_RX_LOS
S7_88E_SFP_TX_DISABLE
S7_88E_SFP_TX_FAULT

S7_SFP_SCL
S7_SFP_SDA
S7_SFP_MOD_ABS
S7_SFP_RX_LOS
S7_SFP_TX_DISABLE
S7_SFP_TX_FAULT



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SPARTAN-7 BANK NC

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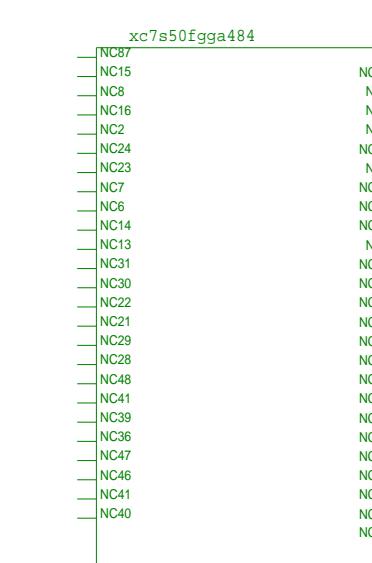
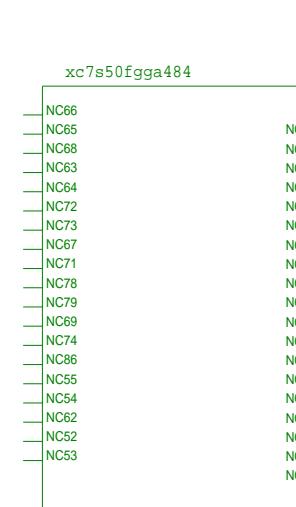
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ARTIX-7 INDEX

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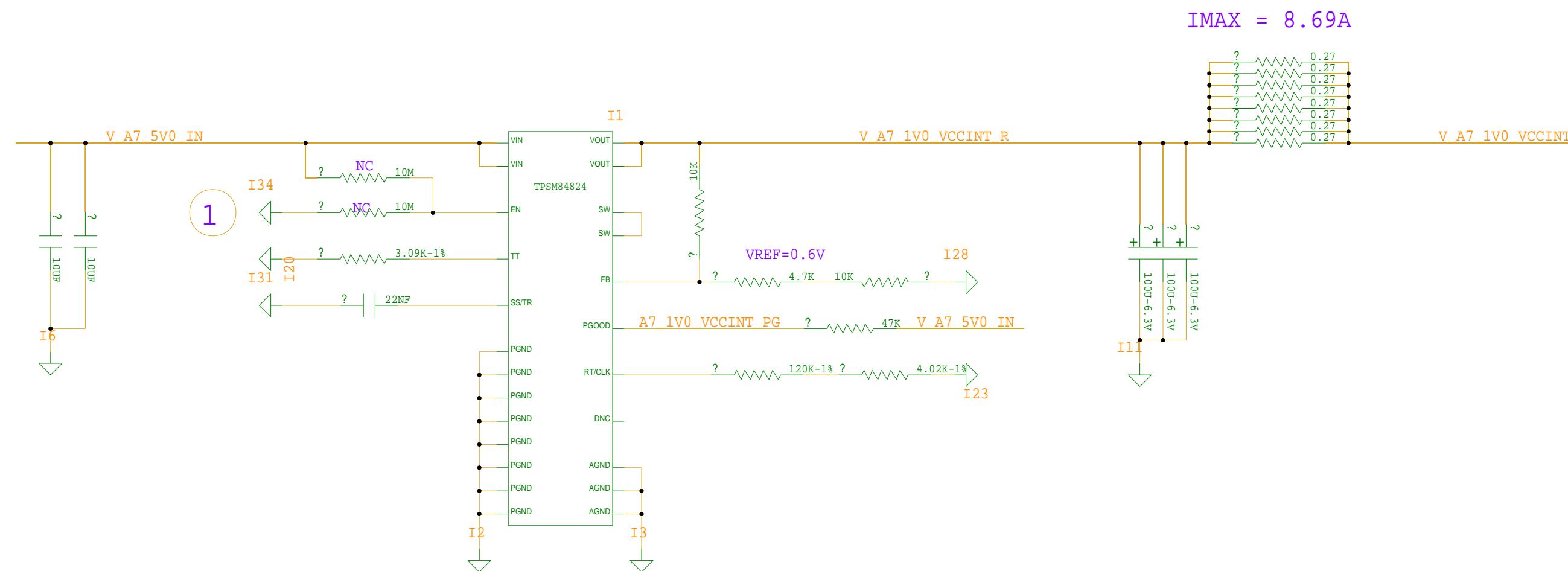
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ARTIX-7 POWER (1)

REVISIONS				
LINE	ITEM	DESCRIPTION	DATE	APPR.



SS/TR	6	I	Soft-start and tracking pin. Connecting an external capacitor to this pin adjusts the output voltage soft-start ramp slower than its 1.2 ms default setting. A voltage applied to this pin allows for tracking and sequencing control.
-------	---	---	--

Table 9. Soft-Start Capacitor Values and Soft-Start Time

C_{SS} (nF)	open	10	15	22	47
SS Time (ms)	1.2	2.4	3	3.8	6.8



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ARTIX-7 POWER (2)

$$V_{OUT} = V_{REF} \times (1 + (R_{TOP}/R_{BOT}))$$

$$R_{RT} (\text{k}\Omega) = [14,822/f_{SW} (\text{kHz})]^{1.08}$$

$$V_{IN_STARTUP} = (0.8 \text{ nA} + (0.8 \text{ V}/R_{BOT_EN})) \times \left(R_{TOP_EN} + \frac{R_{BOT_EN} \times 1 \text{ M}\Omega}{R_{BOT_EN} + 1 \text{ M}\Omega} \right)$$

where:

R_{TOP_EN} is the resistor from V_{IN} to EN

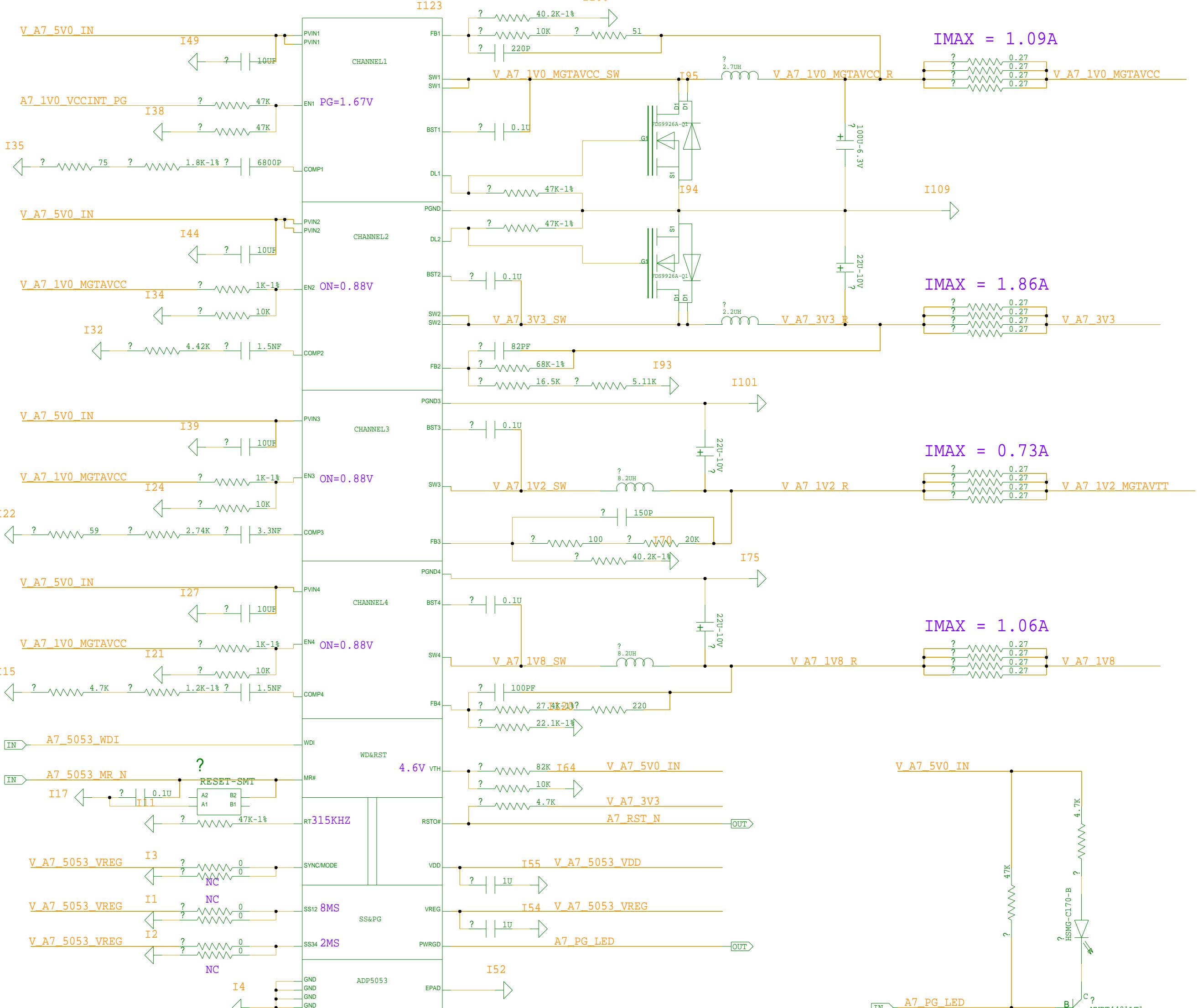
R_{BOT_EN} is the resistor from EN to ground.

Table 9. Soft Start Time Set by the SS12 and SS34 Pin

R _{TOP} (kΩ)	R _{BOT} (kΩ)	Soft Start Time			
		Channel 1	Channel 2	Channel 3	Channel 4
0	N/A ¹	2 ms	2 ms	2 ms	2 ms
100	600	2 ms	Parallel	2 ms	4 ms
200	500	2 ms	8 ms	2 ms	8 ms
300	400	4 ms	2 ms	4 ms	2 ms
400	300	4 ms	4 ms	4 ms	4 ms
500	200	8 ms	2 ms	4 ms	8 ms
600	100	8 ms	Parallel	8 ms	2 ms
N/A ¹	0	8 ms	8 ms	8 ms	8 ms

Table 16. Factory Default Options

Option	Default Value
Channel 1 Output Voltage	0.8 V adjustable output
Channel 2 Output Voltage	0.8 V adjustable output
Channel 3 Output Voltage	0.8 V adjustable output
Channel 4 Output Voltage	0.8 V adjustable output
PWRGD Pin (Pin 20) Output	Monitor Channel 1 output
Output Discharge Function	Enabled for all four buck regulators
Switching Frequency on Channel 1	1 × switching frequency set by the RT pin
Switching Frequency on Channel 3	1 × switching frequency set by the RT pin
SYNC/MODE Pin (Pin 43) Function	Forced PWM/automatic PWM/PSM mode setting with the ability to synchronize to an external clock
Hiccup Protection	Enabled for overcurrent events
Short-Circuit Latch-Off Function	Disabled for output short-circuit events
Oversupply Latch-Off Function	Disabled for output oversupply events
Reset Timeout Period	200 ms
Watchdog Timeout Period	1.6 sec
Manual Reset Input Mode	Processor manual reset mode



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S12

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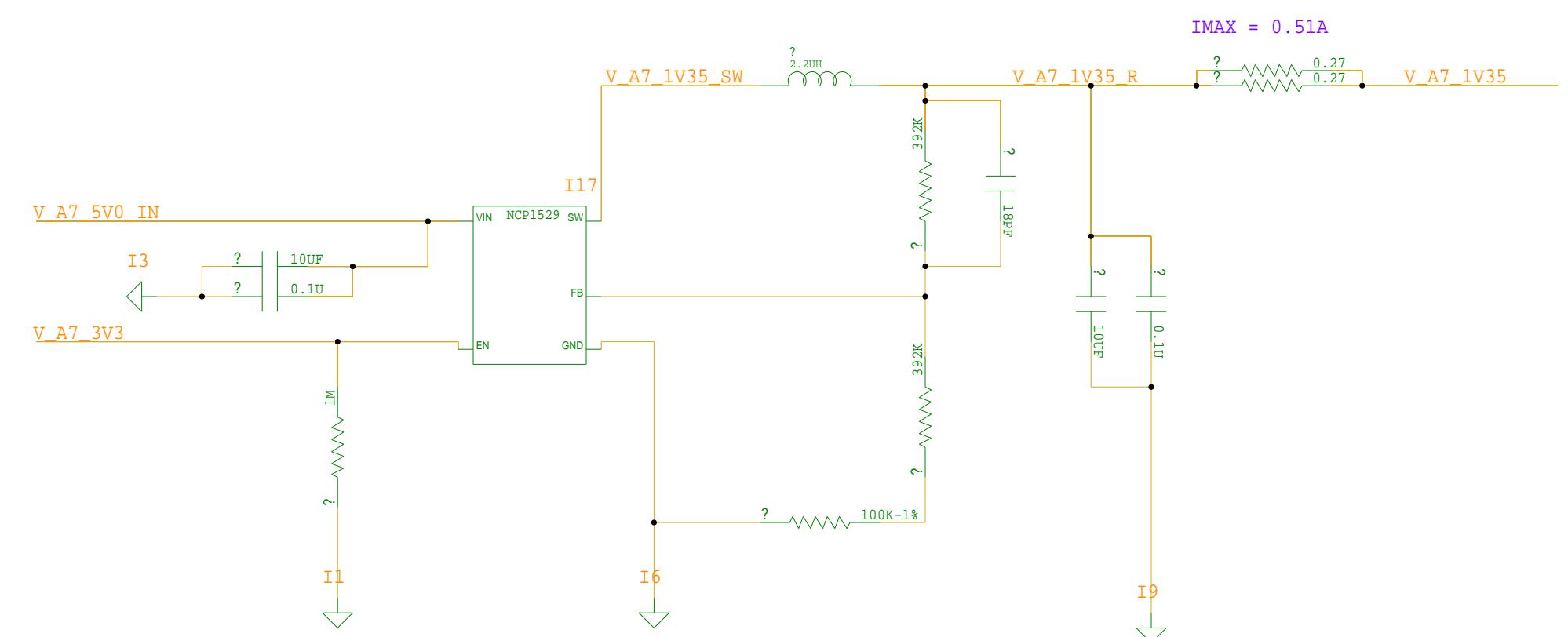
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ARTIX-7 POWER (3)

$$V_{out} = V_{FB} \times (1 + R1/R2)$$

- V_{OUT} : Output Voltage (V)
- V_{FB} : Feedback Voltage = 0.6 V
- $R1$: Feedback Resistor from V_{OUT} to FB
- $R2$: Feedback Resistor from FB to GND

4



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ARTIX-7 HDMI RECEIVER (1)

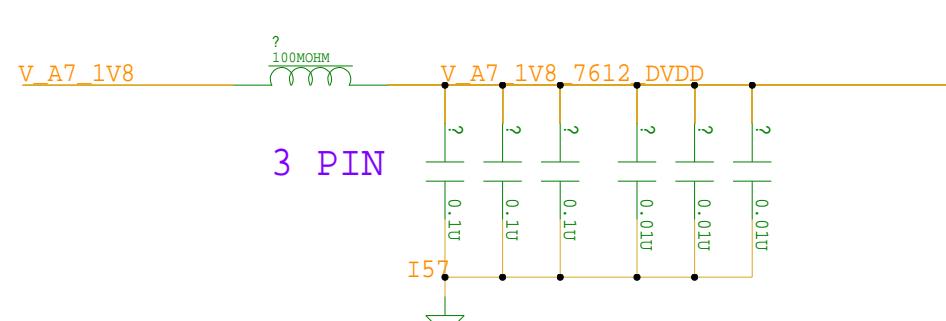
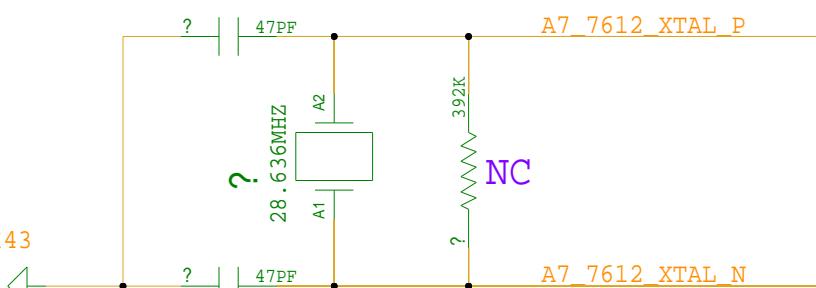
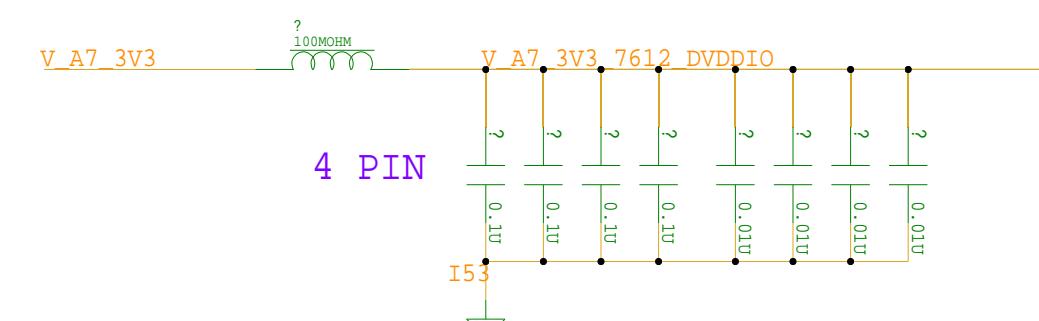
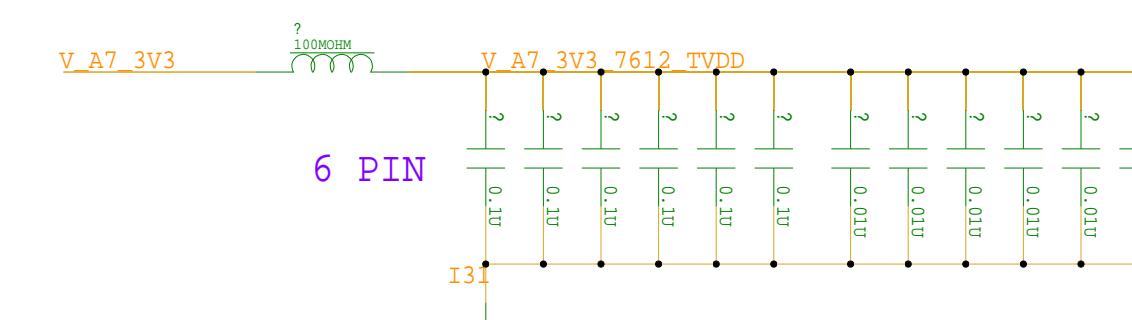
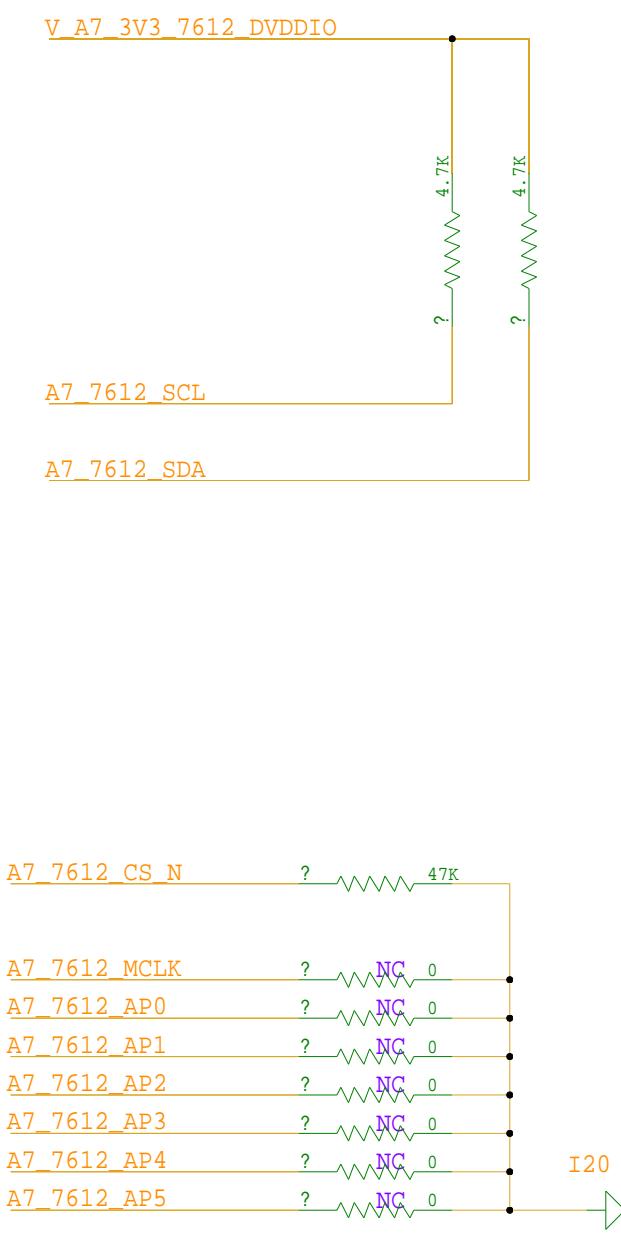
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ARTIX-7 HDMI RECEIVER (2)

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A7_7612_P0
 A7_7612_P1
 A7_7612_P2
 A7_7612_P3
 A7_7612_P4
 A7_7612_P5
 A7_7612_P6
 A7_7612_P7
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 A7_7612_P35



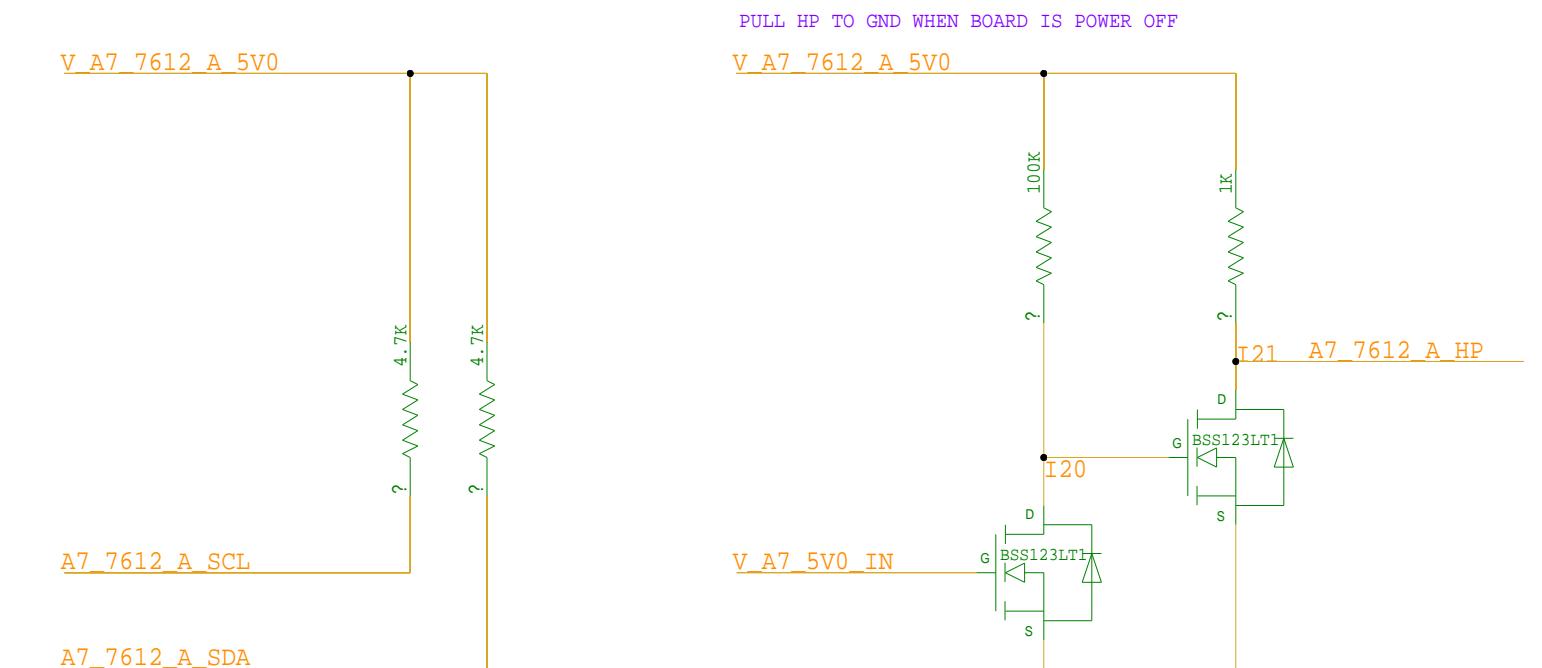
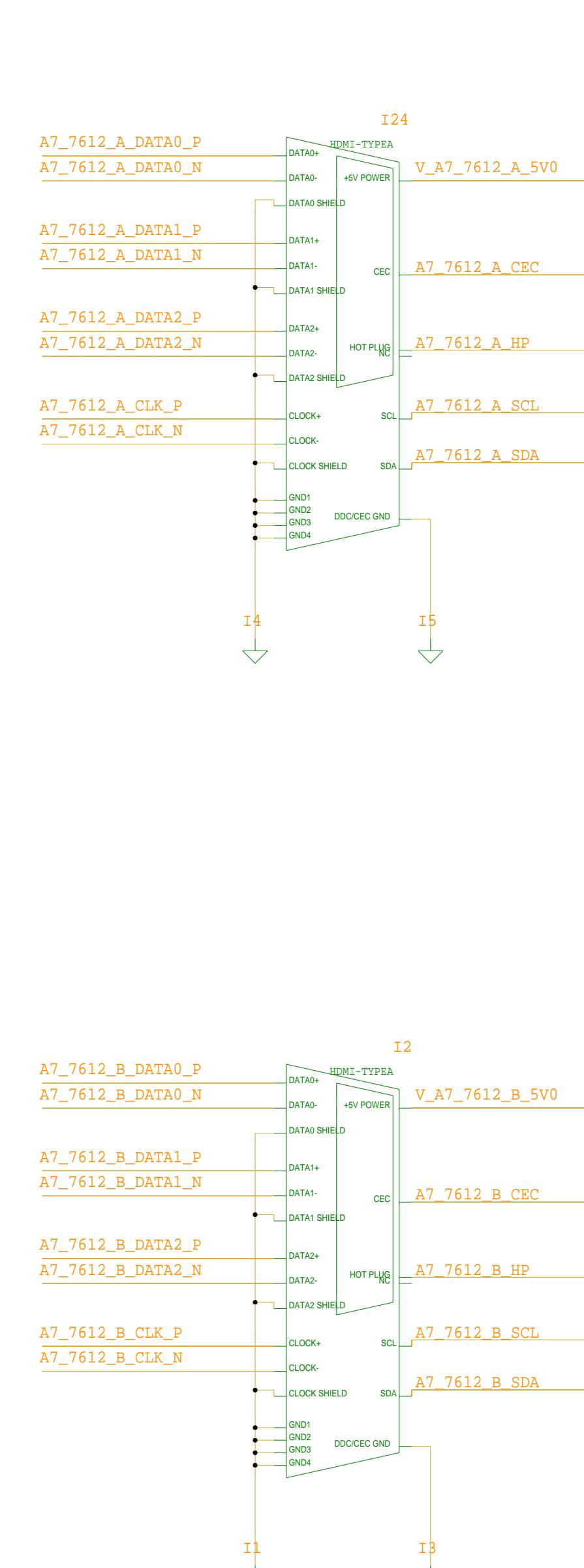
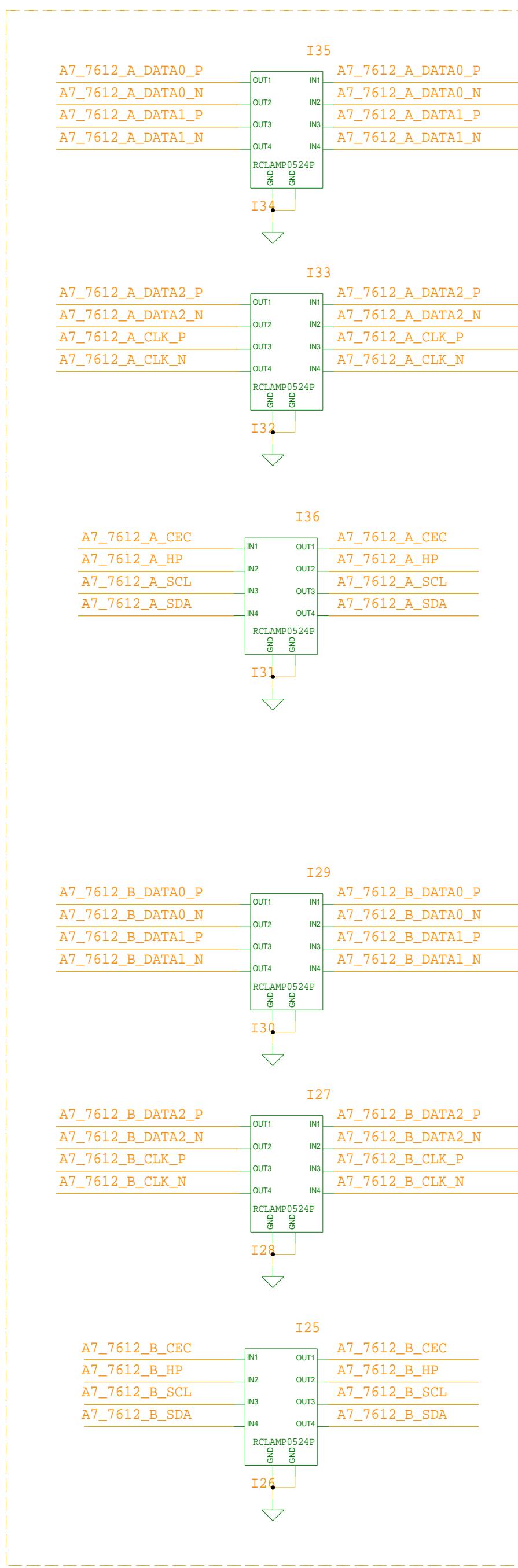
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ARTIX-7 HDMI RECEIVER (3)

CHANGE CONNECTION DUE TO LAYOUT

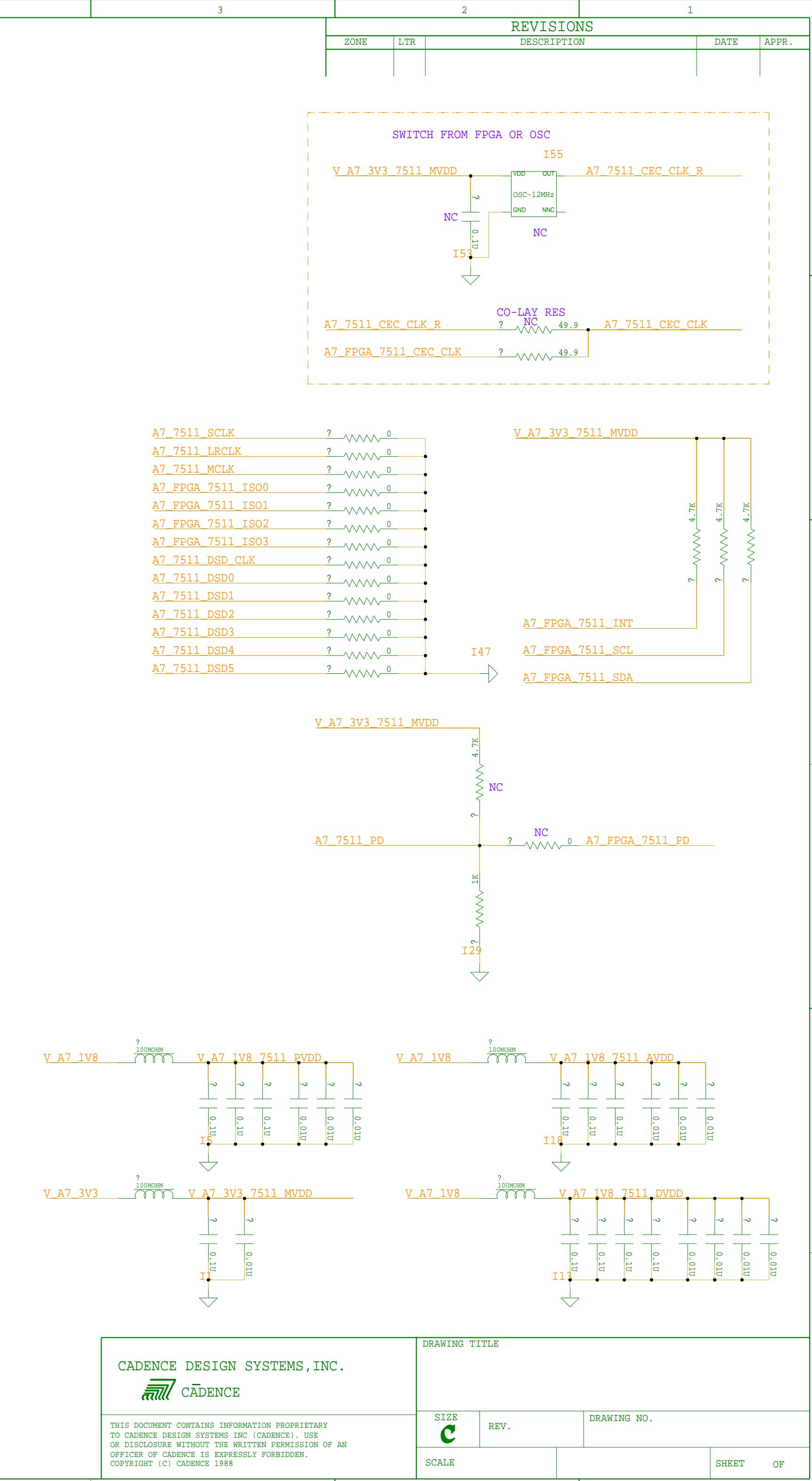
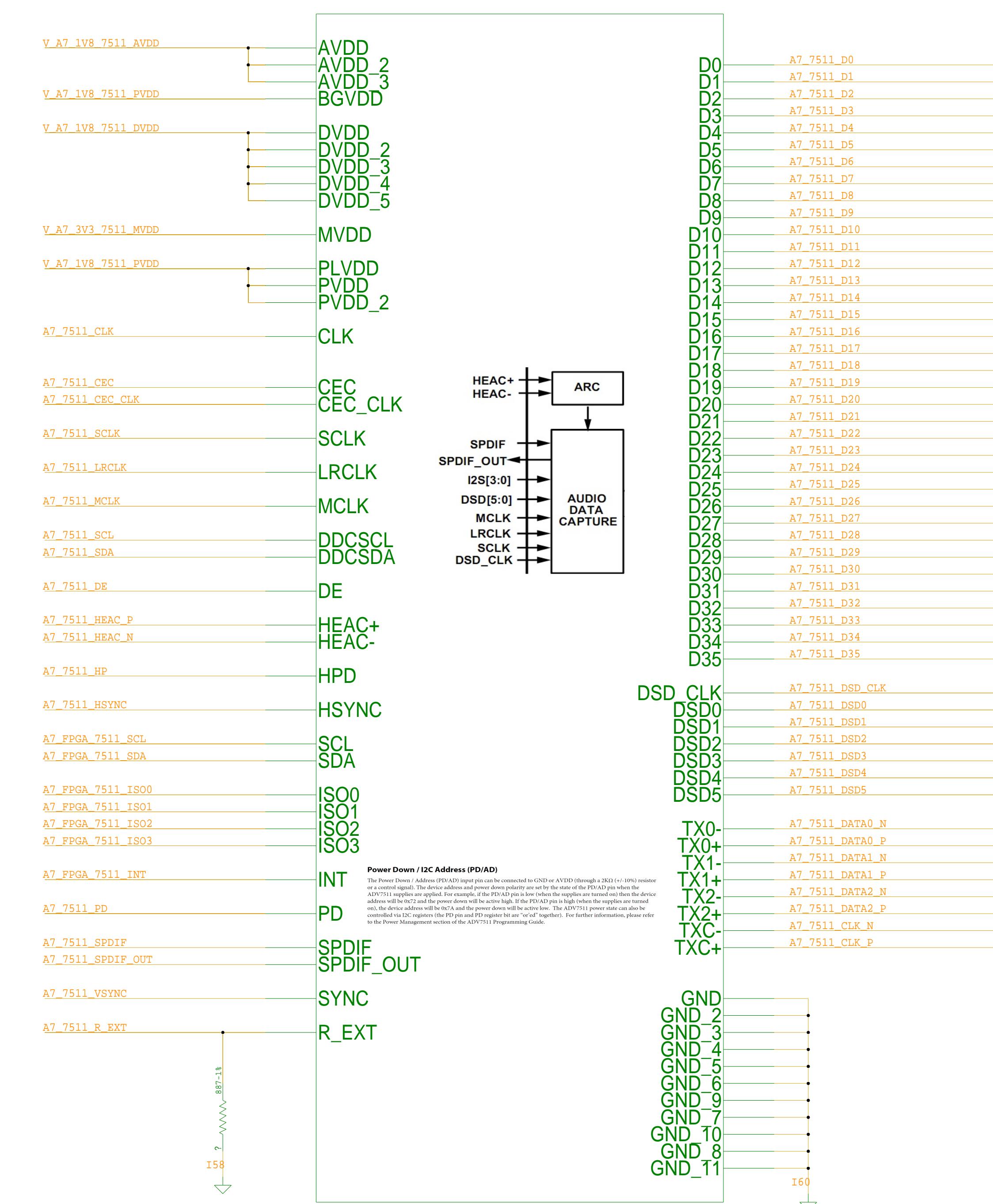


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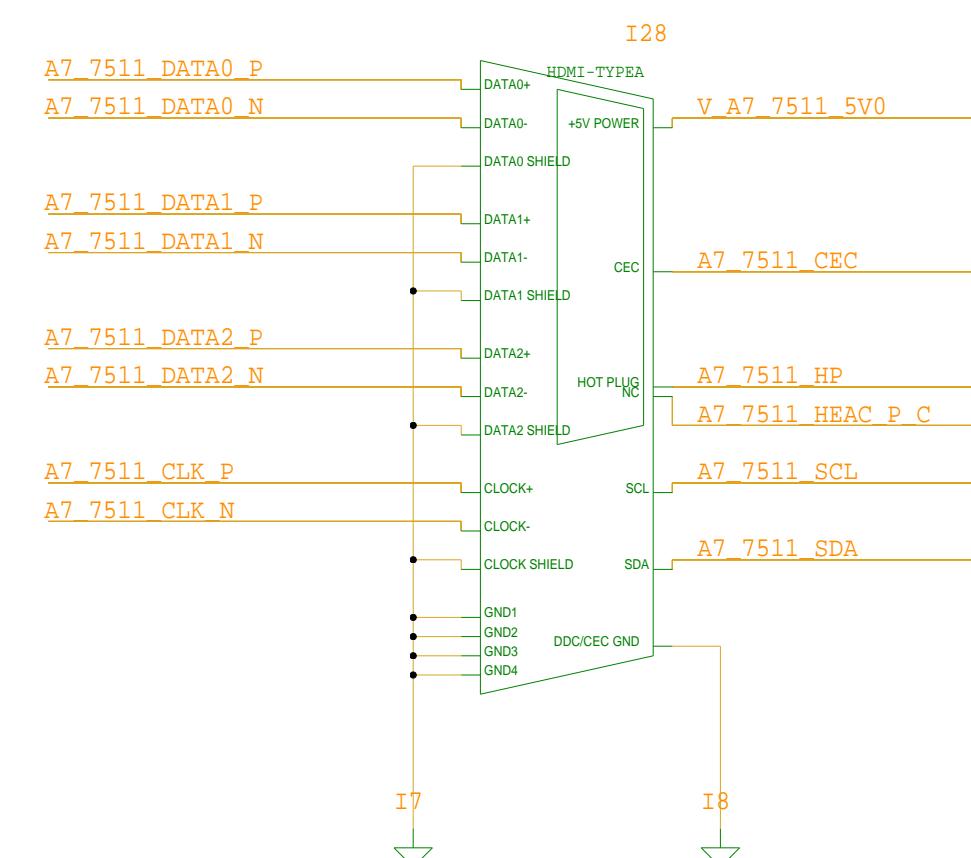
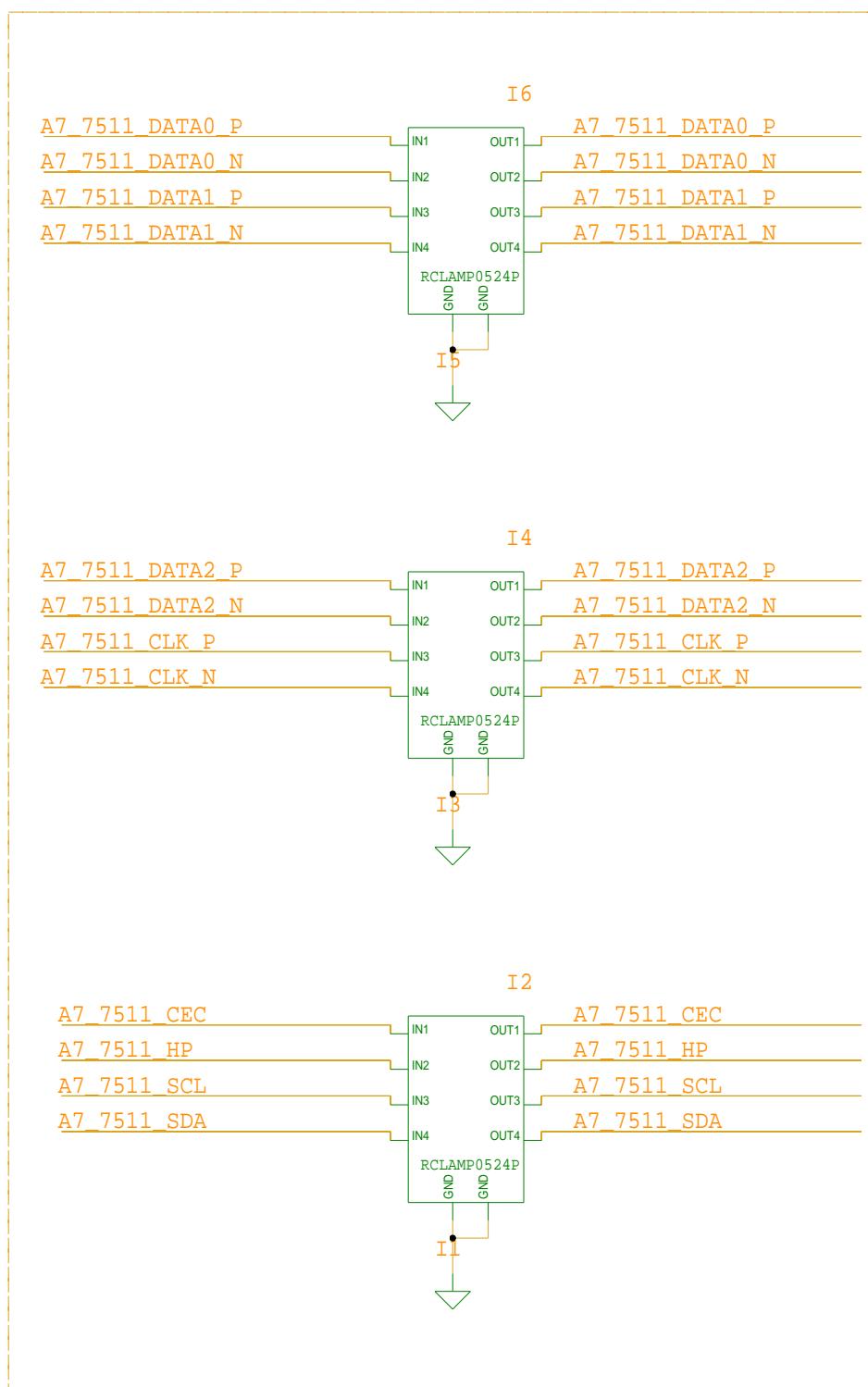


ARTIX-7 HDMI TRANSMITTER (2)

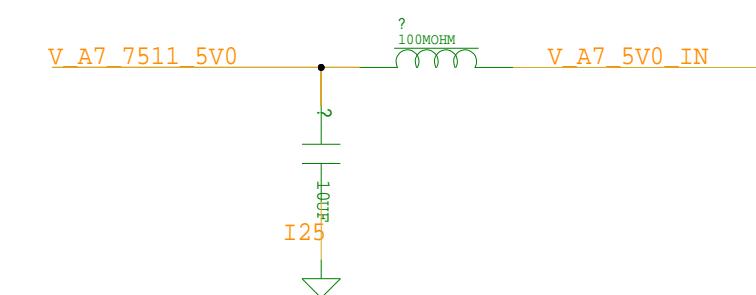
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CHANGE CONNECTION DUE TO LAYOUT



CLOSE TO HDMI CONNECTOR

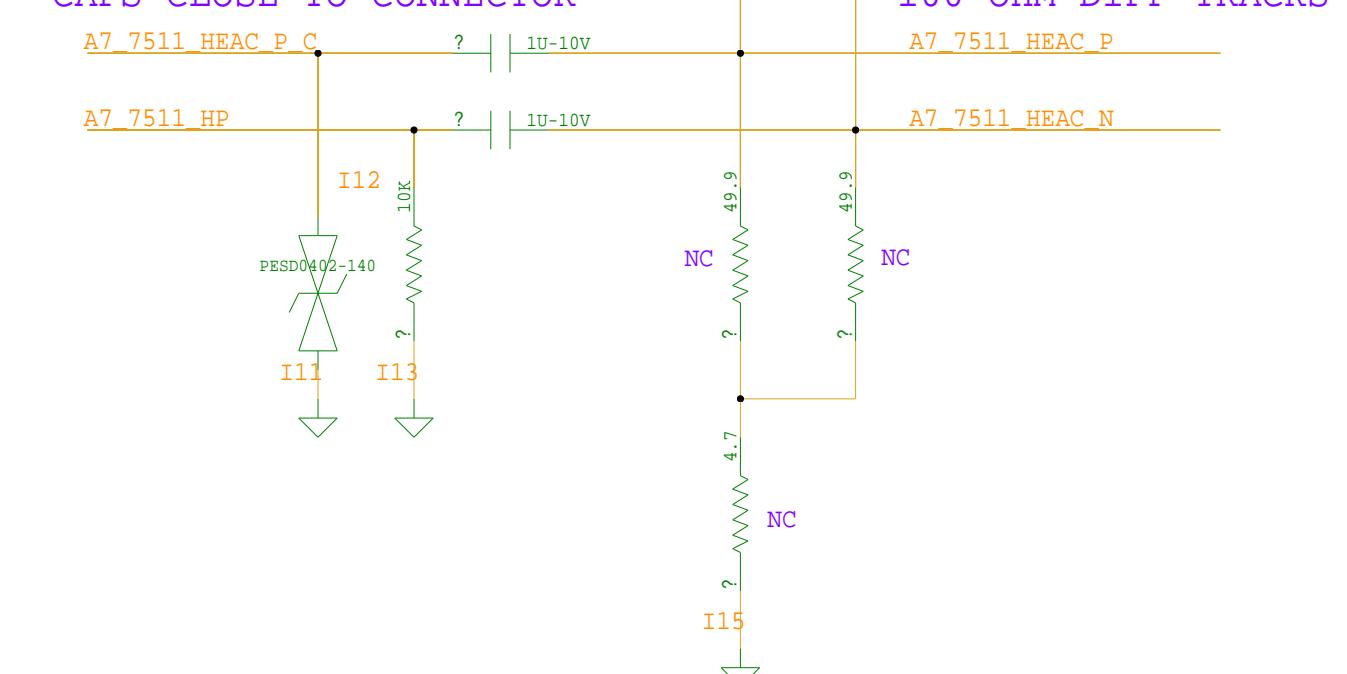


A7_7511_CEC

IN4148

? 27.4K V_A7_3V3_7511_MVDD

CAPS CLOSE TO CONNECTOR



A7_7511_SCL

? 1.8K-1% V_A7_7511_5V0

A7_7511_SDA

? 1.8K-1%

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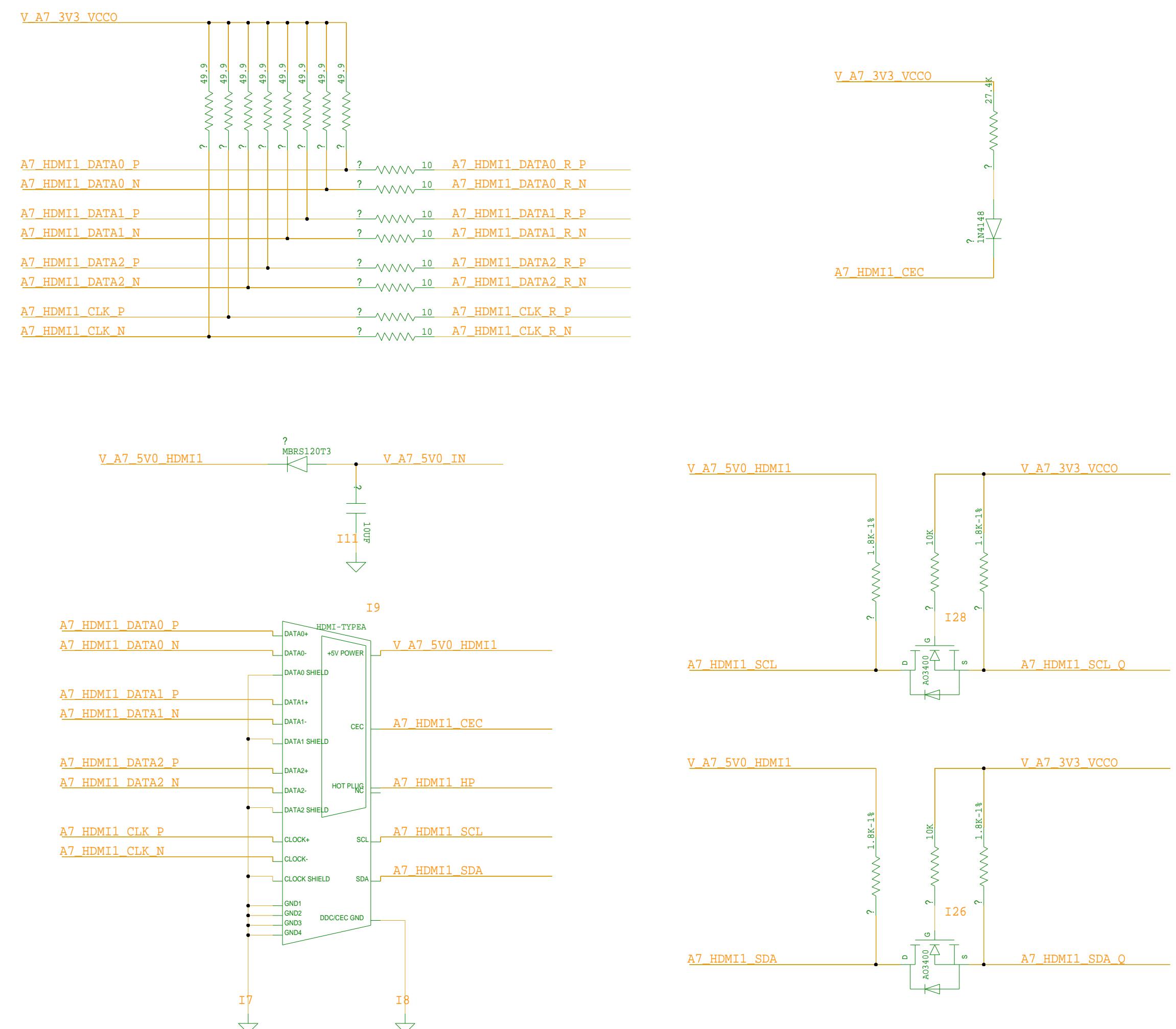
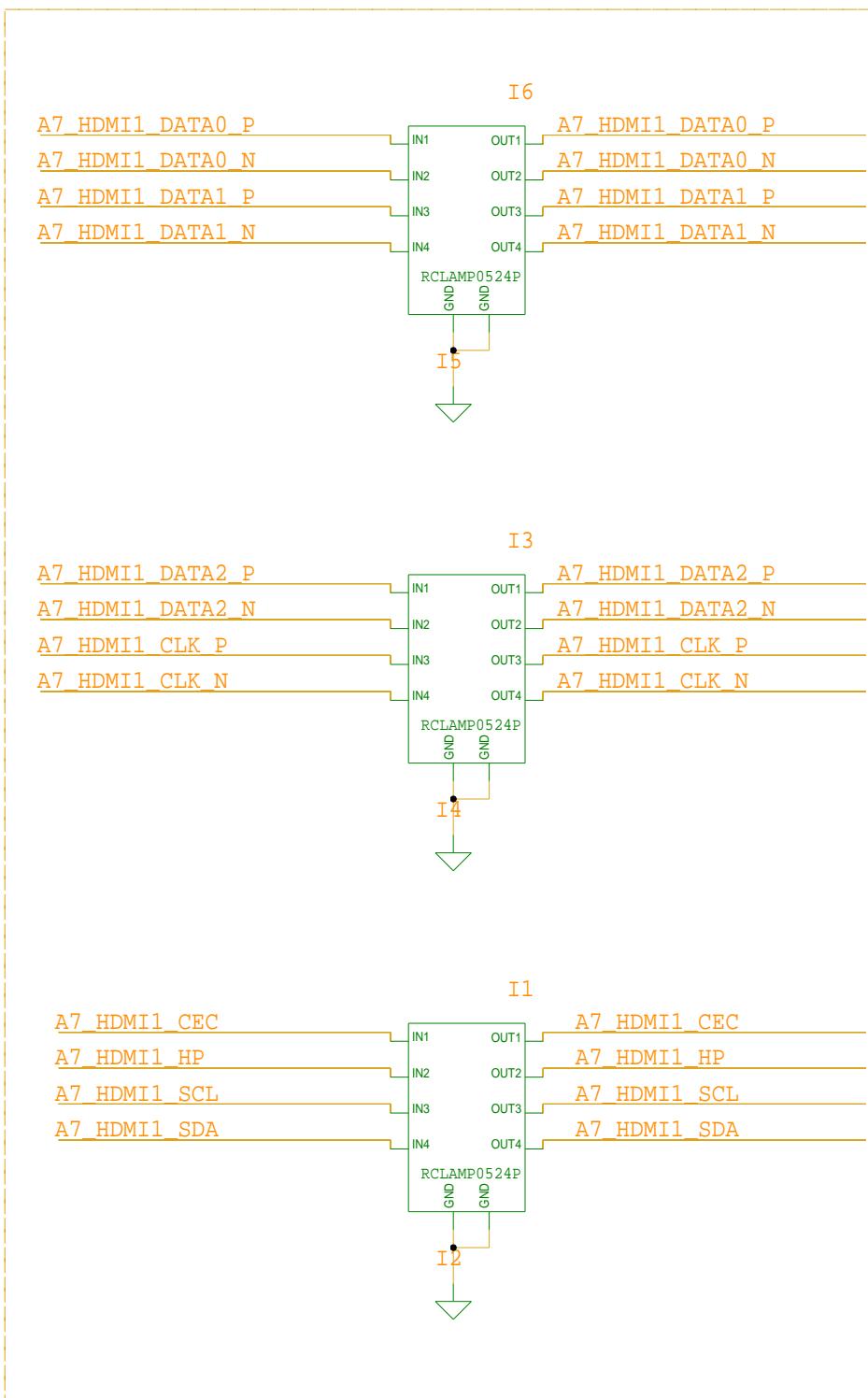
OF

REVISIONS

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ARTIX-7 HDMI INOUT (1)

CHANGE CONNECTION DUE TO LAYOUT



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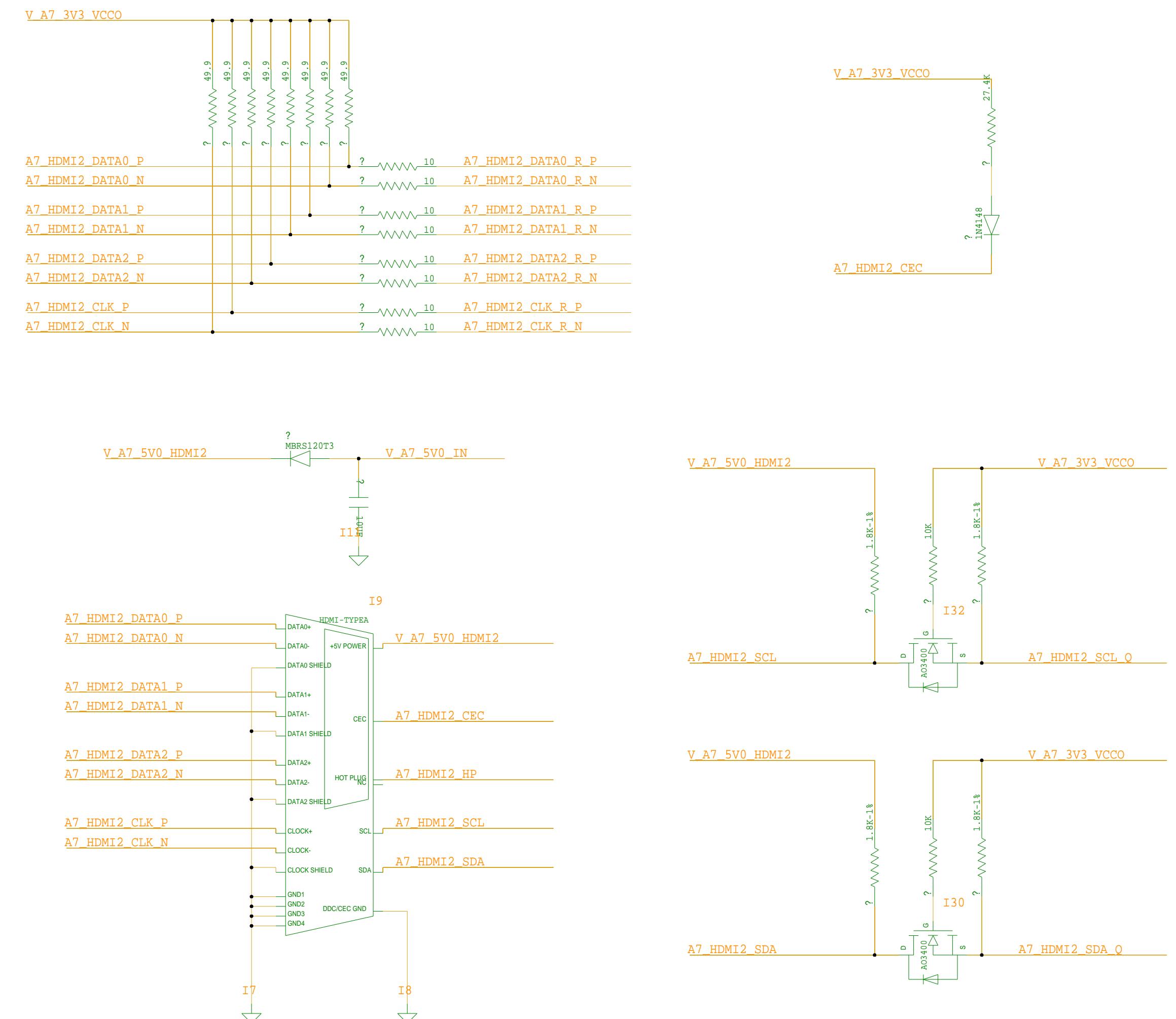
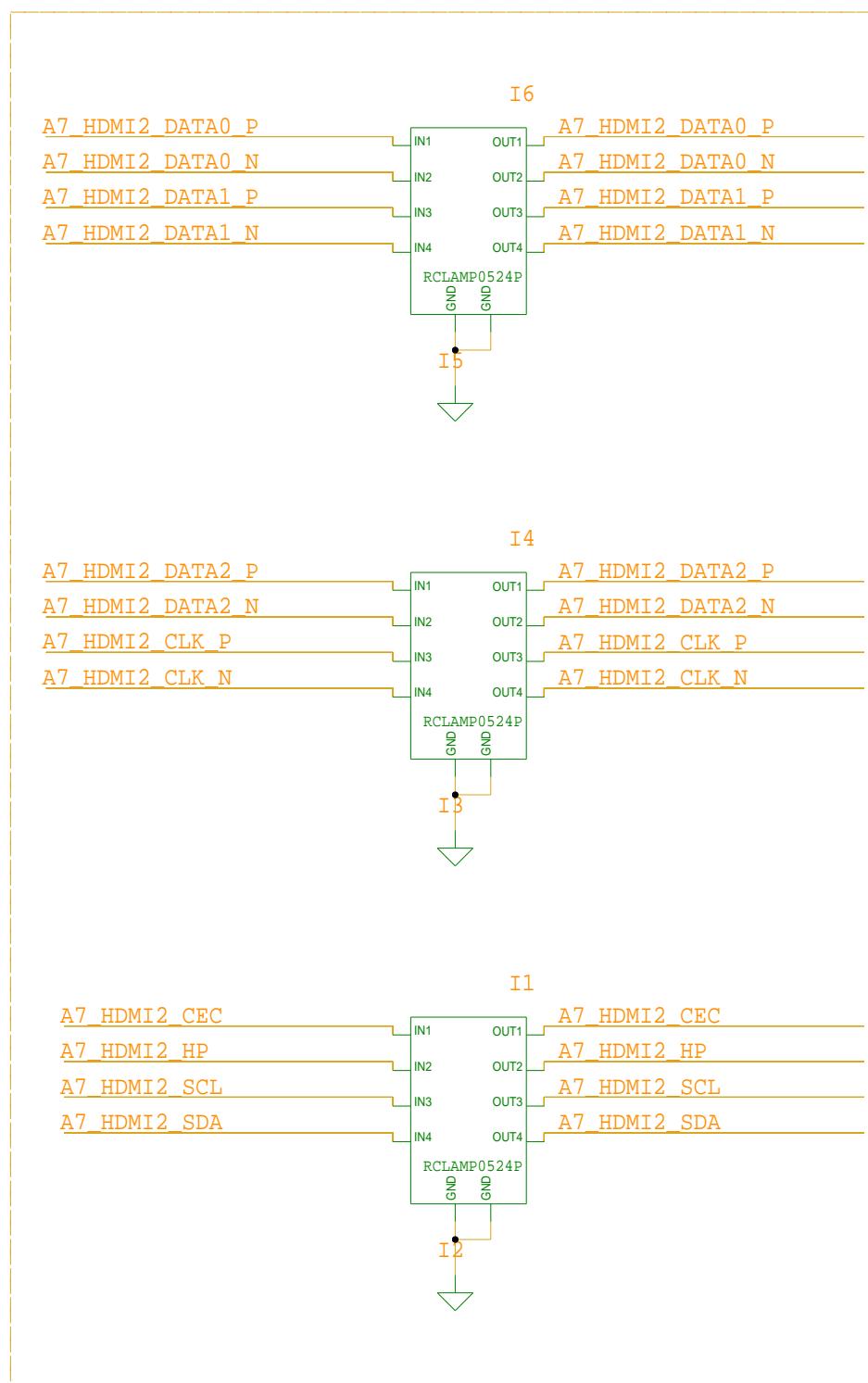
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ARTIX-7 HDMI INOUT (2)

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CHANGE CONNECTION DUE TO LAYOUT



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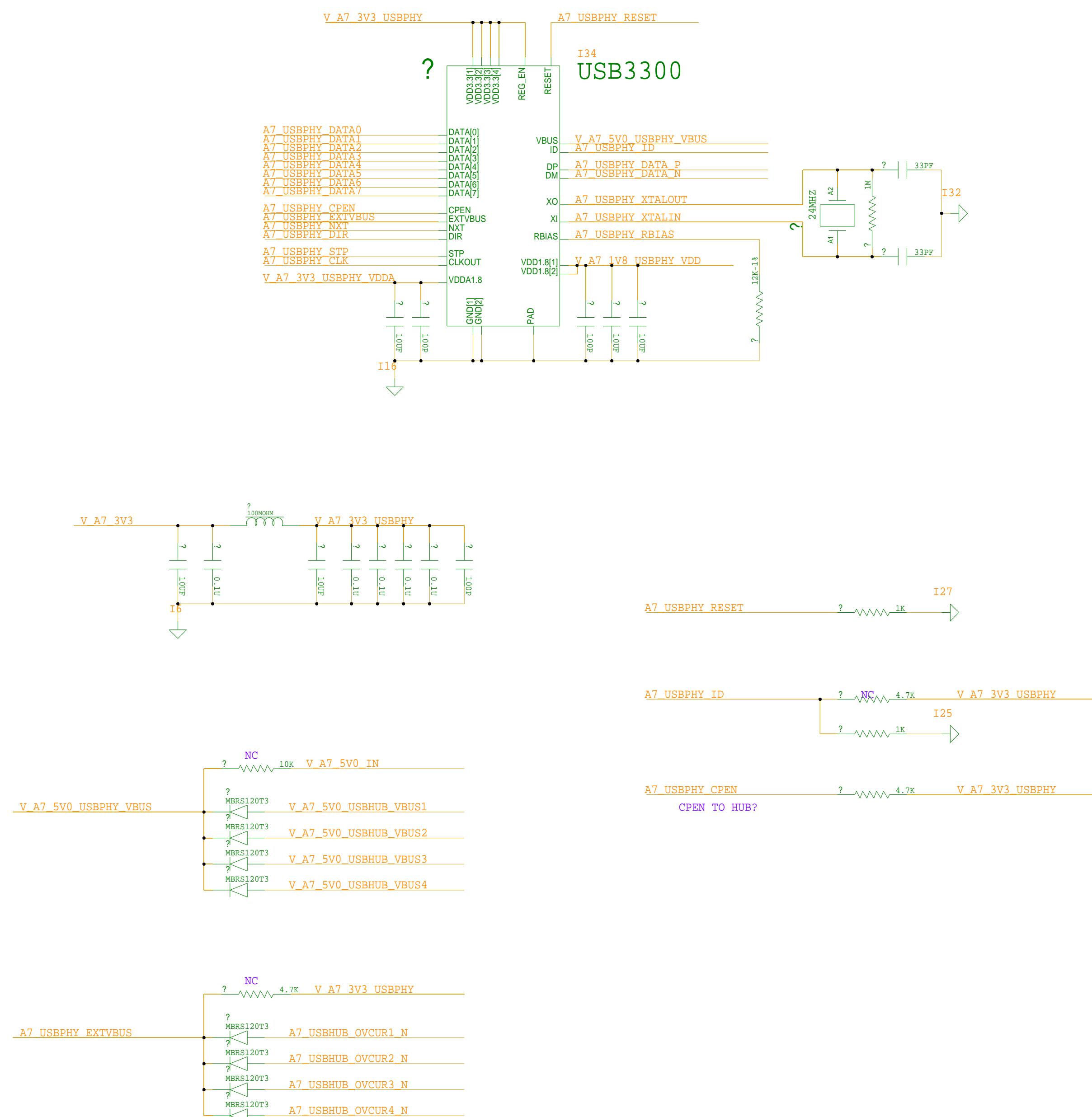
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ARTIX-7 USB PHY (1)

REVISED

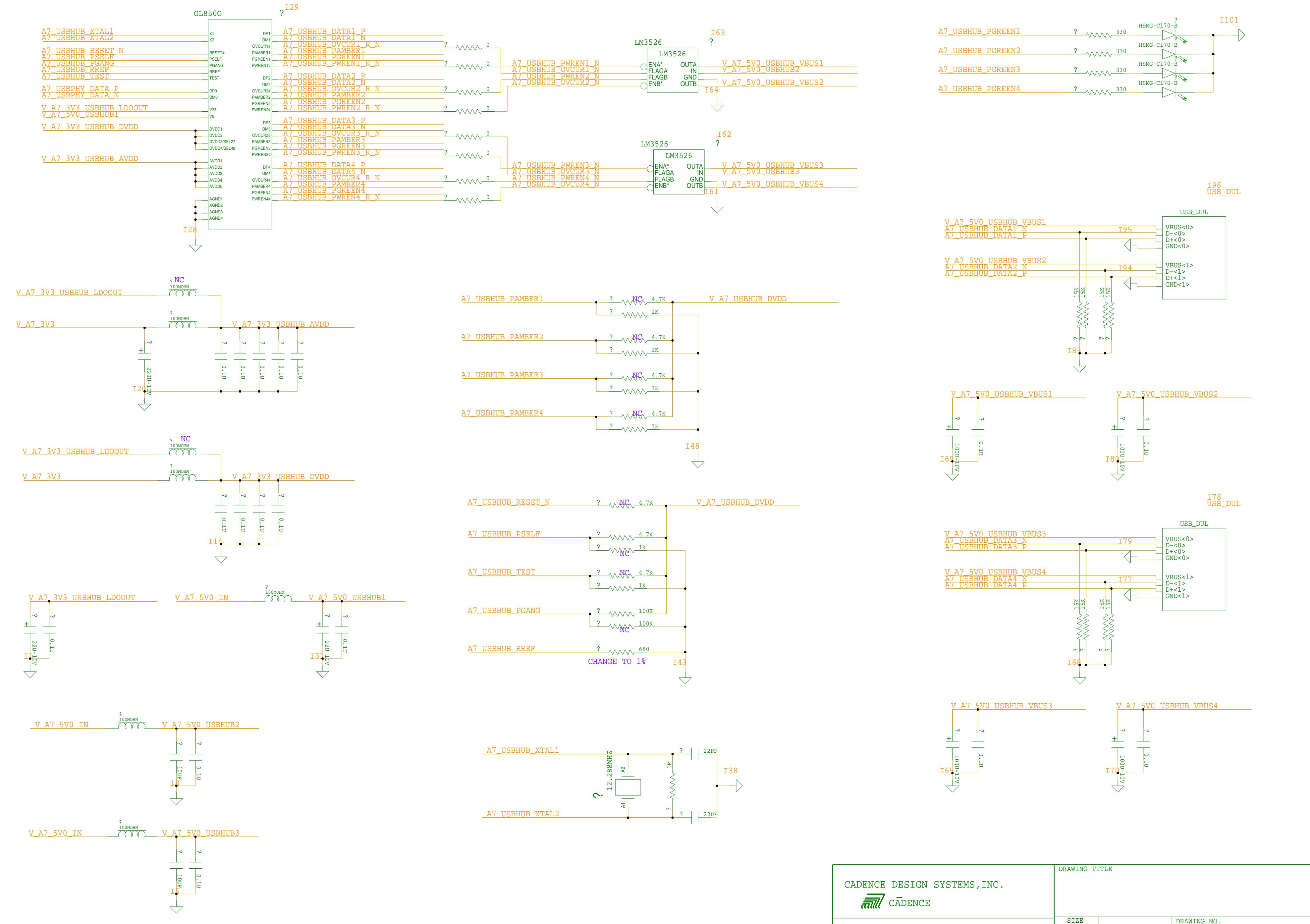
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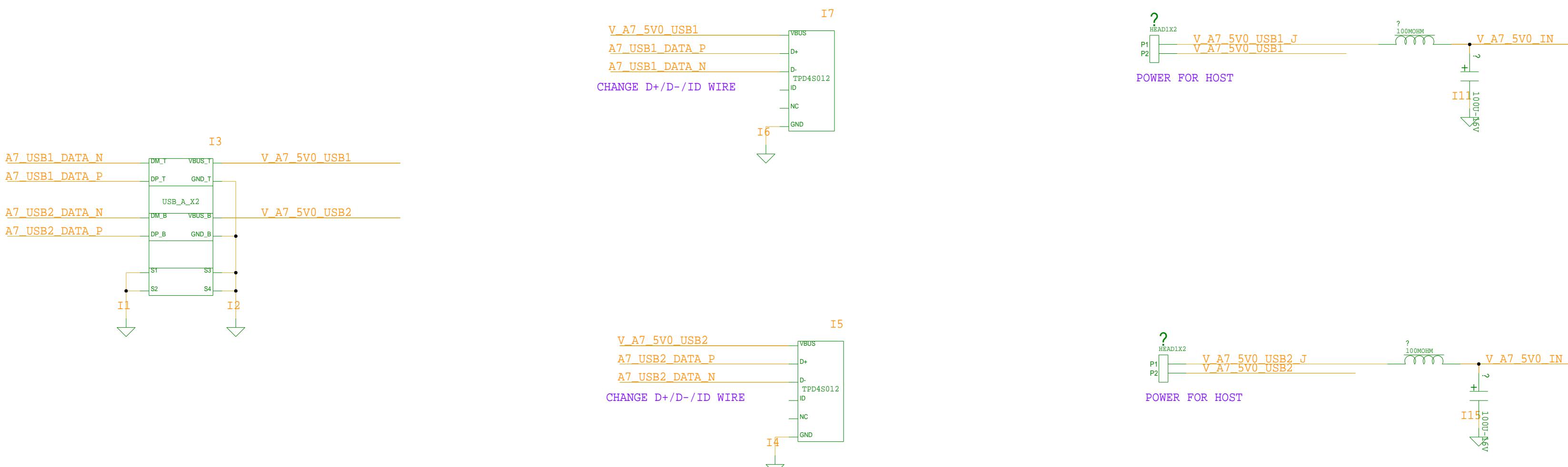
ARTIX-7 USB PHY (2)



ARTIX-7 USB INOUT

REVOLUTIONS

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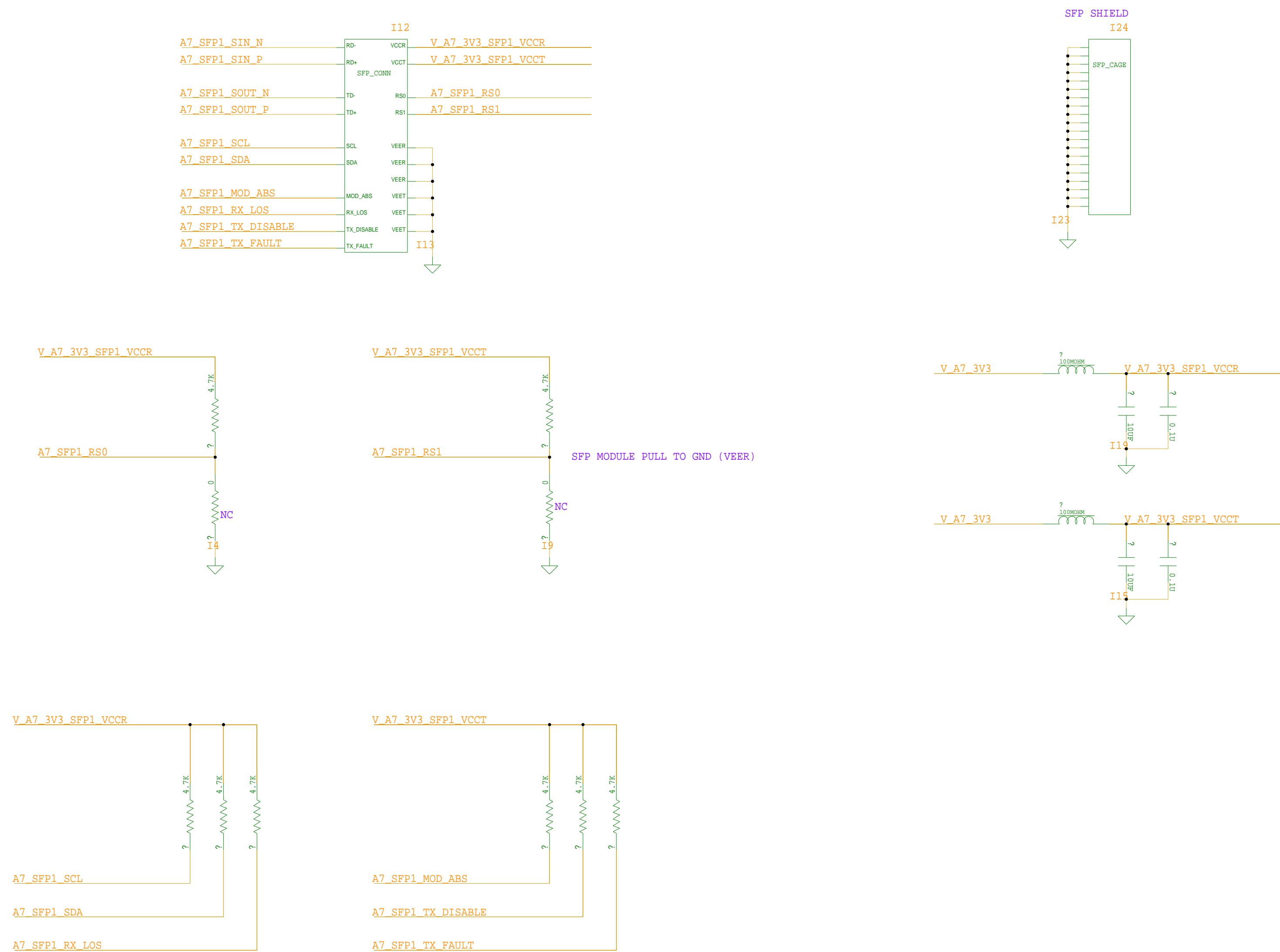
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ARTIX-7 SFP+ / SFP INOUT (1)



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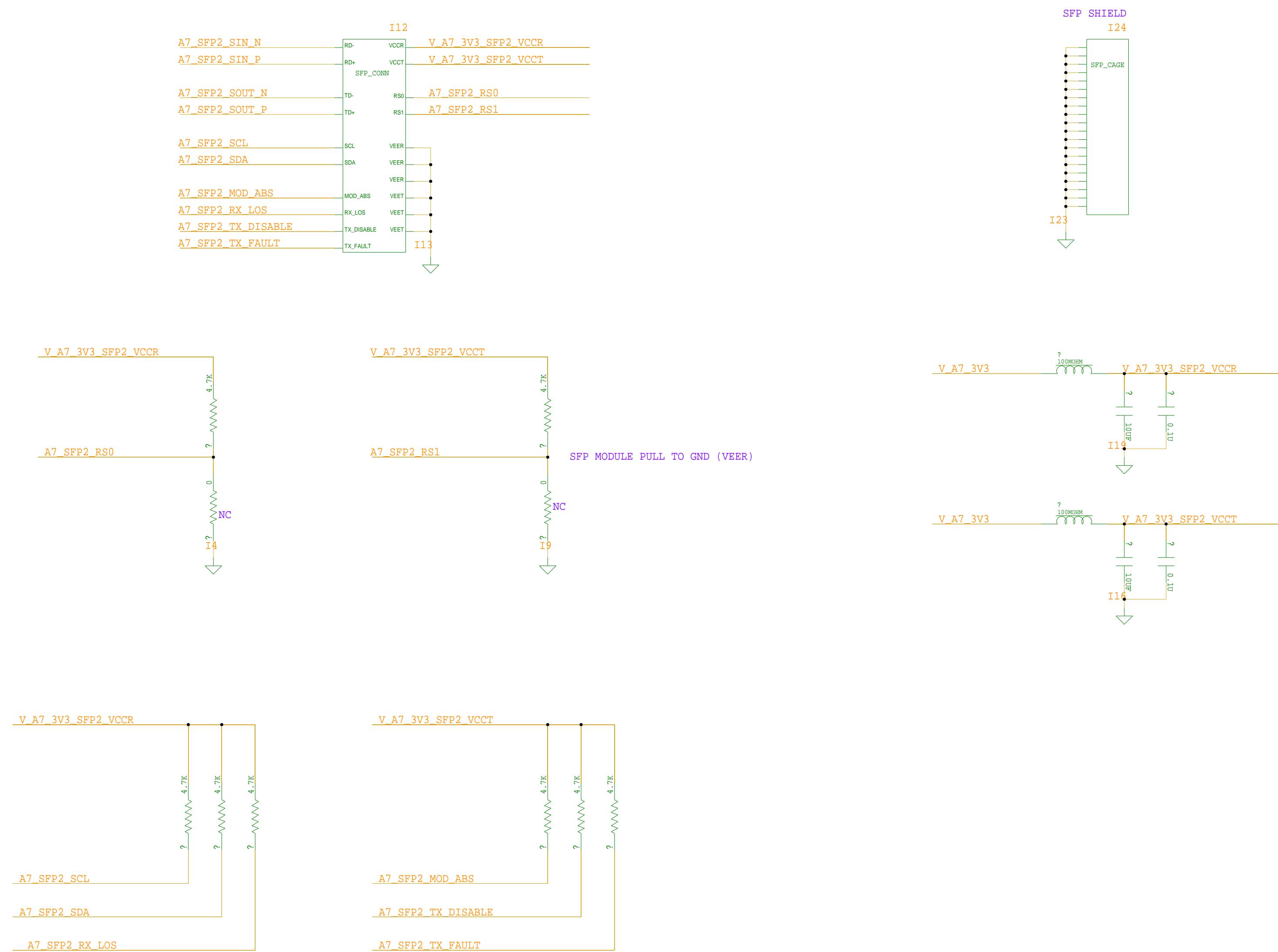
Figure 1. A schematic diagram of the experimental setup.

1

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ARTIX-7 SFP+/SFP INOUT (2)



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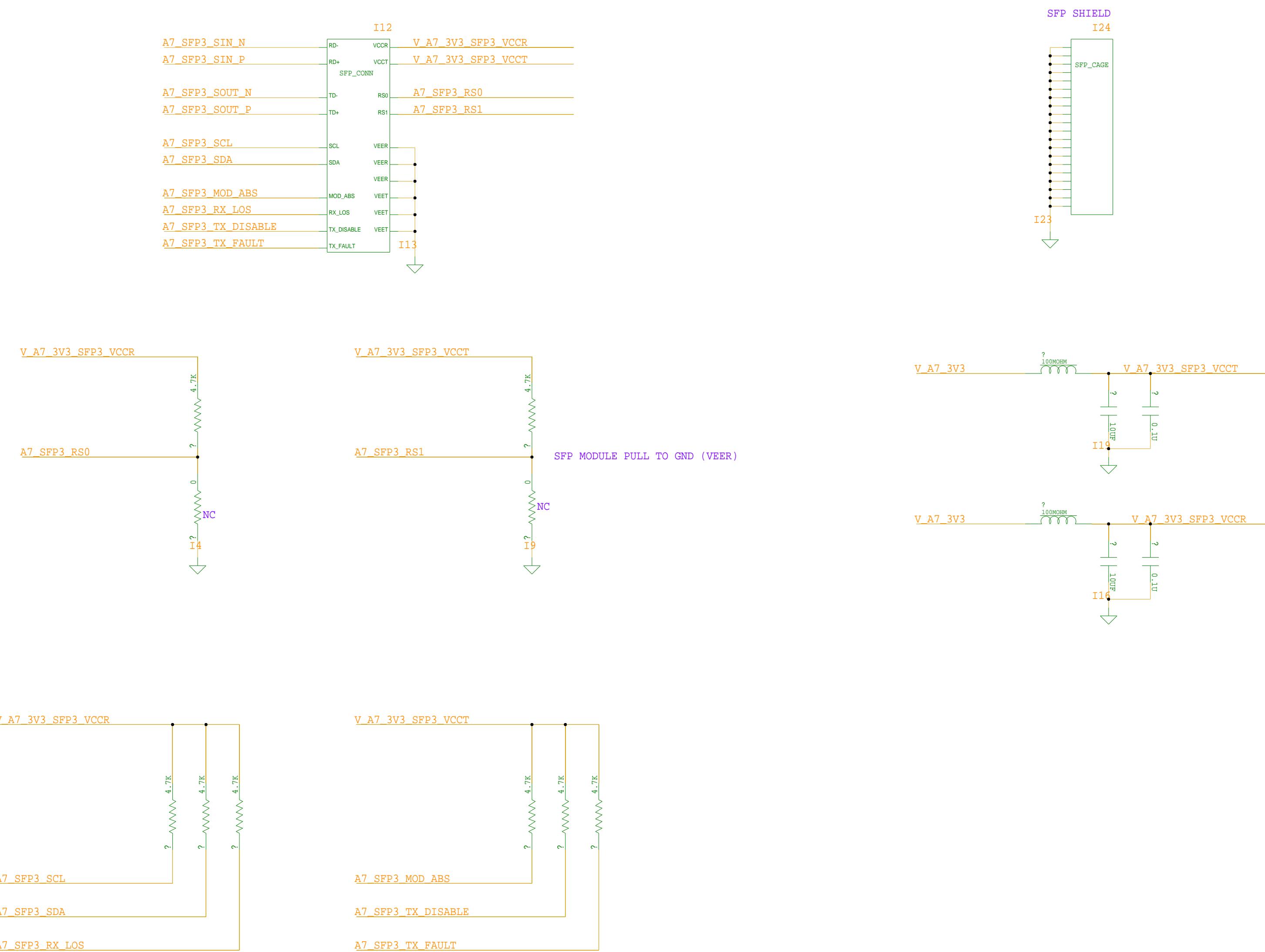
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ARTIX-7 SFP+/SFP INOUT (3)

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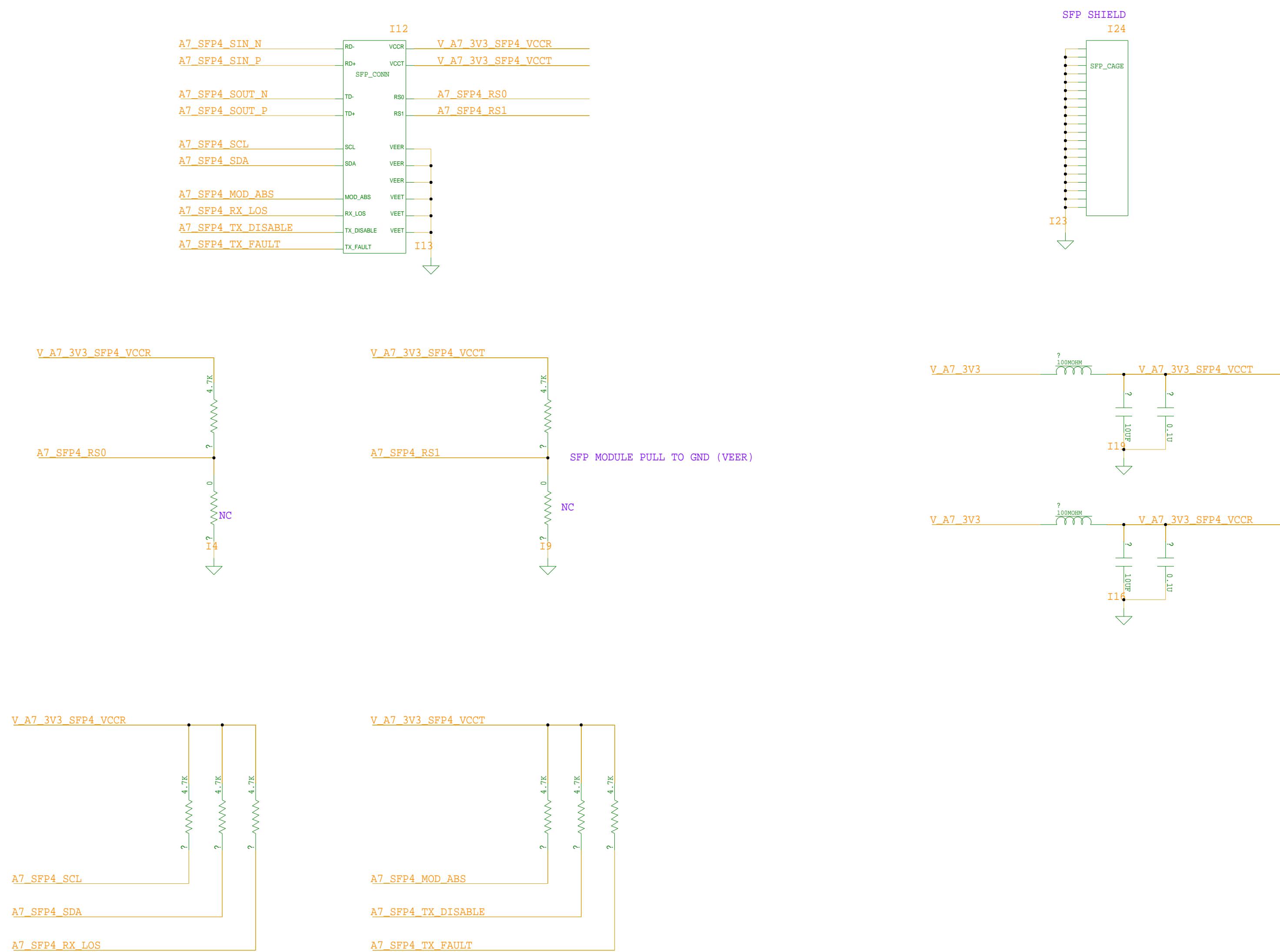
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ARTIX-7 SFP+/SFP INOUT (4)



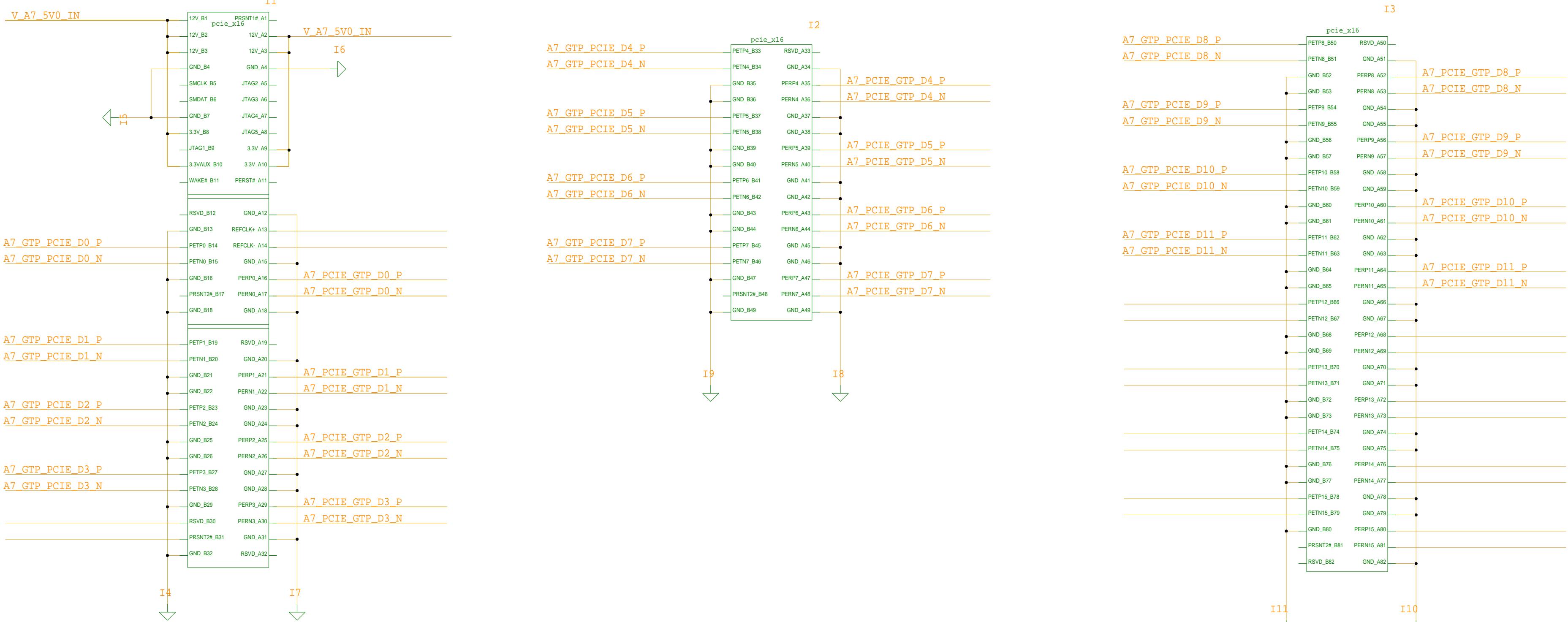
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ARTIX-7 PCIE X16 CONN

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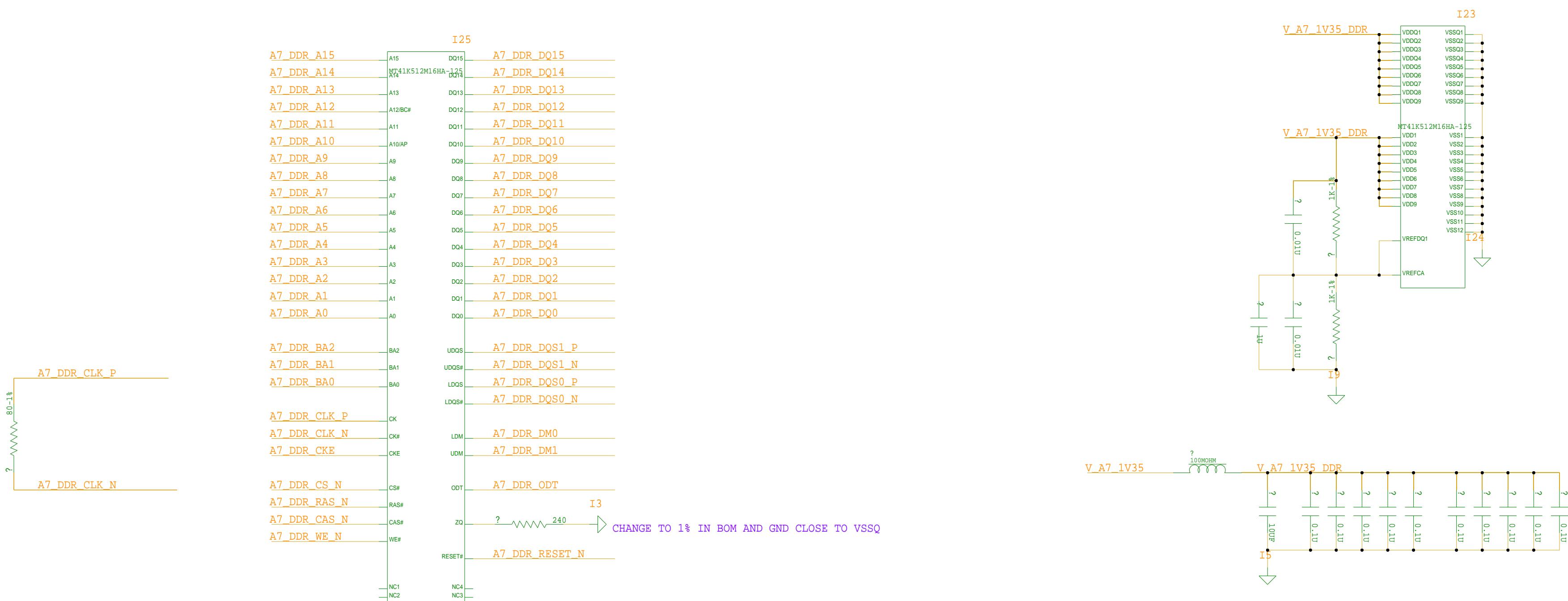
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ARTIX-7 DDR3

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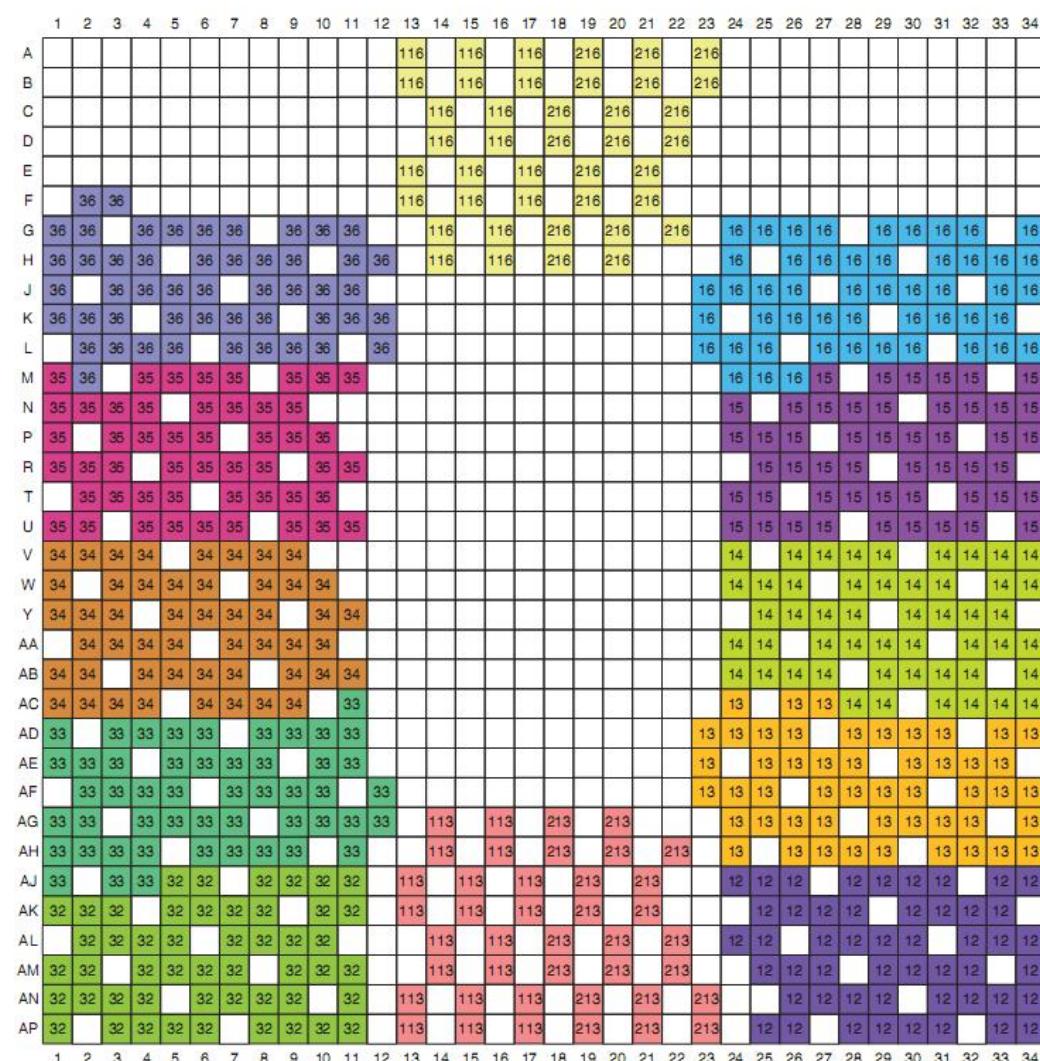


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ARTIX-7 PINOUT MAP

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BANK0 : 3.3V CONFIG

BANK36 : 3.3V USB INOUT 1/2 SFP+ MUX

BANK35 : 3.3V NC

BANK34 : 1.35V DDR3

BANK33 : 3.3V USB PHY

BANK32 : 3.3V NC

BANK116 : 3.3V PCIE X4

BANK216 : 3.3V SFP+ *4

BANK113 : 3.3V PCIE X4

BANK213 : 3.3V PCIE X4

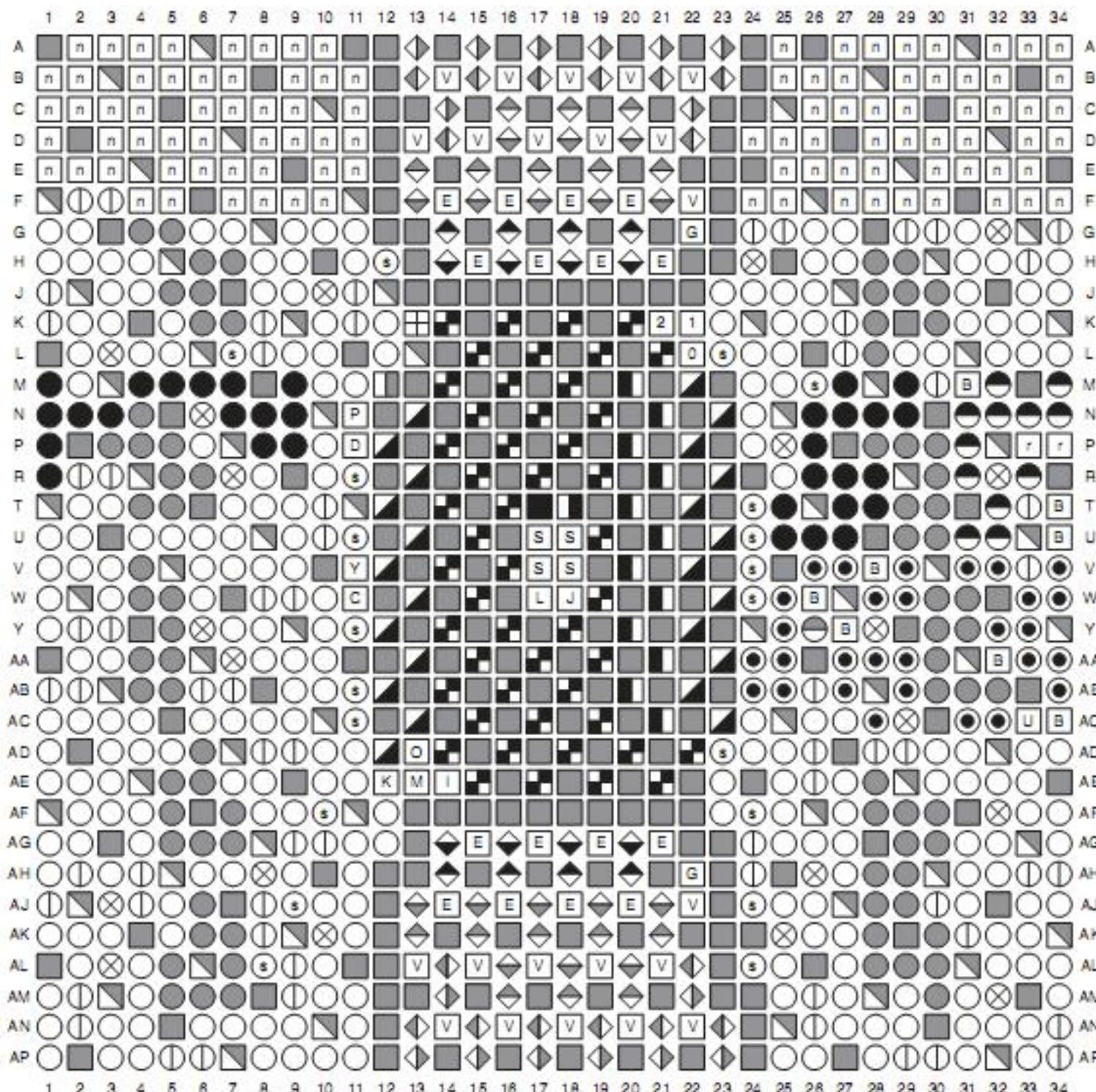
BANK16 : 3.3V NC

BANK15 : 3.3V HDMI RECEIVER

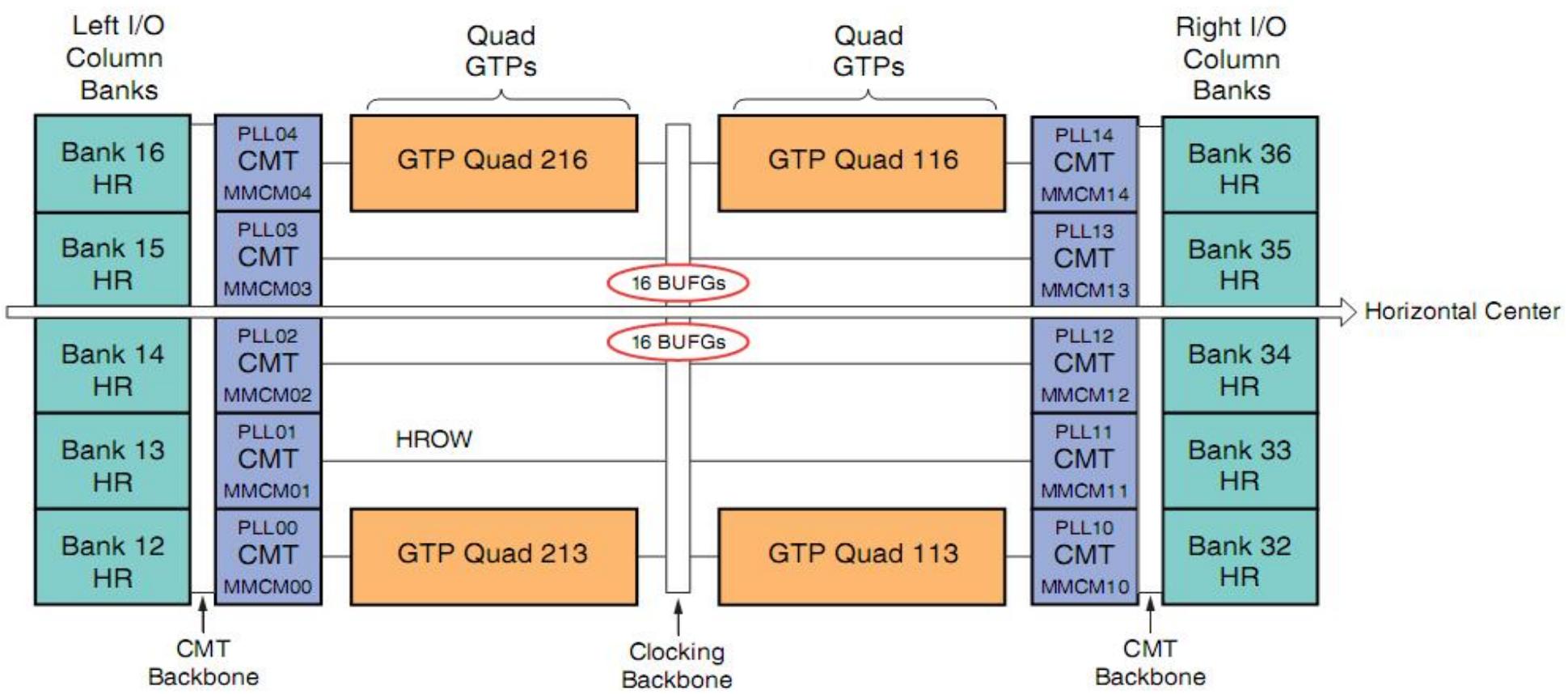
BANK14 : 3.3V SPI FLASH

BANK13 : 3.3V HDMI INOUT 1/2

BANK12 : 3.3V HDMI TRANSMITTER



All HR I/O banks and the GTP Quads are fully bonded out in this package.



User I/O Pins	Transceiver Pins	Dedicated Pins	Other Pins
○ IO_LXXY_# ● IO_XX_#	E MGTAVCC_G# V MGTAVTT_G# A MGTVCVAUX_G# ◀ MGTAVTTRCAL G MGTREFREF B ADV_B B FCS_B B FOE_B B MOSI B FWE_B B DOUT_CSO_B B CSI_B B PUDC_B U RDWR_B r RSD-RS1 ● ADDP/ADON-AD15P/AD15N ● EMCCLK	C CCLK_0 V CFGBVS_0 A DONE_0 ◀ MGTAVTTRCAL J DXP_0 L DXN_0 ■ GNDADC_0 Y INIT_B_0 O M0_0 1 M1_0 2 M2_0 P PROGRAM_B_0 K TCK_0 I TDI_0 O TDO_0 M TMS_0 ■ VCCADC_0 ■ VCCBATT_0	■ GND ■ VCCAUX_IO_G# ■ VCCAUX ■ VCCINT ■ VCCO_# ■ VCCBRAM n NC
Multi-Function Pins			
B FCS_B B FOE_B B MOSI B FWE_B B DOUT_CSO_B B CSI_B B PUDC_B U RDWR_B r RSD-RS1 ● ADDP/ADON-AD15P/AD15N ● EMCCLK	⊕ VRN ○ VRP ○ VREF ● D00-D31 ● A00-A28 ○ DQS ○ MRCC ● SRCC	E MGTAVCC_G# V MGTAVTT_G# A MGTVCVAUX_G# ◀ MGTAVTTRCAL J DXP_0 L DXN_0 ■ GNDADC_0 Y INIT_B_0 O M0_0 1 M1_0 2 M2_0 P PROGRAM_B_0 K TCK_0 I TDI_0 O TDO_0 M TMS_0 ■ VCCADC_0 ■ VCCBATT_0	■ GND ■ VCCAUX_IO_G# ■ VCCAUX ■ VCCINT ■ VCCO_# ■ VCCBRAM n NC

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ARTIX-7 BANK POWER (1)

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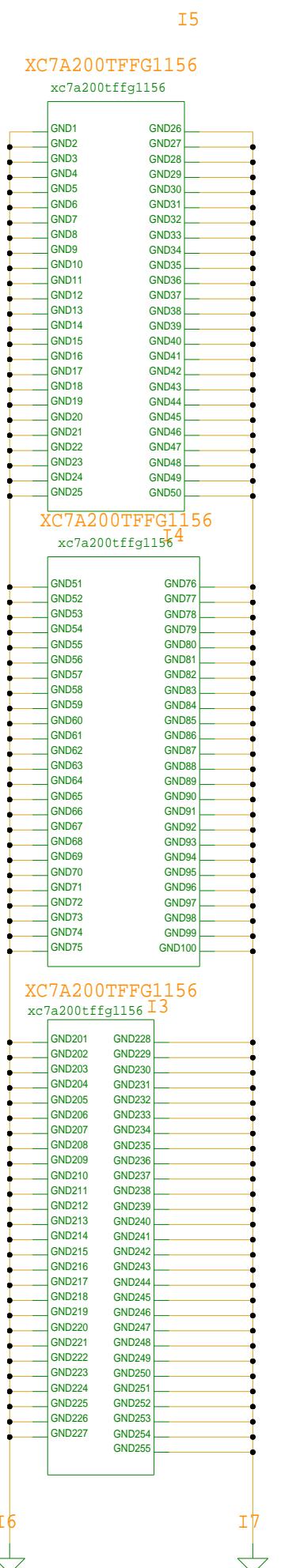
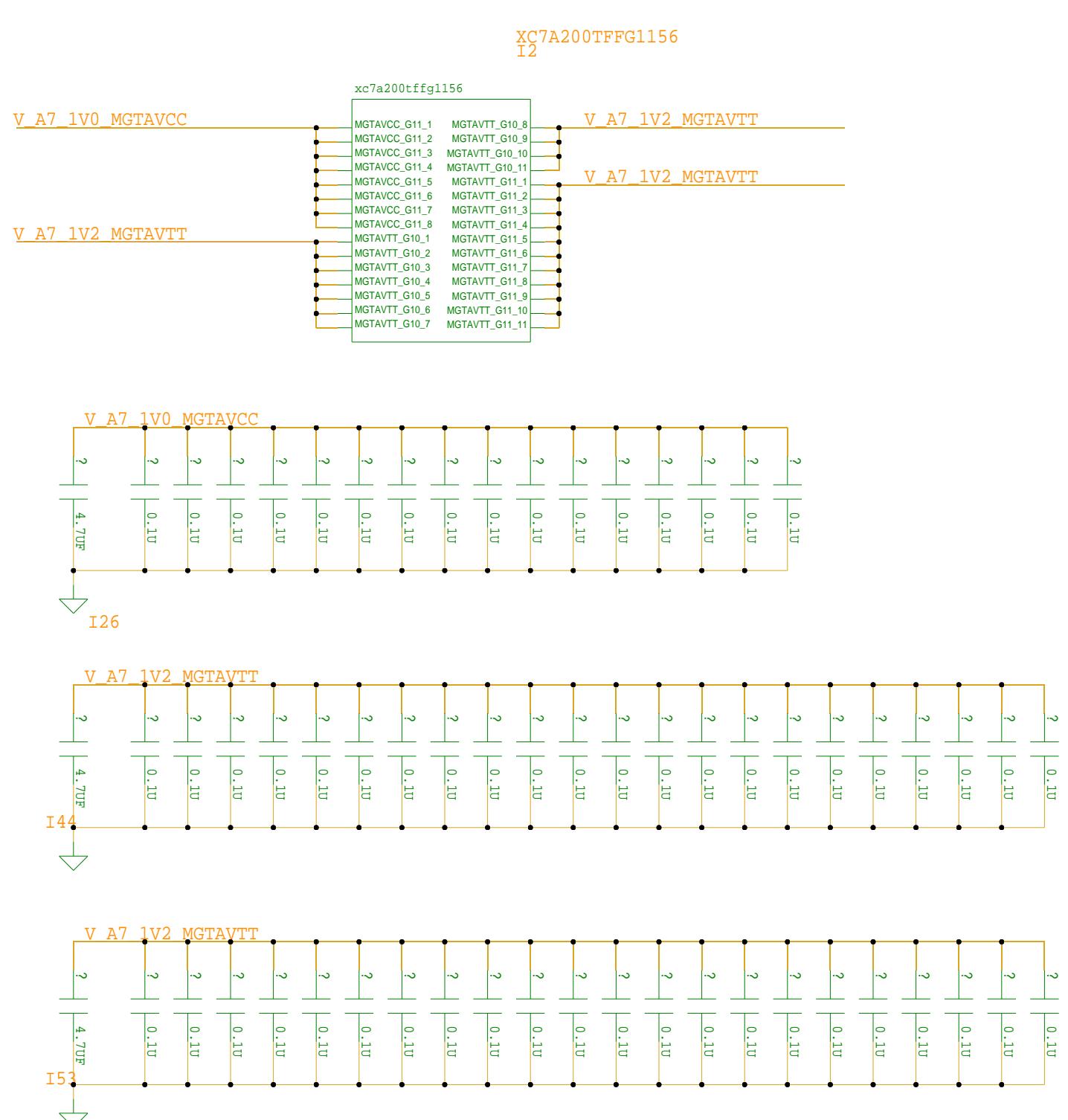
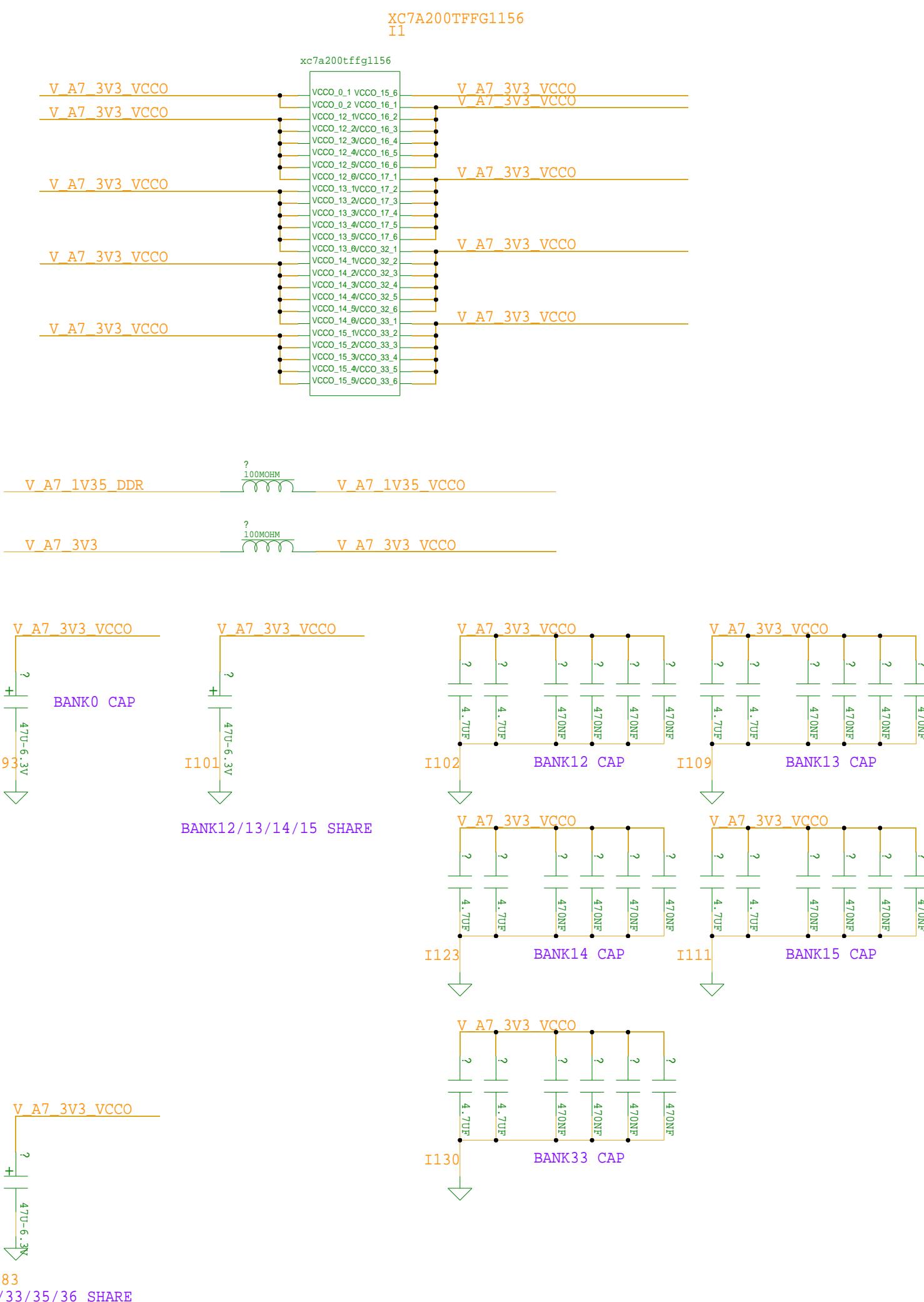
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ARTIX-7 CLOCK

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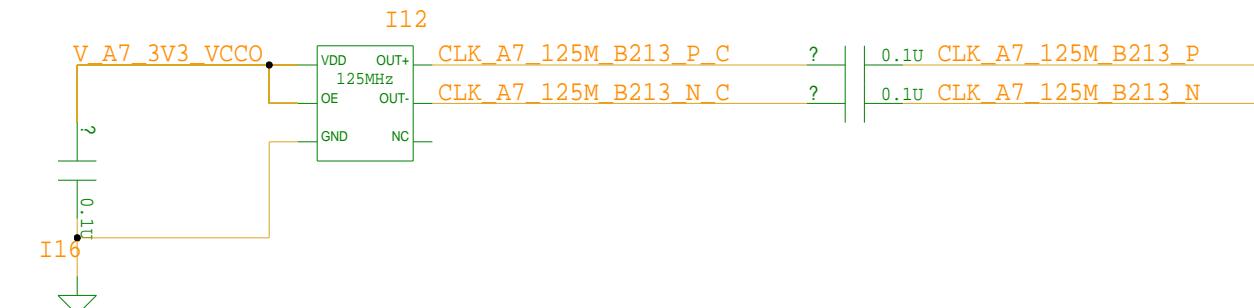
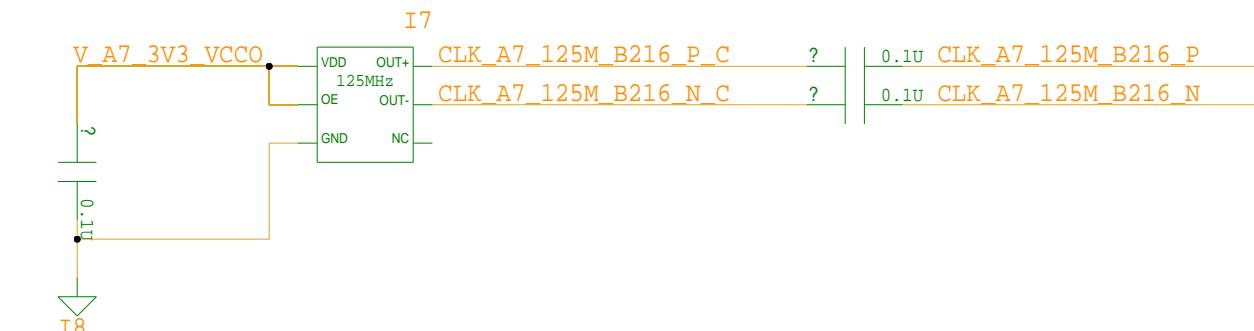
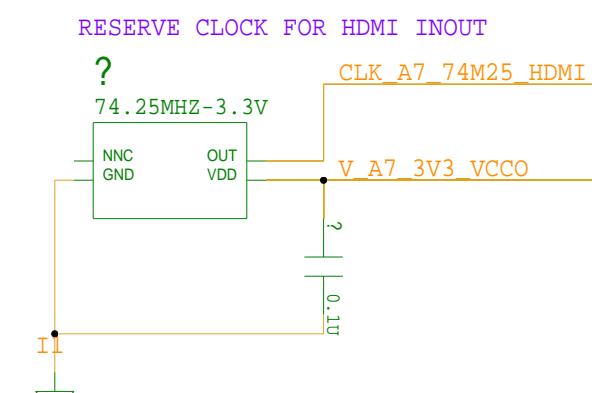
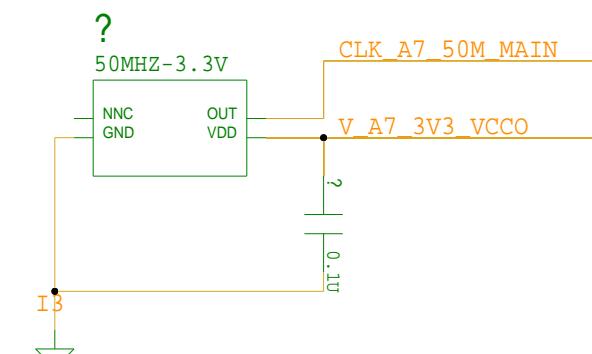
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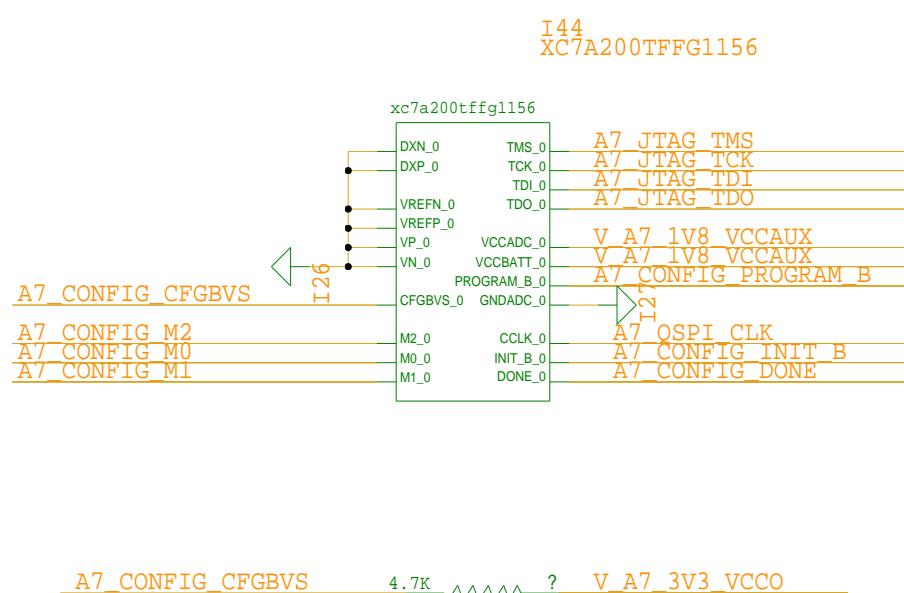
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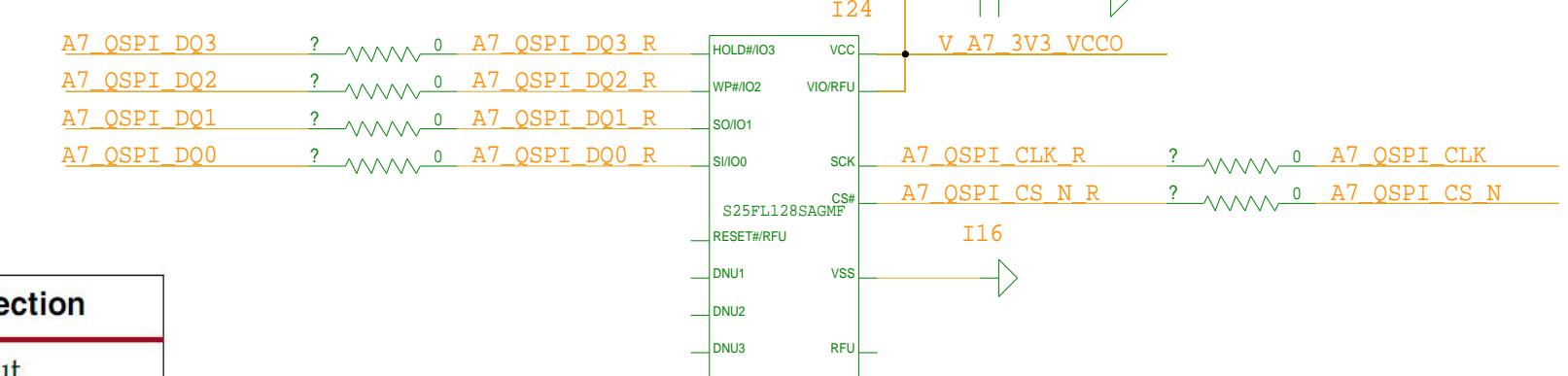
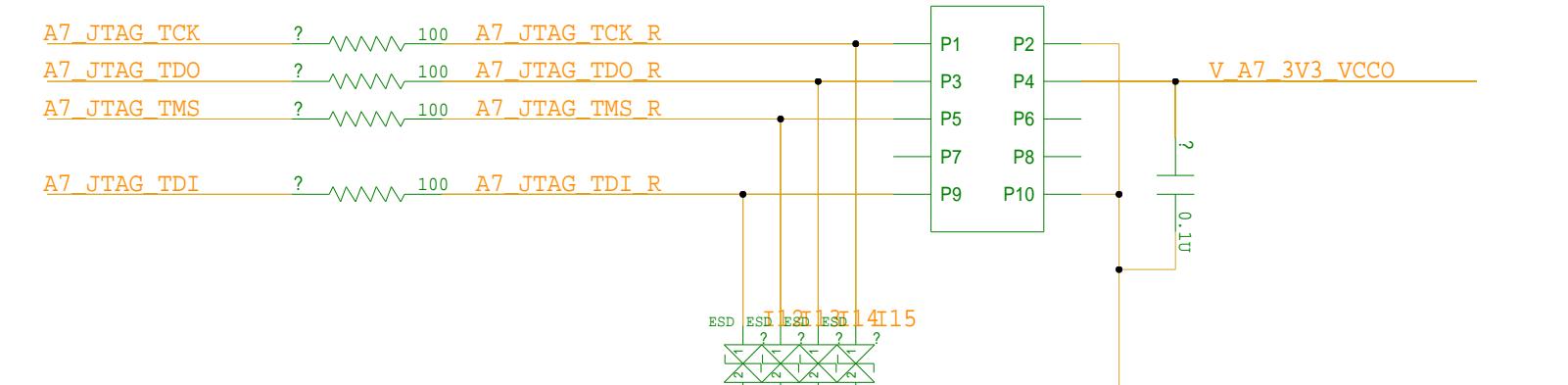
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ARTIX-7 BANK0/14 CONFIG



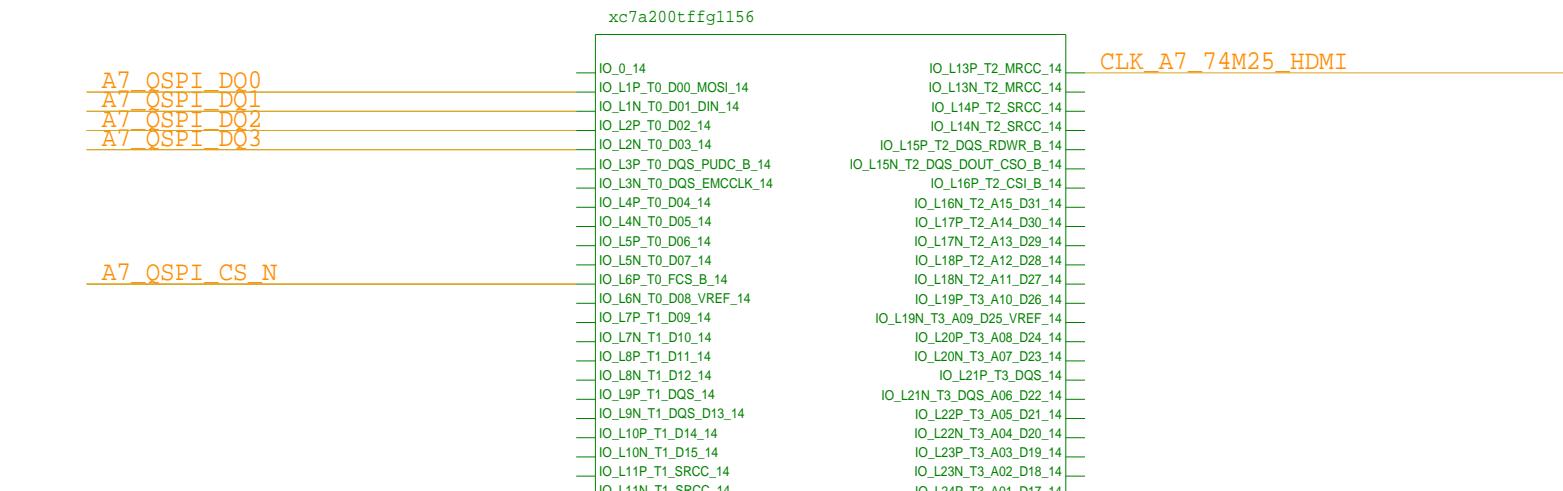
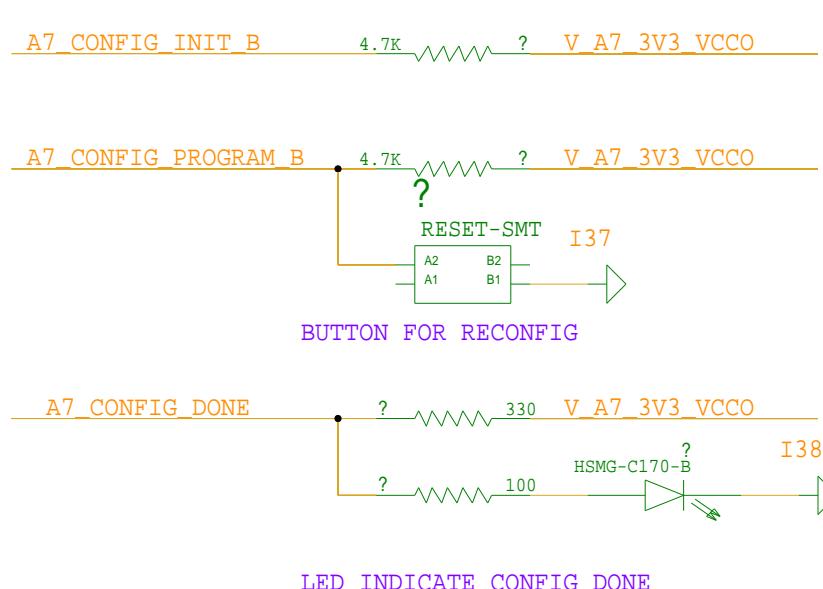
CFGBVS Pin Connection	Supported Configuration Banks 0/14/15 V _{CCO} Supply and I/O Signal Voltages		
	Spartan-7, Artix-7, Kintex-7	Virtex-7 T, XT	Virtex-7 HT
Banks Affected	0, 14, 15	0	none
V _{CCO_0} (3.3V or 2.5V)	3.3V or 2.5V	3.3V or 2.5V	1.8V (no CFGBVS)
GND	1.8V or 1.5V	1.8V or 1.5V	



A7_QSPI_CS_N → 4.7K → ? → V A7 3V3 VCCO

Configuration Mode	M[2:0]	Bus Width	CCLK Direction
Master Serial	000	x1	Output
Master SPI	001	x1, x2, x4	Output
Master BPI	010	x8, x16	Output
Master SelectMAP	100	x8, x16	Output
JTAG	101	x1	Not Applicable
Slave SelectMAP	110	x8, x16, x32 ⁽¹⁾	Input
Slave Serial ⁽²⁾	111	x1	Input

DEFAULT 001 FOR MASTER SPI
101 FOR JTAG(ONLY)
111 FOR SLAVE SERIAL



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ARTIX-7 BANK12

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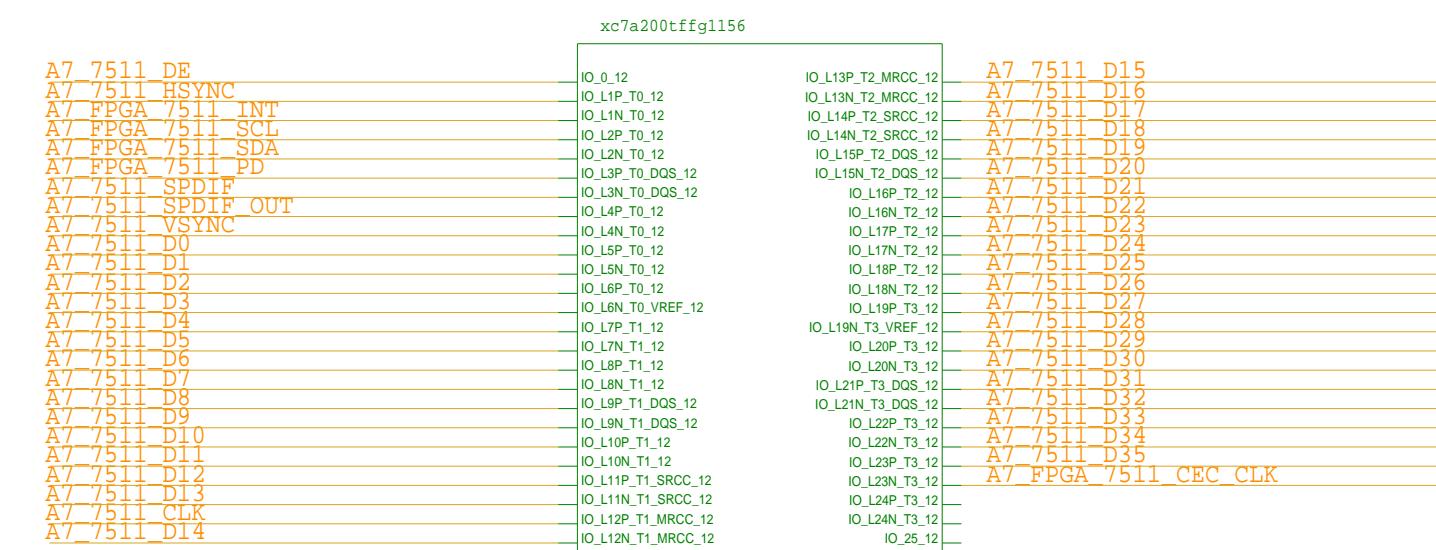
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OD CONFIG AS BELOW:

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A7_FPGA_7511_SDA

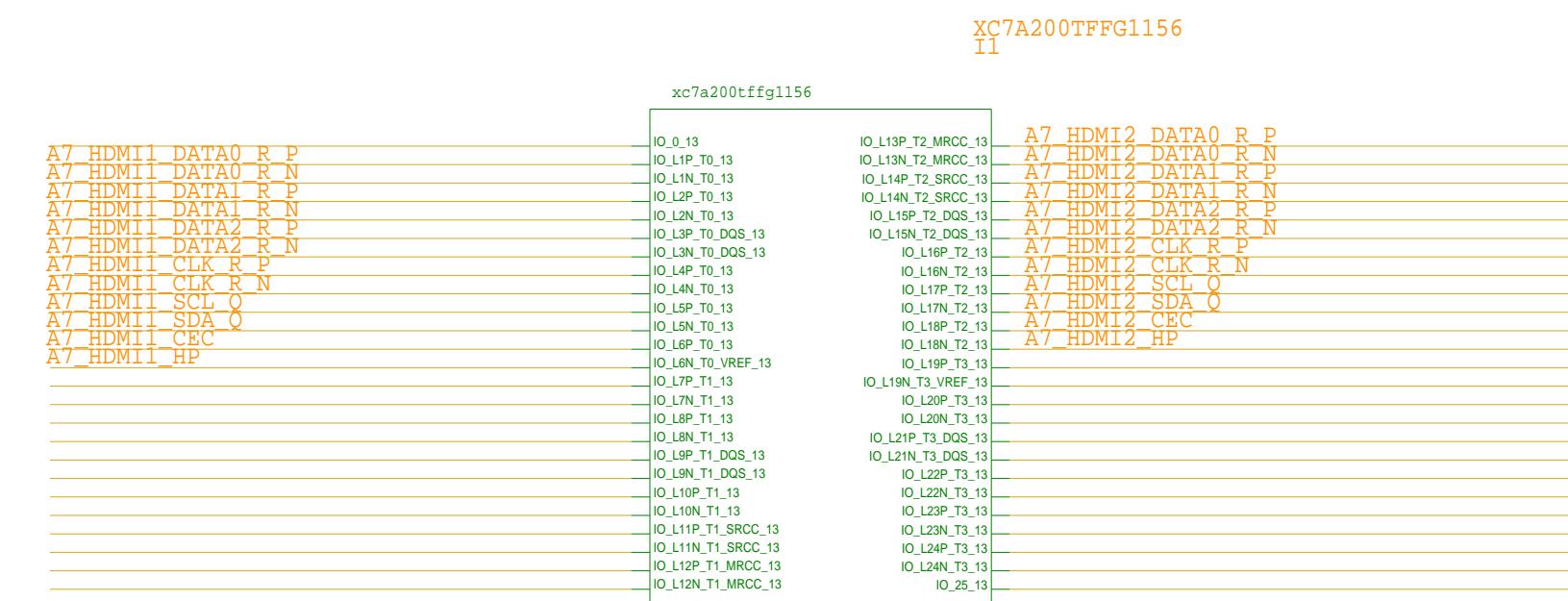
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ARTIX-7 BANK13

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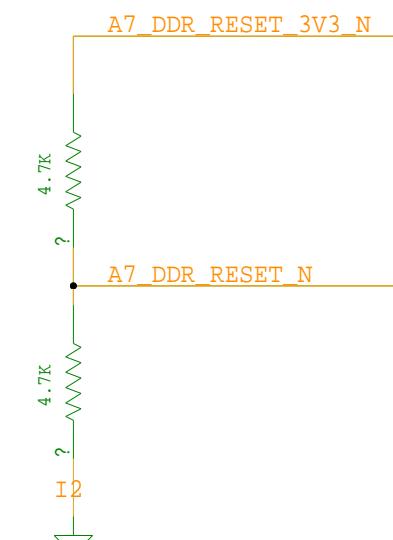
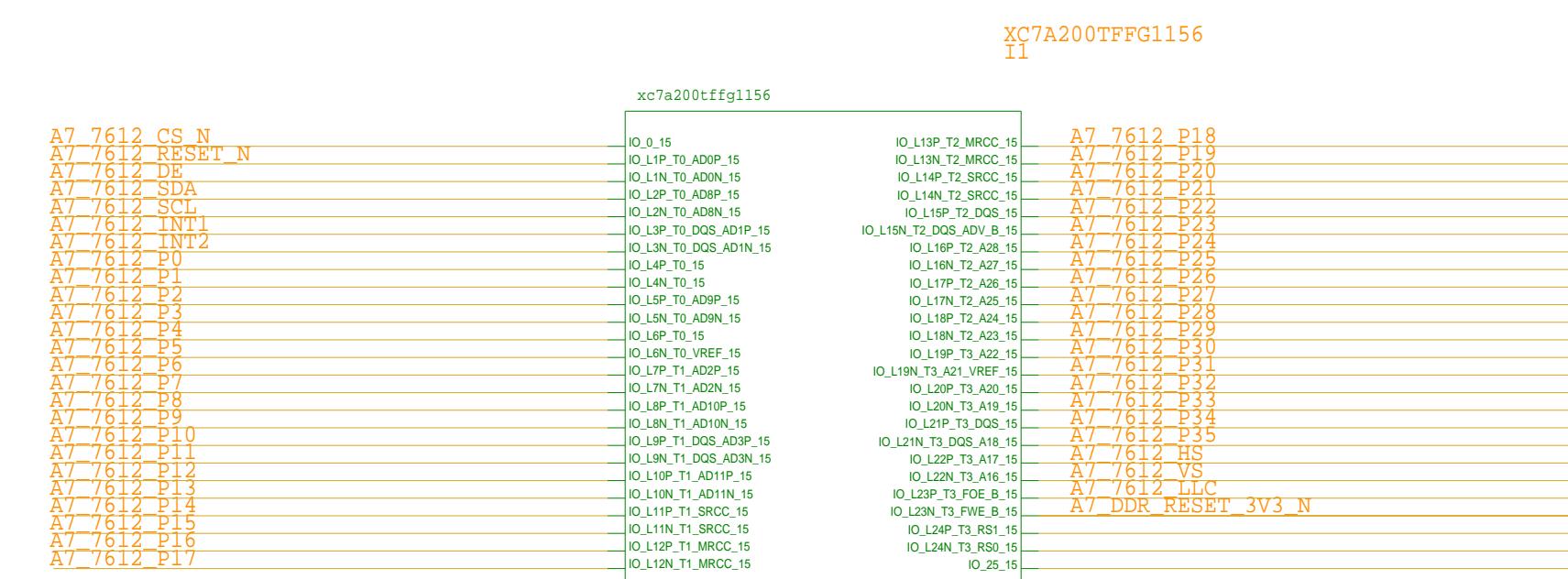
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ARTIX-7 BANK15

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ARTIX-7 BANK32

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IO_0_32	IO_L13P_T2_MRCC_32
IO_L1P_T0_32	IO_L13N_T2_MRCC_32
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IO_L2P_T0_32	IO_L14N_T2_SRCC_32
IO_L2N_T0_32	IO_L15P_T2_DOS_32
IO_L3P_T0_DQS_32	IO_L15N_T2_DQS_32
IO_L3N_T0_DQS_32	IO_L16P_T2_32
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IO_L12N_T1_MRCC_32	IO_25_32

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ARTIX-7 BANK NC

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NC_4	NC_29
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ARTIX-7 BANK32

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IO_L1N_T0_32	IO_L14P_T2_SRCC_32
IO_L2P_T0_32	IO_L14N_T2_SRCC_32
IO_L2N_T0_32	IO_L15P_T2_DOS_32
IO_L3P_T0_DQS_32	IO_L15N_T2_DQS_32
IO_L3N_T0_DQS_32	IO_L16P_T2_32
IO_L4P_T0_32	IO_L16N_T2_32
IO_L4N_T0_32	IO_L17P_T2_32
IO_L5P_T0_32	IO_L17N_T2_32
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IO_L8N_T1_32	IO_L21P_T3_DQS_32
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IO_L11P_T1_SRCC_32	IO_L23N_T3_32
IO_L11N_T1_SRCC_32	IO_L24P_T3_32
IO_L12P_T1_MRCC_32	IO_L24N_T3_32
IO_L12N_T1_MRCC_32	IO_25_32

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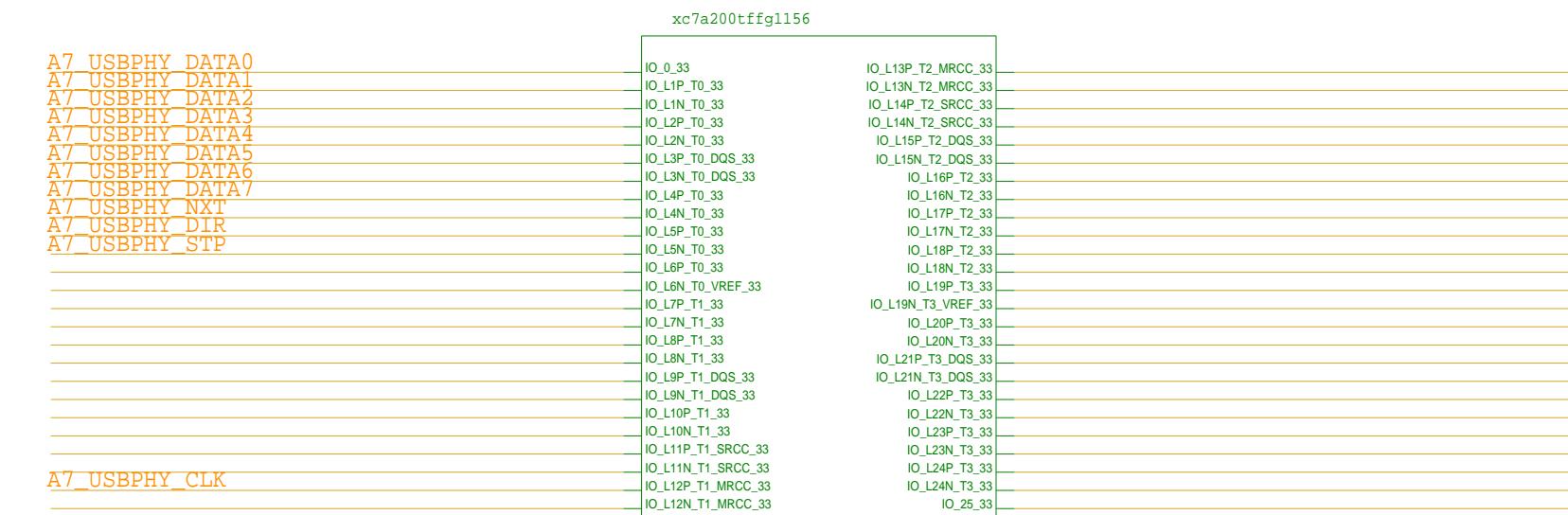
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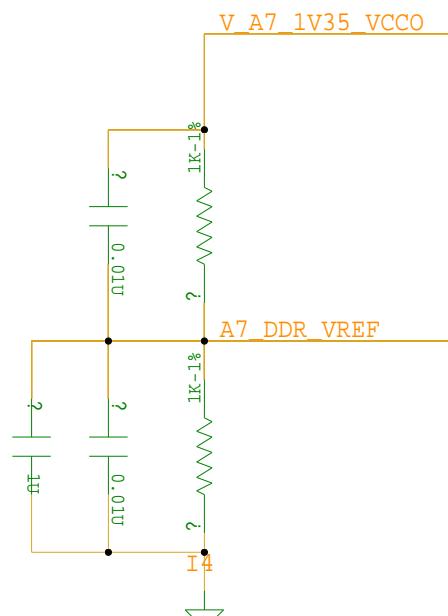
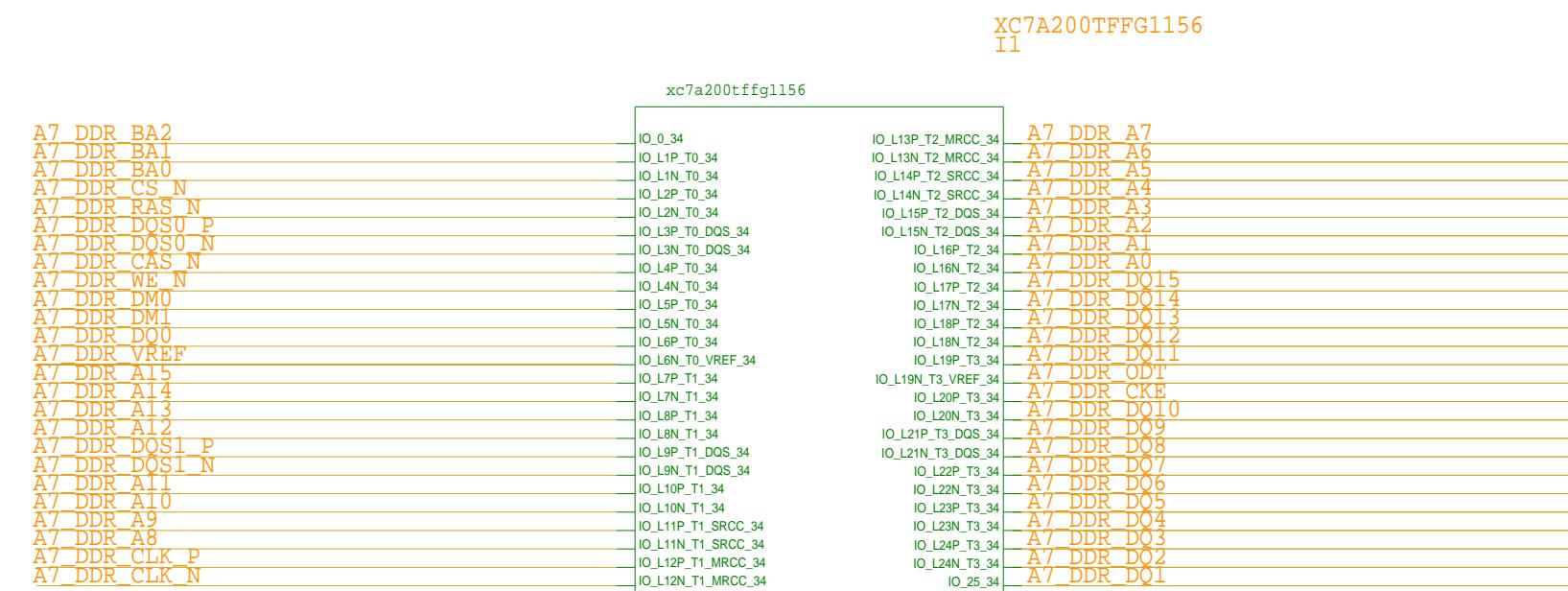
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ARTIX-7 BANK35

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IO_0_35	IO_L13P_T2_MRCC_35
IO_L1P_T0_AD4P_35	IO_L13N_T2_MRCC_35
IO_L1N_T0_ADN_35	IO_L14P_T2_SRCC_35
IO_L2P_T0_ADI2P_35	IO_L14N_T2_SRCC_35
IO_L2N_T0_ADI2N_35	IO_L16P_T2_DOS_35
IO_L3P_T0_DOS_ADS5_35	IO_L18P_T2_DOS_35
IO_L4N_T0_DOS_ADS5N_35	IO_L18P_T2_35
IO_L5P_T0_35	IO_L18N_T2_35
IO_L6N_T0_35	IO_L17P_T2_35
IO_L8P_T0_ADI3P_35	IO_L17N_T2_35
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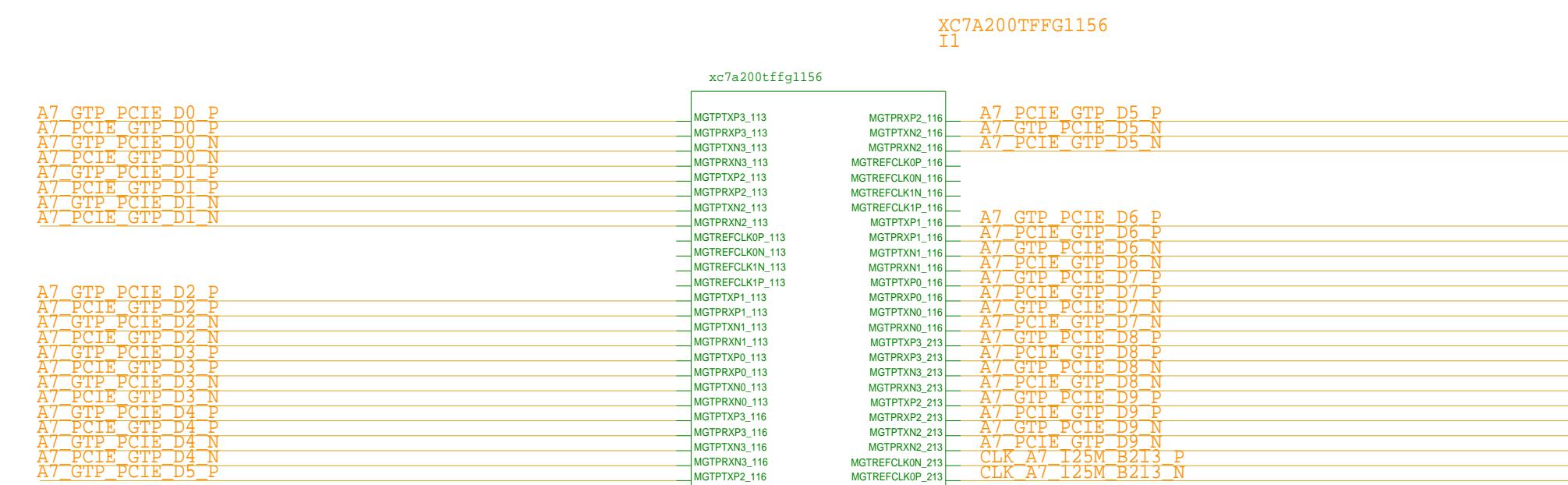
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ARTIX-7 GTP (1)

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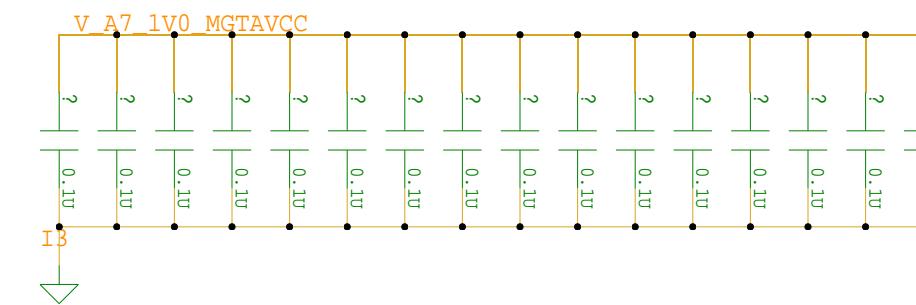
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ARTIX-7 GTP (2)

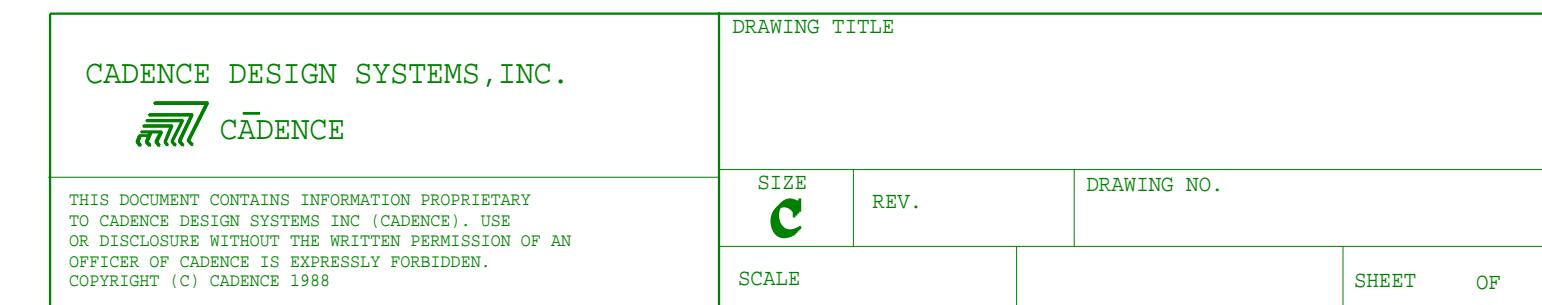
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The diagram shows the physical layout of the xc7a200tffg1156 FPGA board. Components are placed in columns along the top and bottom edges. A central column contains the main chip and various connectors. Numerous orange lines represent signal traces connecting the components. The board features a mix of green and orange colors for different layers or ground planes.



A7 BANK 216 MGTRREF ? ~~~~~ 100 V A7 1V2 MGTAVTT

A7 BANK 213 MGTRREF ? ^^^^ 100 V A7 1V2 MGTAVTT



ZYNQ-7 INDEX

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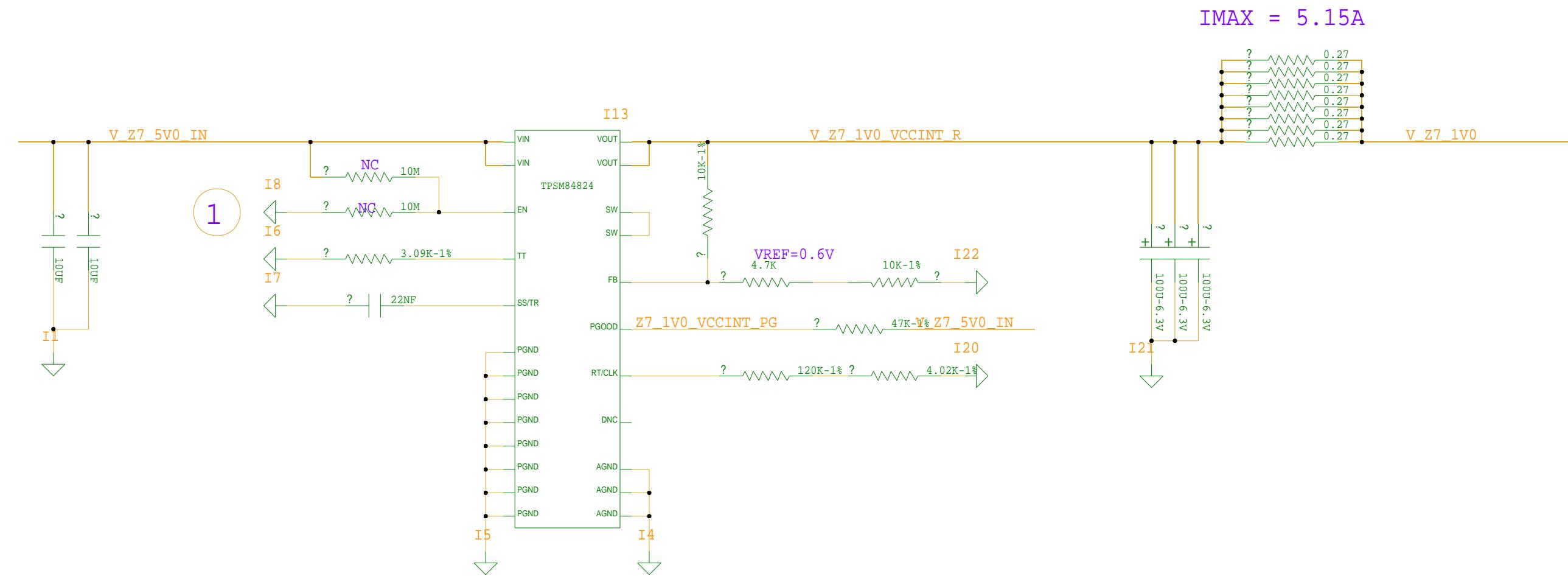
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ZYNQ-7 POWER (1)



SS/TR	6	I	Soft-start and tracking pin. Connecting an external capacitor to this pin adjusts the output voltage soft-start ramp slower than its 1.2 ms default setting. A voltage applied to this pin allows for tracking and sequencing control.
-------	---	---	--

Table 9. Soft-Start Capacitor Values and Soft-Start Time

C _{ss} (nF)	open	10	15	22	47
SS Time (ms)	1.2	2.4	3	3.8	6.8

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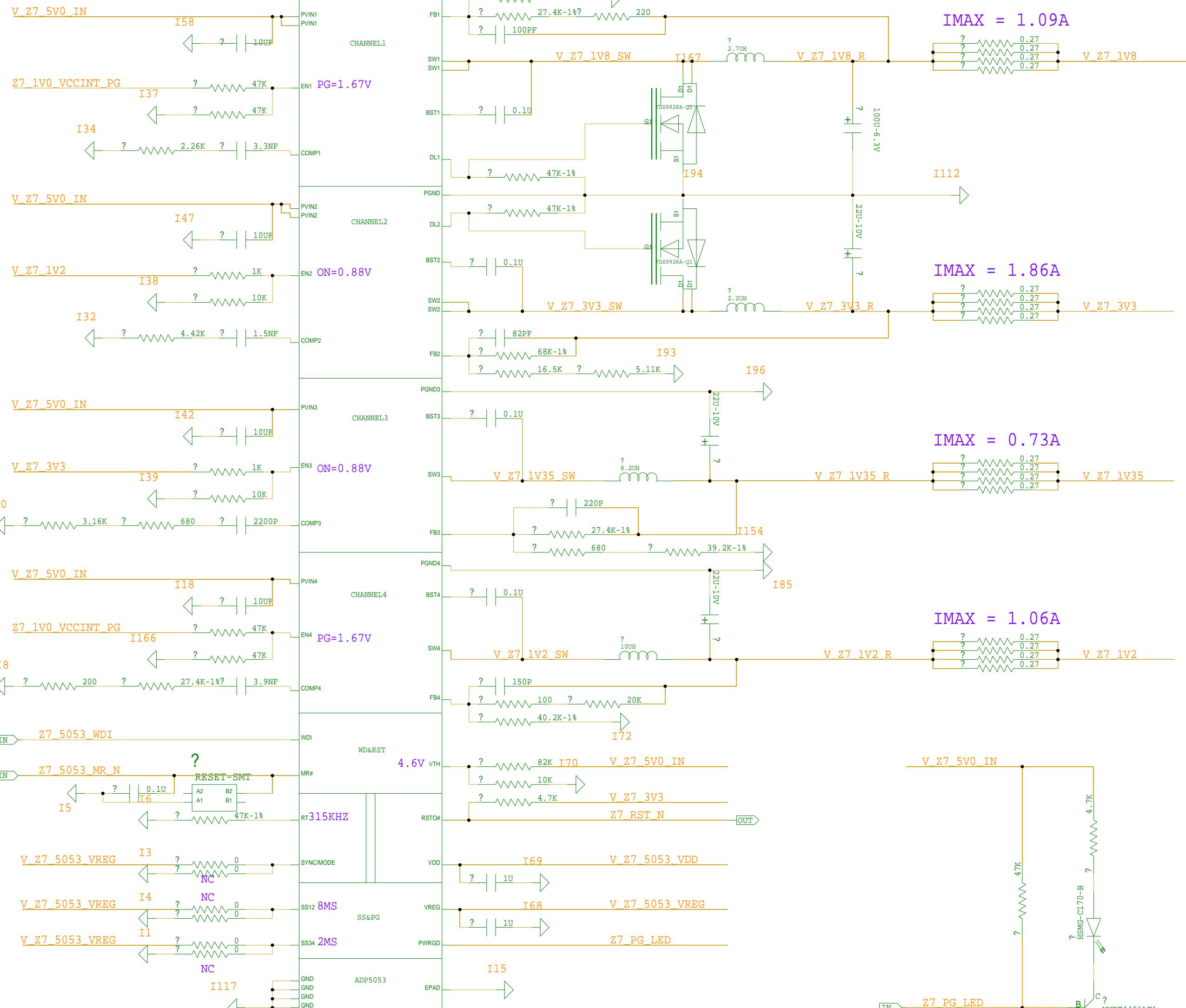


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ZYNQ-7 POWER (2)



$$V_{OUT} = V_{REF} \times (1 + (R_{TOP}/R_{BOT}))$$

$$R_{RT} (\text{k}\Omega) = [14,822/f_{SW} (\text{kHz})]^{1.081}$$

$$V_{IN_STARTUP} = (0.8 \text{ nA} + (0.8 \text{ V}/R_{BOT_EN})) \times \left(R_{TOP_EN} + \frac{R_{BOT_EN} \times 1 \text{ M}\Omega}{R_{BOT_EN} + 1 \text{ M}\Omega} \right)$$

where:

R_{TOP_EN} is the resistor from V_{IN} to EN.

R_{BOT_EN} is the resistor from EN to ground.

Table 9. Soft Start Time Set by the SS12 and SS34 Pins

R_{TOP} (k Ω)	R_{BOT} (k Ω)	Soft Start Time			
		Channel 1	Channel 2	Channel 3	Channel 4
0	N/A ¹	2 ms	2 ms	2 ms	2 ms
100	600	2 ms	Parallel	2 ms	4 ms
200	500	2 ms	8 ms	2 ms	8 ms
300	400	4 ms	2 ms	4 ms	2 ms
400	300	4 ms	4 ms	4 ms	4 ms
500	200	8 ms	2 ms	4 ms	8 ms
600	100	8 ms	Parallel	8 ms	2 ms
N/A ¹	0	8 ms	8 ms	8 ms	8 ms

Table 16. Factory Default Options

Option	Default Value
Channel 1 Output Voltage	0.8V adjustable output
Channel 2 Output Voltage	0.8V adjustable output
Channel 3 Output Voltage	0.8V adjustable output
Channel 4 Output Voltage	0.8V adjustable output
PWRGD Pin (Pin 20) Output	Monitor Channel 1 output
Output Discharge Function	Enabled for all four buck regulators
Switching Frequency on Channel 1	1x switching frequency set by the RT pin
Switching Frequency on Channel 3	1x switching frequency set by the RT pin
SYNC/MODE Pin (Pin 43) Function	Forced PWM/automatic PWM/PSM mode setting with the ability to synchronize to an external clock
Hiccup Protection	Enabled for overcurrent events
Short-Circuit Latch-Off Function	Disabled for output short-circuit events
Oversupply Latch-Off Function	Disabled for output oversupply events
Reset Timeout Period	200 ms
Watchdog Timeout Period	1.6 sec
Manual Reset Input Mode	Processor manual reset mode

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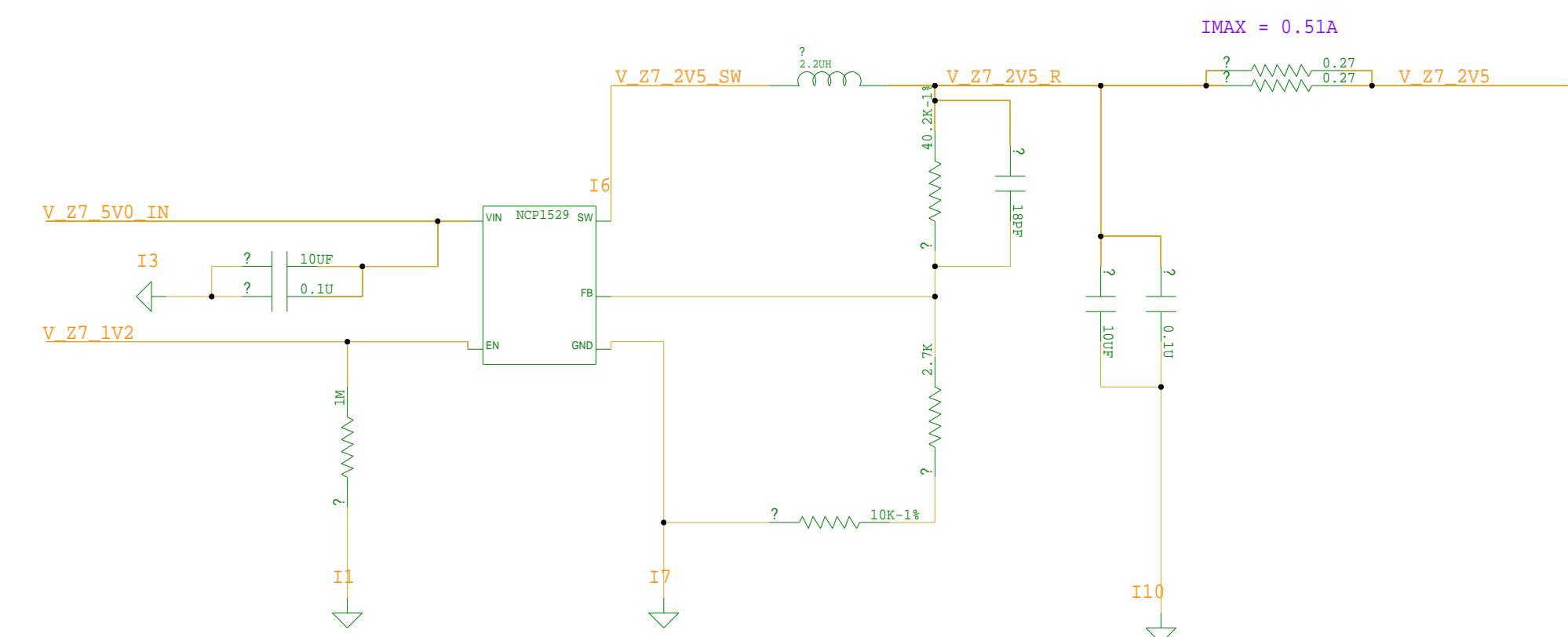
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ZYNQ-7 POWER (3)

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- $V_{out} = V_{FB} \times (1 + R1/R2)$
- V_{OUT} : Output Voltage (V)
 - V_{FB} : Feedback Voltage = 0.6 V
 - $R1$: Feedback Resistor from V_{OUT} to FB
 - $R2$: Feedback Resistor from FB to GND

3

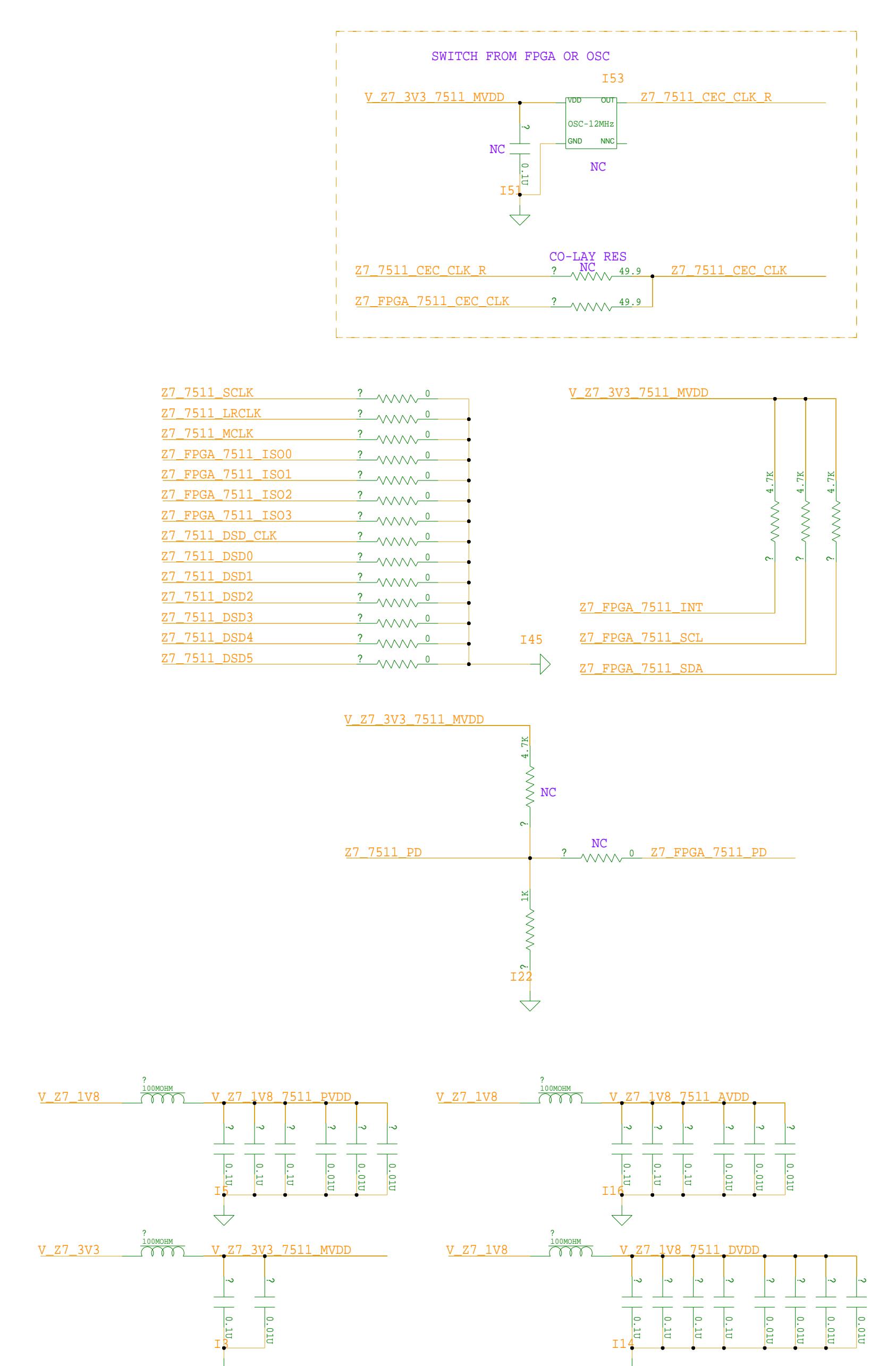
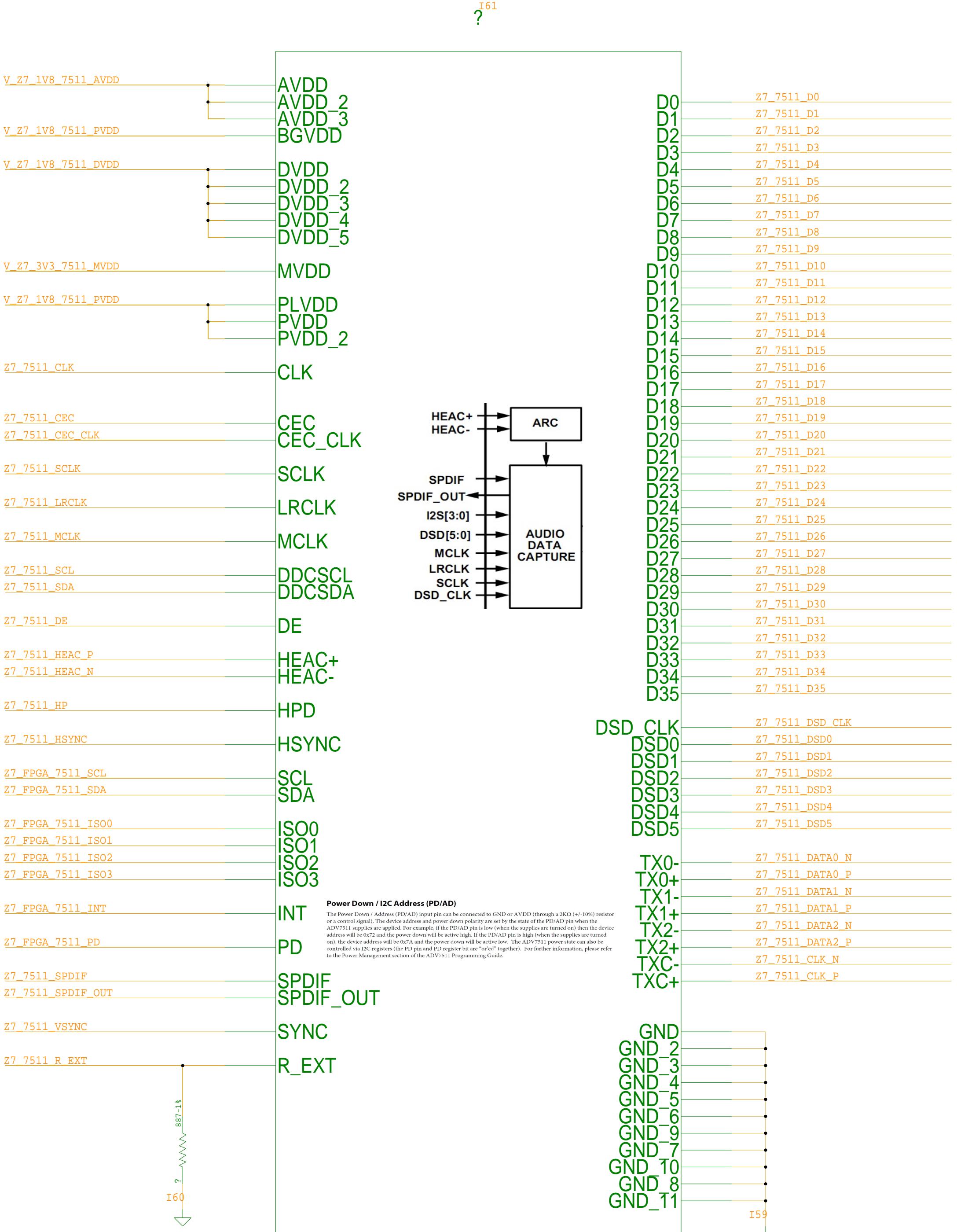


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ZYNQ-7 PL HDMI TRANSMITTER (1)



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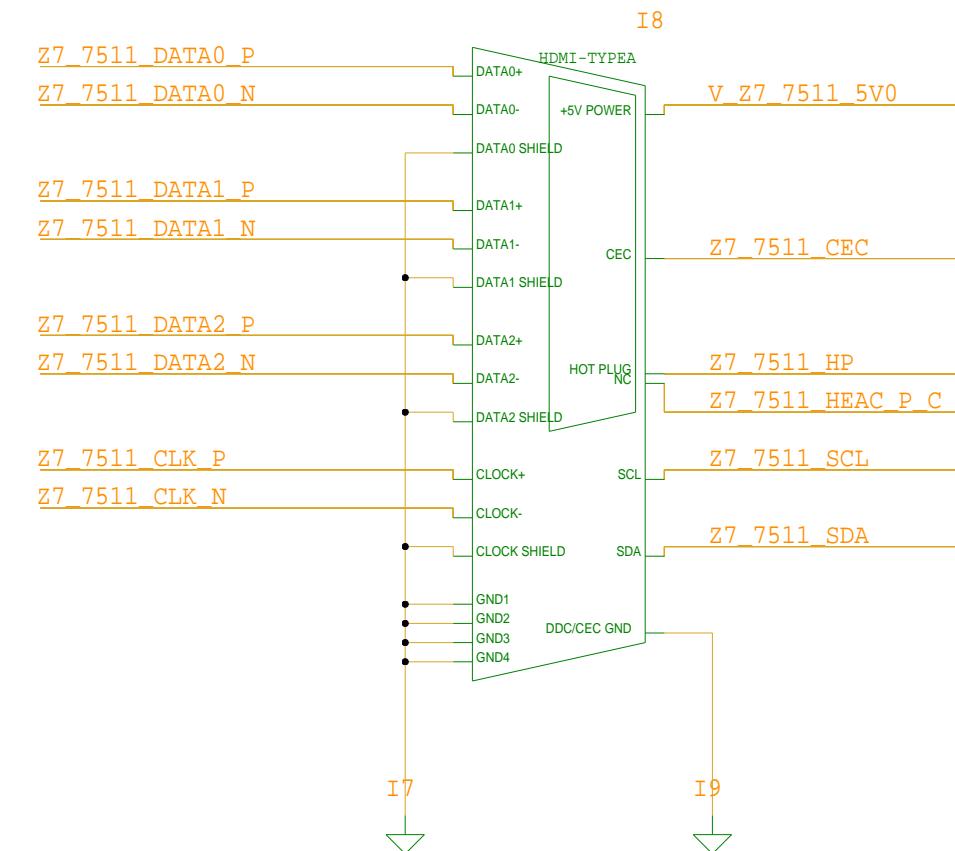
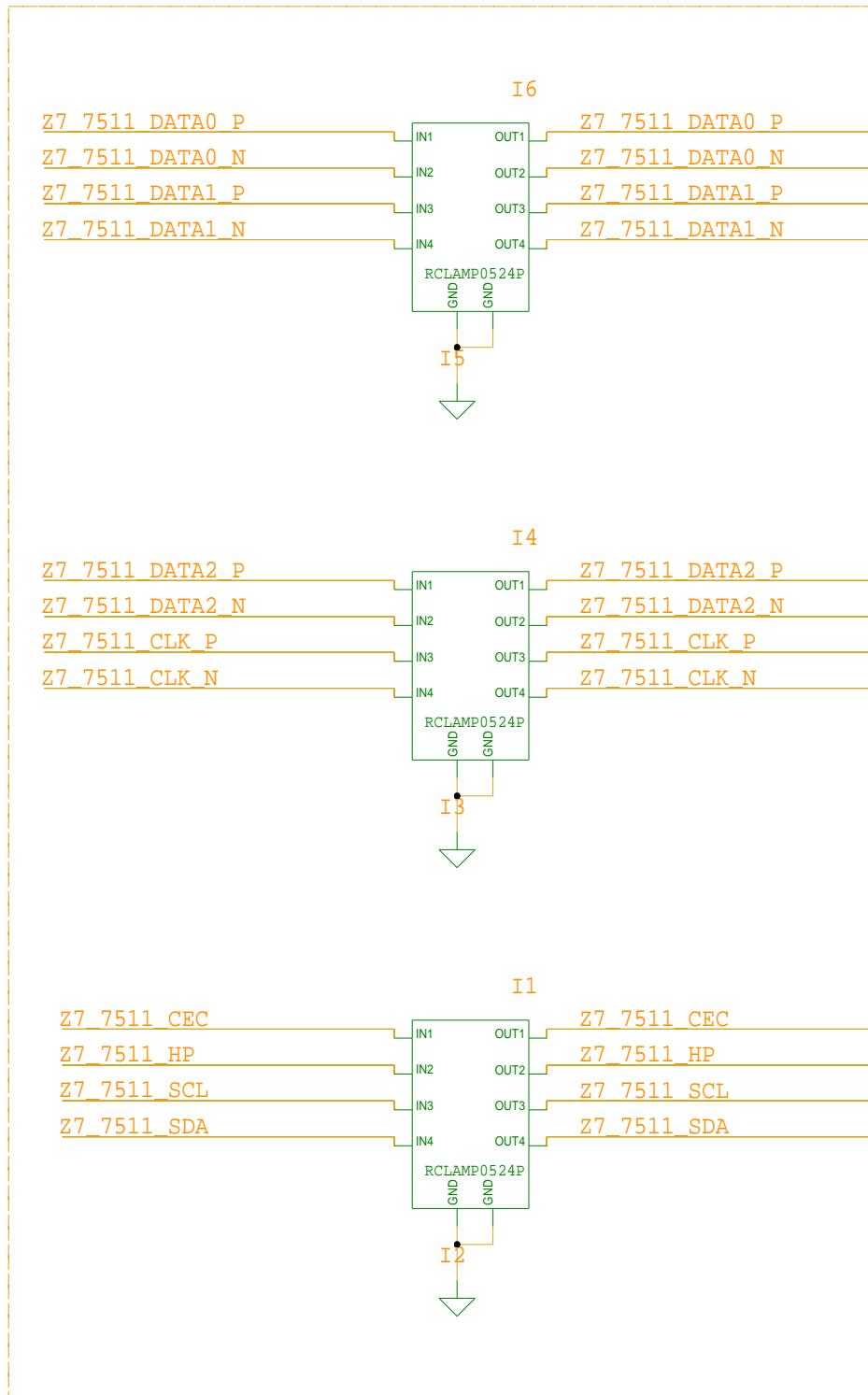
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ZYNQ-7 PL HDMI TRANSMITTER (2)

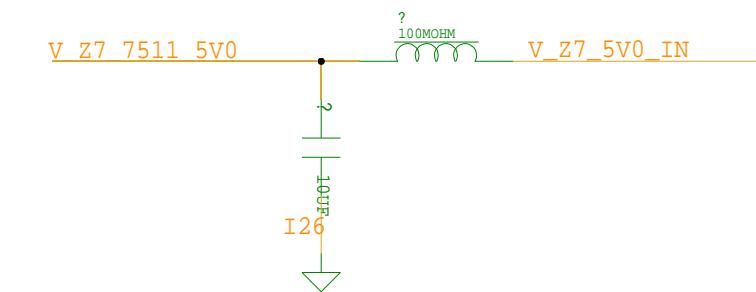
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CHANGE CONNECTION DUE TO LAYOUT



CLOSE TO HDMI CONNECTOR

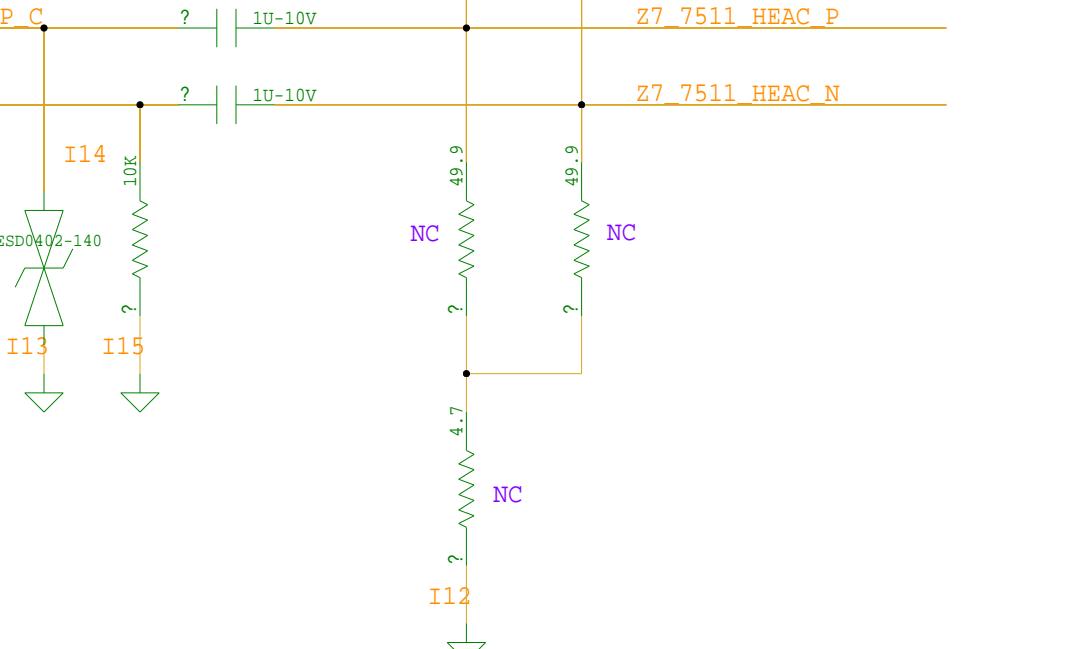


Z7_7511_CEC

? 1N4148 ? 27.4K-? \$ Z7_3V3_7511_MVDD

V_Z7_1V8_7511_DVDD

CAPS CLOSE TO CONNECTOR



Z7_7511_SCL ? 1.8K-? \$ Z7_7511_5V0

Z7_7511_SDA ? 1.8K-? \$

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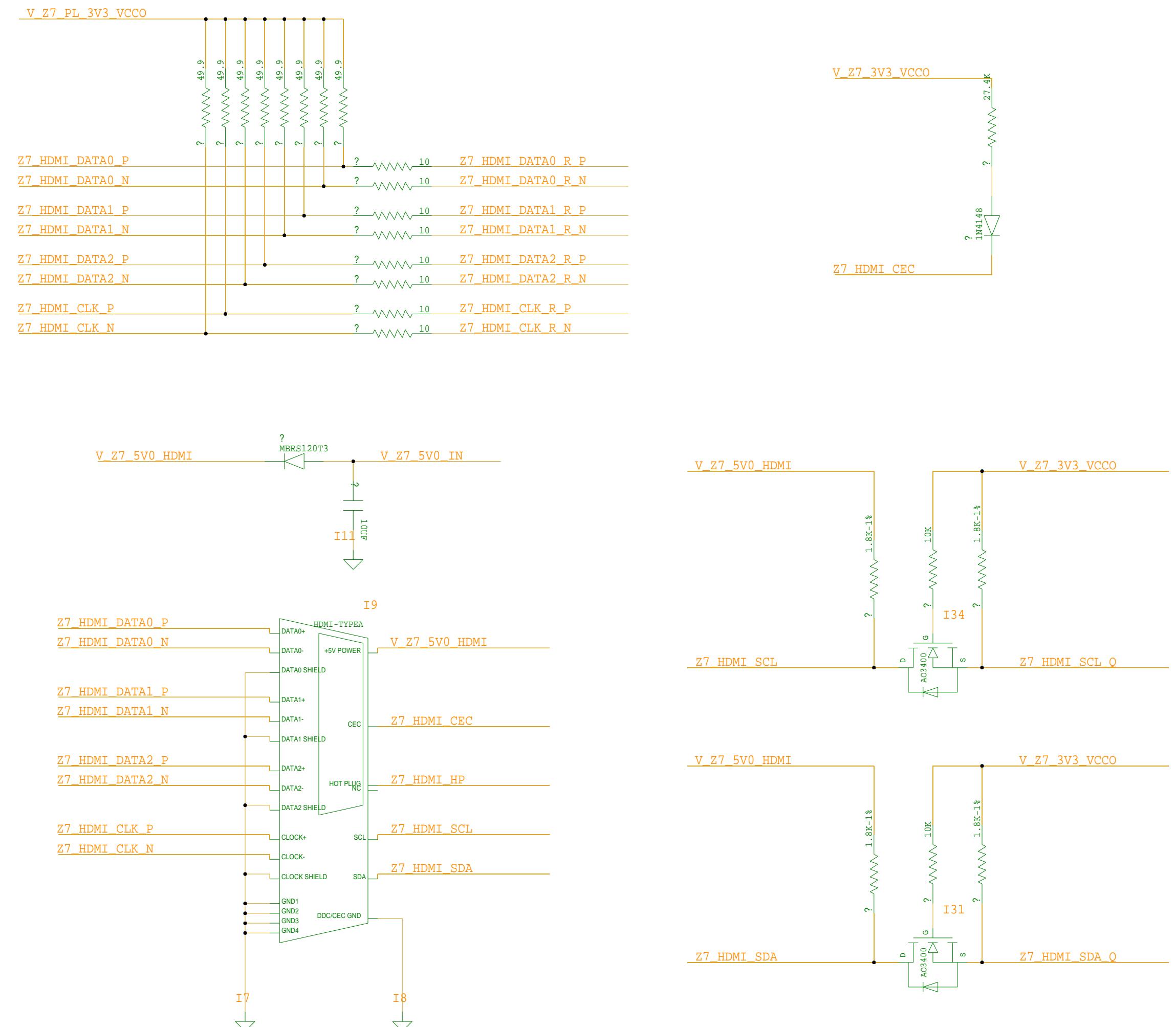
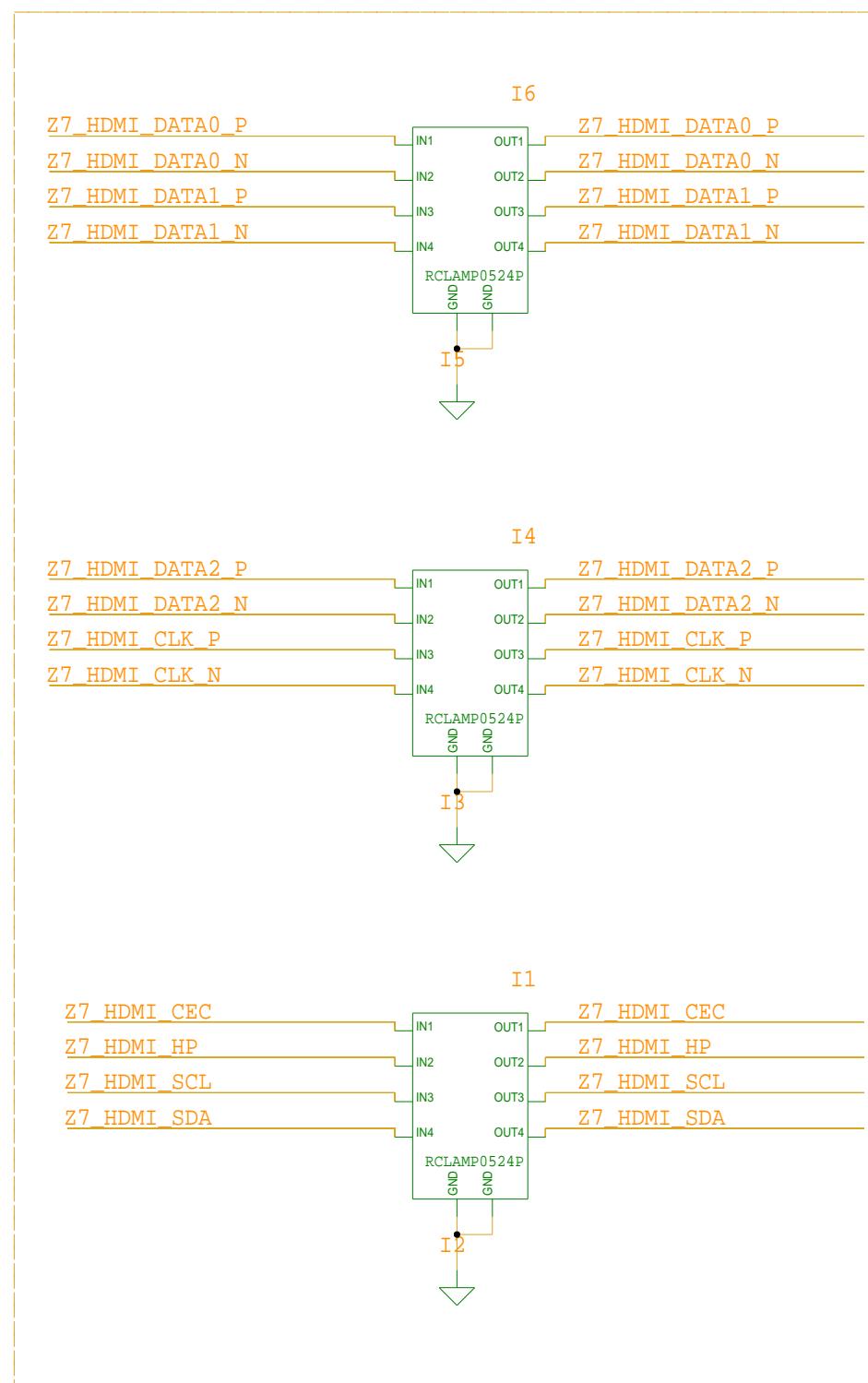
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ZYNQ-7 PL HDMI INOUT

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CHANGE CONNECTION DUE TO LAYOUT



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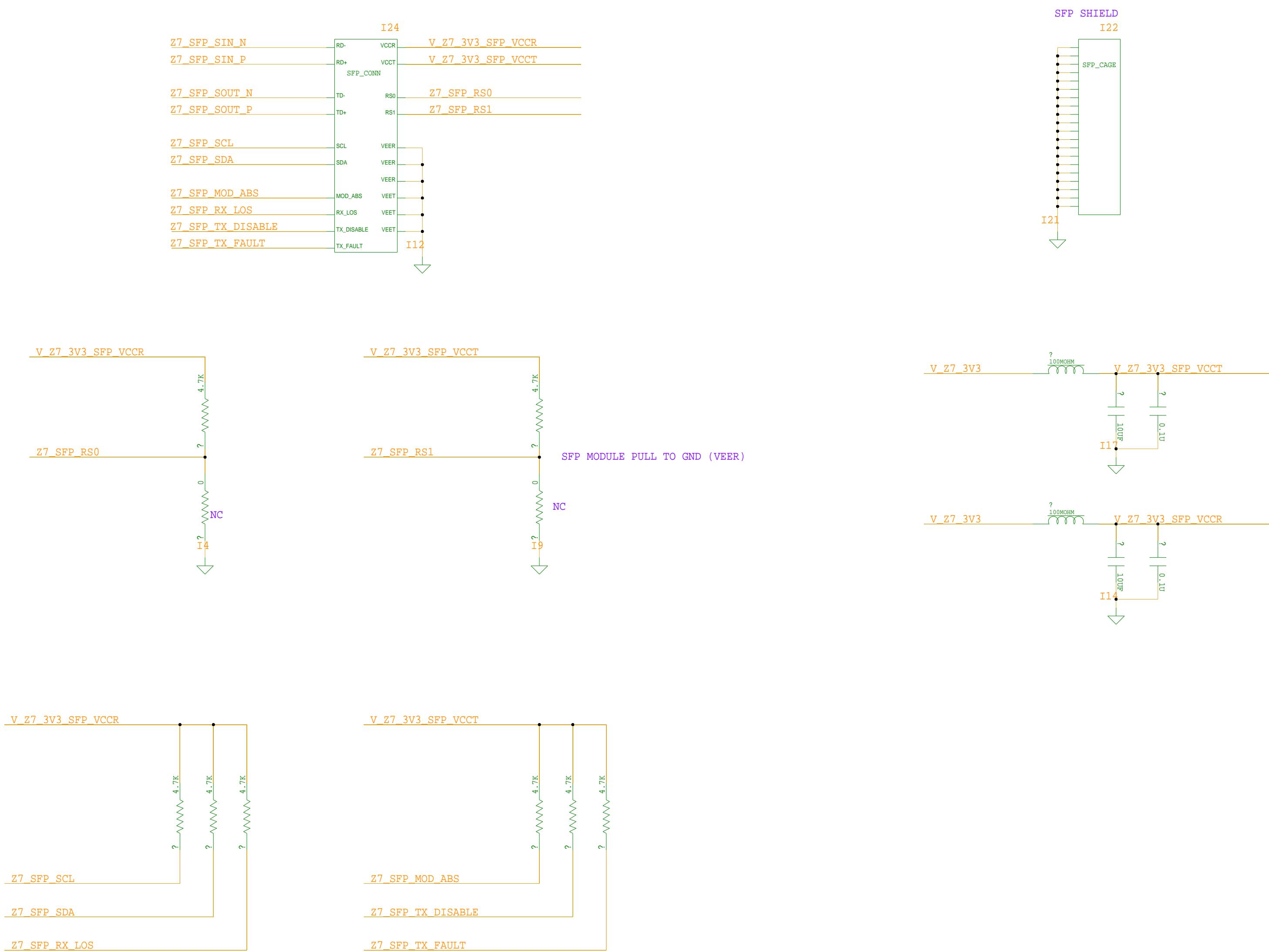
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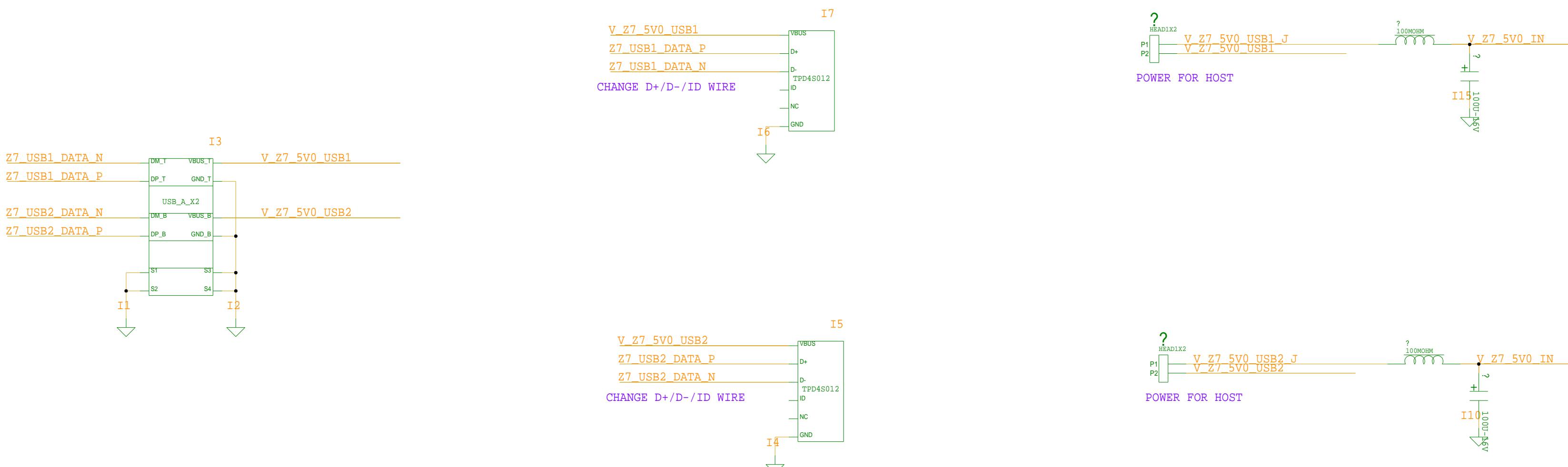
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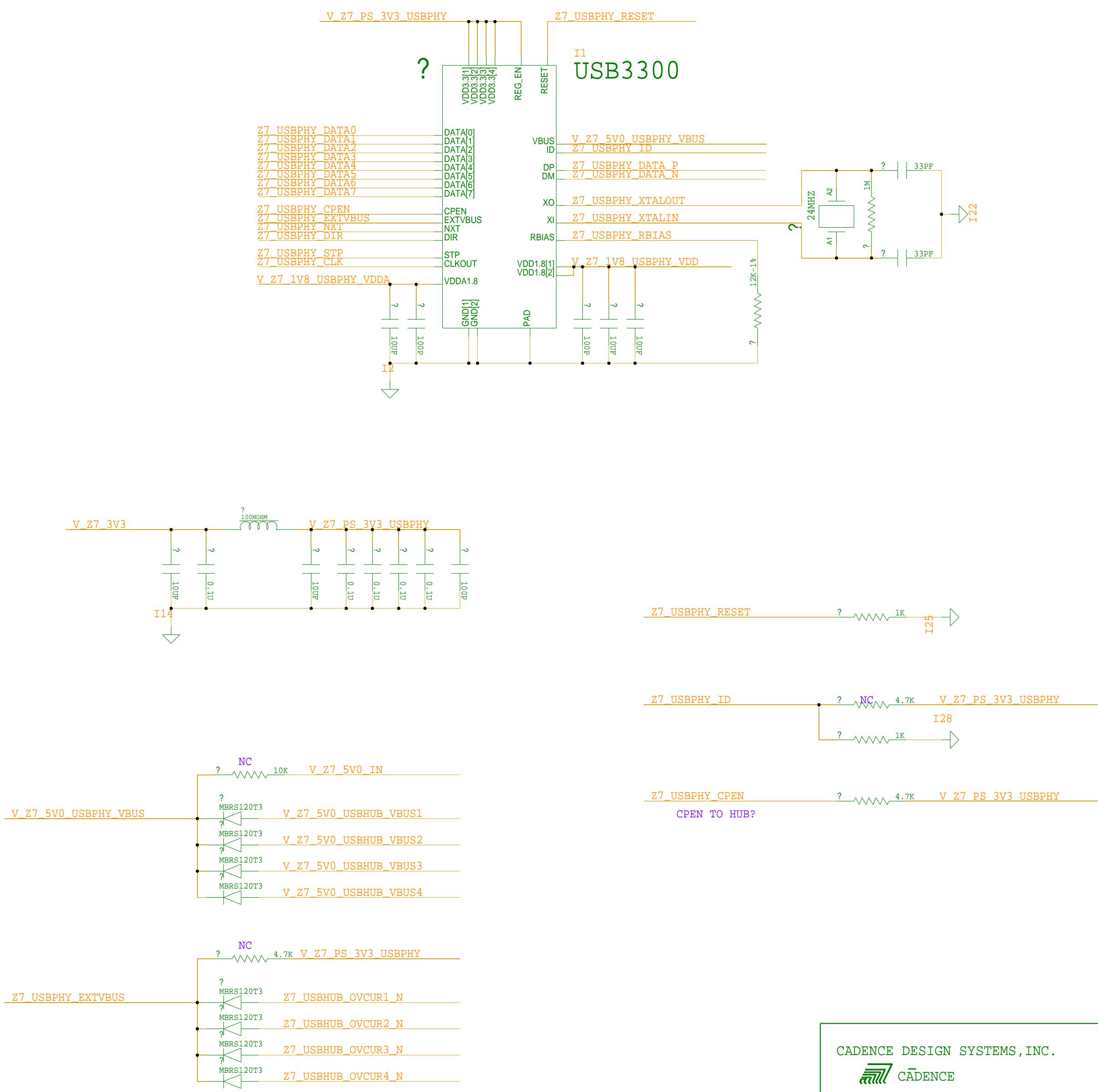
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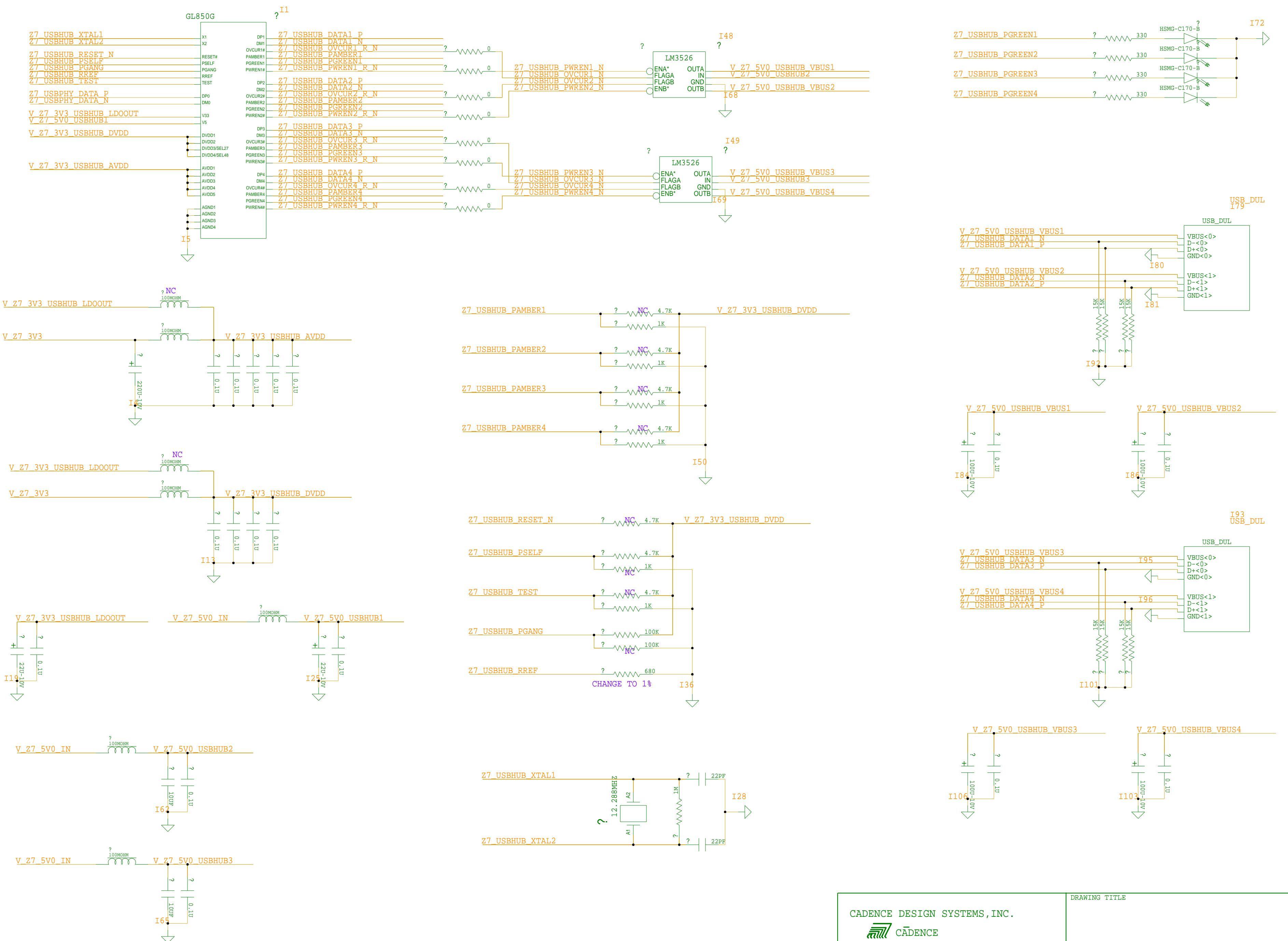
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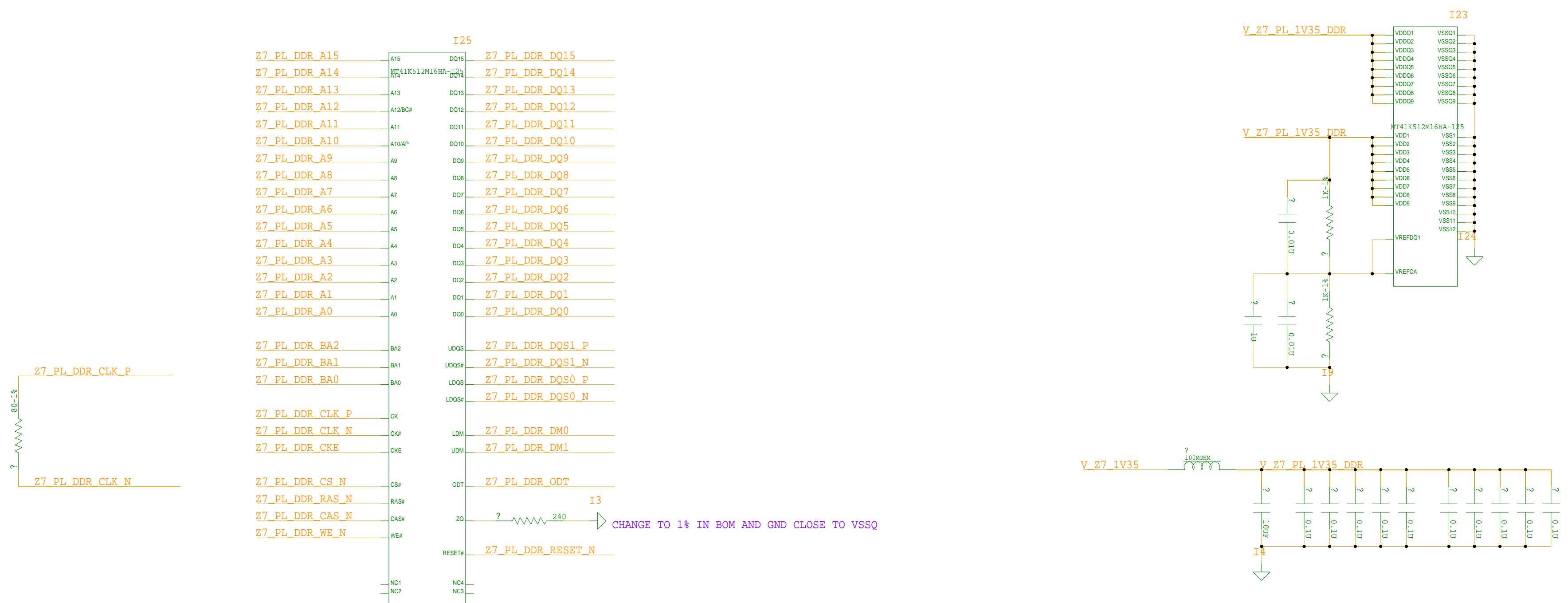
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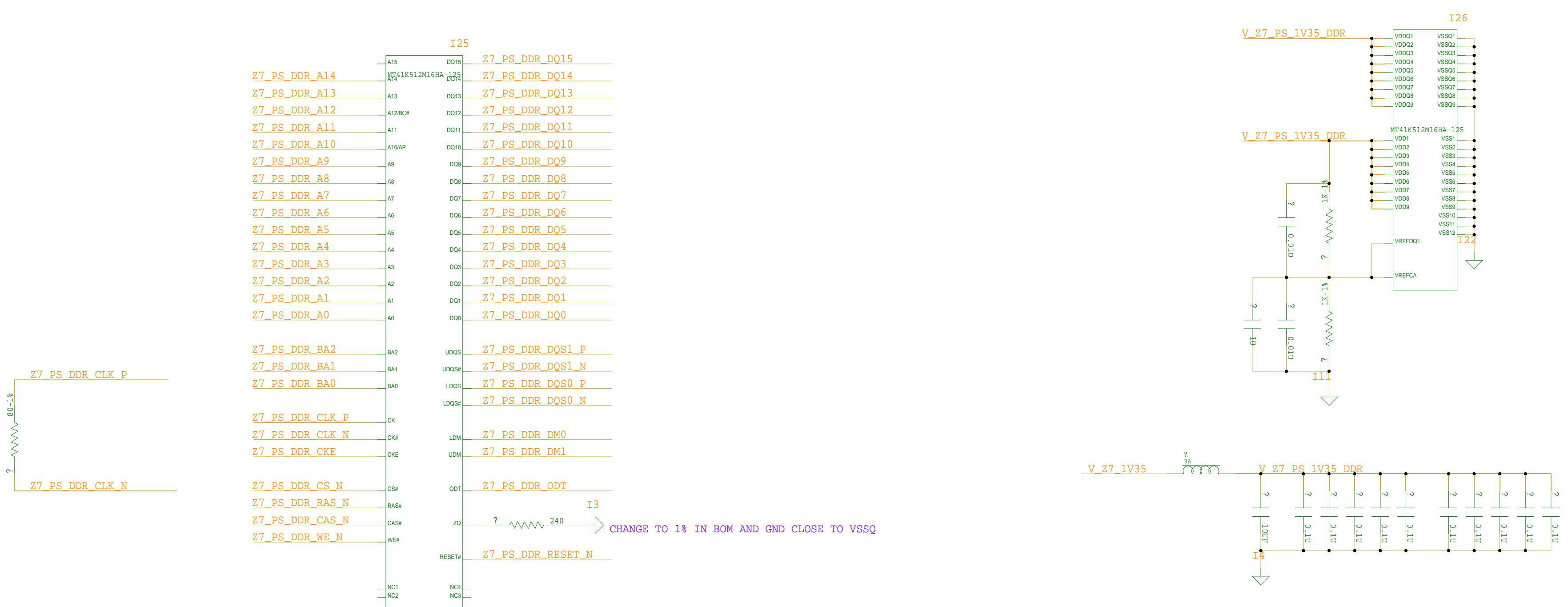
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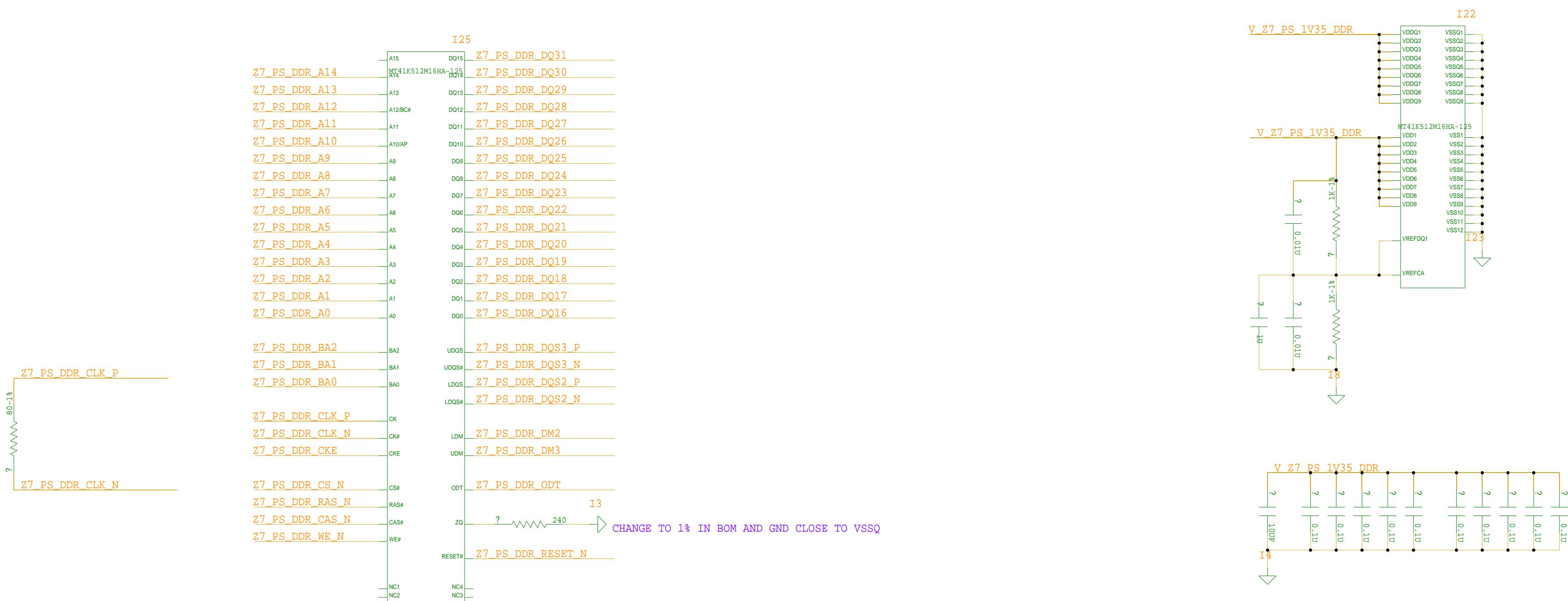
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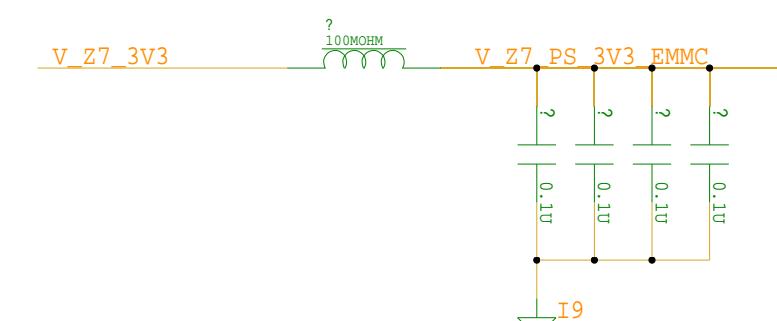
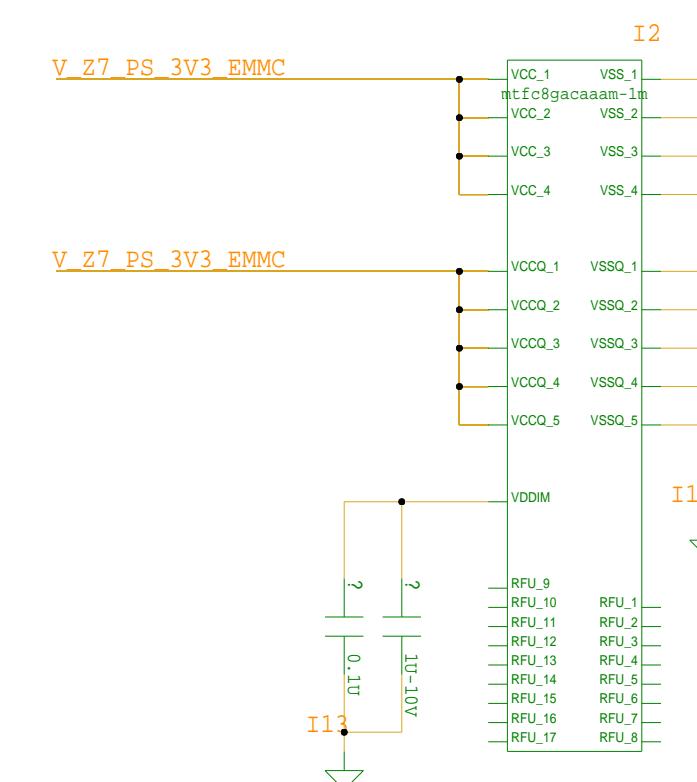
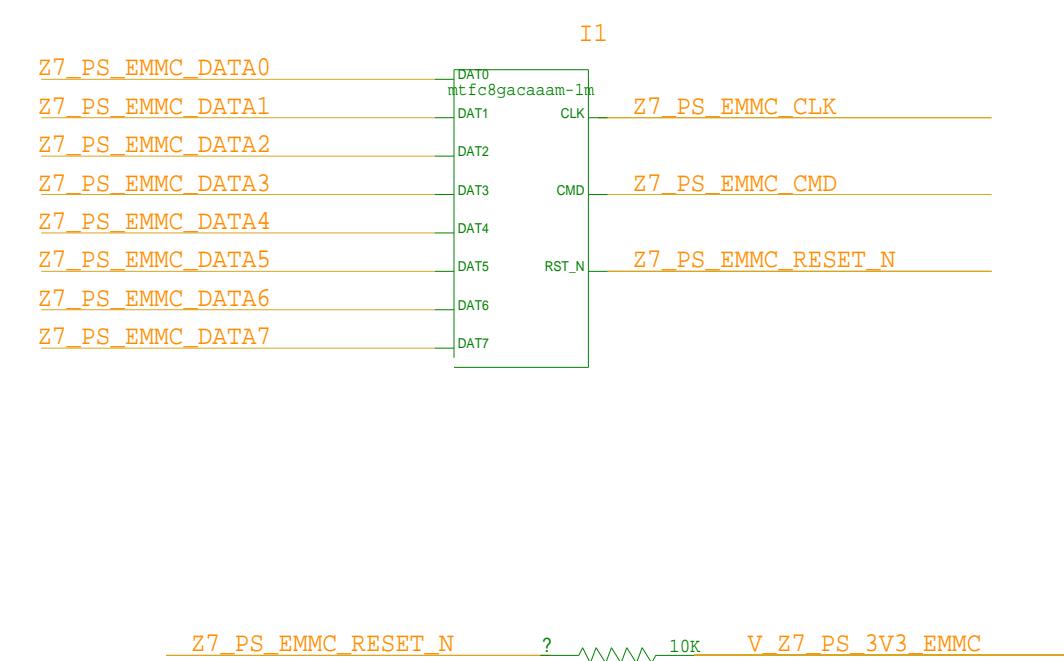
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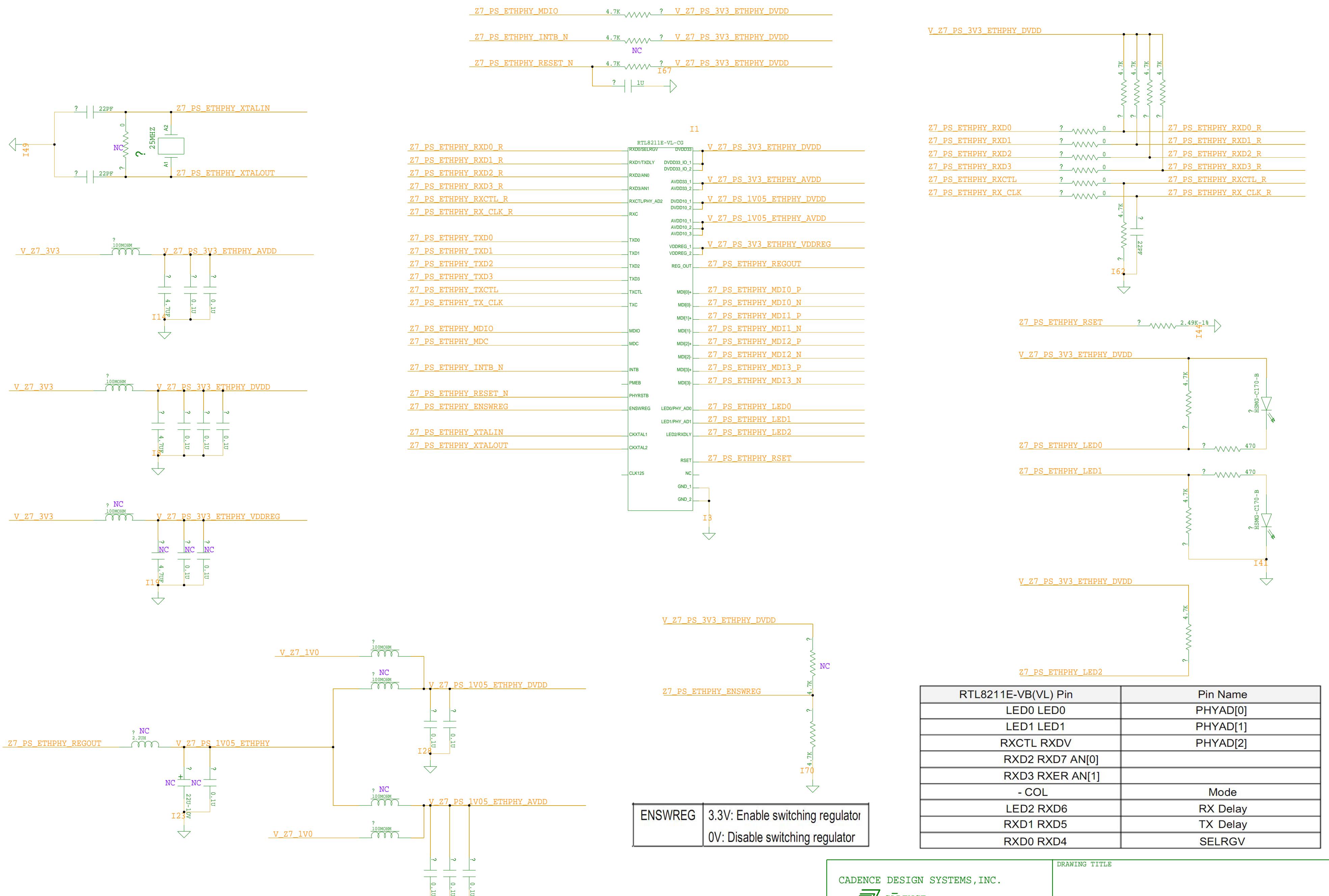
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ZYNQ-7 PS GE PHY (1)

REVISONS

ZONE LTR DESCRIPTION

DATE APPR.



RTL8211E-VB(VL) Pin	Pin Name
LED0 LED0	PHYAD[0]
LED1 LED1	PHYAD[1]
RXCTL RXDV	PHYAD[2]
RXD2 RXD7 AN[0]	- COL
RXD3 RXER AN[1]	Mode
- COL	RX Delay
LED2 RXD6	TX Delay
RXD1 RXD5	SELRGV
RXD0 RXD4	

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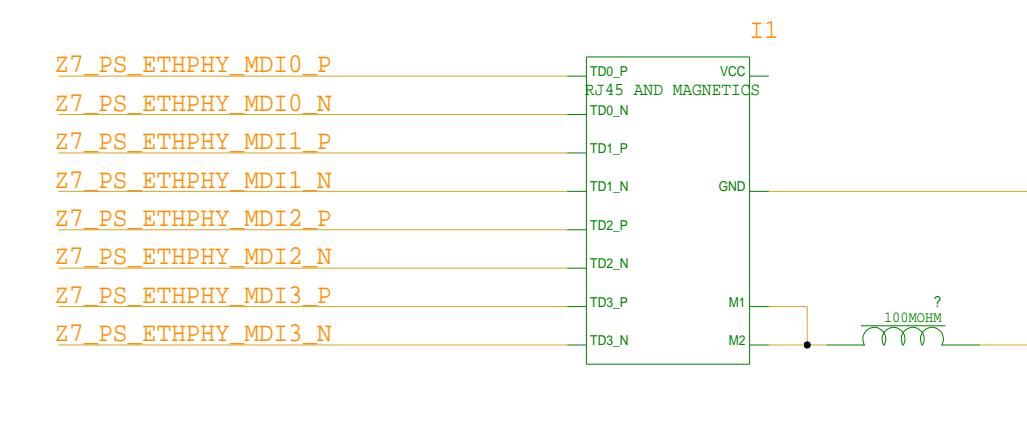
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ZONE	LTR	DESCRIPTION	DATE	APPR.



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ZYNQ-7 SPARTAN6 (2)

REVISIONS

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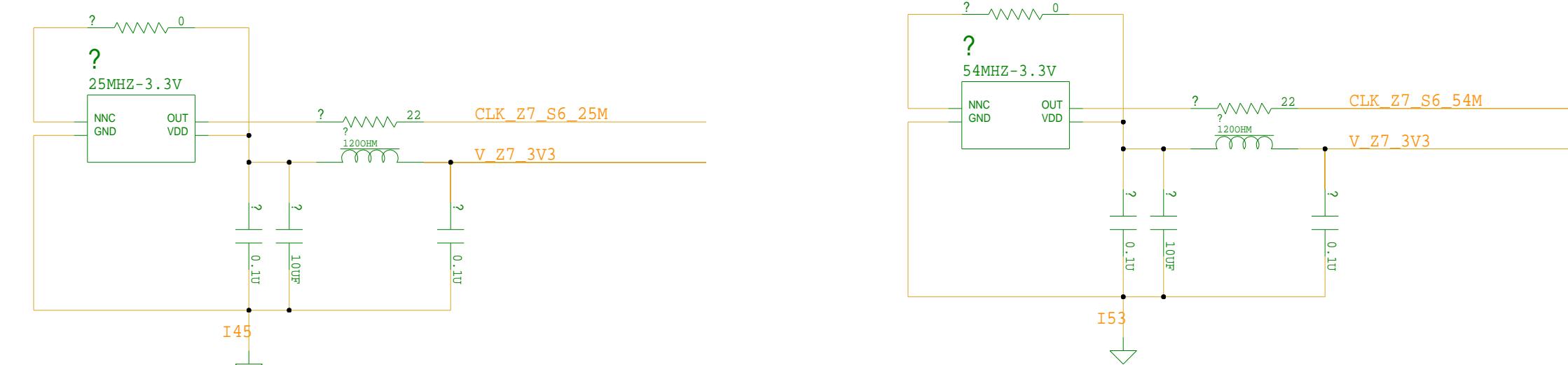
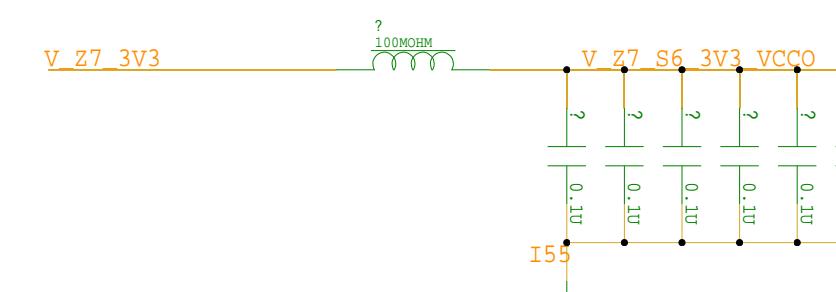
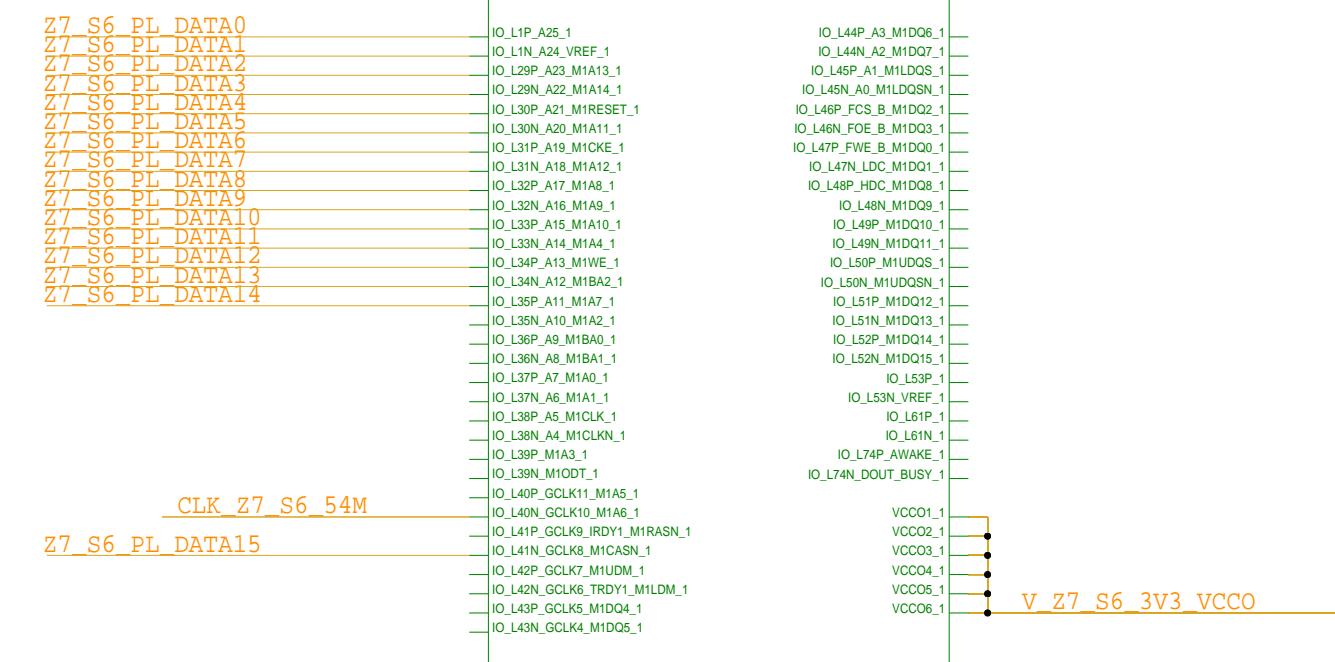
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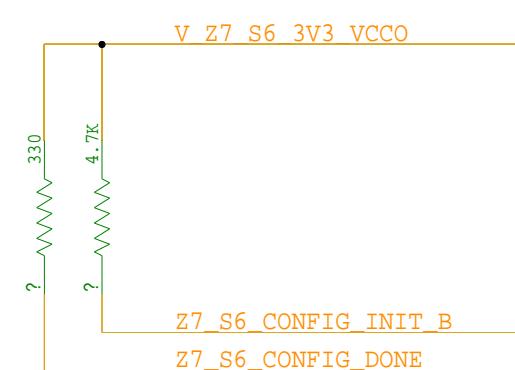
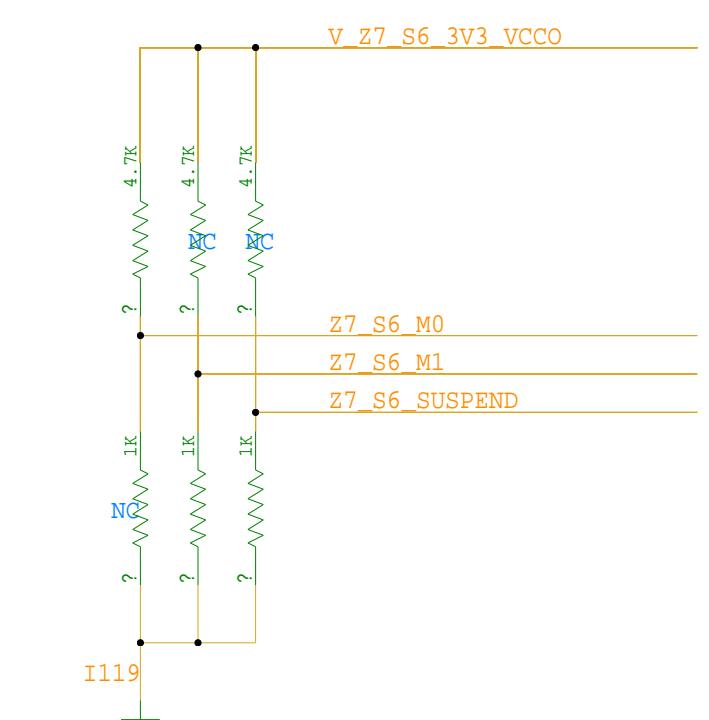
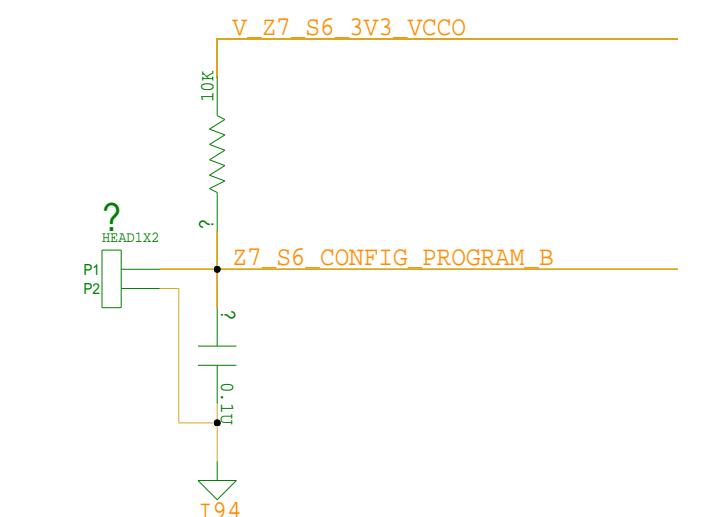
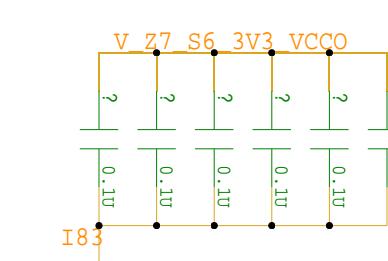
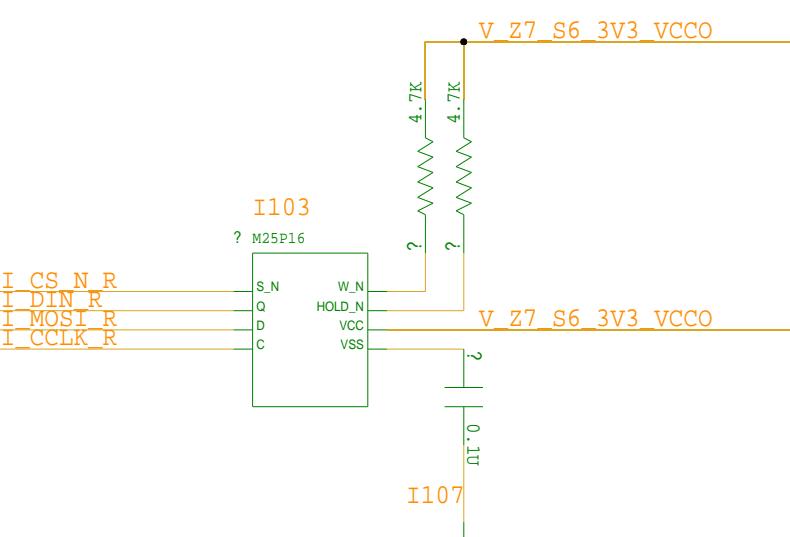
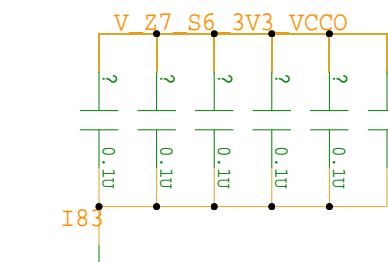
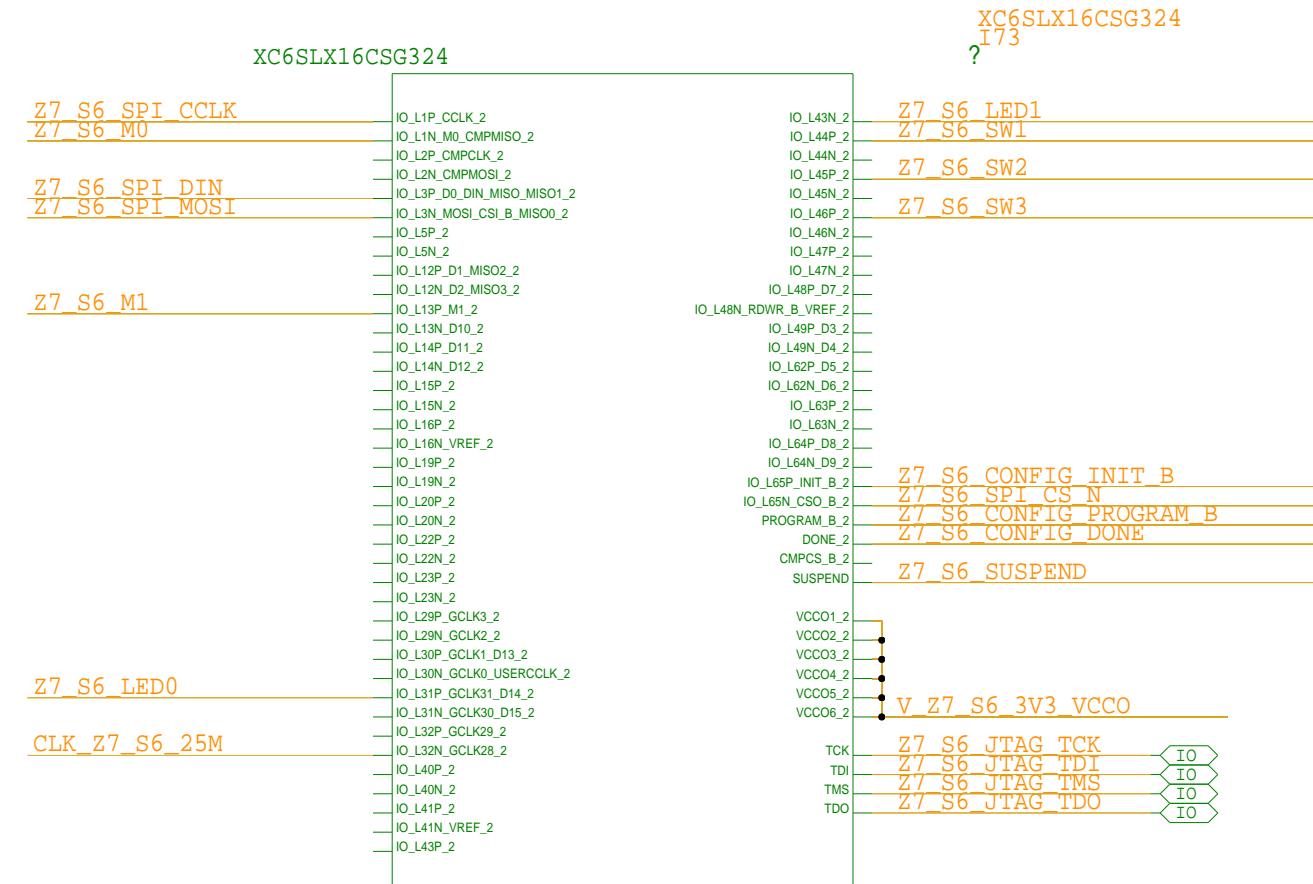
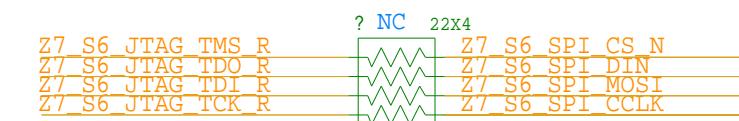
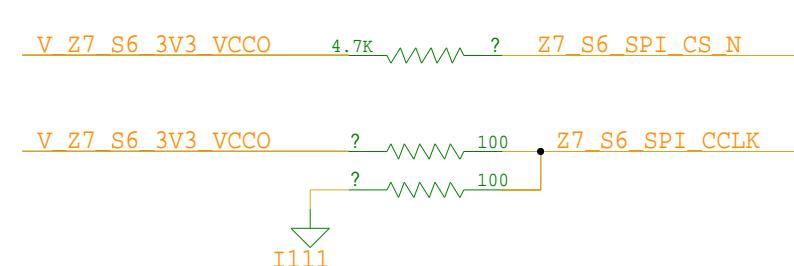
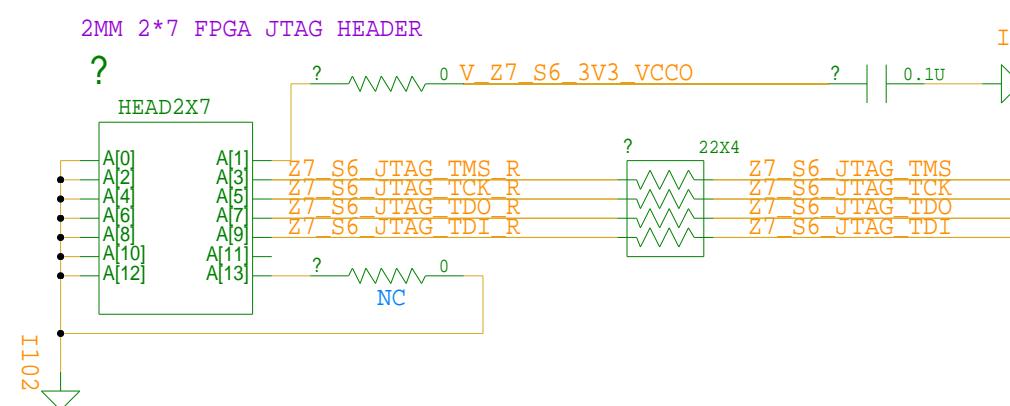
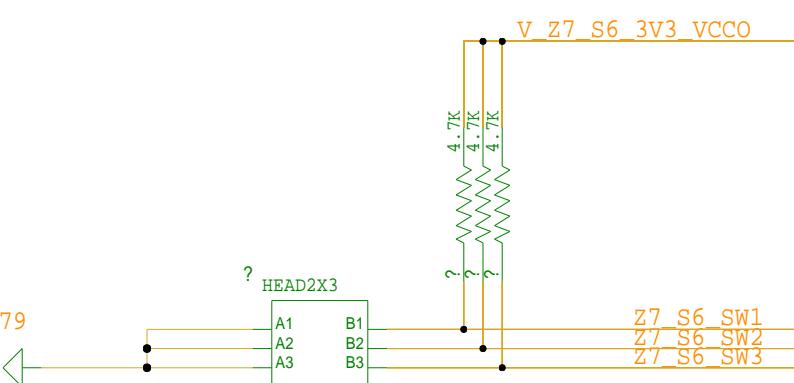
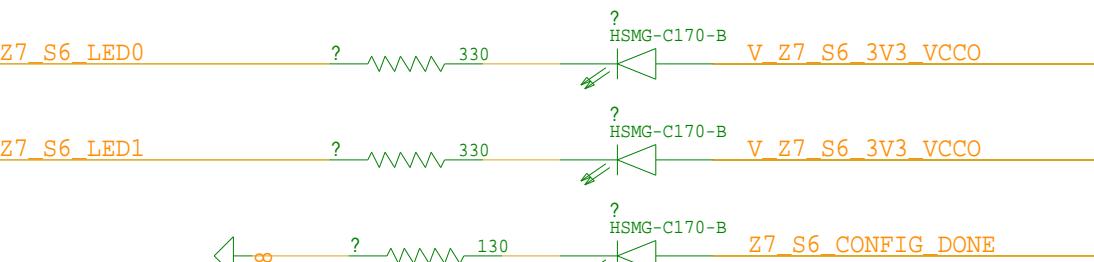
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ZYNQ-7 SPARTAN6 (3)

REVISIONS

ZONE	LTR	DESCRIPTION	DATE	APPR.



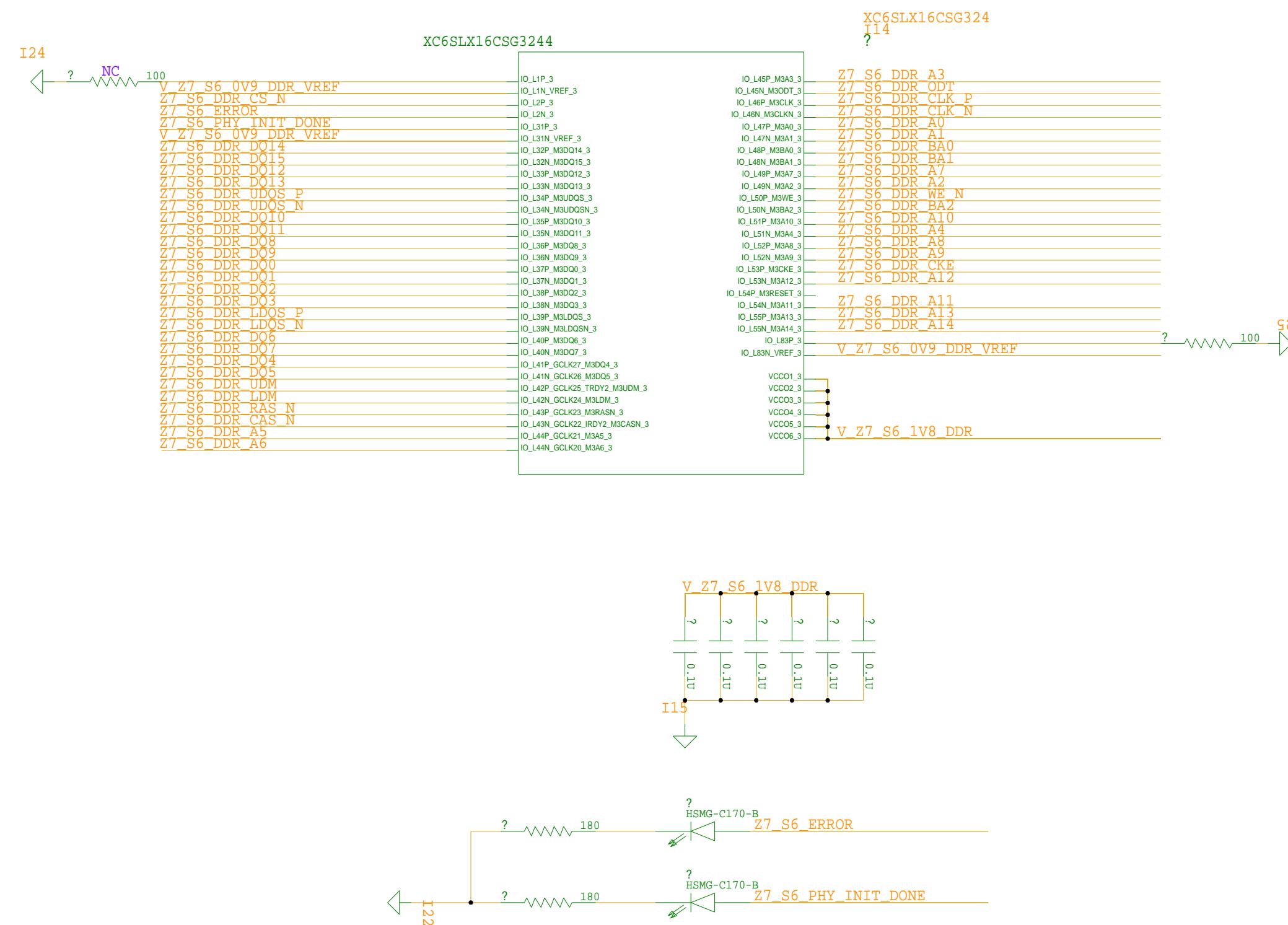
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ZYNQ-7 SPARTAN6 (4)

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ZYNQ-7 SPARTAN6 (5)

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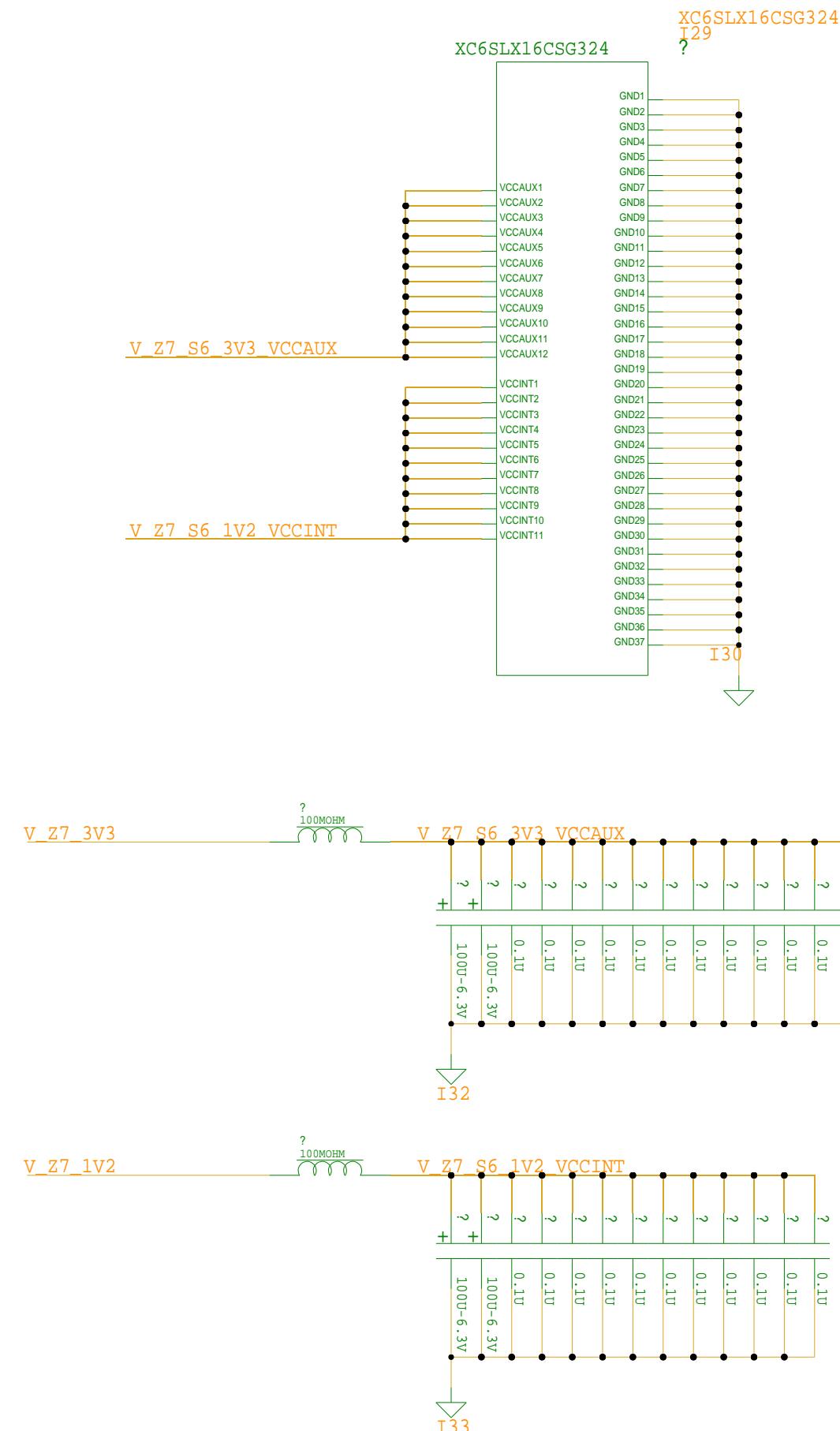
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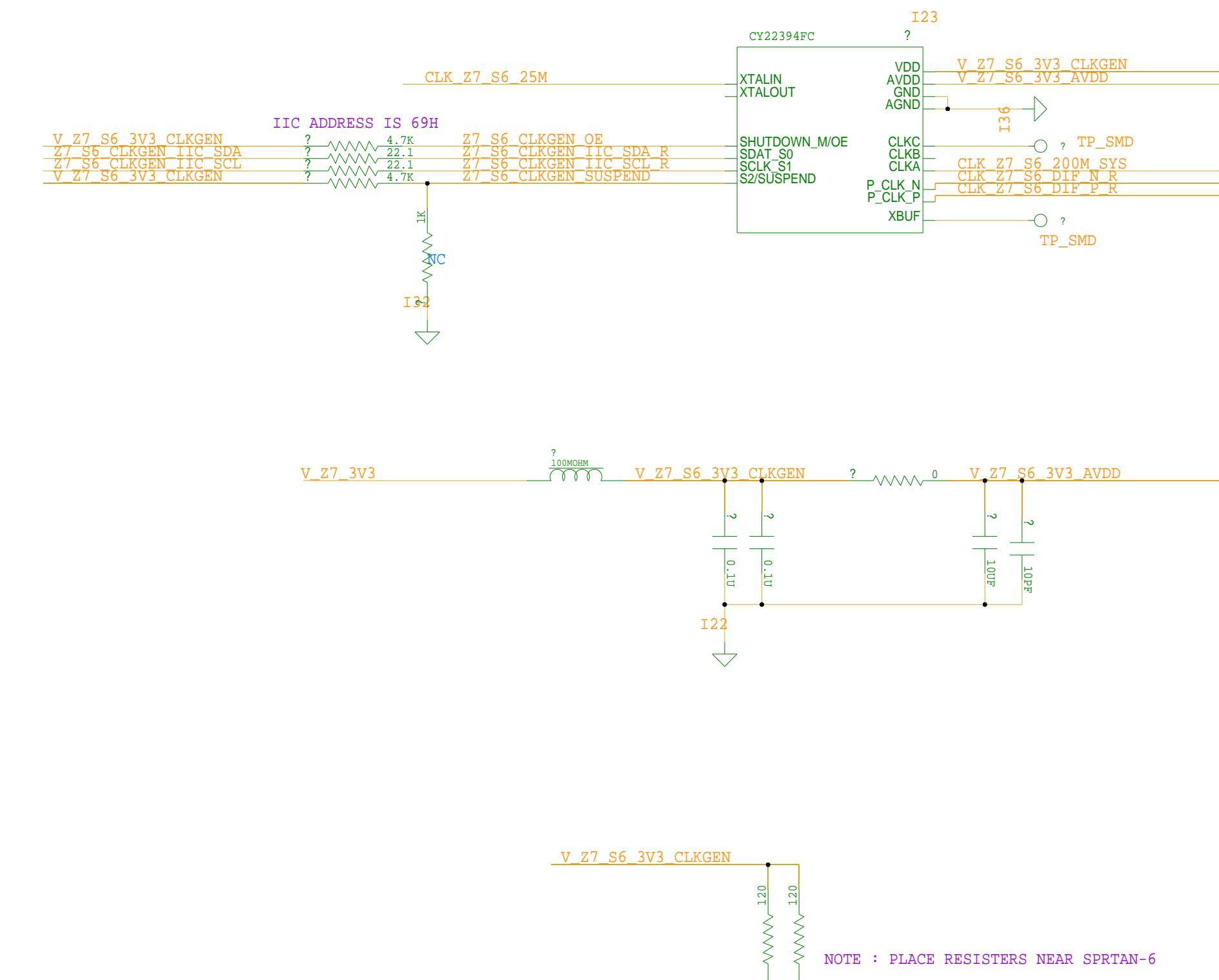
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ZYNQ-7 SPARTAN6 (6)

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ZONE	LTR	DESCRIPTION	DATE	APPR.

FPGA DDR2 200M-CLOCK



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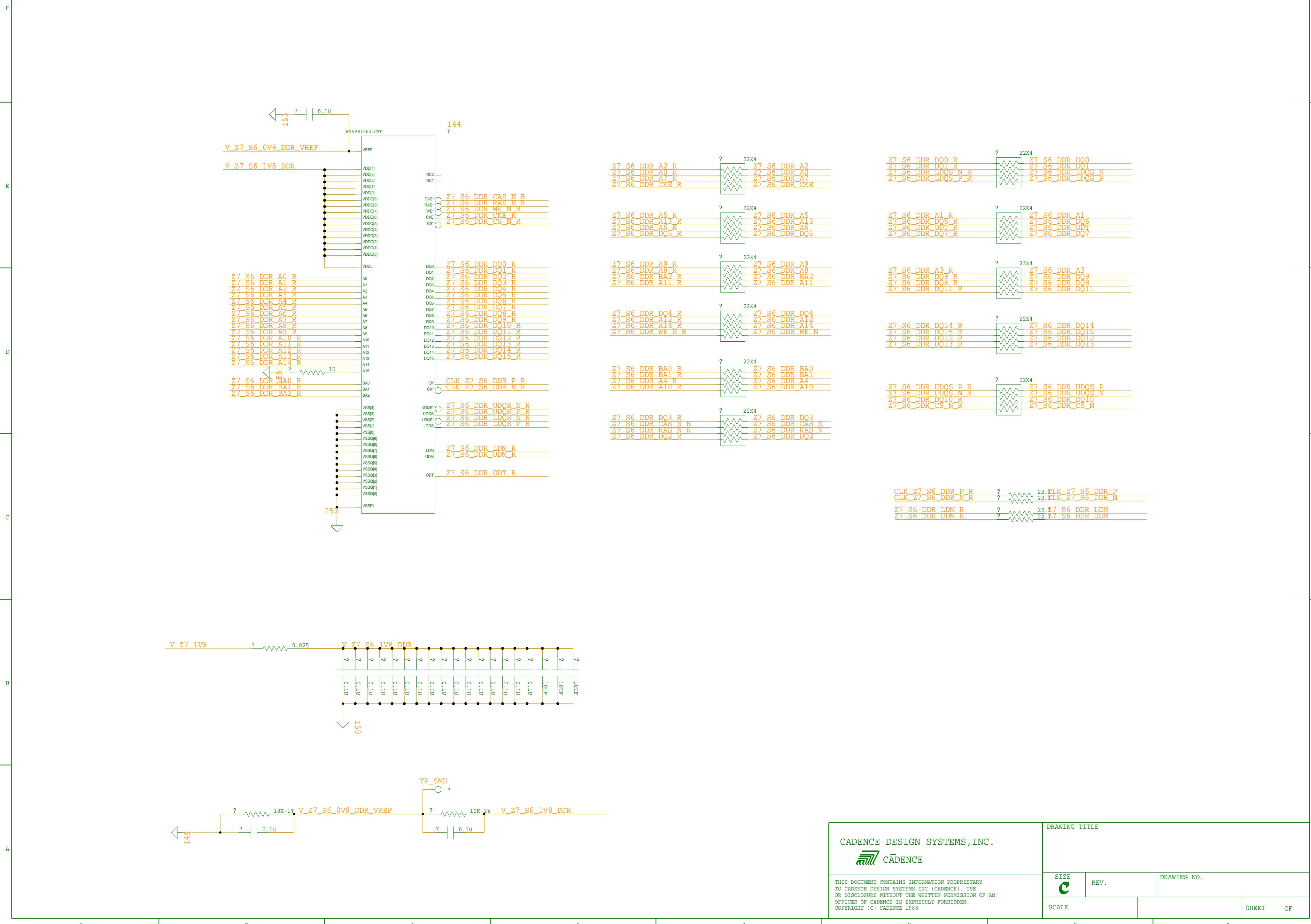
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ZYNQ-7 SPARTAN6 (7)

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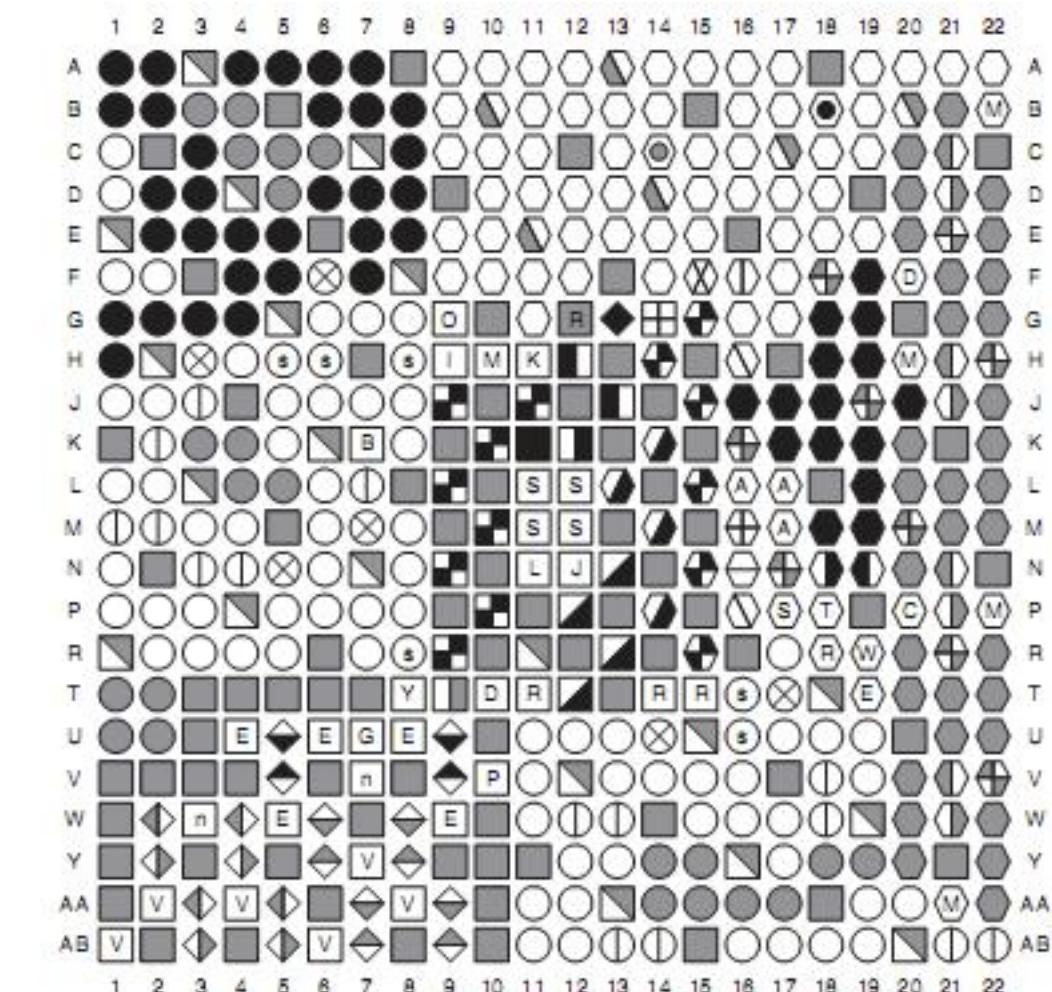
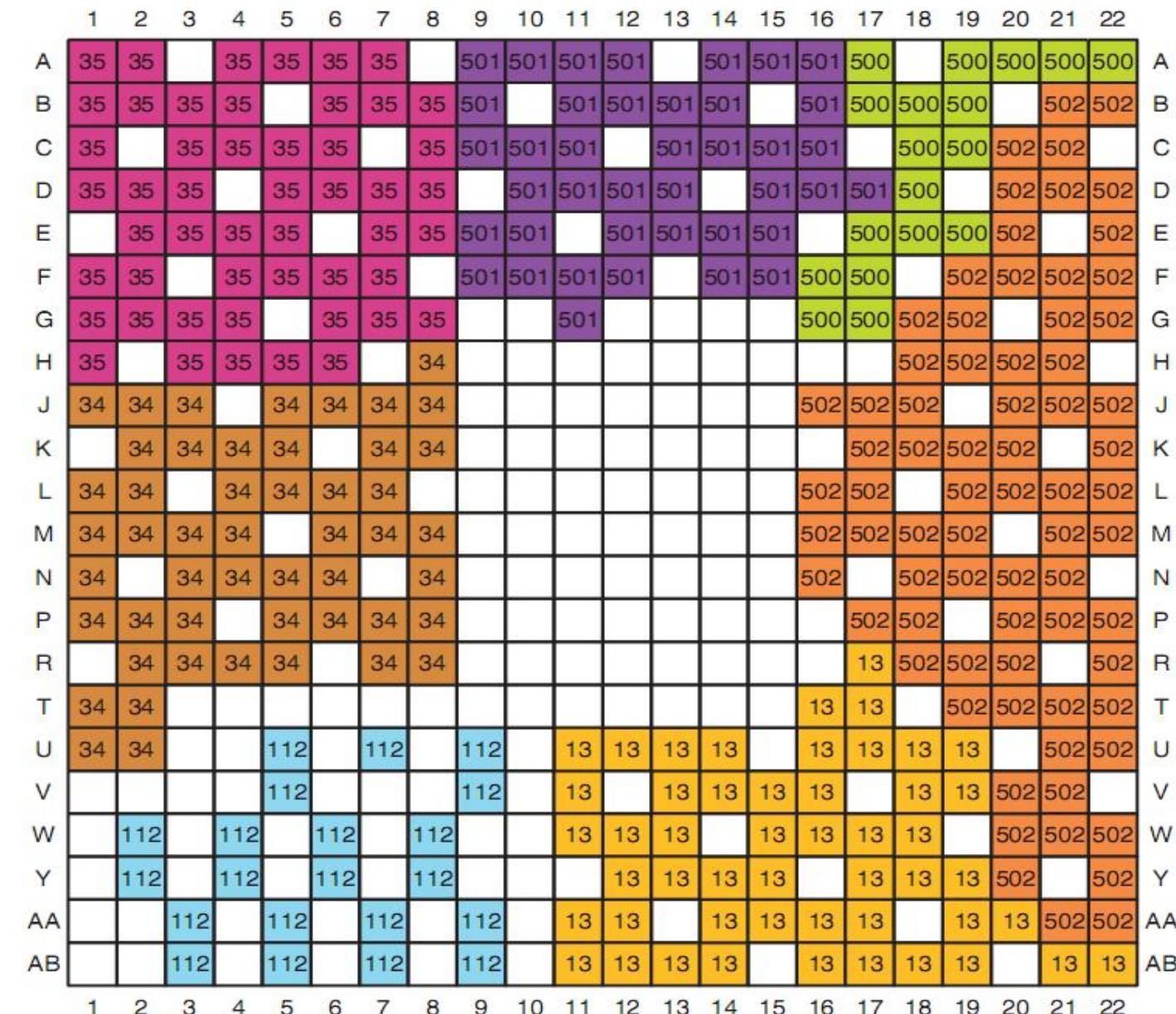
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ZYNQ-7 PINOUT MAP

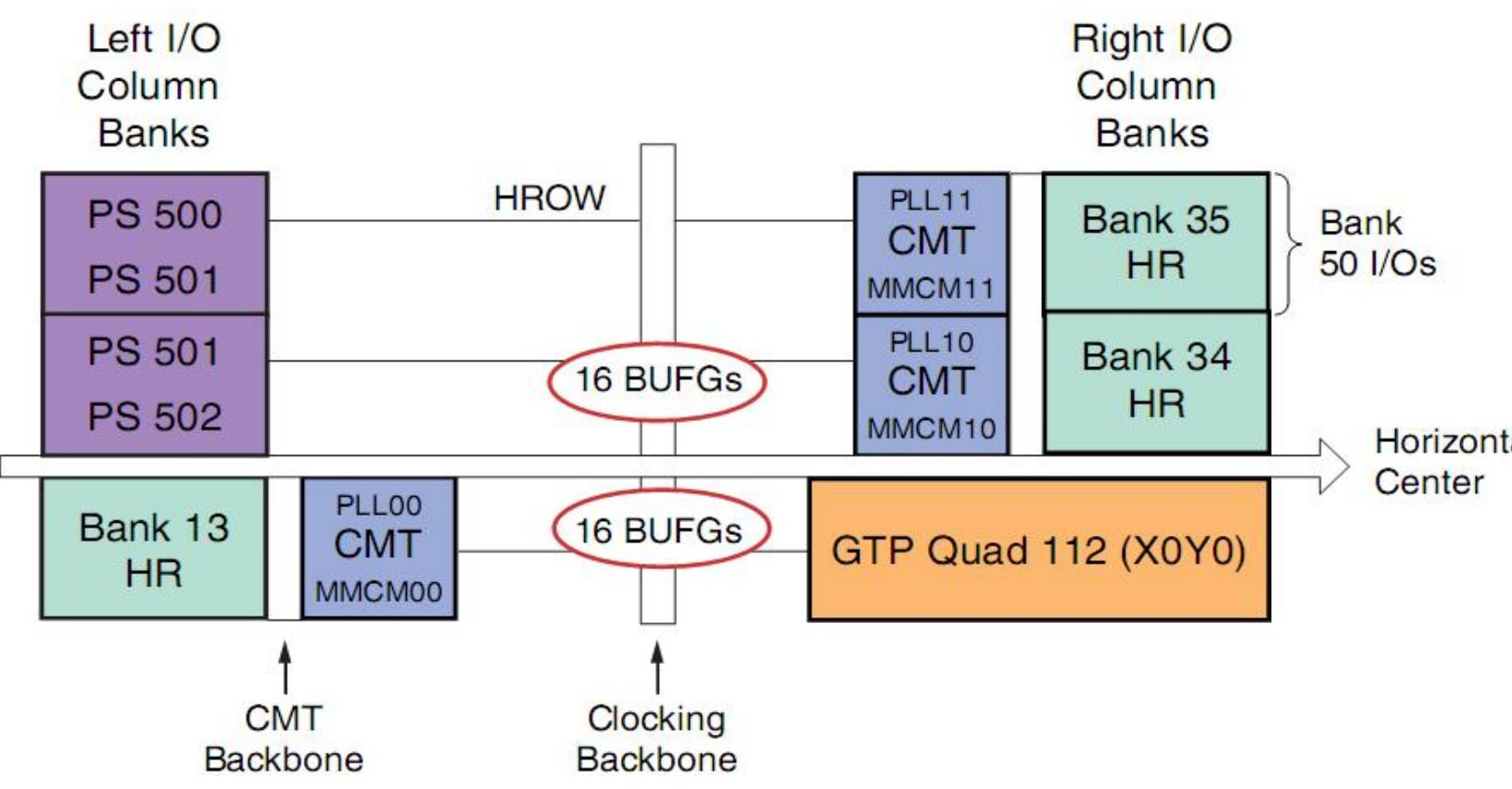
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ZONE	LTR	DESCRIPTION	DATE	APPR.



BANK35 : 3.3V SPARTAN6/ USB/HDMI INOUT
BANK34 : 1.35V DDR3
BANK13 : 3.3V HDMI TRANSMITER
BANK112 : SFP

BANK502 : 1.35V DDR3*2
BANK501 : 2.5V SPARTAN6/ 88E1111
BANK500 : 3.3V SPI FLASH



User I/O Pins	Transceiver Pins	Dedicated Pins	Other Pins	PS MIO Pins	PS DDR Pins
<ul style="list-style-type: none"> ○ IO_LXXY_# ● IO_XX_# 	<ul style="list-style-type: none"> E MGTAVCC_G# V MGTAVTT_G# A MGTVCVAUX_G# < MGTAVTTRCAL G MGTRREF ◆ MGTRFCLK1OP ◆ MGTRFCLK1ON ◆ MGTPRXP ◆ MGTPRXN ◆ MGTPTXP ◆ MGPTXN B PUDC_B ● ADOP/ADON- AD15P/AD15N ⊕ VRN ⊖ VRP ⊗ VREF ⊖ DOS ● MRCC ● SRCC 	<ul style="list-style-type: none"> ■ CFGBVS_0 □ DONE_0 ■ DXP_0 ■ DXN_0 ■ GNDADC_0 ■ INIT_B_0 ■ PROGRAM_B_0 ■ TCK_0 ■ TD_L0 ■ TDO_0 ■ TMS_0 ■ VCCADC_0 ■ VCCBATT_0 ■ VP_0 ■ VN_0 ■ VREFP_0 ■ VREFN_0 	<ul style="list-style-type: none"> ■ GND ■ VCCAUX_IO_G# ■ VCCAUX ■ VCCINT ■ VCCO_# ■ VCCBRAM ■ VCCPINT ■ VCCPAUX ■ VCCO_MIO0 ■ VCCO_MIO1 ■ VCCO_DDR ■ VCCPLL ■ RSVDVCC[3:1] ■ RSVDGND n NC 	<ul style="list-style-type: none"> ● PS_POP_B ○ PS_CLK ○ PS_SRST_B ⊗ PS_MIO_VREF ○ PS_MIO 	<ul style="list-style-type: none"> ○ PS_DDR_CKP ○ PS_DDR_CKN ● PS_DDR_CKE ● PS_DDR_CS_B ○ PS_DDR_RAS_B ○ PS_DDR_CAS_B ● PS_DDR_WE_B ● PS_DDR_BA ● PS_DDR_A ○ PS_DDR_ODT ○ PS_DDR_DRST_B ● PS_DDR_DO ● PS_DDR_DM ● PS_DDR_DOS_P ● PS_DDR_DOS_N ○ PS_DDR_VRP ● PS_DDR_VRN ○ PS_DDR_VREF
<ul style="list-style-type: none"> ○ IO_LXXY_# ● IO_XX_# 	<ul style="list-style-type: none"> E MGTAVCC_G# V MGTAVTT_G# A MGTVCVAUX_G# < MGTAVTTRCAL G MGTRREF ◆ MGTRFCLK1OP ◆ MGTRFCLK1ON ◆ MGTPRXP ◆ MGTPRXN ◆ MGTPTXP ◆ MGPTXN B PUDC_B ● ADOP/ADON- AD15P/AD15N ⊕ VRN ⊖ VRP ⊗ VREF ⊖ DOS ● MRCC ● SRCC 	<ul style="list-style-type: none"> ■ CFGBVS_0 □ DONE_0 ■ DXP_0 ■ DXN_0 ■ GNDADC_0 ■ INIT_B_0 ■ PROGRAM_B_0 ■ TCK_0 ■ TD_L0 ■ TDO_0 ■ TMS_0 ■ VCCADC_0 ■ VCCBATT_0 ■ VP_0 ■ VN_0 ■ VREFP_0 ■ VREFN_0 	<ul style="list-style-type: none"> ■ GND ■ VCCAUX_IO_G# ■ VCCAUX ■ VCCINT ■ VCCO_# ■ VCCBRAM ■ VCCPINT ■ VCCPAUX ■ VCCO_MIO0 ■ VCCO_MIO1 ■ VCCO_DDR ■ VCCPLL ■ RSVDVCC[3:1] ■ RSVDGND n NC 	<ul style="list-style-type: none"> ● PS_POP_B ○ PS_CLK ○ PS_SRST_B ⊗ PS_MIO_VREF ○ PS_MIO 	<ul style="list-style-type: none"> ○ PS_DDR_CKP ○ PS_DDR_CKN ● PS_DDR_CKE ● PS_DDR_CS_B ○ PS_DDR_RAS_B ○ PS_DDR_CAS_B ● PS_DDR_WE_B ● PS_DDR_BA ● PS_DDR_A ○ PS_DDR_ODT ○ PS_DDR_DRST_B ● PS_DDR_DO ● PS_DDR_DM ● PS_DDR_DOS_P ● PS_DDR_DOS_N ○ PS_DDR_VRP ● PS_DDR_VRN ○ PS_DDR_VREF

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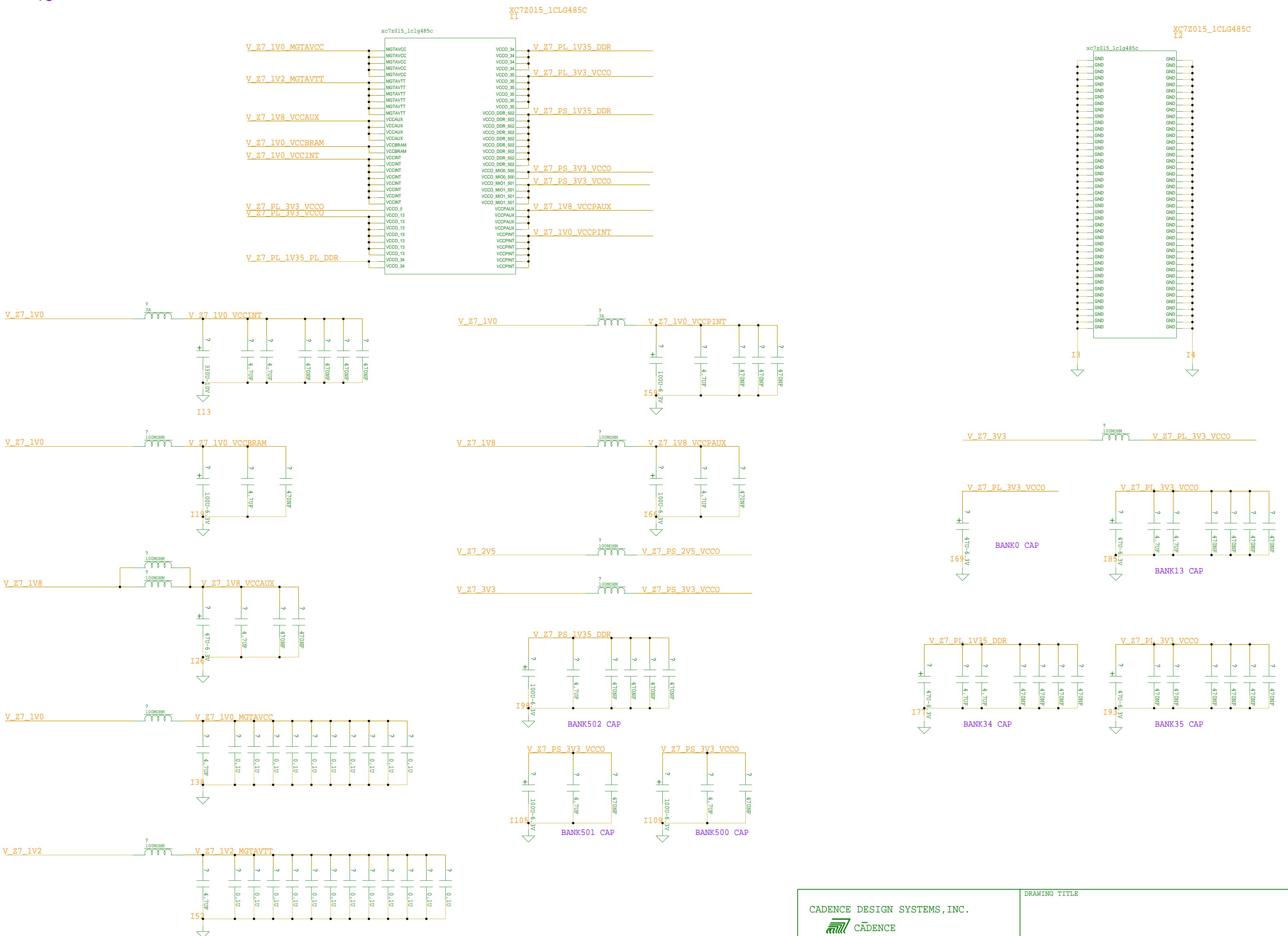
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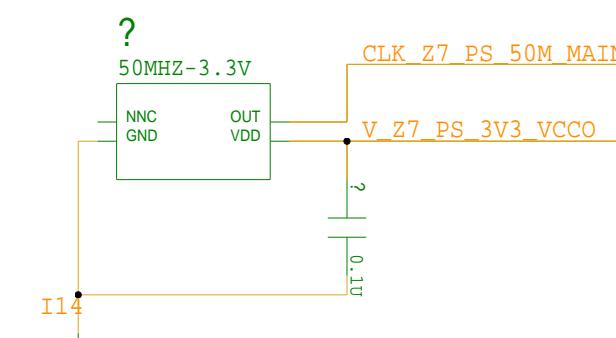
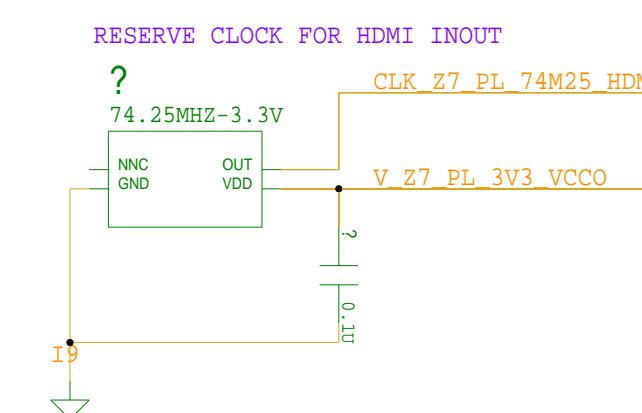
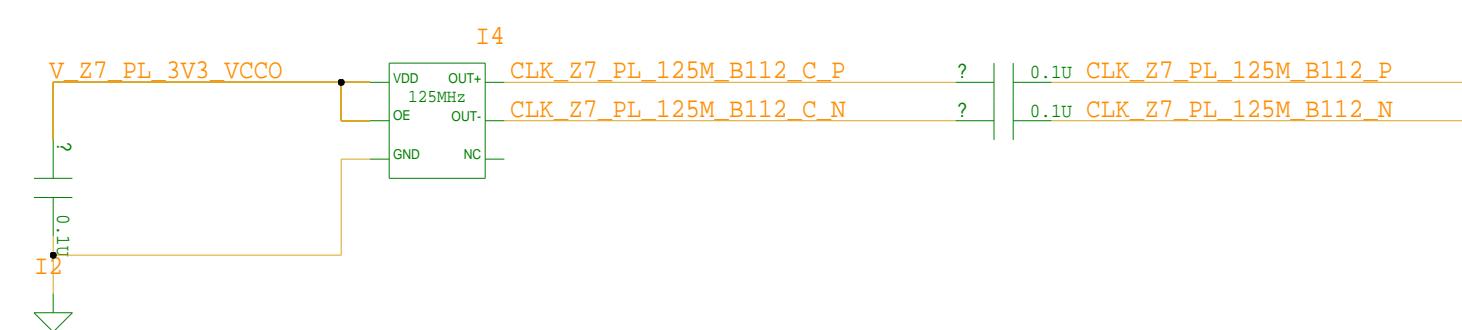
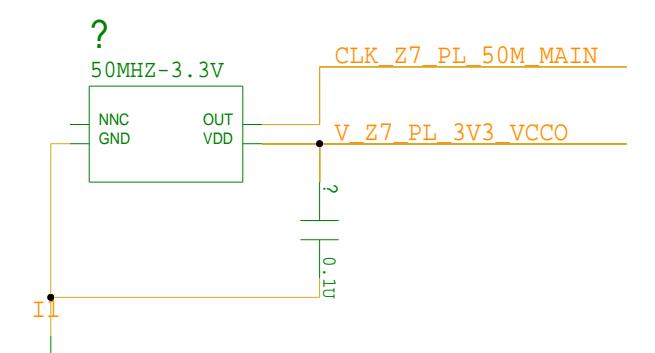
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ZYNQ-7 CLOCK



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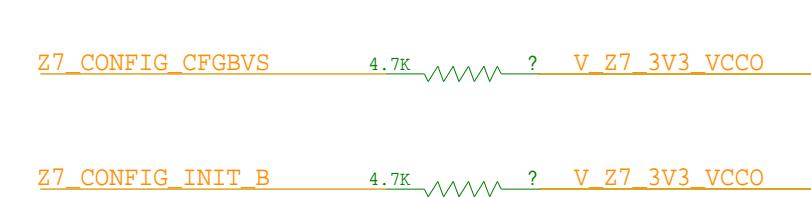
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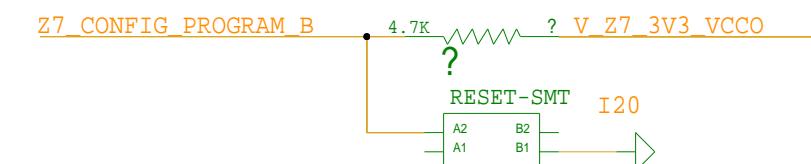
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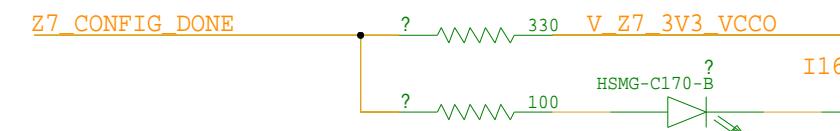
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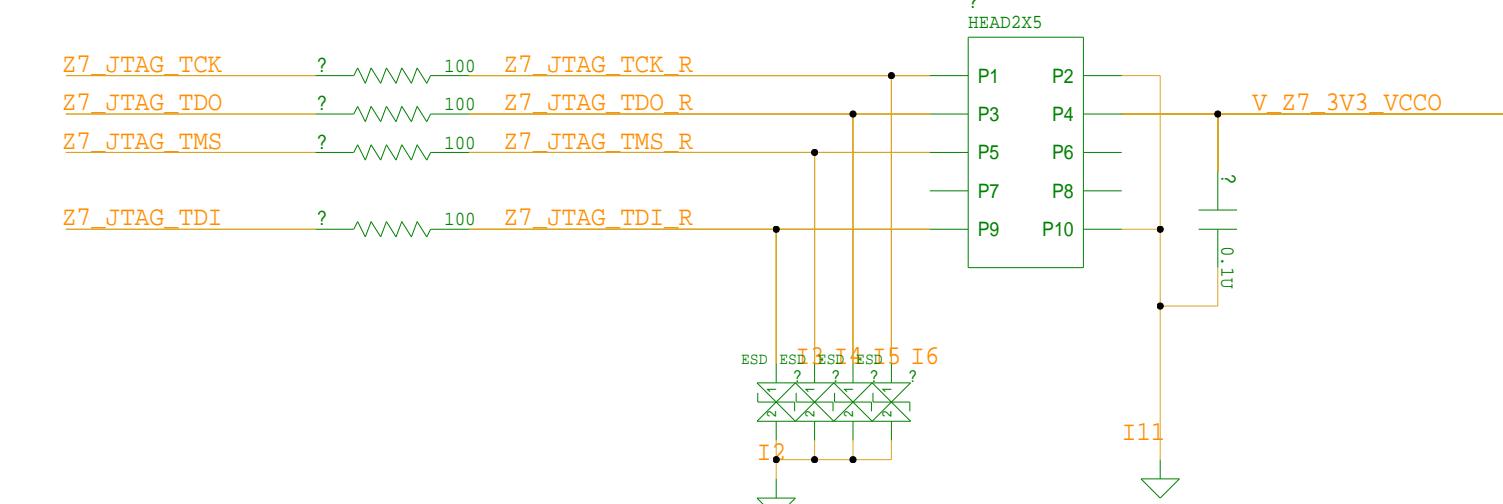
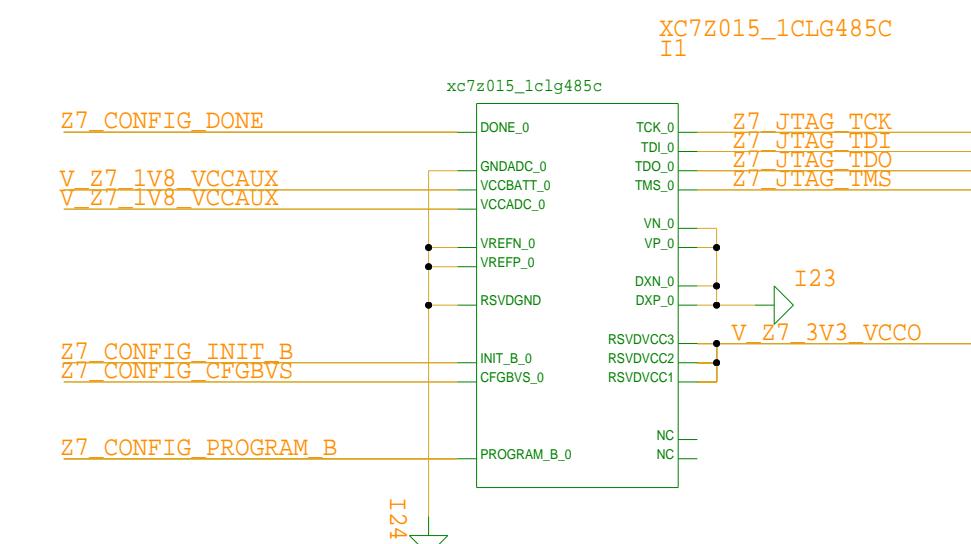
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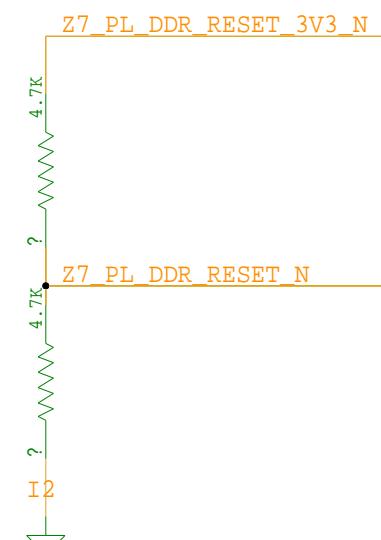
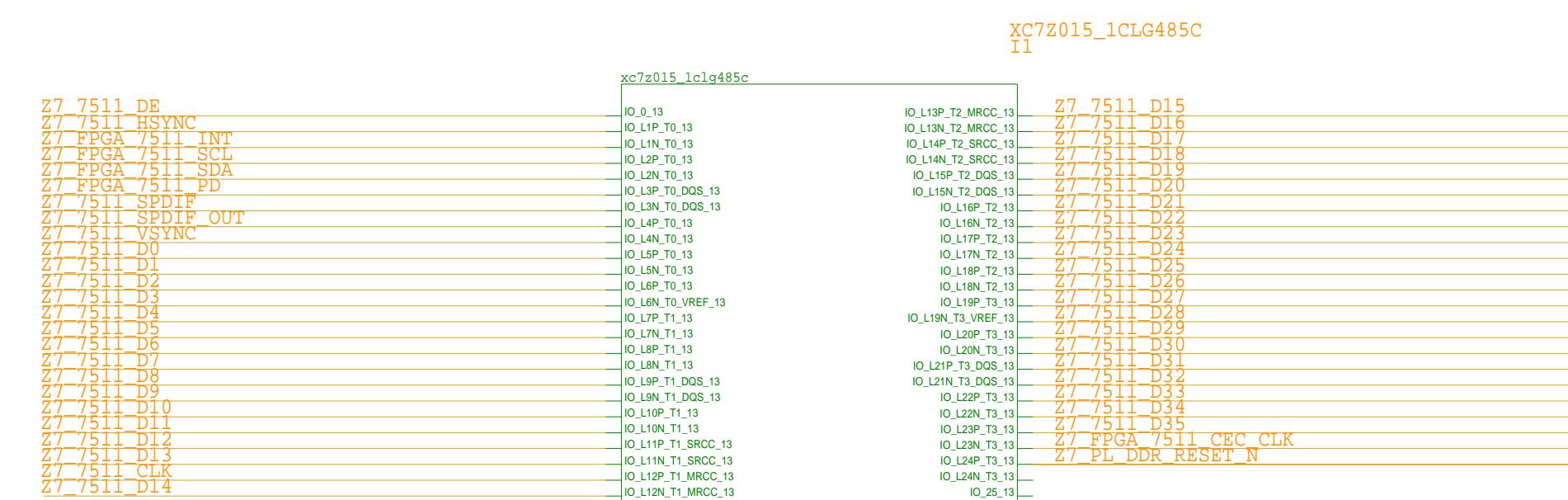
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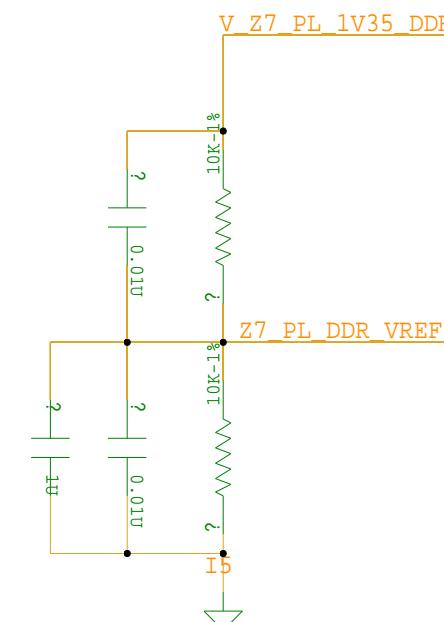
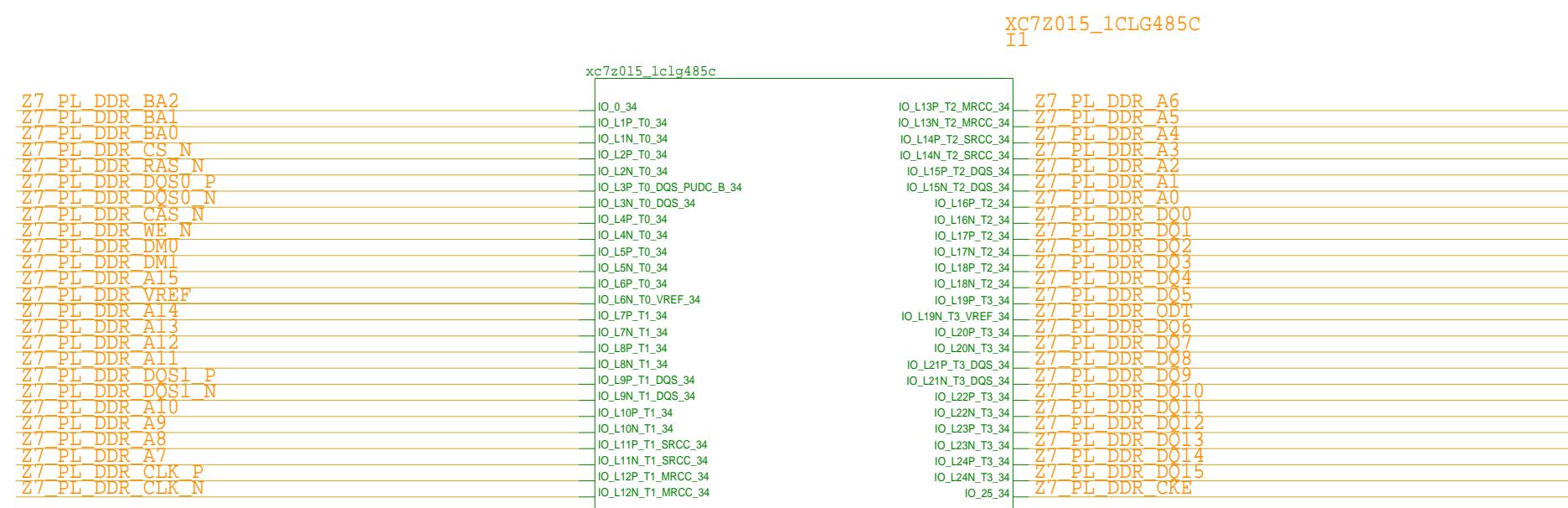
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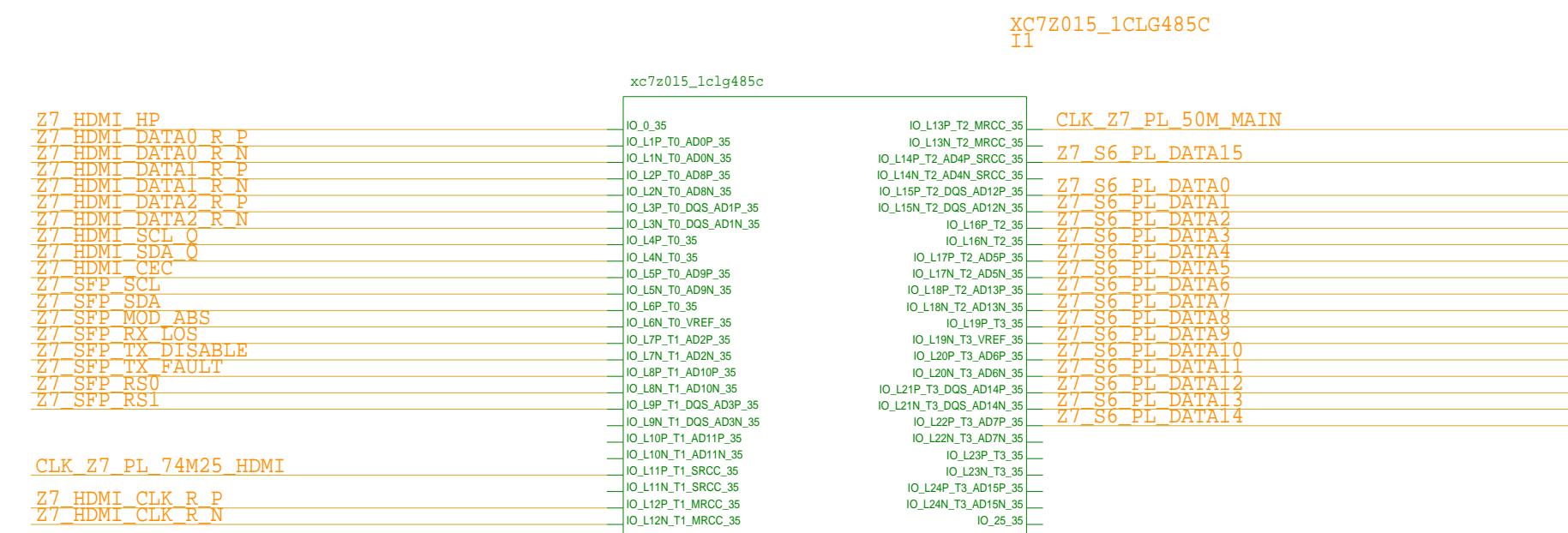
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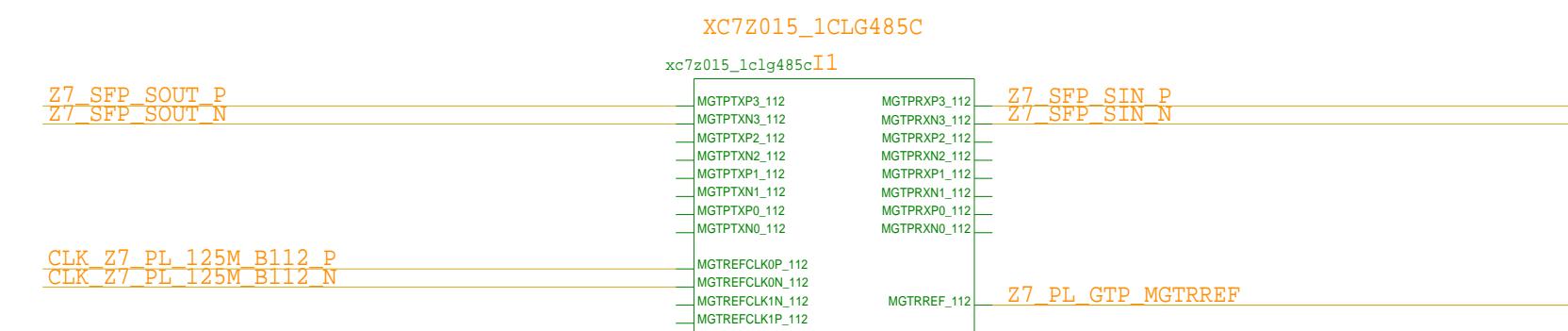
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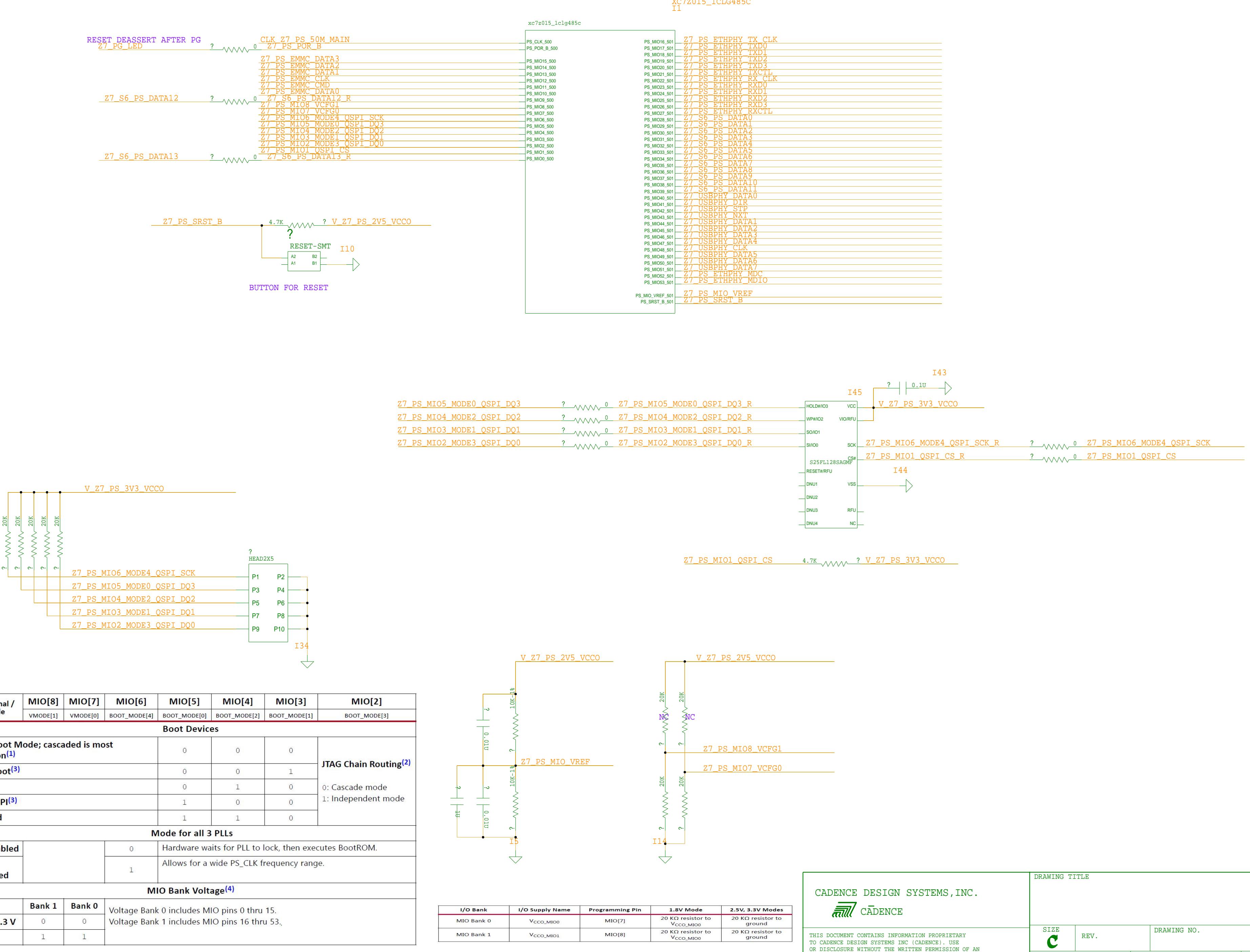
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ZYNQ-7 PS BANK500 / BANK501

REVISIONS

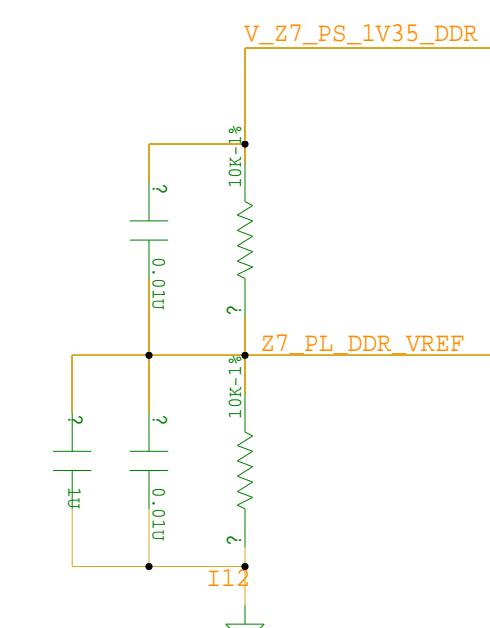
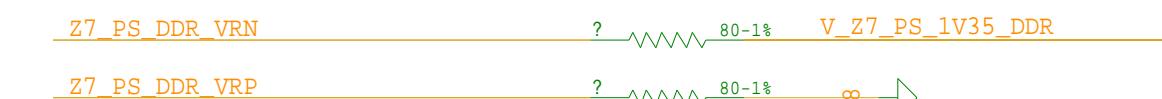
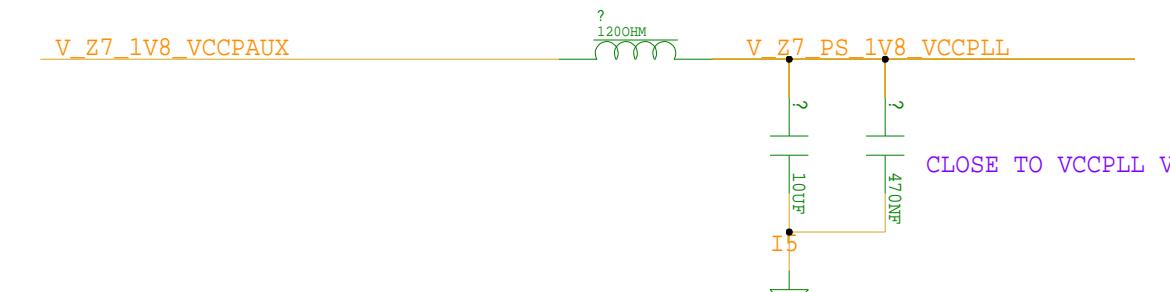
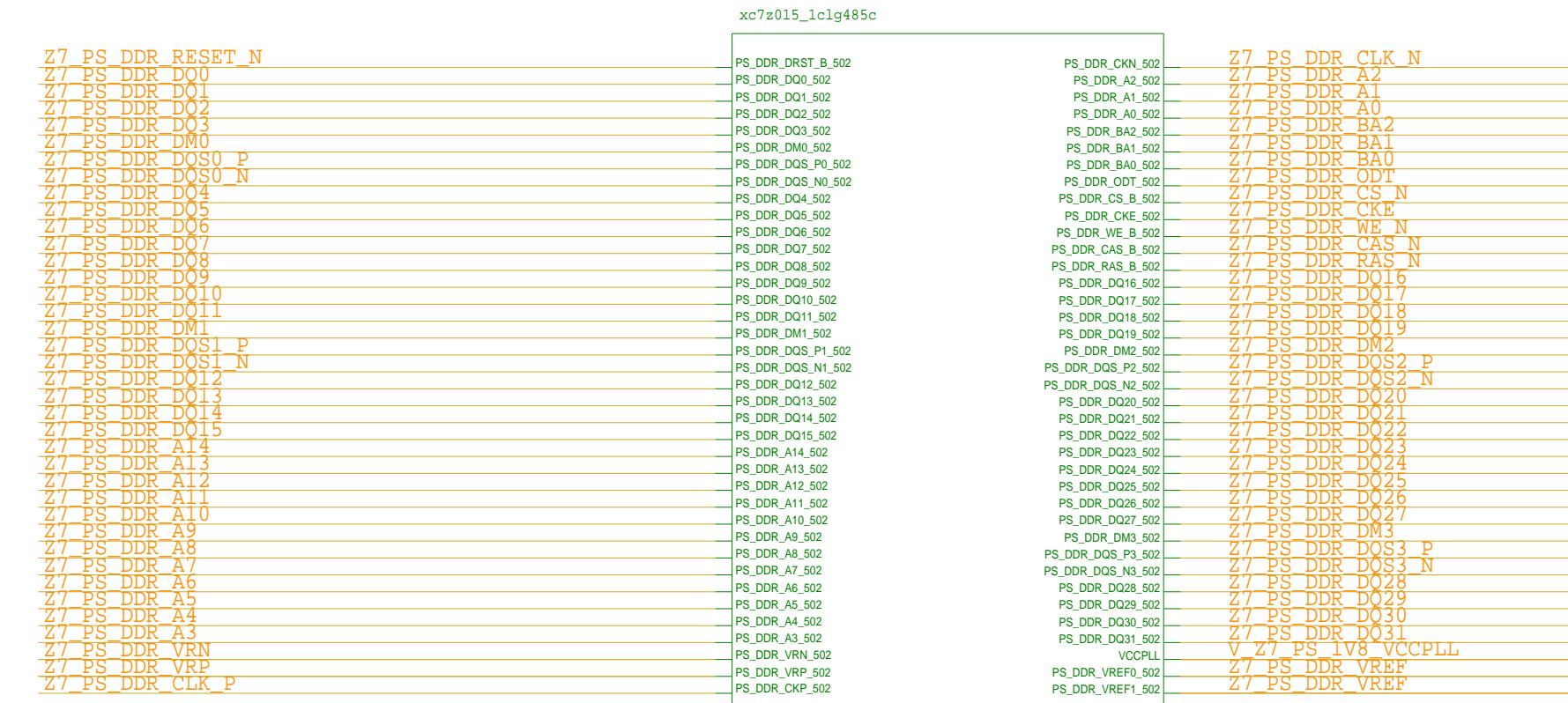
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LINE	ITEM	DESCRIPTION	DATE	APPR.

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