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REVISIONS

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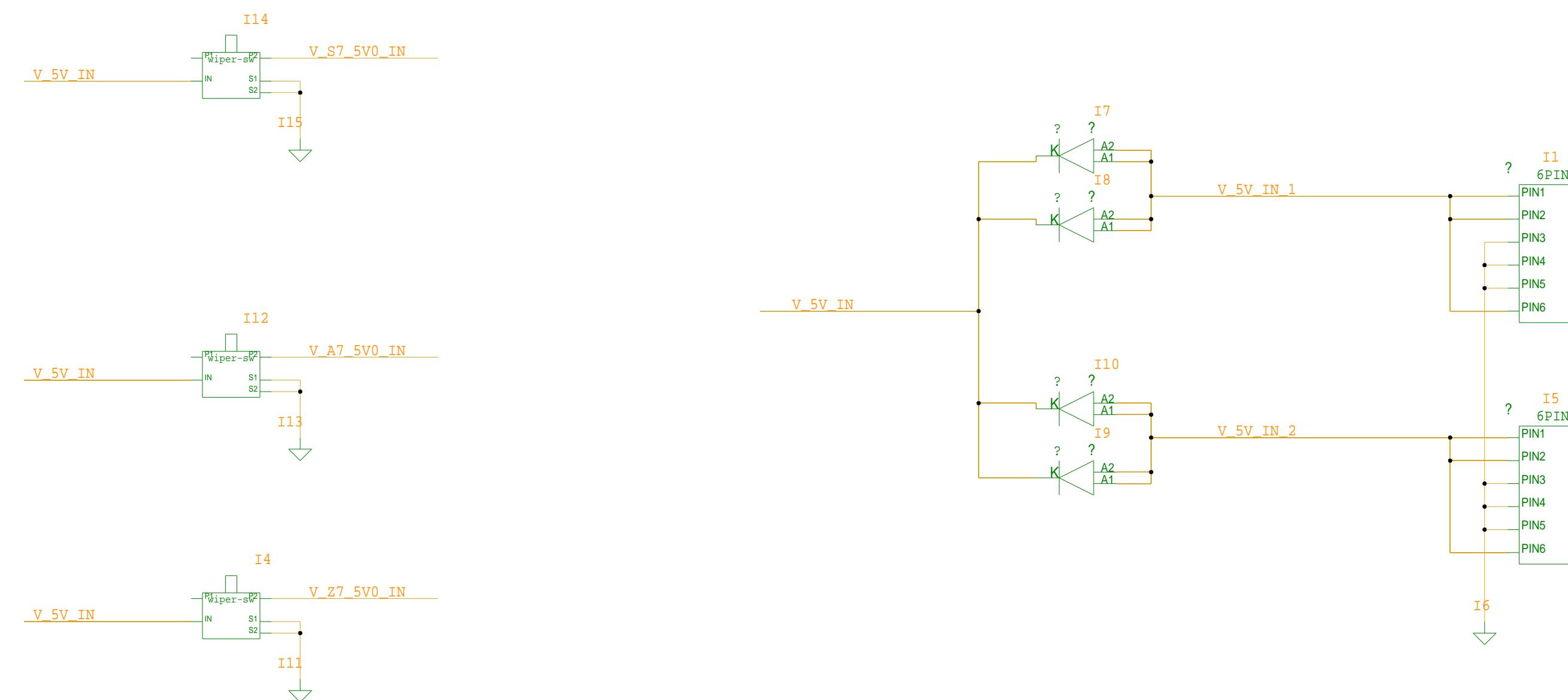
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MAIN POWER

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SPARTAN-7 INDEX

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SPARTAN-7 POWER (1)

$$V_{OUT} = V_{REF} \times (1 + (R_{TOP}/R_{BOT}))$$

$$R_{RT} (\text{k}\Omega) = [14,822/f_{SW} (\text{kHz})]^{1.081}$$

$$V_{IN_STARTUP} = (0.8 \text{ nA} + (0.8 \text{ V}/R_{BOT_EN})) \times \left(R_{TOP_EN} + \frac{R_{BOT_EN} \times 1 \text{ M}\Omega}{R_{BOT_EN} + 1 \text{ M}\Omega} \right)$$

where:

R_{TOP_EN} is the resistor from V_{IN} to EN.

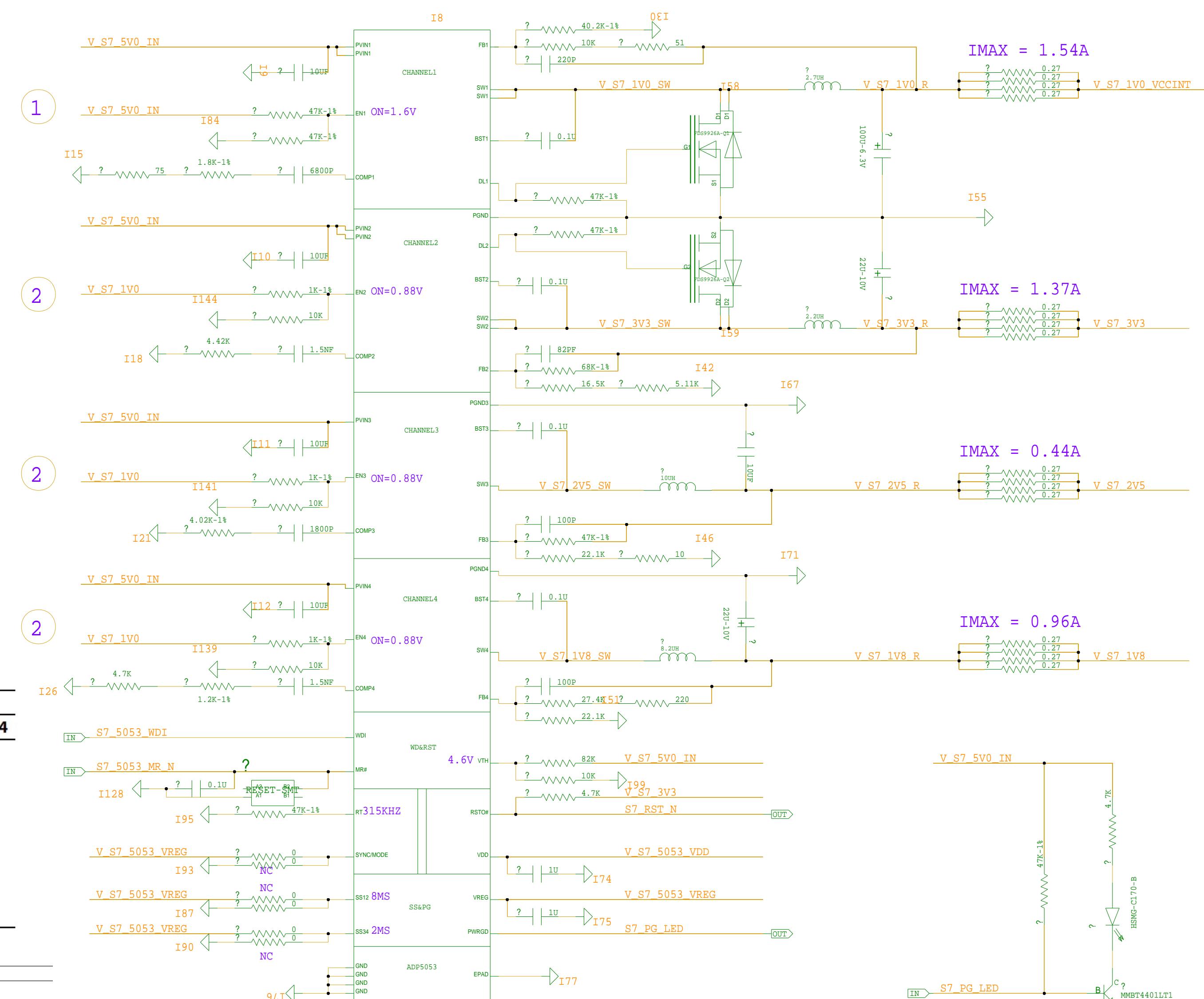
R_{BOT_EN} is the resistor from EN to ground.

Table 9. Soft Start Time Set by the SS12 and SS34 Pins

R_{TOP} ($\text{k}\Omega$)	R_{BOT} ($\text{k}\Omega$)	Soft Start Time			
		Channel 1	Channel 2	Channel 3	Channel 4
0	N/A ¹	2 ms	2 ms	2 ms	2 ms
100	600	2 ms	Parallel	2 ms	4 ms
200	500	2 ms	8 ms	2 ms	8 ms
300	400	4 ms	2 ms	4 ms	2 ms
400	300	4 ms	4 ms	4 ms	4 ms
500	200	8 ms	2 ms	4 ms	8 ms
600	100	8 ms	Parallel	8 ms	2 ms
N/A ¹	0	8 ms	8 ms	8 ms	8 ms

Table 16. Factory Default Options

Option	Default Value
Channel 1 Output Voltage	0.8V adjustable output
Channel 2 Output Voltage	0.8V adjustable output
Channel 3 Output Voltage	0.8V adjustable output
Channel 4 Output Voltage	0.8V adjustable output
PWRGD Pin (Pin 20) Output	Monitor Channel 1 output
Output Discharge Function	Enabled for all four buck regulators
Switching Frequency on Channel 1	1 x switching frequency set by the RT pin
Switching Frequency on Channel 3	1 x switching frequency set by the RT pin
SYNC/MODE Pin (Pin 43) Function	Forced PWM/automatic PWM/PSM mode setting with the ability to synchronize to an external clock
Hiccup Protection	Enabled for overcurrent events
Short-Circuit Latch-Off Function	Disabled for output short-circuit events
Oversupply Latch-Off Function	Disabled for output oversupply events
Reset Timeout Period	200 ms
Watchdog Timeout Period	1.6 sec
Manual Reset Input Mode	Processor manual reset mode



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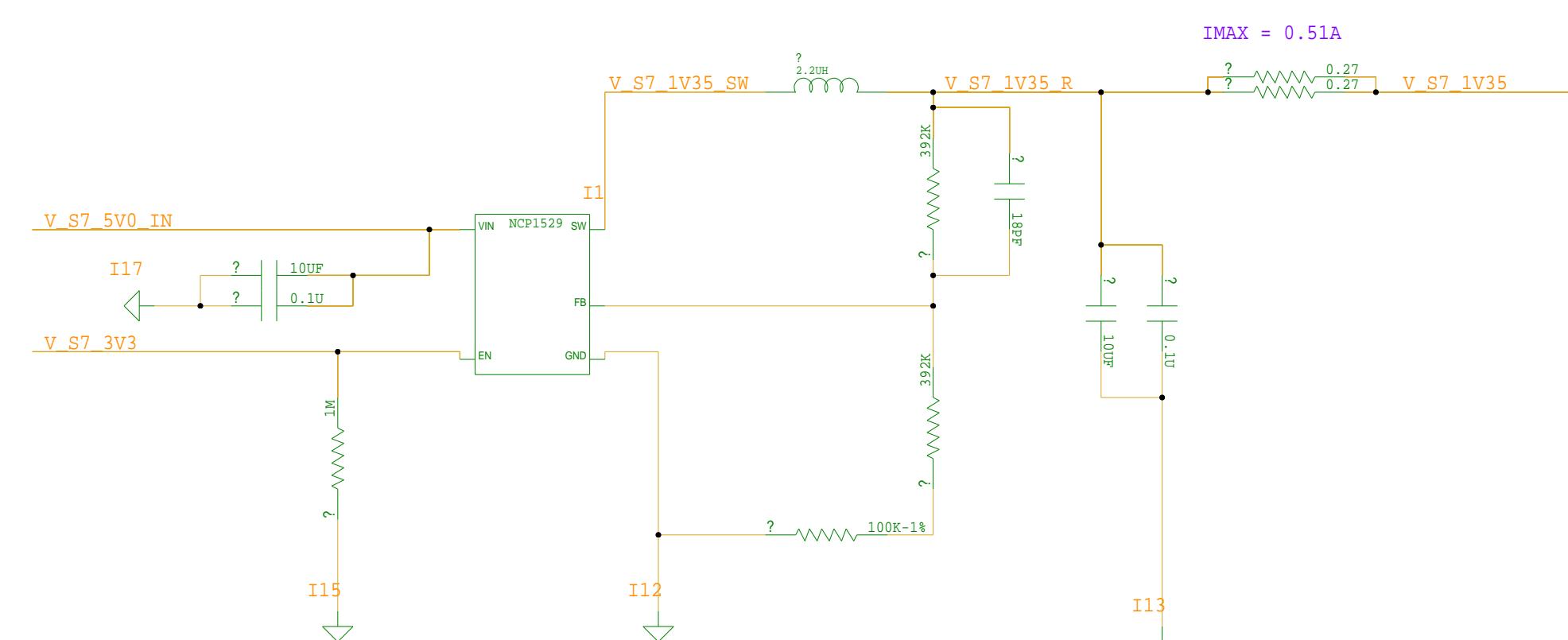
SPARTAN-7 POWER (2)

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$$V_{out} = V_{FB} \times (1 + R1/R2)$$

- V_{OUT} : Output Voltage (V)
- V_{FB} : Feedback Voltage = 0.6 V
- $R1$: Feedback Resistor from V_{OUT} to FB
- $R2$: Feedback Resistor from FB to GND

3



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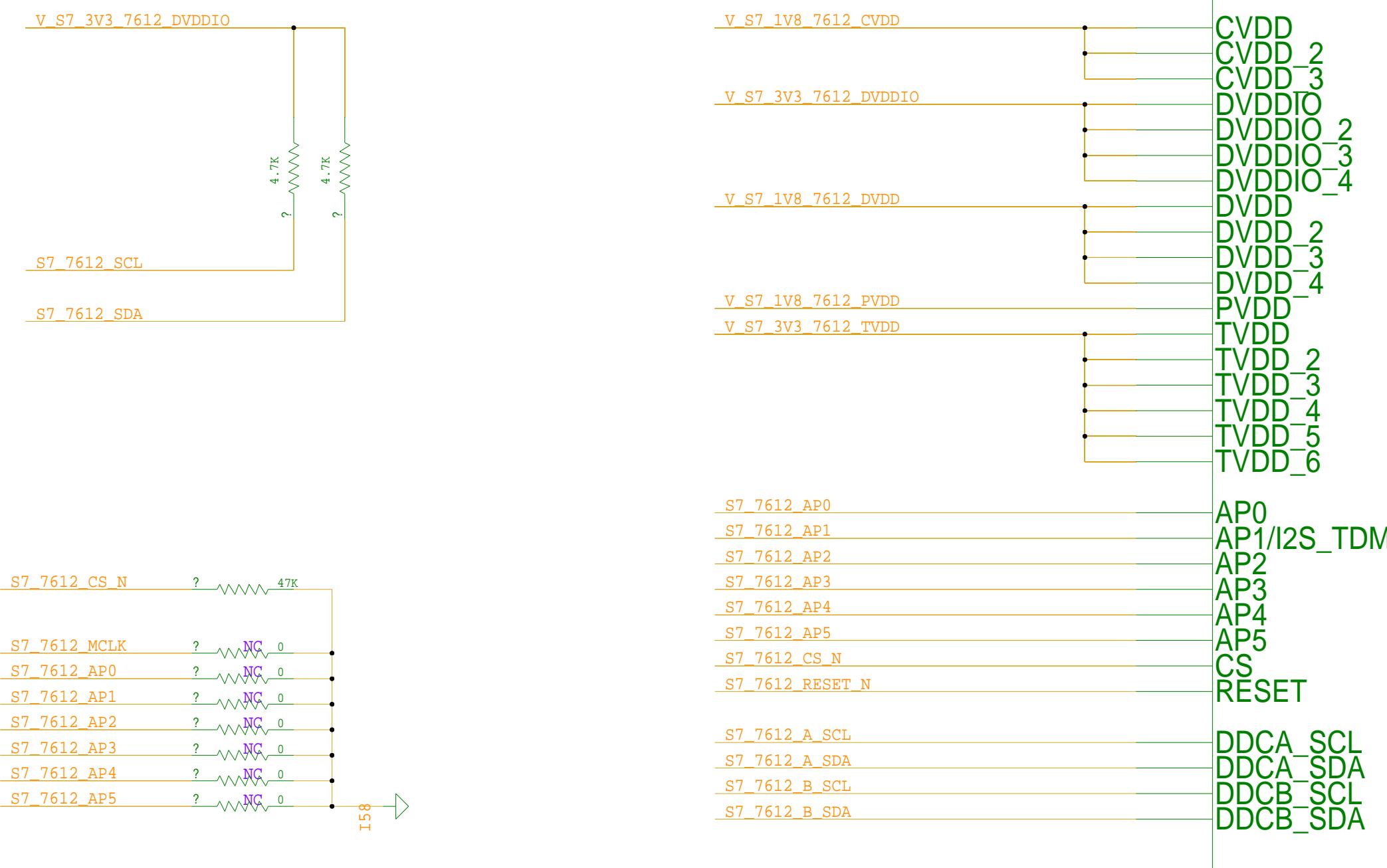
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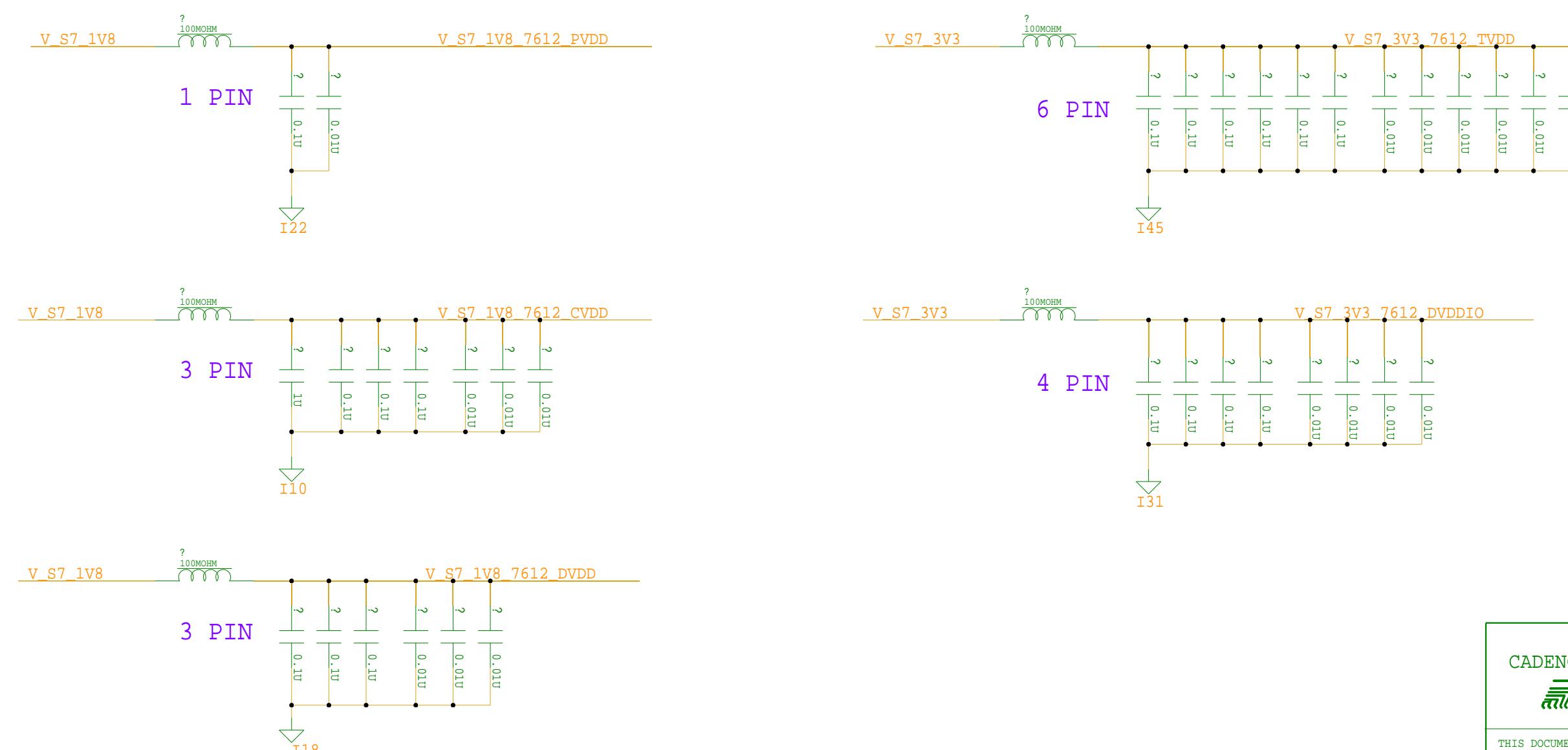
SPARTAN-7 HDMI RECEIVER (1)

REVISED

ZONE	LTR	DESCRIPTION	DATE	APPR.



DE	S7_7612_DE
XTALP	S7_7612_XTAL_P
XTALN	S7_7612_XTAL_N
SDA	S7_7612_SDA
SCLK/INT2	S7_7612_INT2
SCL	S7_7612_SCL
RXB_5V	V_S7_7612_B_5V0
RXA_5V	V_S7_7612_A_5V0
MCLK/INT2	S7_7612_MCLK
INT1	S7_7612_INT1
HPA_B	S7_7612_B_HP
HPA_A/INT2	S7_7612_A_HP
RXB_C+	S7_7612_B_CLK_P
RXB_C-	S7_7612_B_CLK_N
RXB_2-	S7_7612_B_DATA2_N
RXB_1-	S7_7612_B_DATA1_N
RXB_0-	S7_7612_B_DATA0_N
RXB_2+	S7_7612_B_DATA2_P
RXB_1+	S7_7612_B_DATA1_P
RXB_0+	S7_7612_B_DATA0_P
RXA_C+	S7_7612_A_CLK_P
RXA_C-	S7_7612_A_CLK_N
RXA_2-	S7_7612_A_DATA2_N
RXA_1-	S7_7612_A_DATA1_N
RXA_0-	S7_7612_A_DATA0_N
RXA_2+	S7_7612_A_DATA2_P
RXA_1+	S7_7612_A_DATA1_P
RXA_0+	S7_7612_A_DATA0_P



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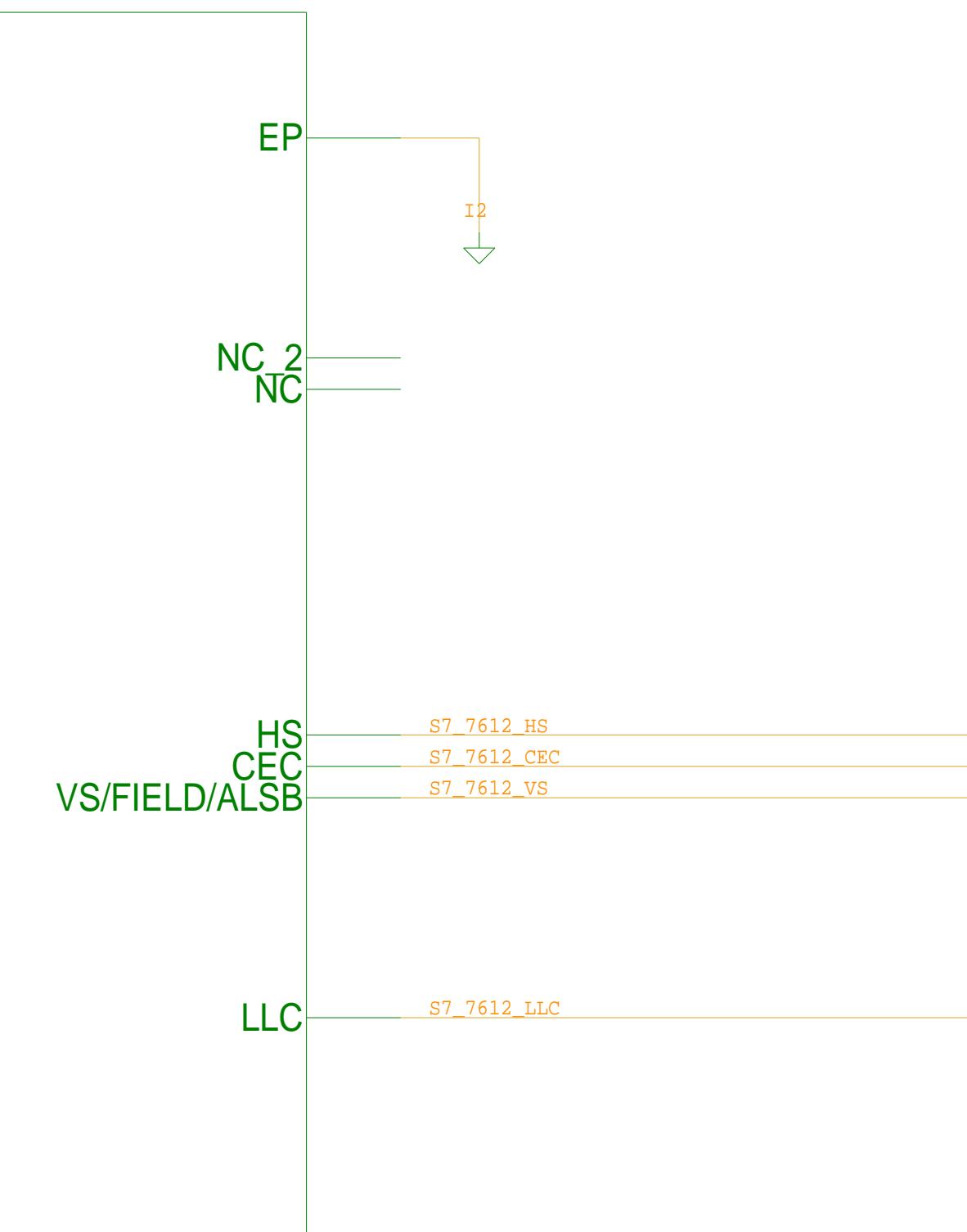
SPARTAN-7 HDMI RECEIVER (2)

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPR.

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S7_7612_P4
S7_7612_P5
S7_7612_P6
S7_7612_P7
S7_7612_P8
S7_7612_P9
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S7_7612_P35

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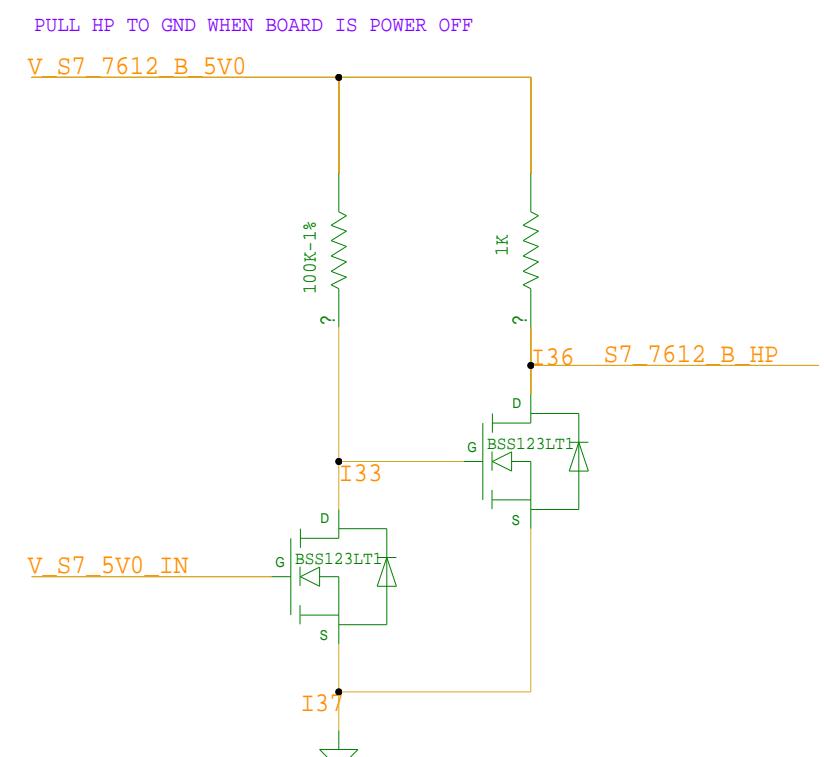
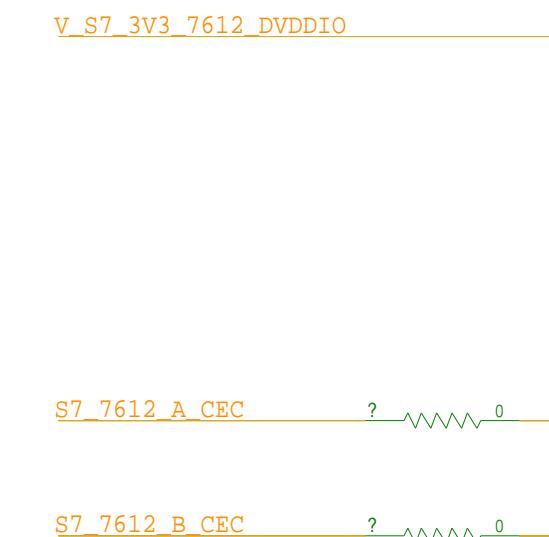
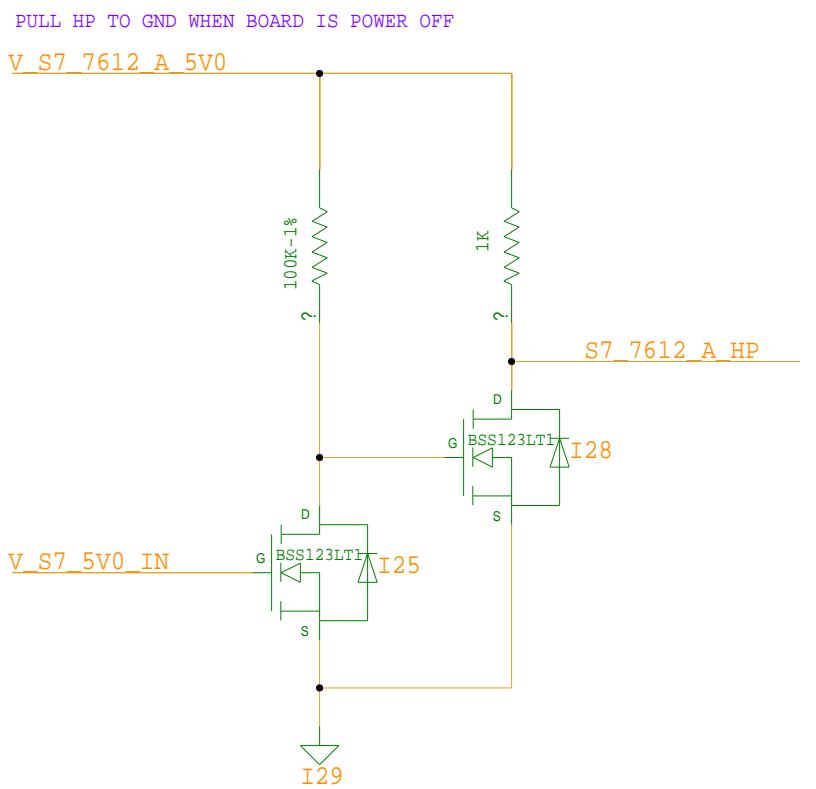
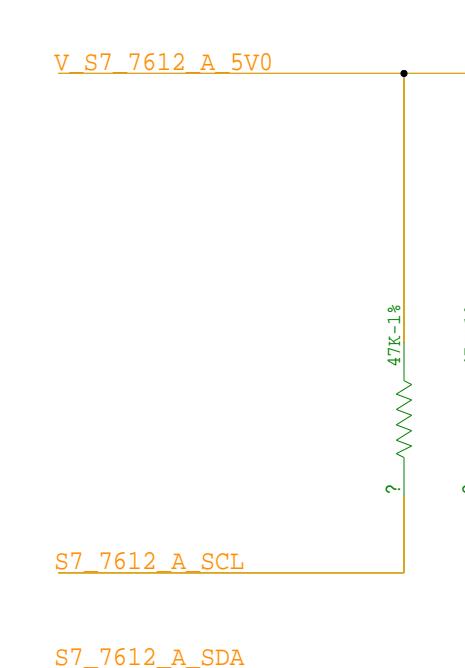
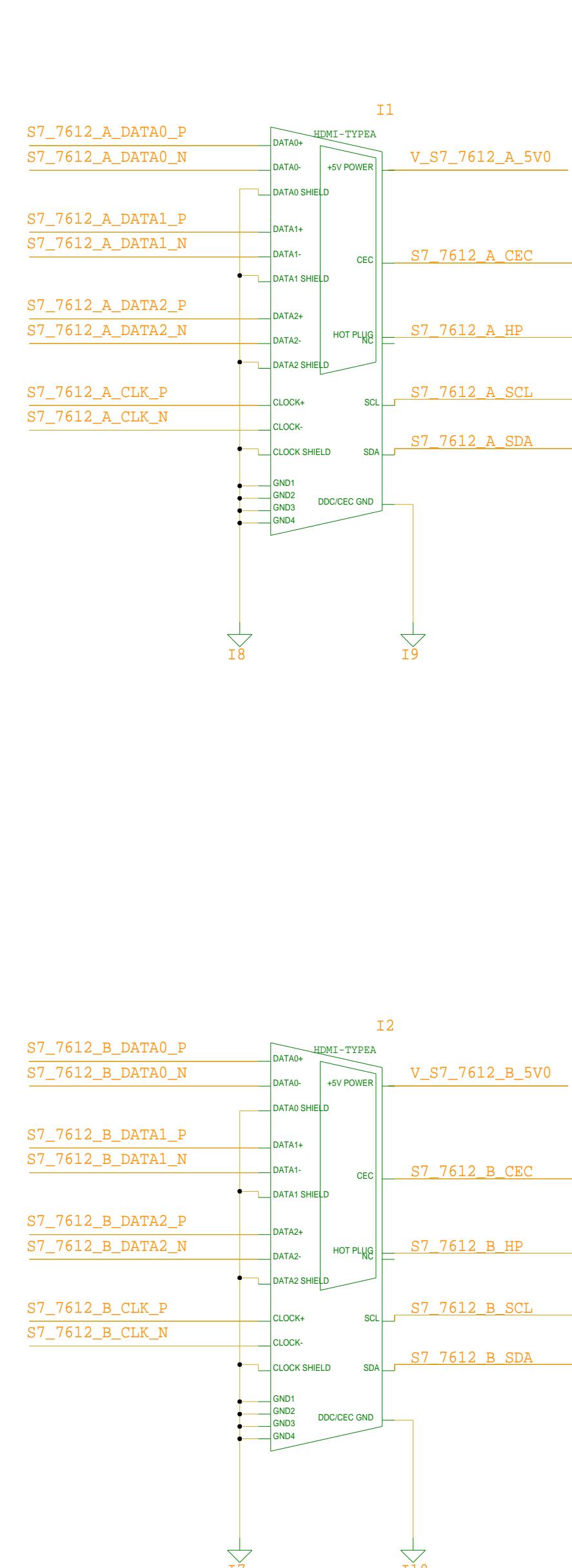
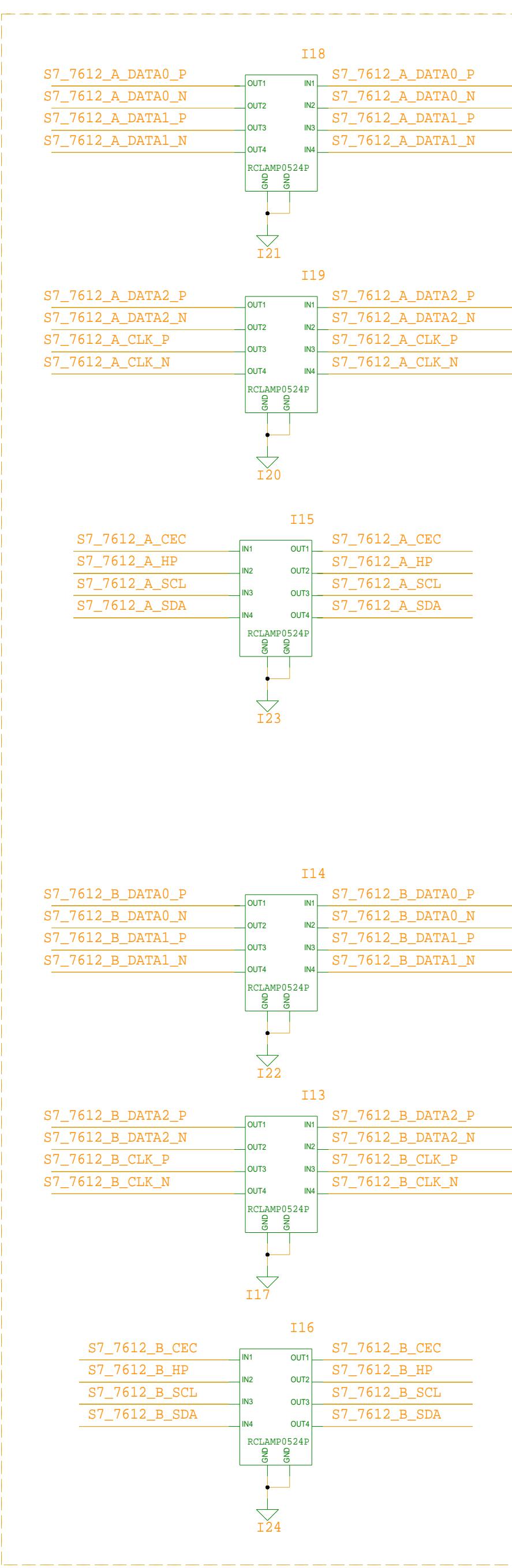
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SPARTAN-7 HDMI RECEIVER (3)

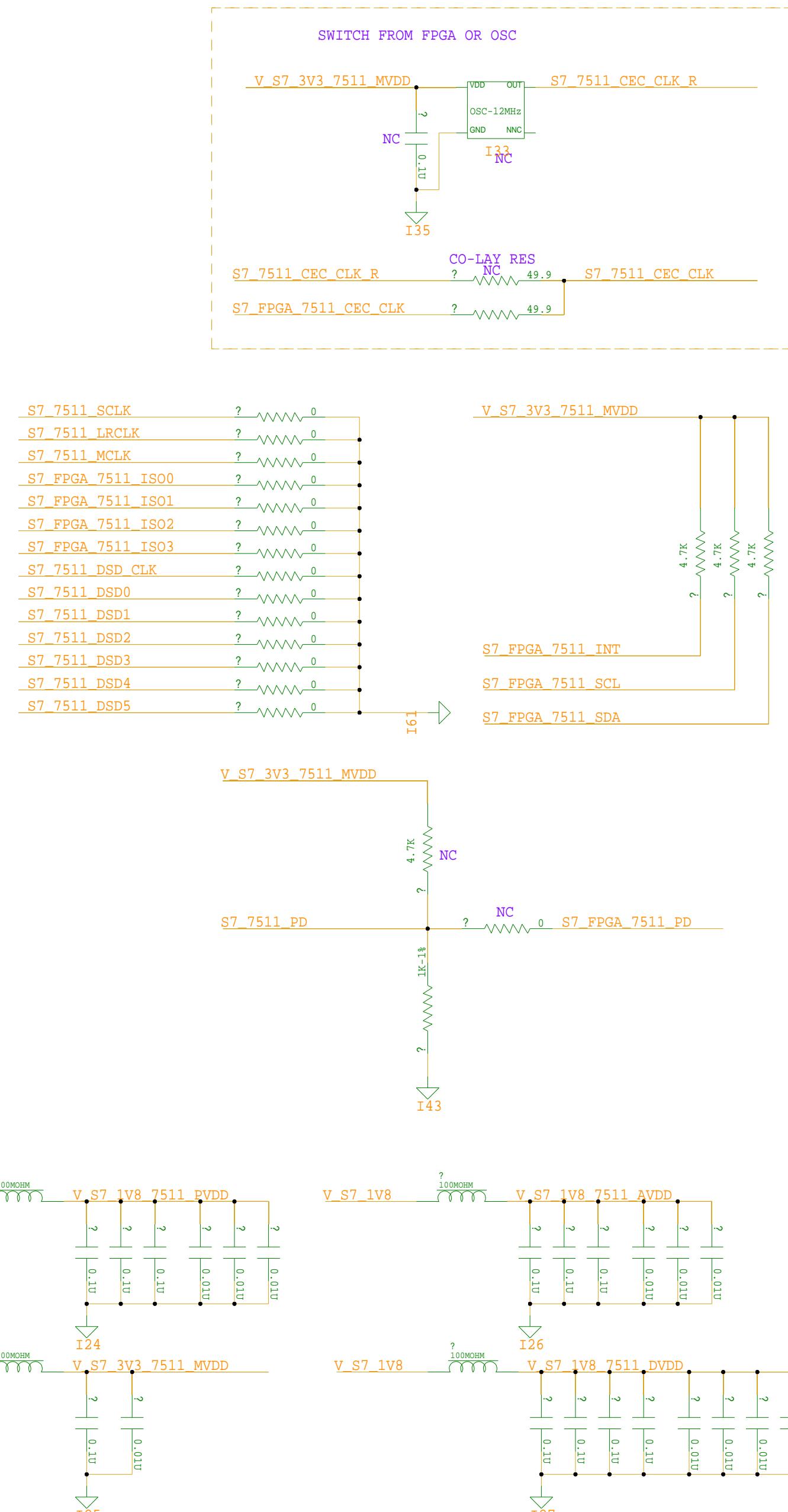
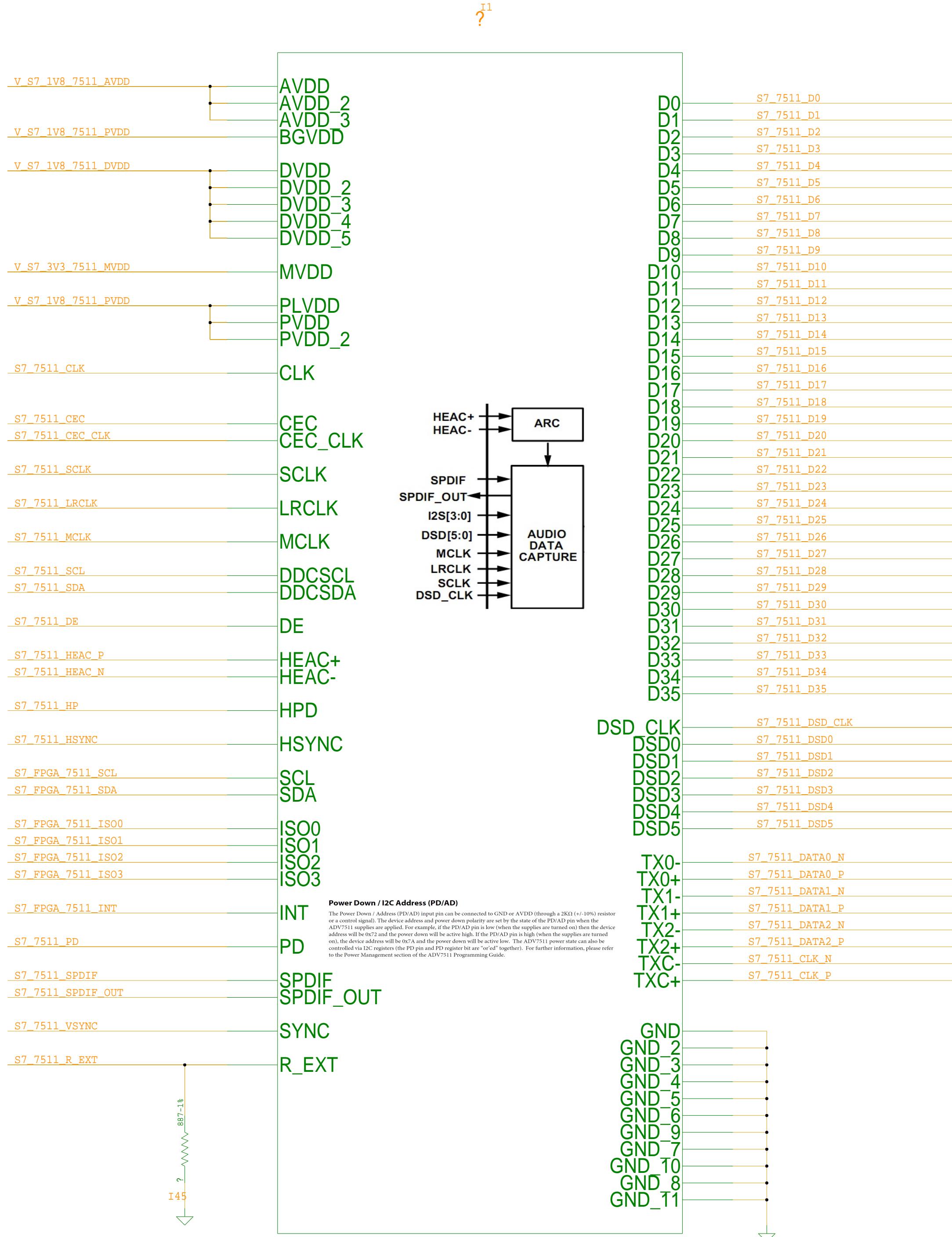
CHANGE CONNECTION DUE TO LAYOUT



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SPARTAN-7 HDMI TRANSMITTER (1)



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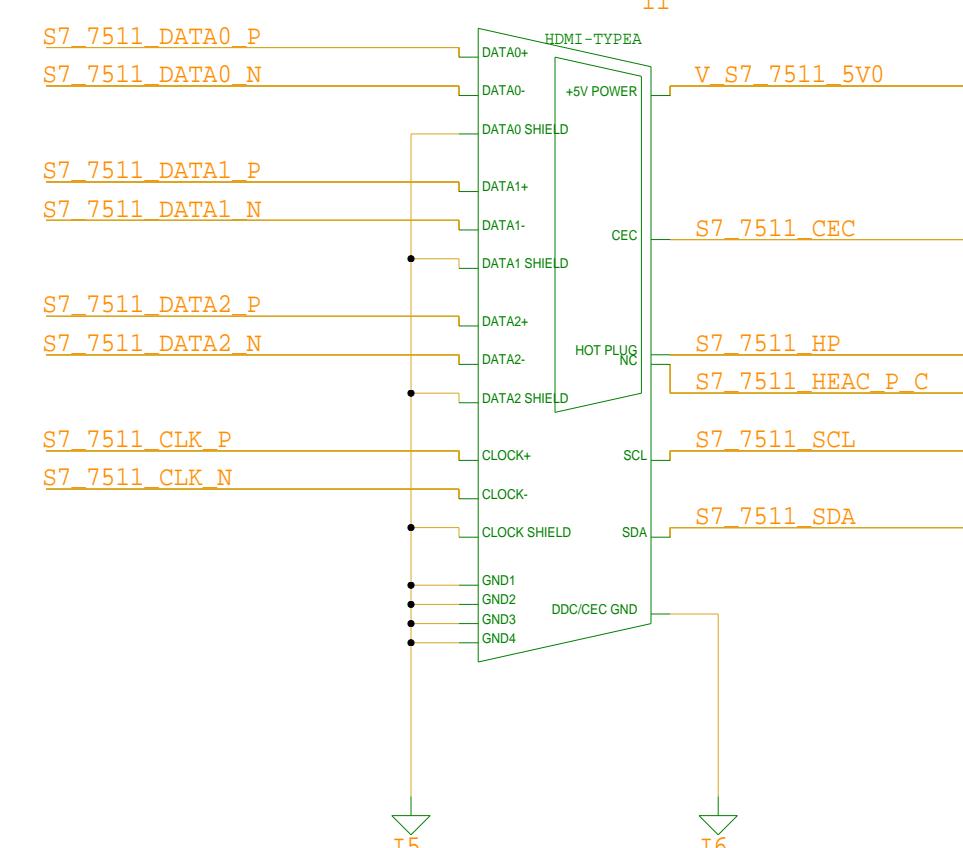
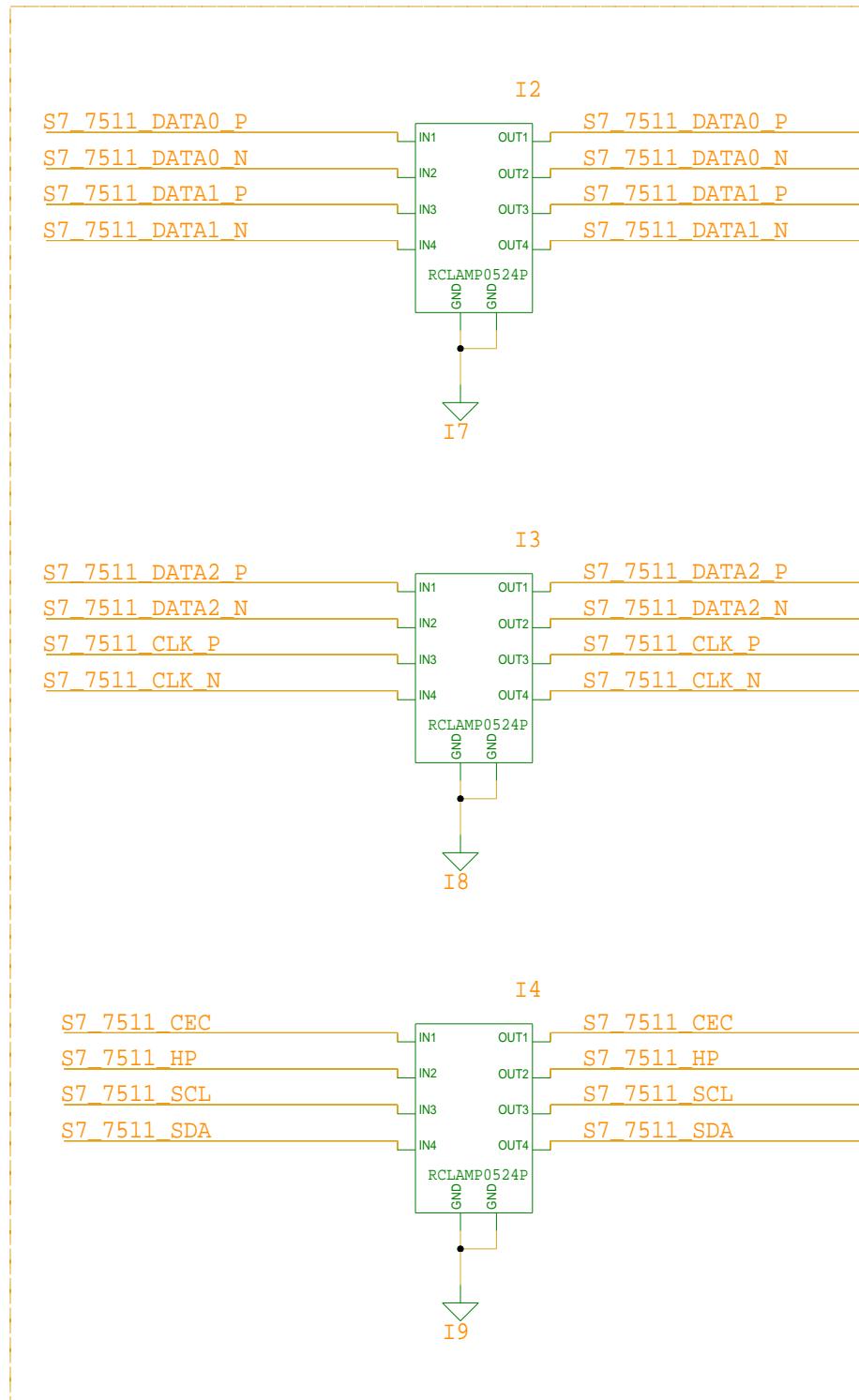
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SPARTAN-7 HDMI TRANSMITTER (2)

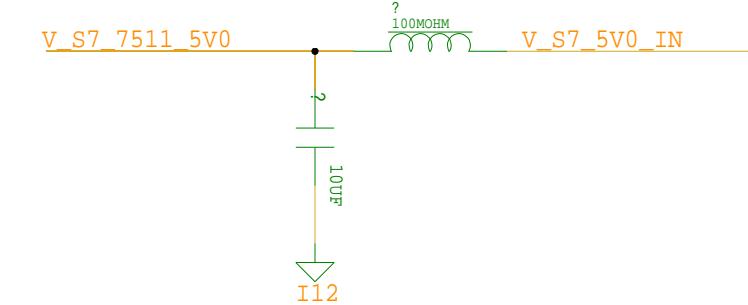
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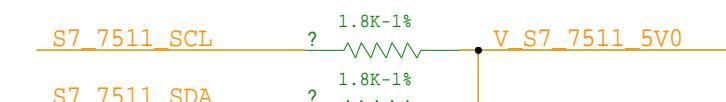
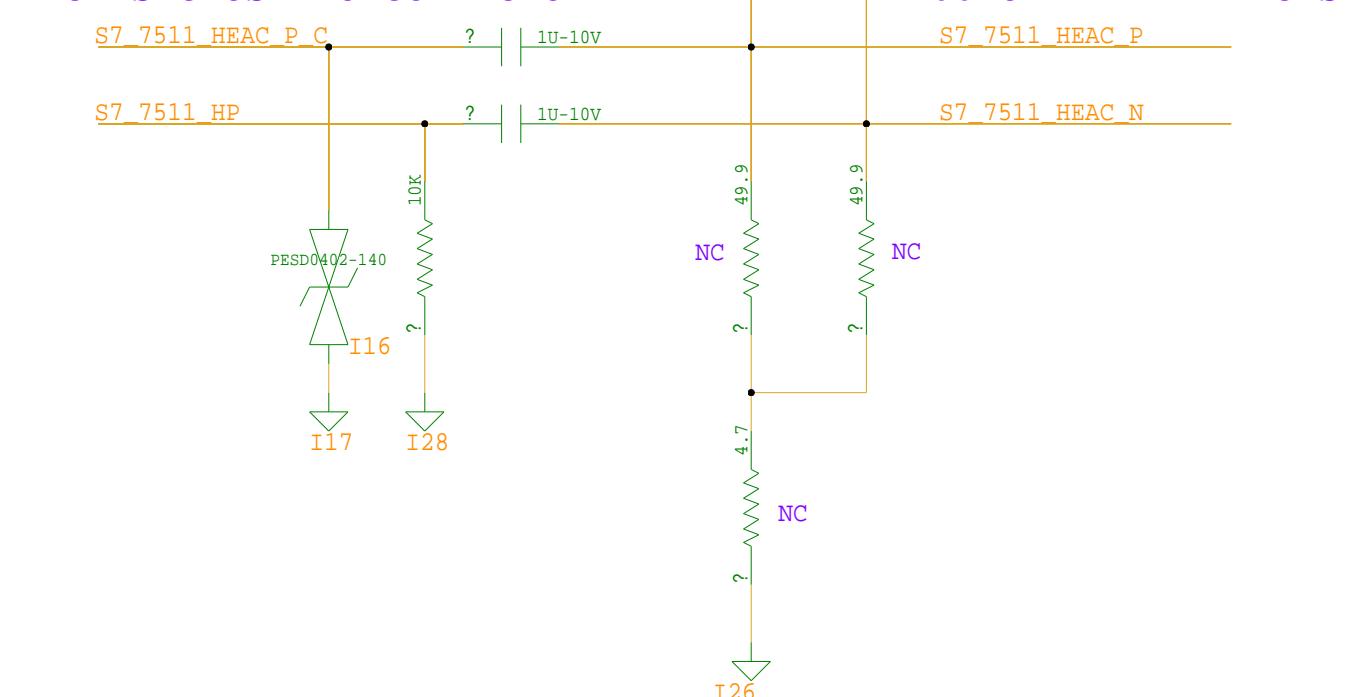
CHANGE CONNECTION DUE TO LAYOUT



CLOSE TO HDMI CONNECTOR



CAPS CLOSE TO CONNECTOR



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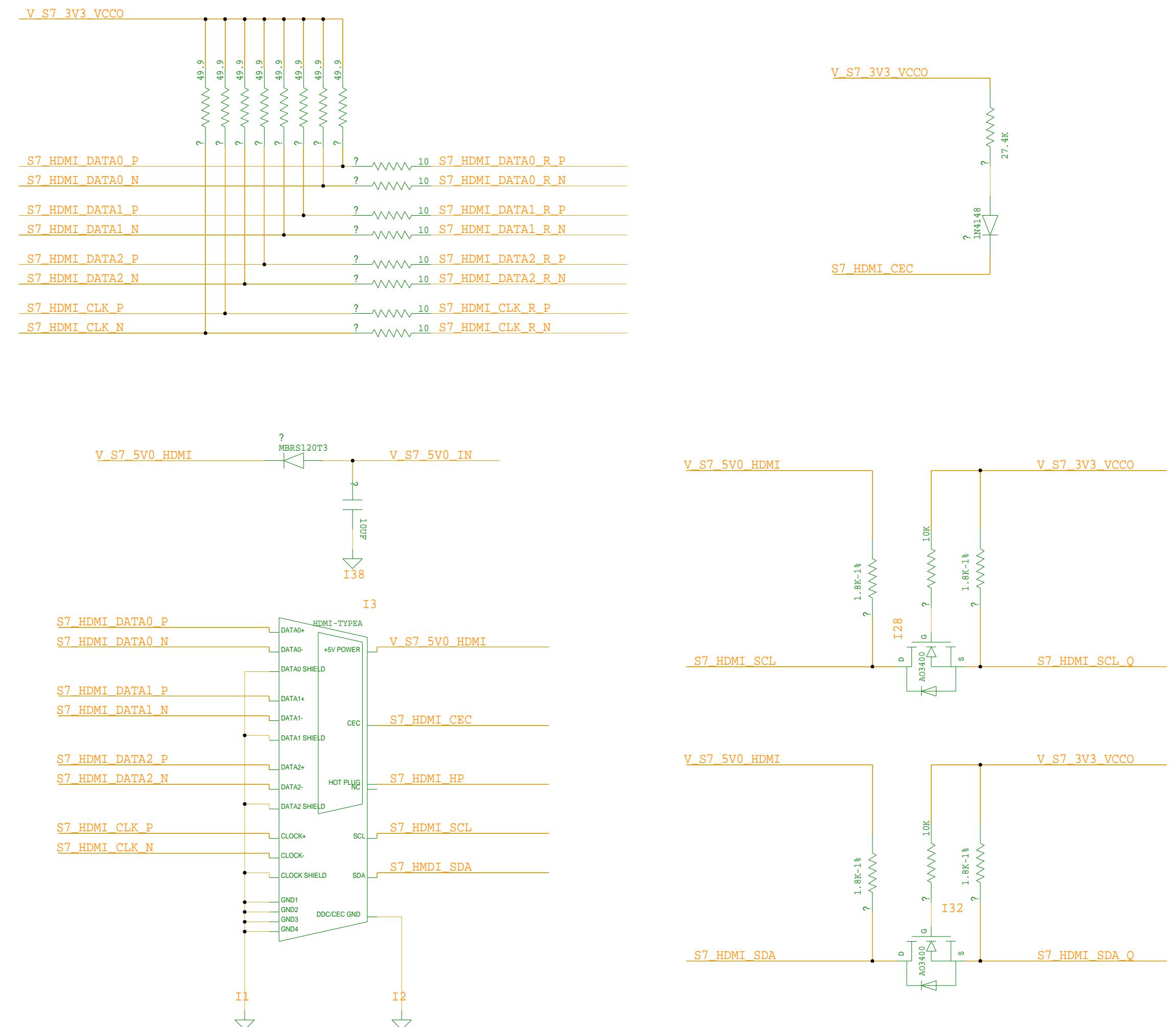
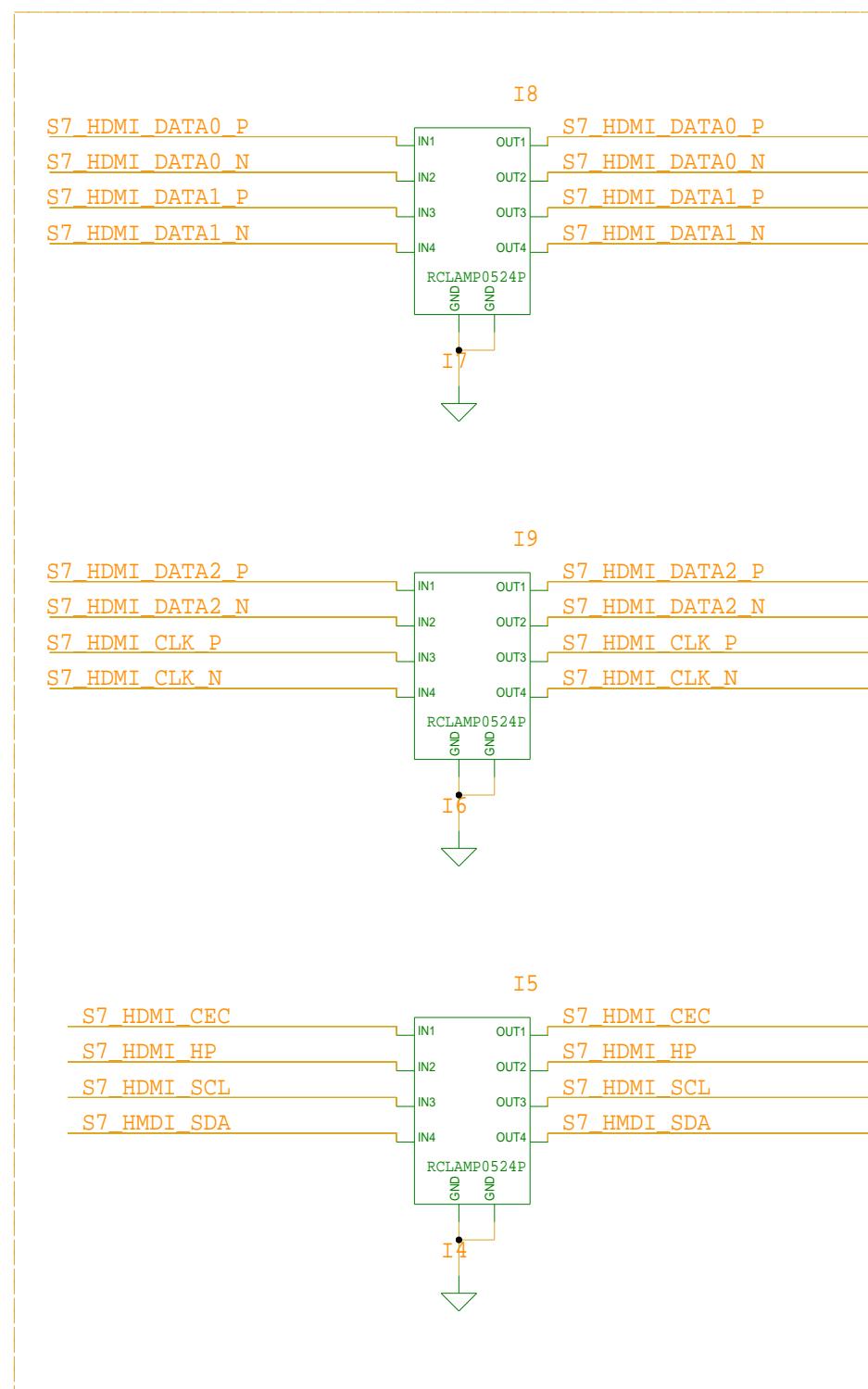
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SPARTAN-7 HDMI INOUT

CHANGE CONNECTION DUE TO LAYOUT



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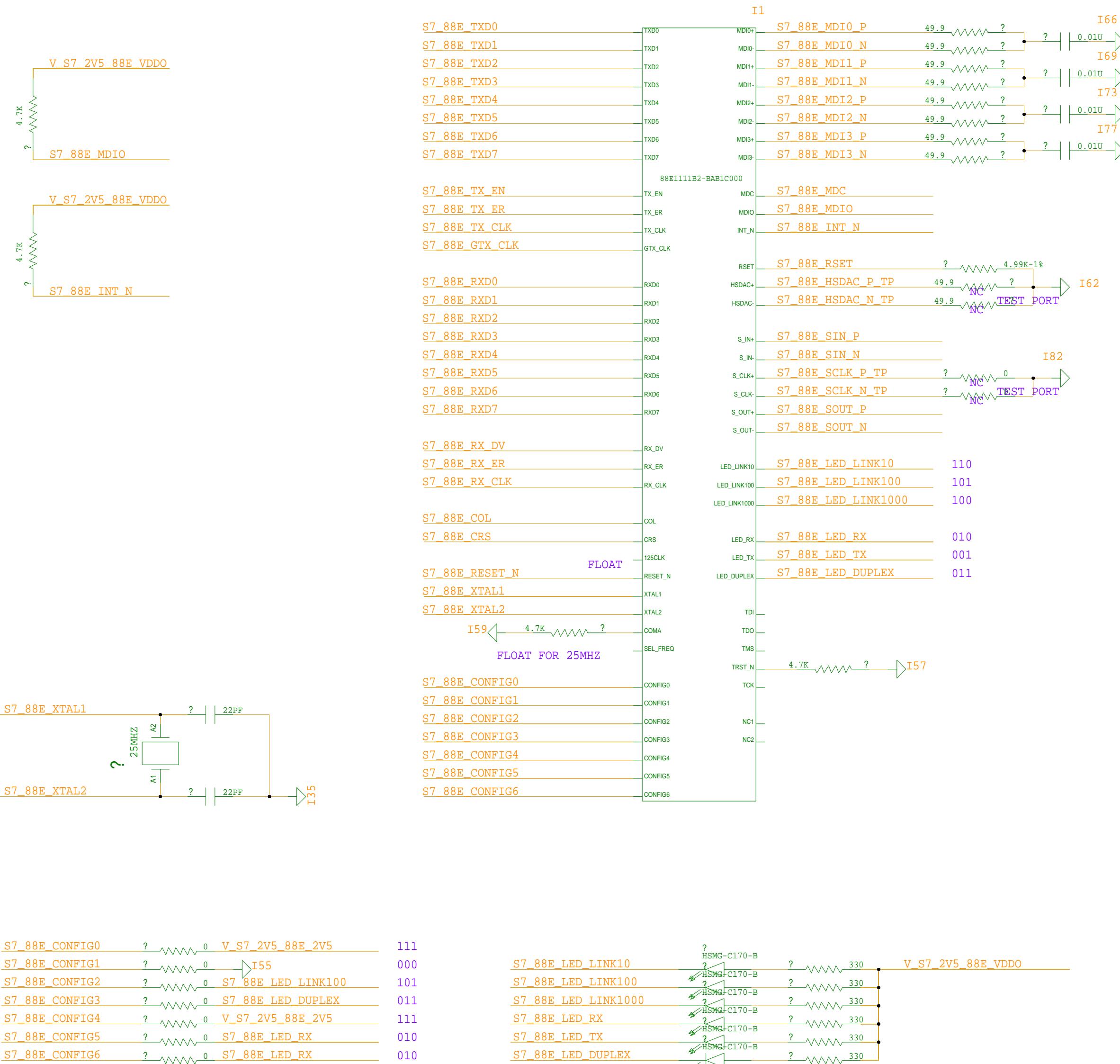
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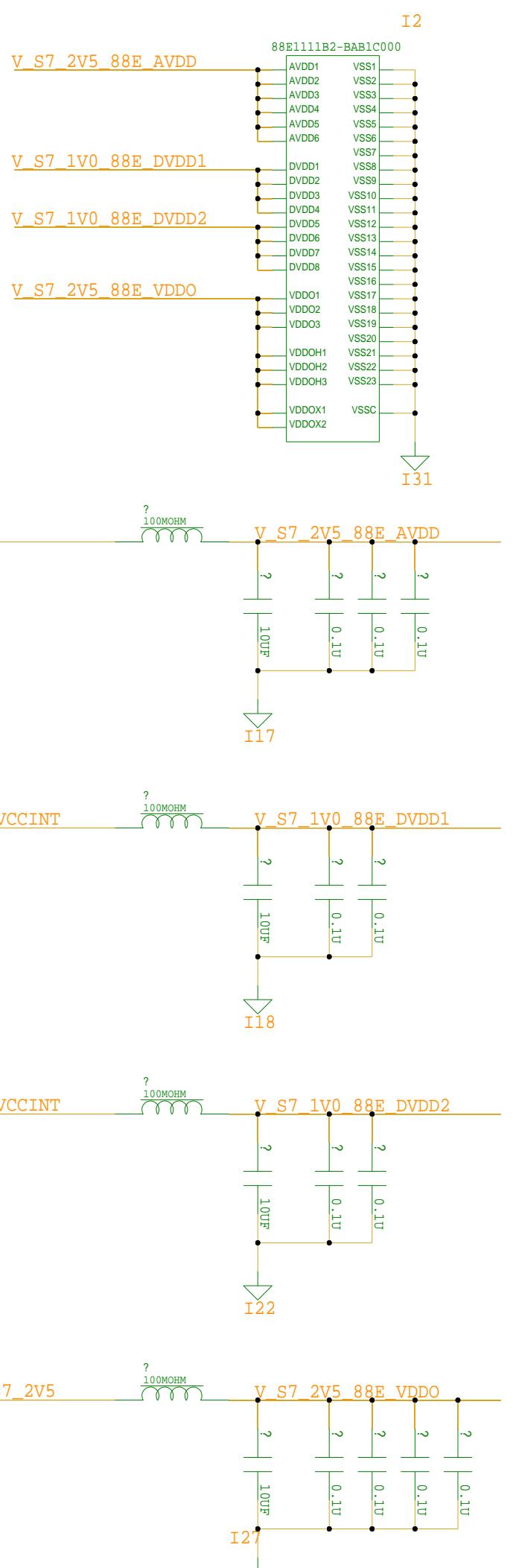
SPARTAN-7 SFP PHY (1)

REVISIONS

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PIN	CONNECTION	BACKUP	REG	VALUE	BACKUP	CONFIGURATION
CONFIG0	VDD	GND	PHYADR[2:0]	111	000	PHYADR=111
CONFIG1	GND	LED_LINK1000	ENA_PAUSE/PHYADR[4:3]	000	100	Disable PAUSE frame, PHYADR=00
CONFIG2	VDD		ANEG[3:1]	101	111	Fiber, force 1000BASE-X full-duplex
CONFIG3	LED_DUPLEX		ANEG[0]/ENA_XC/DIS_125	011		Crossover Enable, Disable 125MHz
CONFIG4	VDD	LED_DUPLEX	HWCFG_MODE[2:0]	111	011	GMII to Fiber 0111
CONFIG5	LED_RX	LED_LINK10	DIS_FC/DIS_SLEEP/HWCFG_MODE[3]	010	110	Enable FC/Copper, Disable Sleep
CONFIG6	LED_RX	LED_LINK10	SEL_TWSI/INT_POL/75_500HM	010	110	MDI/MDC, INT low, 50 ohm serdes



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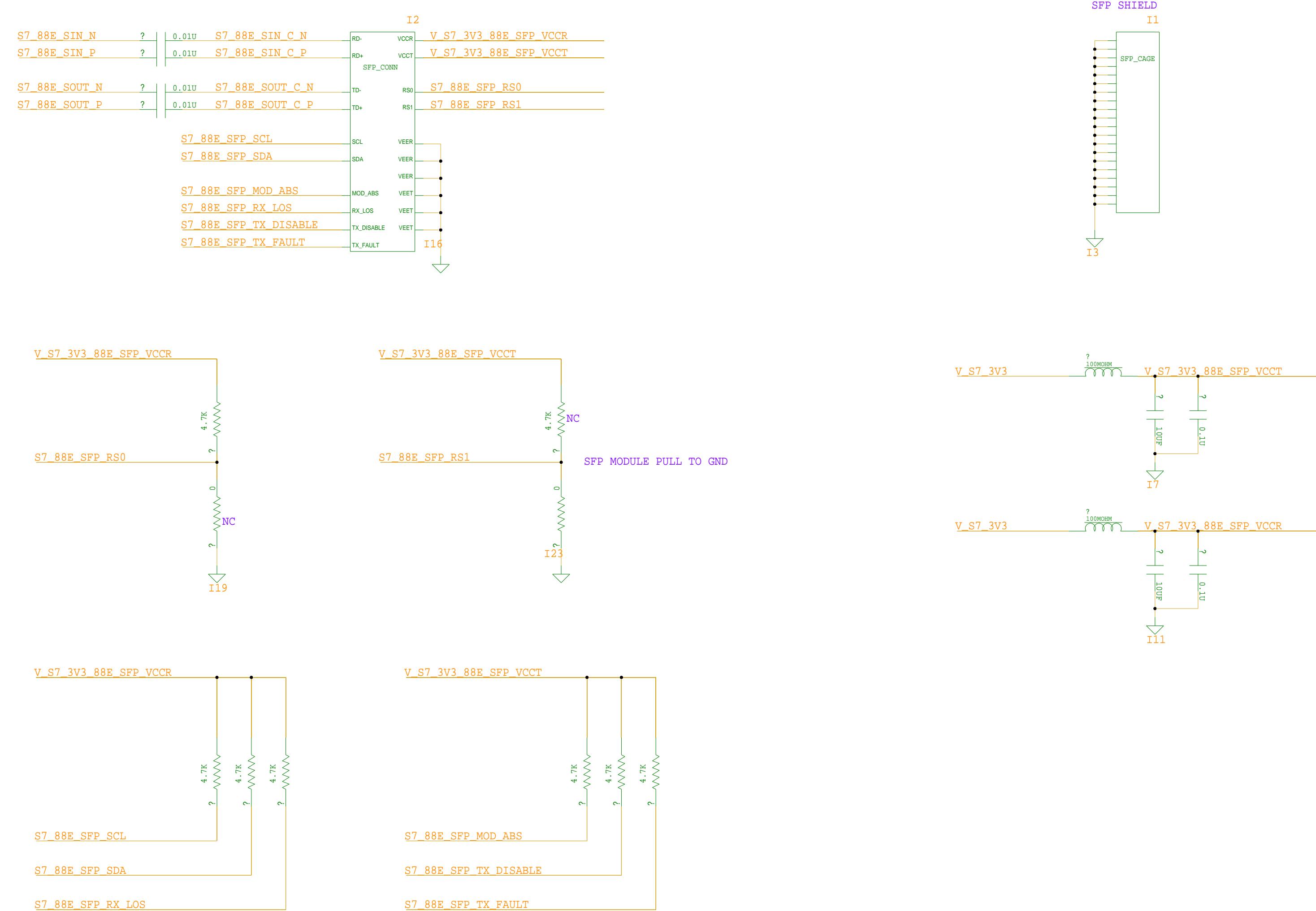
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SPARTAN-7 SFP PHY (2)

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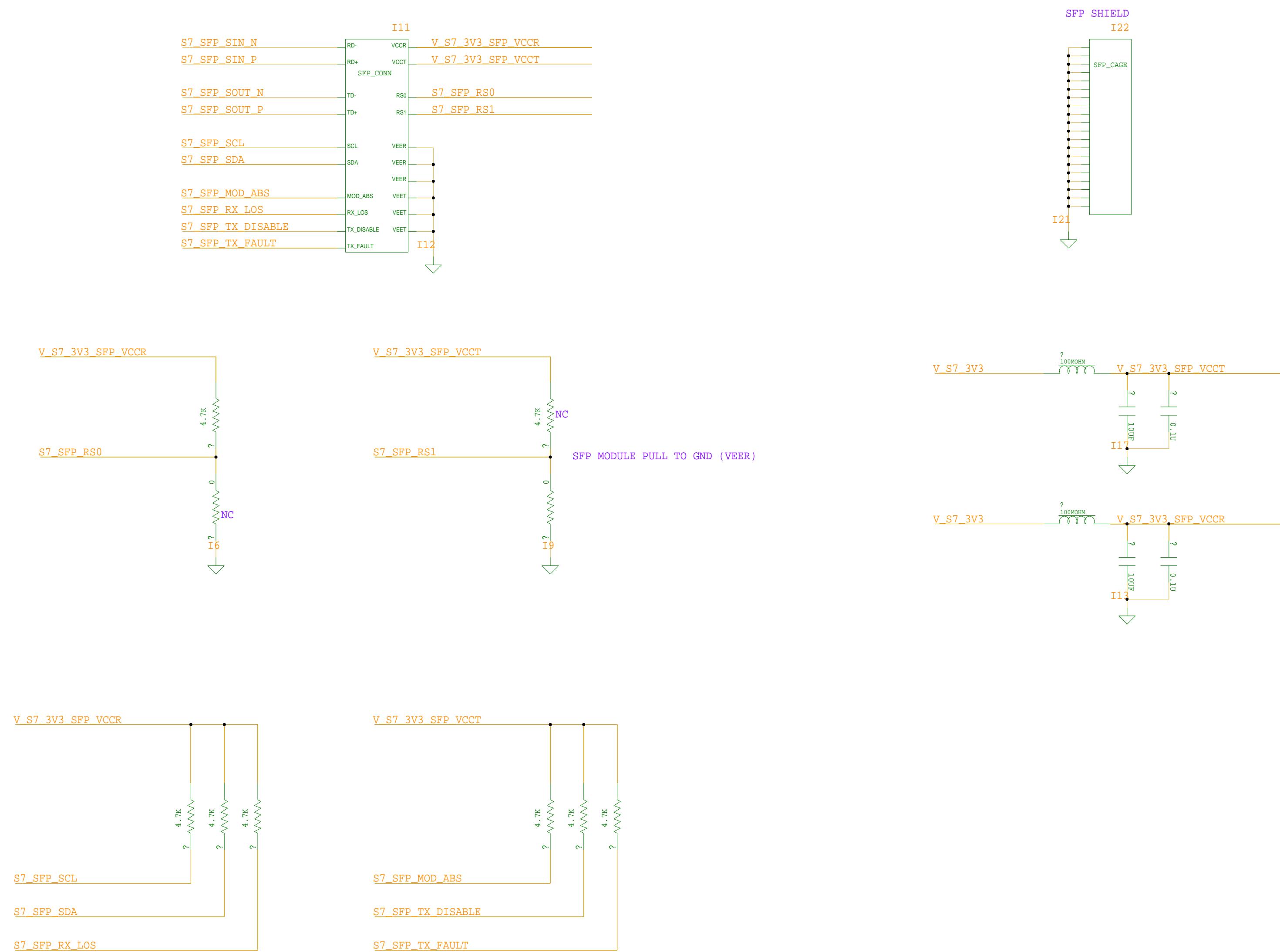
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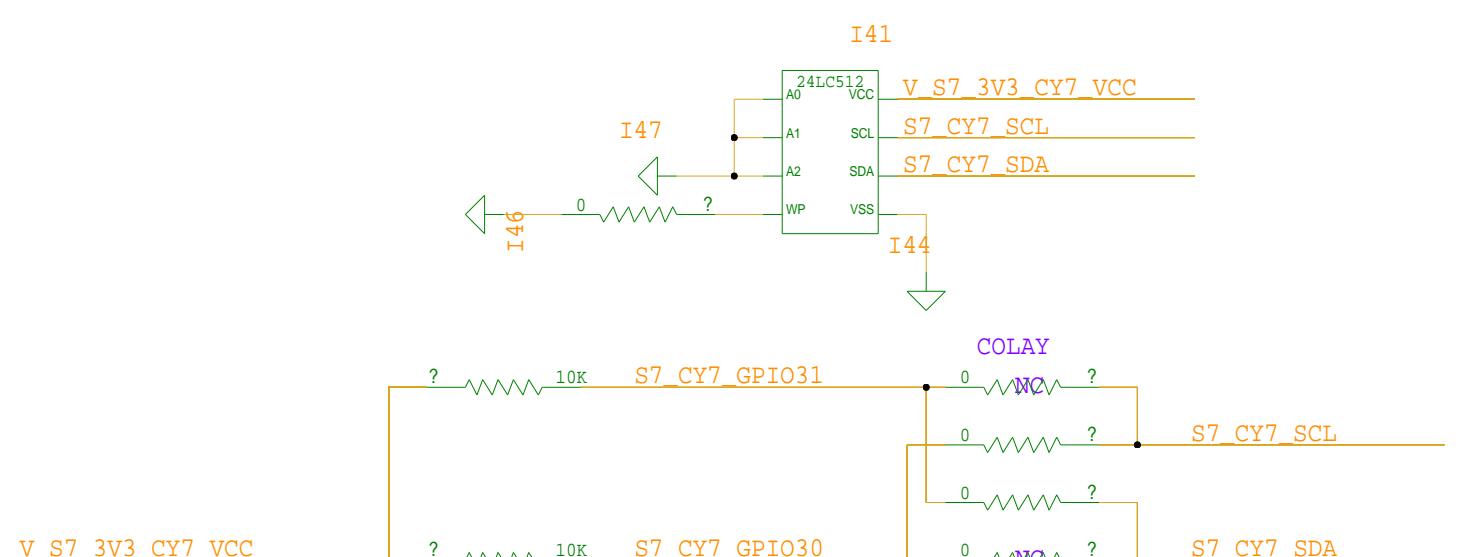
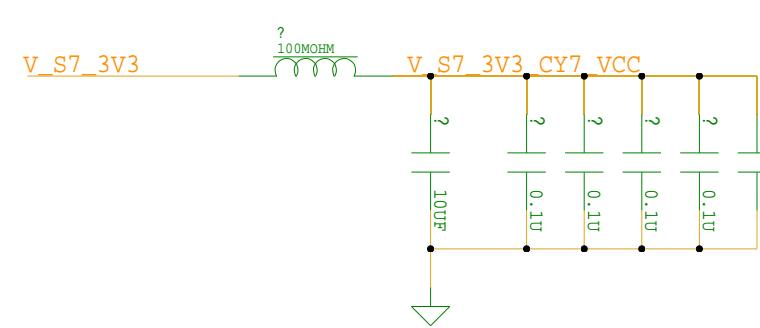
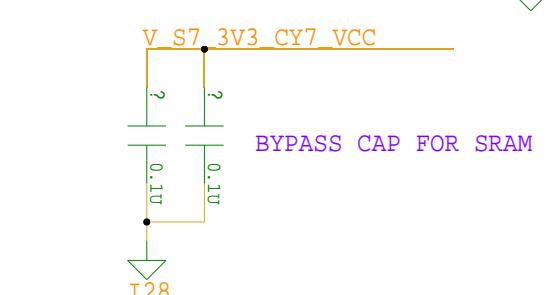
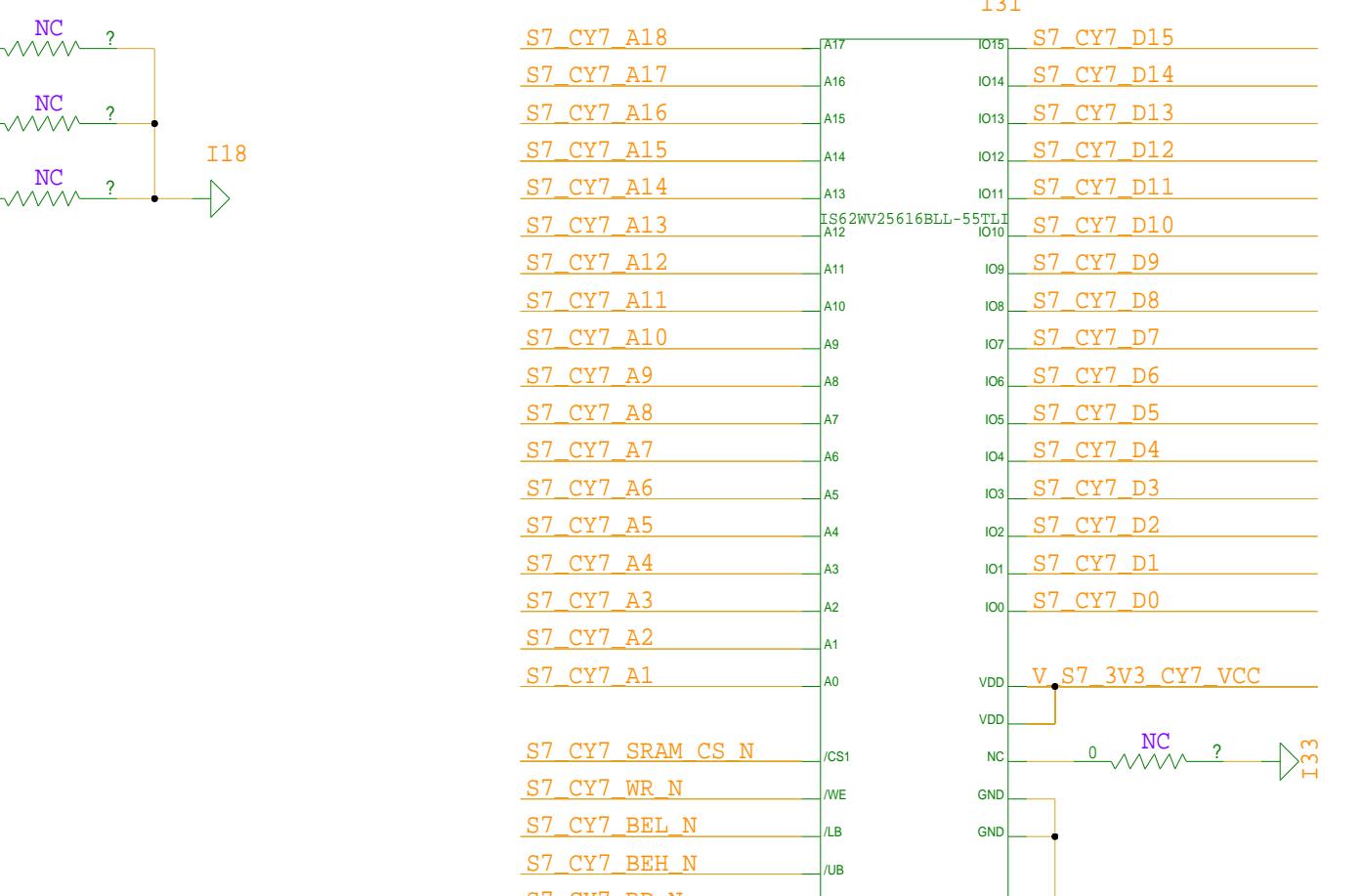
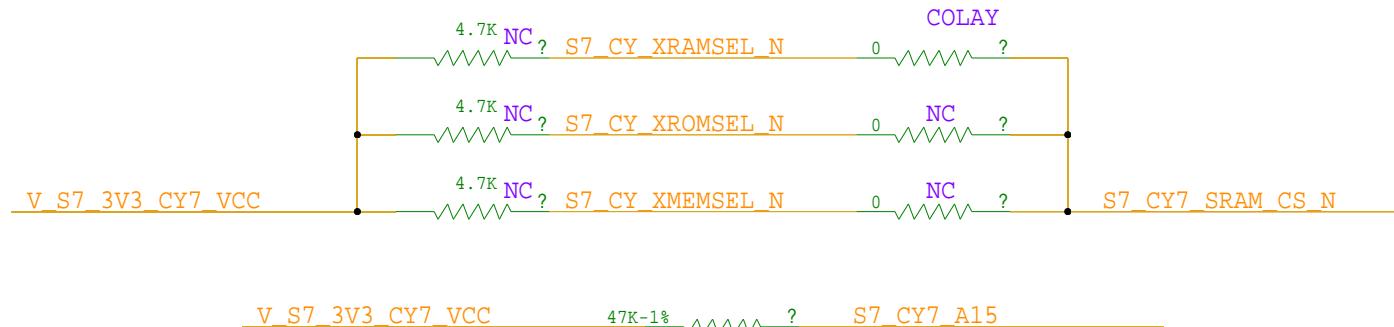
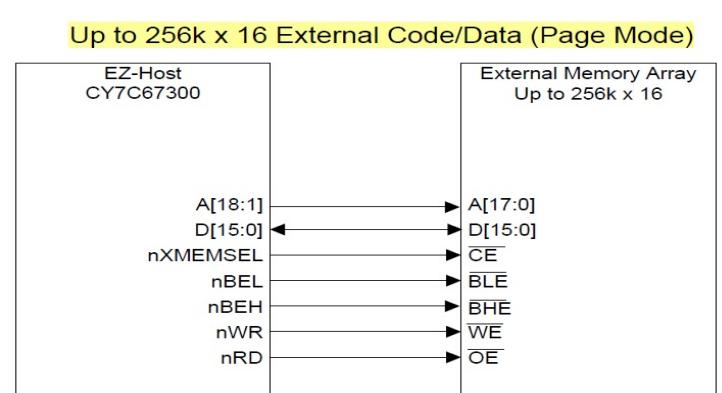
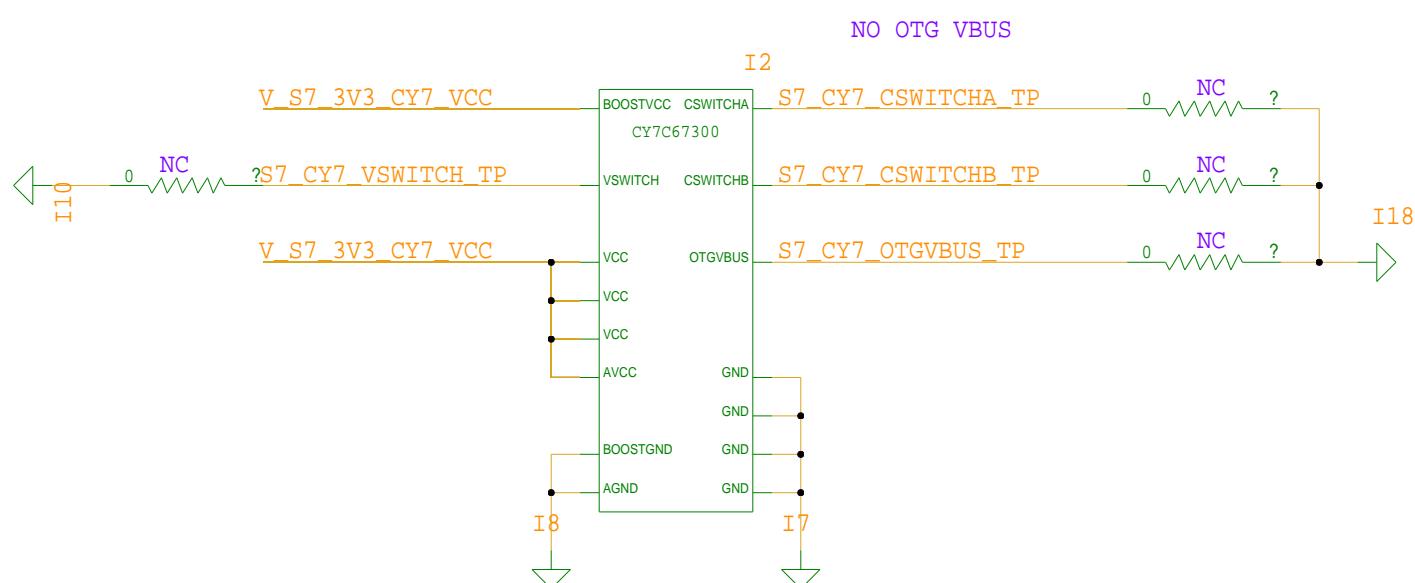
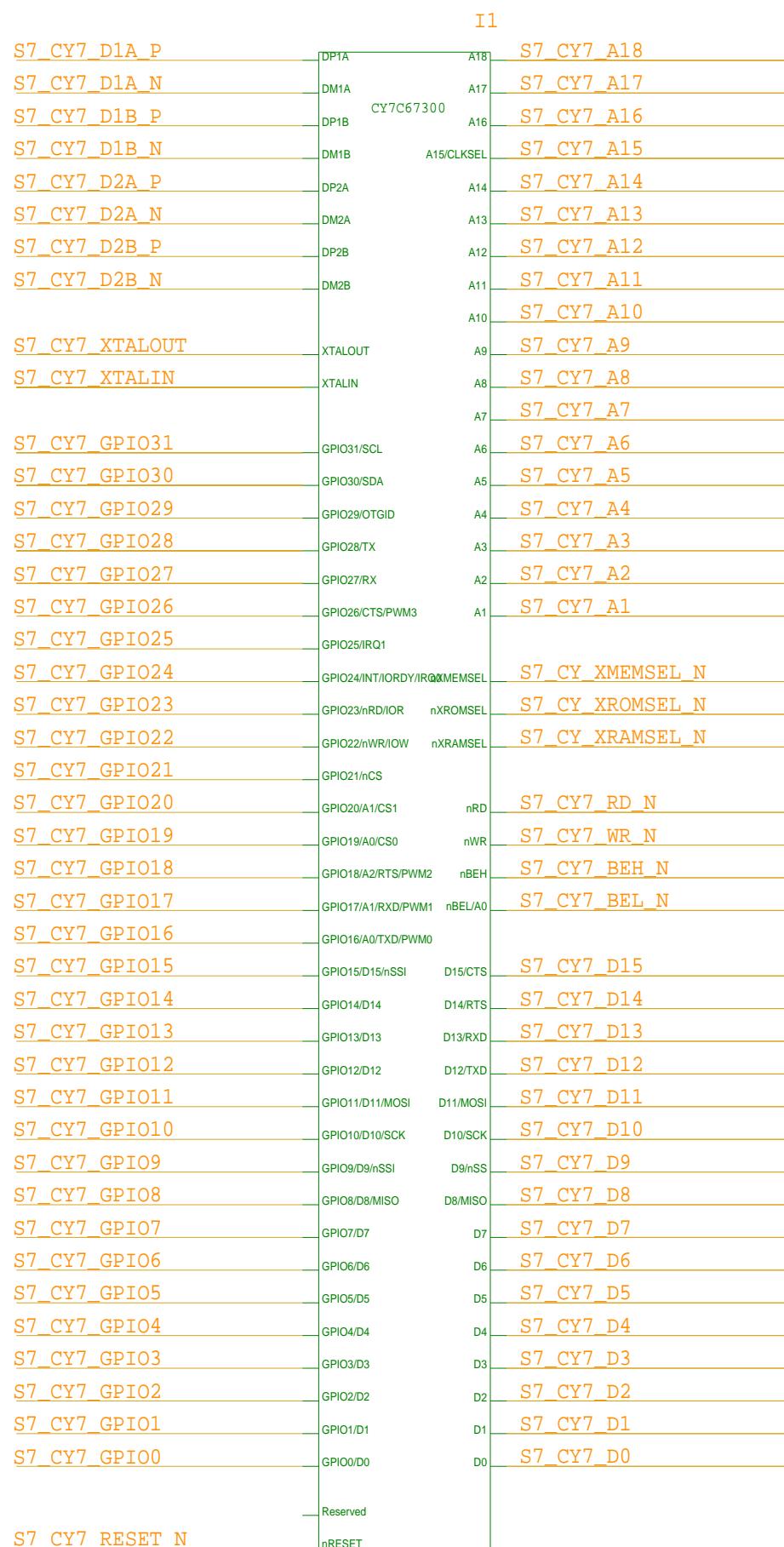


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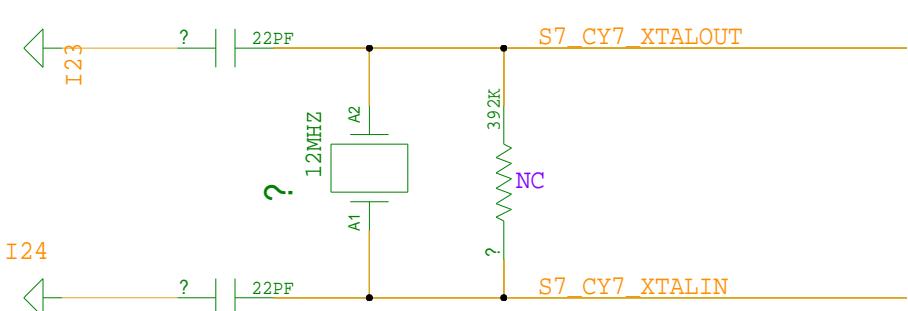
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SPARTAN-7 USB CONTROLLER (1)

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- Standalone Mode
In standalone mode, there is no external processor connected to EZ-Host. Instead, EZ-Host's own internal 16-bit CPU is the main processor and firmware is typically downloaded from an EEPROM. Optionally, firmware may also be downloaded via USB. See [Table 19](#) for booting into standalone mode.
- After booting into standalone mode ($\text{GPIO}[31:30] = '11'$), the following pins are affected:
 - $\text{GPIO}[31:30]$ are configured as output pins to examine the EEPROM contents
 - $\text{GPIO}[28:27]$ are enabled for debug UART mode
 - $\text{GPIO}[29]$ is configured for as OTGID for OTG applications on PORT1A
 - If OTGID is logic 1 then PORT1A (OTG) is configured as a USB peripheral
 - If OTGID is logic 0 then PORT1A (OTG) is configured as a USB host
 - Ports 1B, 2A, and 2B default as USB peripheral ports
 - All other pins remain INPUT pins.



20~33PF CLOAD IN SPEC, HERE 10 PF. CHANGE CRY OR CAP IN DEBUG.

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SPARTAN-7 USB INOUT

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USB IP CORE DOSEN'T SUPPORT SPARTAN-7

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SPARTAN-7 DDR3

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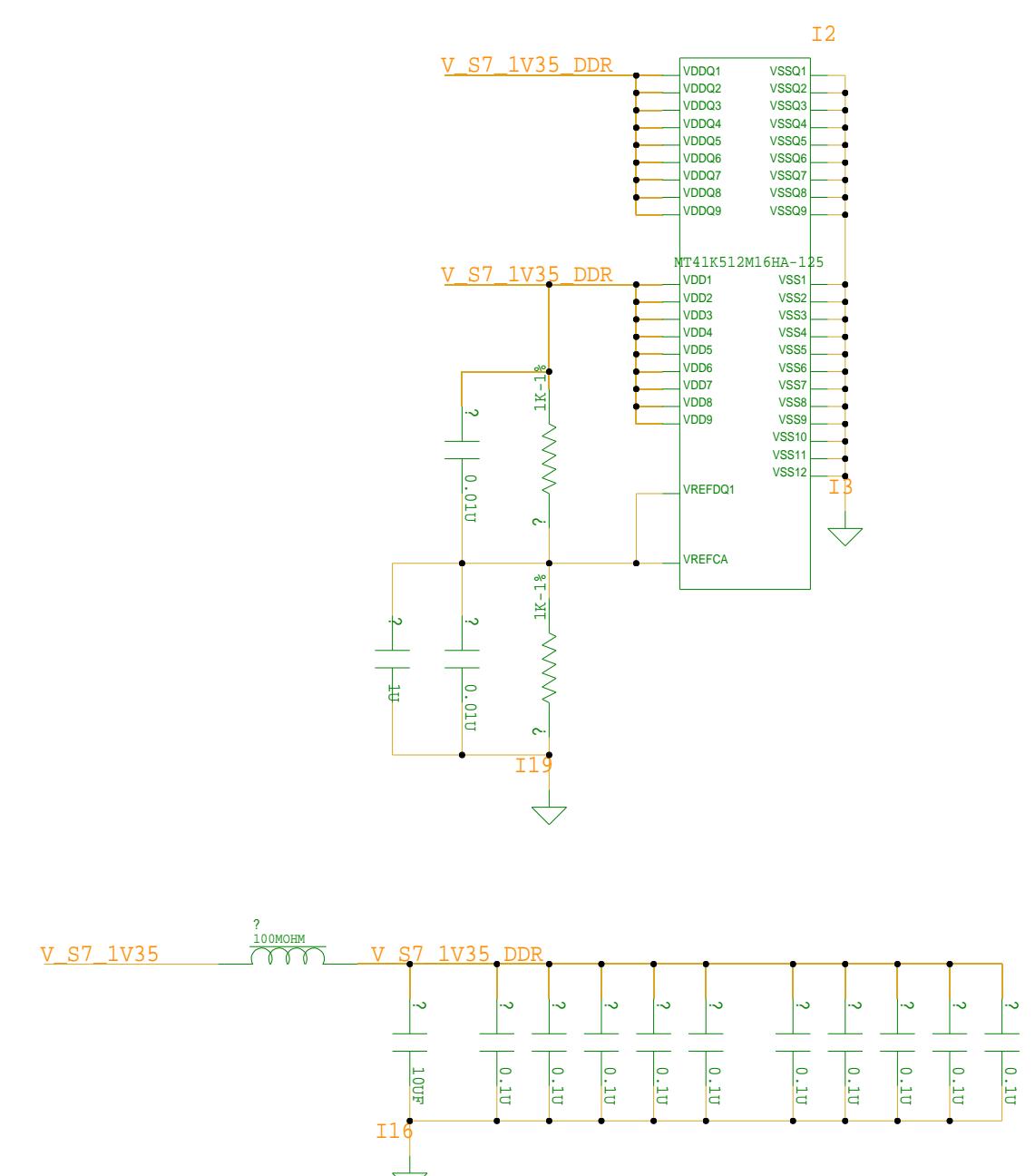
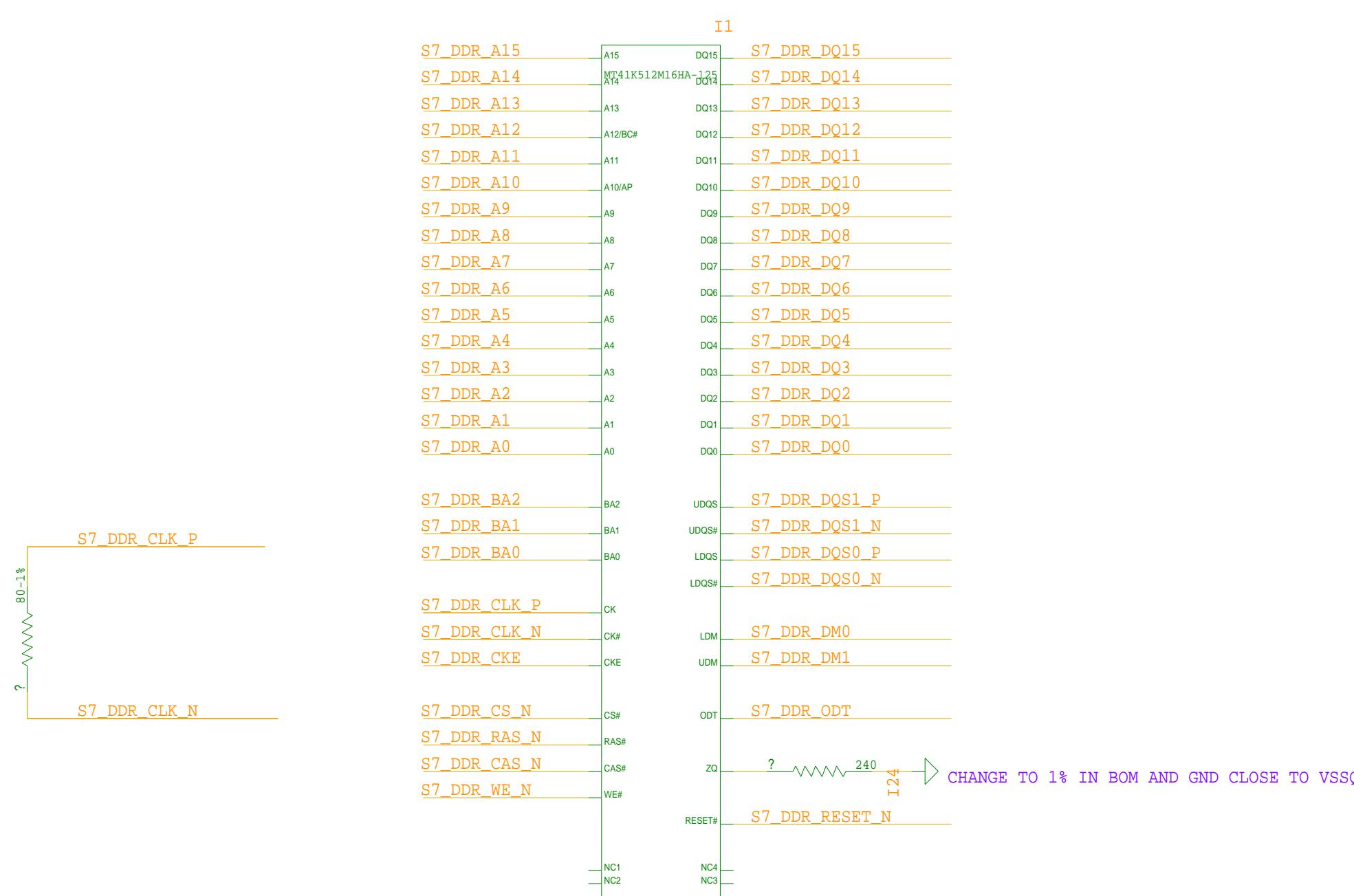
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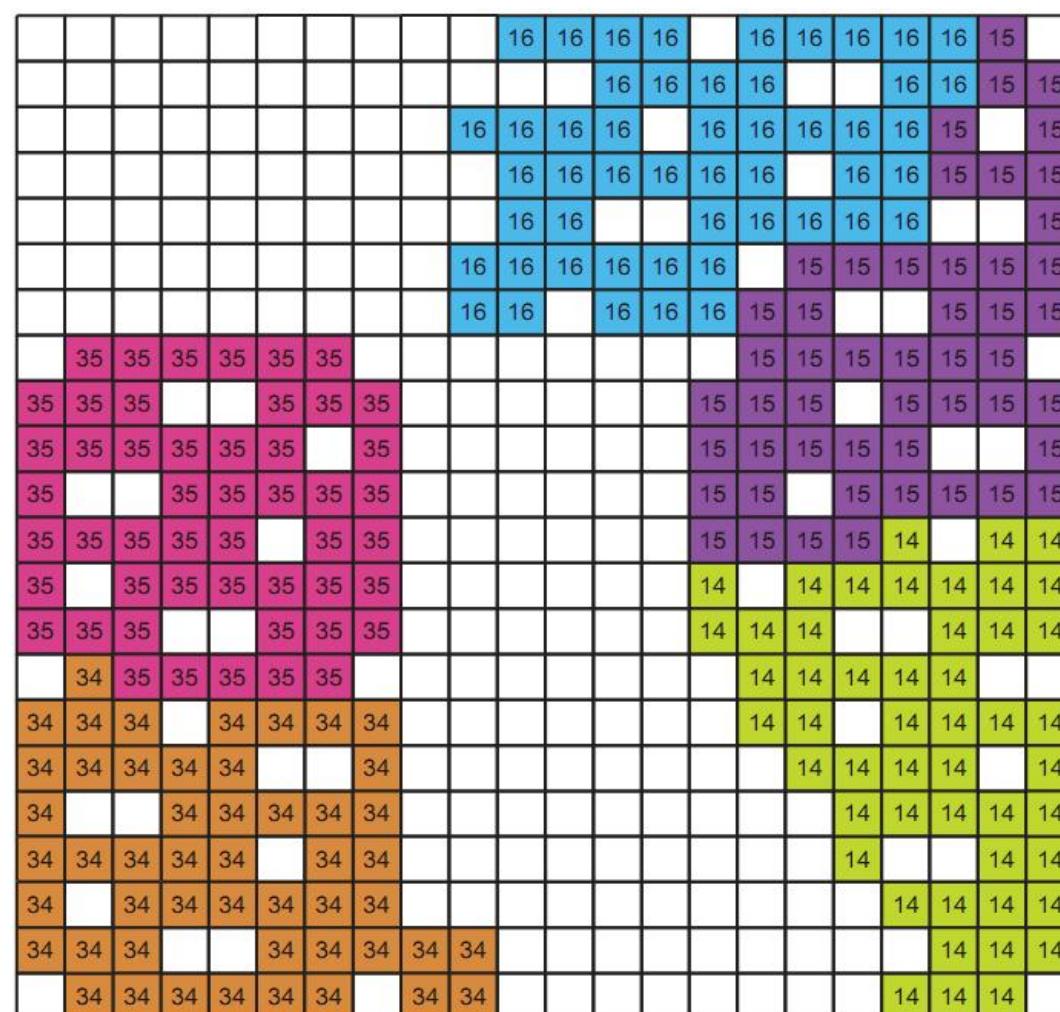
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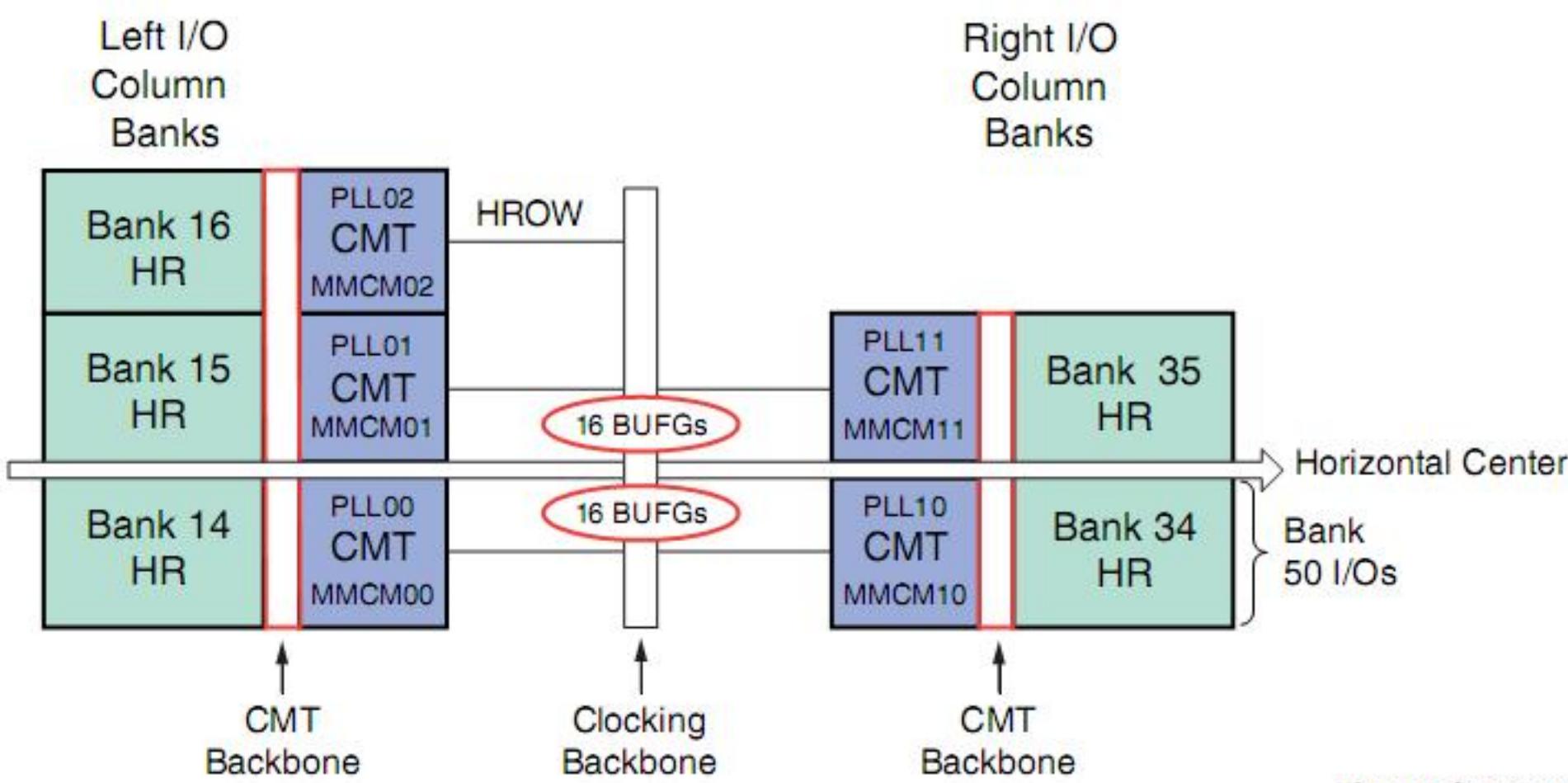
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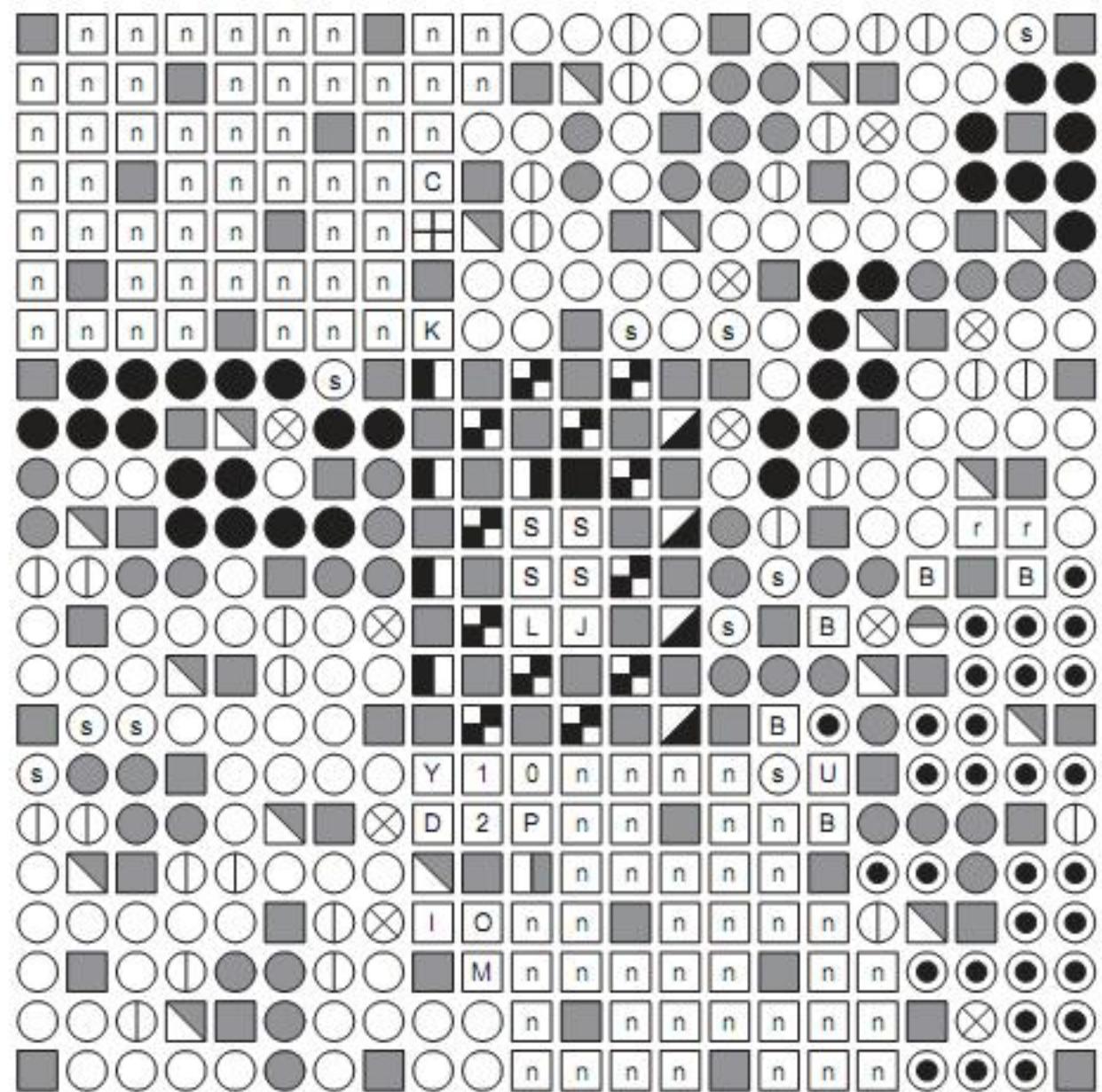
SPARTAN-7 PINOUT MAP



BANK0 : 3.3V CONFIG
 BANK14 : 3.3V HDMI RECEIVER/ HDMI INOUT/ USB PHY
 BANK15 : 3.3V HDMI TRANSMITTER/ RECEIVER
 BANK16 : 3.3V SFP INOUT/ HDMI TRANSMITTER
 BANK34 : 1.35V DDR3
 BANK35 : 2.5V GE PHY/ SFP INOUT



UG475_c1_S3_042717



User I/O Pins	Dedicated Pins	Other Pins
○ IO_LXXY_#	C CCLK_0	GND
○ IO_XX_#	S CFGBVS_0	VCCAUX_IO_G#
	D DONE_0	VCCAUX
	J DXP_0	VCCINT
	L DXN_0	VCCO_#
	Y GNDADC_0	VCCBRAM
	INIT_B_0	NC
	O M0_0	
	1 M1_0	
	2 M2_0	
	P PROGRAM_B_0	
	K TCK_0	
	I TDI_0	
	O TDO_0	
	M TMS_0	
	VCCADC_0	
	U RDWR_B	
	RS0-RS1	
	AD0P/AD0N-AD15P/AD15N	
	EMCCLK	

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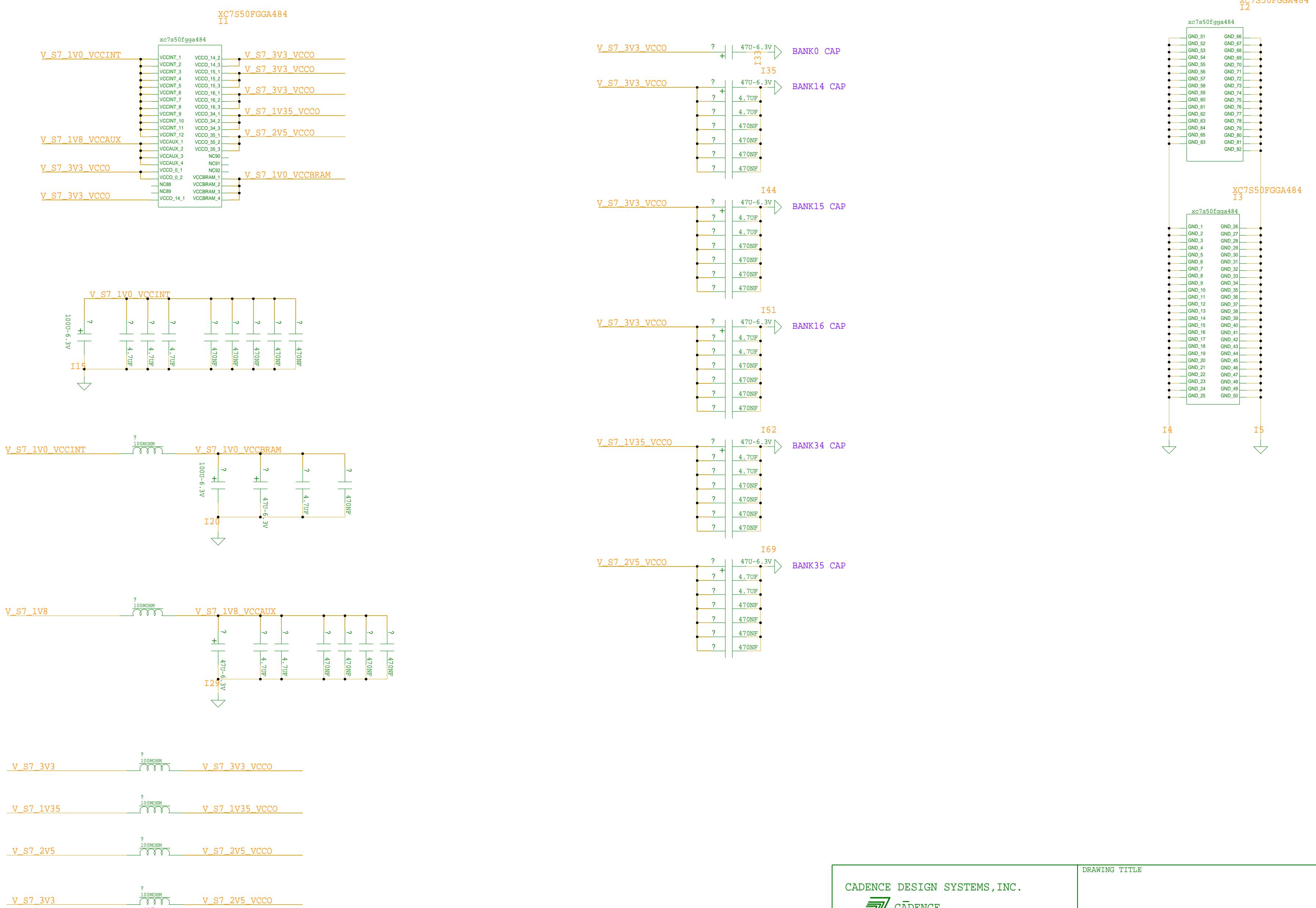
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SPARTAN-7 BANK POWER

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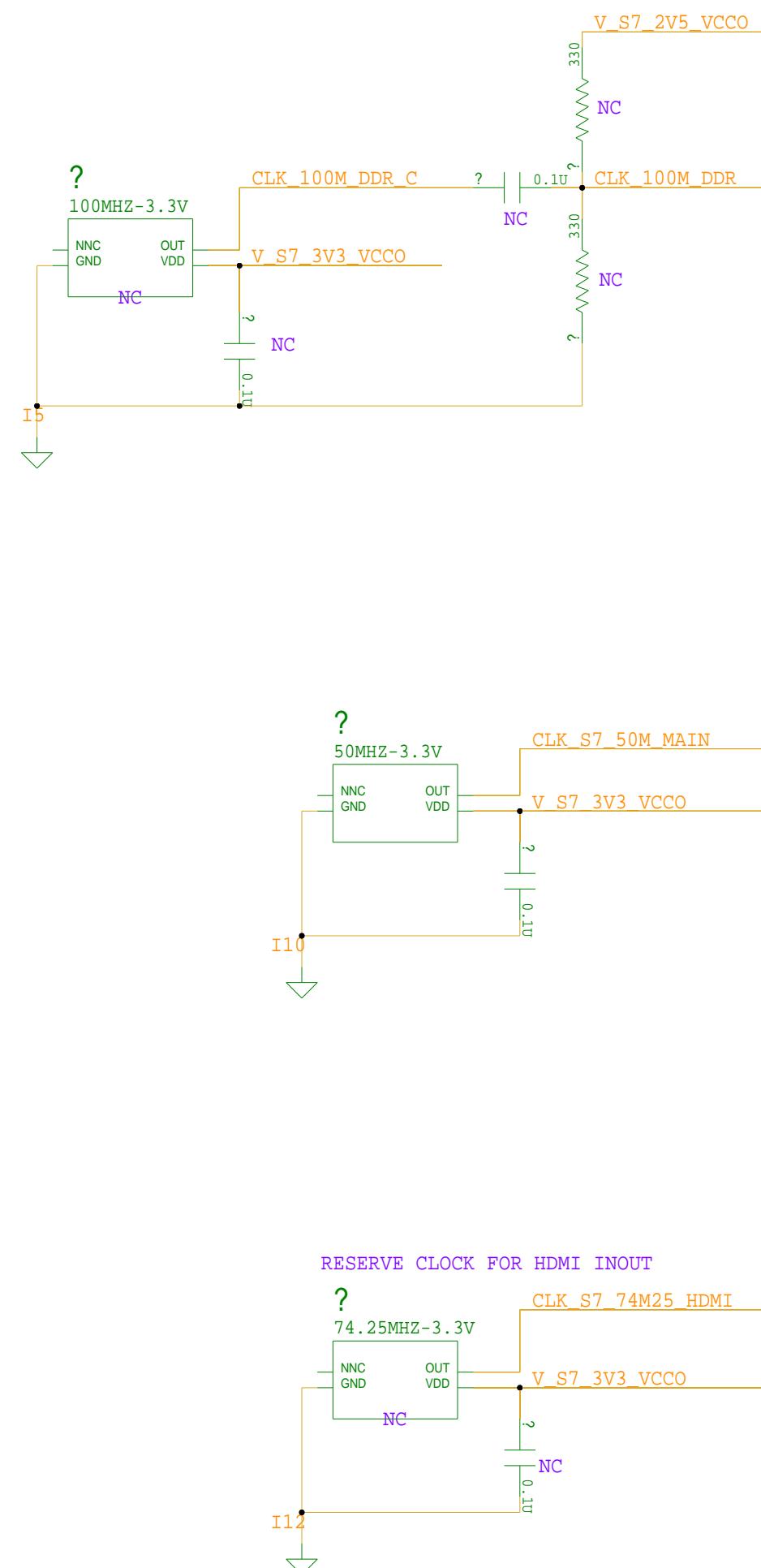
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SPARTAN-7 CLOCK



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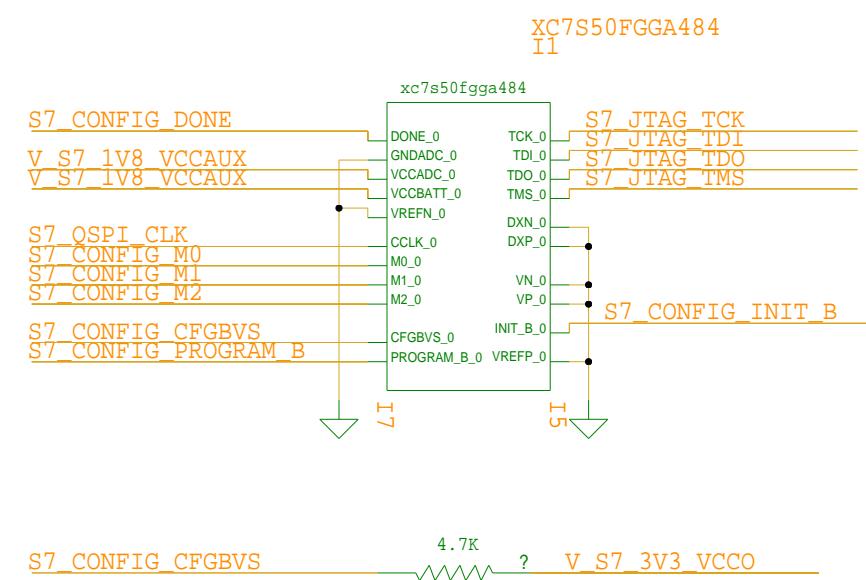
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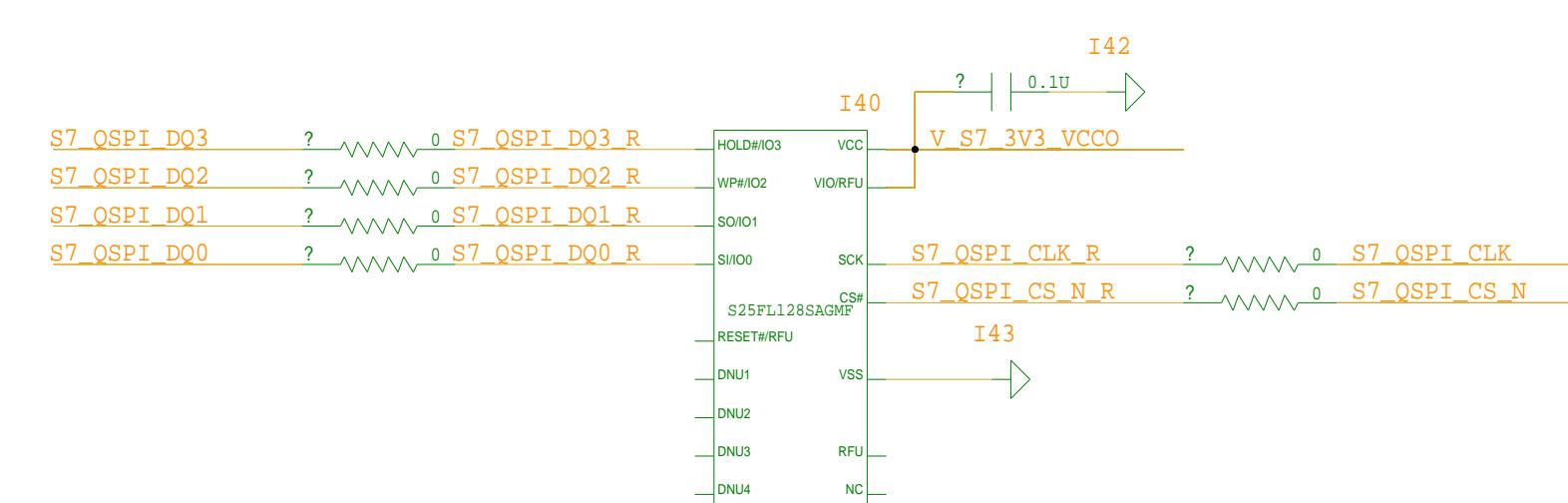
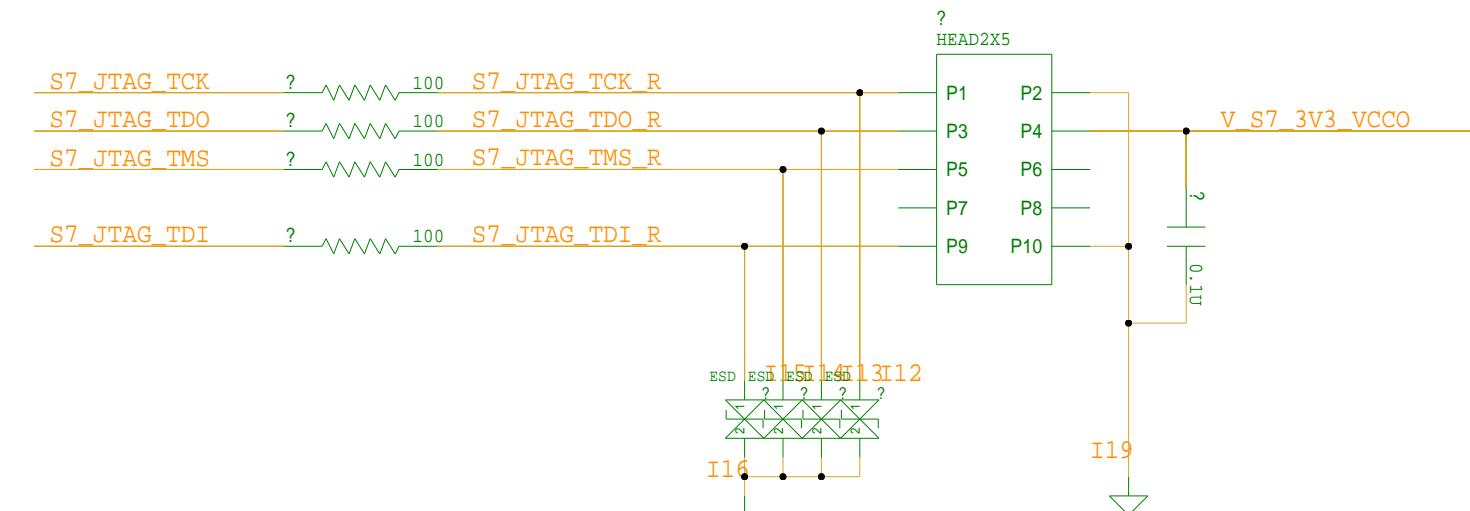
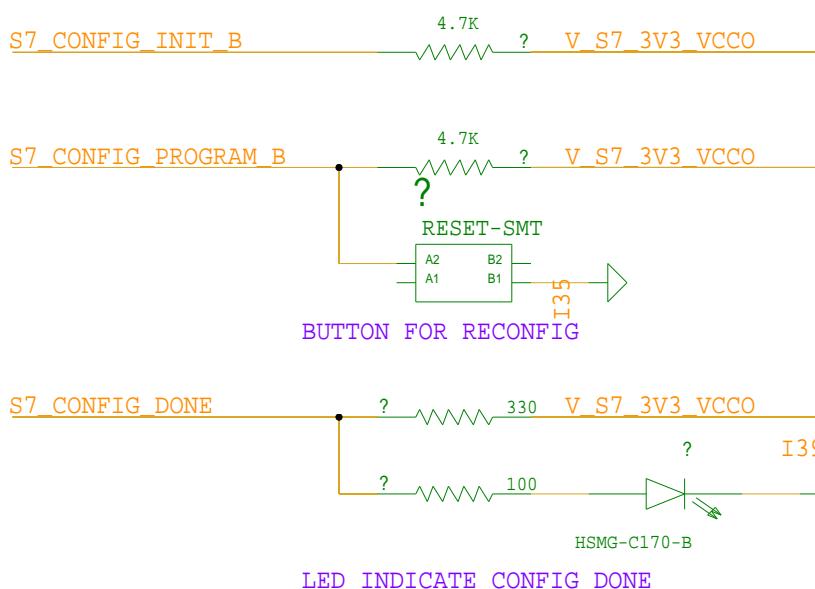
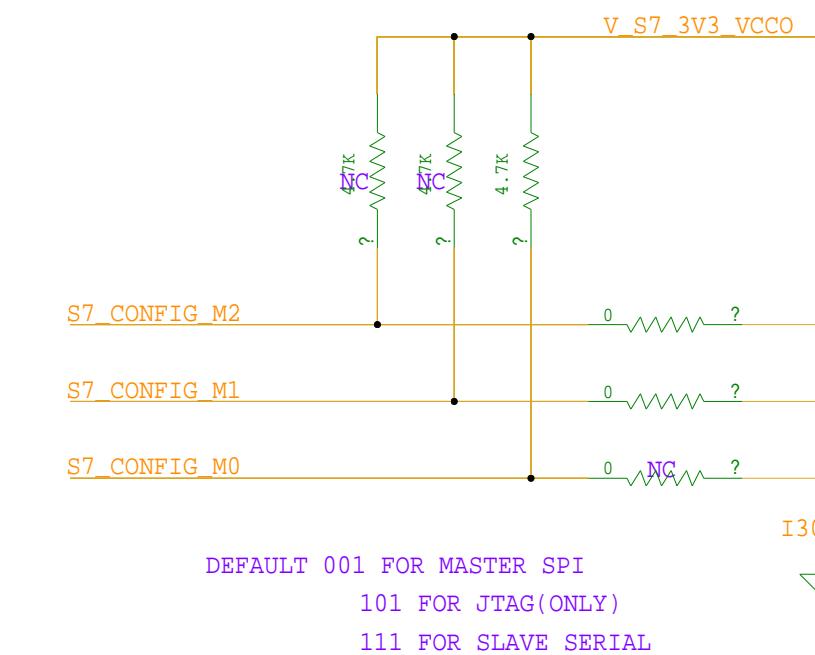
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SPARTAN-7 BANK0/14 CONFIG



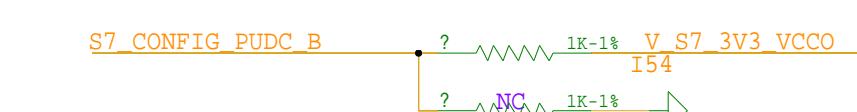
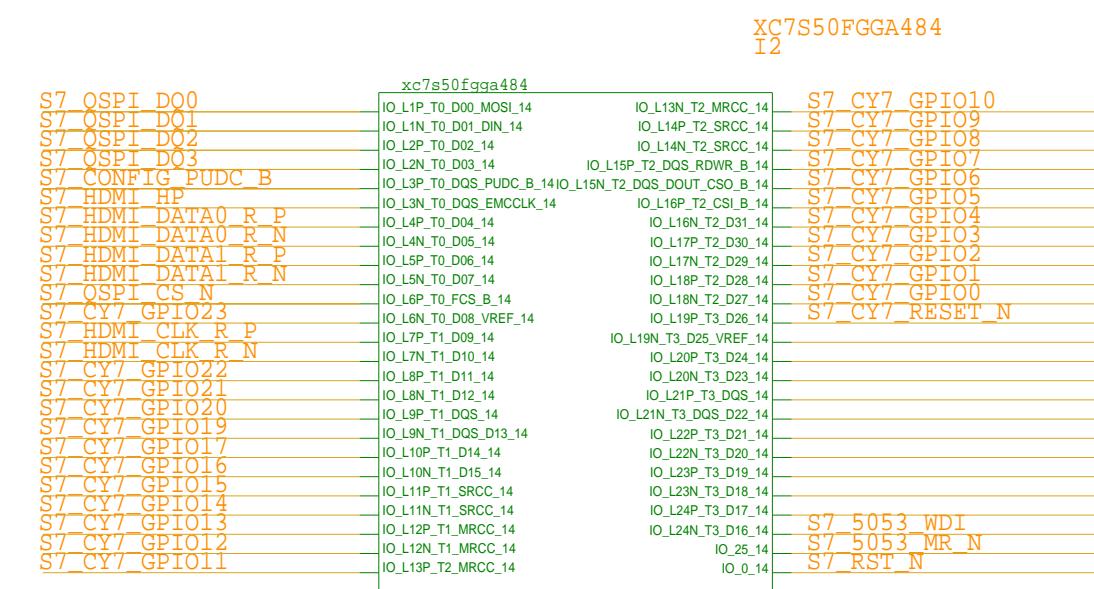
BANK0/14/15 SHOULD BE 3.3V/2.5V

CFGBVS Pin Connection	Supported Configuration Banks 0/14/15 V _{CCO} Supply and I/O Signal Voltages		
	Spartan-7, Artix-7, Kintex-7	Virtex-7 T, XT	Virtex-7 HT
Banks Affected	0, 14, 15	0	none
V _{CCO_0} (3.3V or 2.5V)	3.3V or 2.5V	3.3V or 2.5V	1.8V (no CFGBVS)
GND	1.8V or 1.5V	1.8V or 1.5V	



DO NOT CHANGE WIRES AS BELOW:

S7_QSPI_DQ0
S7_QSPI_DQ1
S7_QSPI_DQ2
S7_QSPI_DQ3
S7_CONFIG_PUDC_B
S7_QSPI_CS_N



PUDC HIGH FOR DISABLE PULLUP RES DURING CONFIGURATION

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SPARTAN-7 BANK15

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPR.

xc7s50fgga484		XC7S50FGGA484 I1
S7_7612_CS_N	IO_L1P_T0_AD0P_15	S7_7612_P14
S7_7612_RESET_N	IO_L1N_T0_AD0N_15	S7_7612_LLC
S7_7612_DE	IO_L2P_T0_AD0P_15	S7_7612_P15
S7_7612_SCL	IO_L2N_T0_AD0N_15	S7_7612_P16
S7_7612_SDA	IO_L3P_T0_DQS_AD1P_15	S7_7612_P17
S7_7612_INT1	IO_L3N_T0_DQS_AD1N_15	S7_7612_P18
S7_7612_INT2	IO_L4P_T0_15	S7_7612_P19
S7_7612_HS	IO_L4N_T0_15	S7_7612_P20
S7_7612_VS	IO_L5P_T0_AD0P_15	S7_7612_P21
S7_7612_P0	IO_L5N_T0_AD0N_15	S7_7612_P22
S7_7612_P1	IO_L6P_T0_15	S7_7612_P23
S7_7612_P2	IO_L6N_T0_VREF_15	S7_7612_P24
S7_7612_P3	IO_L7P_T1_AD2P_15	S7_7612_P25
S7_7612_P4	IO_L7N_T1_AD2N_15	S7_7612_P26
S7_7612_P5	IO_L8P_T1_AD10P_15	S7_7612_P27
S7_7612_P6	IO_L8N_T1_AD10N_15	S7_7612_P28
S7_7612_P7	IO_L9P_T1_DQS_AD3P_15	S7_7612_P29
S7_7612_P8	IO_L9N_T1_DQS_AD3N_15	S7_7612_P30
S7_7612_P9	IO_L10P_T1_AD11P_15	S7_7612_P31
S7_7612_P10	IO_L10N_T1_AD11N_15	S7_7612_P32
S7_7612_P11	IO_L11P_T1_SRCC_15	S7_7612_P33
S7_7612_P12	IO_L11N_T1_SRCC_15	S7_7612_P34
CLK_S7_50M_MAIN	IO_L12P_T1_MRCC_15	IO_L24P_T3_RS1_15
S7_7612_P13	IO_L12N_T1_MRCC_15	IO_L24N_T3_RS0_15
CLK_S7_74M25_HDMI	IO_L13P_T2_MRCC_15	IO_25_15
		S7_HDMI_SCL_Q
		S7_HDMI_SDA_Q

DO NOT CHANGE WIRES AS BELOW:

CLK_50M_MAIN
CLK 74M25 HDMI

OD CONFIG AS BELOW:

S7_7612_SCL
S7_7612_SDA
S7_HDMI_SCL_Q
S7_HDMI_SDA_Q



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SPARTAN-7 BANK16

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S7_SFP_SIN_P	IO_L1P_T0_16	IO_L19N_T2_MRCC_16	S7_7511_D8
S7_SFP_SIN_N	IO_L1N_T0_16	IO_L14P_T2_SRCC_16	S7_7511_D9
S7_SFP_SOUT_P	IO_L2P_T0_16	IO_L14N_T2_SRCC_16	S7_7511_D10
S7_SFP_SOUT_N	IO_L2N_T0_16	IO_L15P_T2_DOS_16	S7_7511_D11
S7_FPGA_7511_SCL	IO_L3P_T0_DQS_16	IO_L15N_T2_DOS_16	S7_7511_D12
S7_FPGA_7511_SDA	IO_L3N_T0_DQS_16	IO_L16P_T2_16	S7_7511_D13
S7_7511_DE	IO_L4P_T0_16	IO_L16N_T2_16	S7_7511_D14
S7_7511_HSYNC	IO_L4N_T0_16	IO_L17P_T2_16	S7_7511_D15
S7_FPGA_7511_INT	IO_L5P_T0_16	IO_L17N_T2_16	S7_7511_D19
S7_7511_SDPFF_OUT	IO_L5N_T0_16	IO_L18P_T2_16	S7_7511_D20
S7_7511_VSYNC	IO_L6P_T0_16	IO_L18N_T2_16	S7_7511_D21
S7_7511_D0	IO_L7P_T0_VREF_16	IO_L19P_T3_16	S7_7511_D22
S7_7511_D1	IO_L7N_T0_VREF_16	IO_L19N_T3_16	S7_7511_D23
S7_7511_D2	IO_L7N_T1_16	IO_L20P_T3_16	S7_7511_D24
S7_7511_D3	IO_L8P_T1_16	IO_L20N_T3_16	S7_7511_D25
S7_7511_D4	IO_L8N_T1_16	IO_L21P_T3_DQS_16	S7_7511_D26
S7_7511_D5	IO_L9P_T1_DQS_16	IO_L21N_T3_DQS_16	S7_7511_D27
S7_7511_D6	IO_L9N_T1_DQS_16	IO_L22P_T3_16	S7_7511_D28
S7_7511_D7	IO_L10P_T1_16	IO_L22N_T3_16	S7_7511_D29
S7_7511_CLK	IO_L10N_T1_16	IO_L23P_T3_16	S7_7511_D30
S7_7511_D16	IO_L11P_T1_SRCC_16	IO_L23N_T3_16	S7_7511_D31
S7_7511_D17	IO_L11N_T1_SRCC_16	IO_L24P_T3_16	S7_7511_D32
S7_7511_D18	IO_L12P_T1_MRCC_16	IO_L24N_T3_16	S7_7511_D33
S7_FPGA_7511_CEC_CLK	IO_L12N_T1_MRCC_16	IO_25_16	S7_7511_D34
		IO_0_16	S7_7511_D35

OD CONFIG AS BELOW:

S7_FPGA_7511_SCL
S7_FPGA_7511_SDA

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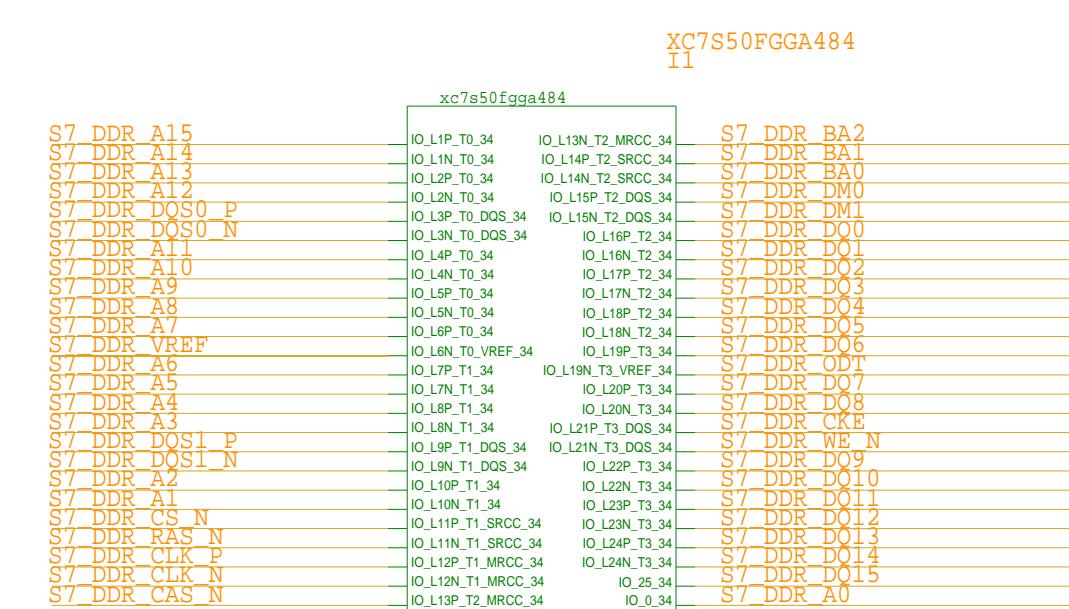

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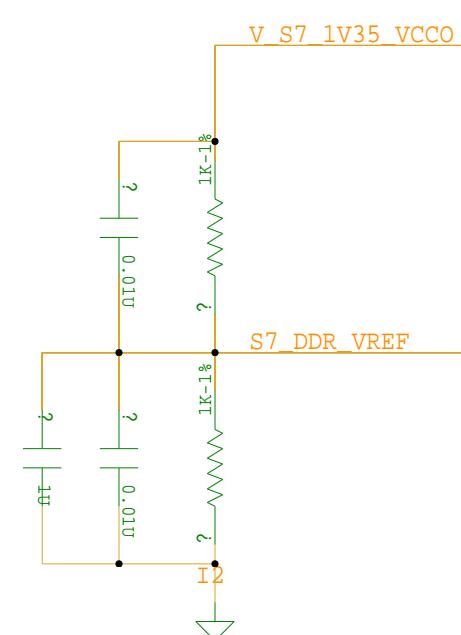
SPARTAN-7 BANK34

REVISED		DESCRIPTION		DATE	APPR.



DO NOT CHANGE WIRES AS BELOW:

S7_DDR_DQSO/1_P/N
S7_DDR_CLK_P/N
S7_DDR_VREF



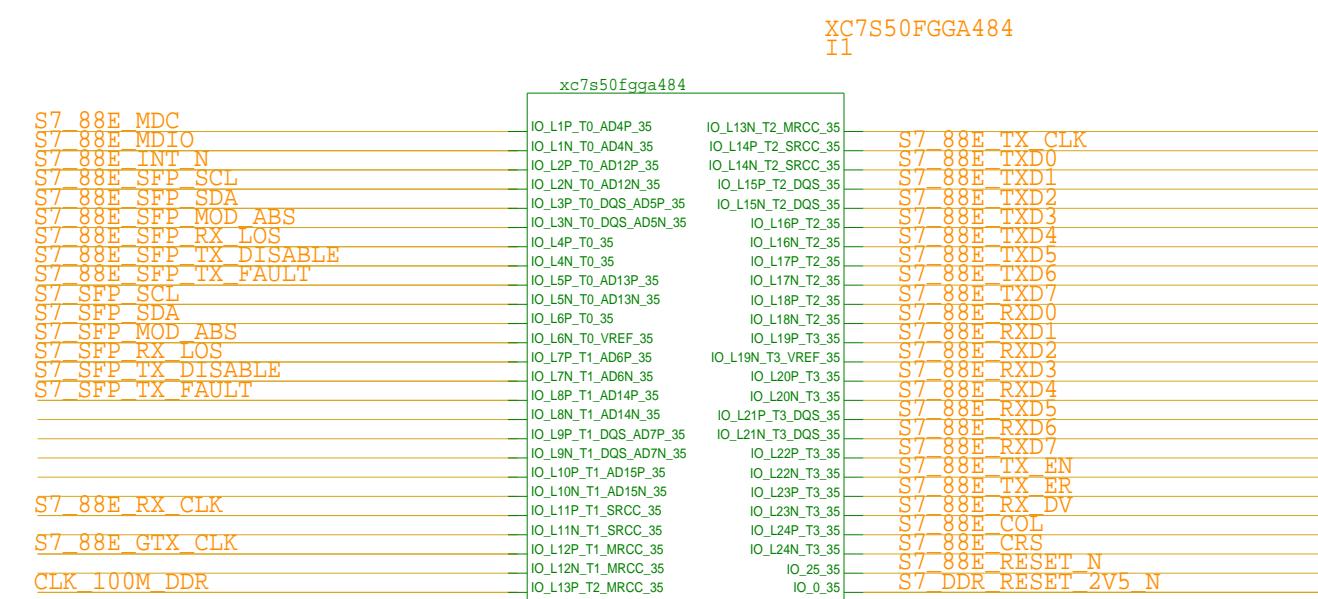
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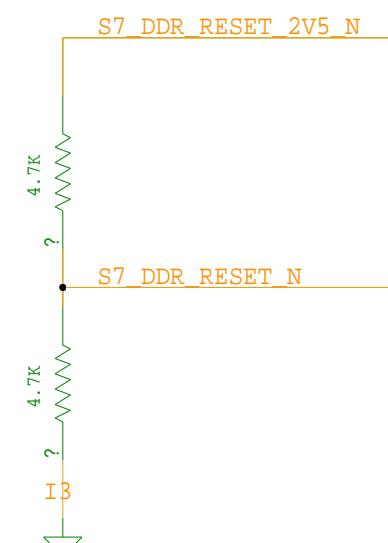
DO NOT CHANGE WIRES AS BELOW:

CLK_100M_DDR
S7_88E_CTX_CLK
S7_88E_RX_CLK

OD CONFIG AS BELOW:

S7_88E_SFP_SCL
S7_88E_SFP_SDA
S7_88E_SFP_MOD_ABS
S7_88E_SFP_RX_LOS
S7_88E_SFP_TX_DISABLE
S7_88E_SFP_TX_FAULT

S7_SFP_SCL
S7_SFP_SDA
S7_SFP_MOD_ABS
S7_SFP_RX_LOS
S7_SFP_TX_DISABLE
S7_SFP_TX_FAULT



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SPARTAN-7 BANK NC

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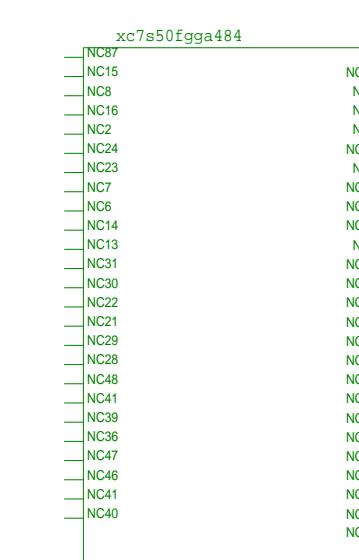
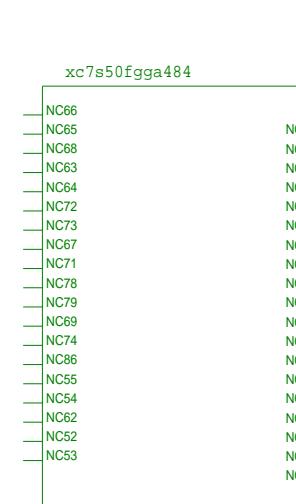
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ARTIX-7 INDEX

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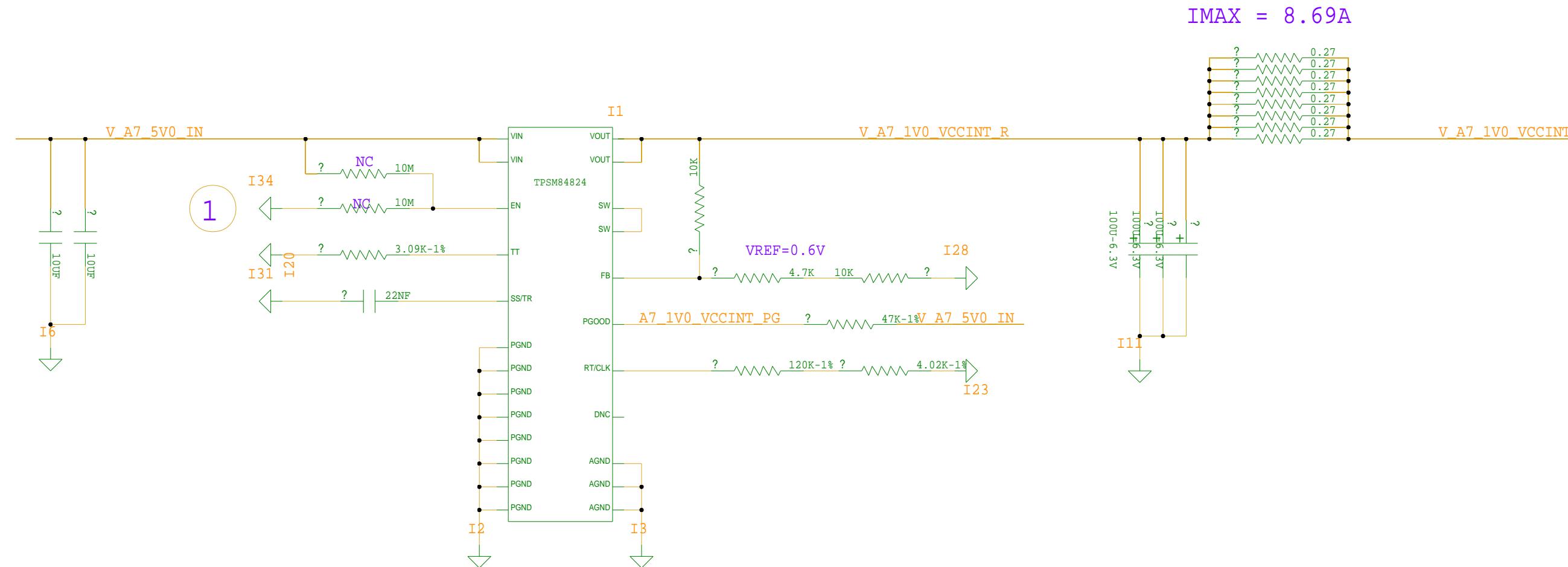
ARTIX-7 POWER (1)

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SS/TR	6	I	Soft-start and tracking pin. Connecting an external capacitor to this pin adjusts the output voltage soft-start ramp slower than its 1.2 ms default setting. A voltage applied to this pin allows for tracking and sequencing control.
-------	---	---	--

Table 9. Soft-Start Capacitor Values and Soft-Start Time

C _{ss} (nF)	open	10	15	22	47
SS Time (ms)	1.2	2.4	3	3.8	6.8

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ARTIX-7 POWER (2)

$$V_{OUT} = V_{REF} \times (1 + (R_{TOP}/R_{BOT}))$$

$$R_{RT} (\text{k}\Omega) = [14,822/f_{SW} (\text{kHz})]^{1.081}$$

$$V_{IN_STARTUP} = (0.8 \text{ nA} + (0.8 \text{ V}/R_{BOT_EN})) \times \left(R_{TOP_EN} + \frac{R_{BOT_EN} \times 1 \text{ M}\Omega}{R_{BOT_EN} + 1 \text{ M}\Omega} \right)$$

where:

R_{TOP_EN} is the resistor from V_{IN} to EN.

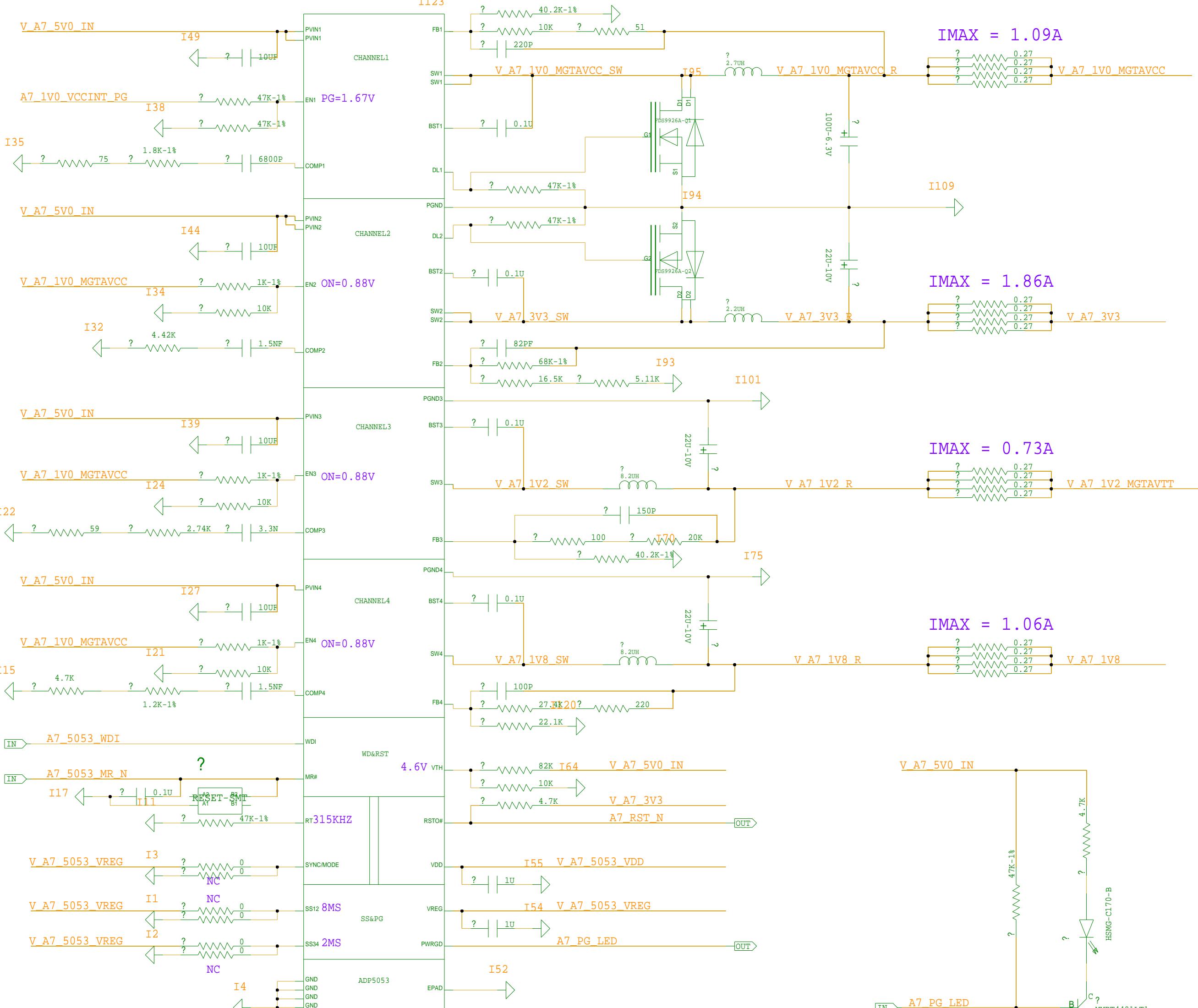
R_{BOT_EN} is the resistor from EN to ground.

Table 9. Soft Start Time Set by the SS12 and SS34 Pins

R_{TOP} (k Ω)	R_{BOT} (k Ω)	Soft Start Time			
		Channel 1	Channel 2	Channel 3	Channel 4
0	N/A ¹	2 ms	2 ms	2 ms	2 ms
100	600	2 ms	Parallel	2 ms	4 ms
200	500	2 ms	8 ms	2 ms	8 ms
300	400	4 ms	2 ms	4 ms	2 ms
400	300	4 ms	4 ms	4 ms	4 ms
500	200	8 ms	2 ms	4 ms	8 ms
600	100	8 ms	Parallel	8 ms	2 ms
N/A ¹	0	8 ms	8 ms	8 ms	8 ms

Table 16. Factory Default Options

Option	Default Value
Channel 1 Output Voltage	0.8V adjustable output
Channel 2 Output Voltage	0.8V adjustable output
Channel 3 Output Voltage	0.8V adjustable output
Channel 4 Output Voltage	0.8V adjustable output
PWRGD Pin (Pin 20) Output	Monitor Channel 1 output
Output Discharge Function	Enabled for all four buck regulators
Switching Frequency on Channel 1	1x switching frequency set by the RT pin
Switching Frequency on Channel 3	1x switching frequency set by the RT pin
SYNC/MODE Pin (Pin 43) Function	Forced PWM/automatic PWM/PSM mode setting with the ability to synchronize to an external clock
Hiccup Protection	Enabled for overcurrent events
Short-Circuit Latch-Off Function	Disabled for output short-circuit events
Oversupply Latch-Off Function	Disabled for output oversupply events
Reset Timeout Period	200 ms
Watchdog Timeout Period	1.6 sec
Manual Reset Input Mode	Processor manual reset mode



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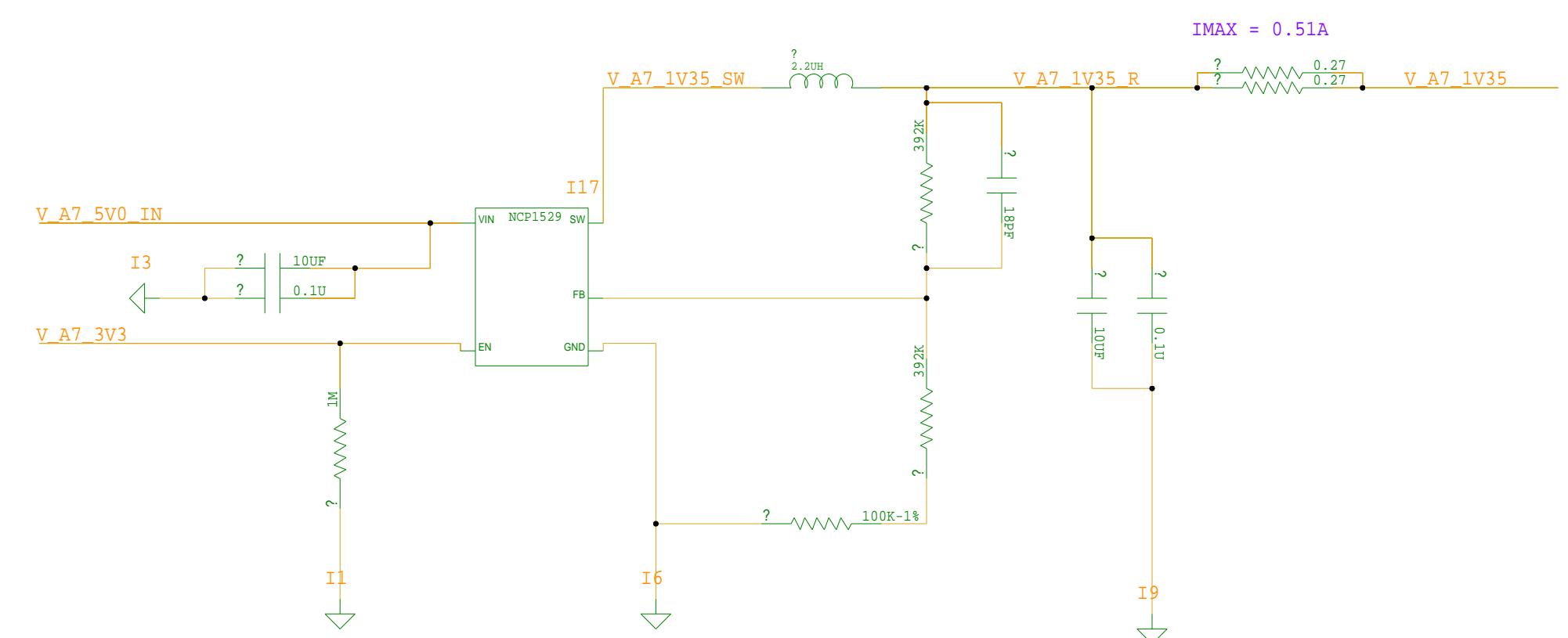
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ARTIX-7 POWER (3)

$$V_{out} = V_{FB} \times (1 + R1/R2)$$

- V_{OUT} : Output Voltage (V)
- V_{FB} : Feedback Voltage = 0.6 V
- $R1$: Feedback Resistor from V_{OUT} to FB
- $R2$: Feedback Resistor from FB to GND

4



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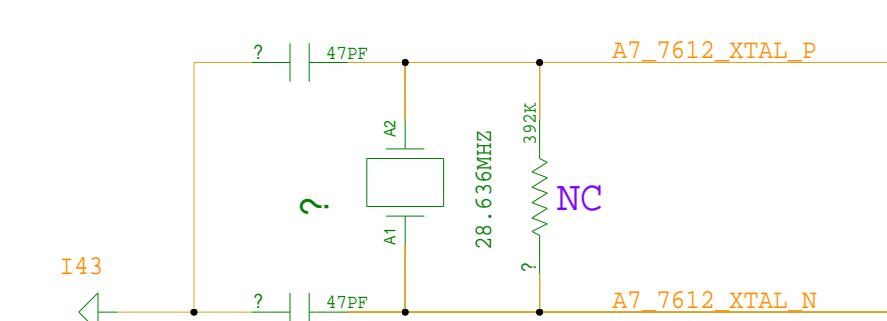
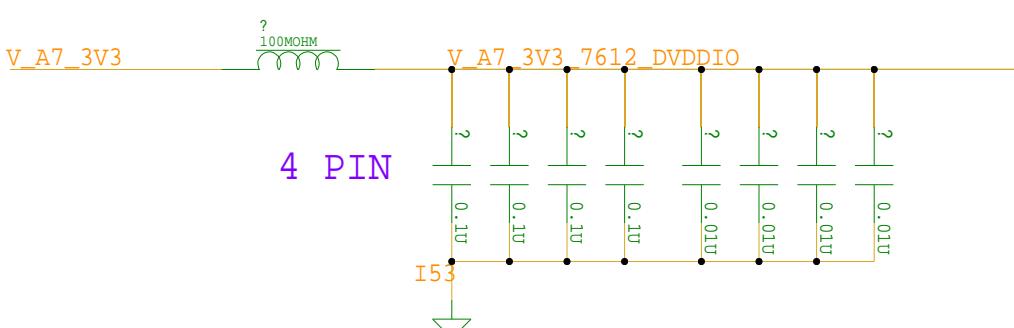
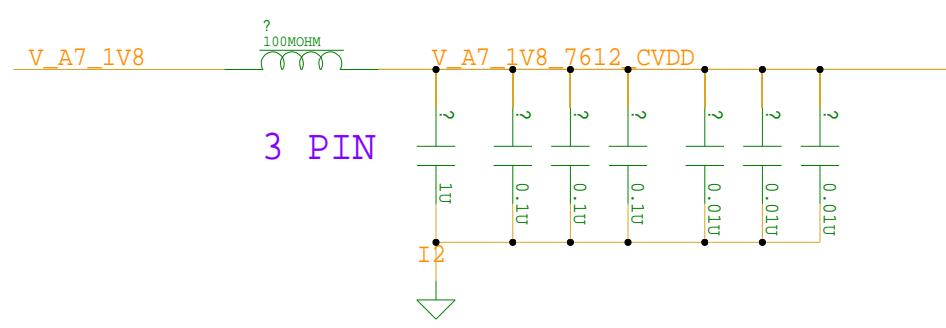
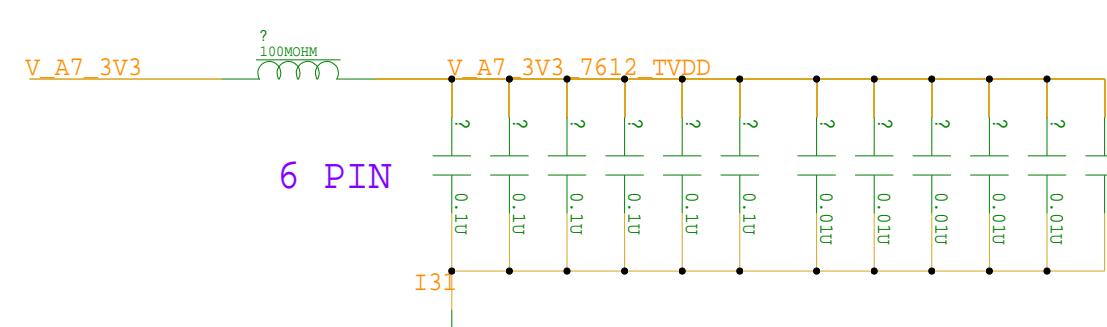
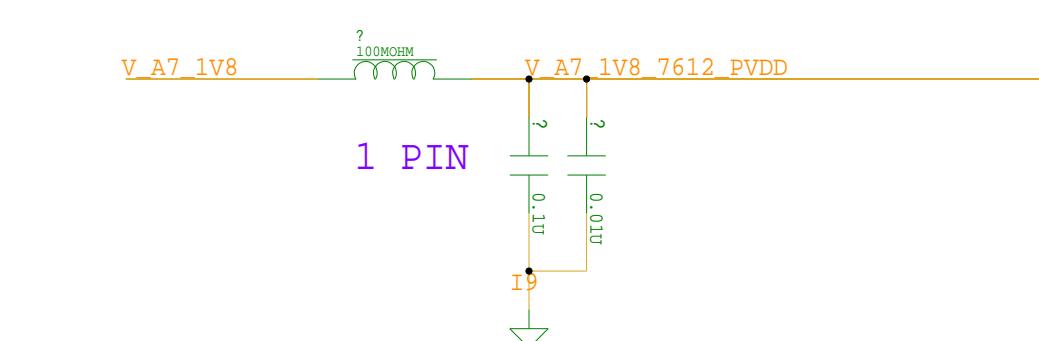
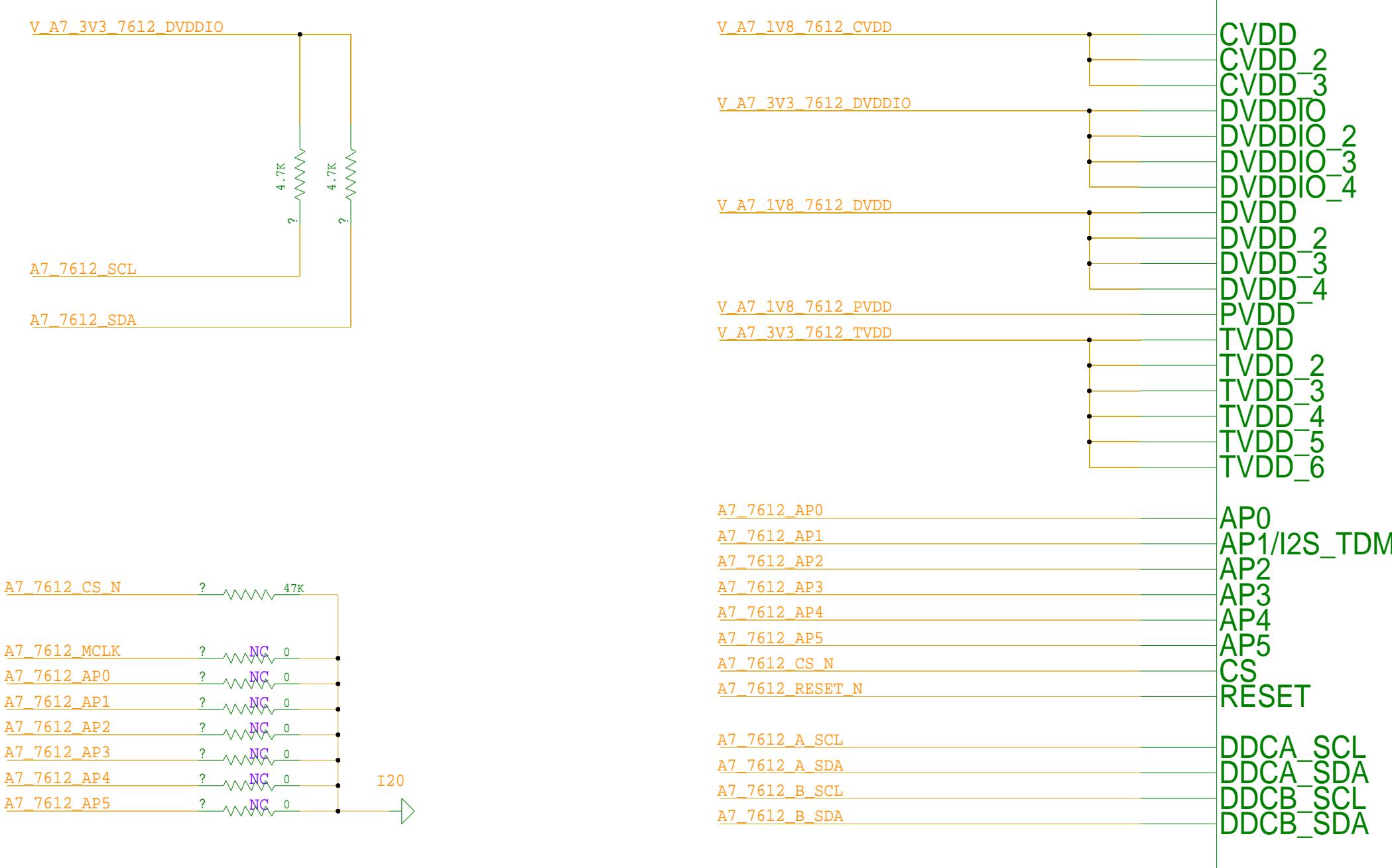
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ARTIX-7 HDMI RECEIVER (1)

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Page 1

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Page 1

ARTIX-7 HDMI RECEIVER (2)

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 A7_7612_P1
 A7_7612_P2
 A7_7612_P3
 A7_7612_P4
 A7_7612_P5
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 A7_7612_P8
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 A7_7612_P11
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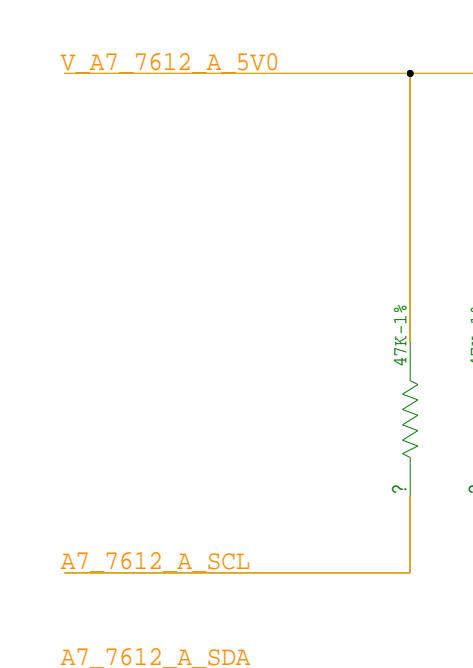
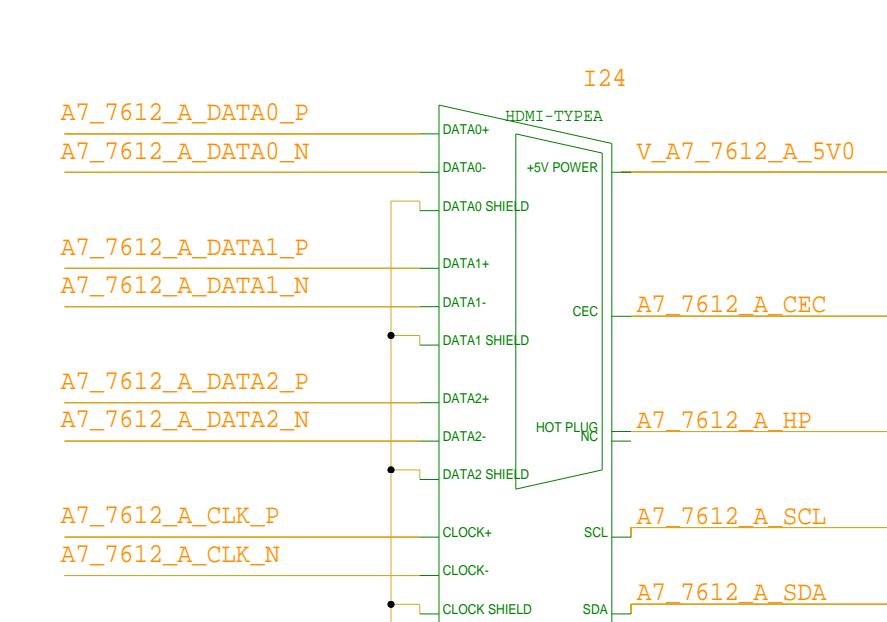
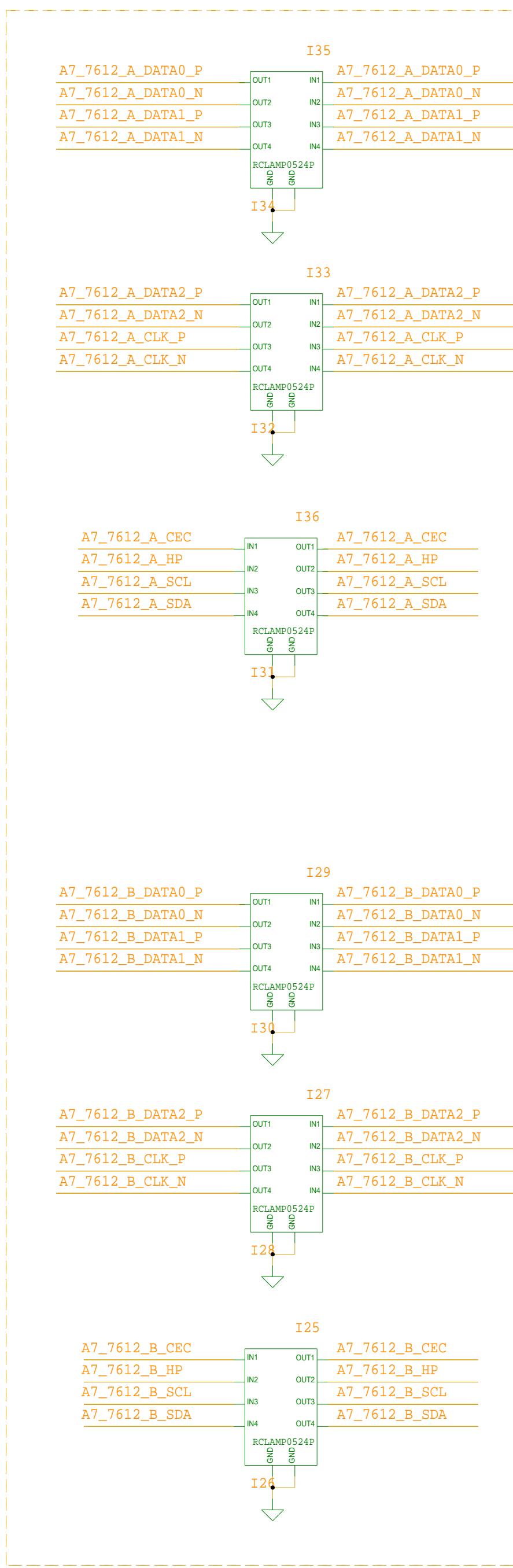
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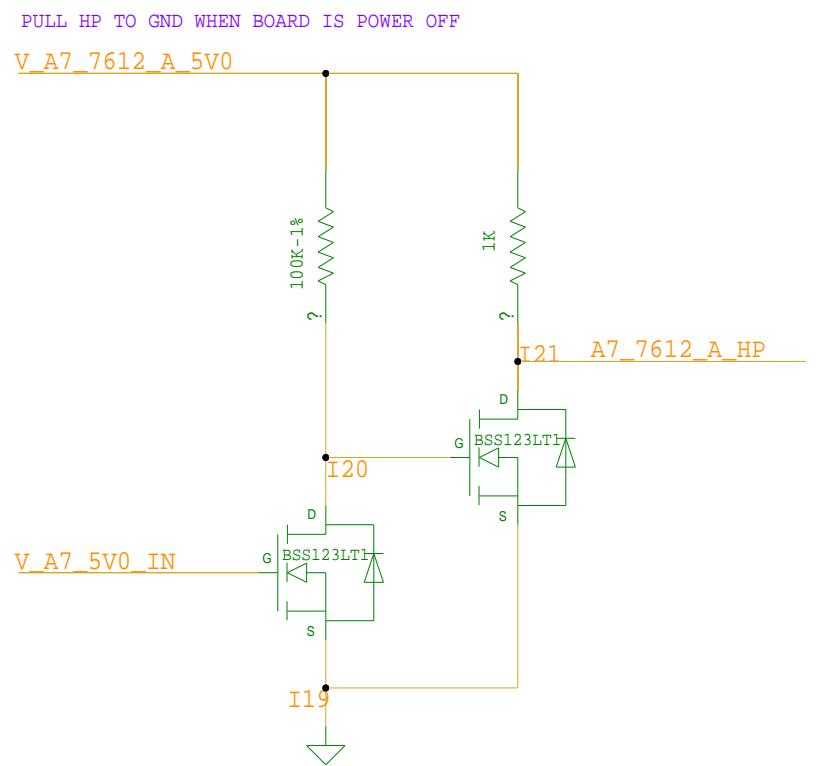
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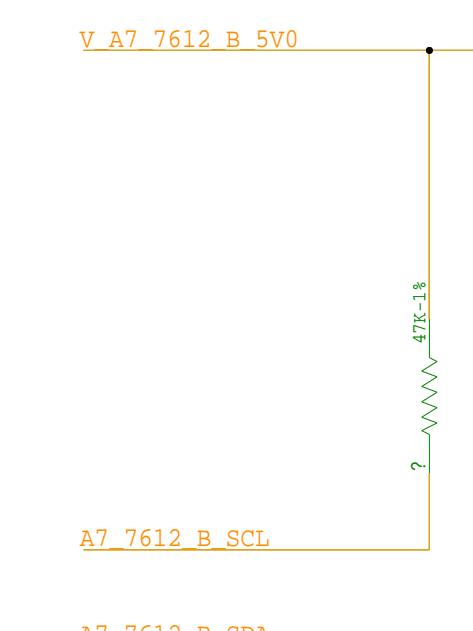
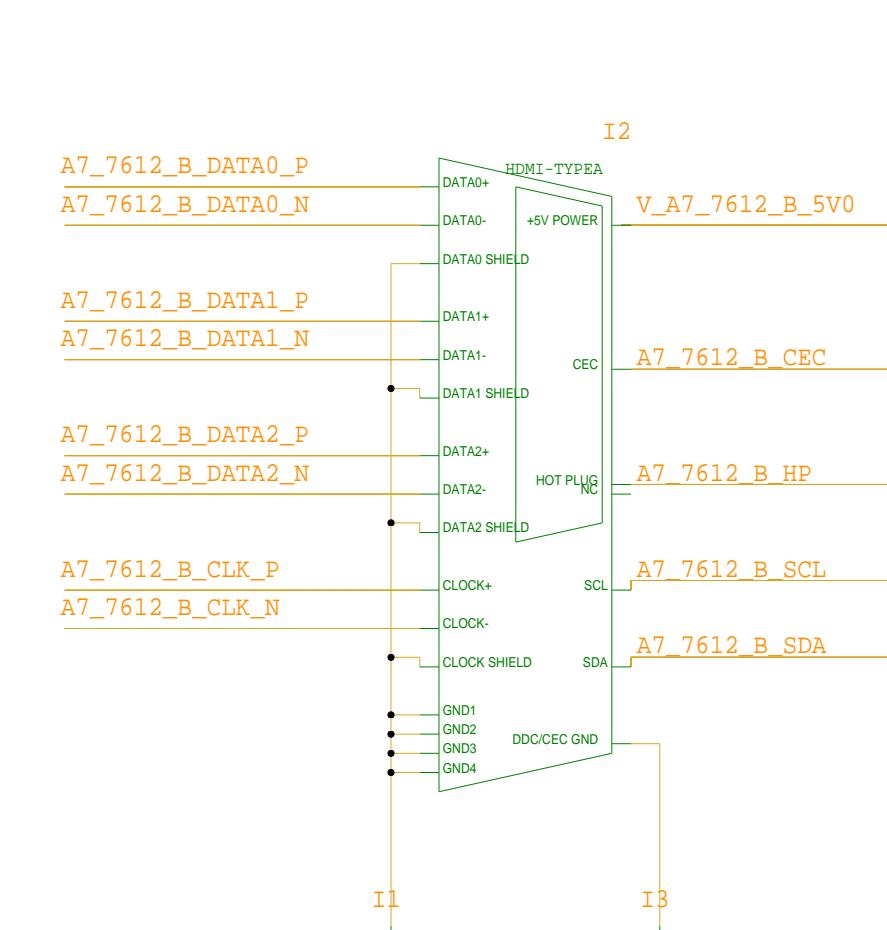
CHANGE CONNECTION DUE TO LAYOUT



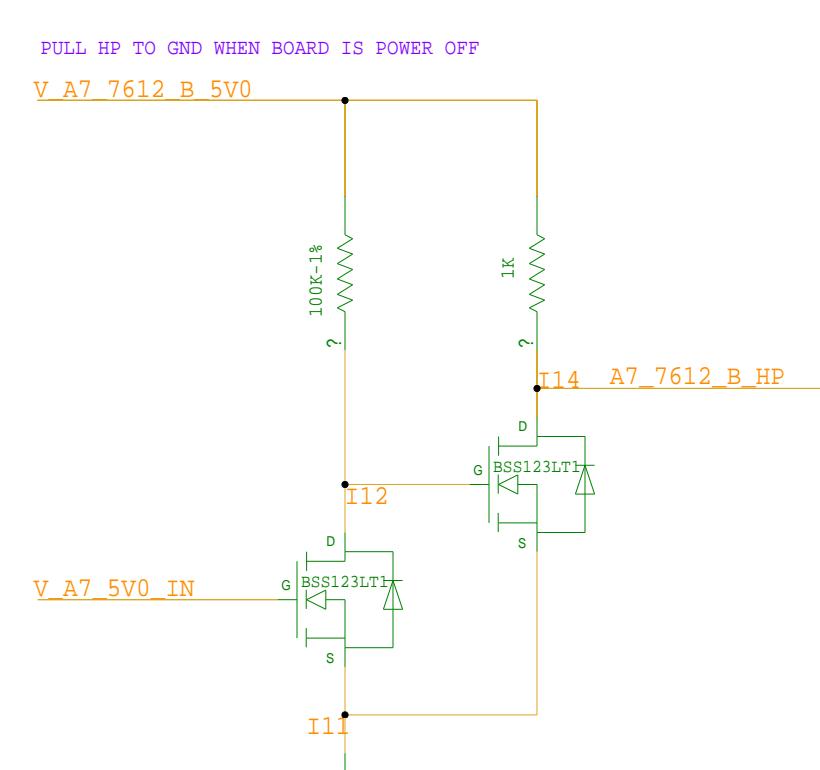
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V_A7_3V3_7612_DVDDIO



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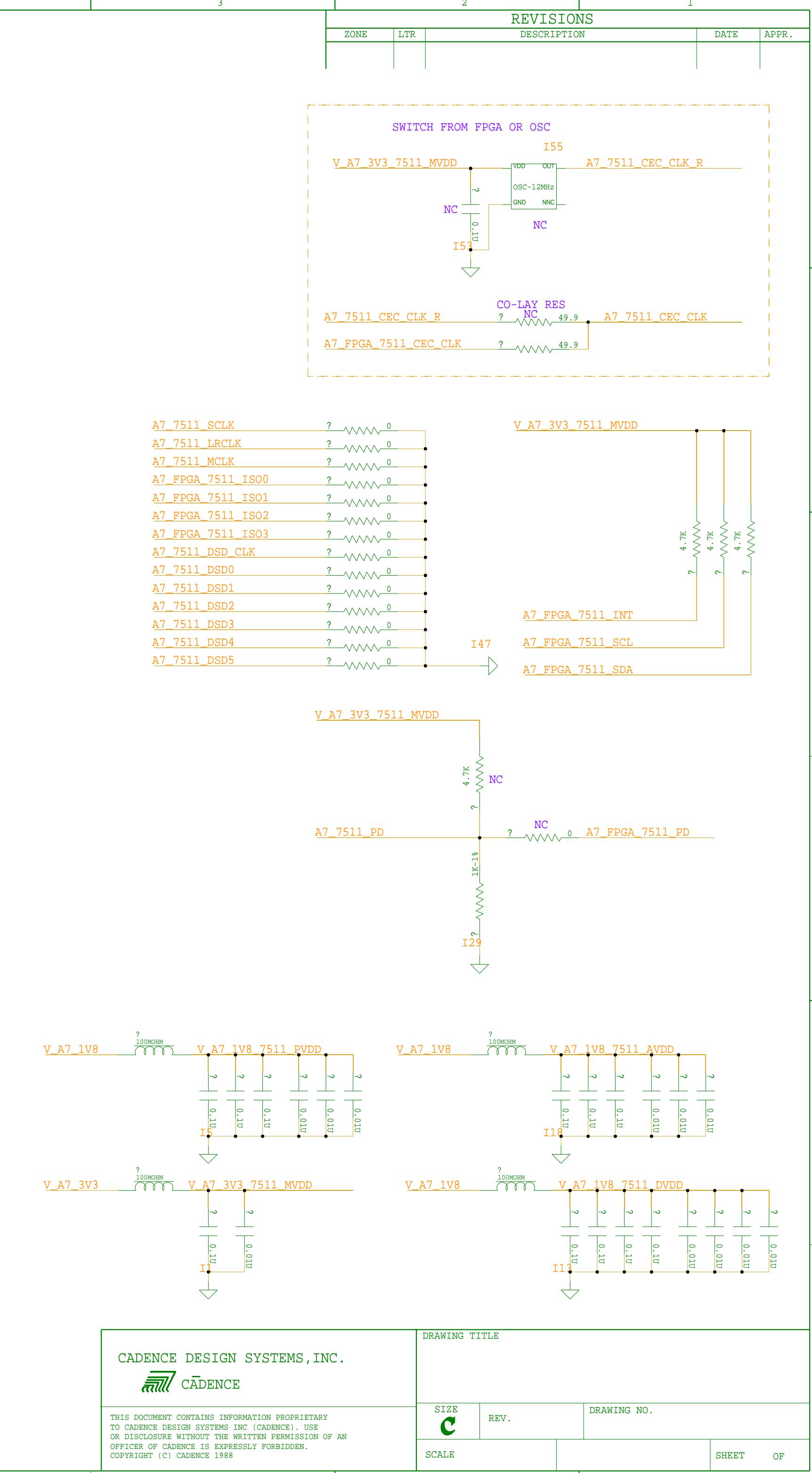
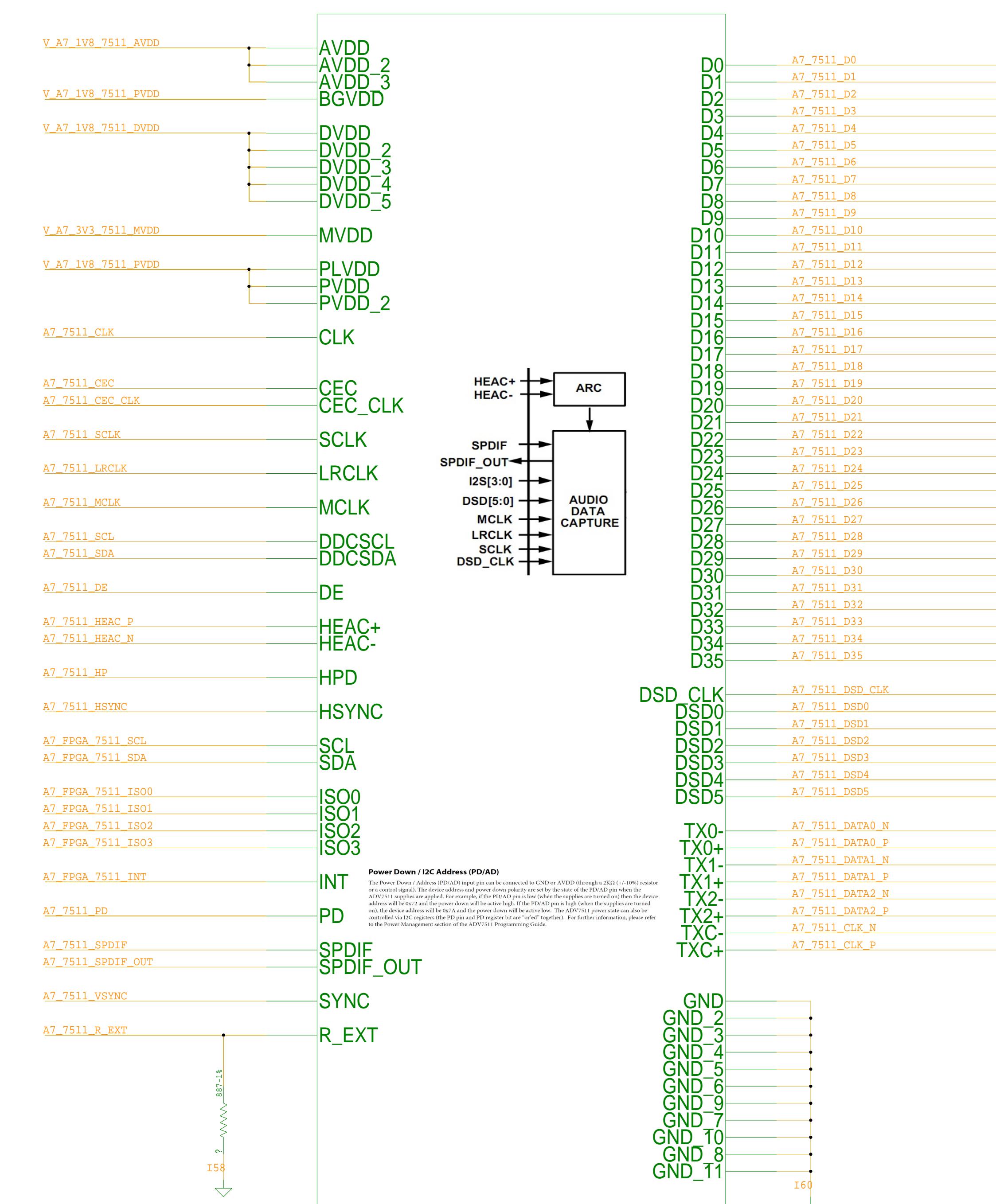
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ARTIX-7 HDMI TRANSMITTER (1)

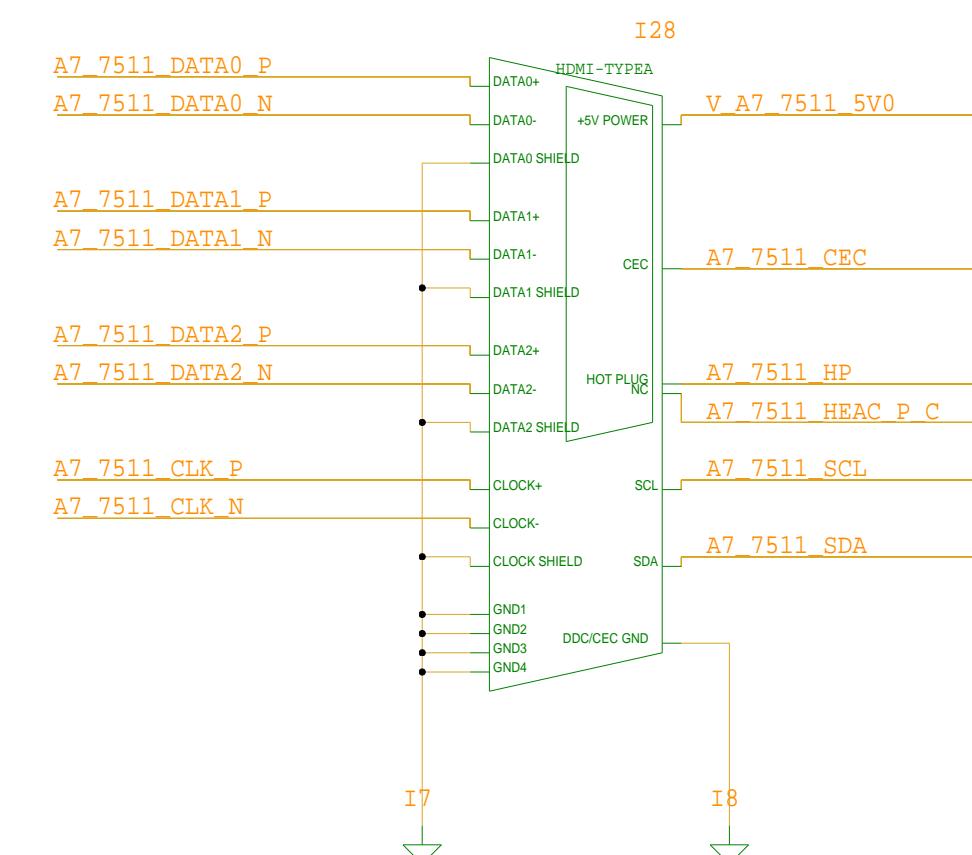
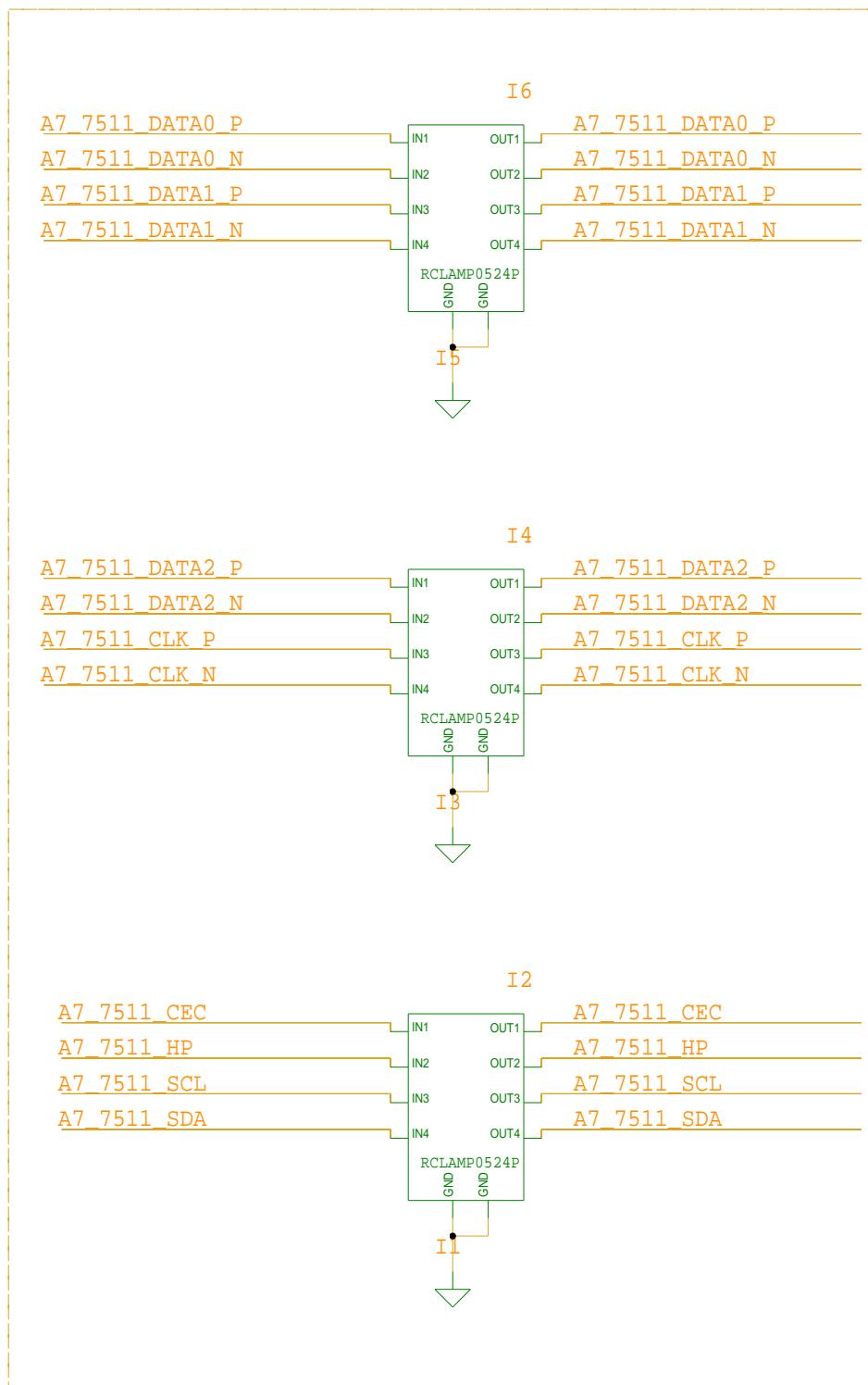


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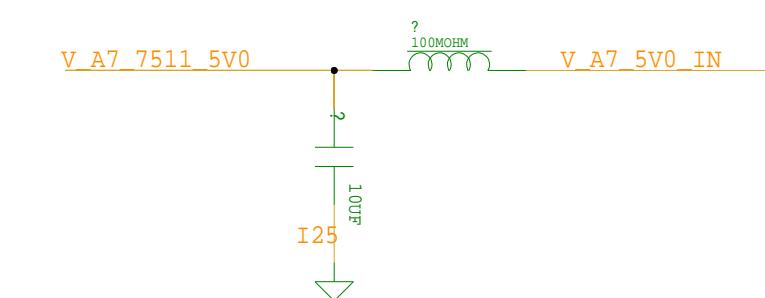
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CHANGE CONNECTION DUE TO LAYOUT



CLOSE TO HDMI CONNECTOR

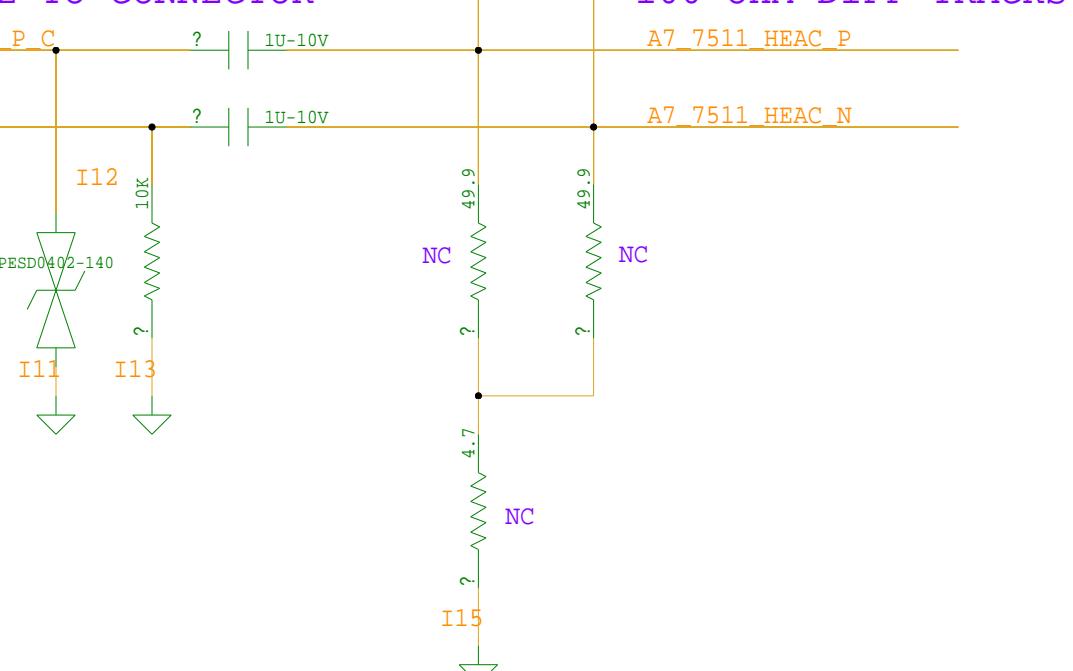


A7_7511_CEC

? IN4148 ? 27.4K V_A7_3V3_7511_MVDD

V_A7_1V8_7511_DVDD

CAPS CLOSE TO CONNECTOR



A7_7511_SCL ? 1.8K-1% V_A7_7511_5V0
A7_7511_SDA ? 1.8K-1%

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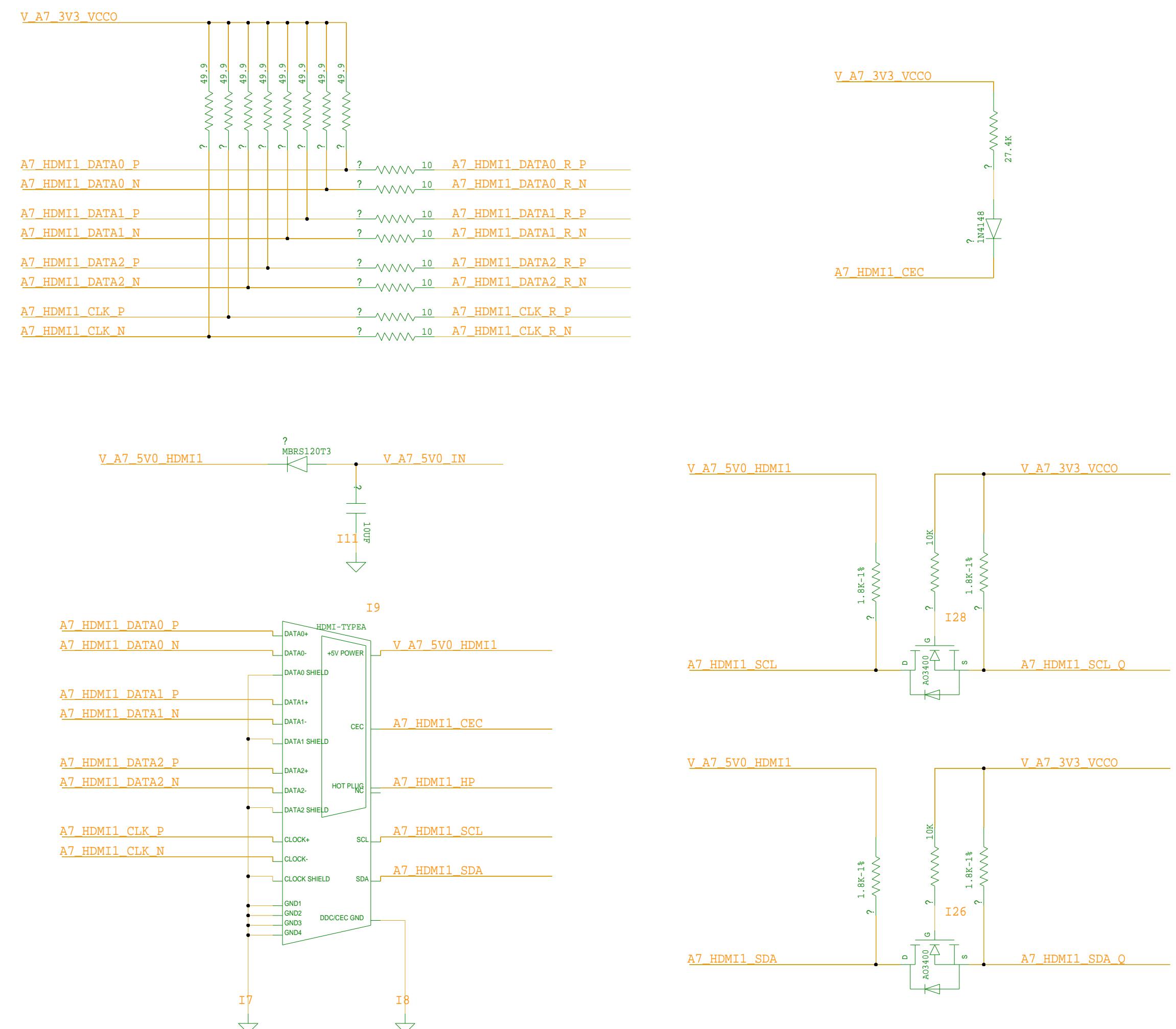
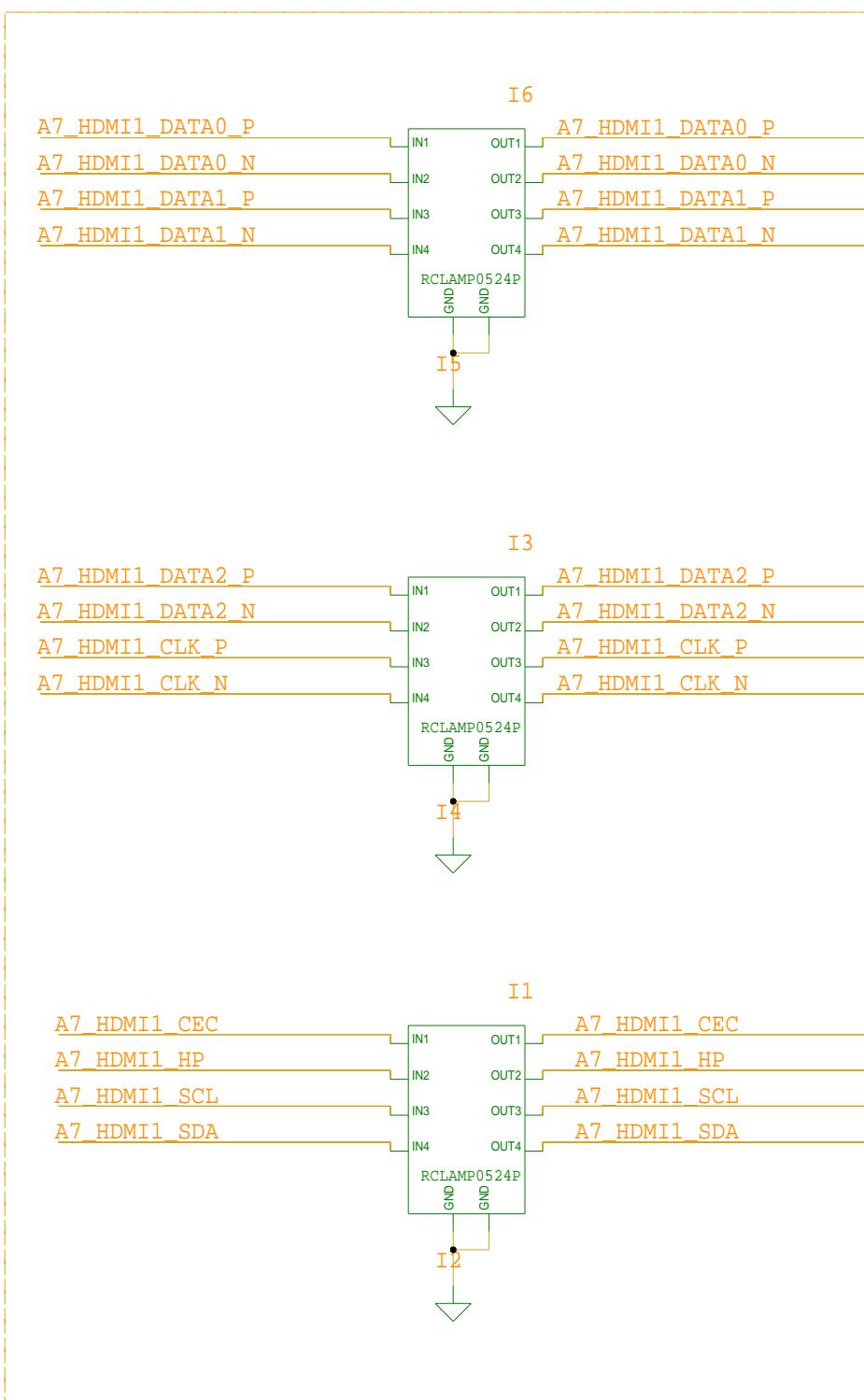
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ARTIX-7 HDMI INOUT (1)

CHANGE CONNECTION DUE TO LAYOUT



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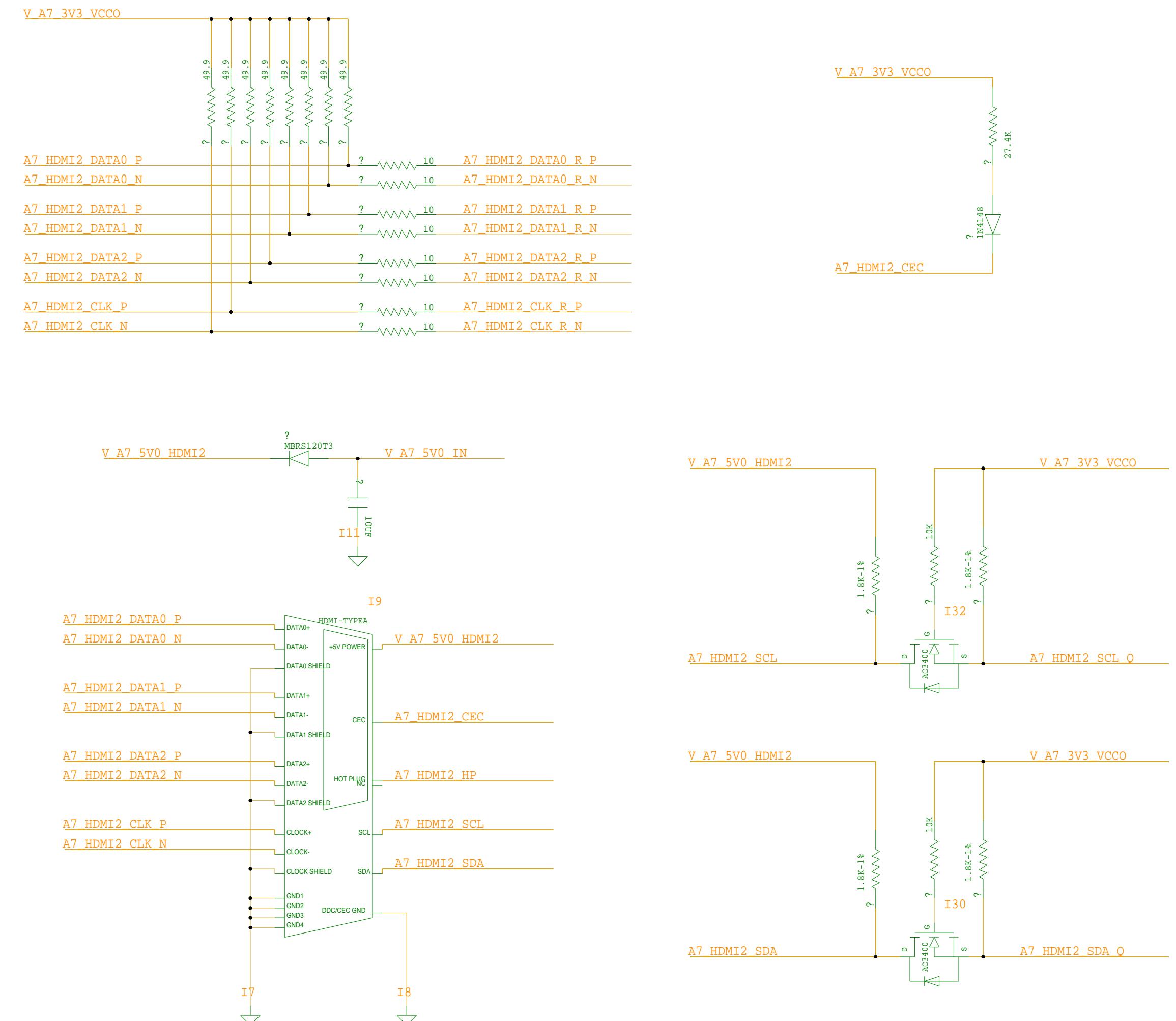
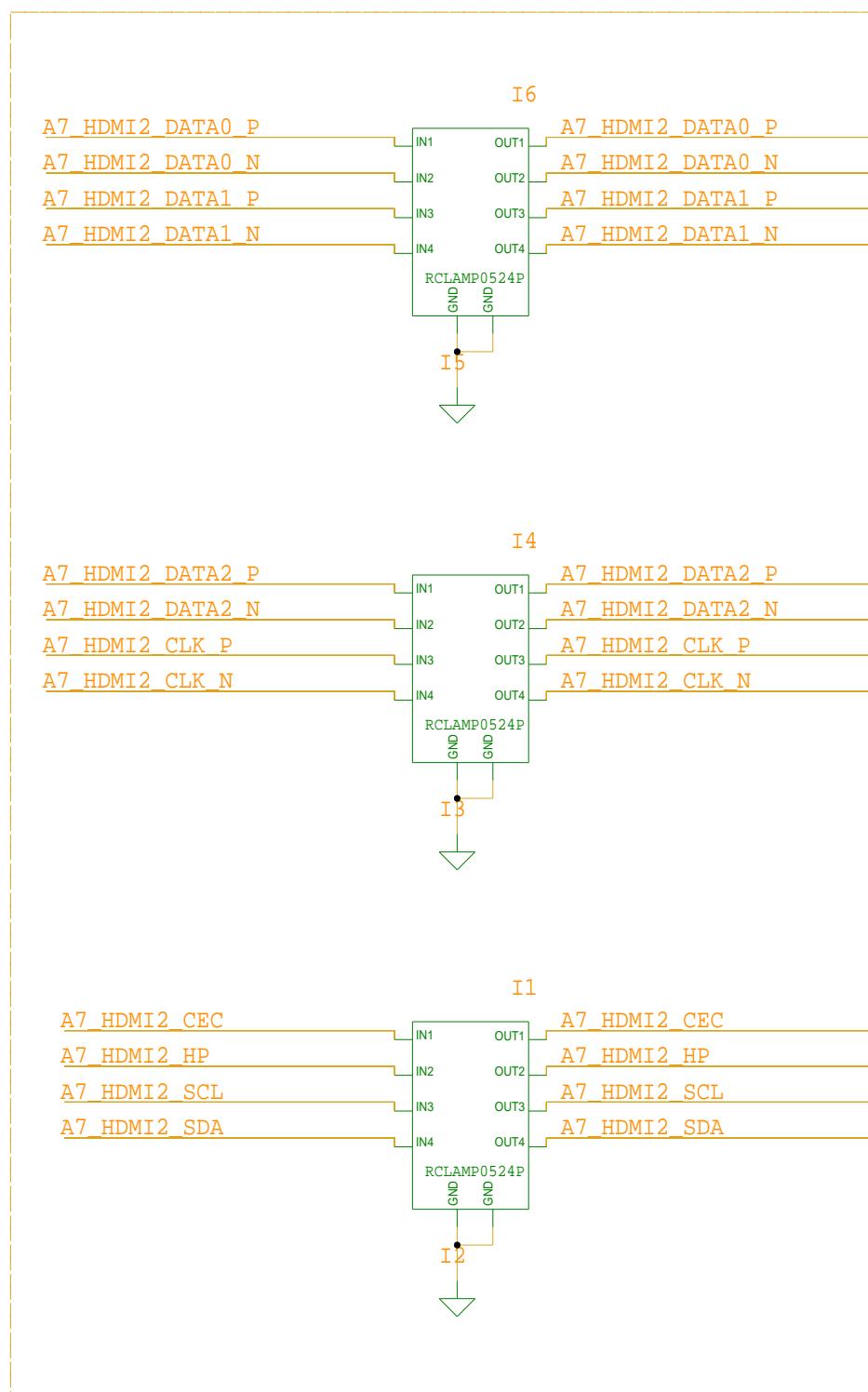
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ARTIX-7 HDMI INOUT (2)

REVISED

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CHANGE CONNECTION DUE TO LAYOUT



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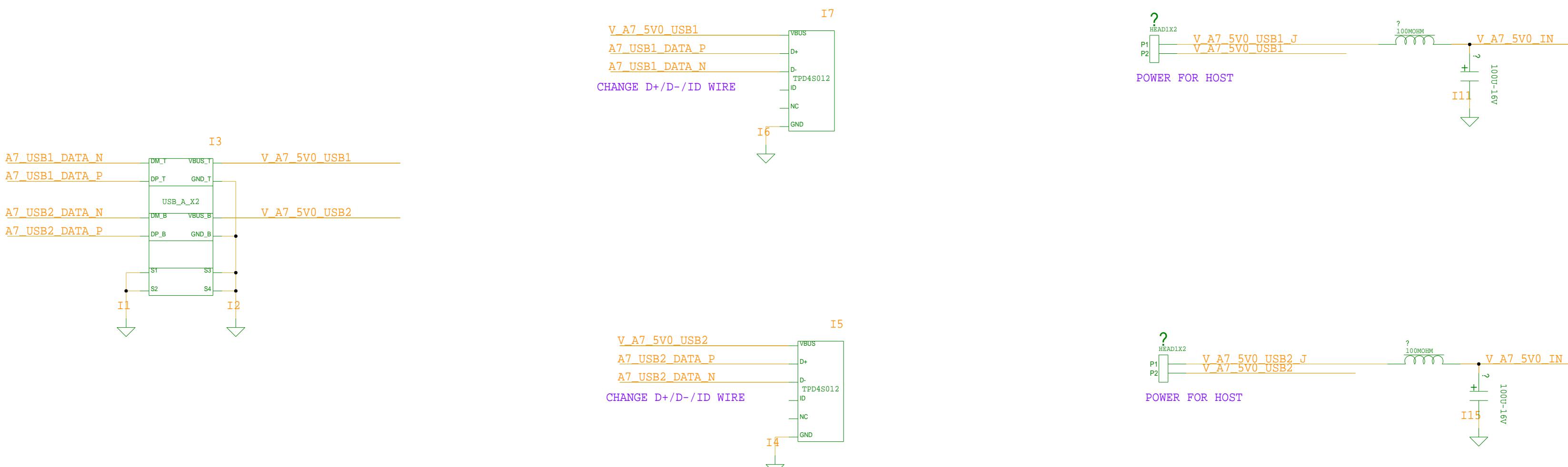
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ARTIX-7 USB INOUT

REVOLUTIONS

ZONE	LTR	DESCRIPTION	DATE	APPR.



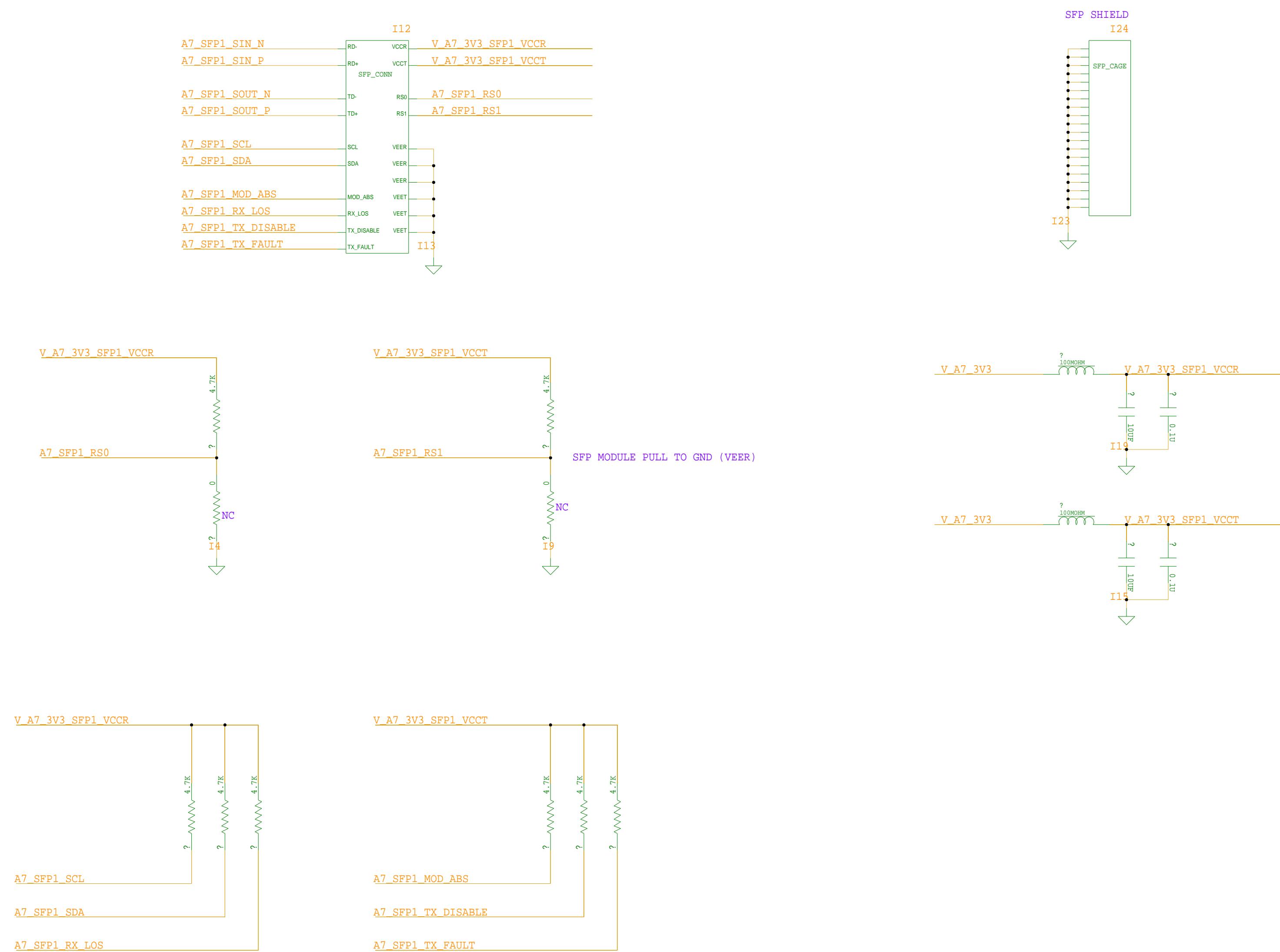
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ZONE	LTR	DESCRIPTION	DATE	APPR.

ARTIX-7 SFP+ / SFP INOUT (1)



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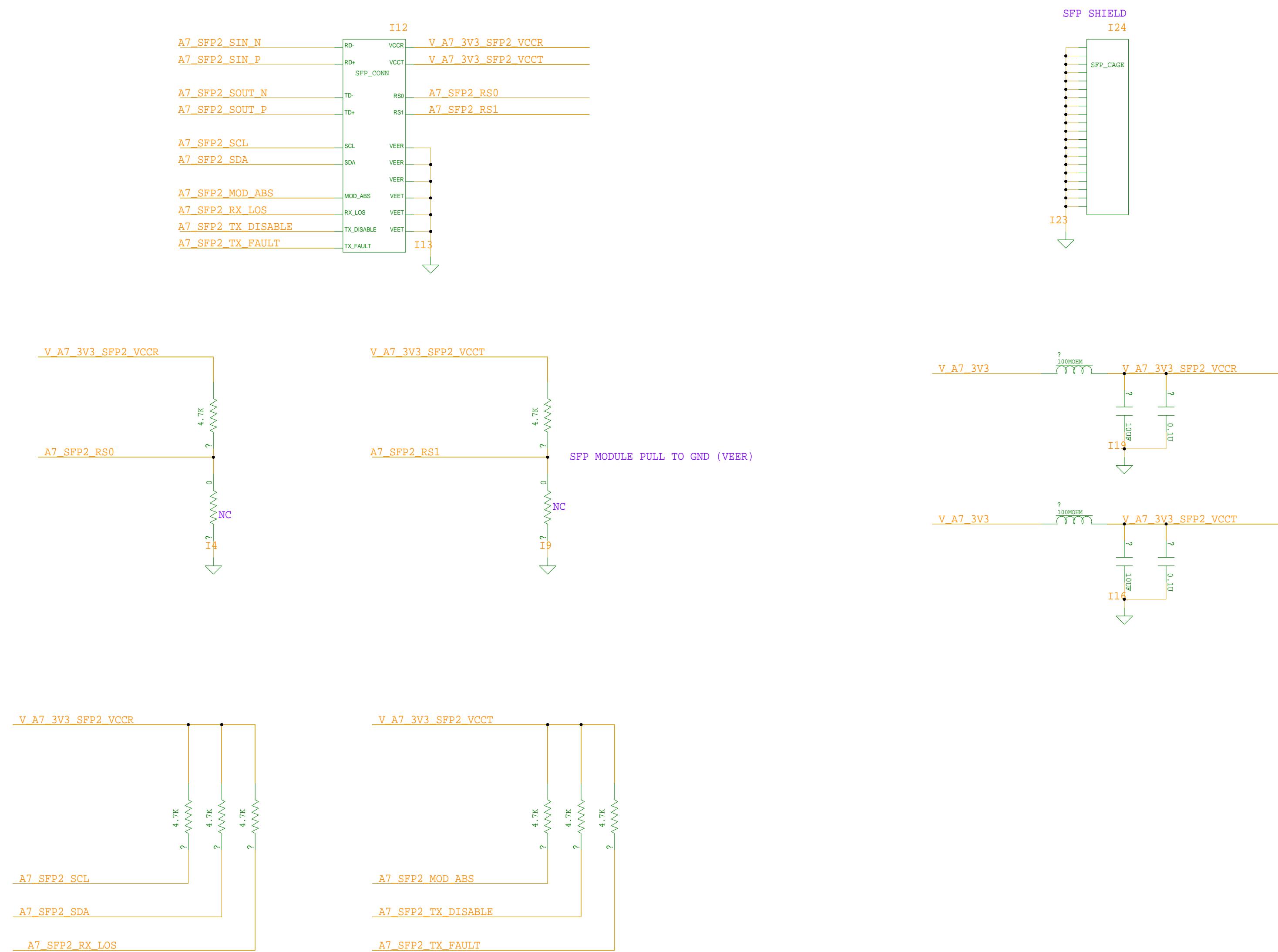
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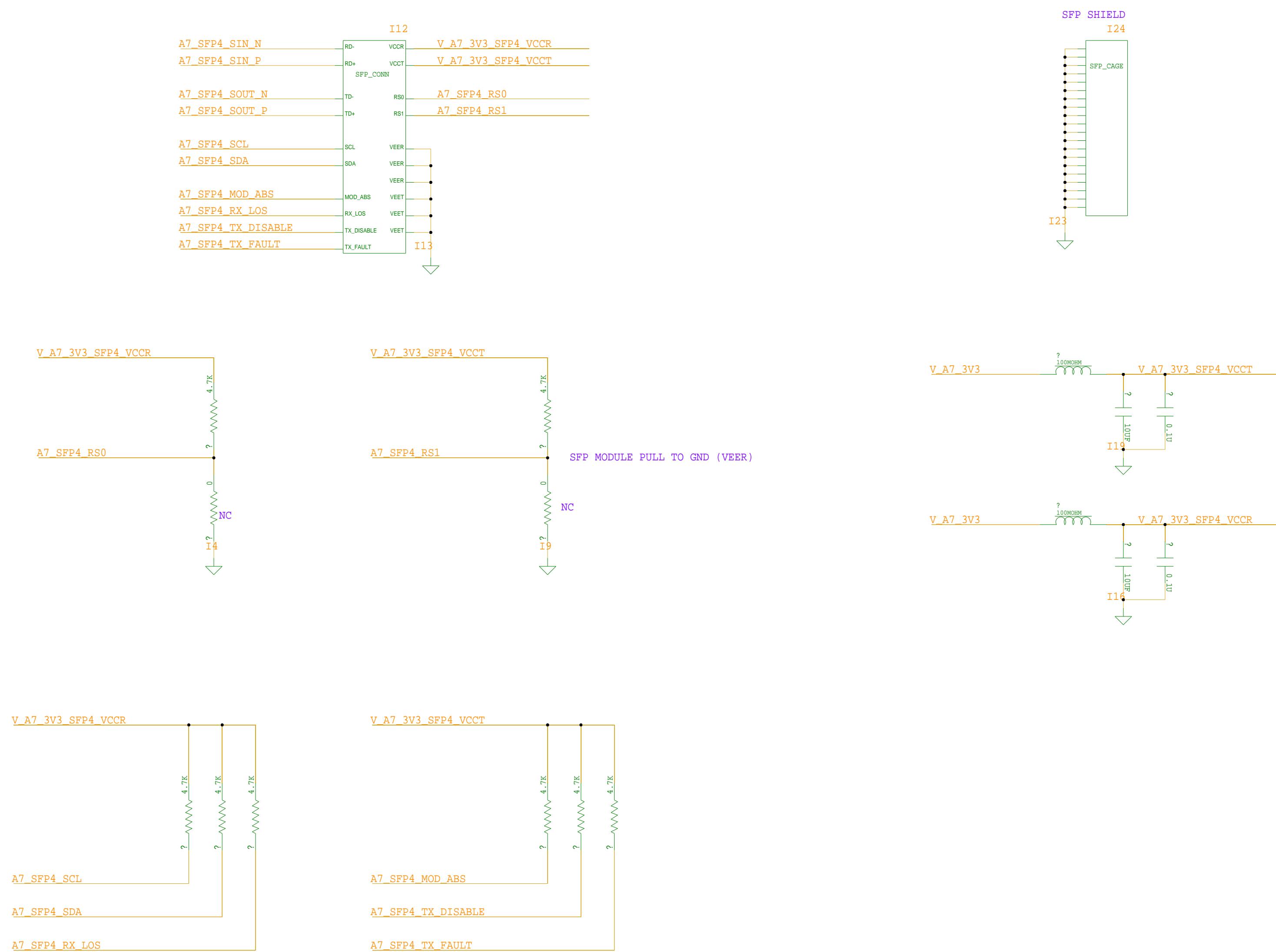
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ARTIX-7 SFP+/SFP INOUT (4)



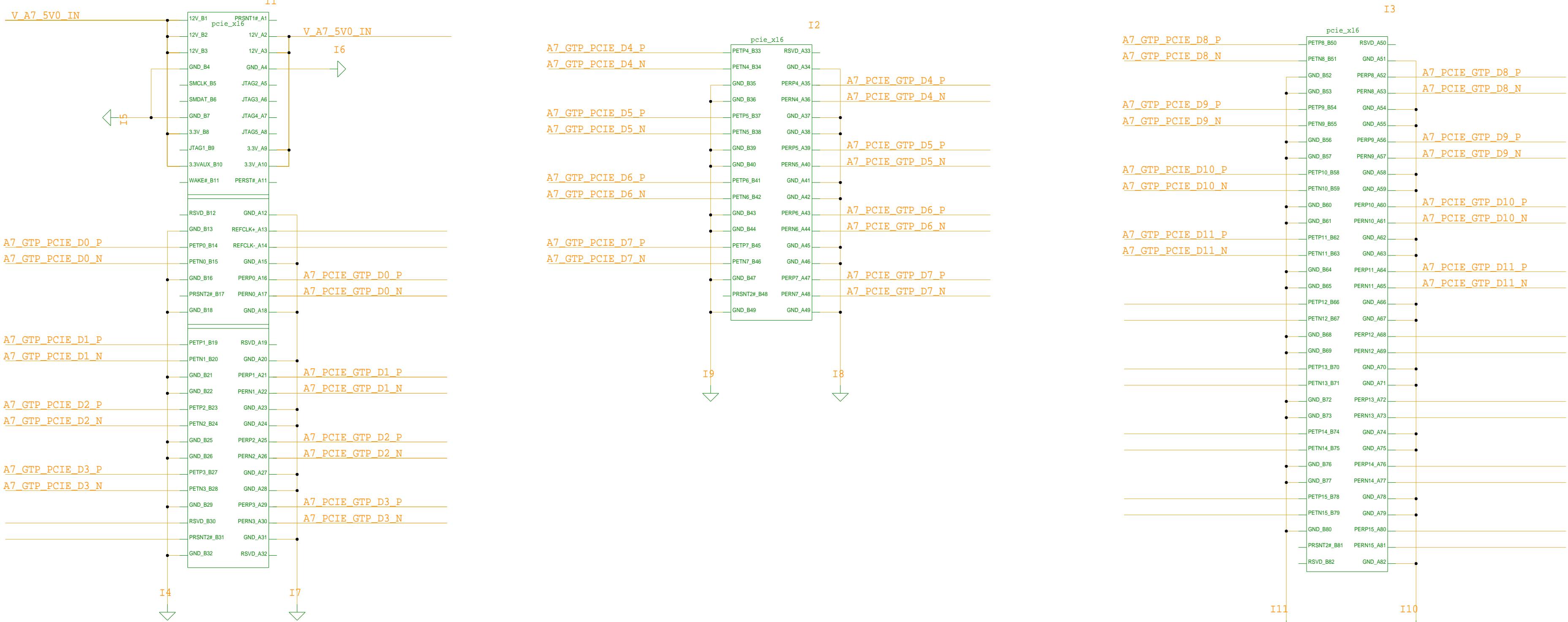
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ARTIX-7 PCIE X16 CONN

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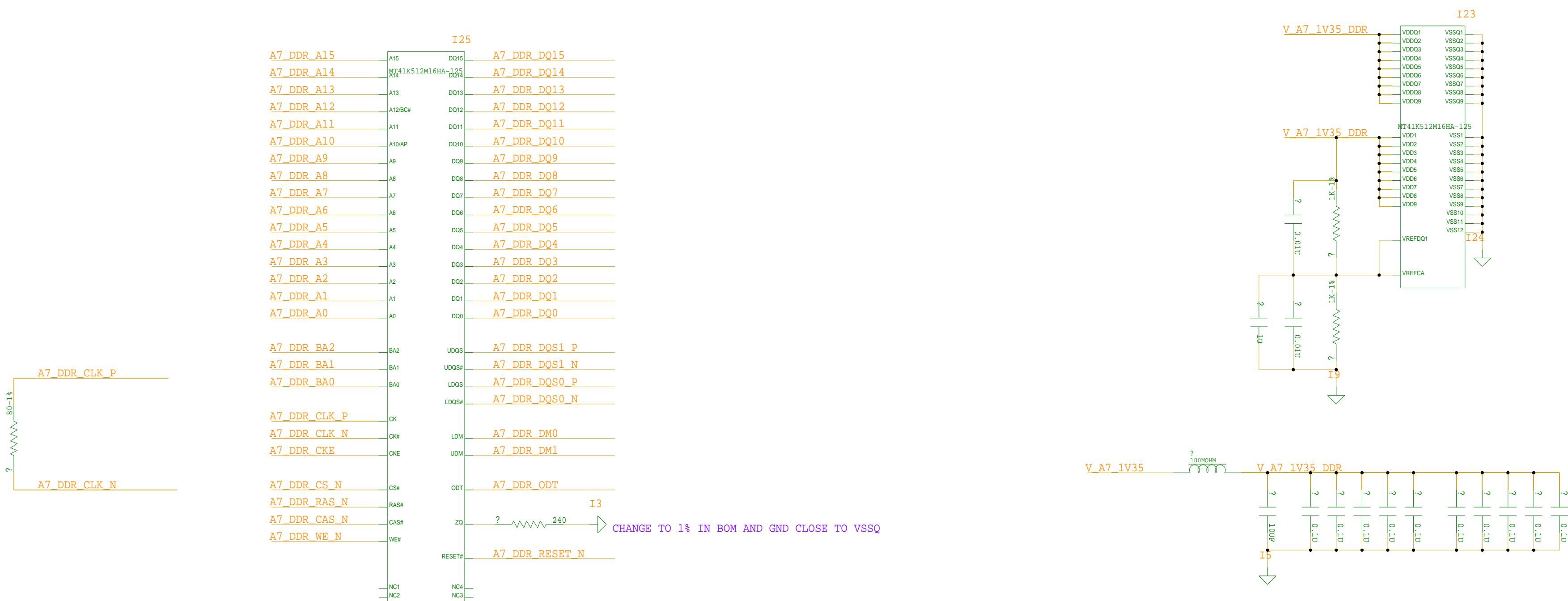
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ARTIX-7 DDR3

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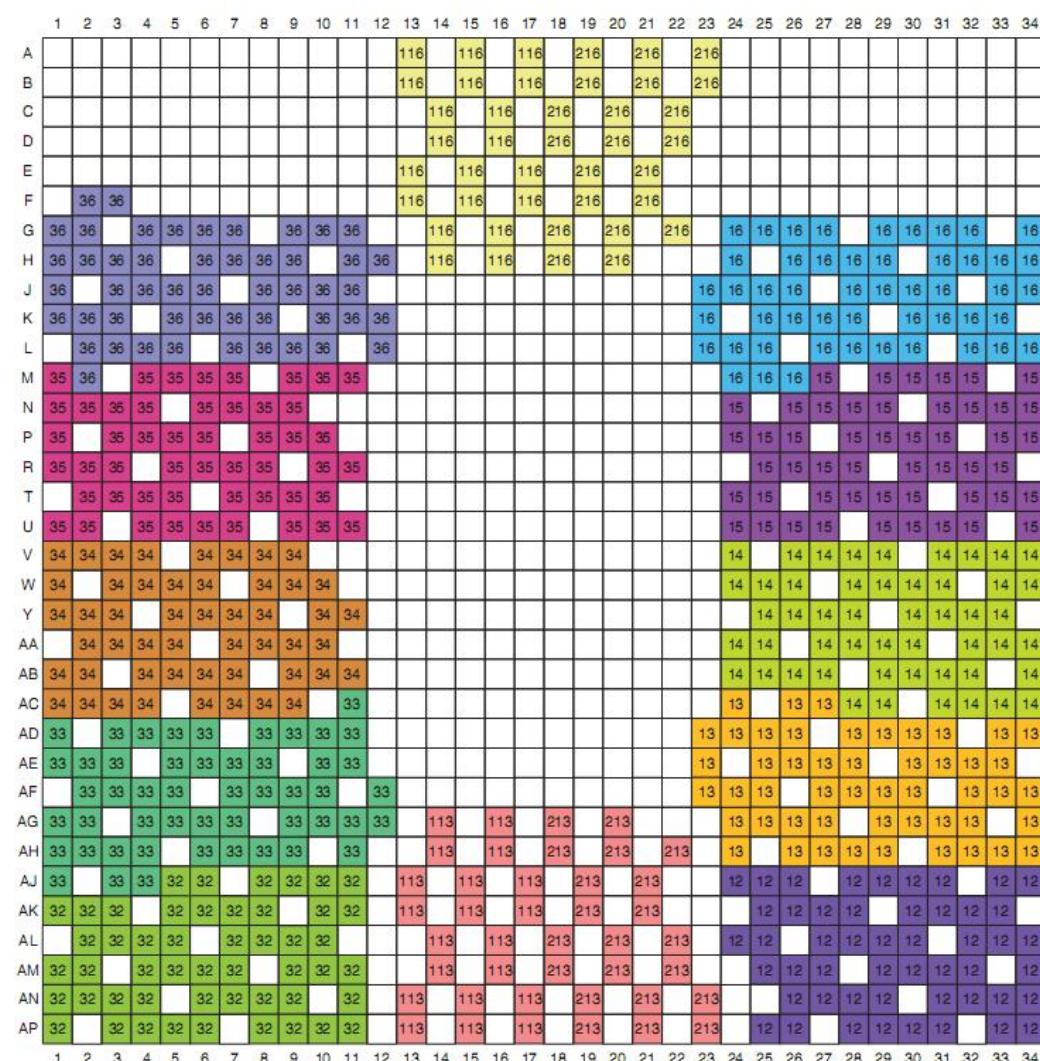


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ARTIX-7 PINOUT MAP

REVISIONS

ZONE	LTR	DESCRIPTION	DATE	APPR.



BANK0 : 3.3V CONFIG

BANK36 : 3.3V USB INOUT 1/2 SFP+ MUX

BANK35 : 3.3V NC

BANK34 : 1.35V DDR3

BANK33 : 3.3V NC

BANK32 : 3.3V NC

BANK16 : 3.3V NC

BANK15 : 3.3V HDMI RECEIVER

BANK14 : 3.3V SPI FLASH

BANK13 : 3.3V HDMI INOUT 1/2

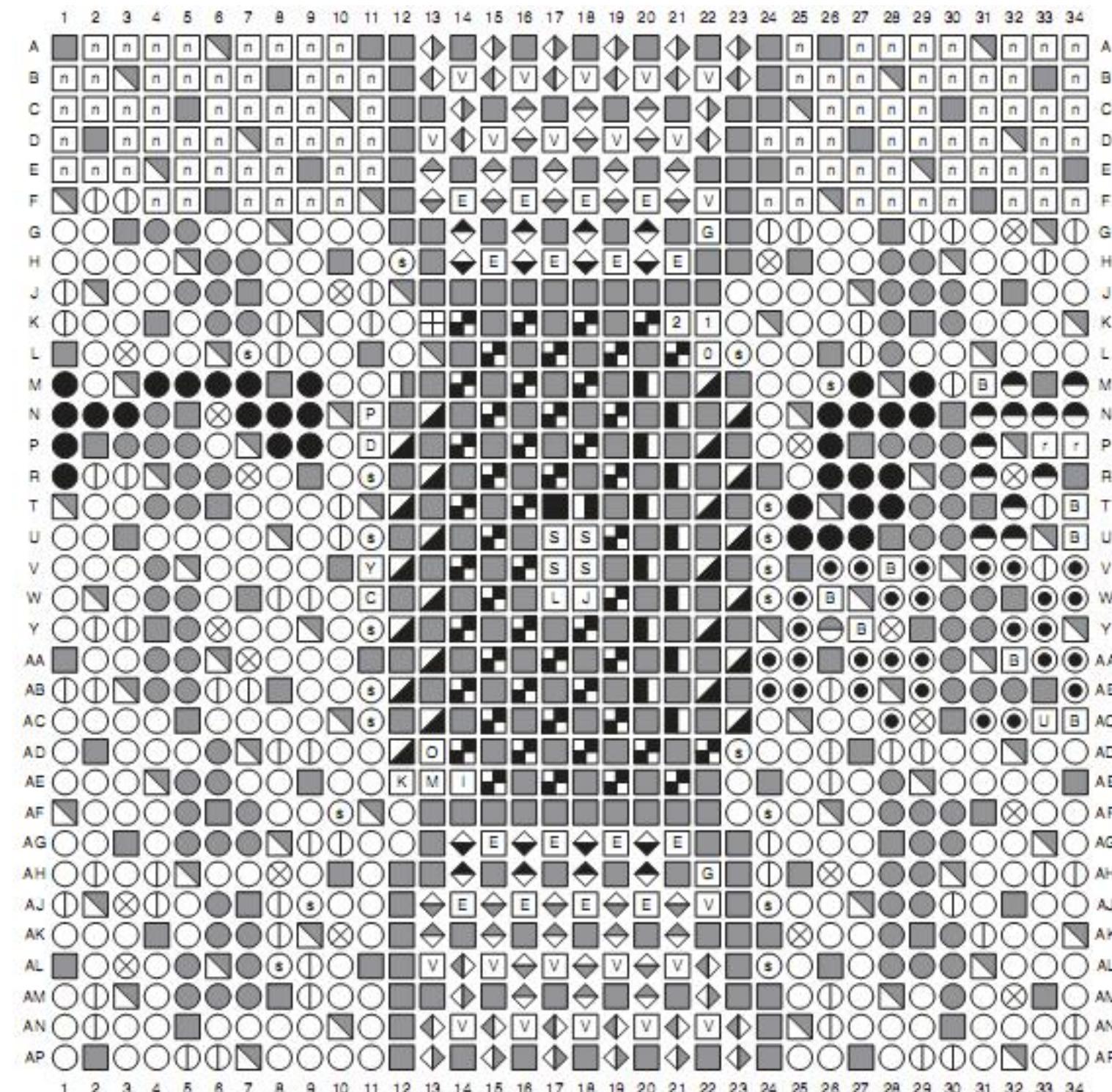
BANK12 : 3.3V HDMI TRANSMITTER

BANK116 : 3.3V PCIE X4

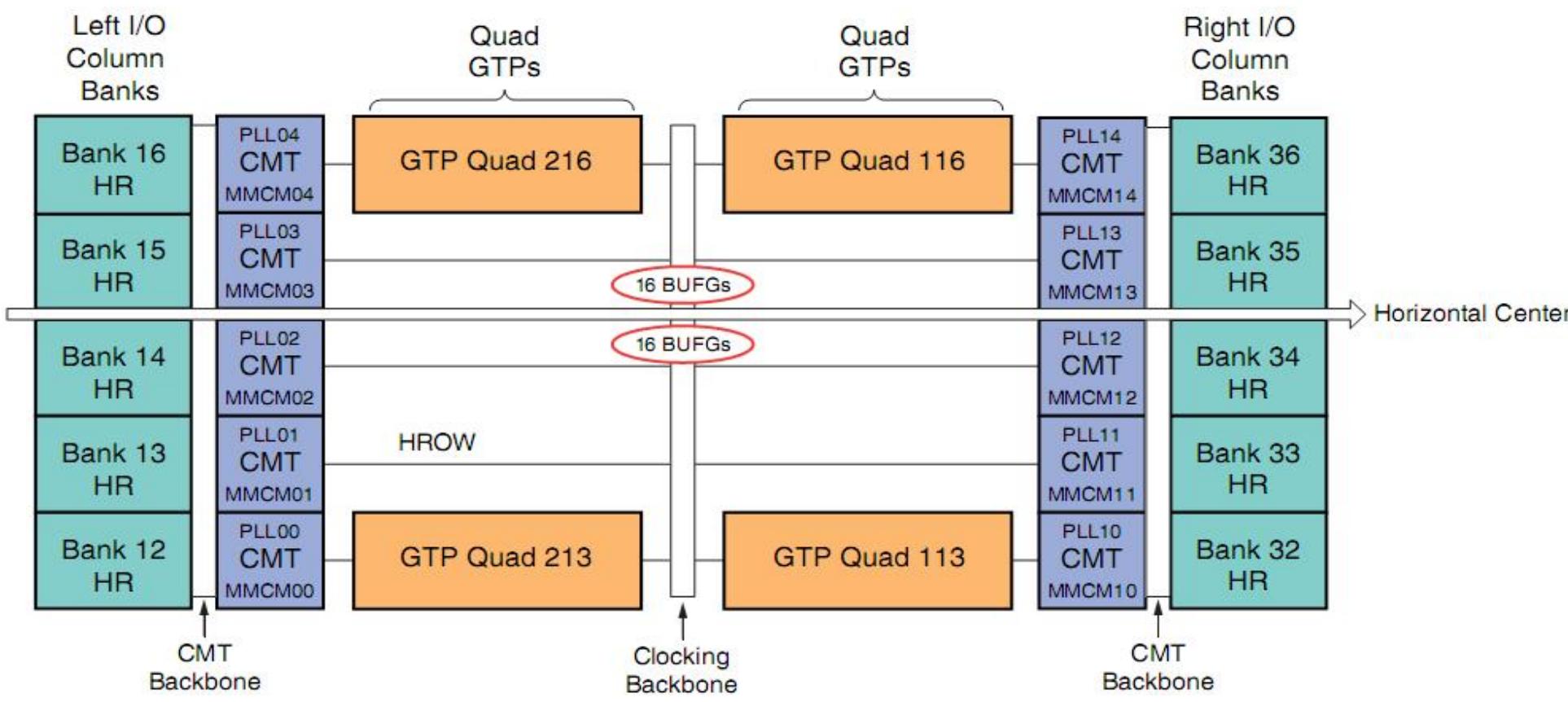
BANK216 : 3.3V SFP+ *4

BANK113 : 3.3V PCIE X4

BANK213 : 3.3V PCIE X4



All HR I/O banks and the GTP Quads are fully bonded out in this package.



User I/O Pins	Transceiver Pins	Dedicated Pins	Other Pins
○ IO_LXXY_# ● IO_XX_#	E MGTAVCC_G# V MGTAVTT_G# A MGTVCVAUX_G# ◀ MGTAVTTRCAL G MGTREFREF B ADV_B B FCS_B B FOE_B B MOSI B FWE_B B DOUT_CSO_B B CSI_B B PUDC_B U RDWR_B r RSD-RS1 ● ADDP/ADON-AD15P/AD15N ● EMCCLK	C CCLK_0 V CFGBVS_0 A DONE_0 ◀ MGTAVTTRCAL J DXP_0 L DXN_0 ■ GNDADC_0 Y INIT_B_0 O M0_0 1 M1_0 2 M2_0 P PROGRAM_B_0 K TCK_0 I TDI_0 O TDO_0 M TMS_0 ■ VCCADC_0 ■ VCCBATT_0	GND VCCAUX_IO_G# VCCAUX VCCINT VCCO_# VCCBRAM NC
Multi-Function Pins			
	B ADV_B B FCS_B B FOE_B B MOSI B FWE_B B DOUT_CSO_B B CSI_B B PUDC_B U RDWR_B r RSD-RS1 ● ADDP/ADON-AD15P/AD15N ● EMCCLK	E VRN ○ VRP ○ VREF ● D00-D31 ● A00-A28 ○ DQS ○ MRCC ● SRCC	

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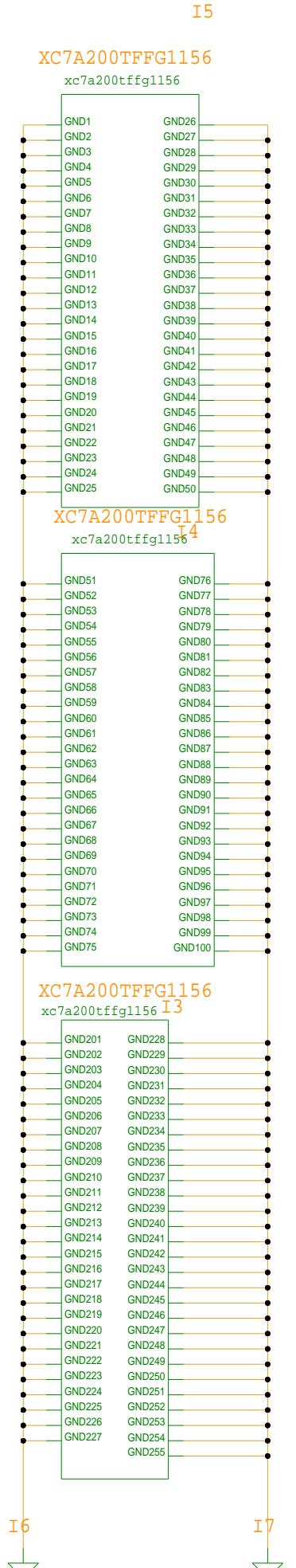
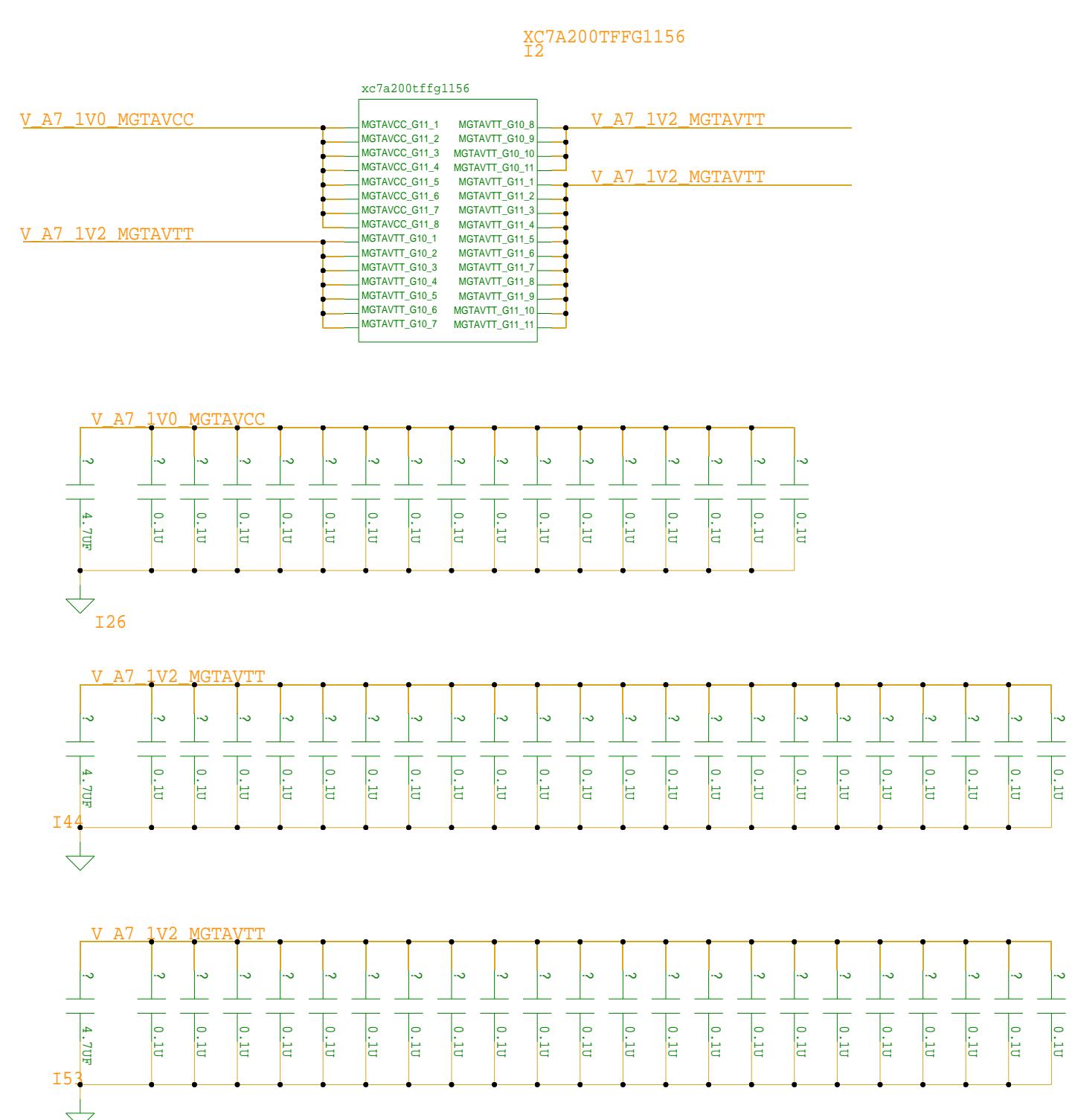
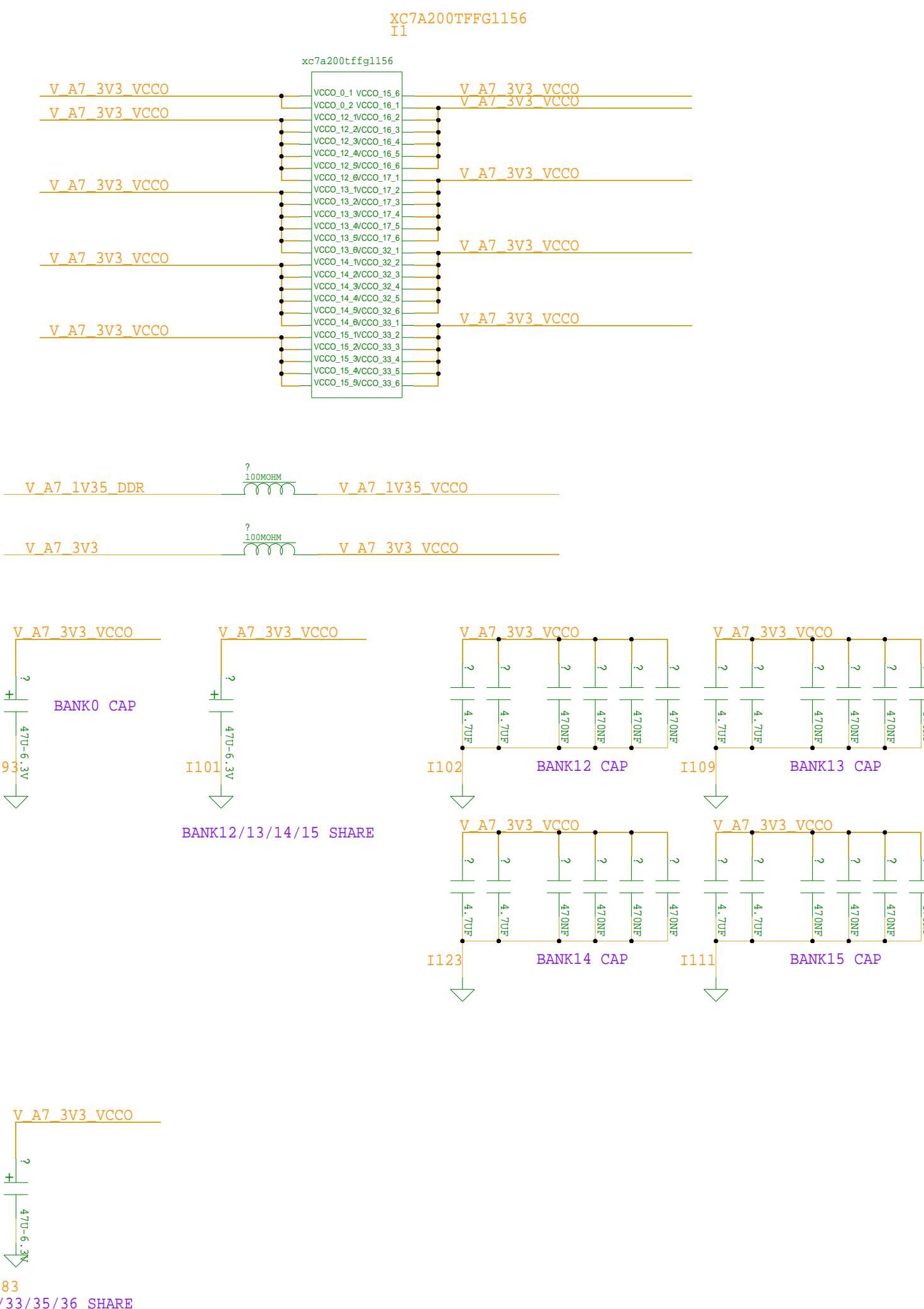


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ARTIX-7 BANK POWER (2)

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ARTIX-7 CLOCK

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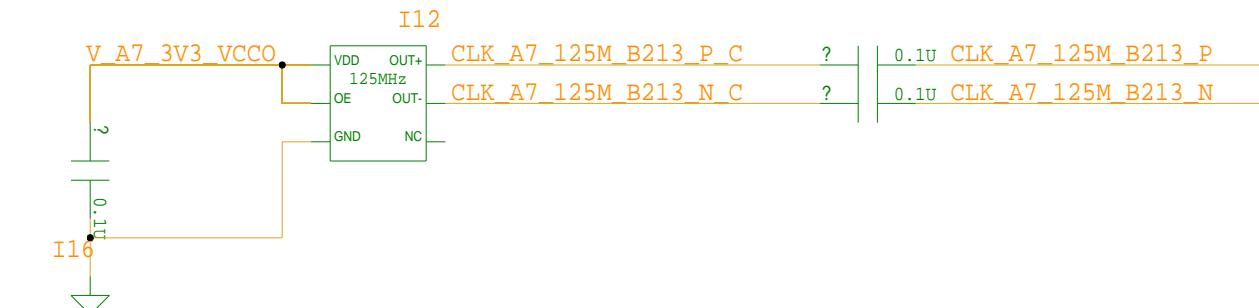
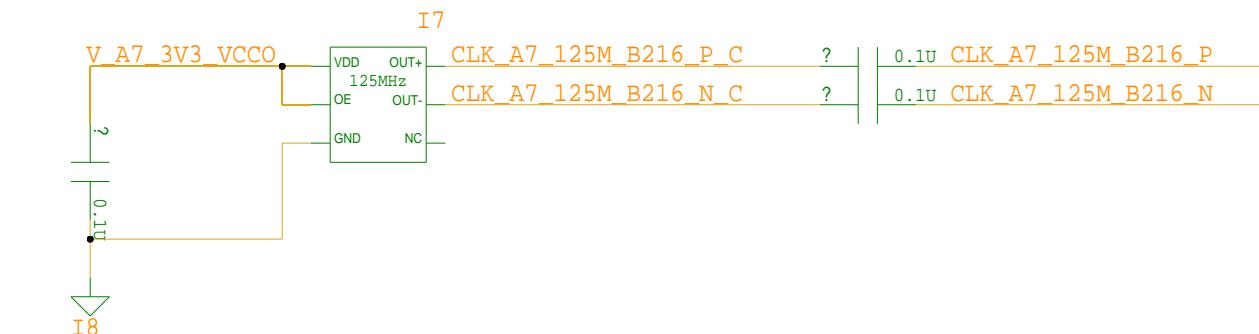
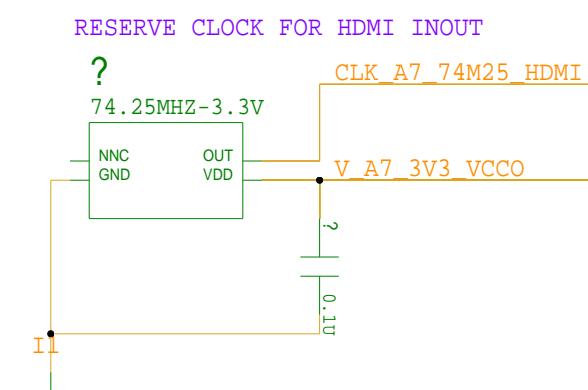
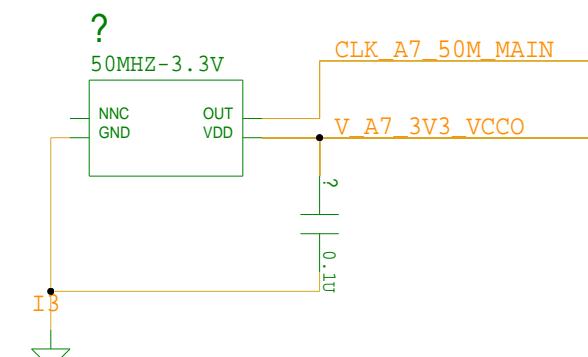
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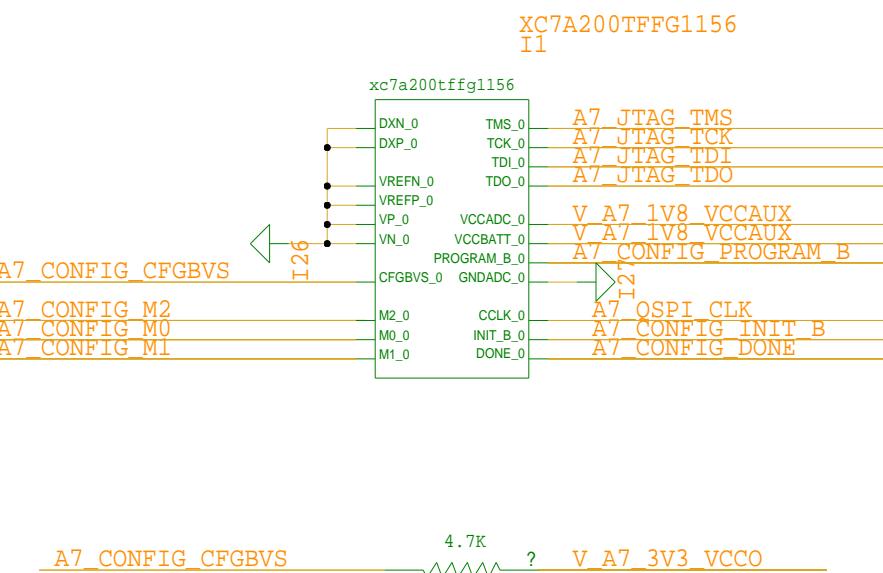
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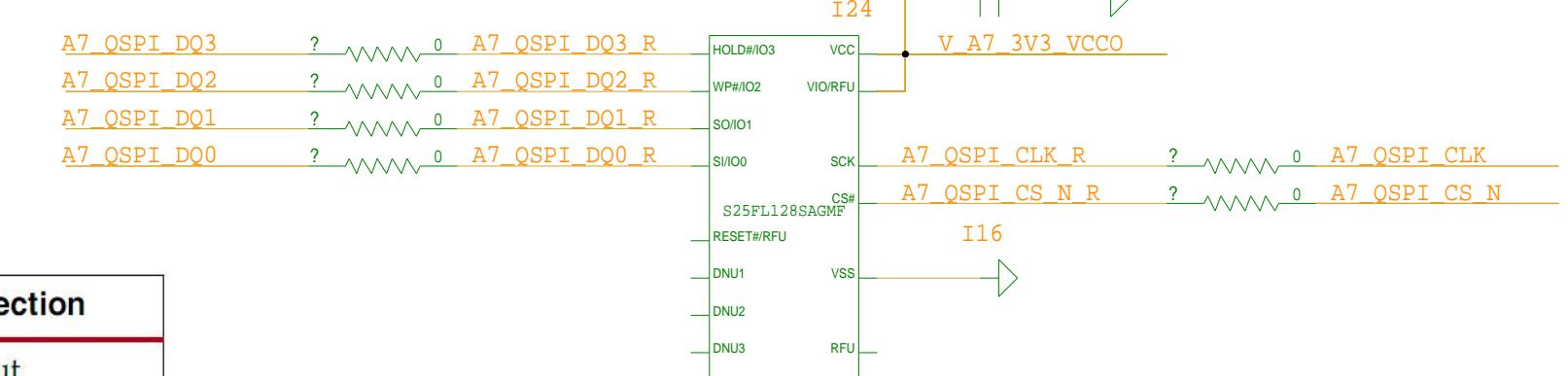
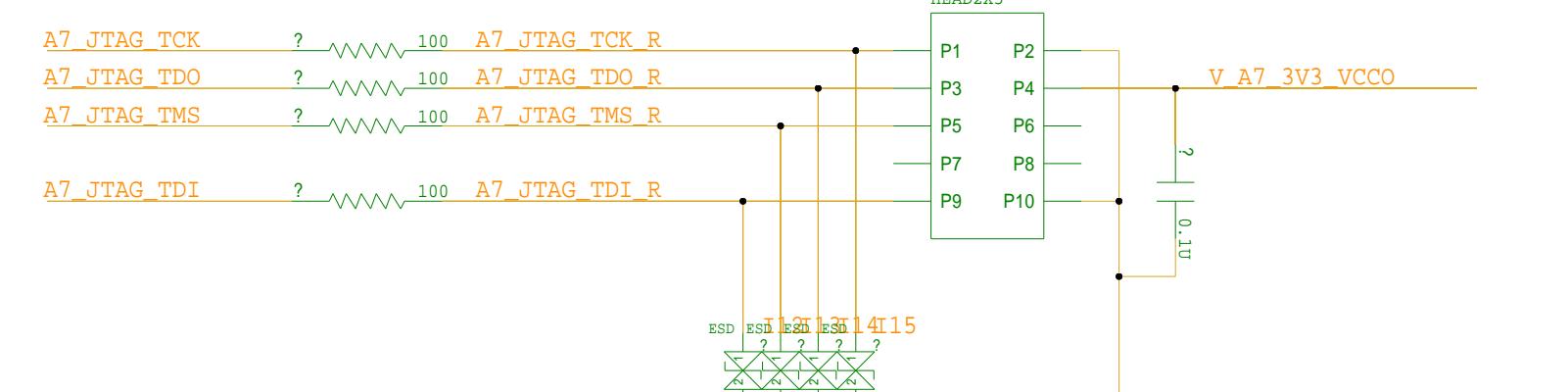
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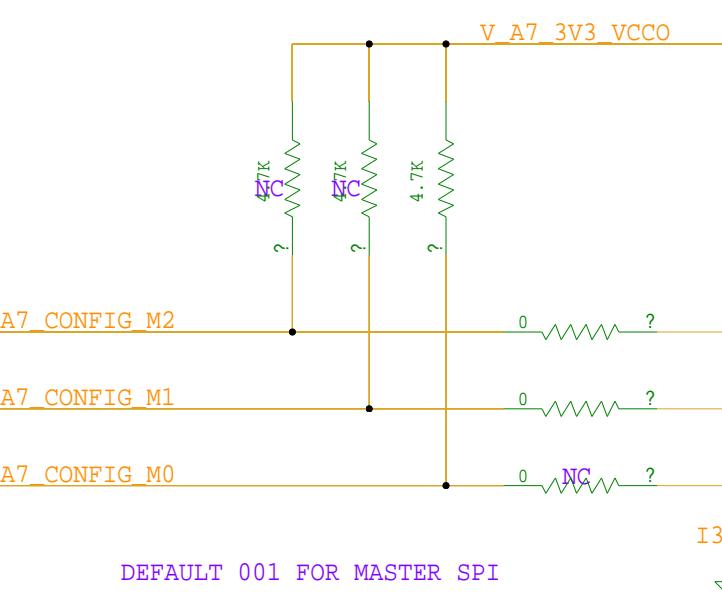
ARTIX-7 BANK0/14 CONFIG



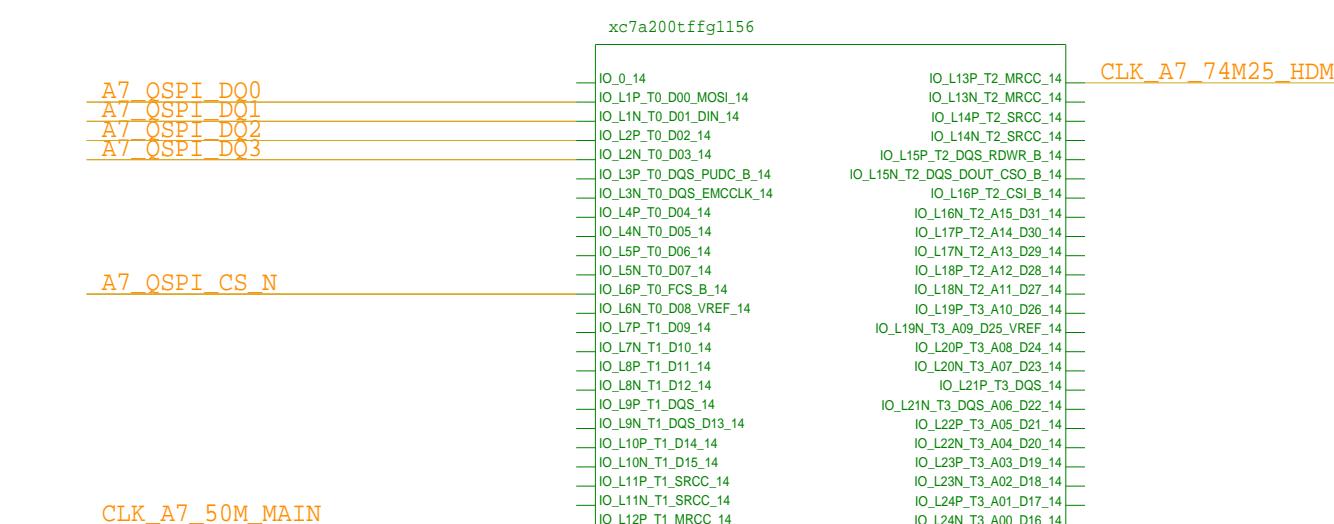
CFGBVS Pin Connection	Supported Configuration Banks 0/14/15 V _{cco} Supply and I/O Signal Voltages		
	Spartan-7, Artix-7, Kintex-7	Virtex-7 T, XT	Virtex-7 HT
Banks Affected	0, 14, 15	0	none
V _{cco} _0 (3.3V or 2.5V)	3.3V or 2.5V	3.3V or 2.5V	1.8V (no CFGBVS)
GND	1.8V or 1.5V	1.8V or 1.5V	



Configuration Mode	M[2:0]	Bus Width	CCLK Direction
Master Serial	000	x1	Output
Master SPI	001	x1, x2, x4	Output
Master BPI	010	x8, x16	Output
Master SelectMAP	100	x8, x16	Output
JTAG	101	x1	Not Applicable
Slave SelectMAP	110	x8, x16, x32 ⁽¹⁾	Input
Slave Serial ⁽²⁾	111	x1	Input



XC7A200TFFG1156
I25



LED INDICATE CONFIG DONE

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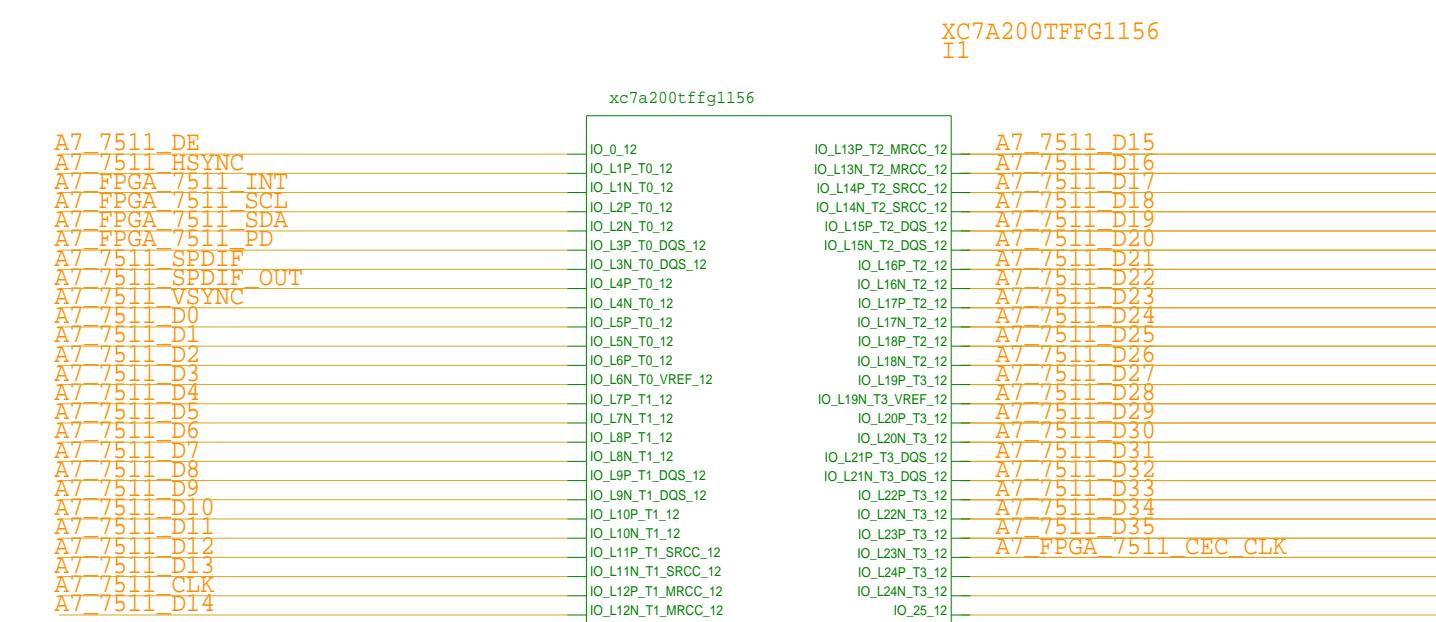
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ARTIX-7 BANK12

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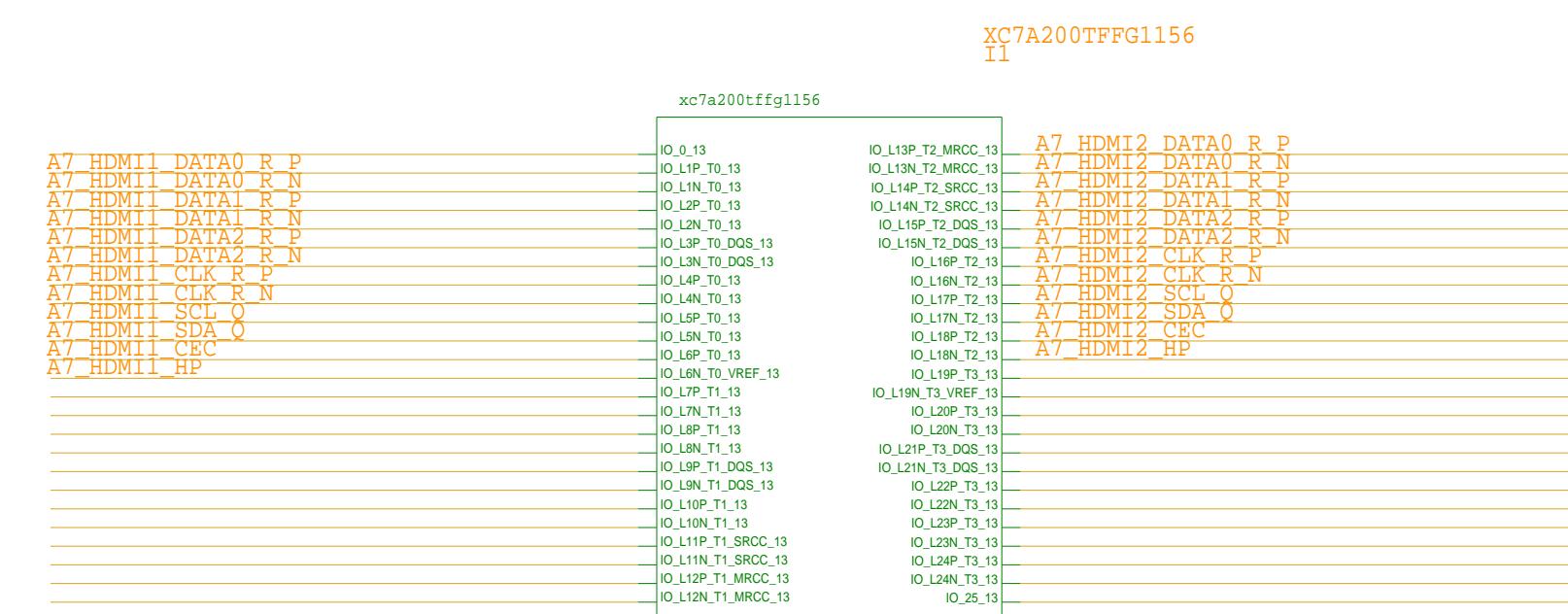


OD CONFIG AS BELOW:
A7_FPGA_7511_SCL
A7_FPGA_7511_SDA

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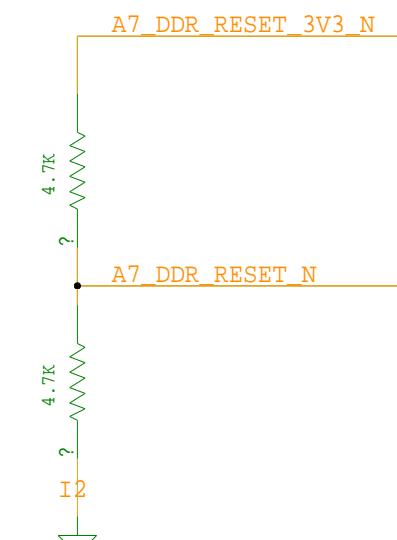
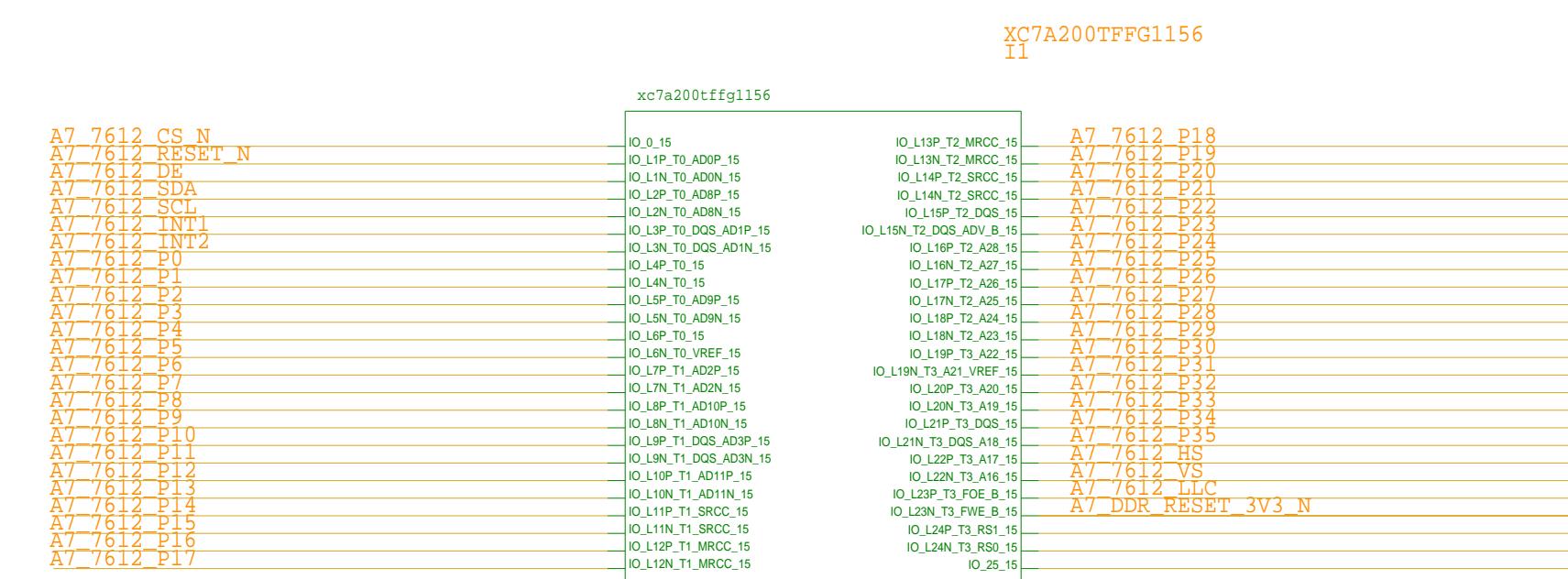
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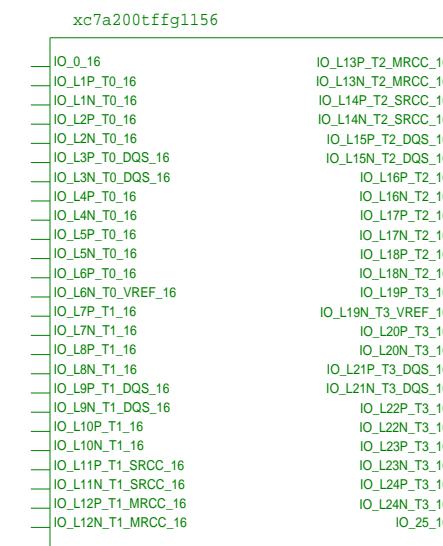
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NC_2	NC_27
NC_3	NC_28
NC_4	NC_29
NC_5	NC_30
NC_6	NC_31
NC_7	NC_32
NC_8	NC_33
NC_9	NC_34
NC_10	NC_35
NC_11	NC_36
NC_12	NC_37
NC_13	NC_38
NC_14	NC_39
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NC_17	NC_42
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NC_20	NC_45
NC_21	NC_46
NC_22	NC_47
NC_23	NC_48
NC_24	NC_49
NC_25	NC_50

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NC_52	NC_77
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IO_0_32	IO_L13P_T2_MRCC_32
IO_L1P_T0_32	IO_L13N_T2_MRCC_32
IO_L1N_T0_32	IO_L14P_T2_SRCC_32
IO_L2P_T0_32	IO_L14N_T2_SRCC_32
IO_L2N_T0_32	IO_L15P_T2_DOS_32
IO_L3P_T0_DQS_32	IO_L15N_T2_DQS_32
IO_L3N_T0_DQS_32	IO_L16P_T2_32
IO_L4P_T0_32	IO_L16N_T2_32
IO_L4N_T0_32	IO_L17P_T2_32
IO_L5P_T0_32	IO_L17N_T2_32
IO_L5N_T0_32	IO_L18P_T2_32
IO_L6P_T0_32	IO_L18N_T2_32
IO_L6N_T0_VREF_32	IO_L19P_T2_32
IO_L7P_T1_32	IO_L19N_T3_VREF_32
IO_L7N_T1_32	IO_L20P_T3_32
IO_L8P_T1_32	IO_L20N_T3_32
IO_L8N_T1_32	IO_L21P_T3_DQS_32
IO_L9P_T1_DQS_32	IO_L21N_T3_DQS_32
IO_L9N_T1_DQS_32	IO_L22P_T3_32
IO_L10P_T1_32	IO_L22N_T3_32
IO_L10N_T1_32	IO_L23P_T3_32
IO_L11P_T1_SRCC_32	IO_L23N_T3_32
IO_L11N_T1_SRCC_32	IO_L24P_T3_32
IO_L12P_T1_MRCC_32	IO_L24N_T3_32
IO_L12N_T1_MRCC_32	IO_25_32

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IO_0_33	IO_L13P_T2_MRCC_33
IO_L1P_T0_33	IO_L13N_T2_MRCC_33
IO_L1N_T0_33	IO_L14P_T2_SRCC_33
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IO_L4P_T0_33	IO_L16N_T2_33
IO_L4N_T0_33	IO_L17P_T2_33
IO_L5P_T0_33	IO_L17N_T2_33
IO_L5N_T0_33	IO_L18P_T2_33
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IO_L7P_T1_33	IO_L19N_T3_VREF_33
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IO_L8N_T1_33	IO_L21P_T3_DQS_33
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IO_L12N_T1_MRCC_33	IO_25_33

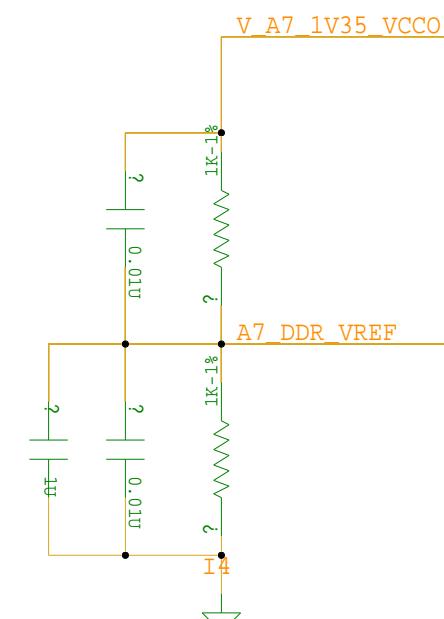
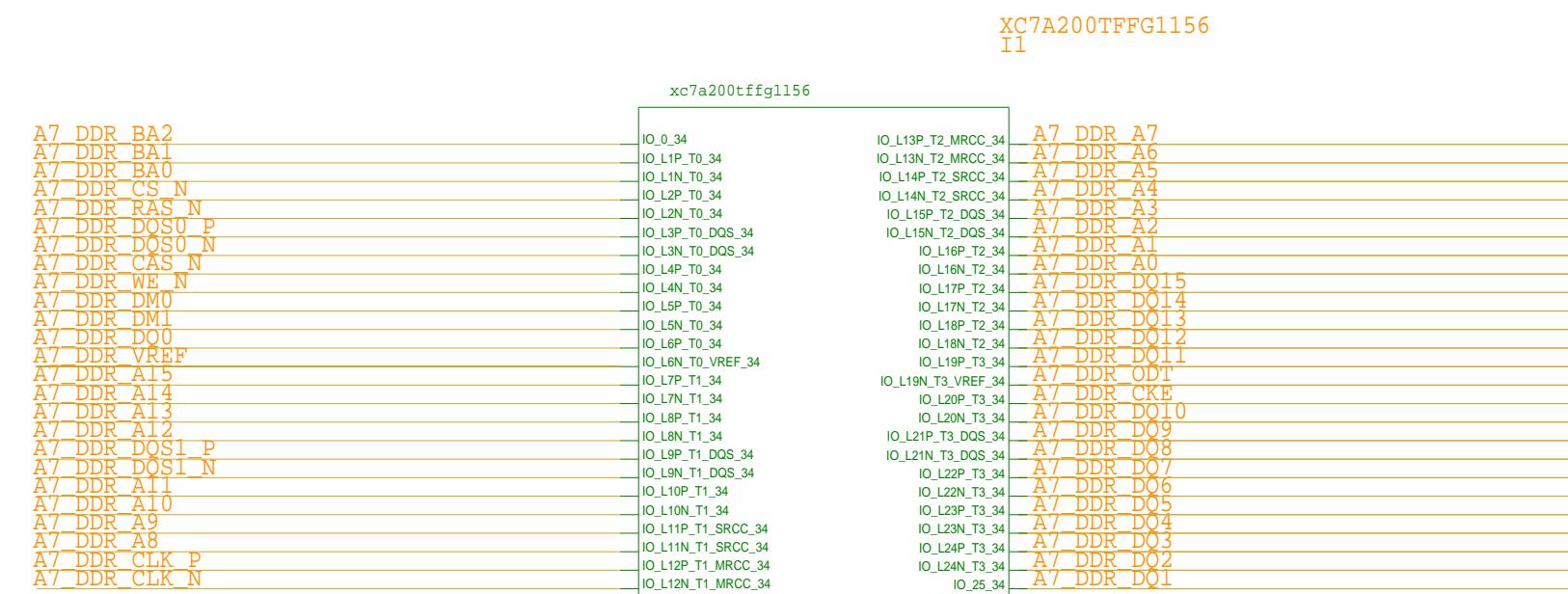
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IO_0_35	IO_L13P_T2_MRCC_35
IO_L1P_T0_AD4P_35	IO_L13N_T2_MRCC_35
IO_L1N_T0_ADN_35	IO_L14P_T2_SRCC_35
IO_L2P_T0_AD12P_35	IO_L14N_T2_SRCC_35
IO_L2N_T0_AD12N_35	IO_L16P_T2_DOS_35
IO_L3P_T0_DOS_ADS5_35	IO_L18P_T2_DOS_35
IO_L4N_T0_DOS_ADS5N_35	IO_L18P_T2_DOS_35
IO_L5P_T0_DOS_35	IO_L18N_T2_35
IO_L6P_T0_35	IO_L17P_T2_35
IO_L7N_T0_35	IO_L17N_T2_35
IO_L8P_T0_ADI3P_35	IO_L18P_T2_35
IO_L9N_T0_ADI3N_35	IO_L18P_T2_35
IO_L6P_T0_35	IO_L18N_T2_35
IO_L6N_T0_VREF_35	IO_L19P_T3_35
IO_L7P_T1_ADP5_35	IO_L19N_T3_VREF_35
IO_L7N_T1_ADN_35	IO_L20P_T3_35
IO_L8P_T1_ADI4P_35	IO_L20N_T3_35
IO_L9N_T1_ADI4N_35	IO_L21P_T3_DOS_35
IO_L9P_T1_DOS_ADP7_35	IO_L21N_T3_DOS_35
IO_L9N_T1_MRCC_35	IO_L22P_T3_35
IO_L10P_T1_ADP5_35	IO_L22N_T3_35
IO_L10N_T1_ADN_35	IO_L23P_T3_35
IO_L11P_T1_SRCC_35	IO_L23N_T3_35
IO_L12P_T1_MRCC_35	IO_L24P_T3_35
IO_L12N_T1_MRCC_35	IO_L24N_T3_35
	IO_25_35

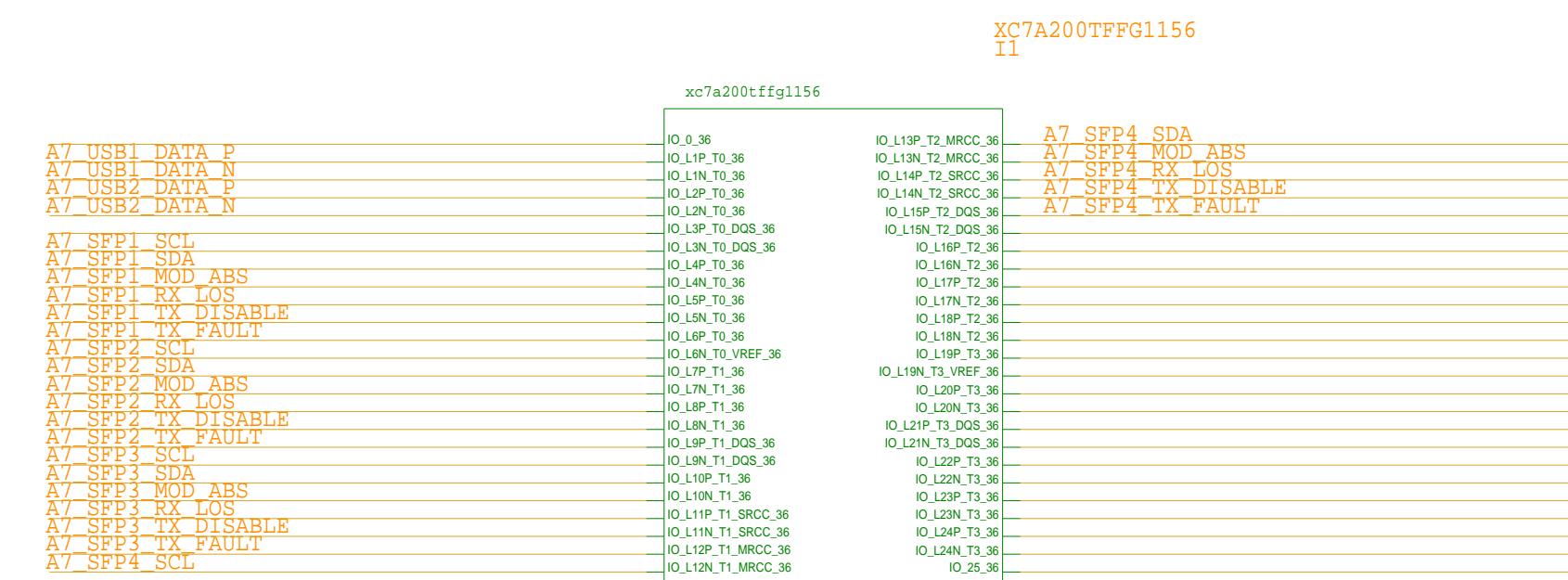
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ARTIX-7 BANK36

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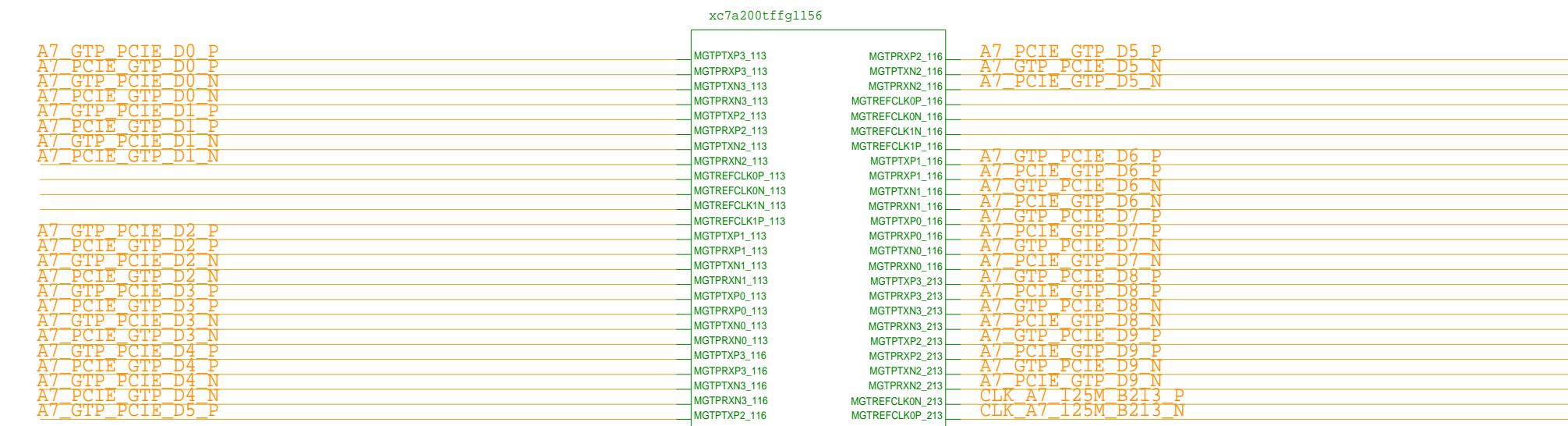

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ARTIX-7 GTP (1)

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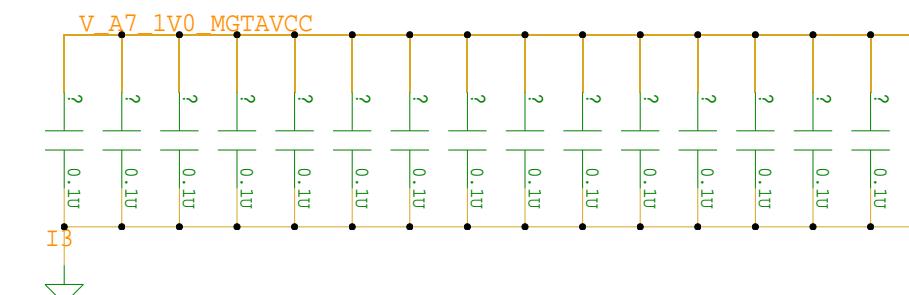
ARTIX-7 GTP (2)

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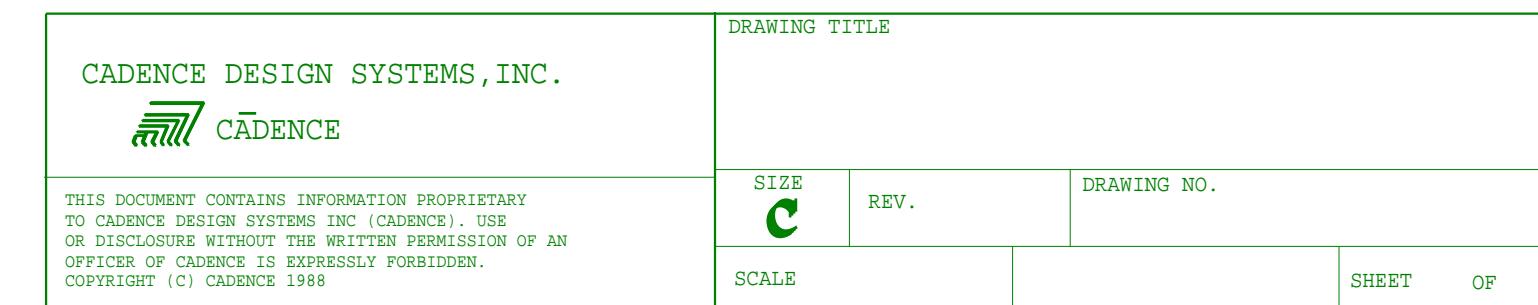
The diagram illustrates the connection between two sets of pins in the xc7a200tffg1156 FPGA. It shows the mapping from A7 BANK 213 MGTRREF pins to A7 BANK 216 MGTRREF pins.

A7 BANK 213 MGTRREF Pin	A7 BANK 216 MGTRREF Pin
MGTRREF_213	MGTRREF_216
MGTREFCLK1_213	MGTREFCLK1_216
MGTREFCLKIN_213	MGTREFCLKIN_216
MGTPTXP1_213	MGTPXP1_216
MGTPRXP1_213	MGTPRXP1_216
MGTPTXN1_213	MGTPTXN1_216
MGTPRXN1_213	MGTPRXN1_216
MGTPRXN1_213	MGTPRXN1_216
MGTPTXP0_213	MGTPXP0_216
MGTPRXP0_213	MGTPRXP0_216
MGTPTXN0_213	MGTPRXN0_216
MGTPRXN0_213	MGTPRXN0_216
MGTPTXP3_216	MGTPRN0_216
MGTPRXP3_216	MGTAVCC_G10_1
MGTPRXN3_216	MGTAVCC_G10_2
MGTPRXN3_216	MGTAVCC_G10_3
MGTPTXP2_216	MGTAVCC_G10_4
MGTPRXP2_216	MGTAVCC_G10_5
MGTPTXN2_216	MGTAVCC_G10_6
MGTPRXN2_216	MGTAVCC_G10_7
MGTREFCLKON_216	MGTAVCC_G10_8



A7 BANK 216 MGTRREF ? ~~~~~ 100 V A7 1V2 MGTAVTT

A7 BANK 213 MGTRREF ? ^^^^ 100 V A7 1V2 MGTAVTT



ZYNQ-7 INDEX

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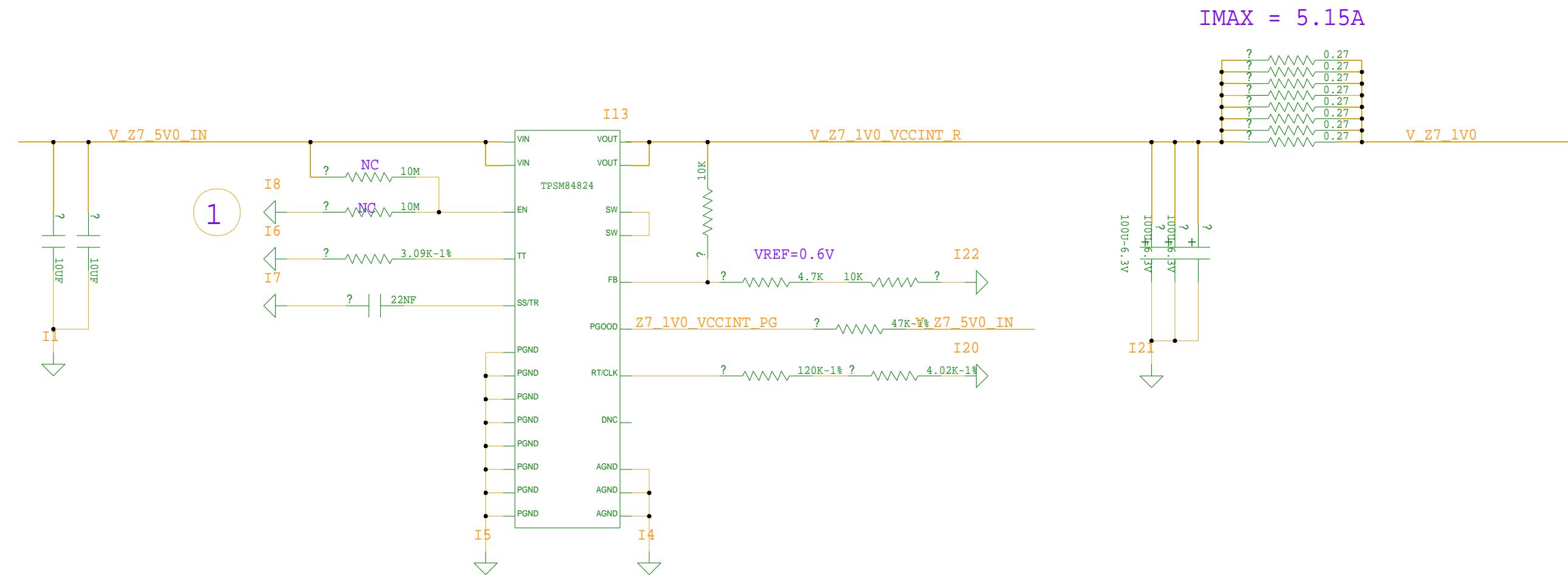
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ZYNQ-7 POWER (1)



SS/TR	6	I	Soft-start and tracking pin. Connecting an external capacitor to this pin adjusts the output voltage soft-start ramp slower than its 1.2 ms default setting. A voltage applied to this pin allows for tracking and sequencing control.
-------	---	---	--

Table 9. Soft-Start Capacitor Values and Soft-Start Time

C _{ss} (nF)	open	10	15	22	47
SS Time (ms)	1.2	2.4	3	3.8	6.8

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ZYNQ-7 POWER (2)

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$$V_{OUT} = V_{REF} \times (1 + (R_{TOP}/R_{BOT}))$$

$$R_{RT} (\text{k}\Omega) = [14,822/f_{SW} (\text{kHz})]^{1.081}$$

$$V_{IN_STARTUP} = (0.8 \text{ nA} + (0.8 \text{ V}/R_{BOT_EN})) \times \left(R_{TOP_EN} + \frac{R_{BOT_EN} \times 1 \text{ M}\Omega}{R_{BOT_EN} + 1 \text{ M}\Omega} \right)$$

where:

R_{TOP_EN} is the resistor from V_{IN} to EN.

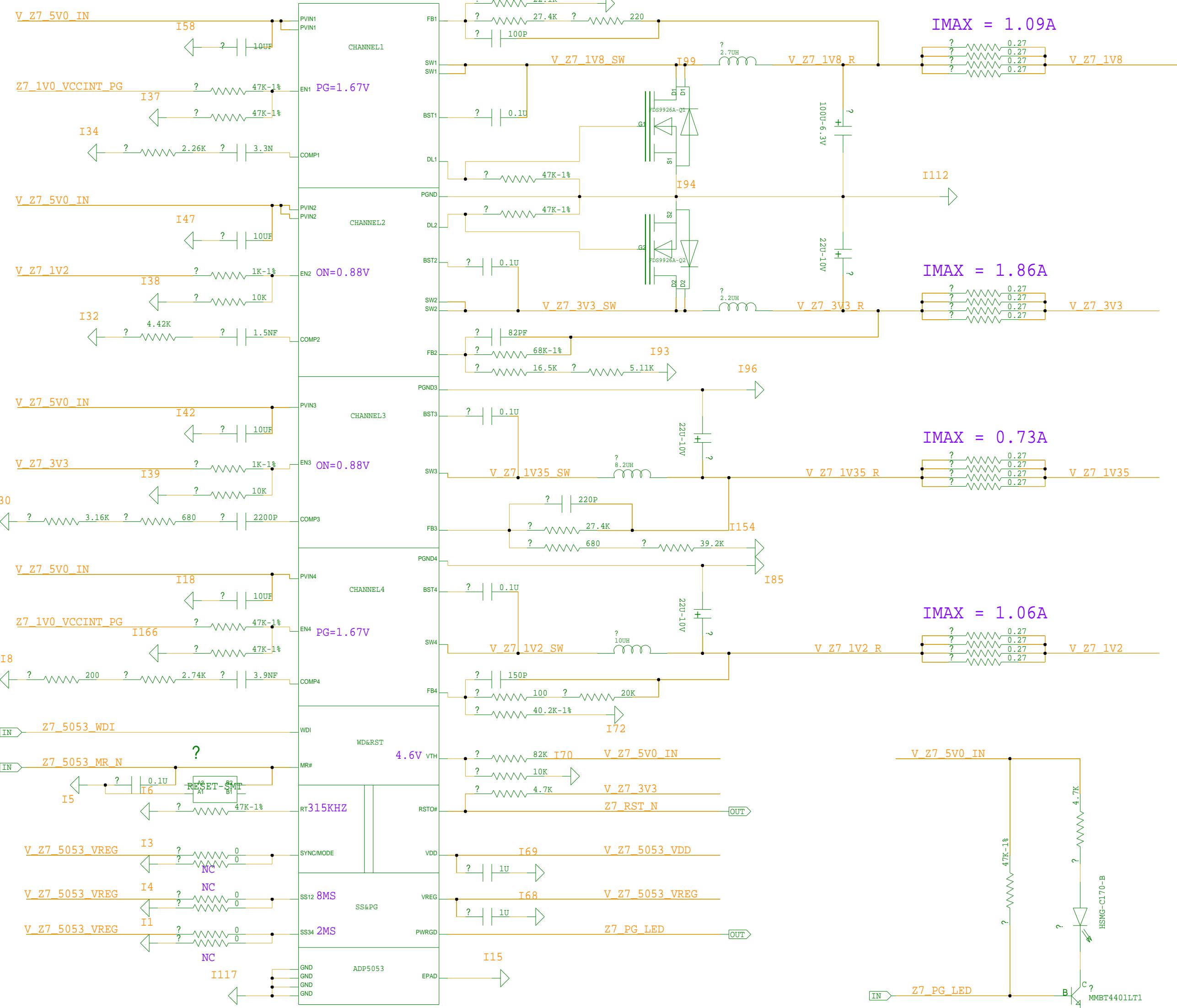
R_{BOT_EN} is the resistor from EN to ground.

Table 9. Soft Start Time Set by the SS12 and SS34 Pins

		Soft Start Time			
R_{TOP} ($\text{k}\Omega$)	R_{BOT} ($\text{k}\Omega$)	Channel 1	Channel 2	Channel 3	Channel 4
0	N/A ¹	2 ms	2 ms	2 ms	2 ms
100	600	2 ms	Parallel	2 ms	4 ms
200	500	2 ms	8 ms	2 ms	8 ms
300	400	4 ms	2 ms	4 ms	2 ms
400	300	4 ms	4 ms	4 ms	4 ms
500	200	8 ms	2 ms	4 ms	8 ms
600	100	8 ms	Parallel	8 ms	2 ms
N/A ¹	0	8 ms	8 ms	8 ms	8 ms

Table 16. Factory Default Options

Option	Default Value
Channel 1 Output Voltage	0.8V adjustable output
Channel 2 Output Voltage	0.8V adjustable output
Channel 3 Output Voltage	0.8V adjustable output
Channel 4 Output Voltage	0.8V adjustable output
PWRGD Pin (Pin 20) Output	Monitor Channel 1 output
Output Discharge Function	Enabled for all four buck regulators
Switching Frequency on Channel 1	1x switching frequency set by the RT pin
Switching Frequency on Channel 3	1x switching frequency set by the RT pin
SYNC/MODE Pin (Pin 43) Function	Forced PWM/automatic PWM/PSM mode setting with the ability to synchronize to an external clock
Hiccup Protection	Enabled for overcurrent events
Short-Circuit Latch-Off Function	Disabled for output short-circuit events
Oversupply Latch-Off Function	Disabled for output oversupply events
Reset Timeout Period	200 ms
Watchdog Timeout Period	1.6 sec
Manual Reset Input Mode	Processor manual reset mode



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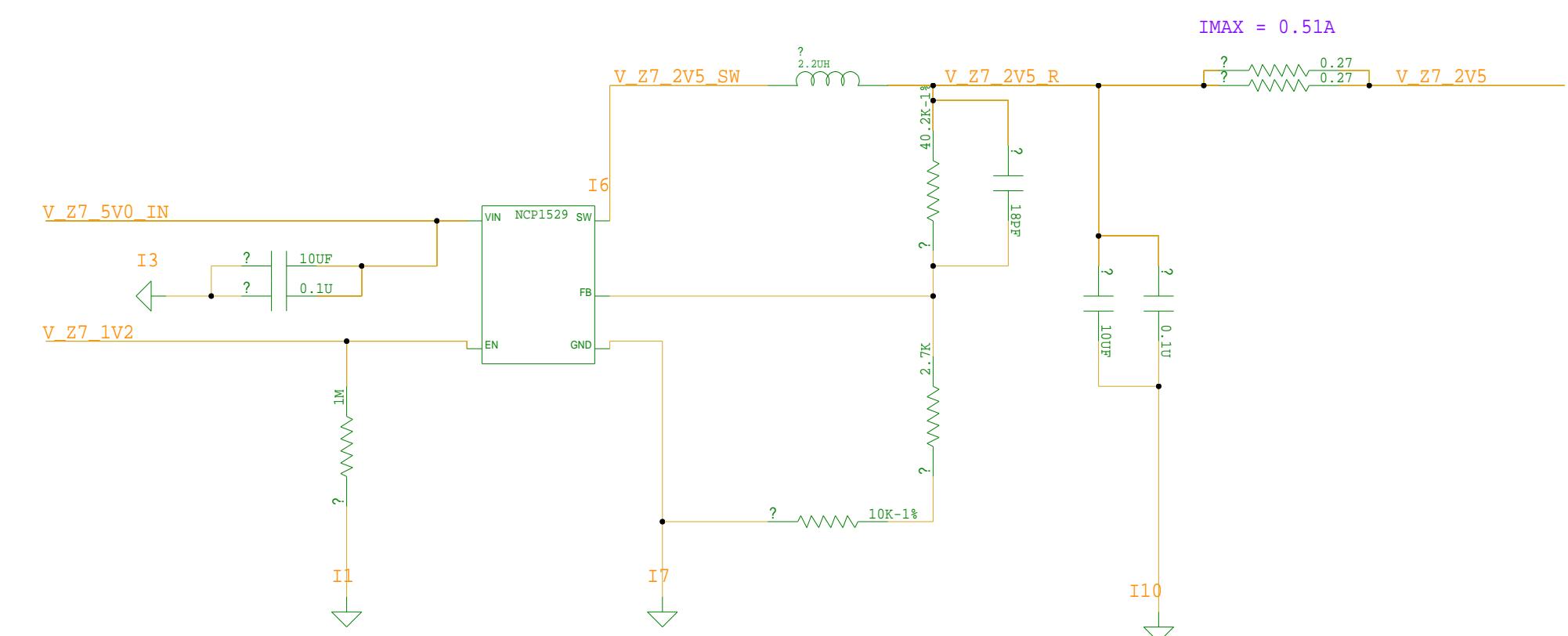
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ZYNQ-7 POWER (3)

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- $V_{out} = V_{FB} \times (1 + R1/R2)$
- V_{OUT} : Output Voltage (V)
 - V_{FB} : Feedback Voltage = 0.6 V
 - $R1$: Feedback Resistor from V_{OUT} to FB
 - $R2$: Feedback Resistor from FB to GND

3

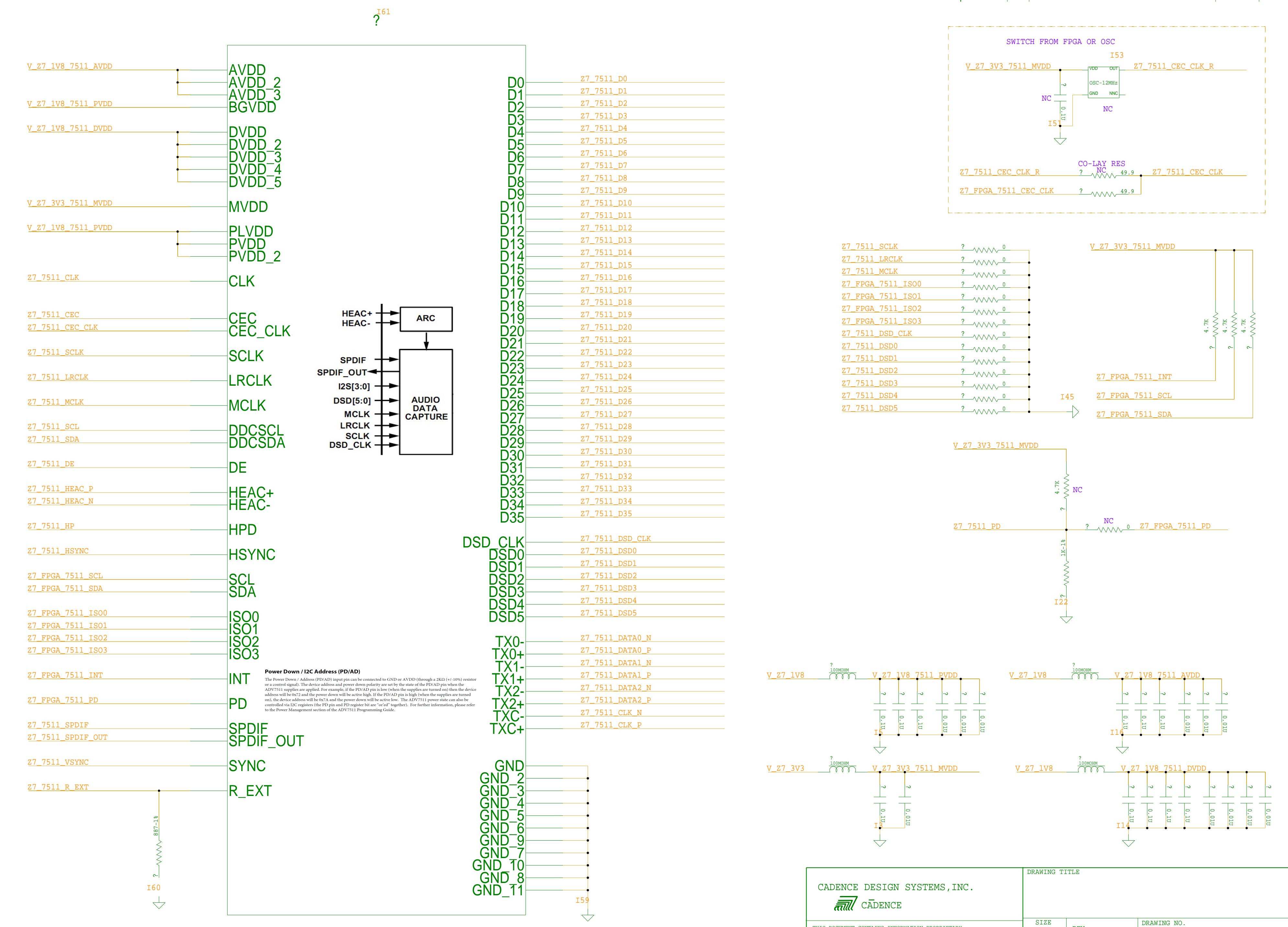


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ZYNQ-7 PL HDMI TRANSMITTER (1)



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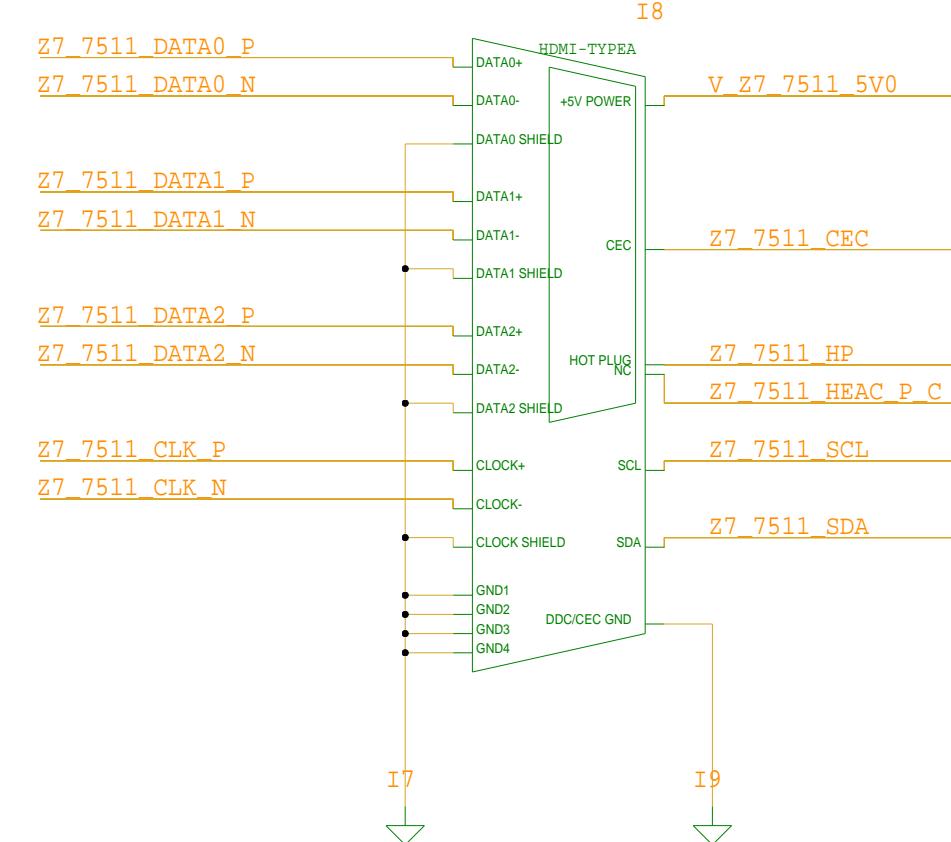
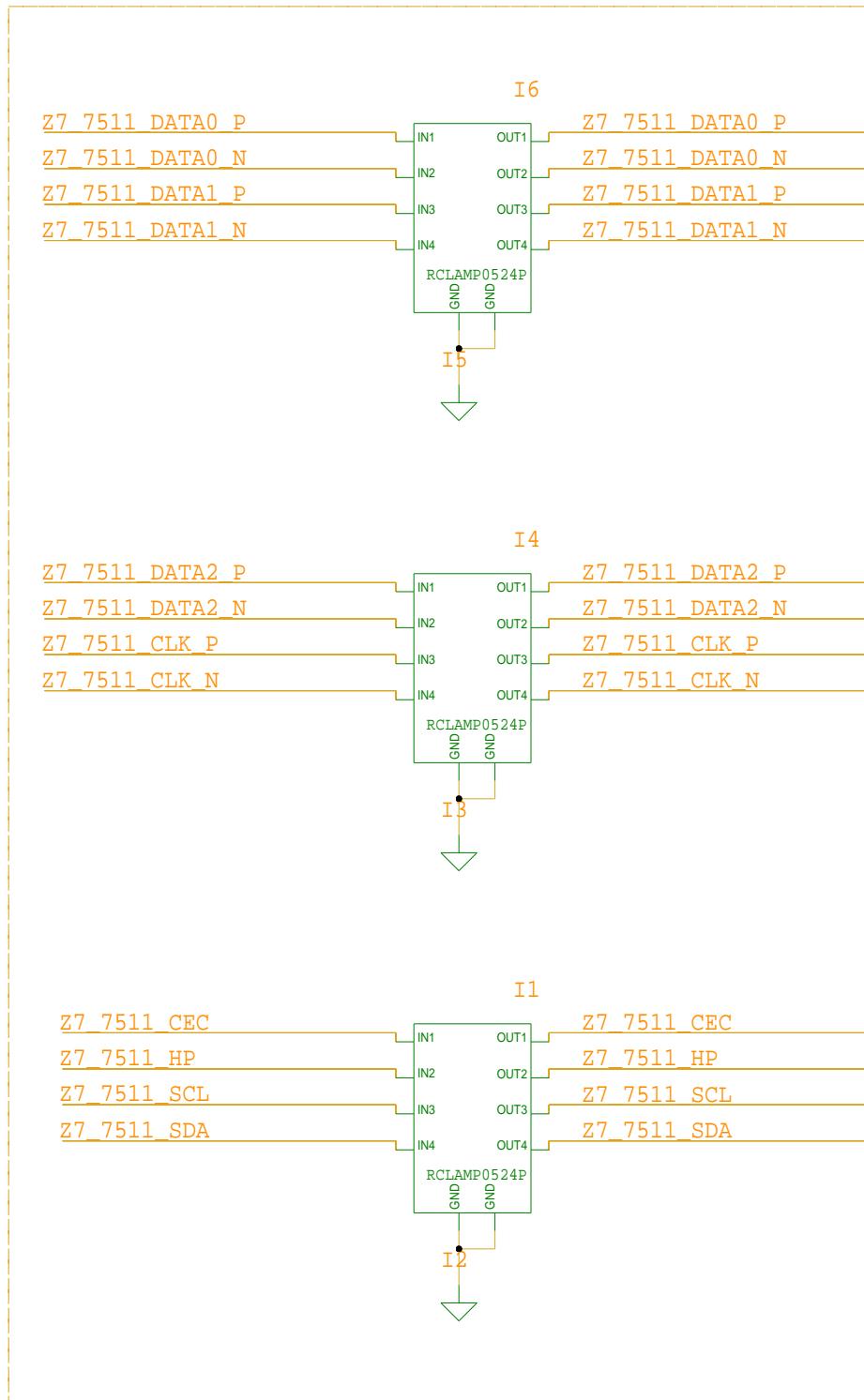
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ZYNQ-7 PL HDMI TRANSMITTER (2)

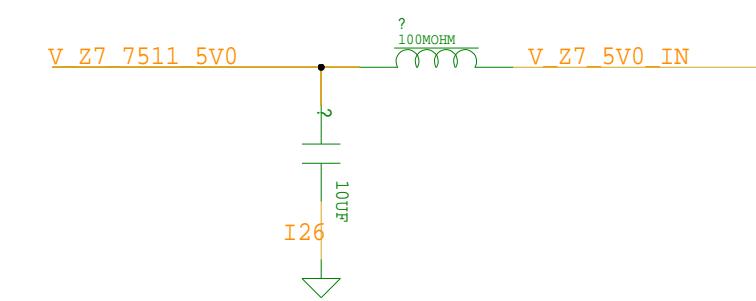
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CHANGE CONNECTION DUE TO LAYOUT

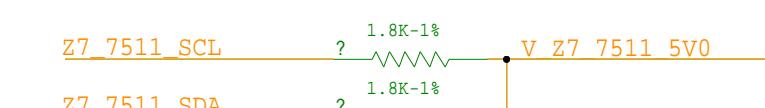
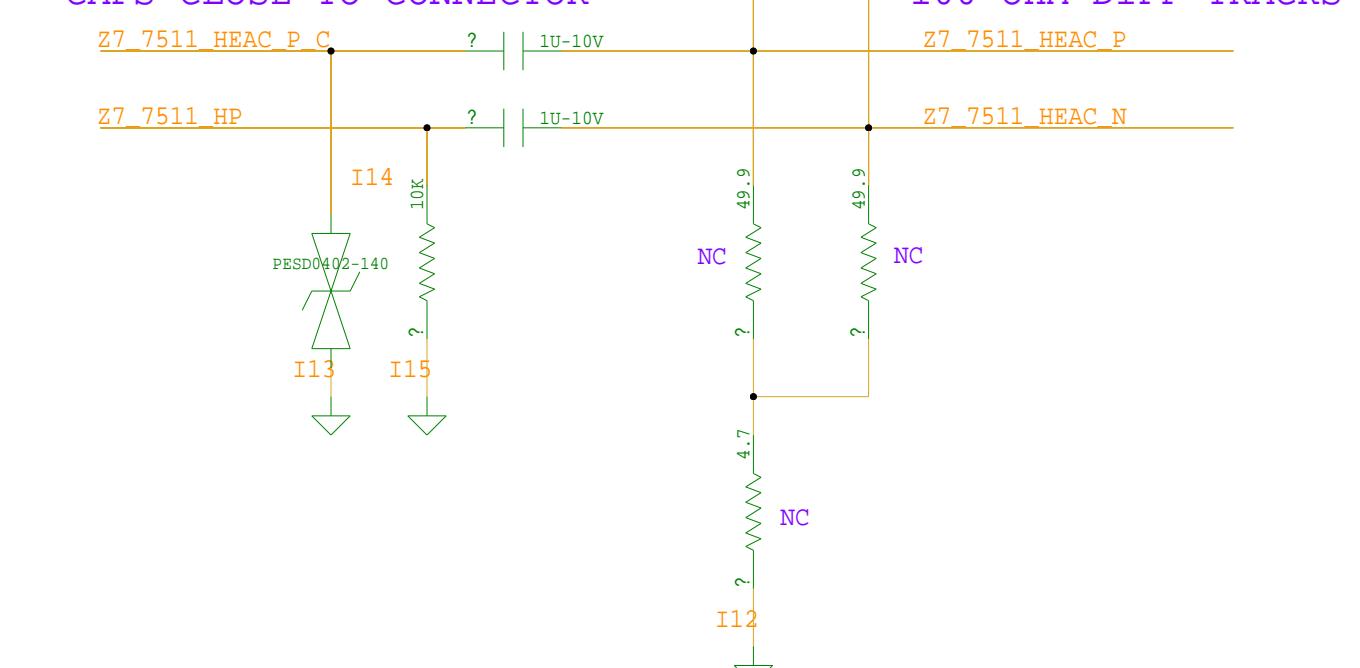


CLOSE TO HDMI CONNECTOR



Z7_7511_CEC → ? IN4148 → ? 27.4K → V_Z7_3V3_7511_MVDD

CAPS CLOSE TO CONNECTOR



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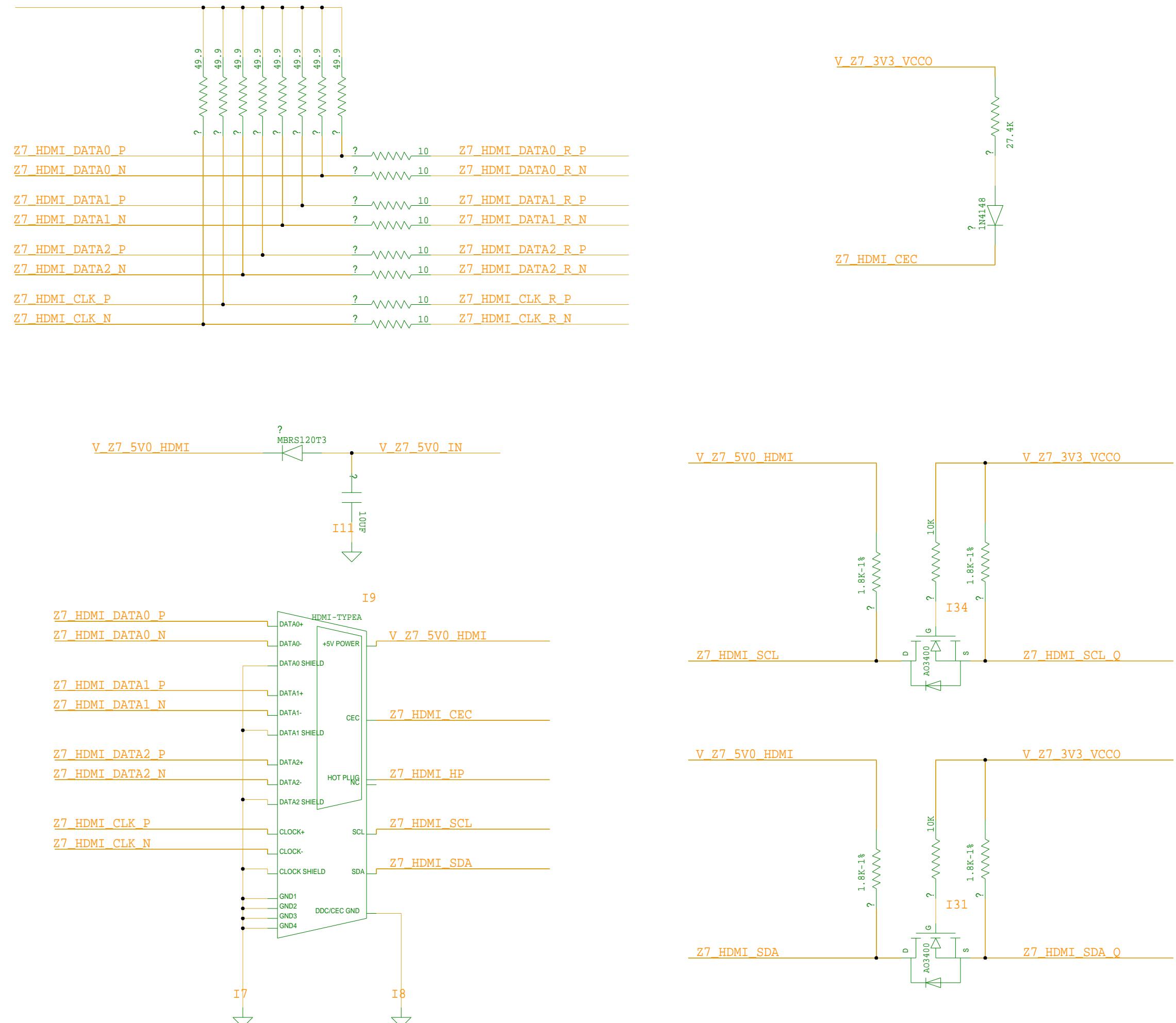
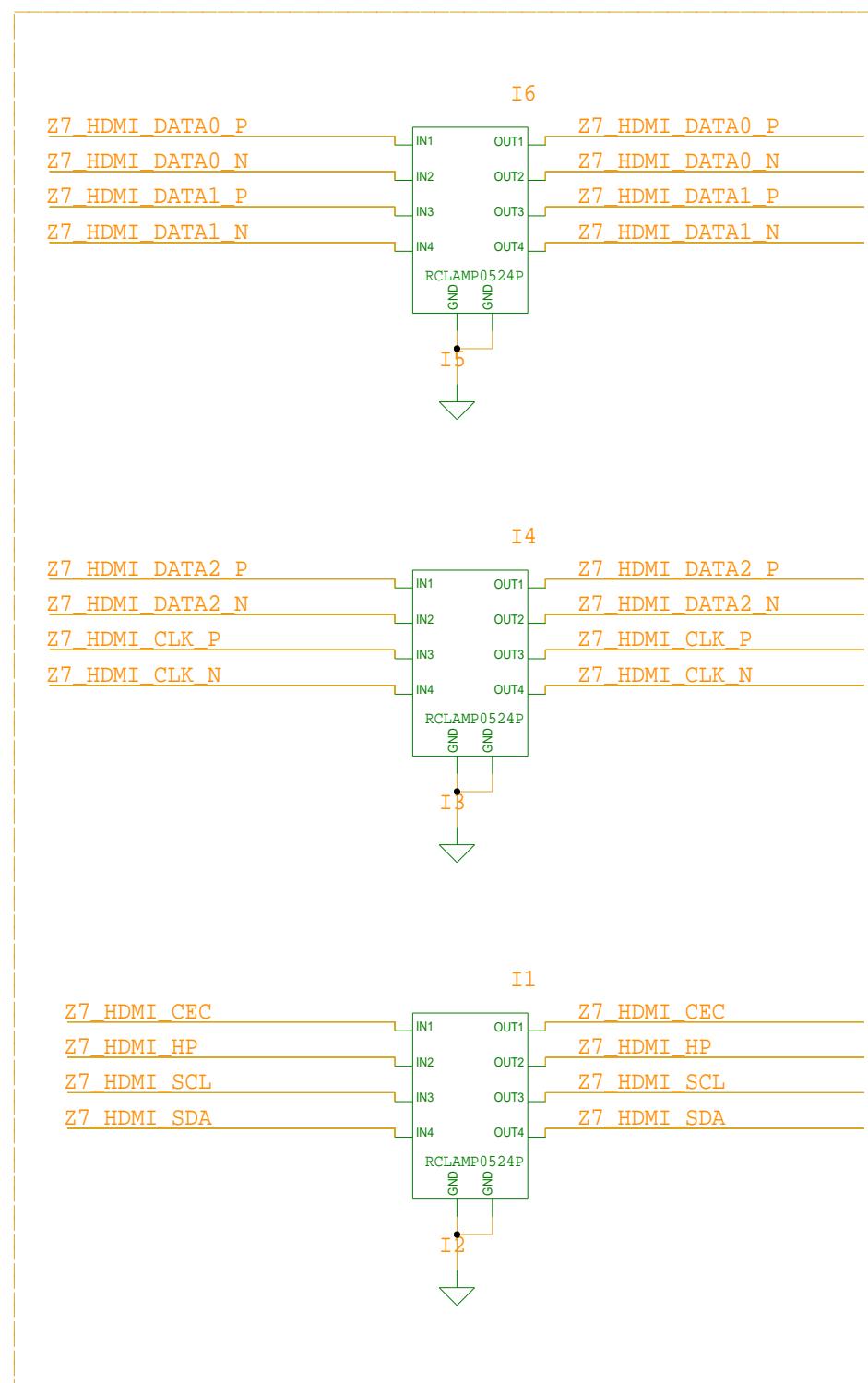
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ZYNQ-7 PL HDMI INOUT

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CHANGE CONNECTION DUE TO LAYOUT



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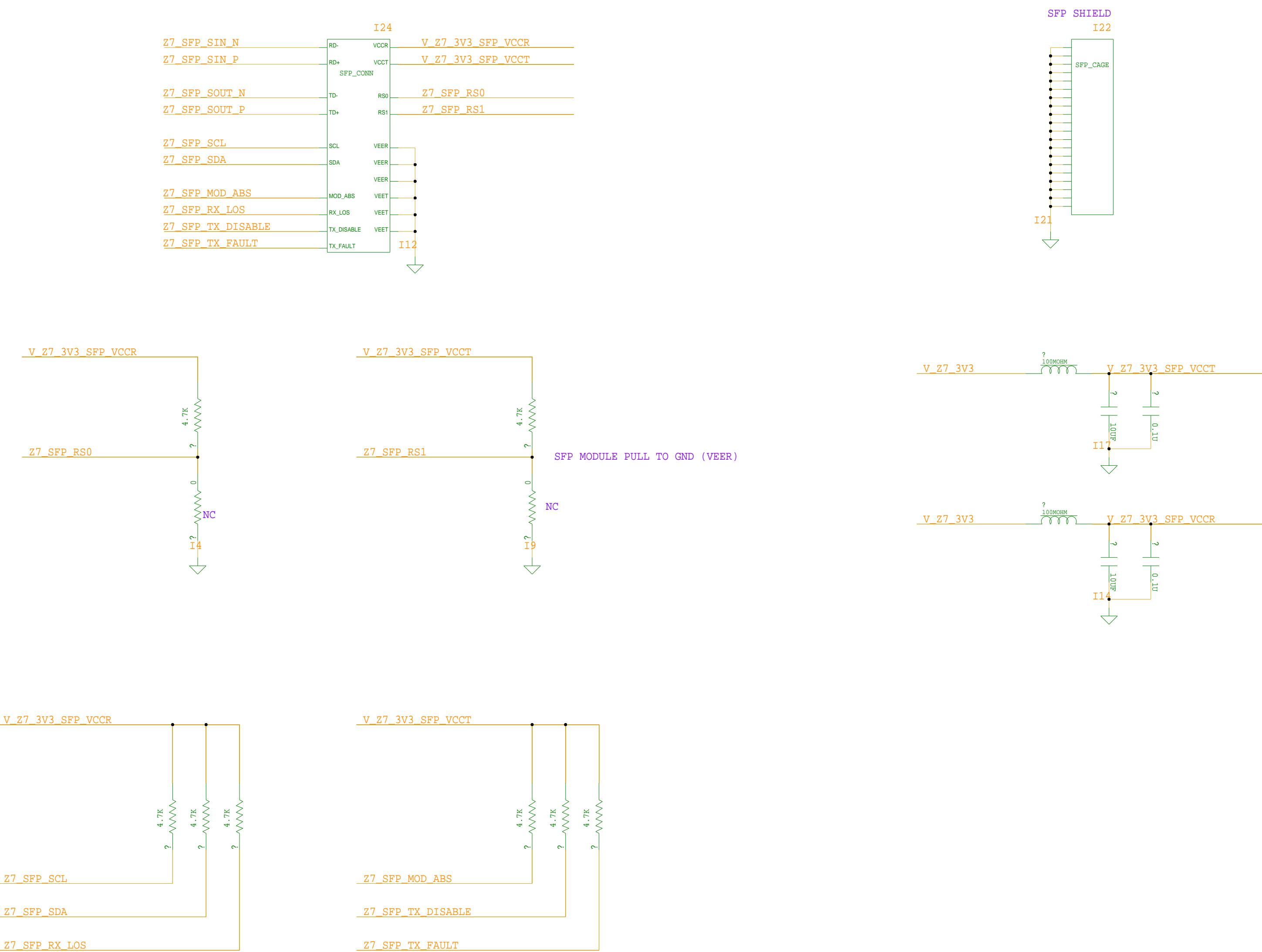
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ZYNQ-7 PL SFP+/SFP INOUT

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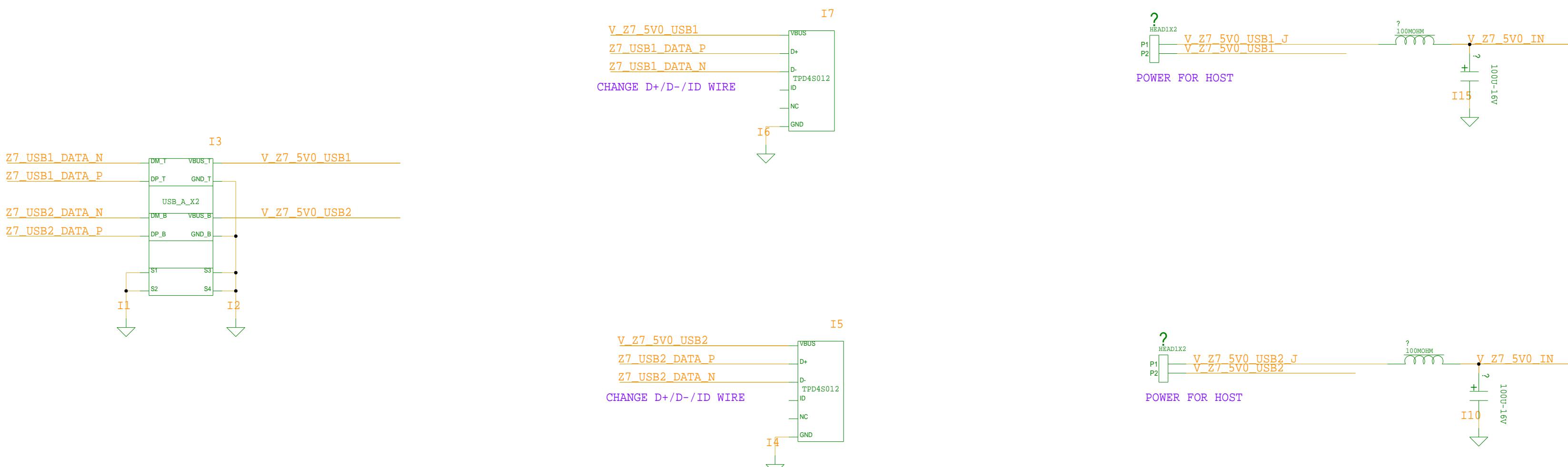
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ZYNQ-7 PL USB INOUT

REVISIONS

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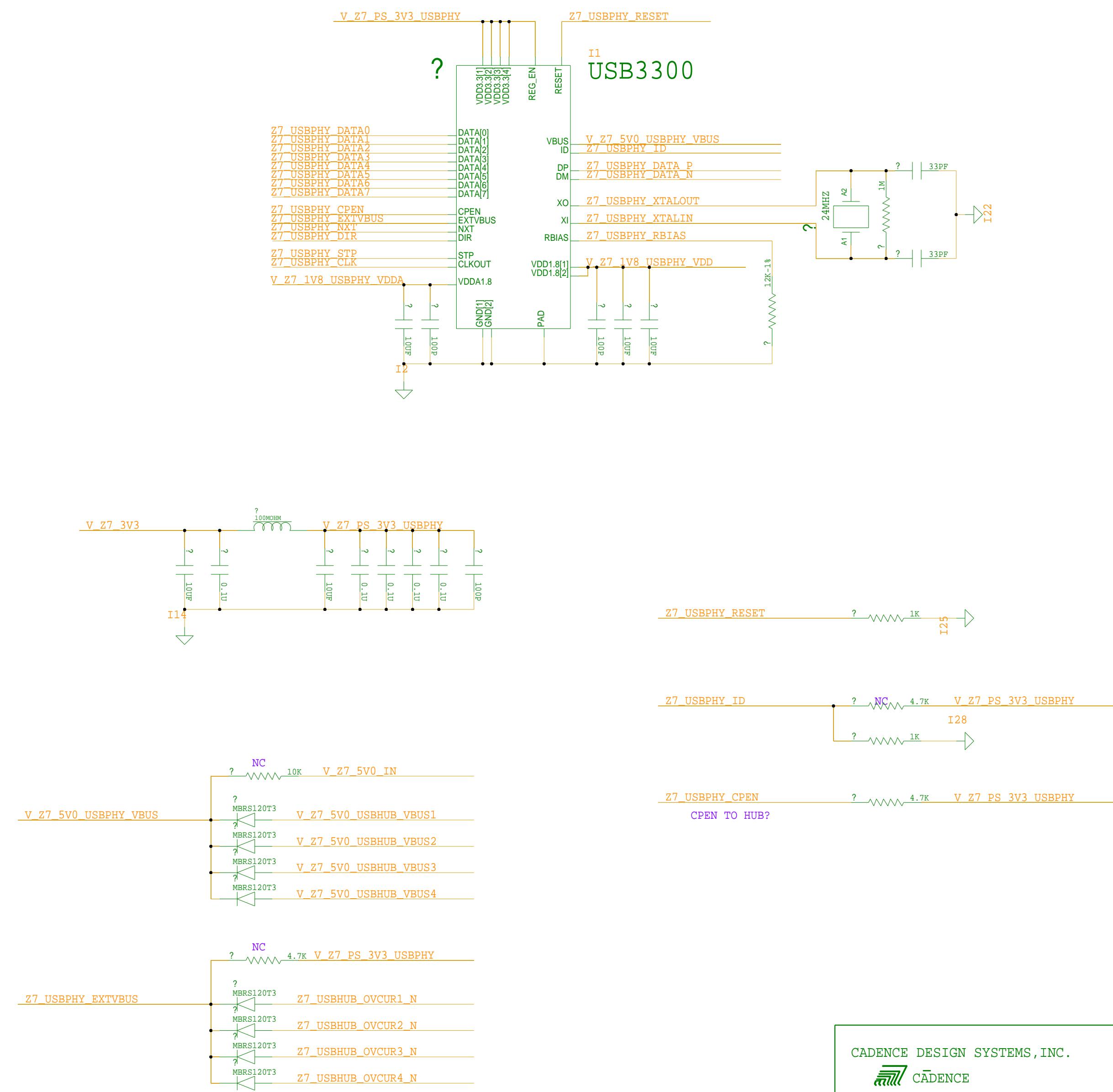
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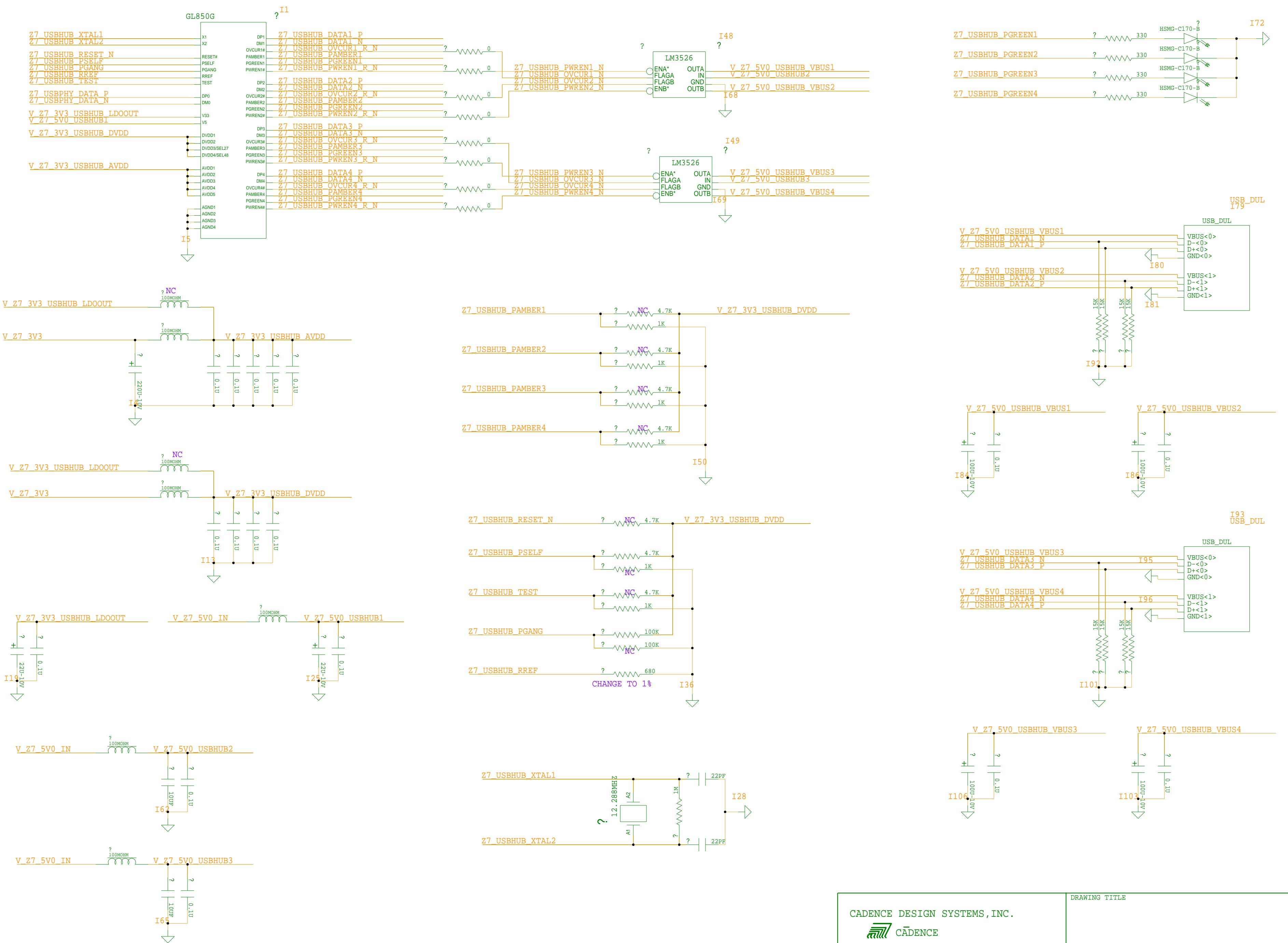
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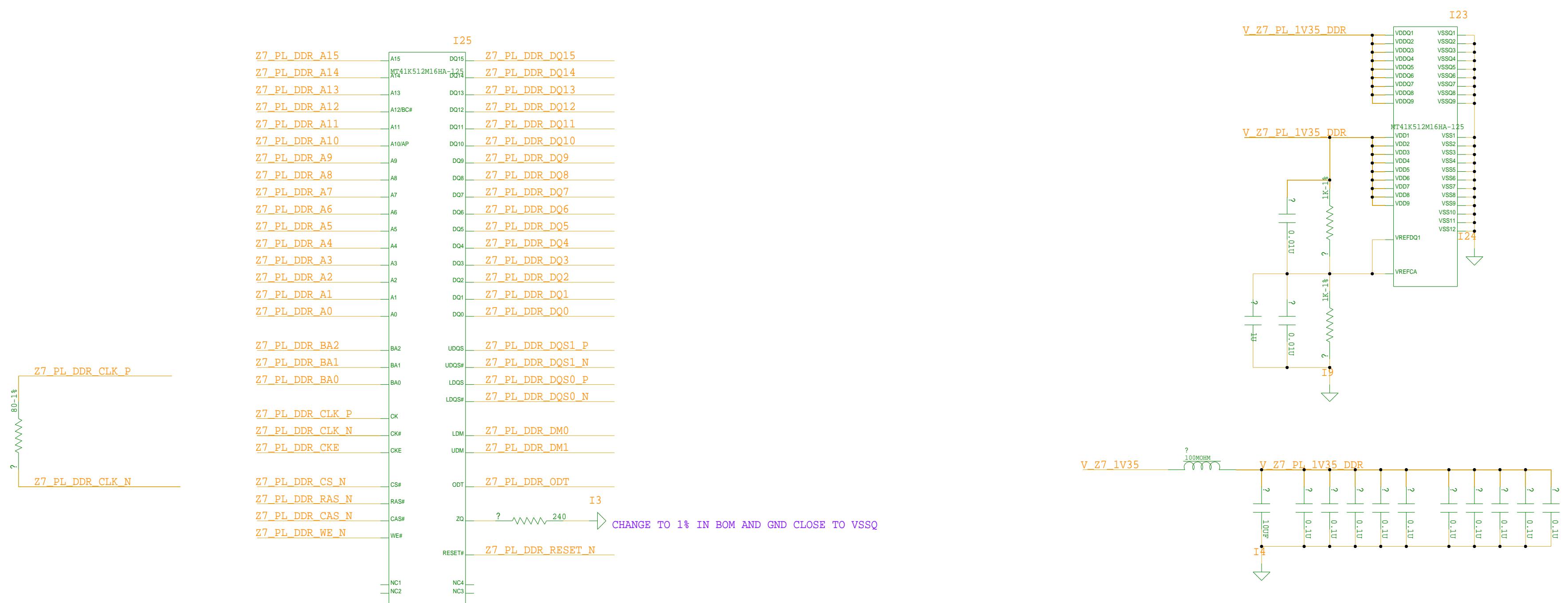
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ZYNQ-7 PL DDR3

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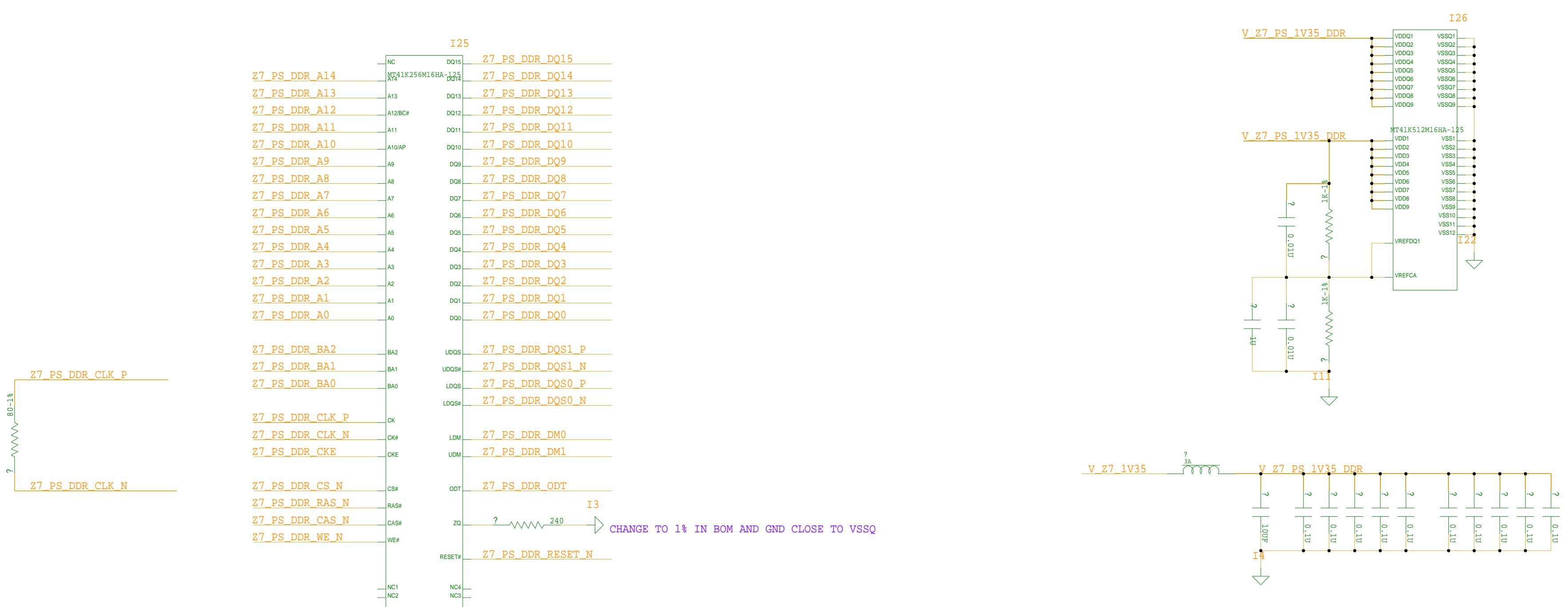
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ZYNQ-7 PS DDR3 (1)

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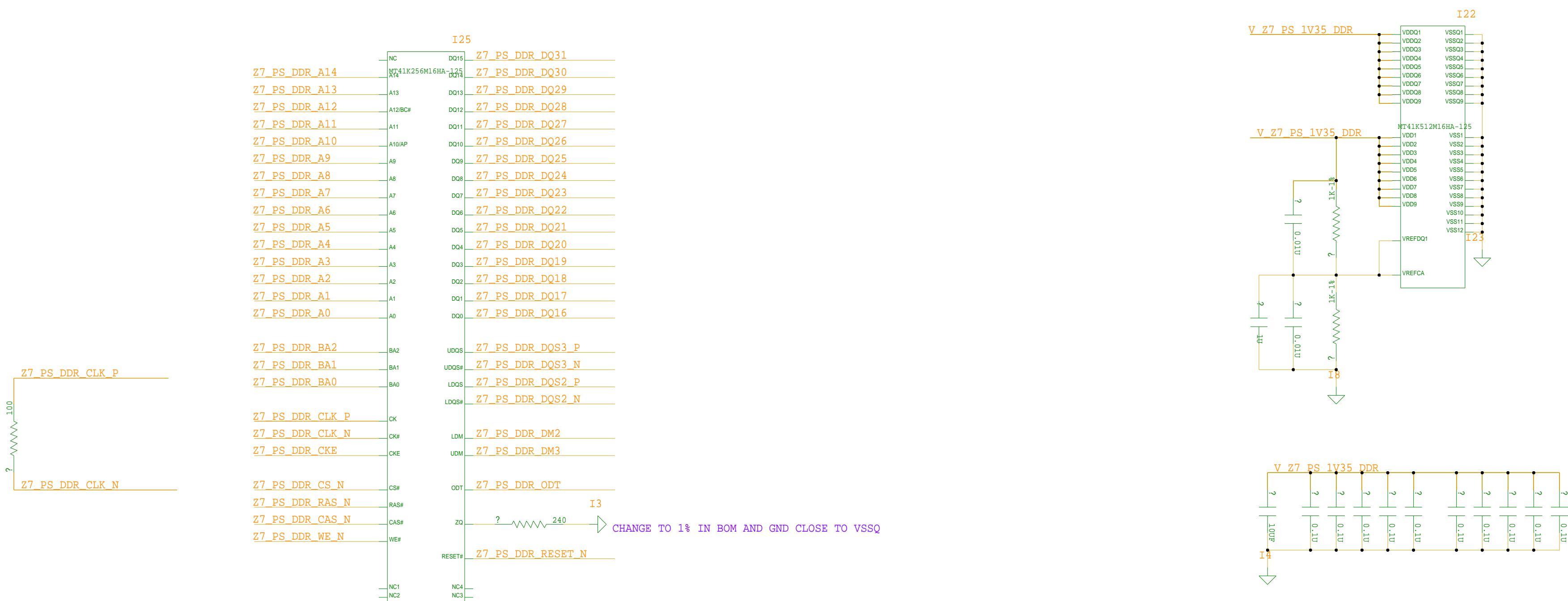
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ZONE	LTR				



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The diagram illustrates the Z7 PS EMMC interface connections. On the left, seven data lines are labeled: Z7_PS_EMMC_DATA0, Z7_PS_EMMC_DATA1, Z7_PS_EMMC_DATA2, Z7_PS_EMMC_DATA3, Z7_PS_EMMC_DATA4, Z7_PS_EMMC_DATA5, Z7_PS_EMMC_DATA6, and Z7_PS_EMMC_DATA7. These lines connect to a green-bordered box representing the Z7 chip. Inside the box, the lines are mapped to internal pins: DAT0 (mtfc8gacaaaam-1n), DAT1, DAT2, DAT3, DAT4, DAT5, DAT6, and DAT7. The DAT1 pin is connected to the CLK pin of the Z7_PS_EMMC_CLK output. The DAT2 pin is connected to the CMD pin of the Z7_PS_EMMC_CMD output. The DAT_N pin is connected to the RST_N pin of the Z7_PS_EMMC_RESET_N output. The Z7_PS_EMMC_RESET_N output is shown as a blue line with a downward-pointing arrow.

I12

VCC_1	VSS_1
mtfc8gacaaam-1m	
VCC_2	VSS_2
VCC_3	VSS_3
VCC_4	VSS_4

I10

VCCQ_1	VSSQ_1
VCCQ_2	VSSQ_2
VCCQ_3	VSSQ_3
VCCQ_4	VSSQ_4
VCCQ_5	VSSQ_5

I13

VDDIM

RFU_9
RFU_10
RFU_11
RFU_12
RFU_13
RFU_14
RFU_15
RFU_16
RFU_17

RFU_1
RFU_2
RFU_3
RFU_4
RFU_5
RFU_6
RFU_7
RFU_8

?

?

0.1U

1U-10V

NC_1	NC_54
NC_2	NC_55
NC_3	NC_56
NC_4	NC_57
NC_5	NC_58
NC_6	NC_59
NC_7	NC_60
NC_8	NC_61
NC_9	NC_62
NC_10	NC_63
NC_11	NC_64
NC_12	NC_65
NC_13	NC_66
NC_14	NC_67
NC_15	NC_68
NC_16	NC_69
NC_17	NC_70
NC_18	NC_71
NC_19	NC_72
NC_20	NC_73
NC_21	NC_74
NC_22	NC_75
NC_23	NC_76
NC_24	NC_77
NC_25	NC_78
NC_26	NC_79
NC_27	NC_80
NC_28	NC_81
NC_29	NC_82
NC_30	NC_83
NC_31	NC_84
NC_32	NC_85
NC_33	NC_86
NC_34	NC_87
NC_35	NC_88
NC_36	NC_89
NC_37	NC_90
NC_38	NC_91
NC_39	NC_92
NC_40	NC_93
NC_41	NC_94
NC_42	NC_95
NC_43	NC_96
NC_44	NC_97
NC_45	NC_98
NC_46	NC_99
NC_47	NC_100
NC_48	NC_101
NC_49	NC_102
NC_50	NC_103
NC_51	NC_104
NC_52	NC_105
NC_53	NC_106

Circuit diagram showing a 100MΩ resistor connected between **V_Z7_3V3** and **V_Z7**. The output of **V_Z7** is connected to **PS_3V3** and **EMMC** through switches. Each switch has a 0.1nF capacitor in series with its ground connection. The output of **EMMC** is labeled **I9**.

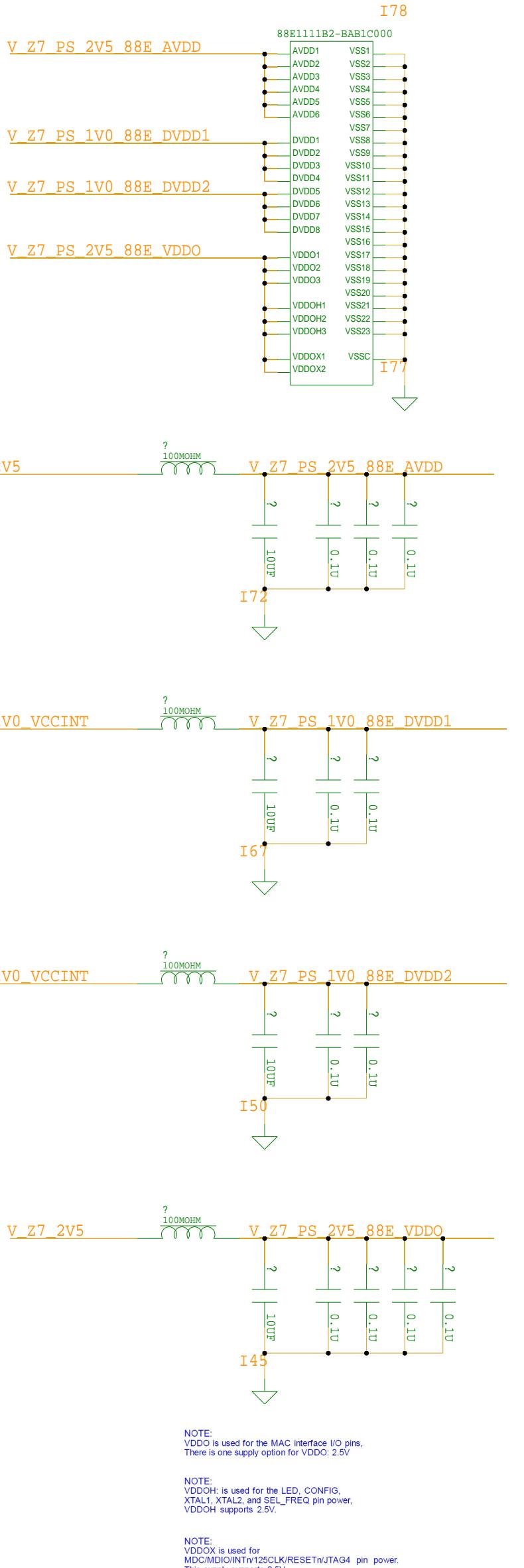
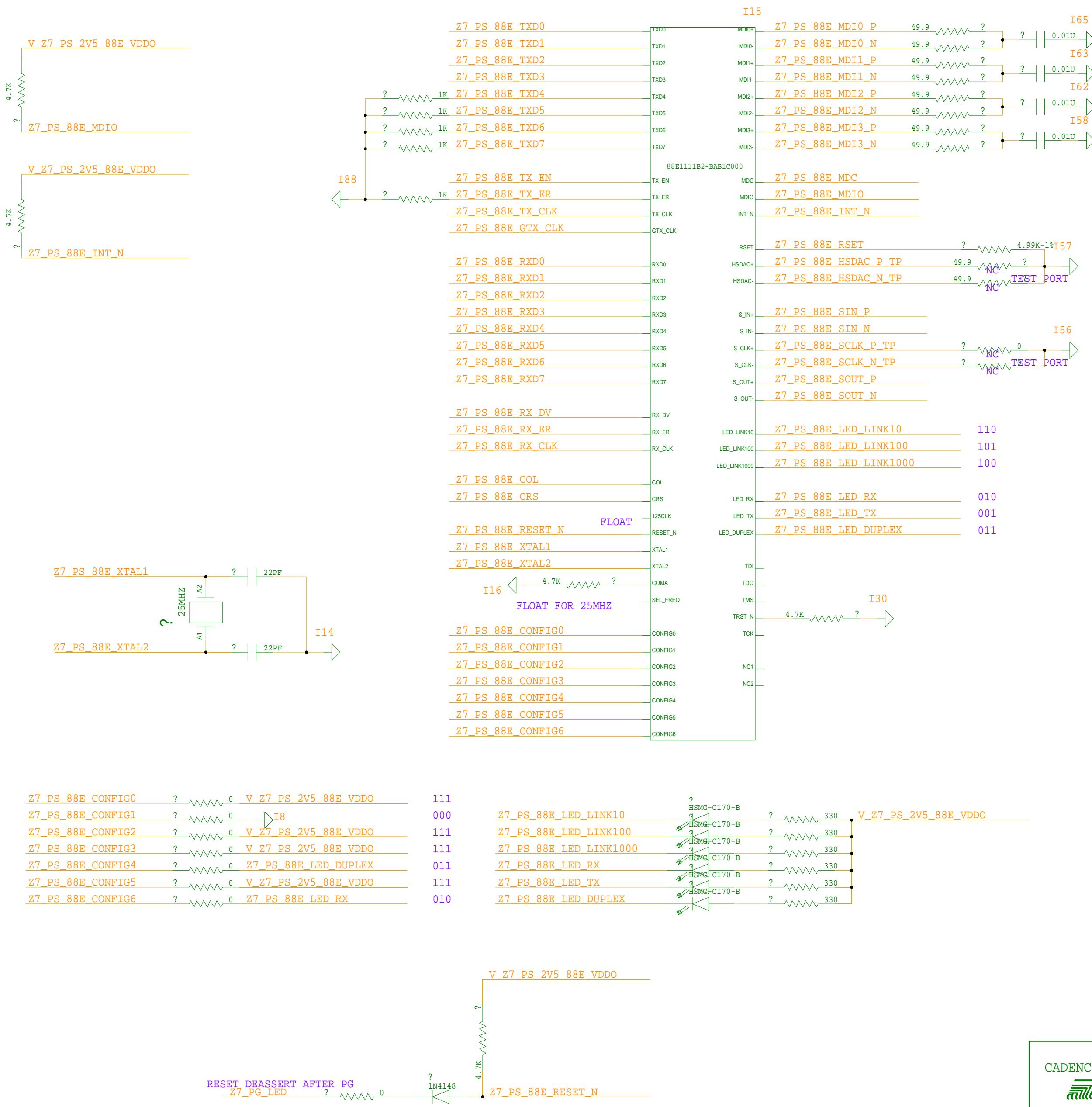
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ZYNQ-7 PS GE PHY (1)

REVISIONS				
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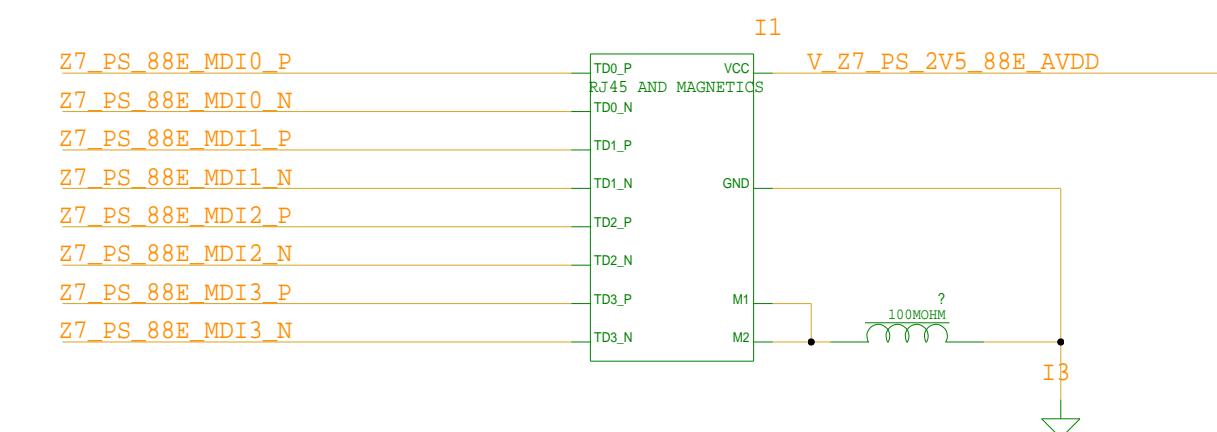
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ZYNQ-7 PS GE PHY (2)

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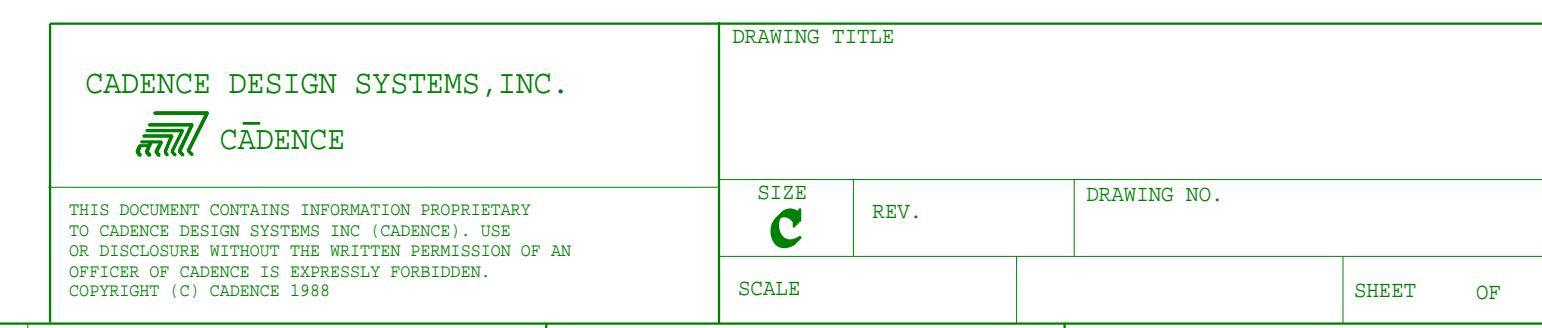
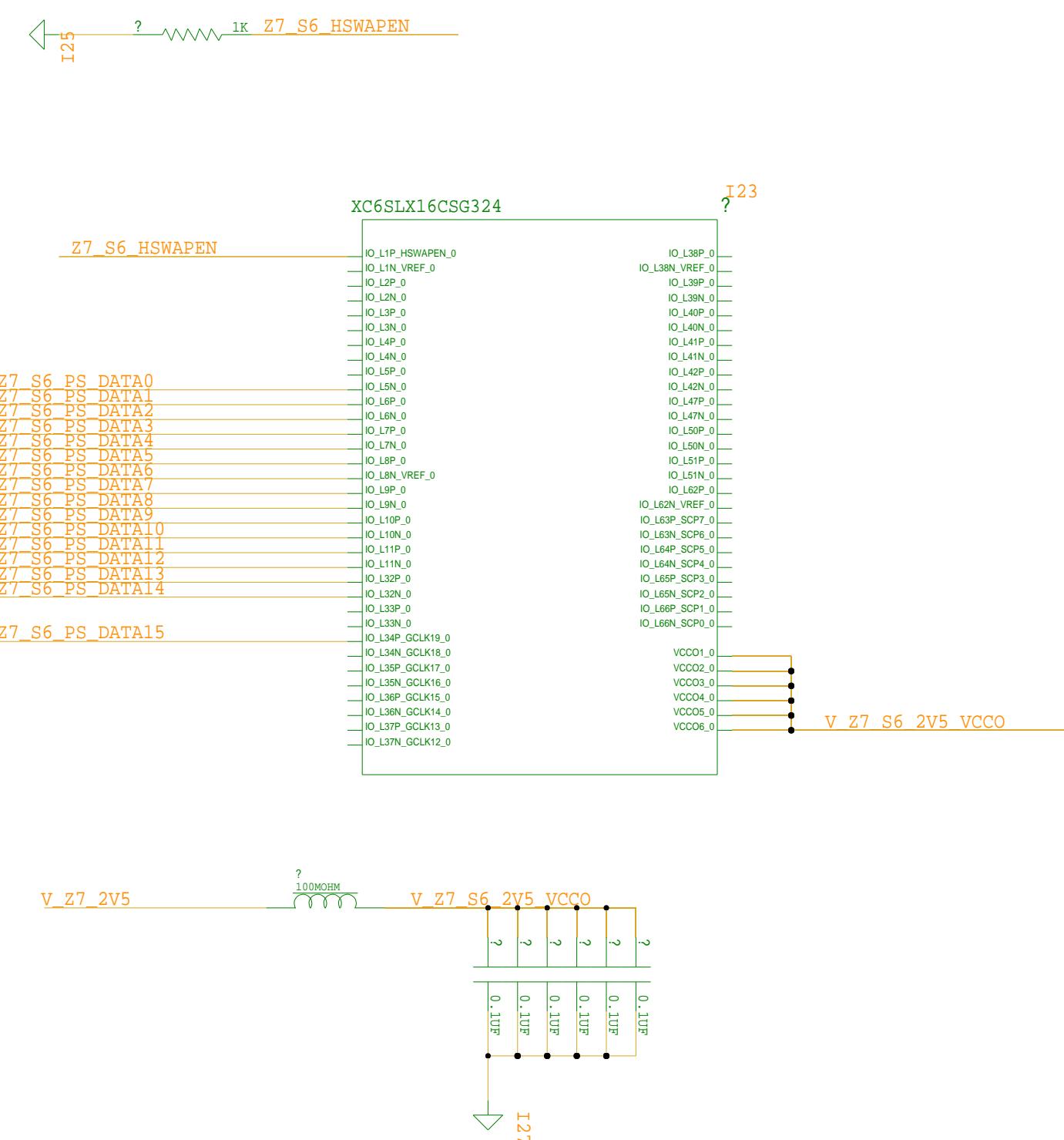
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ZYNQ-7 SPARTAN6 (2)

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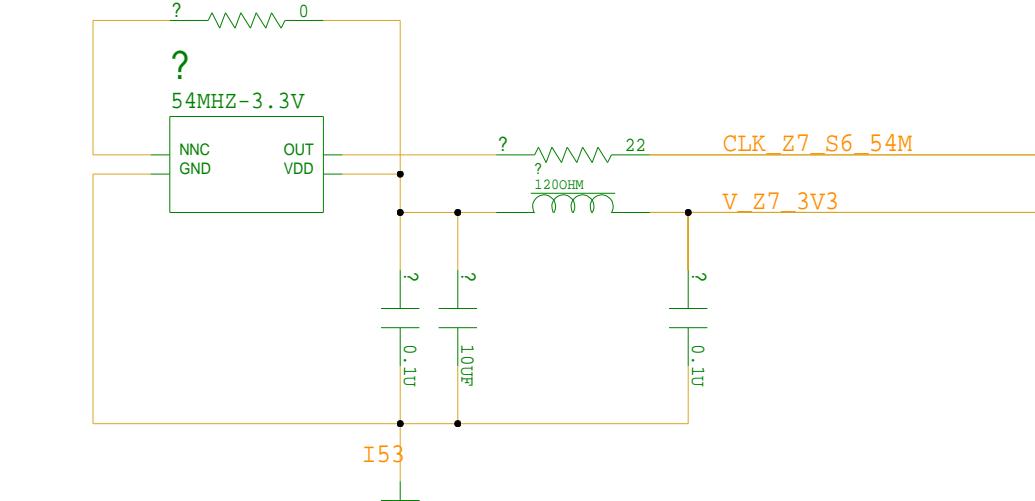
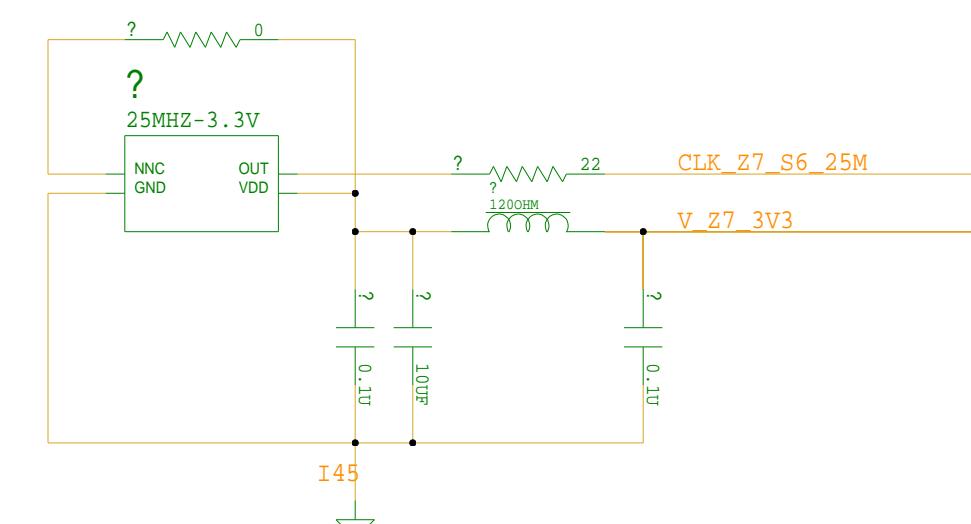
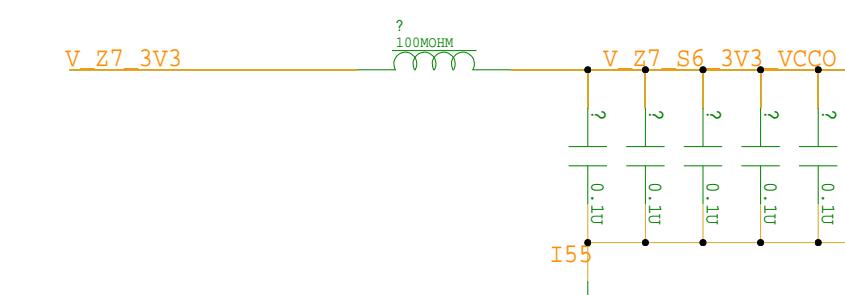
I54

Z7_S6_PL_DATA0
 Z7_S6_PL_DATA1
 Z7_S6_PL_DATA2
 Z7_S6_PL_DATA3
 Z7_S6_PL_DATA4
 Z7_S6_PL_DATA5
 Z7_S6_PL_DATA6
 Z7_S6_PL_DATA7
 Z7_S6_PL_DATA8
 Z7_S6_PL_DATA9
 Z7_S6_PL_DATA10
 Z7_S6_PL_DATA11
 Z7_S6_PL_DATA12
 Z7_S6_PL_DATA13
 Z7_S6_PL_DATA14

IO_L1P_A25_1
 IO_L1N_A24_VREF_1
 IO_L2P_A23_M1A13_1
 IO_L2N_A22_M1A14_1
 IO_L3P_A21_M1RESET_1
 IO_L3N_A20_M1A15_1
 IO_L4P_A19_M1OKE_1
 IO_L5N_A18_M1A12_1
 IO_L6P_A17_M1A10_1
 IO_L2N_A16_M1A09_1
 IO_L3P_A15_M1A10_1
 IO_L3N_A14_M1A11_1
 IO_L4P_A13_M1WE_1
 IO_L5N_A12_M1BA2_1
 IO_L6P_A11_M1A7_1
 IO_L8N_A10_M1A2_1
 IO_L3P_A9_M1BA0_1
 IO_L8N_A8_M1BA1_1
 IO_L5P_A7_M1A0_1
 IO_L5P_A6_M1CK1_1
 IO_L3N_A4_M1CKN_1
 IO_L3P_M1A3_1
 IO_L3N_M1DDT_1
 IO_L4P_GCLK11_M1A5_1
 IO_L4N_GCLK10_M1A6_1
 IO_L4P_GCLK9_IRDY1_M1RASN_1
 IO_L4N_GCLK8_M1CASN_1
 IO_L4P_GCLK7_M1UDM_1
 IO_L4N_GCLK6_M1DDY1_M1LDM_1
 IO_L4P_GCLK5_M1DD4_1
 IO_L4N_GCLK4_M1DD5_1

IO_L4P_A3_M1D06_1
 IO_L4N_A2_M1D07_1
 IO_L4P_A1_M1LDDQS_1
 IO_L4N_A0_M1LDDSN_1
 IO_L4P_FCS_B_M1D01_1
 IO_L4N_FCS_B_M1D02_1
 IO_L4P_FIVE_B_M1D00_1
 IO_L4N_LDC_M1D01_1
 IO_L4P_HDC_M1D00_1
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 IO_L5P_M1D012_1
 IO_L5N_M1D013_1
 IO_L5P_M1D014_1
 IO_L5N_M1D015_1
 IO_L5N_VREF_1
 IO_L6P_1
 IO_L6N_1
 IO_L7P_AWAKE_1
 IO_L74N_DOUT_BUSY_1

CLK_Z7_S6_54M
 Z7_S6_PL_DATA15



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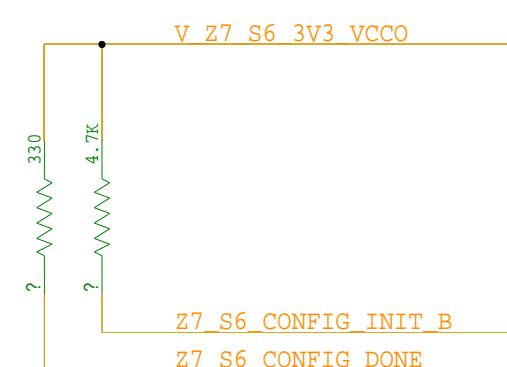
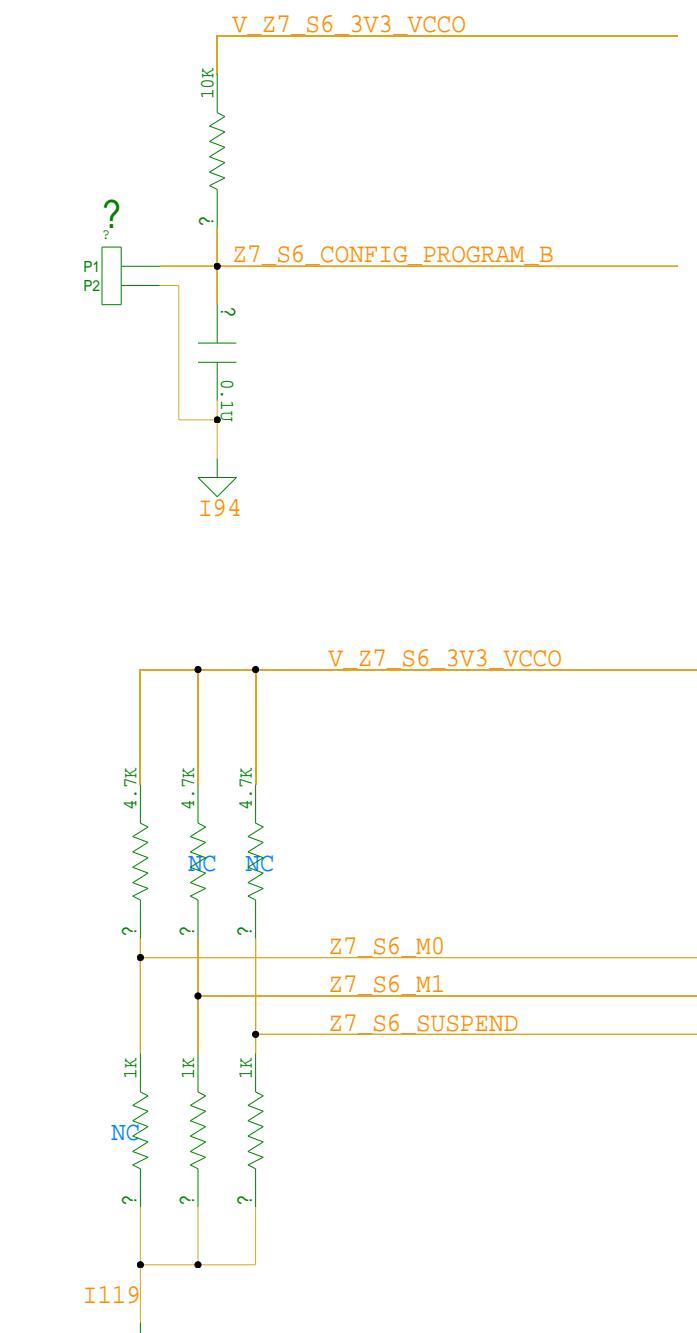
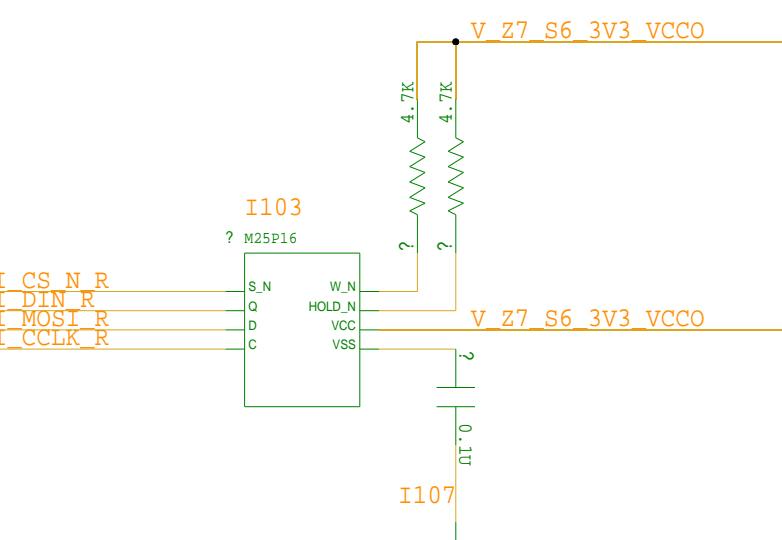
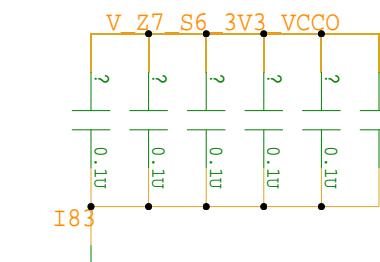
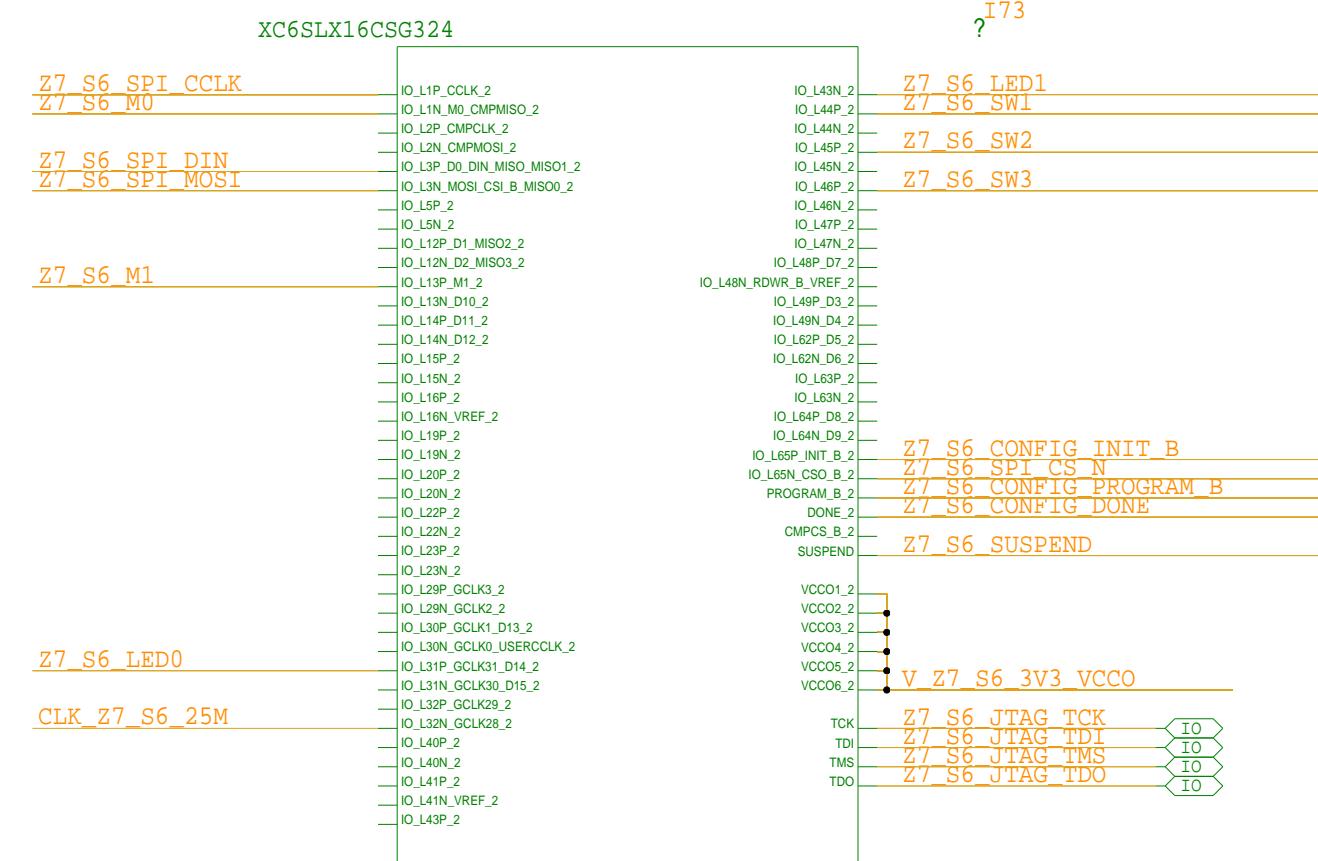
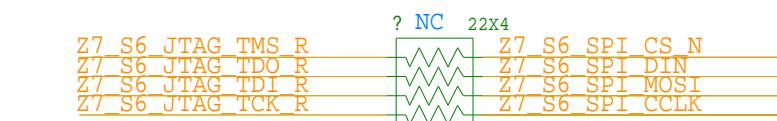
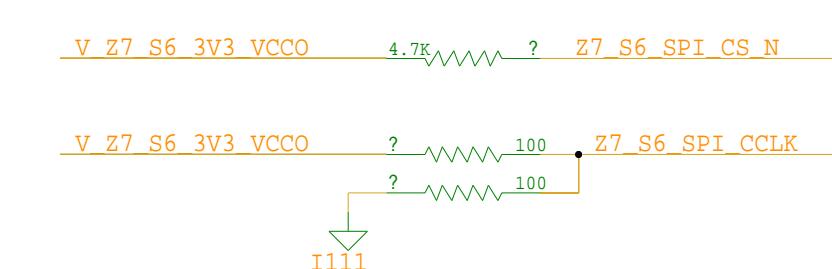
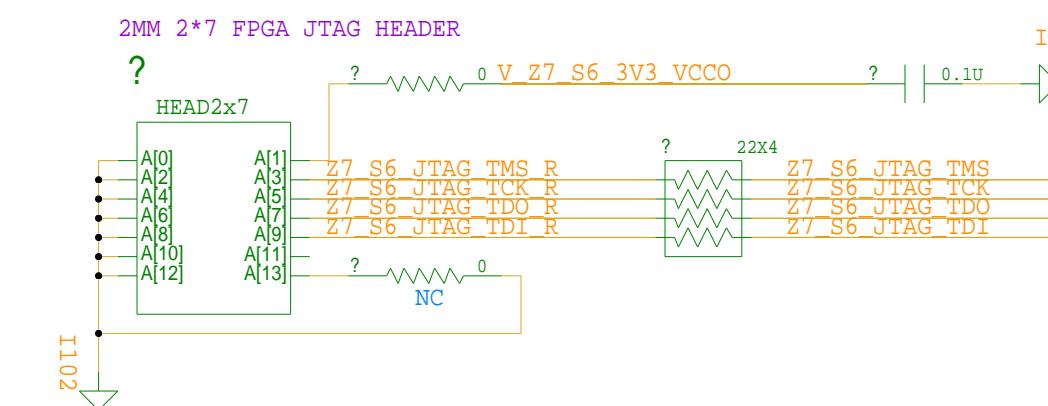
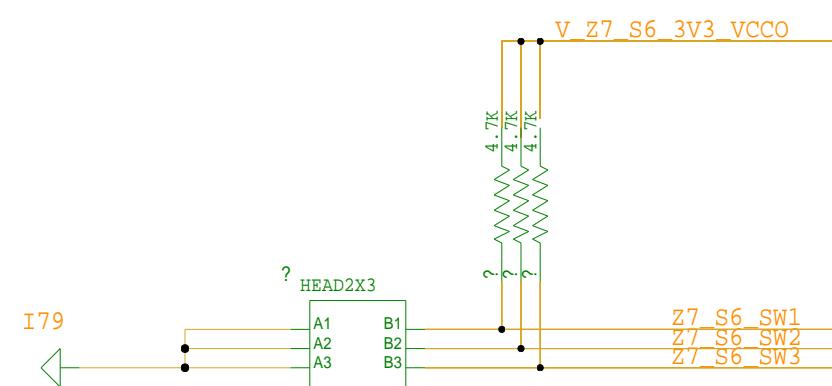
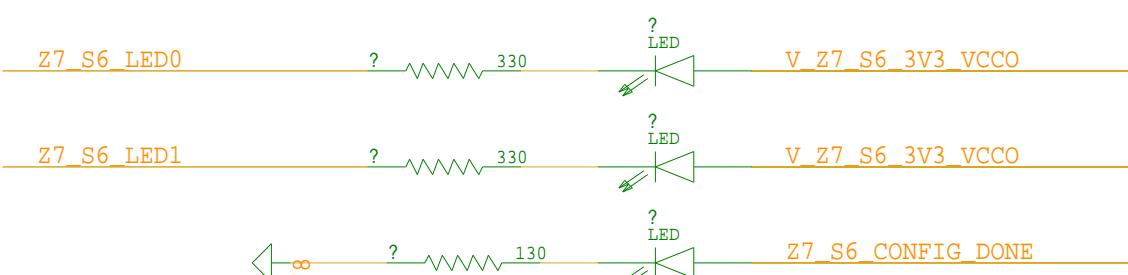
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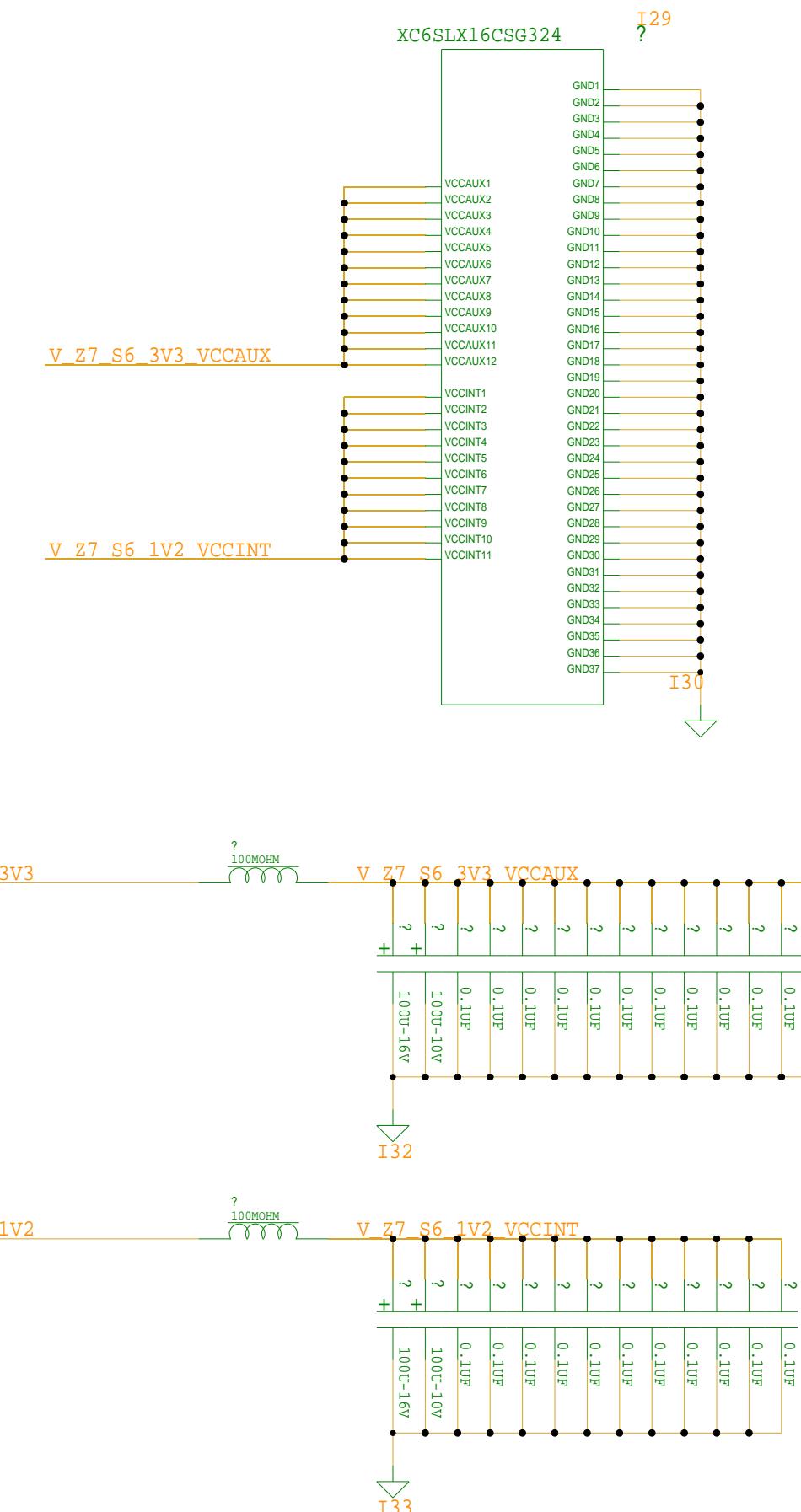
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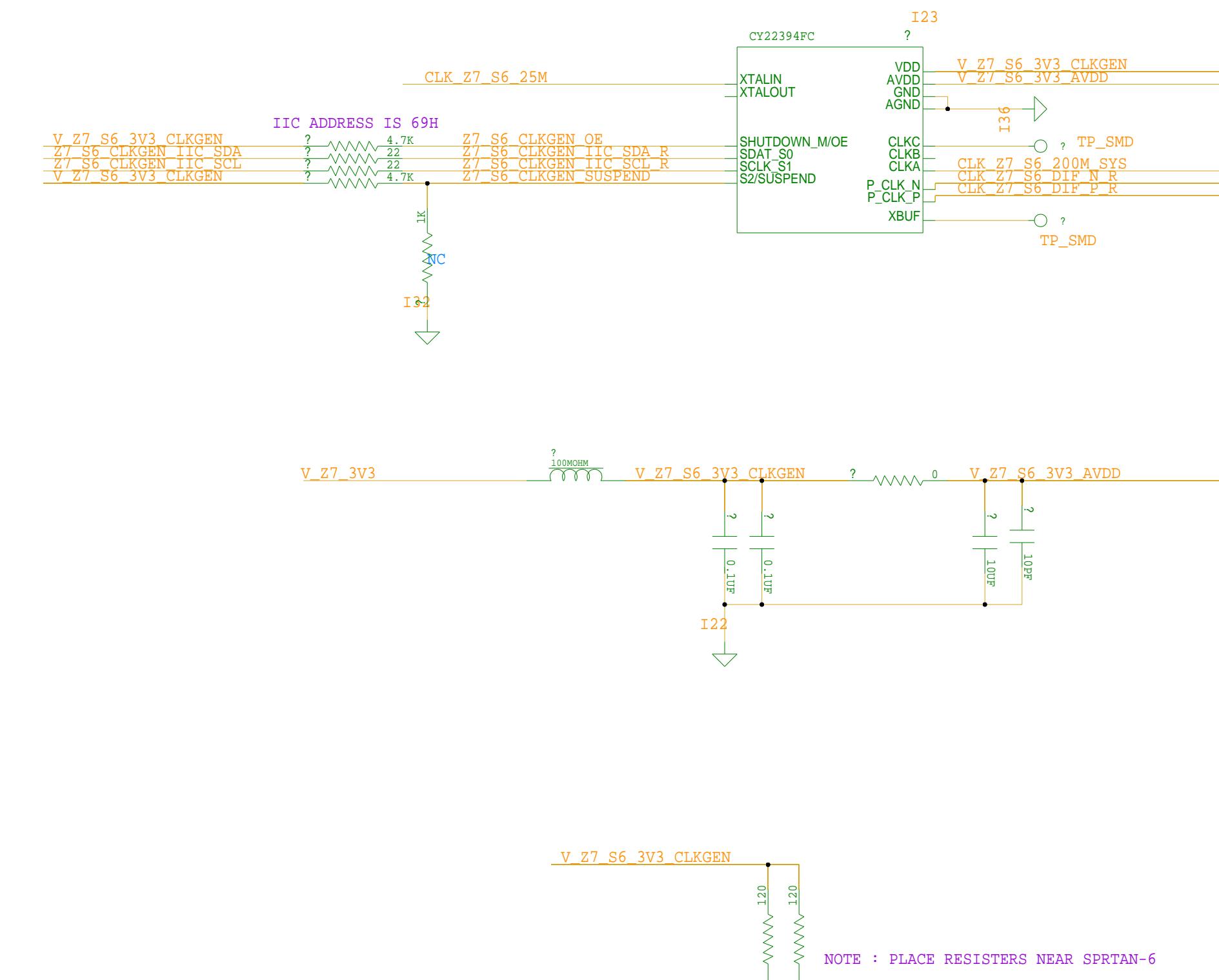
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ZYNQ-7 SPARTAN6 (6)

REVISIONS

ZONE	LTR	DESCRIPTION	DATE	APPR.

FPGA DDR2 200M-CLOCK



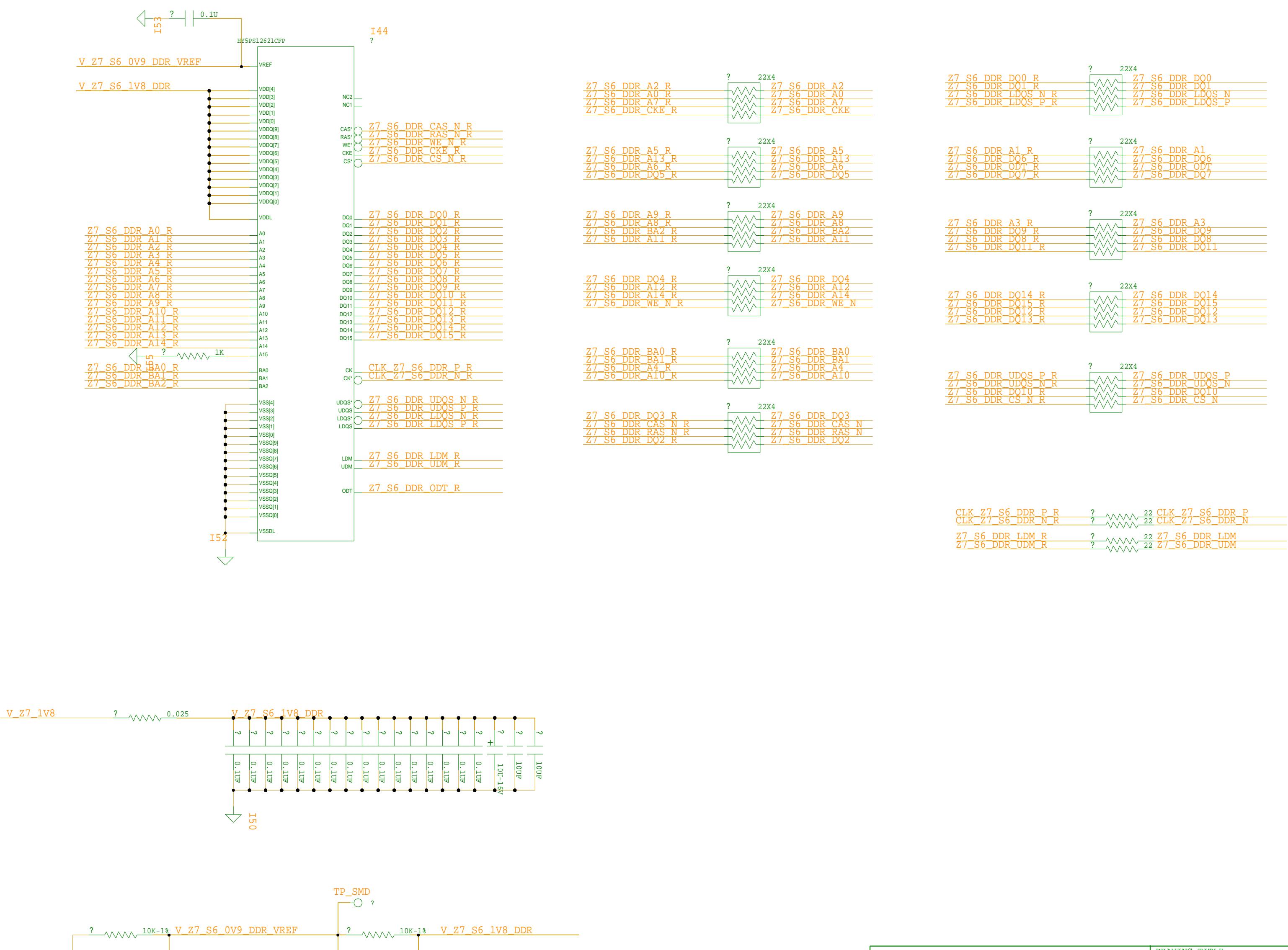
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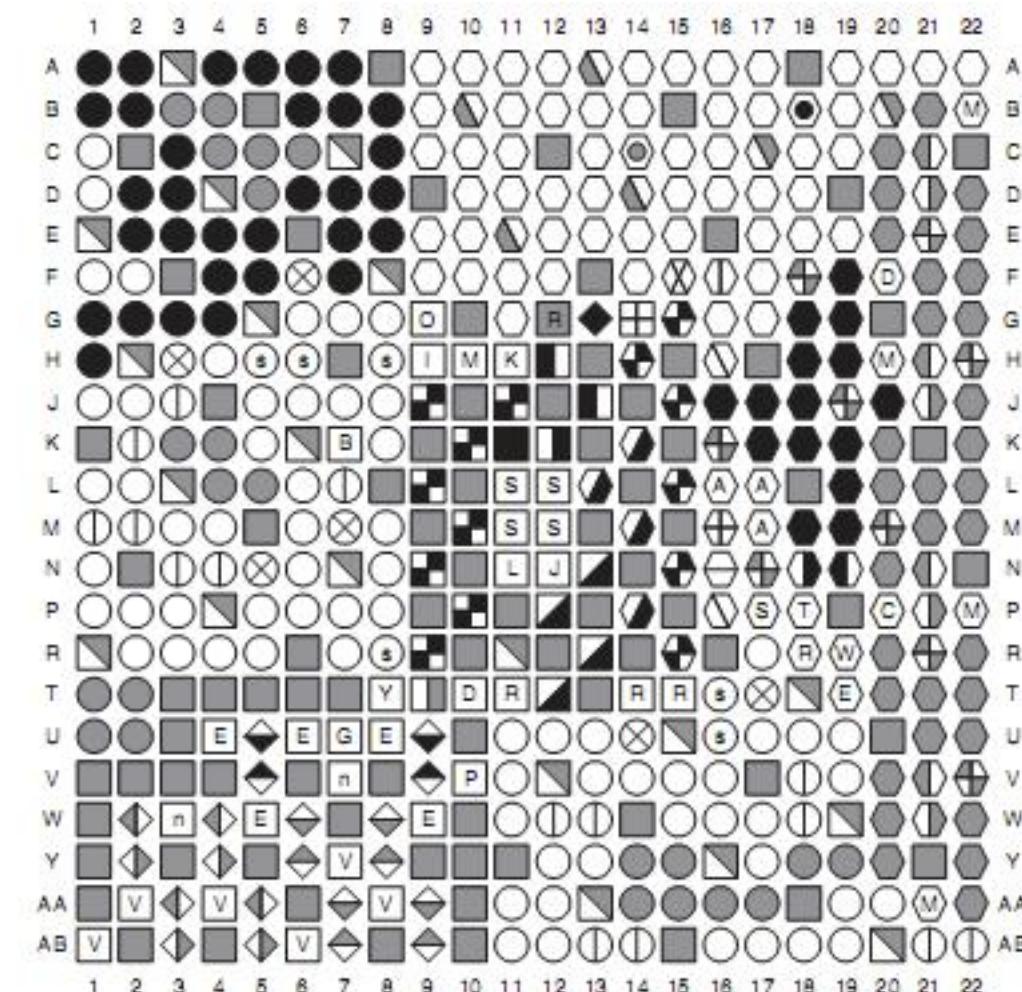
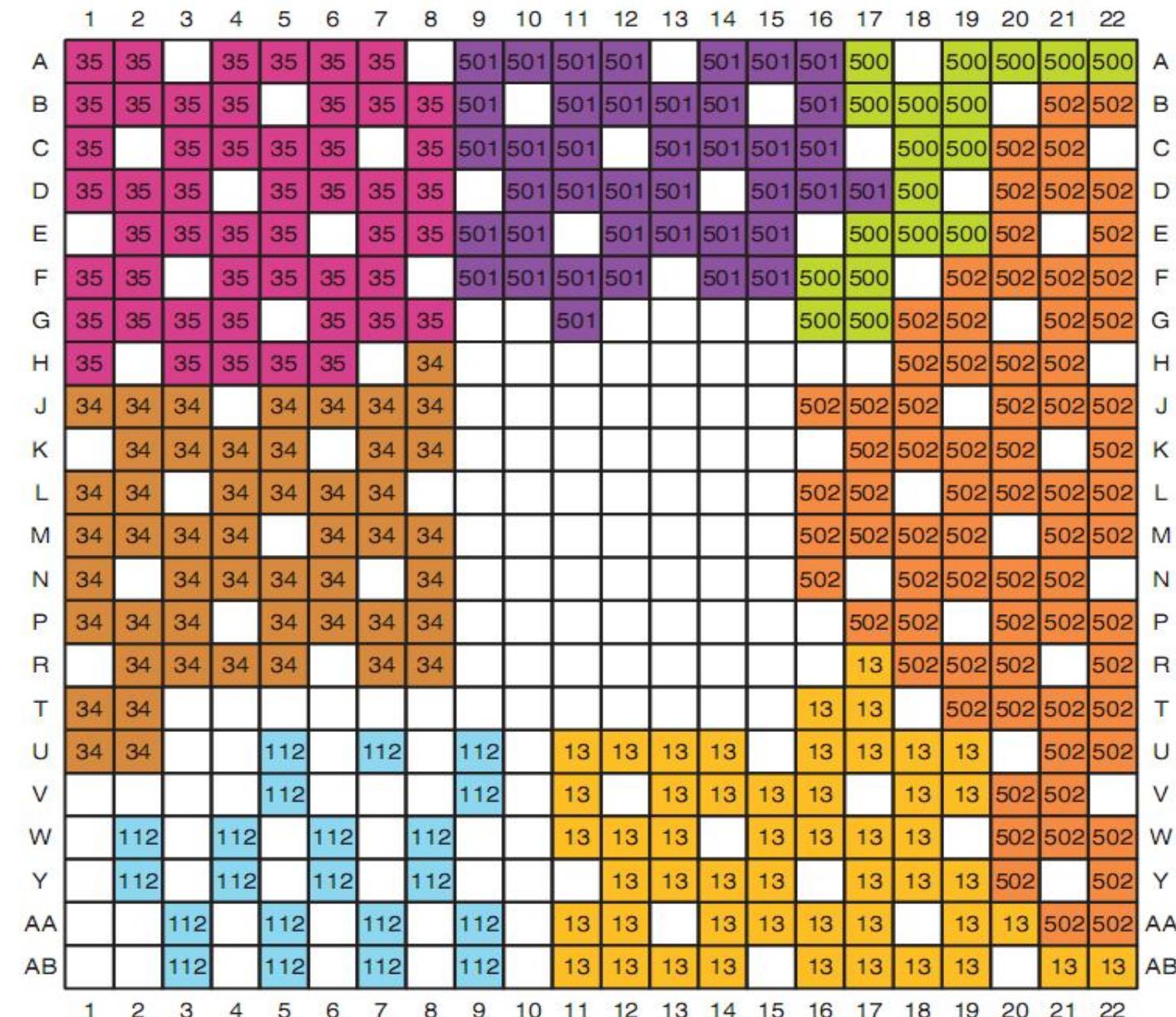
Table 1. Summary of the main characteristics of the four groups of patients.

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ZYNQ-7 PINOUT MAP

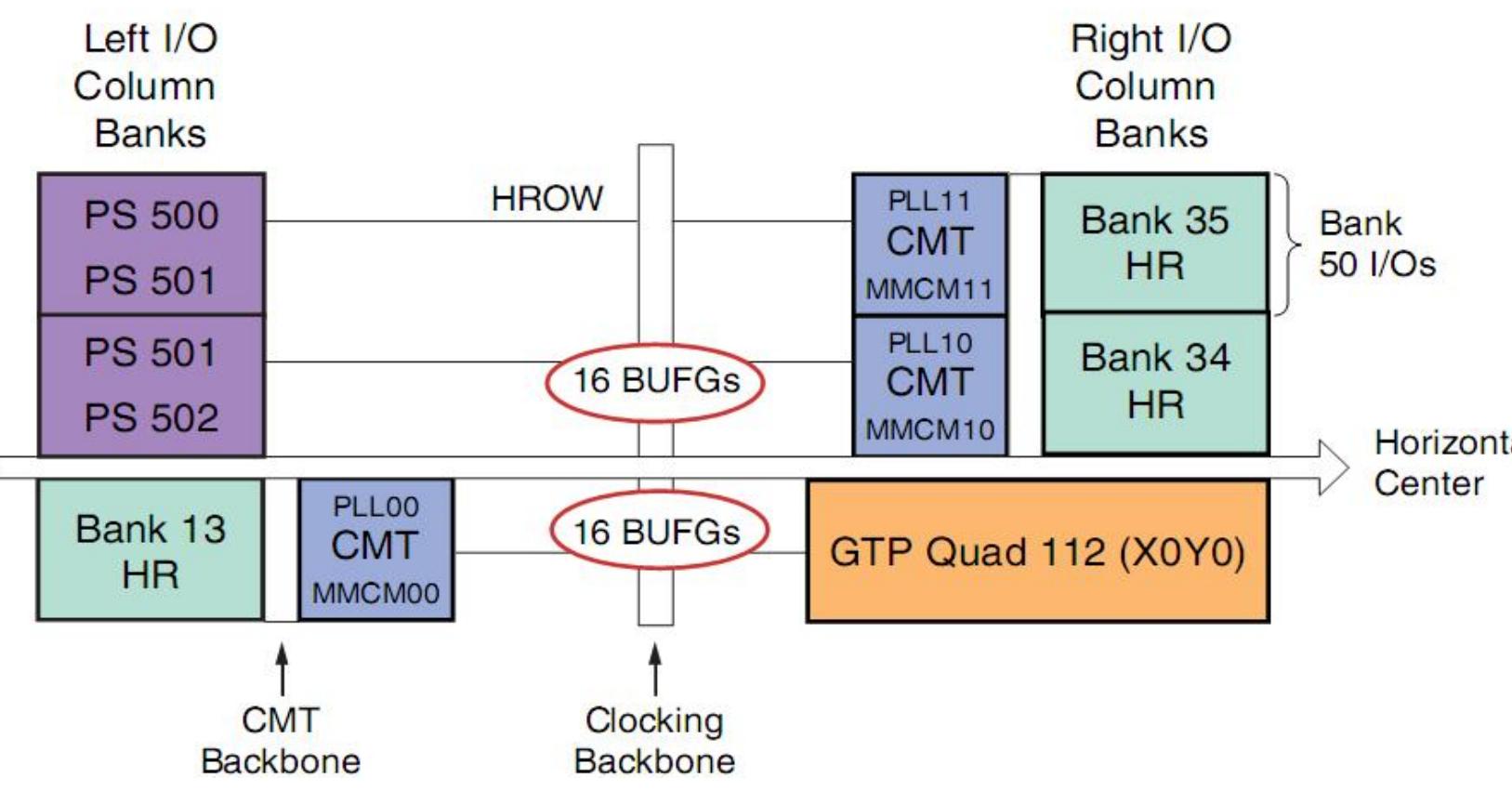
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ZONE	LTR	DESCRIPTION	DATE	APPR.



BANK35 : 3.3V SPARTAN6/ USB/HDMI INOUT
BANK34 : 1.35V DDR3
BANK13 : 3.3V HDMI TRANSMITER
BANK112 : SFP

BANK502 : 1.35V DDR3*2
BANK501 : 2.5V SPARTAN6/ 88E1111
BANK500 : 3.3V SPI FLASH



User I/O Pins	Transceiver Pins	Dedicated Pins	Other Pins	PS MIO Pins	PS DDR Pins
○ IO_LXXY_# ● IO_XX_#	E MGTAVCC_G# V MGTAVTT_G# A MGTVCVAUX_G# < MGTAVTTRCAL G MGTRREF ◆ MGTRFCLK1OP ◆ MGTRFCLK1ON ◆ MGTPRXP ◆ MGTPRXN ◆ MGTPTXP ◆ MGPTXN B PUDC_B ● ADOP/ADON- AD15P/AD15N ⊕ VRN ○ VRP ⊗ VREF ○ DOS ● MRCC ● SRCC	■ CFGBVS_0 D DONE_0 J DXP_0 L DXN_0 ■ GNDADC_0 Y INIT_B_0 P PROGRAM_B_0 K TCK_0 I TD_L_0 O TDO_0 M TMS_0 ■ VCCADC_0 ■ VCCBATT_0 S VP_0 S VN_0 S VREFP_0 S VREFN_0	GND ■ VCCAUX_J_O_G# ■ VCCAUX ■ VCCINT ■ GNDADC_0 ■ VCCO_# ■ VCCBRAM ■ VCCPINT ■ VCCPAUX ■ VCCO_MIO0 ■ VCCO_MIO1 ■ VCCO_DDR ■ VCCPLL ■ RSVDVCC[3:1] ■ RSVDGND ■ NC	● PS_POP_B ○ PS_CLK ○ PS_SRST_B ⊗ PS_MIO_VREF ○ PS_MIO	○ PS_DDR_CKP ○ PS_DDR_CKN ● PS_DDR_CKE ● PS_DDR_CS_B ○ PS_DDR_RAS_B ○ PS_DDR_CAS_B ○ PS_DDR_WE_B ● PS_DDR_BA ● PS_DDR_A ○ PS_DDR_ODT ○ PS_DDR_DRST_B ● PS_DDR_DO ● PS_DDR_DM ● PS_DDR_DOS_P ● PS_DDR_DOS_N ○ PS_DDR_VRP ○ PS_DDR_VRN ○ PS_DDR_VREF
Multi-Function Pins					

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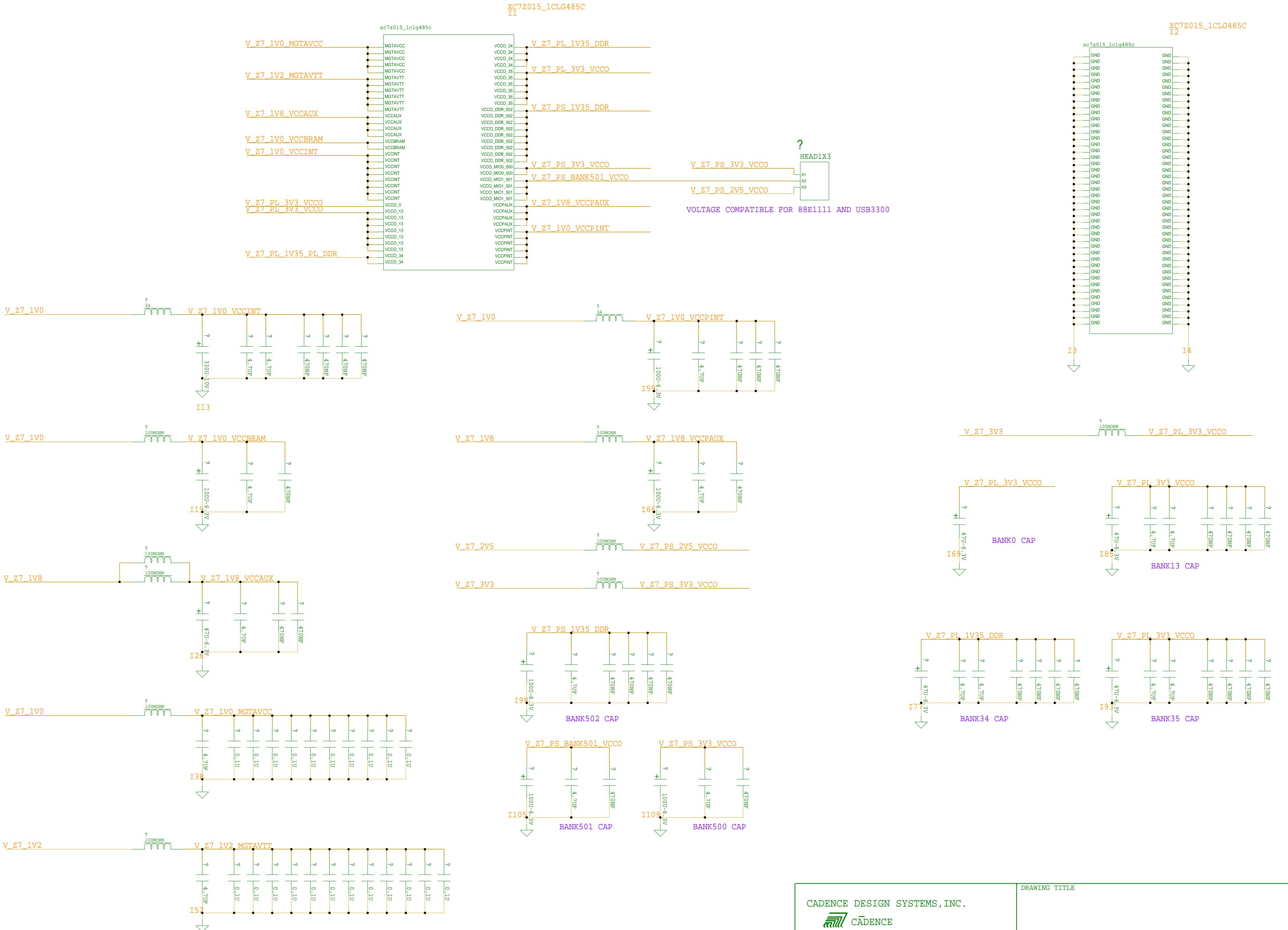
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ZYNQ-7 BANK POWER

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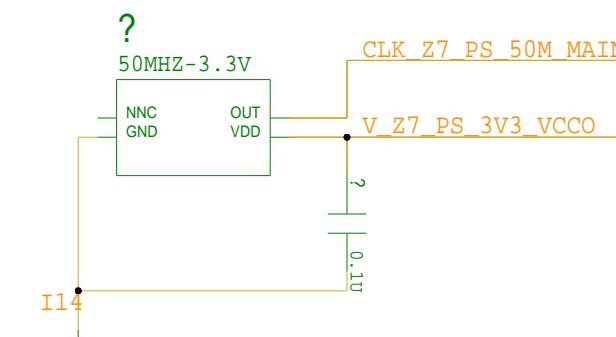
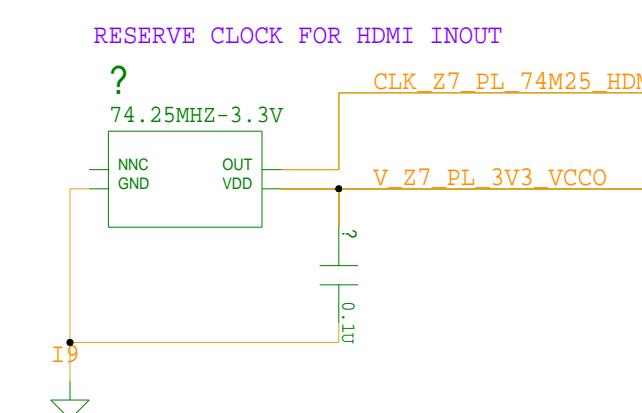
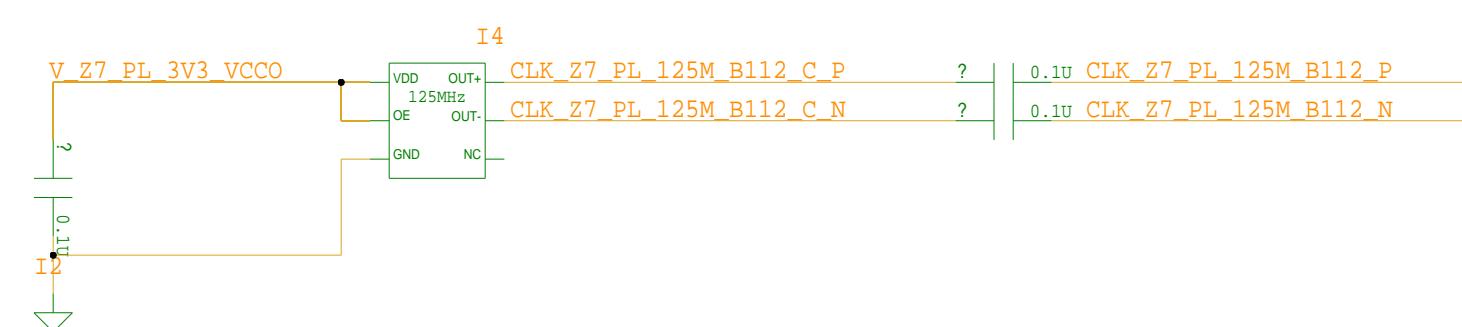
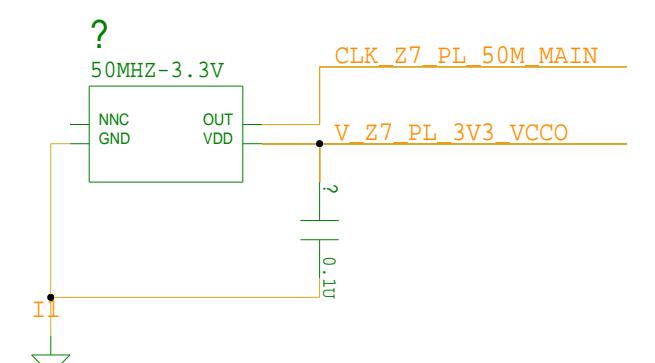
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ZYNQ-7 CLOCK



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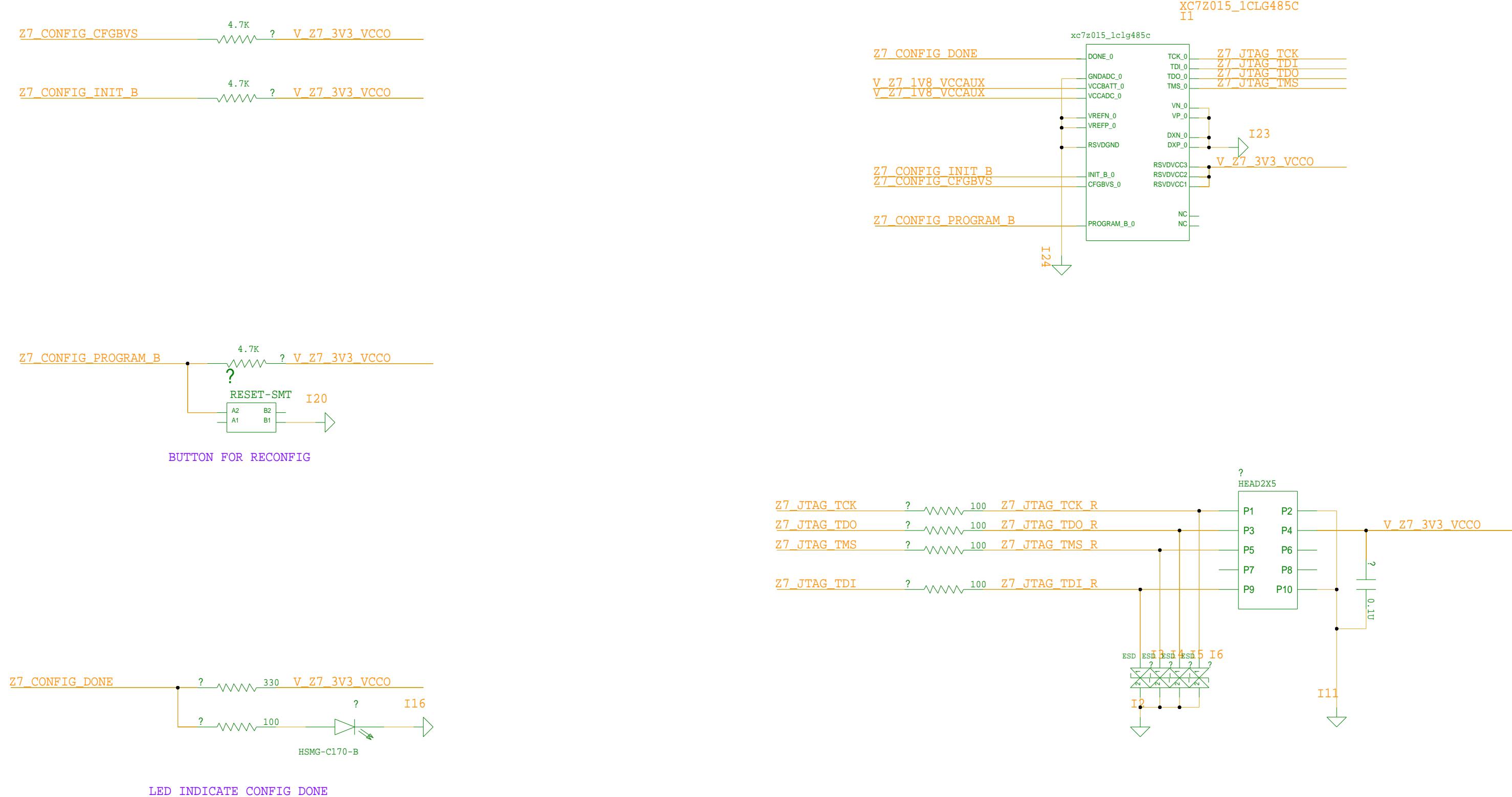
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ZYNQ-7 PL BANK0 JTAG

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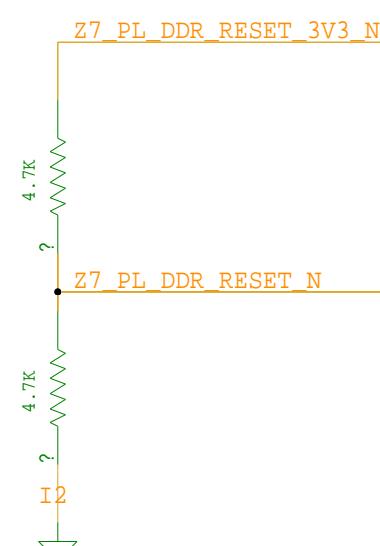
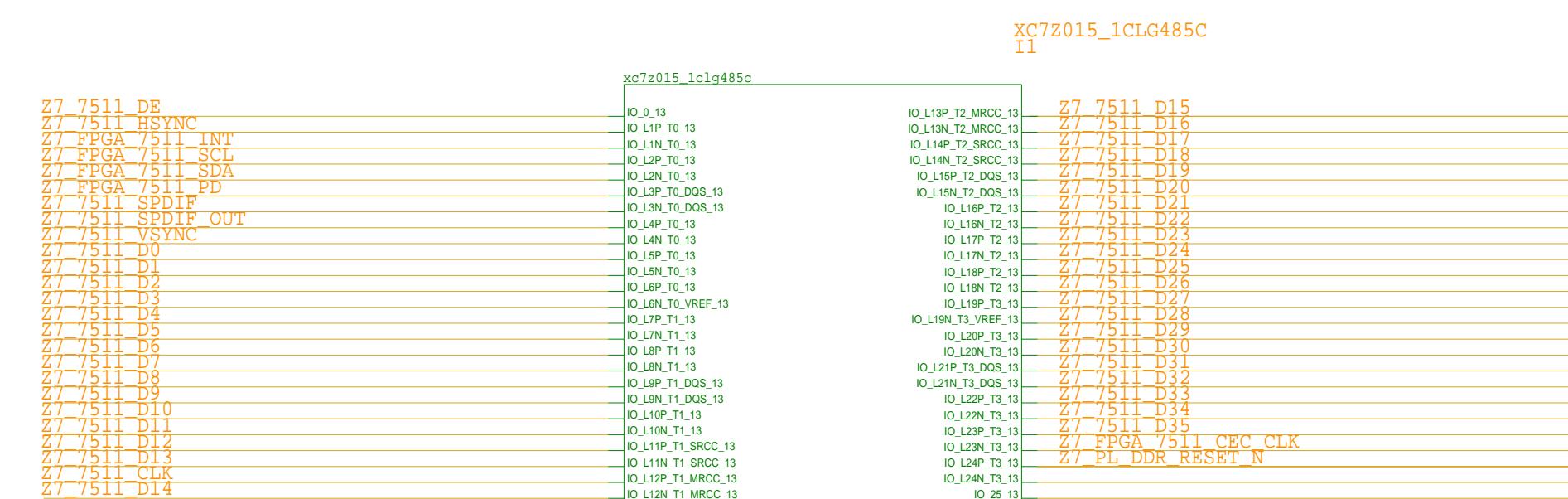
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ZYNQ-7 PL BANK13

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		DATE APPR.



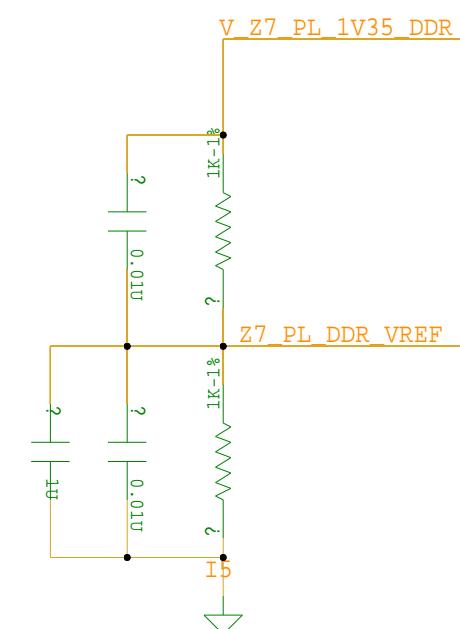
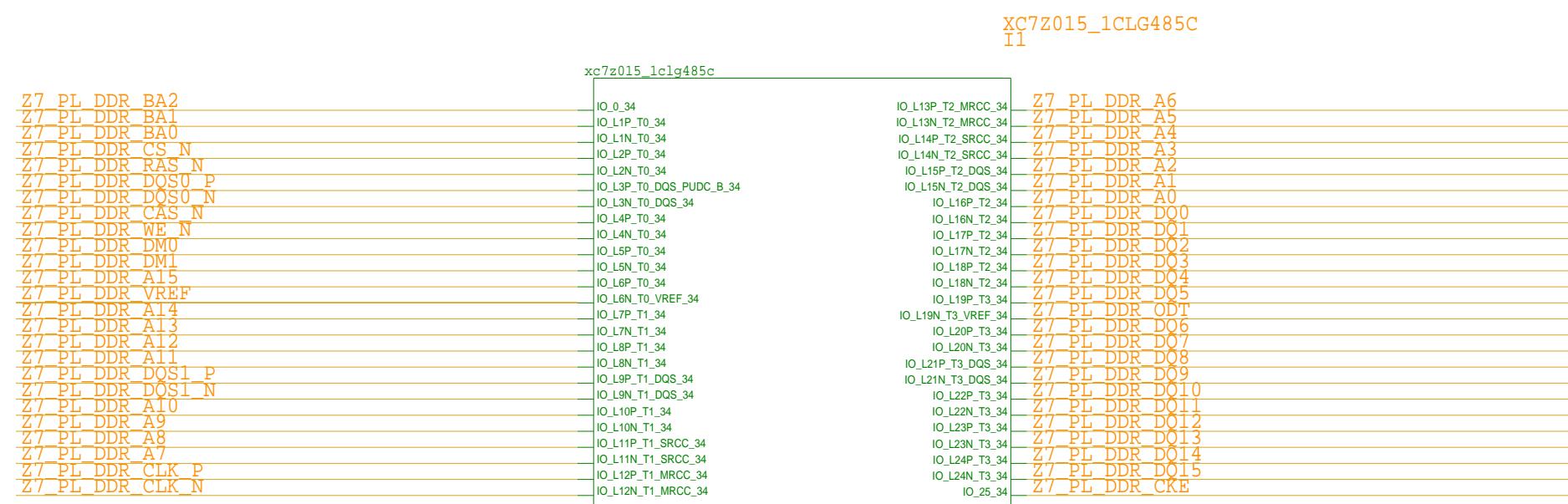
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ZYNQ-7 PL BANK34

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ZYNQ-7 PL BANK35

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ZONE	LTR	DESCRIPTION	DATE	APPR.

xc7z015_1clg485c		XC7Z015_1CLG485C I1
Z7 HDMI HP	IO_0_35	CLK_Z7_PL_50M_MAIN
Z7 HDMI DATA0 R P	IO_L1P_T0_AD0P_35	Z7 S6 PL DATA15
Z7 HDMI DATA0 R N	IO_L1N_T0_AD0N_35	
Z7 HDMI DATA1 R P	IO_L2P_T0_AD0P_35	
Z7 HDMI DATA1 R N	IO_L2N_T0_AD0N_35	Z7 S6 PL DATA0
Z7 HDMI DATA2 R P	IO_L3P_T0_DOS_AD1P_35	Z7 S6 PL DATA1
Z7 HDMI DATA2 R N	IO_L3N_T0_DOS_AD1N_35	Z7 S6 PL DATA2
Z7 HDMI SCL Q	IO_L4P_T0_35	Z7 S6 PL DATA3
Z7 HDMI SDA Q	IO_L4N_T0_35	Z7 S6 PL DATA4
Z7 HDMI CEC	IO_L5P_T0_AD0P_35	Z7 S6 PL DATA5
Z7 SFP SCL	IO_L5N_T0_AD0N_35	Z7 S6 PL DATA6
Z7 SFP SDA	IO_L6P_T0_35	Z7 S6 PL DATA7
Z7 SFP MOD ABS	IO_L6N_T0_VREF_35	Z7 S6 PL DATA8
Z7 SFP RX LOS	IO_L7P_T1_AD2P_35	Z7 S6 PL DATA9
Z7 SFP TX DISABLE	IO_L7N_T1_AD2N_35	Z7 S6 PL DATA10
Z7 SFP TX FAULT	IO_L8P_T1_AD10P_35	Z7 S6 PL DATA11
Z7 SFP RS0	IO_L8N_T1_AD10N_35	Z7 S6 PL DATA12
Z7 SFP RS1	IO_L9P_T1_DOS_AD3P_35	Z7 S6 PL DATA13
	IO_L9N_T1_DOS_AD3N_35	Z7 S6 PL DATA14
	IO_L10P_T1_AD11P_35	
	IO_L10N_T1_AD11N_35	
	IO_L11P_T1_SRCC_35	
	IO_L11N_T1_SRCC_35	
	IO_L12P_T1_MRCC_35	IO_L24P_T3_AD15P_35
	IO_L12N_T1_MRCC_35	IO_L24N_T3_AD15N_35
		IO_25_35
CLK_Z7_PL_74M25_HDMI		
Z7 HDMI CLK R P		
Z7 HDMI CLK R N		



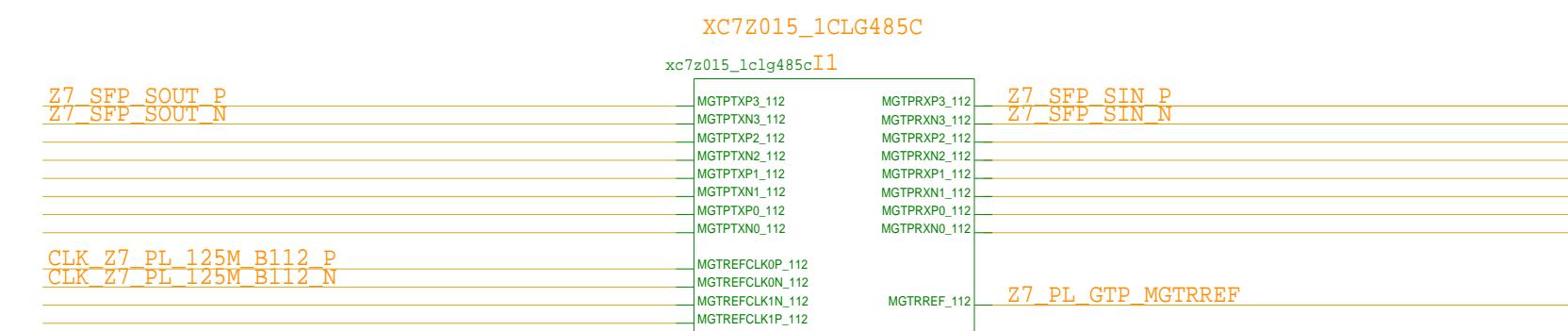
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ZYNQ-7 PL BANK112

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Z7_PL_GTP_MGTRREF 100 V_Z7_1V2_MGTAVTT

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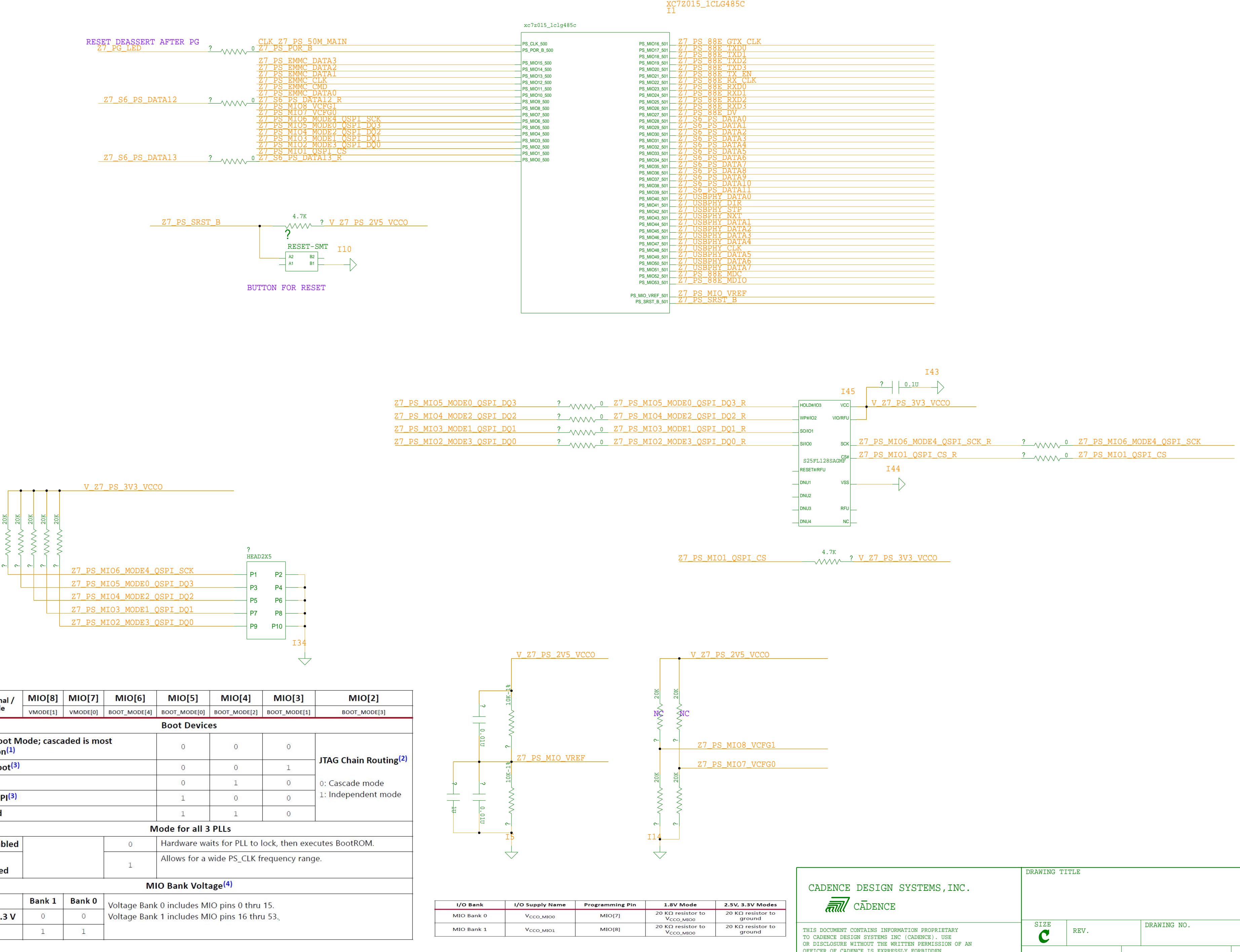
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ZYNQ-7 PS BANK500 / BANK501

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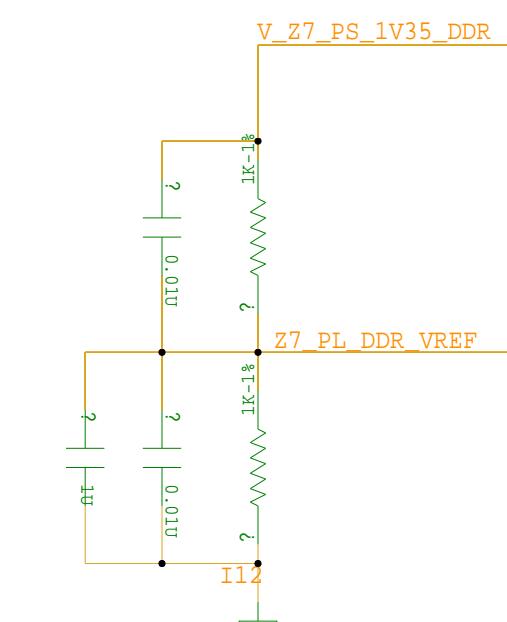
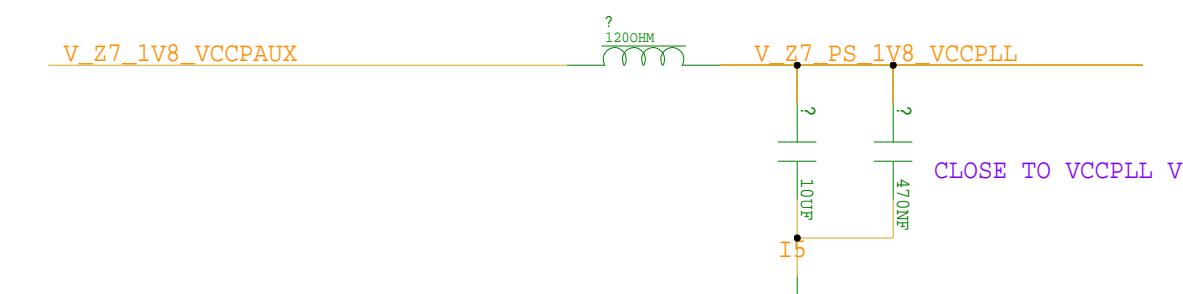
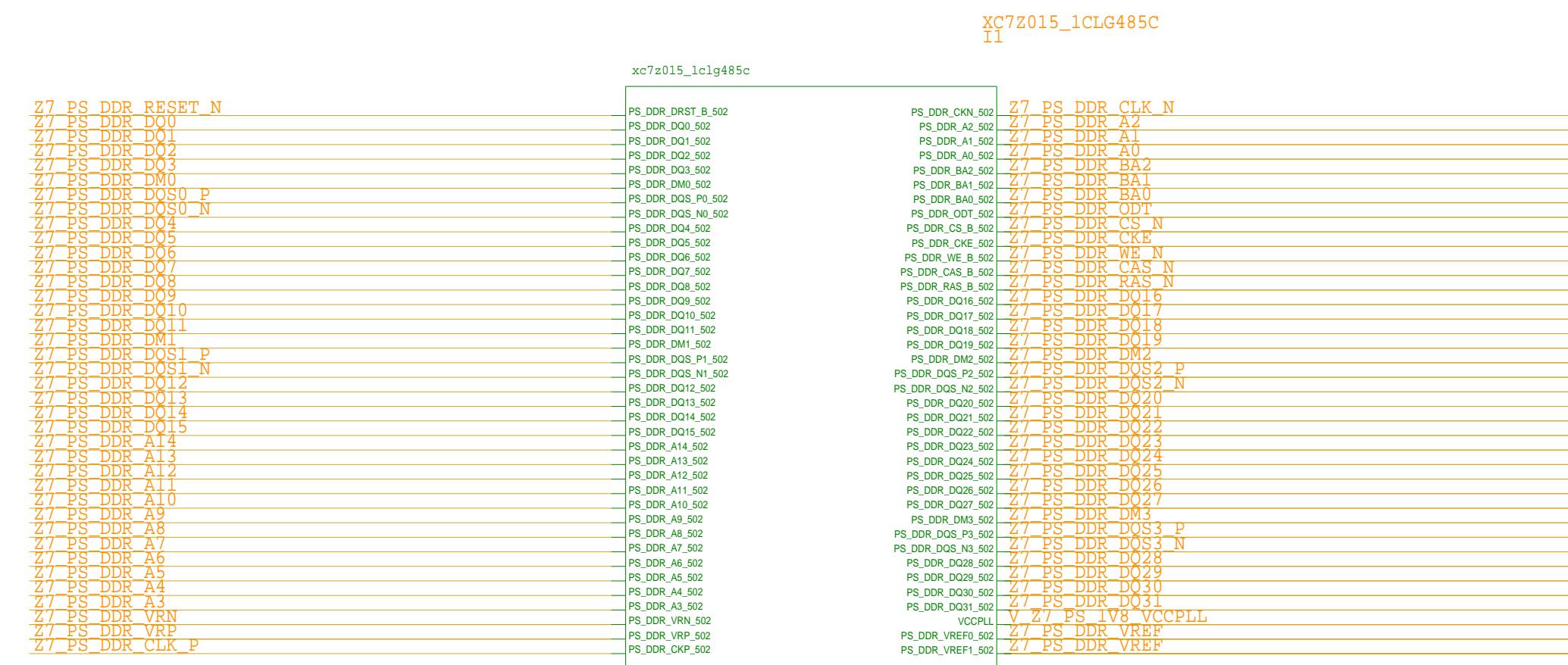
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ZYNQ-7 PS BANK502

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