

8

7

6

5

4

3

2

1

REVISIONS

ZONE	LTR	DESCRIPTION	DATE	APPR.

F

F

E

E

D

D

C

C

B

B

A

A

CADENCE DESIGN SYSTEMS, INC.
 CADENCETHIS DOCUMENT CONTAINS INFORMATION PROPRIETARY
TO CADENCE DESIGN SYSTEMS INC (CADENCE). USE
OR DISCLOSURE WITHOUT THE WRITTEN PERMISSION OF AN
OFFICER OF CADENCE IS EXPRESSLY FORBIDDEN.
COPYRIGHT (C) CADENCE 1988

DRAWING TITLE

SIZE **C** REV. DRAWING NO.

SCALE SHEET OF

8

7

6

5

4

3

2

1

8

7

6

5

4

3

2

1

REVISIONS

ZONE	LTR	DESCRIPTION	DATE	APPR.

F

F

E

E

D

D

C

C

B

B

A

A

CADENCE DESIGN SYSTEMS, INC.
 CADENCE

THIS DOCUMENT CONTAINS INFORMATION PROPRIETARY
TO CADENCE DESIGN SYSTEMS INC (CADENCE). USE
OR DISCLOSURE WITHOUT THE WRITTEN PERMISSION OF AN
OFFICER OF CADENCE IS EXPRESSLY FORBIDDEN.
COPYRIGHT (C) CADENCE 1988

DRAWING TITLE

SIZE **C** REV. DRAWING NO.

SCALE SHEET OF

8

7

6

5

4

3

2

1

SPARTAN-7 INDEX

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPR.

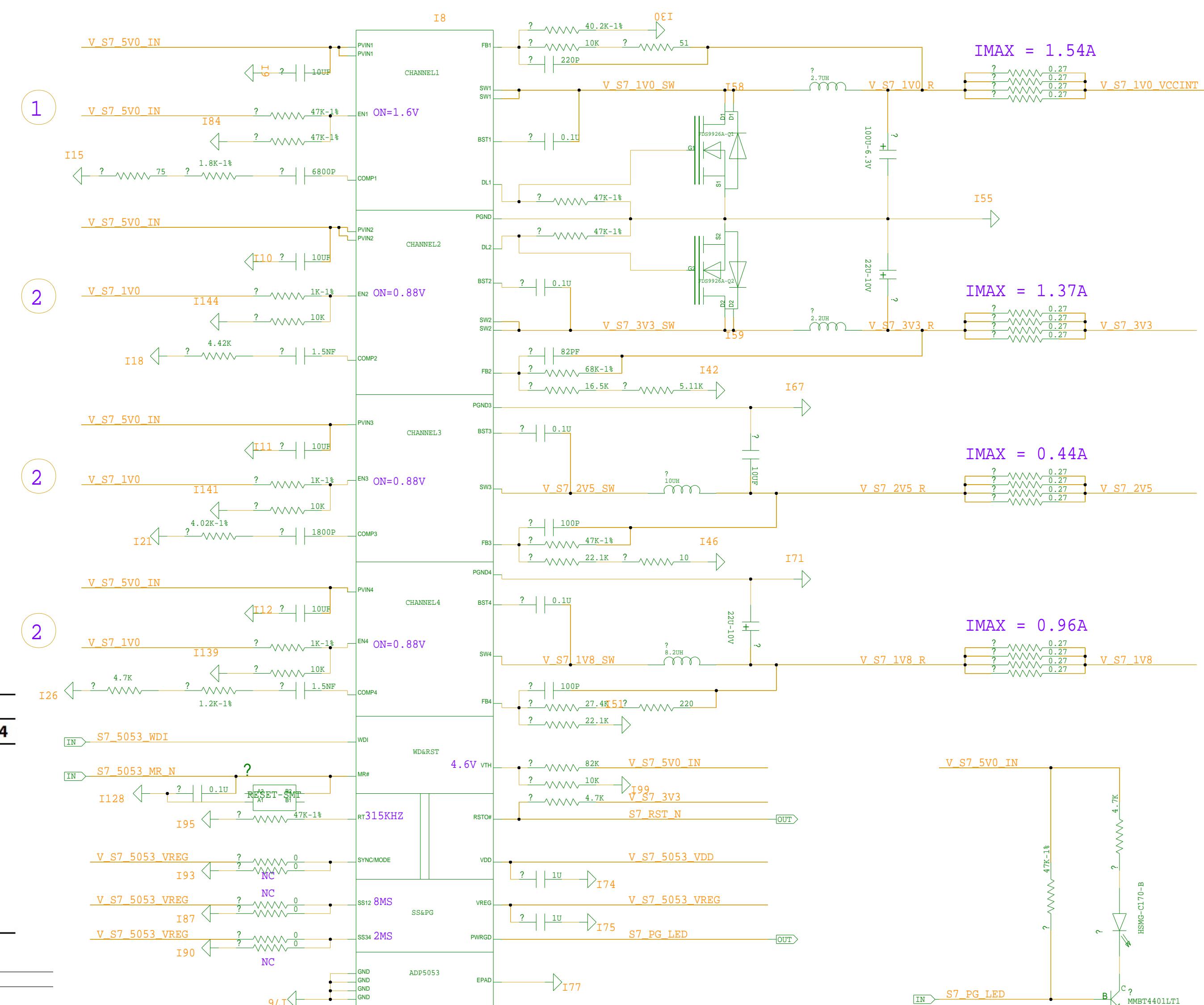
POWER	PAGE 4-5
HDMI RECEVIER	PAGE 6-8
HDMI TRANSMITER	PAGE 9-10
HDMI INOUT	PAGE 11
SFP PHY	PAGE 12-13
SFP INOUT	PAGE 14
USB CONTROLLER	PAGE 15-16
DDR3	PAGE 18
CLOCK	PAGE 21
BANK	PAGE 22-27

CADENCE DESIGN SYSTEMS, INC.  CADENCE	DRAWING TITLE		
	SIZE 	REV.	DRAWING NO.
THIS DOCUMENT CONTAINS INFORMATION PROPRIETARY TO CADENCE DESIGN SYSTEMS INC (CADENCE). USE OR DISCLOSURE WITHOUT THE WRITTEN PERMISSION OF AN OFFICER OF CADENCE IS EXPRESSLY FORBIDDEN. COPYRIGHT (C) CADENCE 1988			
SCALE			SHEET OF

SPARTAN-7 POWER (1)

DESCRIPTION

DATE APPR.



$$V_{OUT} = V_{REF} \times (1 + (R_{TOP}/R_{BOT}))$$

$$R_{RT} (\text{k}\Omega) = [14,822/f_{SW} (\text{kHz})]^{1.081}$$

$$V_{IN_STARTUP} = (0.8 \text{ nA} + (0.8 \text{ V}/R_{BOT_EN})) \times \left(R_{TOP_EN} + \frac{R_{BOT_EN} \times 1 \text{ M}\Omega}{R_{BOT_EN} + 1 \text{ M}\Omega} \right)$$

where:

 R_{TOP_EN} is the resistor from V_{IN} to EN. R_{BOT_EN} is the resistor from EN to ground.

Table 9. Soft Start Time Set by the SS12 and SS34 Pins

R_{TOP} (k Ω)	R_{BOT} (k Ω)	Soft Start Time			
		Channel 1	Channel 2	Channel 3	Channel 4
0	N/A ¹	2 ms	2 ms	2 ms	2 ms
100	600	2 ms	Parallel	2 ms	4 ms
200	500	2 ms	8 ms	2 ms	8 ms
300	400	4 ms	2 ms	4 ms	2 ms
400	300	4 ms	4 ms	4 ms	4 ms
500	200	8 ms	2 ms	4 ms	8 ms
600	100	8 ms	Parallel	8 ms	2 ms
N/A ¹	0	8 ms	8 ms	8 ms	8 ms

Table 16. Factory Default Options

Option	Default Value
Channel 1 Output Voltage	0.8V adjustable output
Channel 2 Output Voltage	0.8V adjustable output
Channel 3 Output Voltage	0.8V adjustable output
Channel 4 Output Voltage	0.8V adjustable output
PWRGD Pin (Pin 20) Output	Monitor Channel 1 output
Output Discharge Function	Enabled for all four buck regulators
Switching Frequency on Channel 1	1 x switching frequency set by the RT pin
Switching Frequency on Channel 3	1 x switching frequency set by the RT pin
SYNC/MODE Pin (Pin 43) Function	Forced PWM/automatic PWM/PSM mode setting with the ability to synchronize to an external clock
Hiccup Protection	Enabled for overcurrent events
Short-Circuit Latch-Off Function	Disabled for output short-circuit events
Oversupply Latch-Off Function	Disabled for output oversupply events
Reset Timeout Period	200 ms
Watchdog Timeout Period	1.6 sec
Manual Reset Input Mode	Processor manual reset mode

CADENCE DESIGN SYSTEMS, INC.

CADENCE

THIS DOCUMENT CONTAINS INFORMATION PROPRIETARY
TO CADENCE DESIGN SYSTEMS INC (CADENCE). USE
OR DISCLOSURE WITHOUT THE WRITTEN PERMISSION OF AN
OFFICER OF CADENCE IS EXPRESSLY FORBIDDEN.
COPYRIGHT (C) CADENCE 1988

DRAWING TITLE

SIZE	REV.	DRAWING NO.
C		

SCALE SHEET OF

1

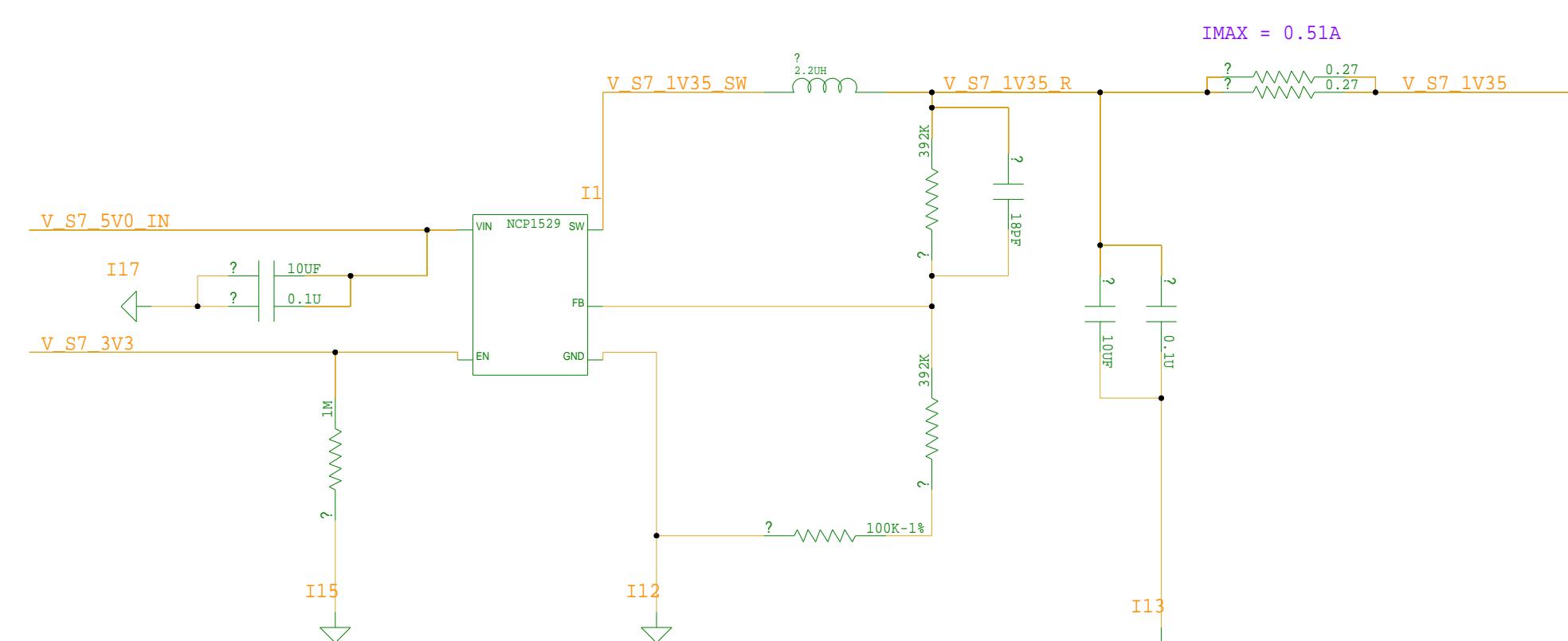
SPARTAN-7 POWER (2)

REVOLUTIONS		DESCRIPTION		DATE	APPR.
ZONE	LTR				

$$V_{out} = V_{FB} \times (1 + R1/R2)$$

- V_{OUT} : Output Voltage (V)
- V_{FB} : Feedback Voltage = 0.6 V
- $R1$: Feedback Resistor from V_{OUT} to FB
- $R2$: Feedback Resistor from FB to GND

3



CADENCE DESIGN SYSTEMS, INC.
 CADENCE

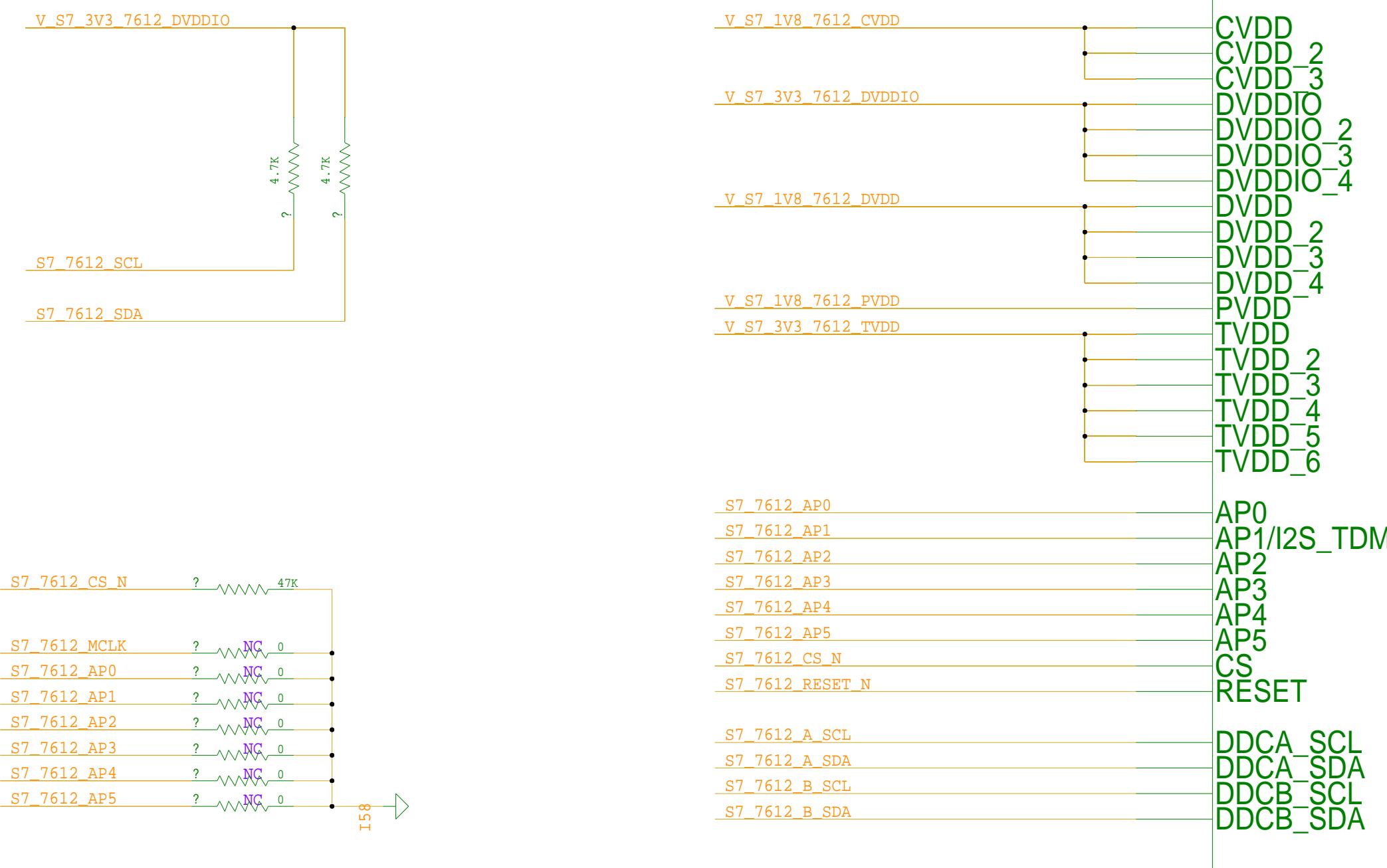
THIS DOCUMENT CONTAINS INFORMATION PROPRIETARY
 TO CADENCE DESIGN SYSTEMS INC (CADENCE). USE
 OR DISCLOSURE WITHOUT THE WRITTEN PERMISSION OF AN
 OFFICER OF CADENCE IS EXPRESSLY FORBIDDEN.
 COPYRIGHT (C) CADENCE 1988

DRAWING TITLE		SIZE		DRAWING NO.	
SCALE	REV.	IN	MM	IN	MM

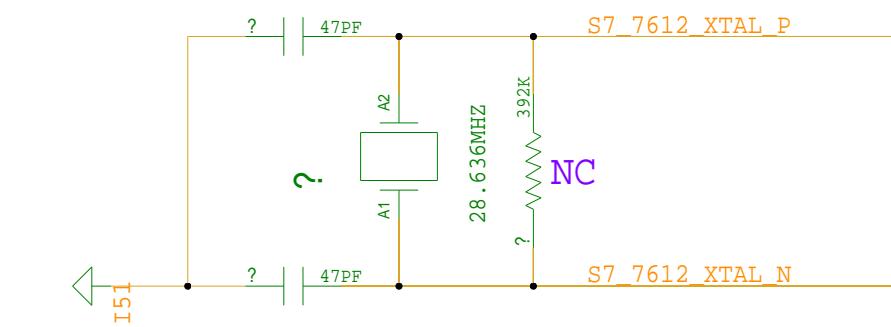
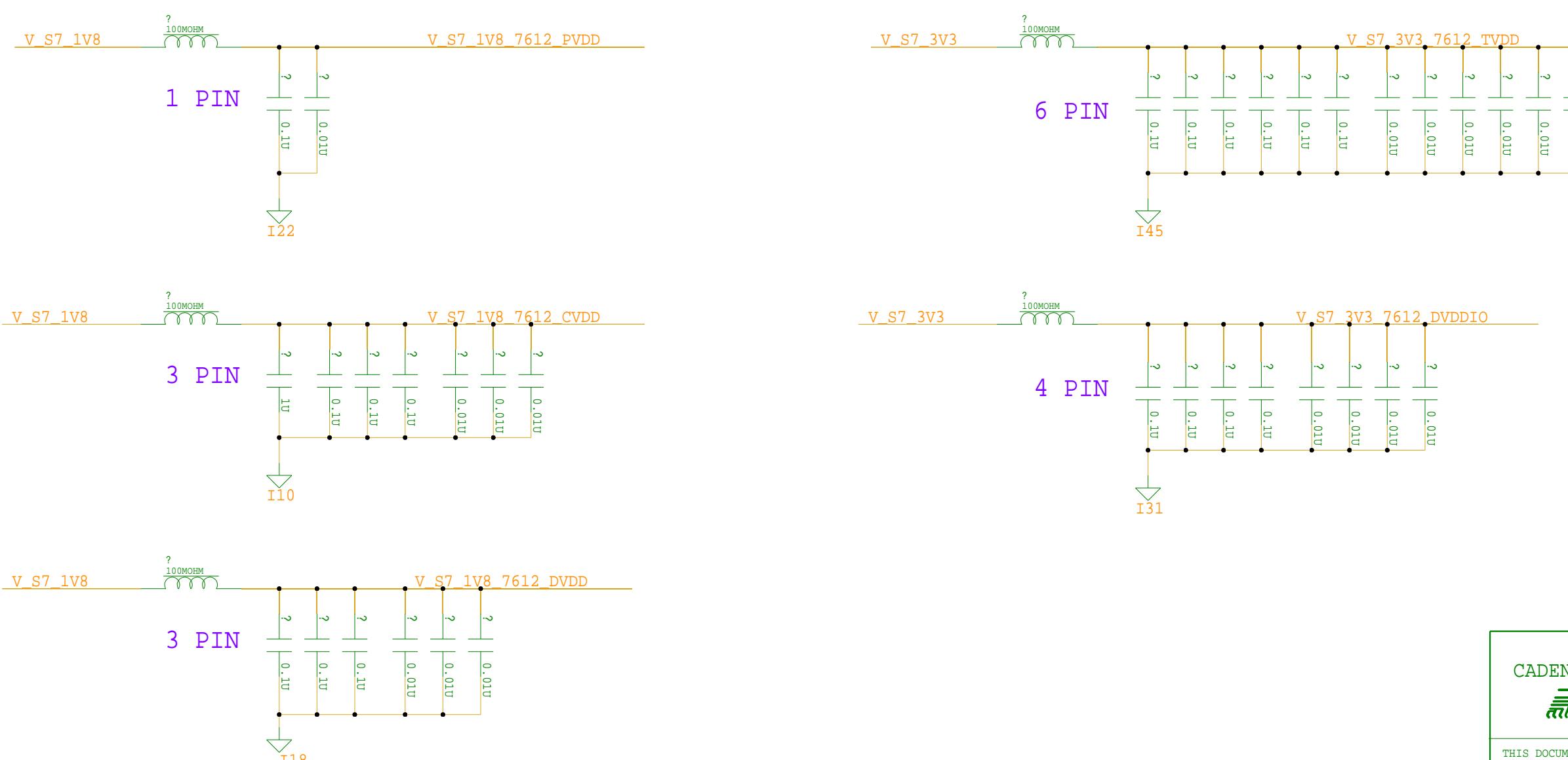
SPARTAN-7 HDMI RECEIVER (1)

REVISED

ZONE	LTR	DESCRIPTION	DATE	APPR.



DE	S7_7612_DE
XTALP	S7_7612_XTAL_P
XTALN	S7_7612_XTAL_N
SDA	S7_7612_SDA
SCLK/INT2	S7_7612_INT2
SCL	S7_7612_SCL
RXB_5V	V_S7_7612_B_5V0
RXA_5V	V_S7_7612_A_5V0
MCLK/INT2	S7_7612_MCLK
INT1	S7_7612_INT1
HPA_B	S7_7612_B_HP
HPA_A/INT2	S7_7612_A_HP
RXB_C+	S7_7612_B_CLK_P
RXB_C-	S7_7612_B_CLK_N
RXB_2-	S7_7612_B_DATA2_N
RXB_1-	S7_7612_B_DATA1_N
RXB_0-	S7_7612_B_DATA0_N
RXB_2+	S7_7612_B_DATA2_P
RXB_1+	S7_7612_B_DATA1_P
RXB_0+	S7_7612_B_DATA0_P
RXA_C+	S7_7612_A_CLK_P
RXA_C-	S7_7612_A_CLK_N
RXA_2-	S7_7612_A_DATA2_N
RXA_1-	S7_7612_A_DATA1_N
RXA_0-	S7_7612_A_DATA0_N
RXA_2+	S7_7612_A_DATA2_P
RXA_1+	S7_7612_A_DATA1_P
RXA_0+	S7_7612_A_DATA0_P



CADENCE DESIGN SYSTEMS, INC.
CADENCE

THIS DOCUMENT CONTAINS INFORMATION PROPRIETARY
TO CADENCE DESIGN SYSTEMS INC (CADENCE). USE
OR DISCLOSURE WITHOUT THE WRITTEN PERMISSION OF AN
OFFICER OF CADENCE IS EXPRESSLY FORBIDDEN.
COPYRIGHT (C) CADENCE 1988

DRAWING TITLE		SIZE		REV.		DRAWING NO.	
SCALE	OF						

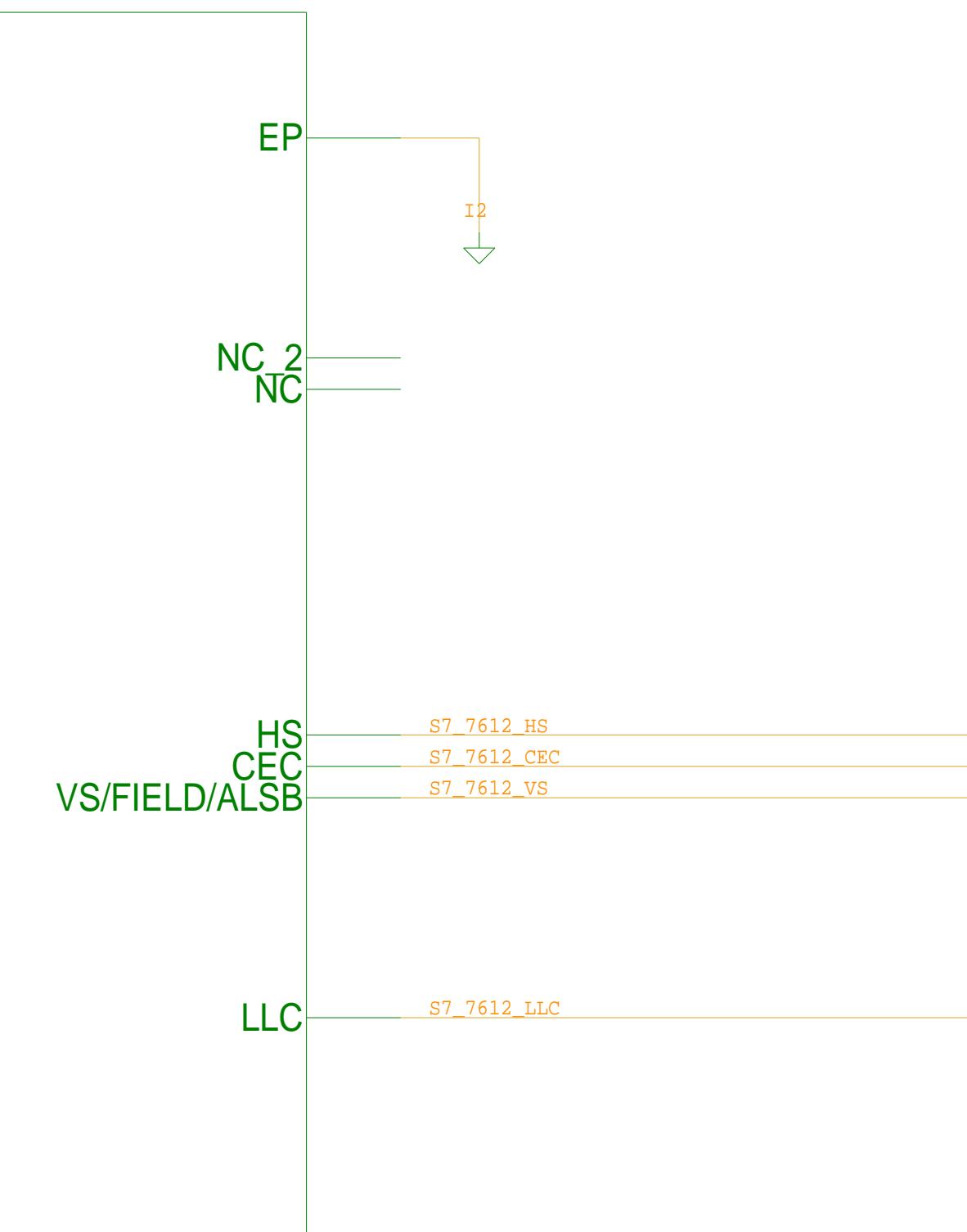
SPARTAN-7 HDMI RECEIVER (2)

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPR.

S7_7612_P0
S7_7612_P1
S7_7612_P2
S7_7612_P3
S7_7612_P4
S7_7612_P5
S7_7612_P6
S7_7612_P7
S7_7612_P8
S7_7612_P9
S7_7612_P10
S7_7612_P11
S7_7612_P12
S7_7612_P13
S7_7612_P14
S7_7612_P15
S7_7612_P16
S7_7612_P17
S7_7612_P18
S7_7612_P19
S7_7612_P20
S7_7612_P21
S7_7612_P22
S7_7612_P23
S7_7612_P24
S7_7612_P25
S7_7612_P26
S7_7612_P27
S7_7612_P28
S7_7612_P29
S7_7612_P30
S7_7612_P31
S7_7612_P32
S7_7612_P33
S7_7612_P34
S7_7612_P35

P0
P1
P2
P3
P4
P5
P6
P7
P8
P9
P10
P11
P12
P13
P14
P15
P16
P17
P18
P19
P20
P21
P22
P23
P24
P25
P26
P27
P28
P29
P30
P31
P32
P33
P34
P35

?



CADENCE DESIGN SYSTEMS, INC.
 CADENCE

THIS DOCUMENT CONTAINS INFORMATION PROPRIETARY
TO CADENCE DESIGN SYSTEMS INC (CADENCE). USE
OR DISCLOSURE WITHOUT THE WRITTEN PERMISSION OF AN
OFFICER OF CADENCE IS EXPRESSLY FORBIDDEN.
COPYRIGHT (C) CADENCE 1988

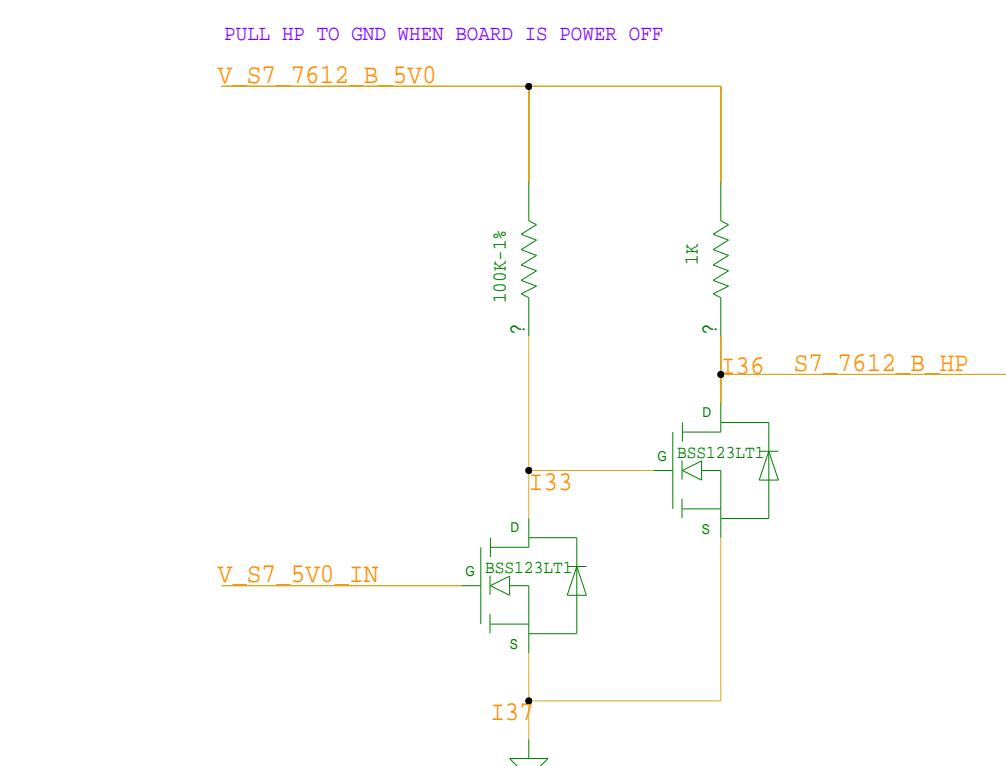
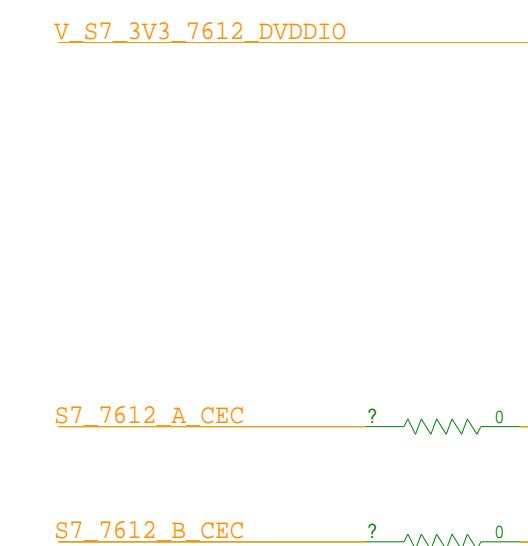
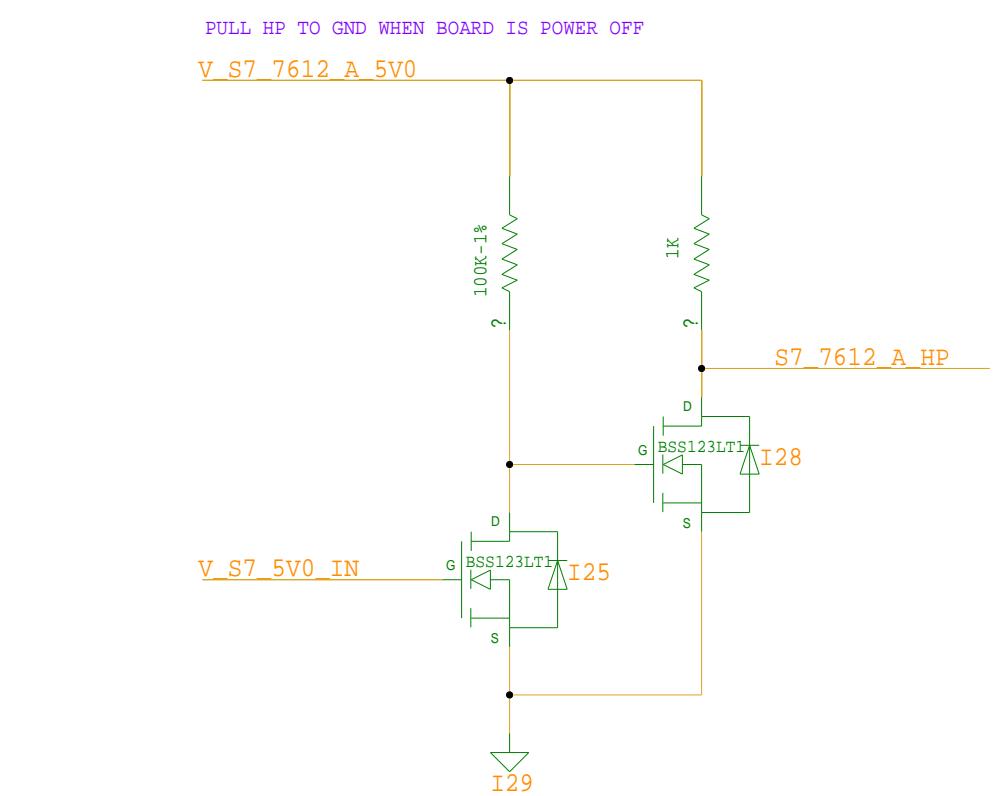
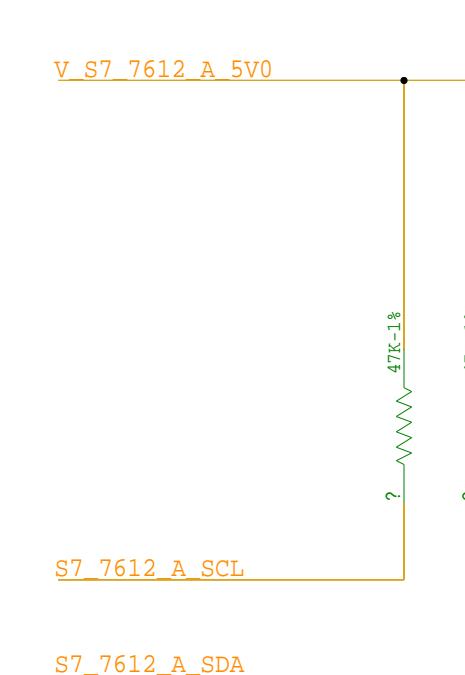
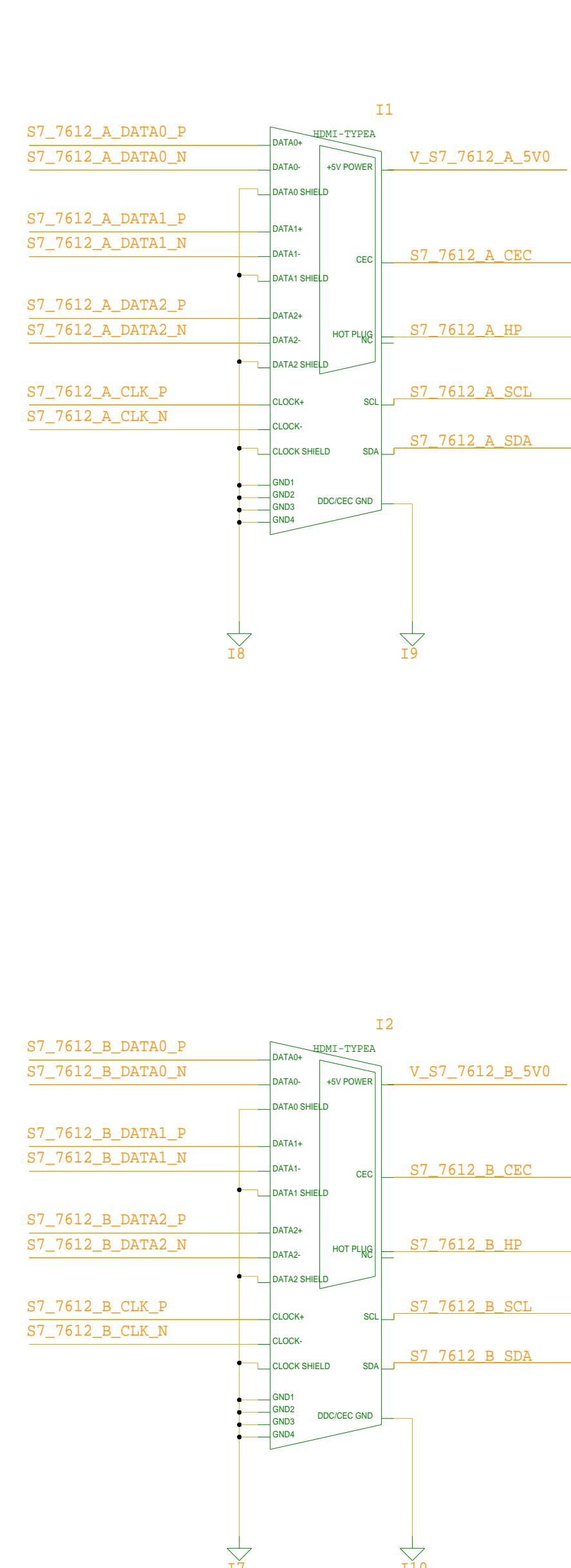
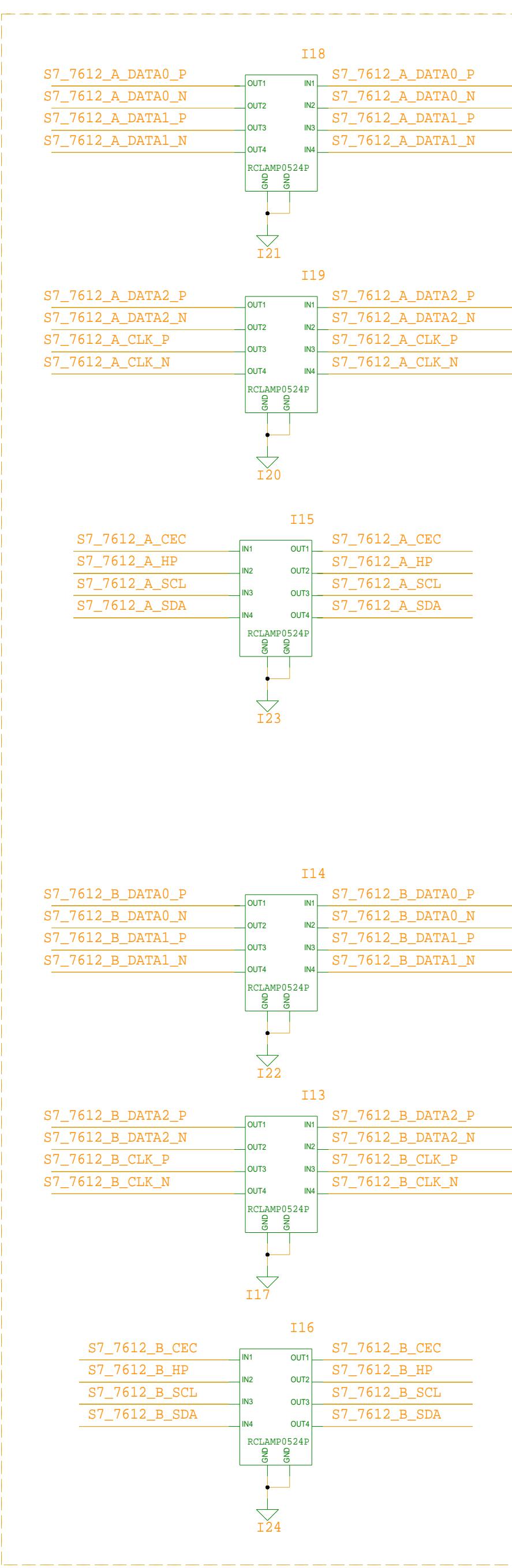
DRAWING TITLE		
SIZE	REV.	DRAWING NO.
SCALE		SHEET OF

REVISED

ZONE	LTR	DESCRIPTION	DATE	APPR.

SPARTAN-7 HDMI RECEIVER (3)

CHANGE CONNECTION DUE TO LAYOUT

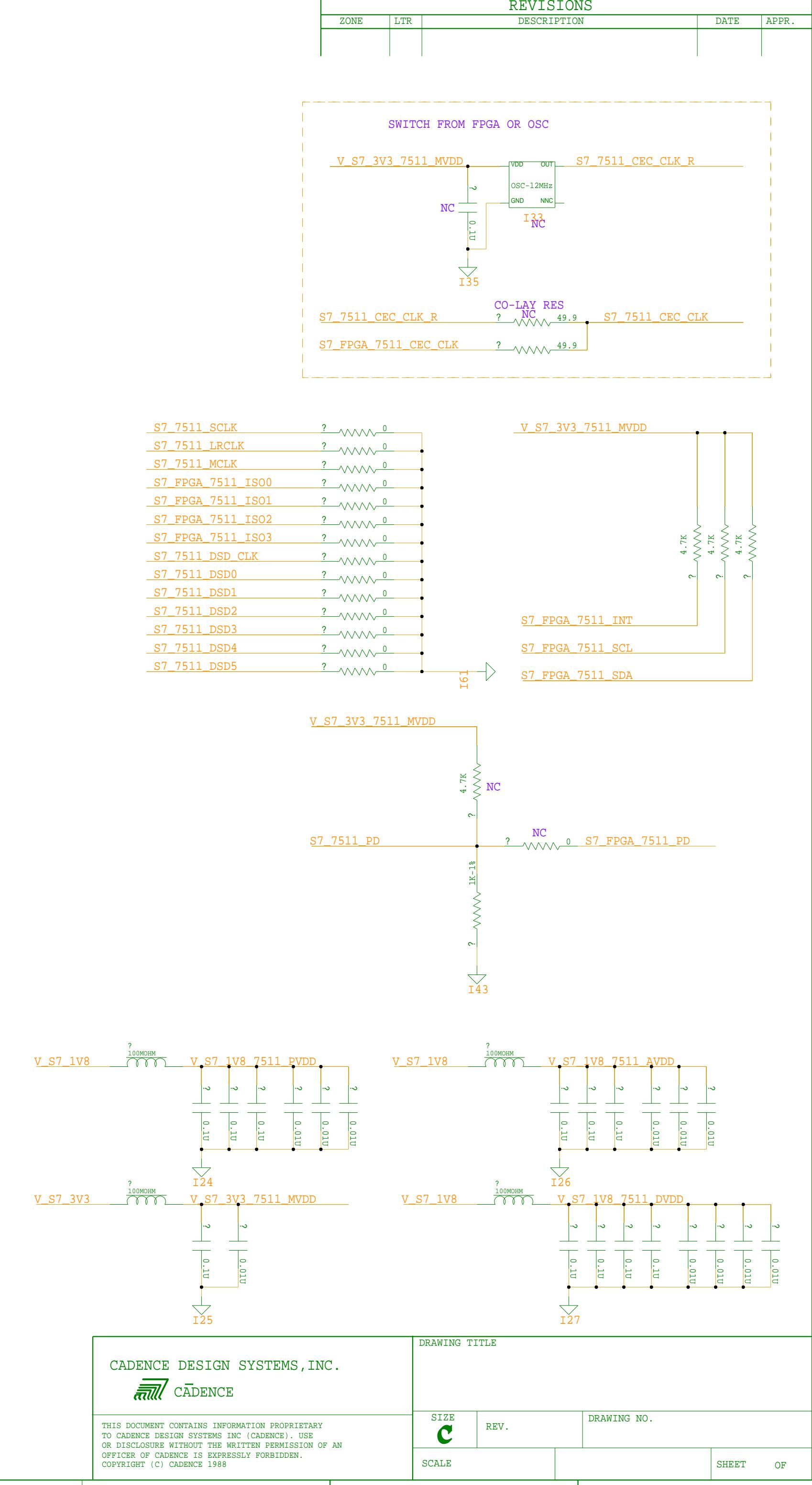
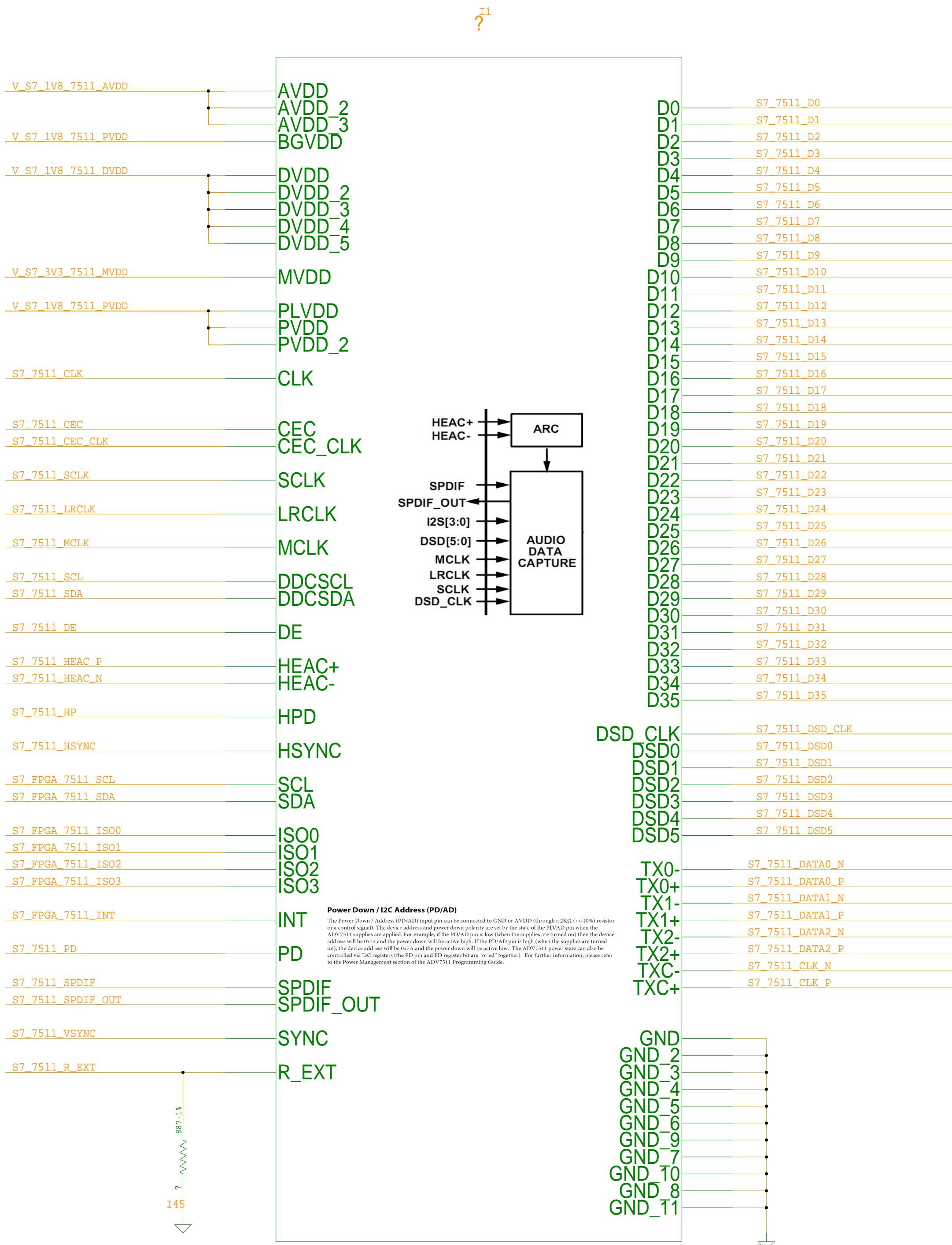


CADENCE DESIGN SYSTEMS, INC.


THIS DOCUMENT CONTAINS INFORMATION PROPRIETARY
 TO CADENCE DESIGN SYSTEMS INC (CADENCE). USE
 OR DISCLOSURE WITHOUT THE WRITTEN PERMISSION OF AN
 OFFICER OF CADENCE IS EXPRESSLY FORBIDDEN.
 COPYRIGHT (C) CADENCE 1988

DRAWING TITLE		SIZE		REV.		DRAWING NO.	
		SCALE	OF				

SPARTAN-7 HDMI TRANSMITTER (1)

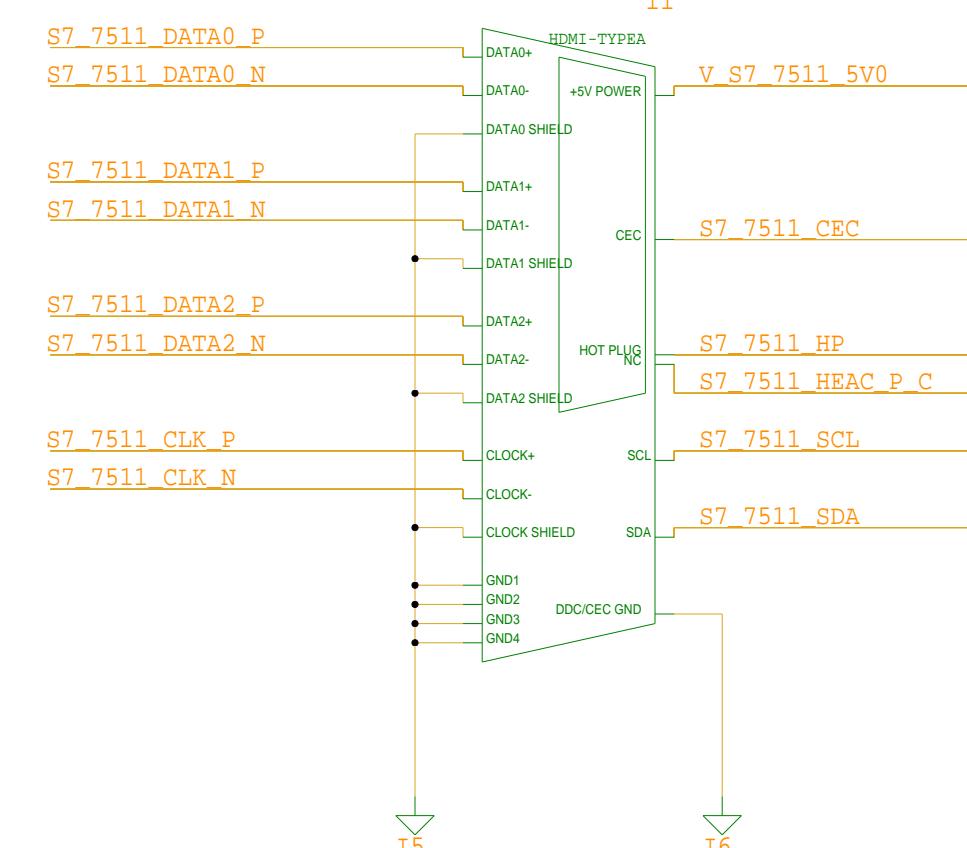
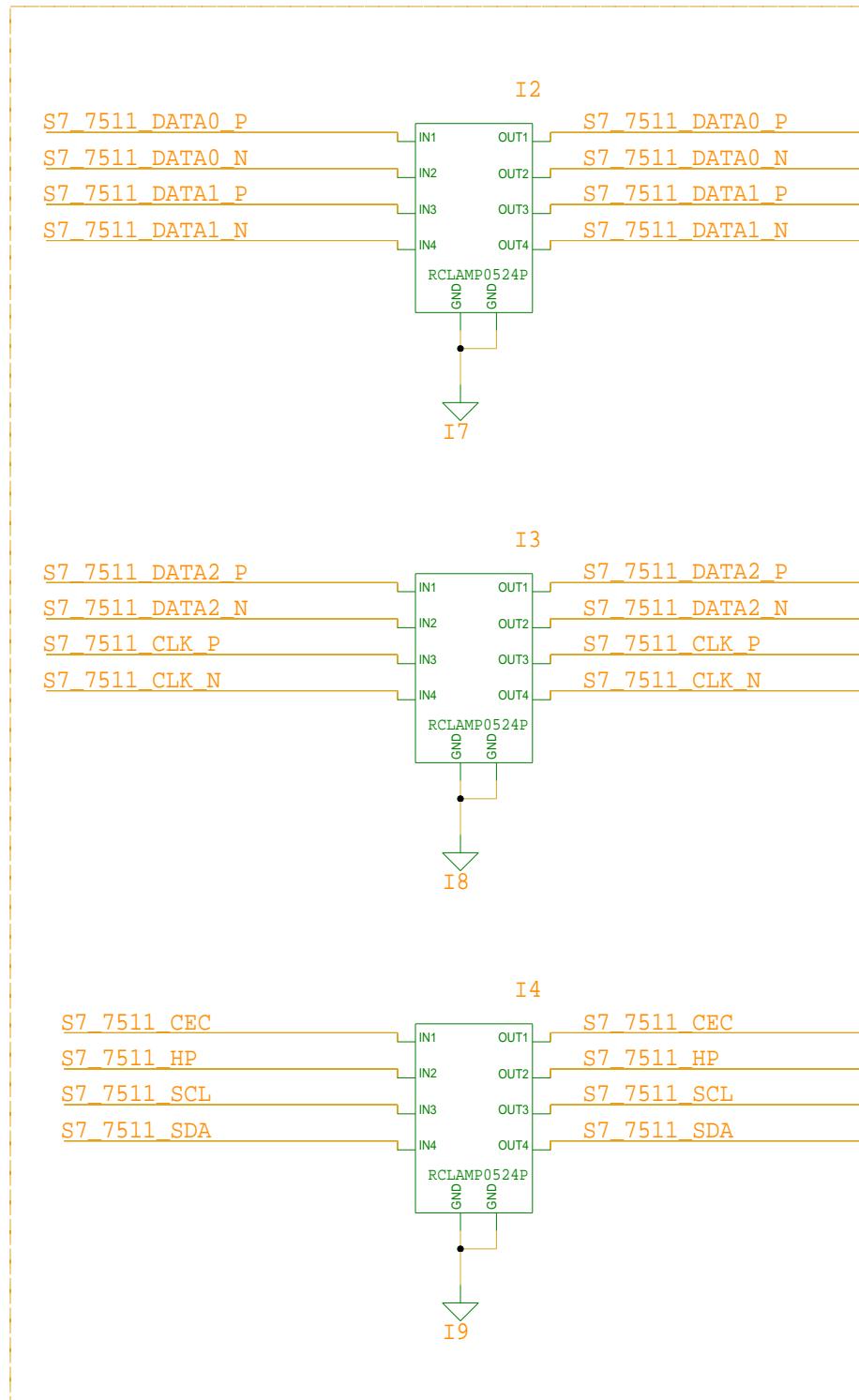


SPARTAN-7 HDMI TRANSMITTER (2)

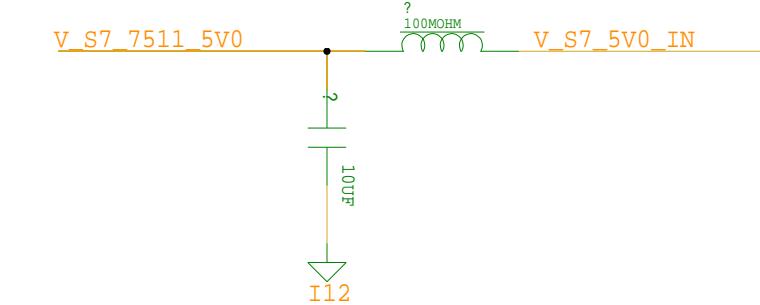
REVISONS

ZONE	LTR	DESCRIPTION	DATE	APPR.

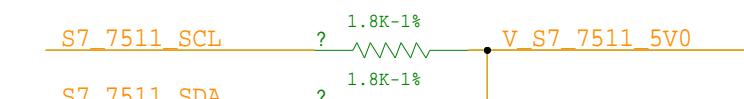
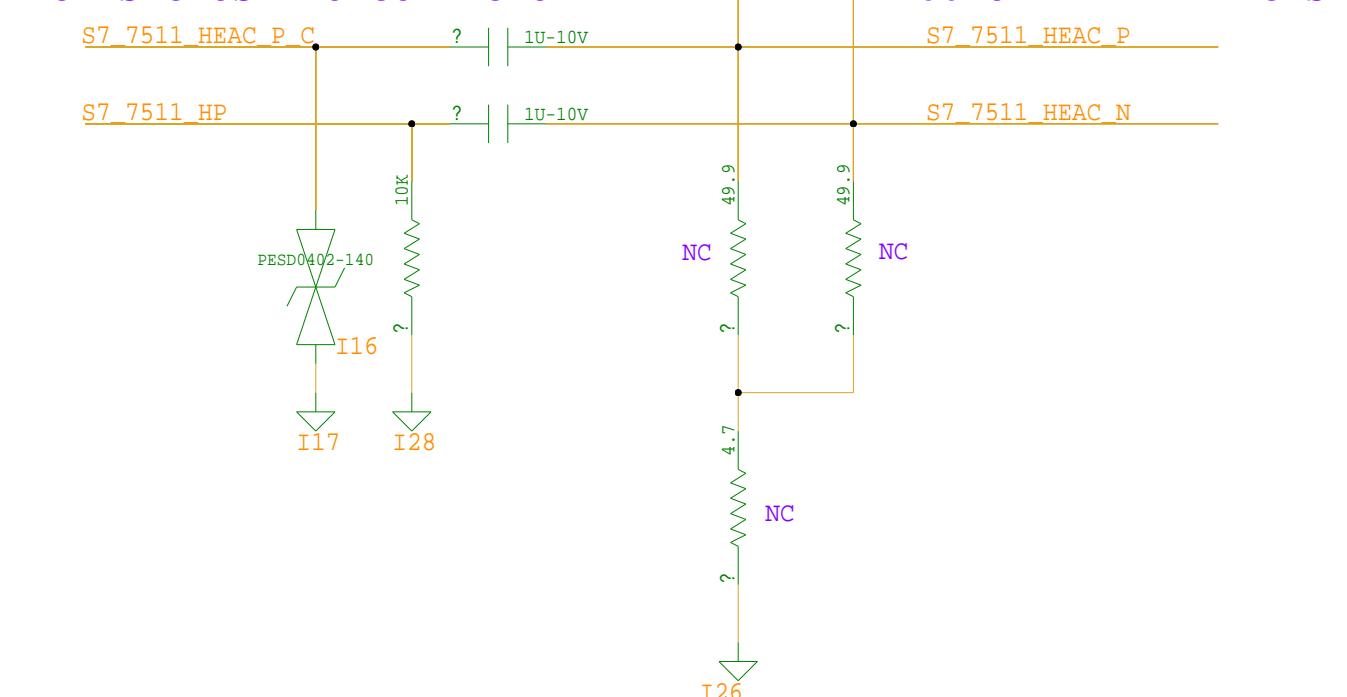
CHANGE CONNECTION DUE TO LAYOUT



CLOSE TO HDMI CONNECTOR



CAPS CLOSE TO CONNECTOR



CADENCE DESIGN SYSTEMS, INC.



THIS DOCUMENT CONTAINS INFORMATION PROPRIETARY
TO CADENCE DESIGN SYSTEMS INC (CADENCE). USE
OR DISCLOSURE WITHOUT THE WRITTEN PERMISSION OF AN
OFFICER OF CADENCE IS EXPRESSLY FORBIDDEN.
COPYRIGHT (C) CADENCE 1988

DRAWING TITLE

SIZE	REV.	DRAWING NO.
C		

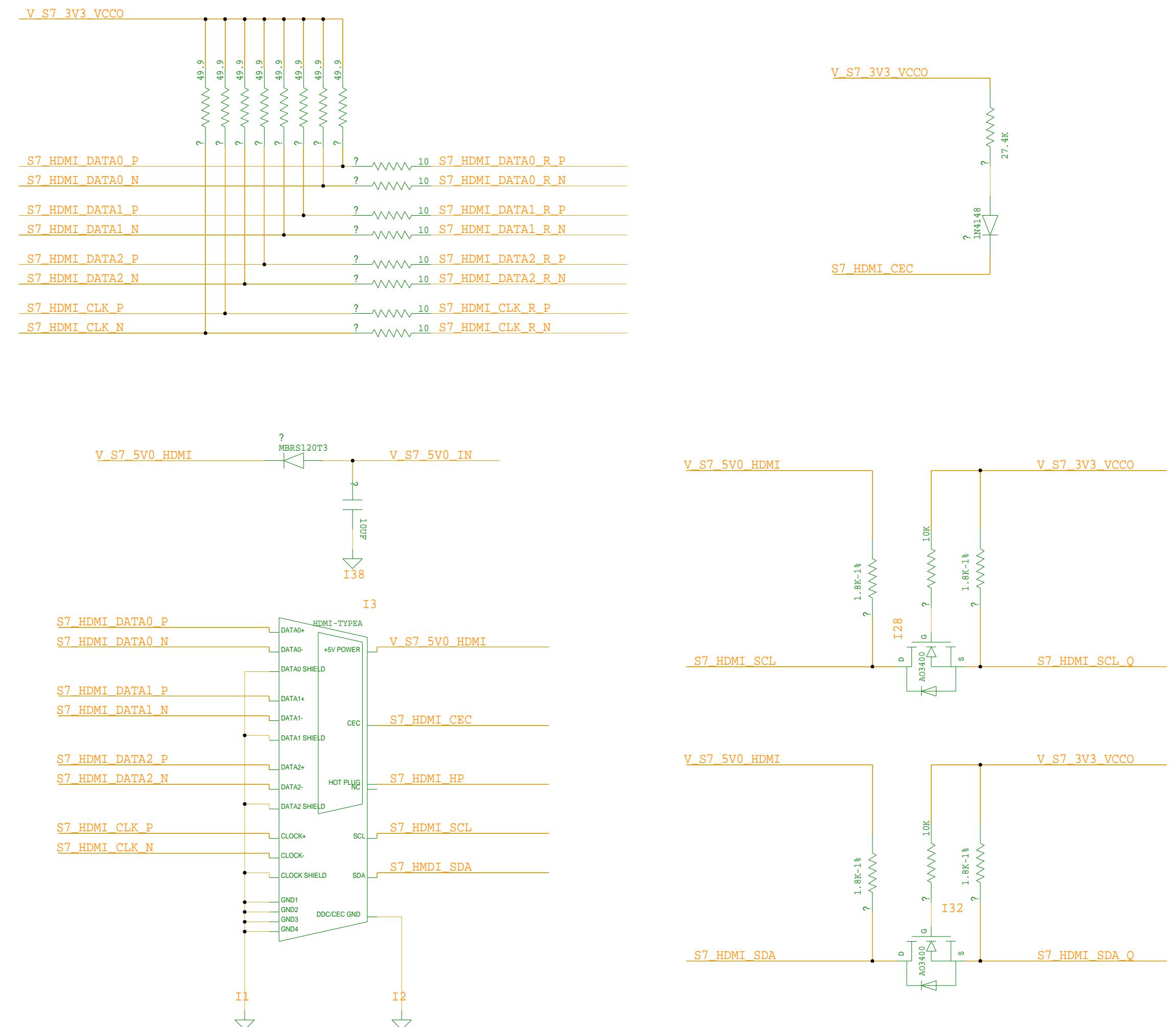
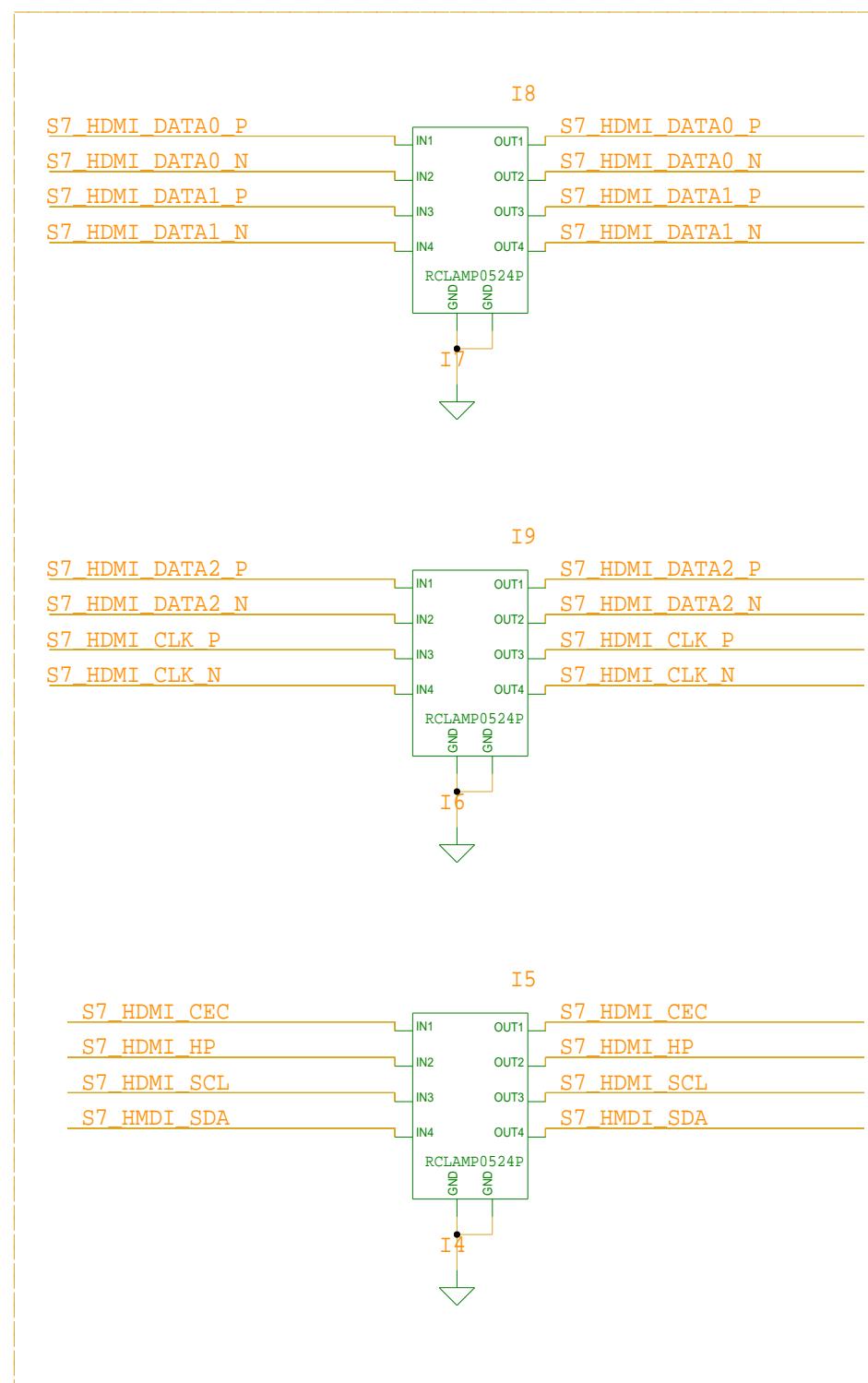
SCALE

SHEET OF

ZONE	LTR	DESCRIPTION	DATE	APPR.

SPARTAN-7 HDMI INOUT

CHANGE CONNECTION DUE TO LAYOUT



CADENCE DESIGN SYSTEMS, INC.
CADENCE

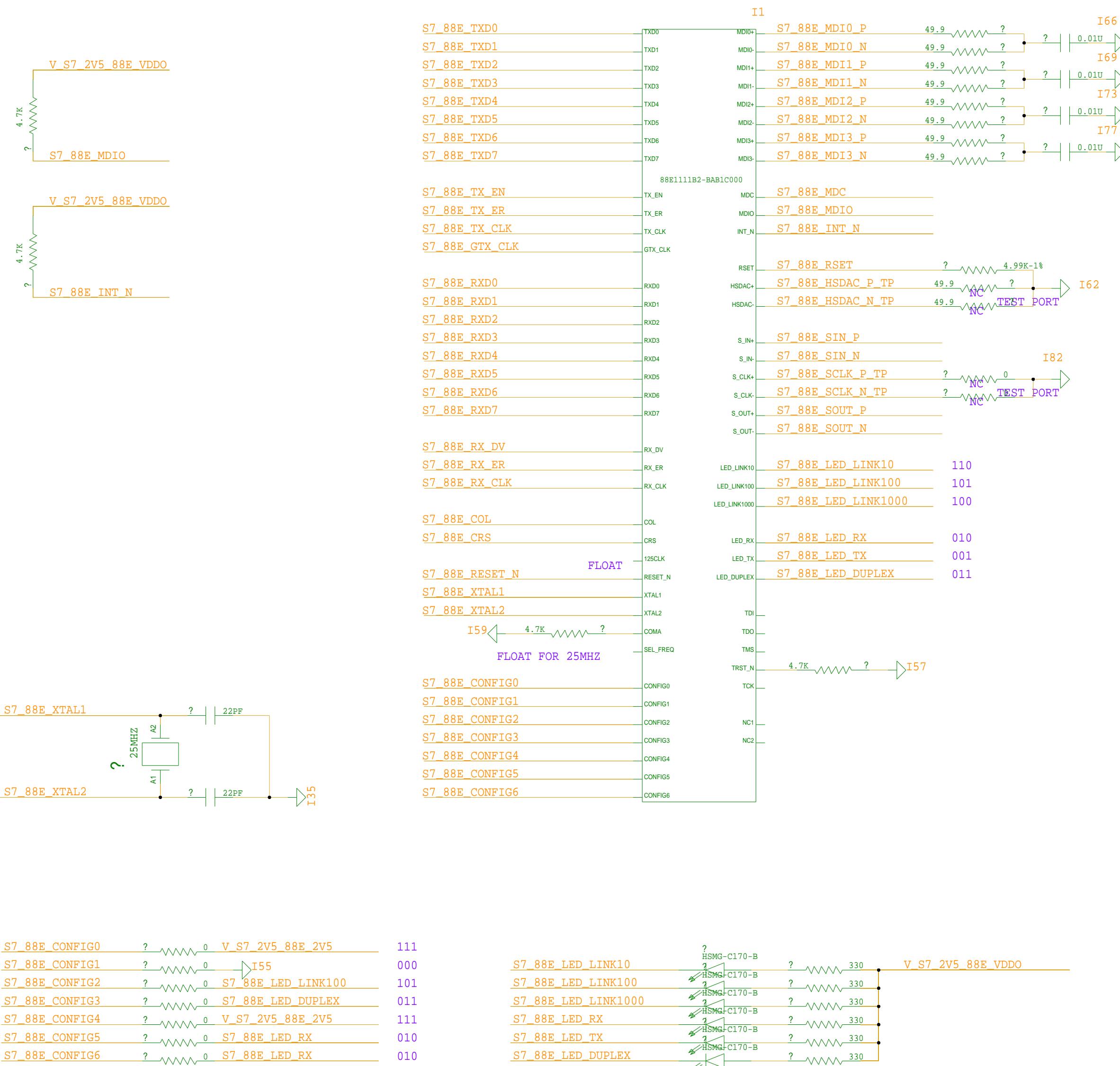
THIS DOCUMENT CONTAINS INFORMATION PROPRIETARY
TO CADENCE DESIGN SYSTEMS INC (CADENCE). USE
OR DISCLOSURE WITHOUT THE WRITTEN PERMISSION OF AN
OFFICER OF CADENCE IS EXPRESSLY FORBIDDEN.
COPYRIGHT (C) CADENCE 1988

DRAWING TITLE		SIZE		REV.		DRAWING NO.	
SCALE	OF	REV.	SIZE	DRAWING NO.	OF	SCALE	OF

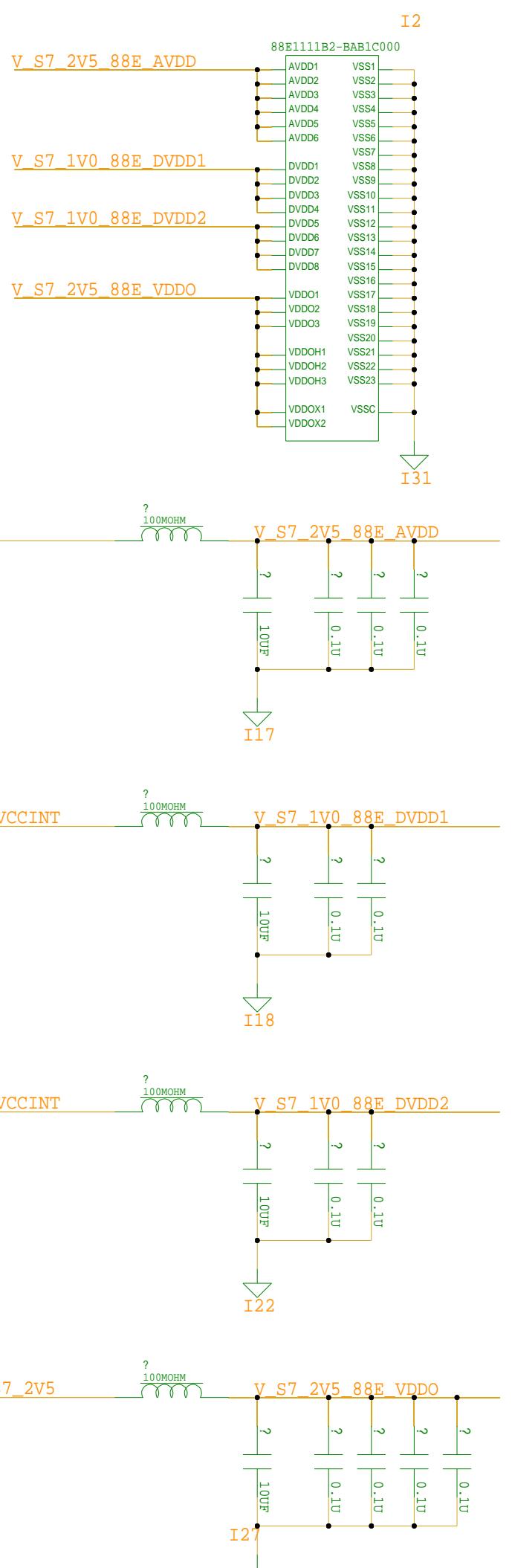
SPARTAN-7 SFP PHY (1)

REVISIONS

ZONE	LTR	DESCRIPTION	DATE	APPR.



PIN	CONNECTION	BACKUP	REG	VALUE	BACKUP	CONFIGURATION
CONFIG0	VDD	GND	PHYADR[2:0]	111	000	PHYADR=111
CONFIG1	GND	LED_LINK1000	ENA_PAUSE/PHYADR[4:3]	000	100	Disable PAUSE frame, PHYADR=00
CONFIG2	VDD		ANEG[3:1]	101	111	Fiber, force 1000BASE-X full-duplex
CONFIG3	LED_DUPLEX		ANEG[0]/ENA_XC/DIS_125	011		Crossover Enable, Disable 125MHz
CONFIG4	VDD	LED_DUPLEX	HWCFG_MODE[2:0]	111	011	GMII to Fiber 0111
CONFIG5	LED_RX	LED_LINK10	DIS_FC/DIS_SLEEP/HWCFG_MODE[3]	010	110	Enable FC/Copper, Disable Sleep
CONFIG6	LED_RX	LED_LINK10	SEL_TWSI/INT_POL/75_500HM	010	110	MDI/MDC, INT low, 50 ohm serdes



NOTE:
VDDO is used for the MAC interface I/O pins.
There is one supply option for VDDO: 2.5V.

NOTE:
VDDO is used for the LED CONFIG, XTAL1, XTAL2, and SEL_FREQ pin power.
VDDO supports 2.5V.

NOTE:
VDDO is used for MDI/MDIO/INT/125CLK/RESETn/TAG4 pin power.
This supply supports 2.5V.

NOTE:
AVDD is used for the analog high digital logic.
AVDD is used as the 2.5V analog supply.

NOTE:
DVDD is used for the digital logic.
DVDD is the 1.0V digital supply.
1.2V can be used instead of 1V.

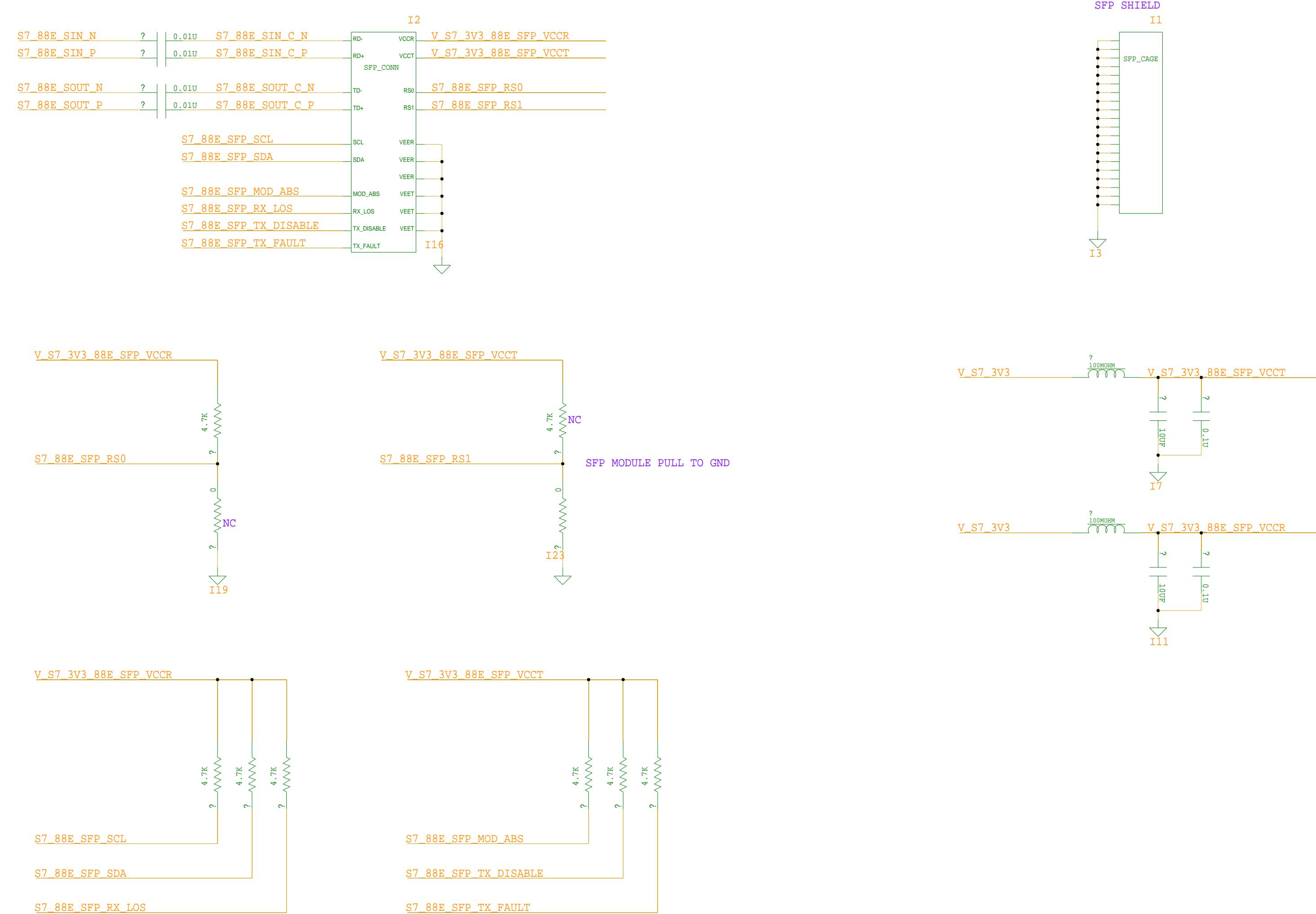
CADENCE DESIGN SYSTEMS, INC.

DRAWING TITLE		SIZE		DRAWING NO.	
SCALE	REV.				

SPARTAN-7 SFP PHY (2)

REVISIONS

ZONE	LTR	DESCRIPTION	DATE	APPR.



CADENCE DESIGN SYSTEMS, INC.
CADENCE

THIS DOCUMENT CONTAINS INFORMATION PROPRIETARY
TO CADENCE DESIGN SYSTEMS INC (CADENCE). USE
OR DISCLOSURE WITHOUT THE WRITTEN PERMISSION OF AN
OFFICER OF CADENCE IS EXPRESSLY FORBIDDEN.
COPYRIGHT (C) CADENCE 1988

DRAWING TITLE

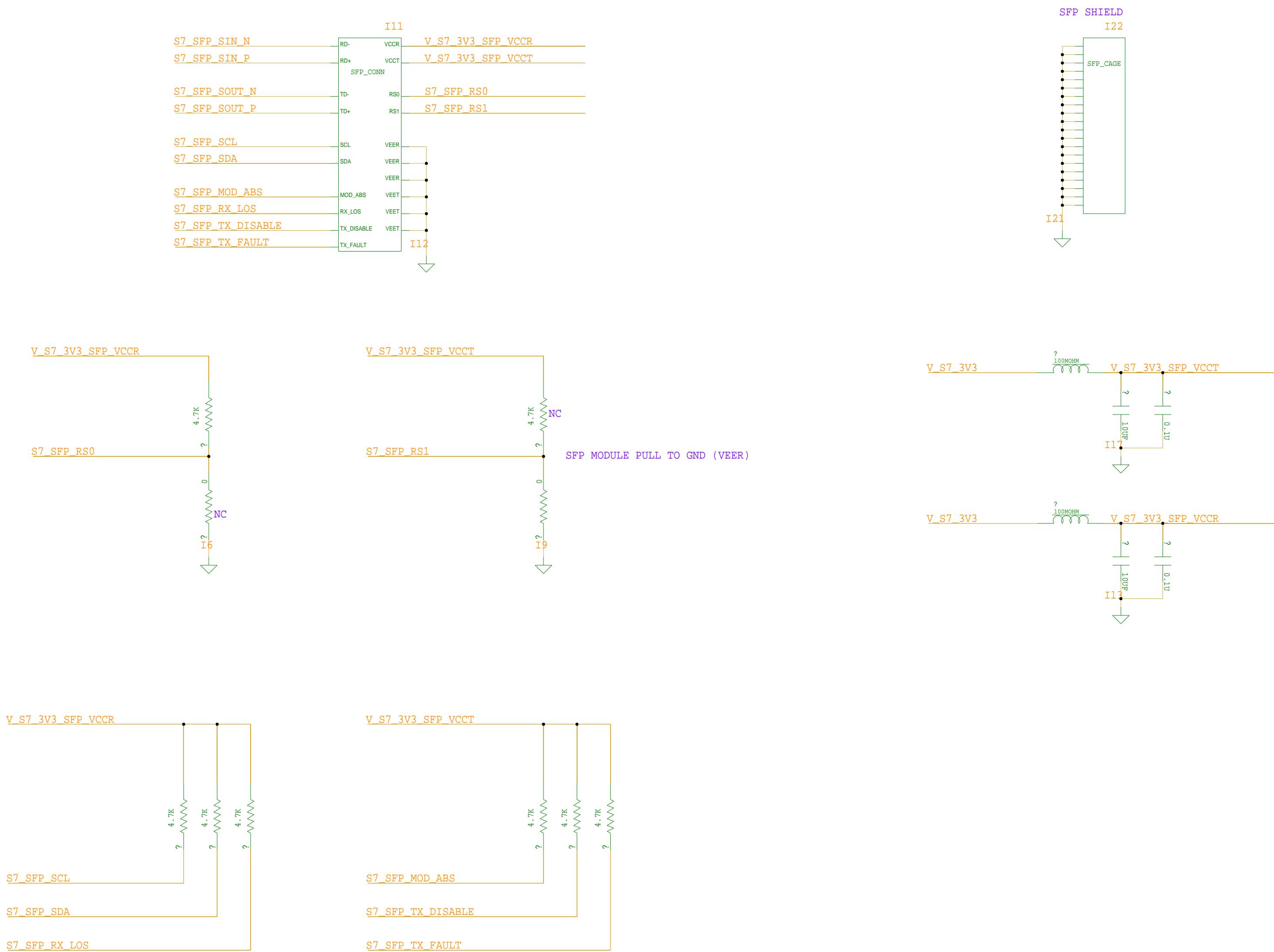
SIZE	REV.	DRAWING NO.
C		

SCALE SHEET OF

SPARTAN-7 SFP INOUT

REVOLUTIONS

ZONE	LTR	DESCRIPTION	DATE	APPR.



CADENCE DESIGN SYSTEMS, INC.
 CADENCE

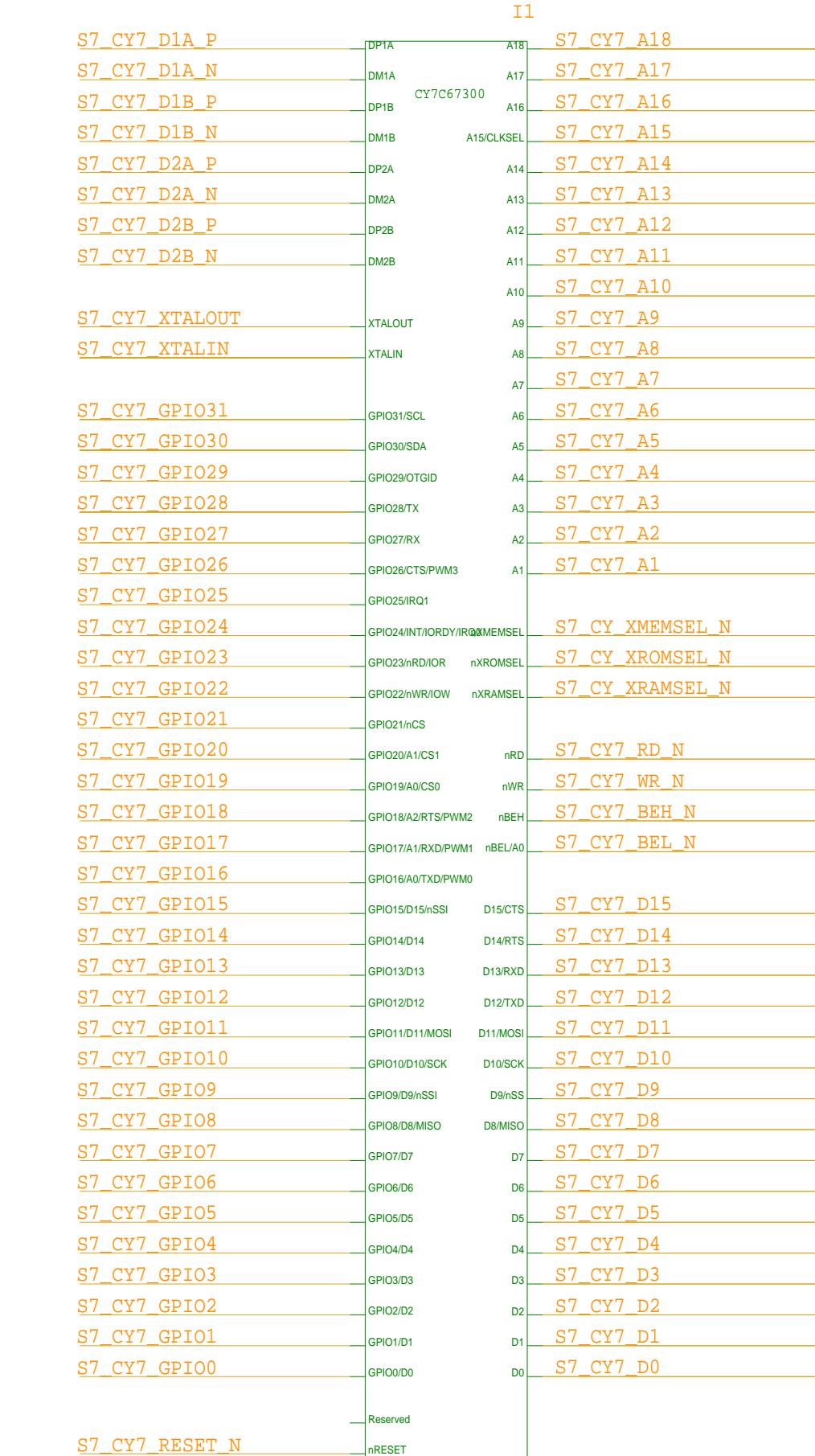
THIS DOCUMENT CONTAINS INFORMATION PROPRIETARY
 TO CADENCE DESIGN SYSTEMS INC (CADENCE). USE
 OR DISCLOSURE WITHOUT THE WRITTEN PERMISSION OF AN
 OFFICER OF CADENCE IS EXPRESSLY FORBIDDEN.
 COPYRIGHT (C) CADENCE 1988

DRAWING TITLE		SIZE		REV.		DRAWING NO.	
		C					

SPARTAN-7 USB CONTROLLER (1)

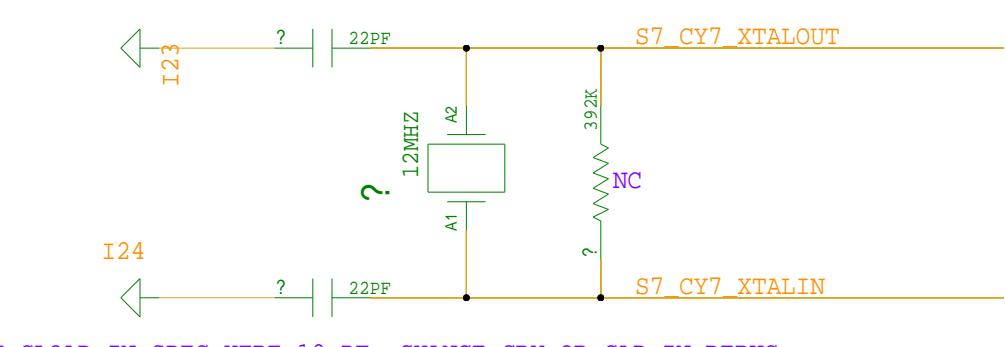
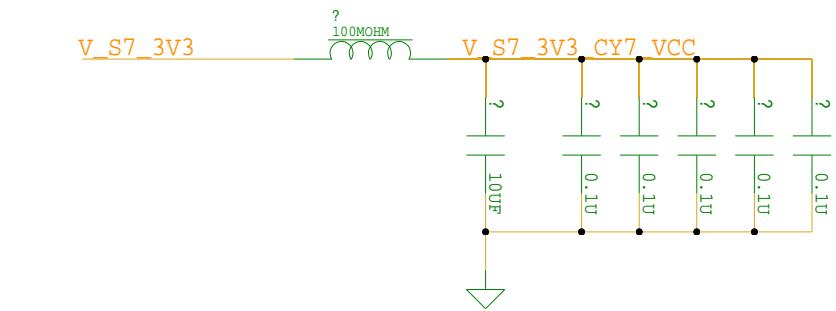
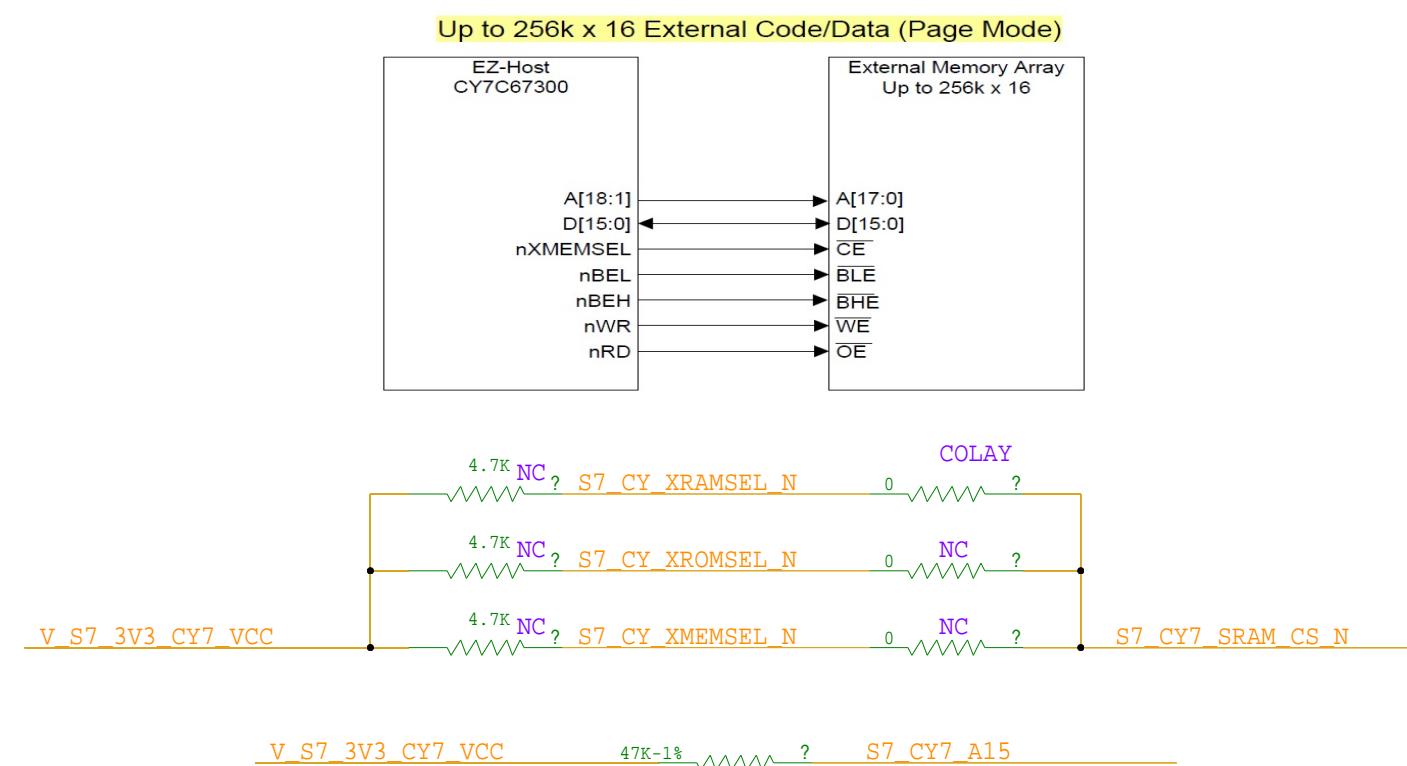
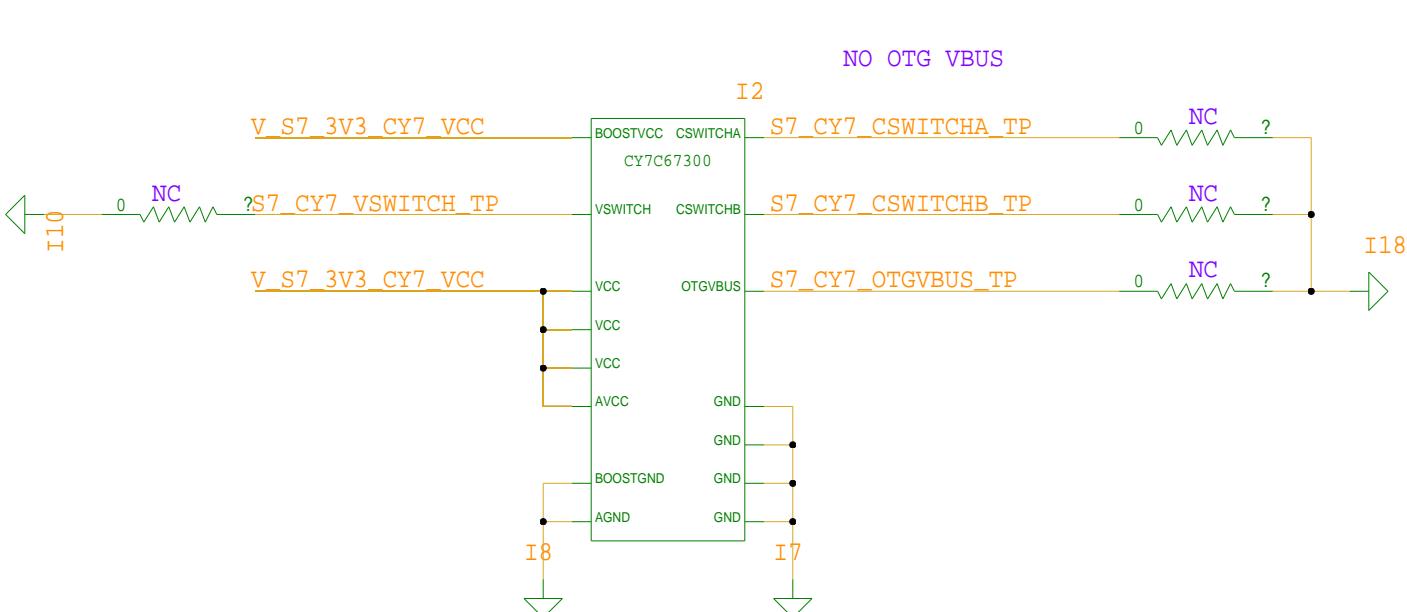
REVISED

ZONE	LTR	DESCRIPTION	DATE	APPR.

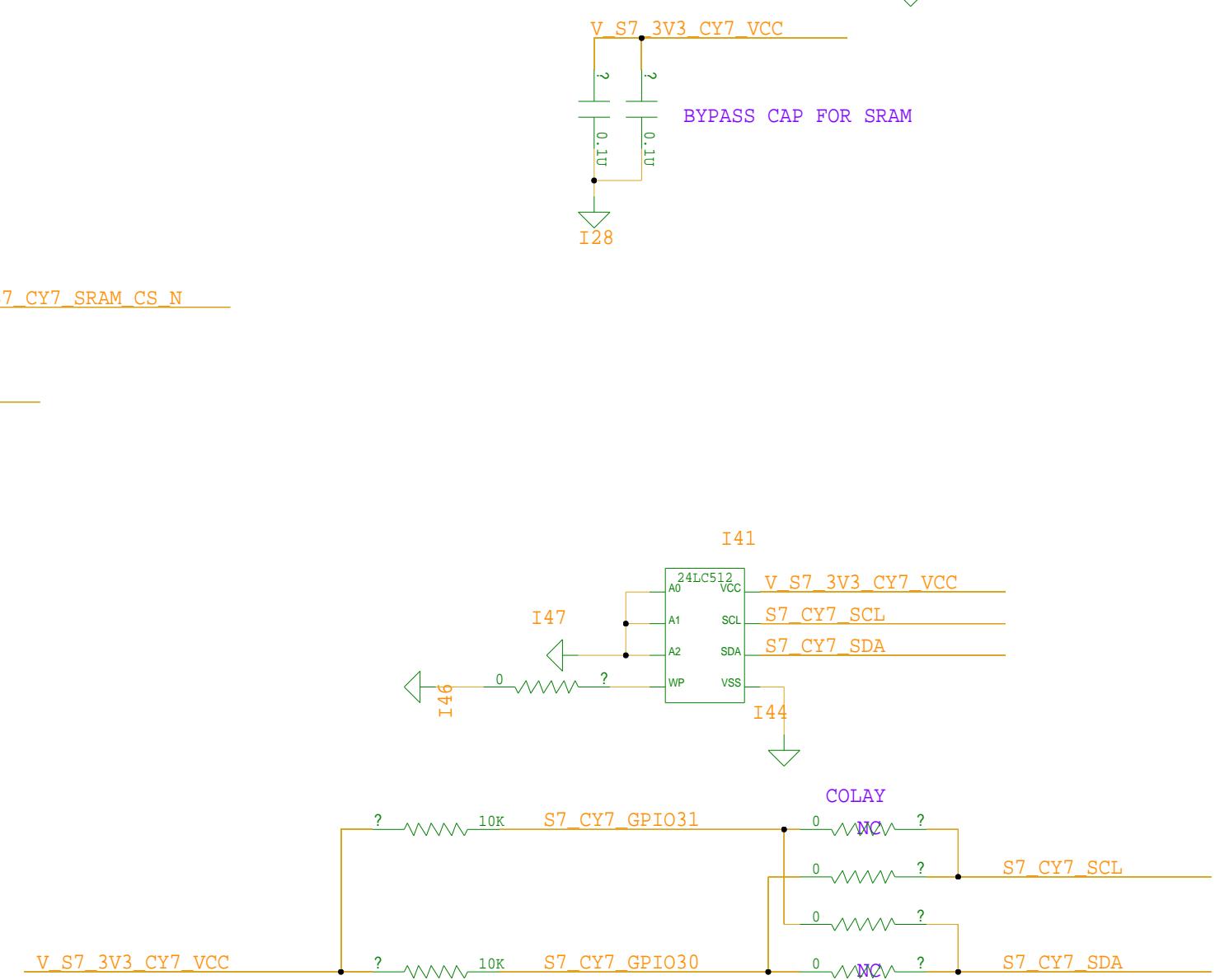
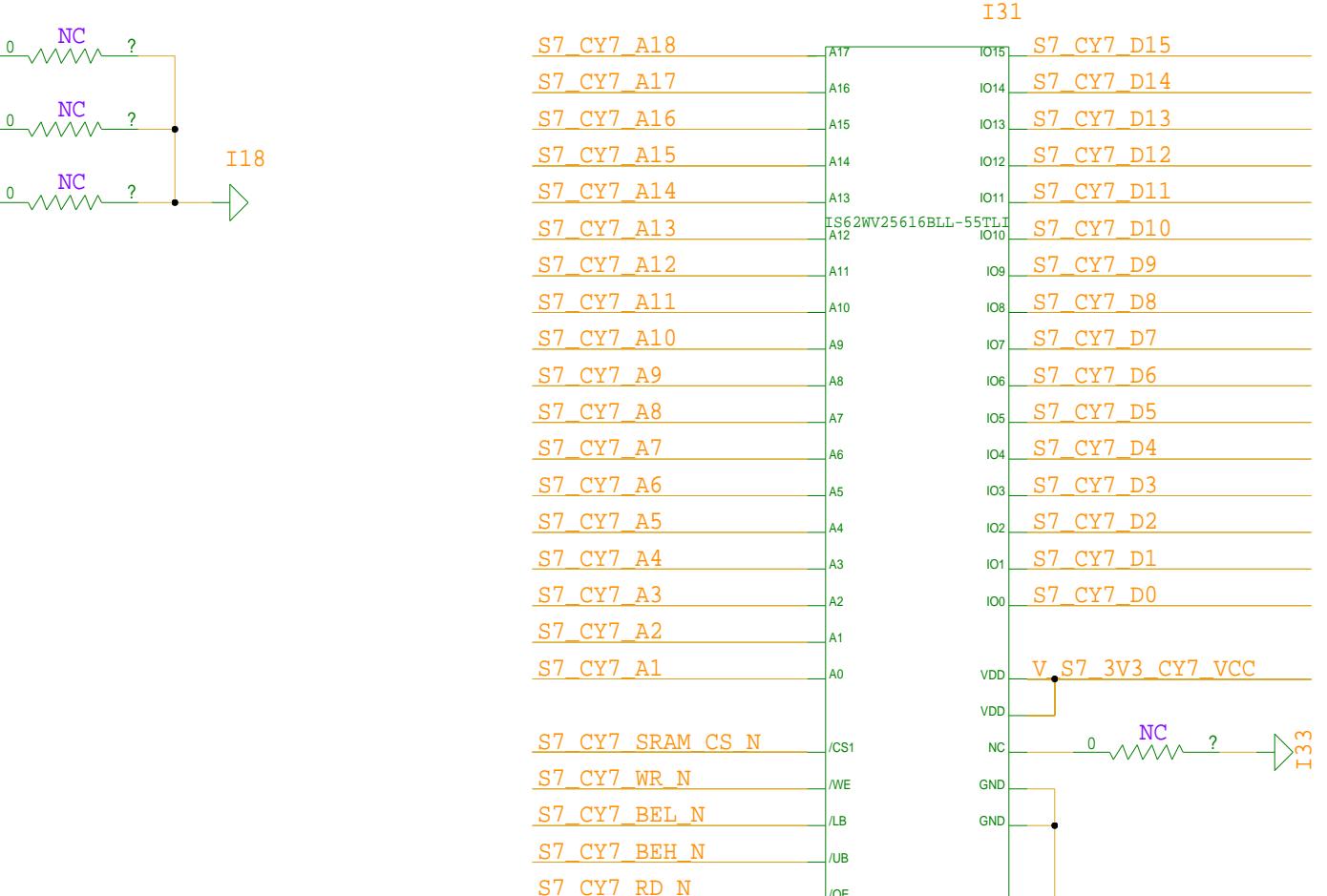


Standalone Mode
In standalone mode, there is no external processor connected to EZ-Host. Instead, EZ-Host's own internal 16-bit CPU is the main processor and firmware is typically downloaded from an EEPROM. Optionally, firmware may also be downloaded via USB. See Table 19 for booting into standalone mode.
After booting into standalone mode (GPIO[31:30] = '11'), the following pins are active:

- GPIO[31:30] are configured as output pins to examine the EEPROM contents
- GPIO[28:27] are enabled for debug UART mode
- GPIO[29] is configured for OTGID for OTG applications on PORT1A
 - If OTGID is logic 1 then PORT1A (OTG) is configured as a USB peripheral
 - If OTGID is logic 0 then PORT1A (OTG) is configured as a USB host
- Ports 1B, 2A, and 2B default as USB peripheral ports
- All other pins remain INPUT pins.



20~33PF CLOAD IN SPEC, HERE 10 PF. CHANGE CRY OR CAP IN DEBUG.



*GPIO[31:30] 31 30
Up to 2k x8 SCL SDA
>2k x8 to 64k x8 SDA SCL

CADENCE DESIGN SYSTEMS, INC.
CADENCE

THIS DOCUMENT CONTAINS INFORMATION PROPRIETARY
TO CADENCE DESIGN SYSTEMS INC (CADENCE). USE
OR DISCLOSURE WITHOUT THE WRITTEN PERMISSION OF AN
OFFICER OF CADENCE IS EXPRESSLY FORBIDDEN.
COPYRIGHT (C) CADENCE 1988

SIZE	REV.	DRAWING NO.
8	7	6

SPARTAN-7 USB CONTROLLER (2)

REVISED

ZONE

LTR

DESCRIPTION

DATE

APPR.

Port Configurations	Port 1A	Port 1B	Port 2A	Port 2B
2 Hosts + 1 Peripheral	Host	Host	Peripheral	-
2 Peripherals	-	Peripheral	-	Peripheral



CADENCE DESIGN SYSTEMS, INC.



THIS DOCUMENT CONTAINS INFORMATION PROPRIETARY
TO CADENCE DESIGN SYSTEMS INC (CADENCE). USE
OR DISCLOSURE WITHOUT THE WRITTEN PERMISSION OF AN
OFFICER OF CADENCE IS EXPRESSLY FORBIDDEN.
COPYRIGHT (C) CADENCE 1988

DRAWING TITLE

SIZE

REV.

DRAWING NO.

SCALE

SHEET

OF

SPARTAN-7 USB INOUT

REVISIONS

ZONE	LTR	DESCRIPTION	DATE	APPR.

USB IP CORE DOSEN'T SUPPORT SPARTAN-7

CADENCE DESIGN SYSTEMS, INC.
 CADENCE

THIS DOCUMENT CONTAINS INFORMATION PROPRIETARY
TO CADENCE DESIGN SYSTEMS INC (CADENCE). USE
OR DISCLOSURE WITHOUT THE WRITTEN PERMISSION OF AN
OFFICER OF CADENCE IS EXPRESSLY FORBIDDEN.
COPYRIGHT (C) CADENCE 1988

DRAWING TITLE

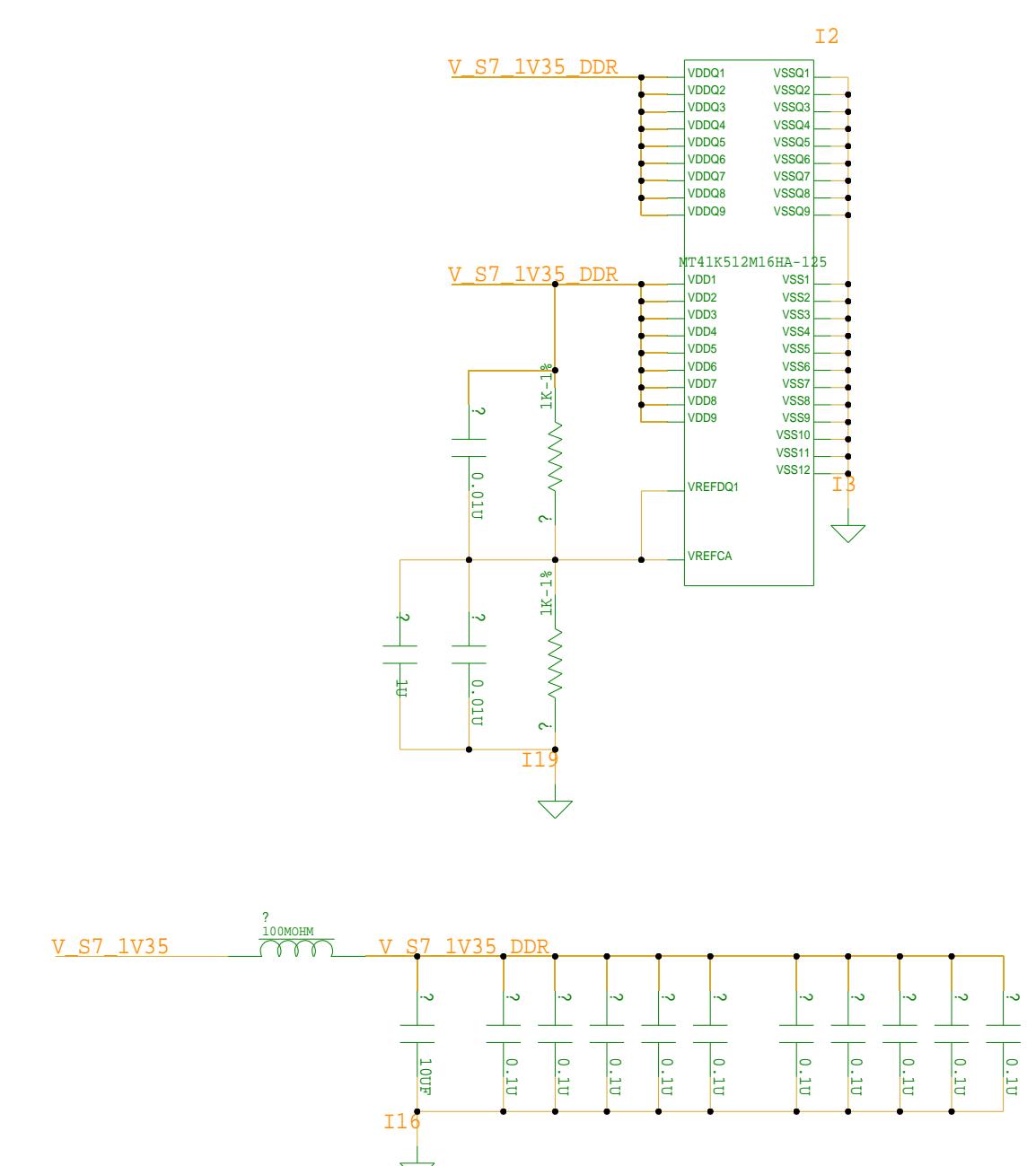
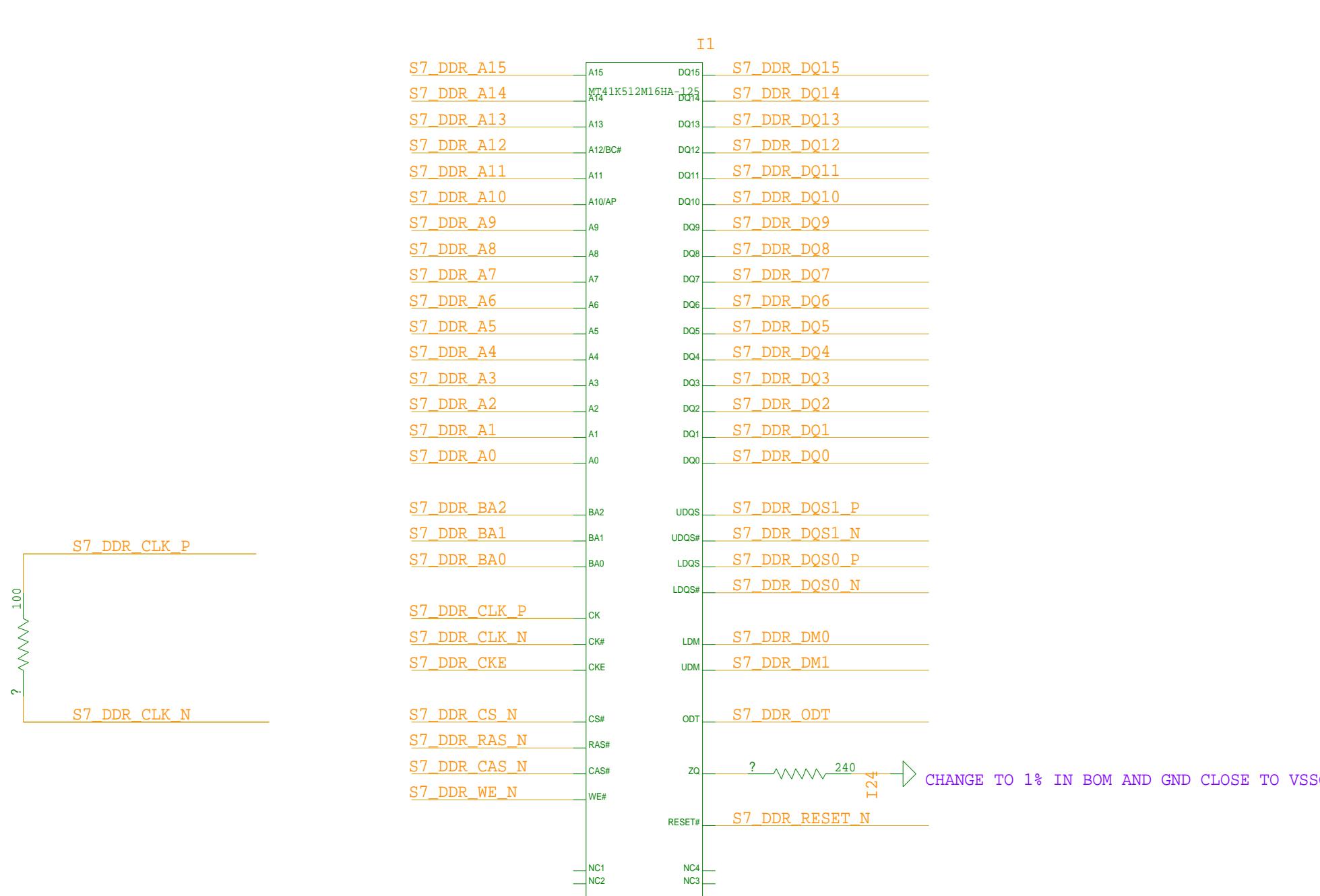
SIZE  REV. DRAWING NO.

SCALE SHEET OF

SPARTAN-7 DDR3

REVISIONS

ZONE	LTR	DESCRIPTION	DATE	APPR.

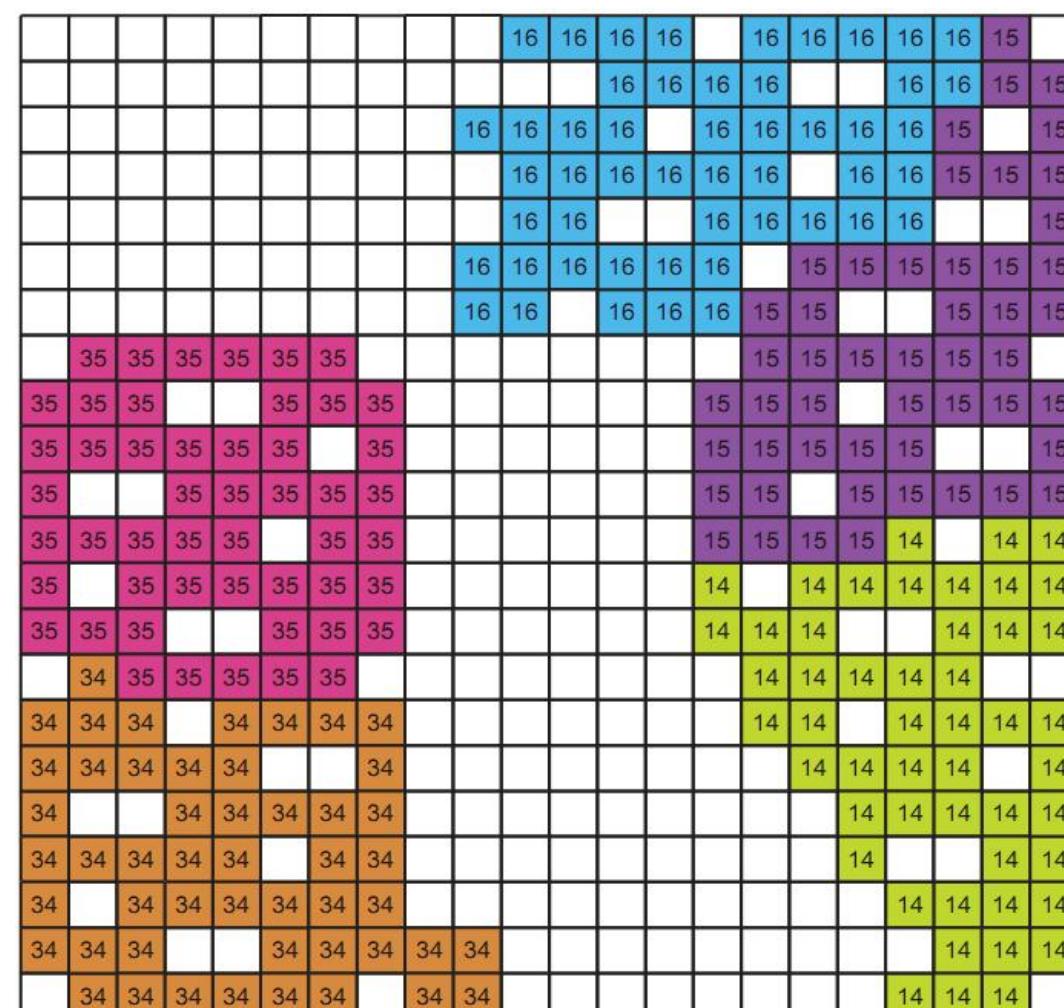


CADENCE DESIGN SYSTEMS, INC.
 CADENCE

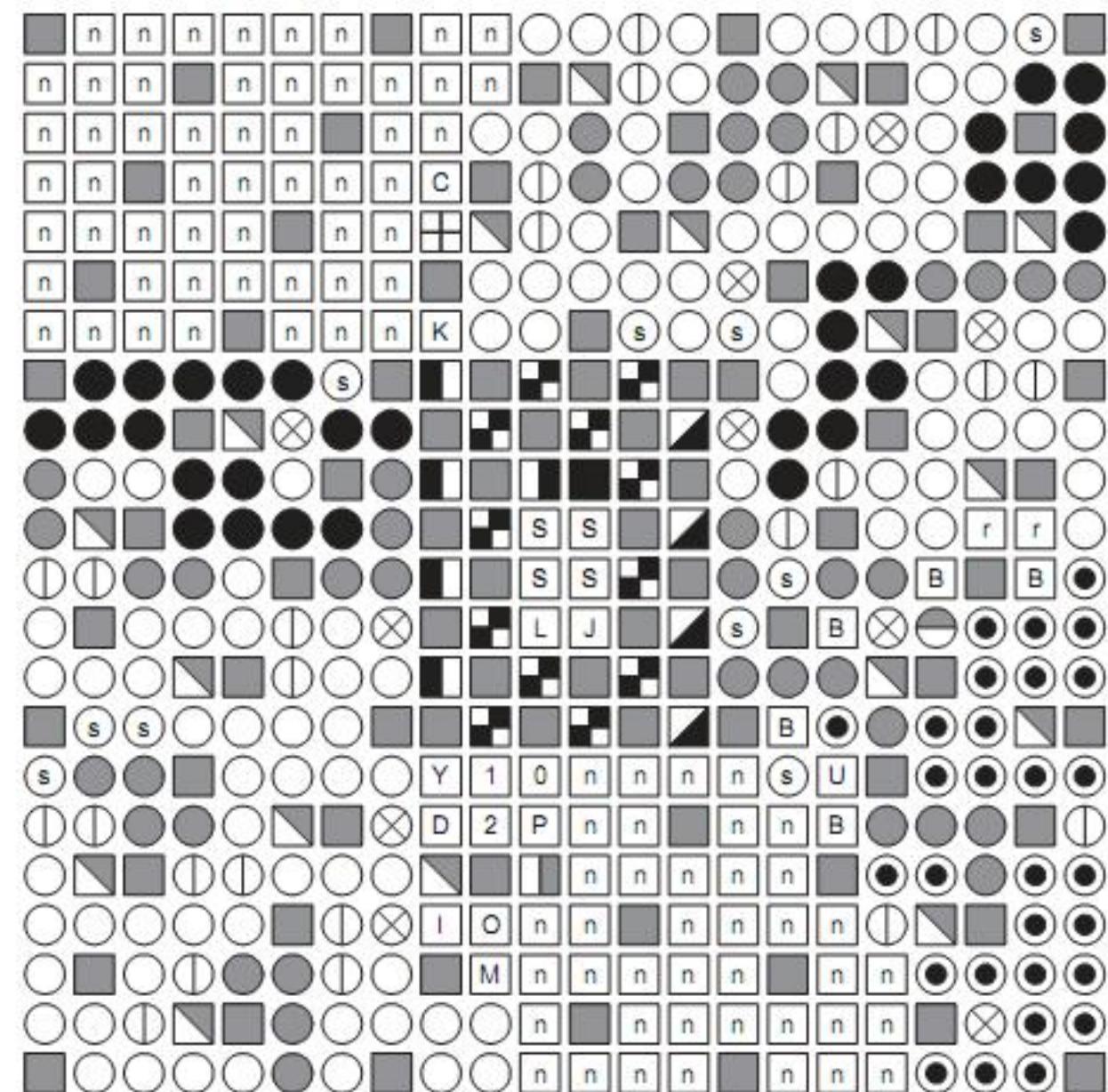
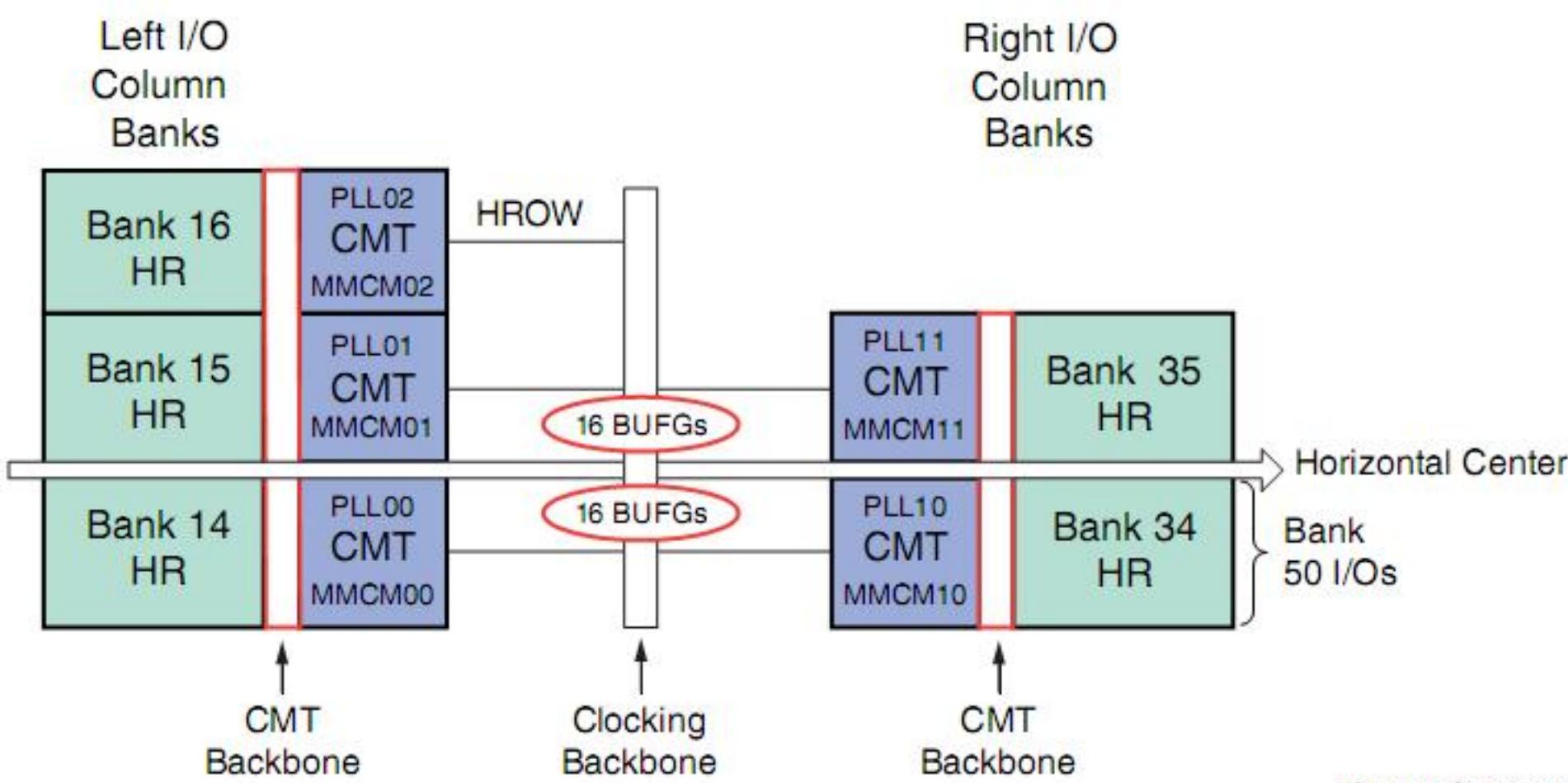
THIS DOCUMENT CONTAINS INFORMATION PROPRIETARY
TO CADENCE DESIGN SYSTEMS INC (CADENCE). USE
OR DISCLOSURE WITHOUT THE WRITTEN PERMISSION OF AN
OFFICER OF CADENCE IS EXPRESSLY FORBIDDEN.
COPYRIGHT (C) CADENCE 1988

DRAWING TITLE		SIZE		REV.		DRAWING NO.	
SCALE	OF	REV.	SIZE	DRAWING NO.	OF	SCALE	OF

SPARTAN-7 PINOUT MAP



BANK0 : 3.3V CONFIG
BANK14 : 3.3V HDMI RECEIVER/ HDMI INOUT/ USB 1
BANK15 : 3.3V HDMI TRANSMITER/ RECEIVER
BANK16 : 3.3V SFP INOUT/ HDMI TRANSMITER
BANK34 : 1.35V DDR3
BANK35 : 2.5V GE PHY/ SFP INOUT

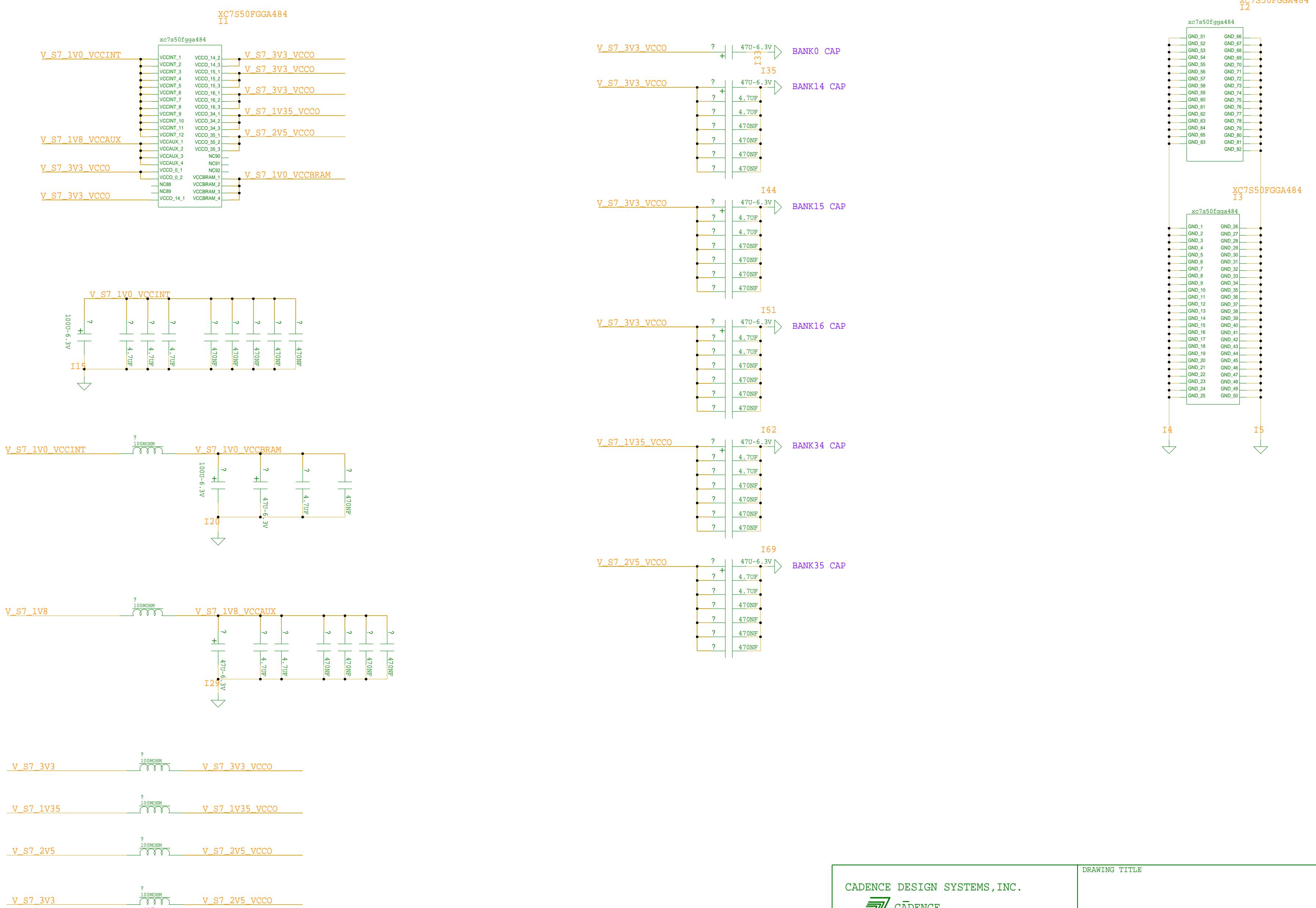


User I/O Pins	Dedicated Pins	Other Pins
○ IO_LXXY_#	C CCLK_0	S VP_0
(s) IO_XX_#	I CFGBVS_0	S VN_0
	D DONE_0	S VREFP_0
	J DXP_0	S VREFN_0
	L DXN_0	
	GNDADC_0	
B ADV_B	⊕ VRN	
B FCS_B	⊖ VRP	
B FOE_B	⊗ VREF	
B MOSI	● D00-D31	
B FWE_B	● A00-A28	
B DOUT_CS0_B	○ DQS	
B CSI_B	● MRCC	
B PUDC_B	● SRCC	
U RDWR_B		
r RS0-RS1		
● AD0P/AD0N-AD15P/AD15N		
● EMCCLK		
		GND
		VCCAUX_IO_G#
		VCCAUX
		VCCINT
		VCCO_#
		VCCBRAM
		n NC

SPARTAN-7 BANK POWER

REVISIONS

ZONE	LTR	DESCRIPTION	DATE	APPR.



CADENCE DESIGN SYSTEMS, INC.
CADENCE

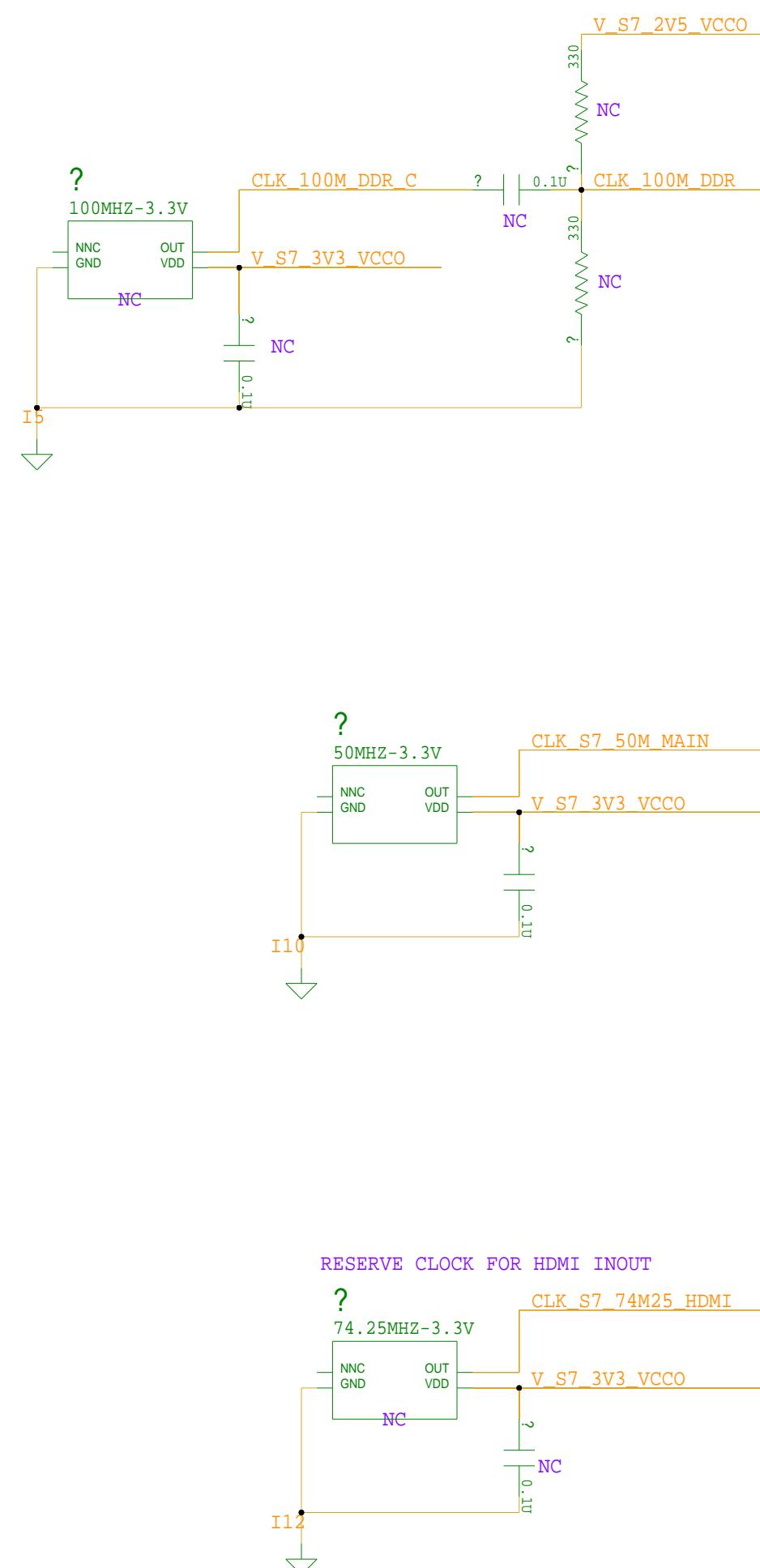
THIS DOCUMENT CONTAINS INFORMATION PROPRIETARY
TO CADENCE DESIGN SYSTEMS INC (CADENCE). USE
OR DISCLOSURE WITHOUT THE WRITTEN PERMISSION OF AN
OFFICER OF CADENCE IS EXPRESSLY FORBIDDEN.
COPYRIGHT (C) CADENCE 1988

DRAWING TITLE		SIZE		REV.		DRAWING NO.	
SCALE	OF						

REVISIONS

ZONE	LTR	DESCRIPTION	DATE	APPR.

SPARTAN-7 CLOCK

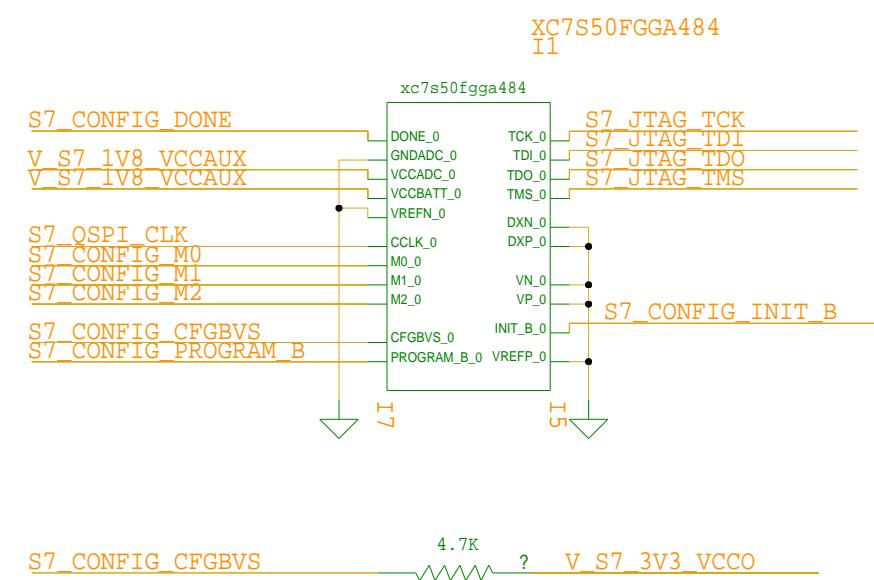


CADENCE DESIGN SYSTEMS, INC.
 CADENCE

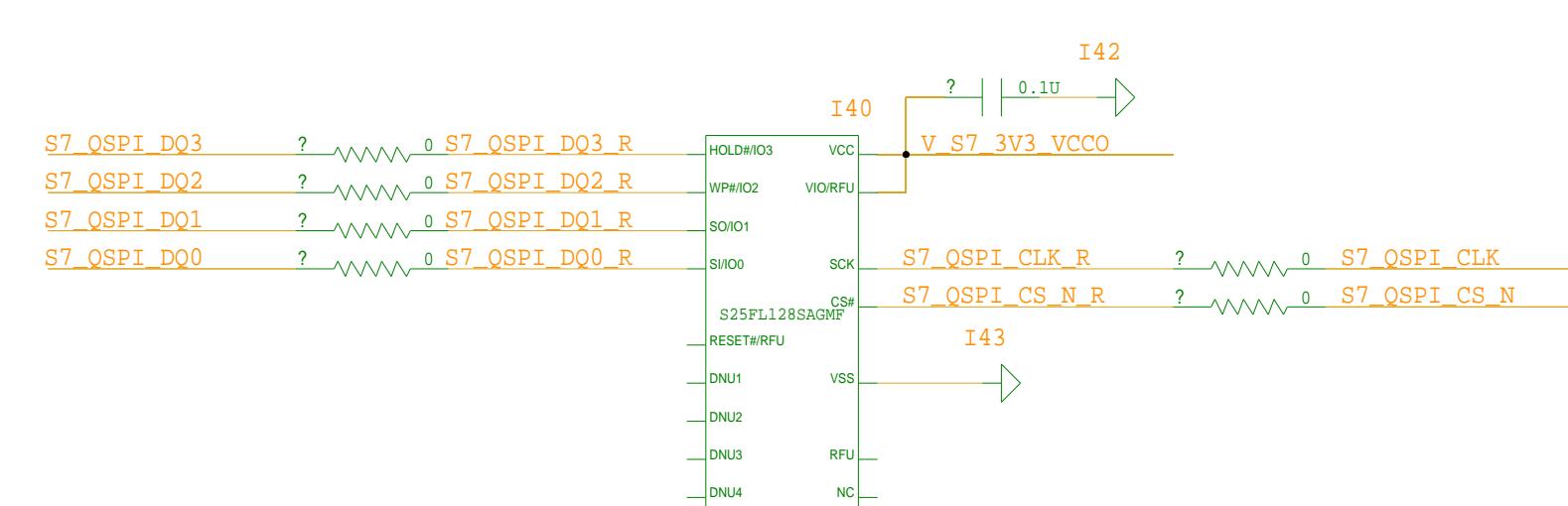
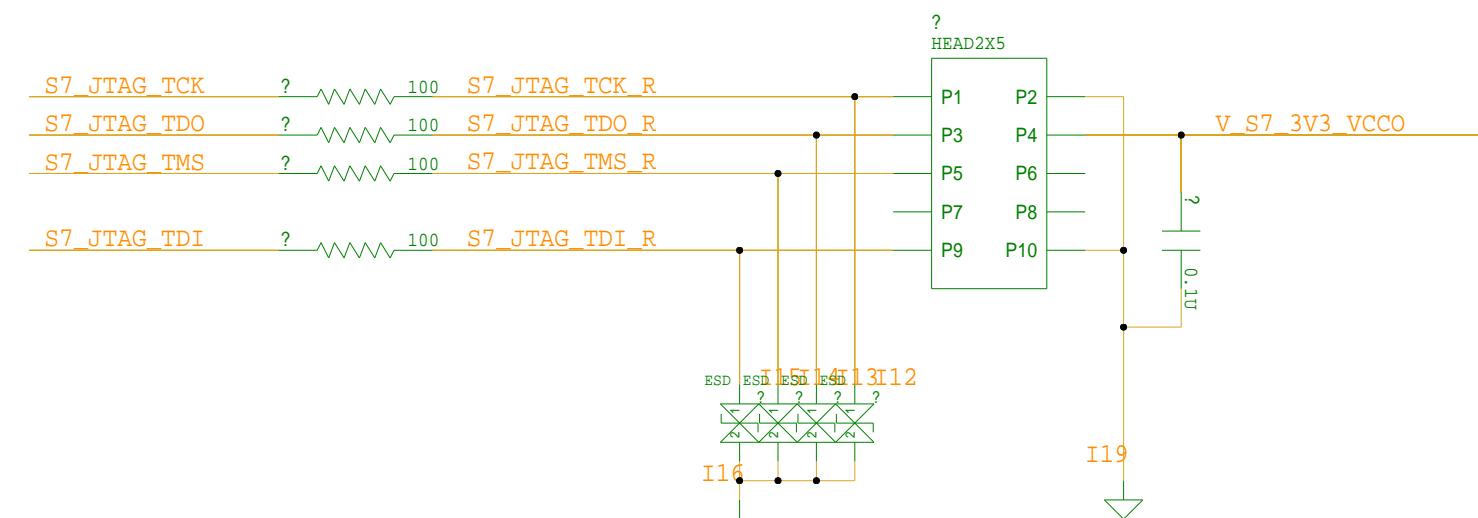
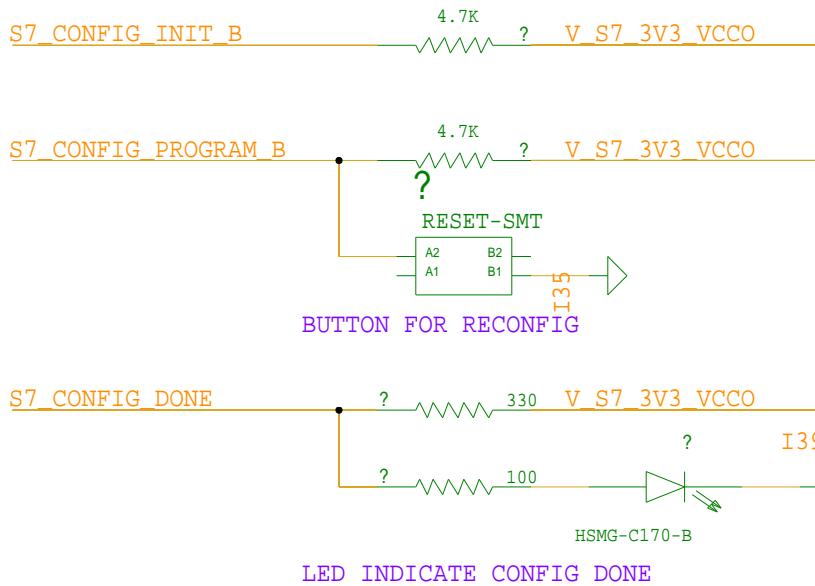
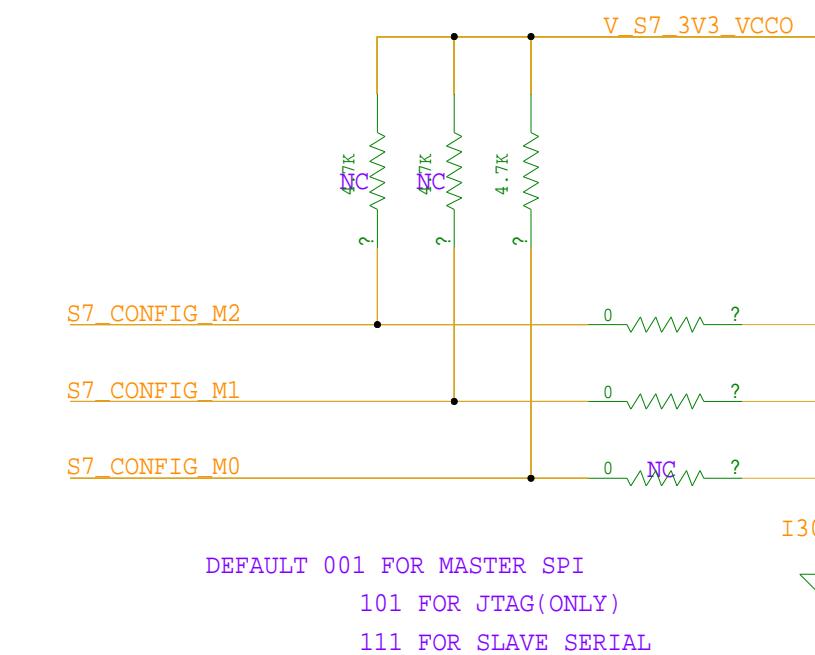
THIS DOCUMENT CONTAINS INFORMATION PROPRIETARY
 TO CADENCE DESIGN SYSTEMS INC (CADENCE). USE
 OR DISCLOSURE WITHOUT THE WRITTEN PERMISSION OF AN
 OFFICER OF CADENCE IS EXPRESSLY FORBIDDEN.
 COPYRIGHT (C) CADENCE 1988

DRAWING TITLE		SIZE		REV.		DRAWING NO.	
SCALE	OF	REV.	SIZE	NO.	OF	SCALE	OF

SPARTAN-7 BANK0/14 CONFIG

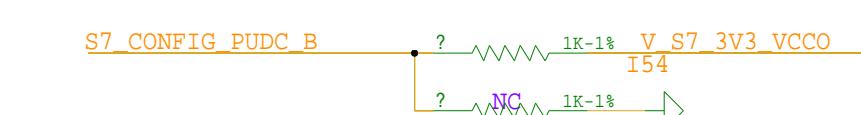
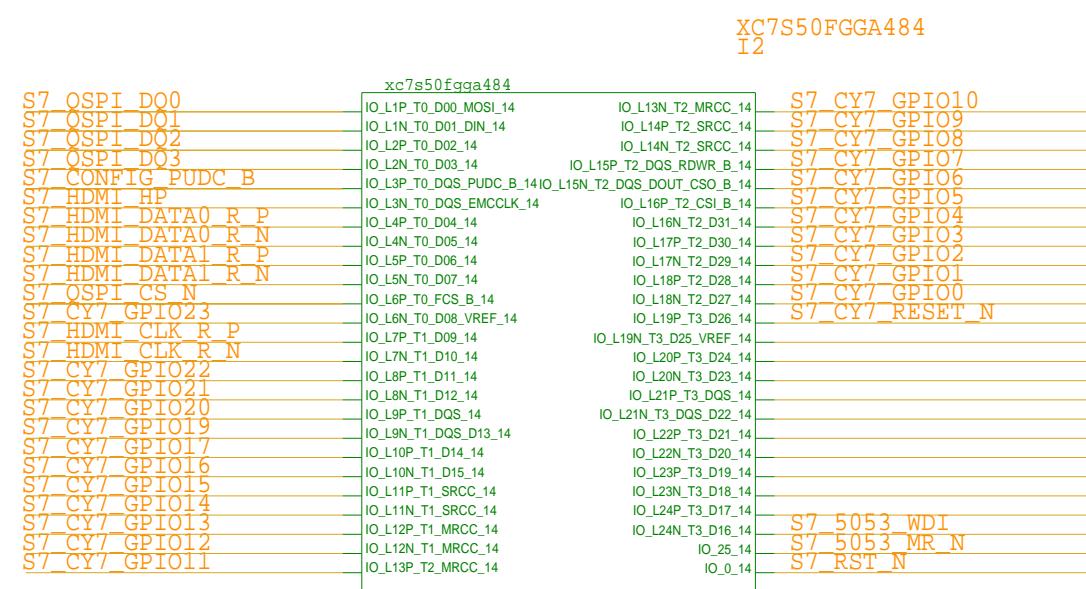


CFGBVS Pin Connection	Supported Configuration Banks 0/14/15 V _{CCO} Supply and I/O Signal Voltages		
	Spartan-7, Artix-7, Kintex-7	Virtex-7 T, XT	Virtex-7 HT
Banks Affected	0, 14, 15	0	none
V _{CCO_0} (3.3V or 2.5V)	3.3V or 2.5V	3.3V or 2.5V	1.8V (no CFGBVS)
GND	1.8V or 1.5V	1.8V or 1.5V	



DO NOT CHANGE WIRES AS BELOW:

S7_QSPI_DQ0
S7_QSPI_DQ1
S7_QSPI_DQ2
S7_QSPI_DQ3
S7_CONFIG_PUDC_B
S7_QSPI_CS_N



PUDC HIGH FOR DISABLE PULLUP RES DURING CONFIGURATION

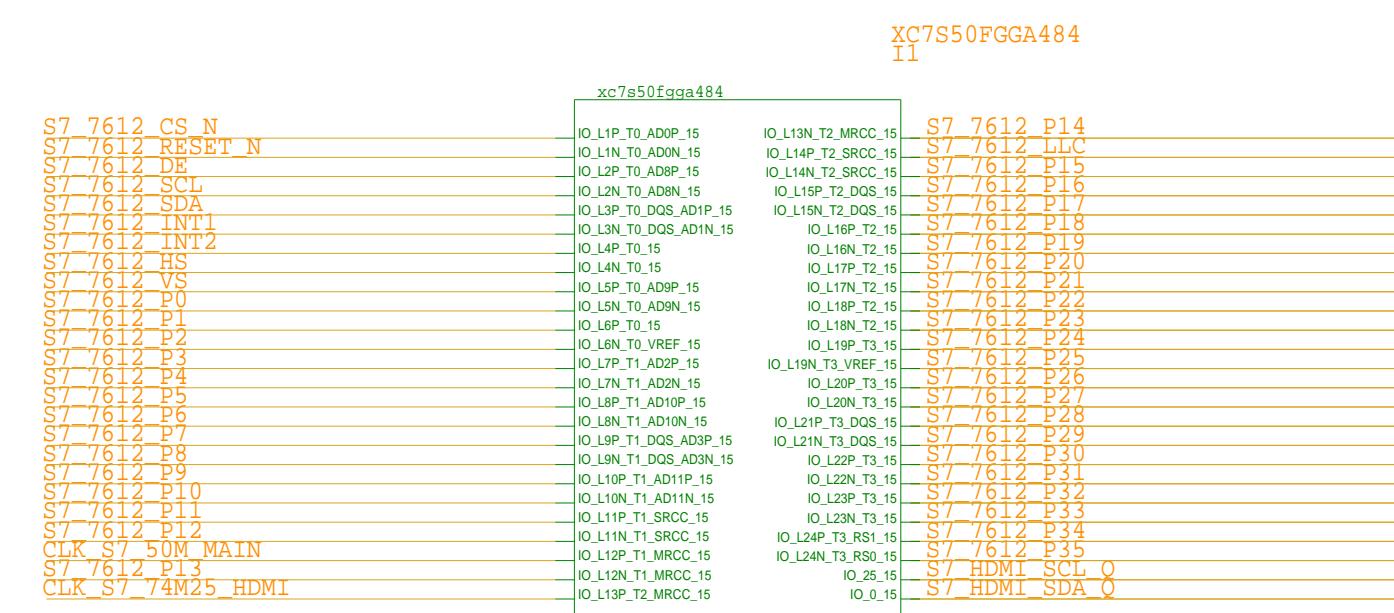
CADENCE DESIGN SYSTEMS, INC.
CADENCE

THIS DOCUMENT CONTAINS INFORMATION PROPRIETARY
TO CADENCE DESIGN SYSTEMS INC (CADENCE). USE
OR DISCLOSURE WITHOUT THE WRITTEN PERMISSION OF AN
OFFICER OF CADENCE IS EXPRESSLY FORBIDDEN.
COPYRIGHT (C) CADENCE 1988

DRAWING TITLE			
SIZE	REV.	DRAWING NO.	
C			
SCALE			SHEET OF

SPARTAN-7 BANK15

REVISIONS		
ZONE	LTR	DESCRIPTION
		DATE APPR.



DO NOT CHANGE WIRES AS BELOW:

CLK_50M_MAIN
CLK_74M25_HDMI

OD CONFIG AS BELOW:

S7_7612_SCL
S7_7612_SDA
S7_HDMI_SCL_Q
S7_HDMI_SDA_Q

CADENCE DESIGN SYSTEMS, INC.


THIS DOCUMENT CONTAINS INFORMATION PROPRIETARY
TO CADENCE DESIGN SYSTEMS INC (CADENCE). USE
OR DISCLOSURE WITHOUT THE WRITTEN PERMISSION OF AN
OFFICER OF CADENCE IS EXPRESSLY FORBIDDEN.
COPYRIGHT (C) CADENCE 1988

DRAWING TITLE			
SIZE	REV.	DRAWING NO.	
		SCALE	SHEET OF
			

SPARTAN-7 BANK16

REVISIONS

ZONE	LTR	DESCRIPTION	DATE	APPR.

F

F

E

E

D

D

C

C

B

B

A

A

xc7s50fgga484
II

xc7s50fgga484

S7_SFP_SIN_P	IO_L1P_T0_16	IO_L19N_T2_MRCC_16	S7_7511_D8
S7_SFP_SIN_N	IO_L1N_T0_16	IO_L14P_T2_SRCC_16	S7_7511_D9
S7_SFP_SOUT_P	IO_L2P_T0_16	IO_L14N_T2_SRCC_16	S7_7511_D10
S7_SFP_SOUT_N	IO_L2N_T0_16	IO_L15P_T2_DOS_16	S7_7511_D11
S7_FPGA_7511_SCL	IO_L3P_T0_DQS_16	IO_L15N_T2_DOS_16	S7_7511_D12
S7_FPGA_7511_SDA	IO_L3N_T0_DQS_16	IO_L16P_T2_16	S7_7511_D13
S7_7511_DE	IO_L4P_T0_16	IO_L16N_T2_16	S7_7511_D14
S7_7511_HSYNC	IO_L4N_T0_16	IO_L17P_T2_16	S7_7511_D15
S7_7511_INT	IO_L5P_T0_16	IO_L17N_T2_16	S7_7511_D19
S7_7511_SPDIF	IO_L5N_T0_16	IO_L18P_T2_16	S7_7511_D20
S7_7511_SPDIF_OUT	IO_L6P_T0_16	IO_L18N_T2_16	S7_7511_D21
S7_7511_VSYNC	IO_L6N_T0_16	IO_L19P_T3_16	S7_7511_D22
S7_7511_D0	IO_L7P_T0_16	IO_L19N_T3_VREF_16	S7_7511_D23
S7_7511_D1	IO_L7N_T1_16	IO_L20P_T3_16	S7_7511_D24
S7_7511_D2	IO_L8P_T1_16	IO_L20N_T3_16	S7_7511_D25
S7_7511_D3	IO_L8N_T1_16	IO_L21P_T3_DQS_16	S7_7511_D26
S7_7511_D4	IO_L9P_T1_16	IO_L21N_T3_DQS_16	S7_7511_D27
S7_7511_D5	IO_L9N_T1_DQS_16	IO_L22P_T3_16	S7_7511_D28
S7_7511_D6	IO_L10P_T1_16	IO_L22N_T3_16	S7_7511_D29
S7_7511_D7	IO_L10N_T1_16	IO_L23P_T3_16	S7_7511_D30
S7_7511_CLK	IO_L11P_T1_SRCC_16	IO_L23N_T3_16	S7_7511_D31
S7_7511_D16	IO_L11N_T1_SRCC_16	IO_L24P_T3_16	S7_7511_D32
S7_7511_D17	IO_L12P_T1_MRCC_16	IO_L24N_T3_16	S7_7511_D33
S7_7511_D18	IO_L12N_T1_MRCC_16	IO_25_16	S7_7511_D34
S7_FPGA_7511_CEC_CLK	IO_L13P_T2_MRCC_16	IO_0_16	S7_7511_D35

OD CONFIG AS BELOW:

S7_FPGA_7511_SCL
S7_FPGA_7511_SDA

CADENCE DESIGN SYSTEMS, INC.


THIS DOCUMENT CONTAINS INFORMATION PROPRIETARY
TO CADENCE DESIGN SYSTEMS INC (CADENCE). USE
OR DISCLOSURE WITHOUT THE WRITTEN PERMISSION OF AN
OFFICER OF CADENCE IS EXPRESSLY FORBIDDEN.
COPYRIGHT (C) CADENCE 1988

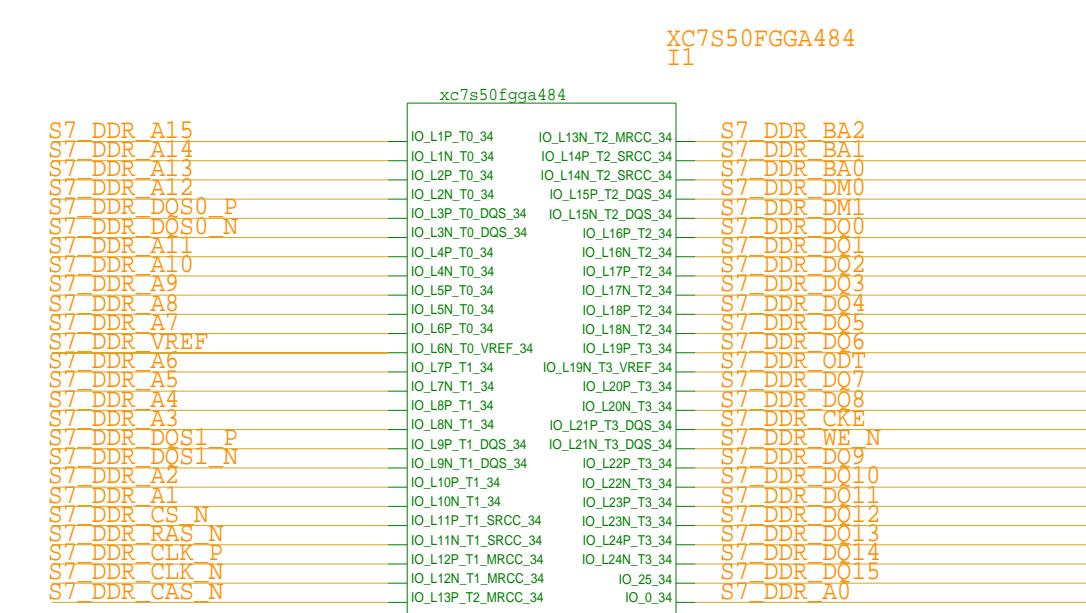
DRAWING TITLE

SIZE	REV.	DRAWING NO.
		
SCALE		

SHEET OF

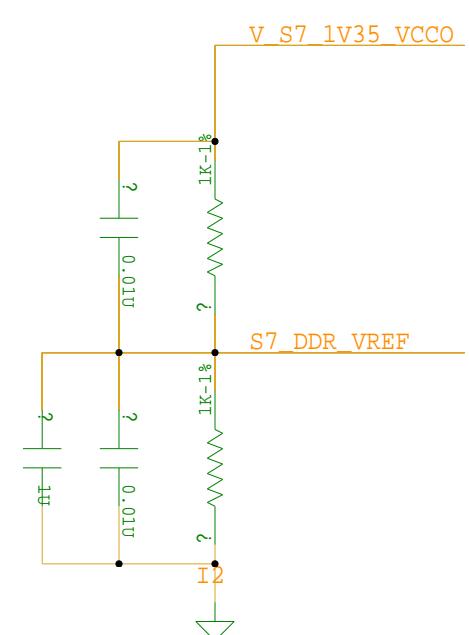
SPARTAN-7 BANK34

REVISED		DESCRIPTION		DATE	APPR.



DO NOT CHANGE WIRES AS BELOW:

S7_DDR_DQSO/1_P/N
S7_DDR_CLK_P/N
S7_DDR_VREF



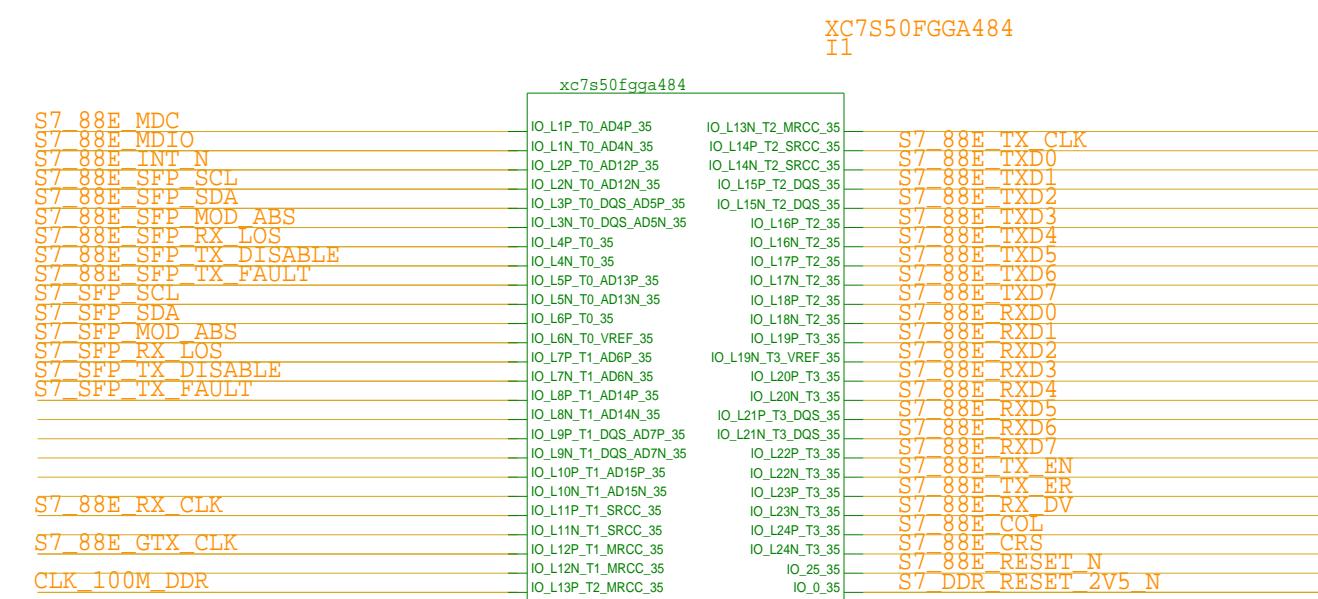
CADENCE DESIGN SYSTEMS, INC.
 CADENCE

THIS DOCUMENT CONTAINS INFORMATION PROPRIETARY
TO CADENCE DESIGN SYSTEMS INC (CADENCE). USE
OR DISCLOSURE WITHOUT THE WRITTEN PERMISSION OF AN
OFFICER OF CADENCE IS EXPRESSLY FORBIDDEN.
COPYRIGHT (C) CADENCE 1988

DRAWING TITLE		SIZE		DRAWING NO.	
SCALE	REV.				

SPARTAN-7 BANK35

REVISIONS		
ZONE	LTR	DESCRIPTION
		DATE APPR.



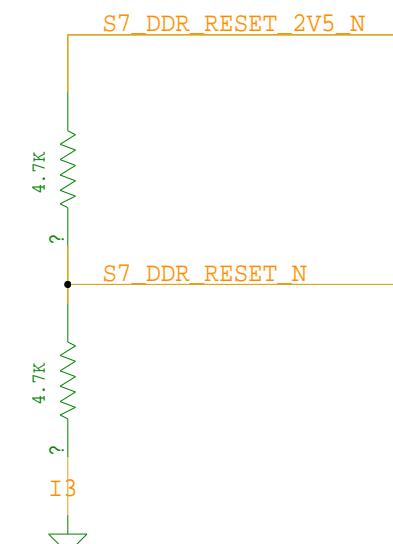
DO NOT CHANGE WIRES AS BELOW:

CLK_100M_DDR
S7_88E_CTX_CLK
S7_88E_RX_CLK

OD CONFIG AS BELOW:

S7_88E_SFP_SCL
S7_88E_SFP_SDA
S7_88E_SFP_MOD_ABS
S7_88E_SFP_RX_LOS
S7_88E_SFP_TX_DISABLE
S7_88E_SFP_TX_FAULT

S7_SFP_SCL
S7_SFP_SDA
S7_SFP_MOD_ABS
S7_SFP_RX_LOS
S7_SFP_TX_DISABLE
S7_SFP_TX_FAULT



CADENCE DESIGN SYSTEMS, INC.



THIS DOCUMENT CONTAINS INFORMATION PROPRIETARY
TO CADENCE DESIGN SYSTEMS INC (CADENCE). USE
OR DISCLOSURE WITHOUT THE WRITTEN PERMISSION OF AN
OFFICER OF CADENCE IS EXPRESSLY FORBIDDEN.
COPYRIGHT (C) CADENCE 1988

DRAWING TITLE

SIZE	REV.	DRAWING NO.
C		
SCALE	SHEET OF	

SPARTAN-7 BANK NC

REVISIONS

ZONE	LTR	DESCRIPTION	DATE	APPR.

F

F

E

E

D

D

C

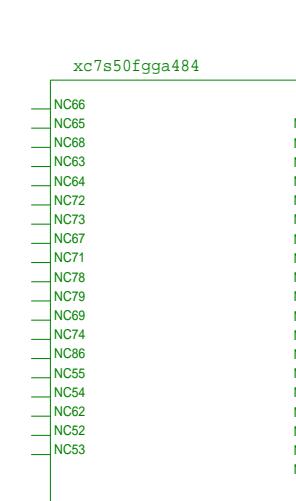
C

B

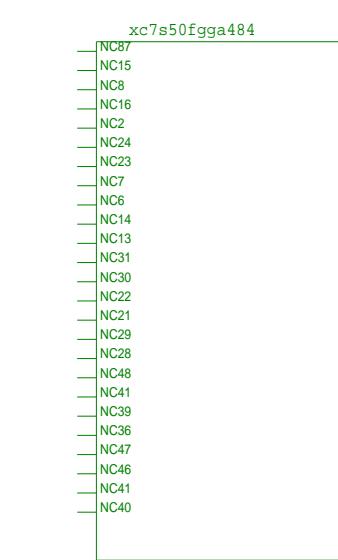
B

A

A



XC7S50FGGA484



XC7S50FGGA484

CADENCE DESIGN SYSTEMS, INC.
 CADENCE

THIS DOCUMENT CONTAINS INFORMATION PROPRIETARY
TO CADENCE DESIGN SYSTEMS INC (CADENCE). USE
OR DISCLOSURE WITHOUT THE WRITTEN PERMISSION OF AN
OFFICER OF CADENCE IS EXPRESSLY FORBIDDEN.
COPYRIGHT (C) CADENCE 1988

DRAWING TITLE

SIZE  REV. DRAWING NO.

SCALE SHEET OF

ARTIX-7 INDEX

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPR.

F

F

E

E

D

D

C

C

B

B

A

A

CADENCE DESIGN SYSTEMS, INC.
 CADENCE

THIS DOCUMENT CONTAINS INFORMATION PROPRIETARY
 TO CADENCE DESIGN SYSTEMS INC (CADENCE). USE
 OR DISCLOSURE WITHOUT THE WRITTEN PERMISSION OF AN
 OFFICER OF CADENCE IS EXPRESSLY FORBIDDEN.
 COPYRIGHT (C) CADENCE 1988

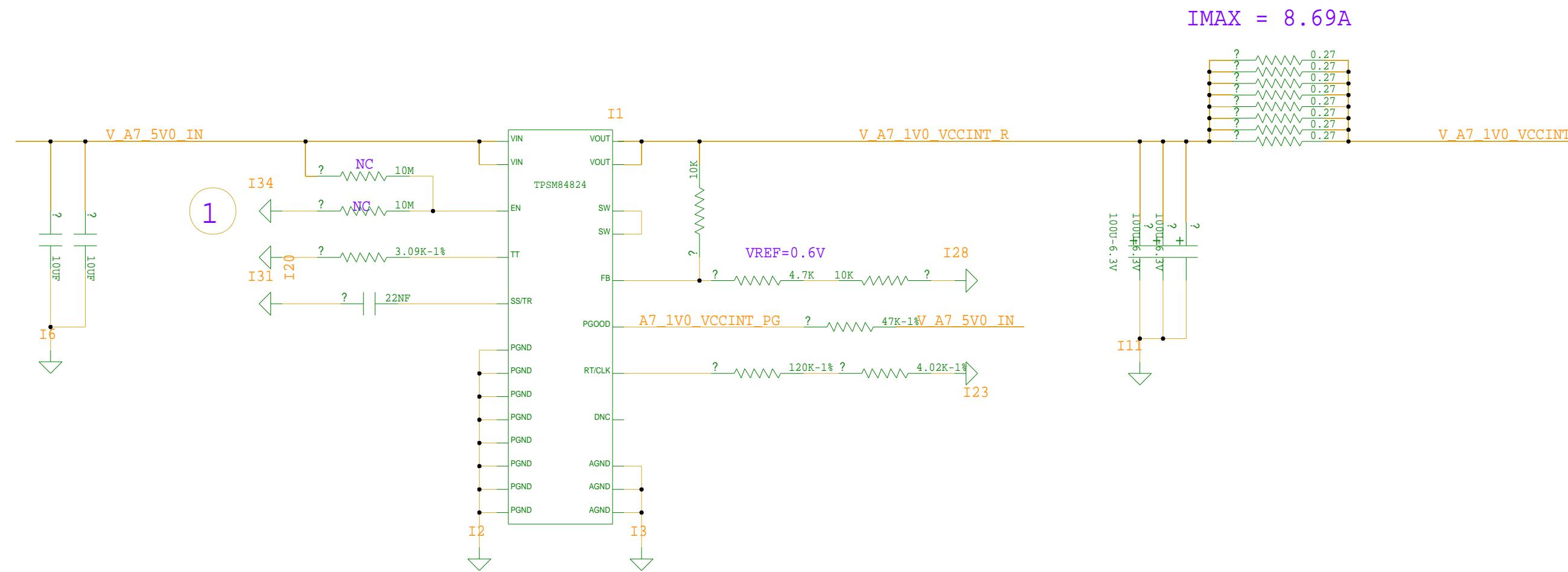
DRAWING TITLE

SIZE	REV.	DRAWING NO.
		
SCALE		SHEET OF

ARTIX-7 POWER (1)

REVISI

ZONE	LTR	DESCRIPTION	DATE	APPR.



SS/TR	6	I	Soft-start and tracking pin. Connecting an external capacitor to this pin adjusts the output voltage soft-start ramp slower than its 1.2 ms default setting. A voltage applied to this pin allows for tracking and sequencing control.
-------	---	---	--

Table 9. Soft-Start Capacitor Values and Soft-Start Time

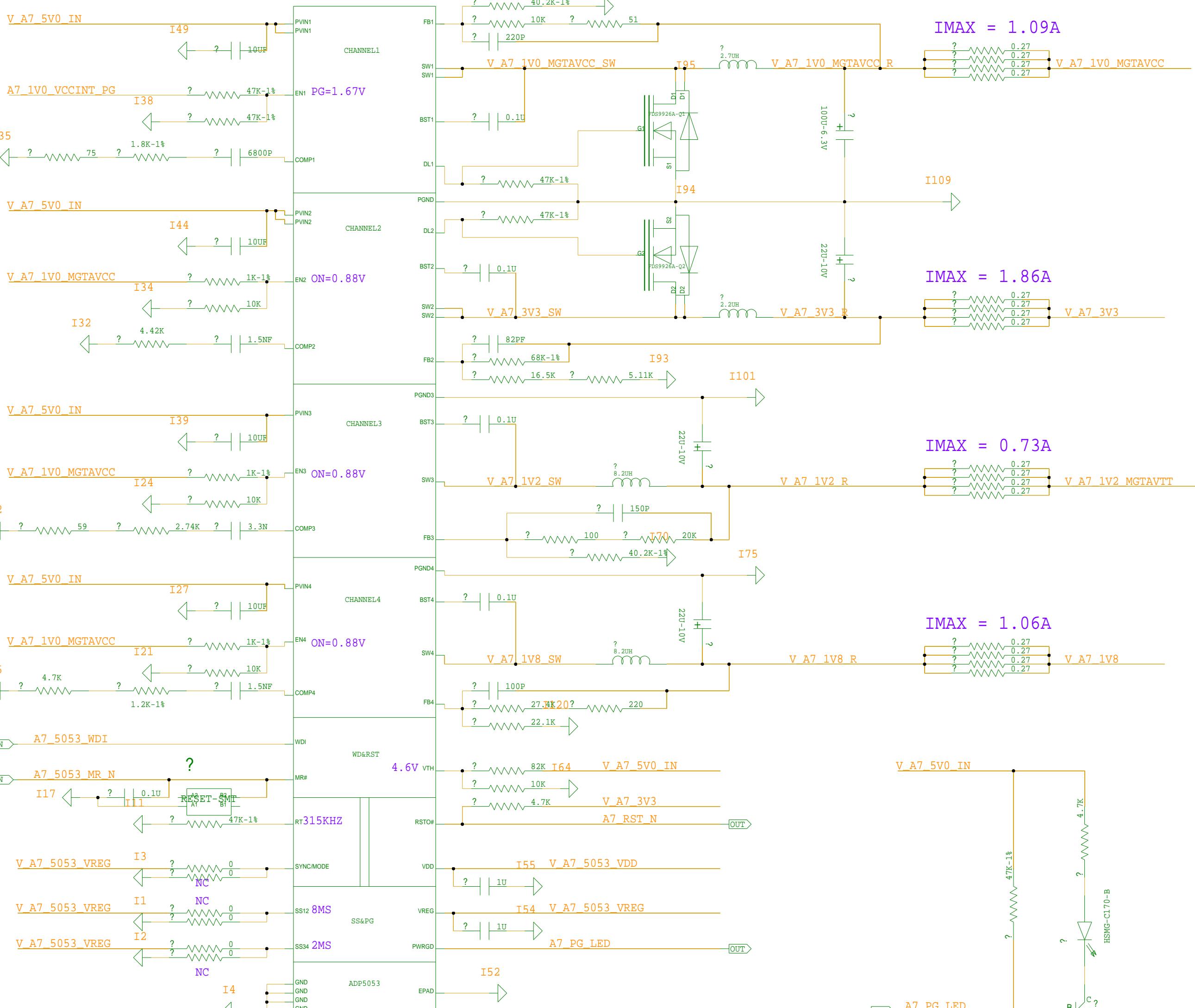
C _{ss} (nF)	open	10	15	22	47
SS Time (ms)	1.2	2.4	3	3.8	6.8

CADENCE DESIGN SYSTEMS, INC.


THIS DOCUMENT CONTAINS INFORMATION PROPRIETARY
 TO CADENCE DESIGN SYSTEMS INC (CADENCE). USE
 OR DISCLOSURE WITHOUT THE WRITTEN PERMISSION OF AN
 OFFICER OF CADENCE IS EXPRESSLY FORBIDDEN.
 COPYRIGHT (C) CADENCE 1988

DRAWING TITLE		SIZE		DRAWING NO.	
SCALE	REV.	INCHES	MM	INCHES	MM

ARTIX-7 POWER (2)



$$V_{OUT} = V_{REF} \times (1 + (R_{TOP}/R_{BOT}))$$

$$R_{RT} (\text{k}\Omega) = [14,822/f_{SW} (\text{kHz})]^{1.081}$$

$$V_{IN_STARTUP} = (0.8 \text{ nA} + (0.8 \text{ V}/R_{BOT_EN})) \times \left(R_{TOP_EN} + \frac{R_{BOT_EN} \times 1 \text{ M}\Omega}{R_{BOT_EN} + 1 \text{ M}\Omega} \right)$$

where:

R_{TOP_EN} is the resistor from V_{IN} to EN.

R_{BOT_EN} is the resistor from EN to ground.

Table 9. Soft Start Time Set by the SS12 and SS34 Pins

R_{TOP} (k Ω)	R_{BOT} (k Ω)	Soft Start Time			
		Channel 1	Channel 2	Channel 3	Channel 4
0	N/A ¹	2 ms	2 ms	2 ms	2 ms
100	600	2 ms	Parallel	2 ms	4 ms
200	500	2 ms	8 ms	2 ms	8 ms
300	400	4 ms	2 ms	4 ms	2 ms
400	300	4 ms	4 ms	4 ms	4 ms
500	200	8 ms	2 ms	4 ms	8 ms
600	100	8 ms	Parallel	8 ms	2 ms
N/A ¹	0	8 ms	8 ms	8 ms	8 ms

Table 16. Factory Default Options

Option	Default Value
Channel 1 Output Voltage	0.8V adjustable output
Channel 2 Output Voltage	0.8V adjustable output
Channel 3 Output Voltage	0.8V adjustable output
Channel 4 Output Voltage	0.8V adjustable output
PWRGD Pin (Pin 20) Output	Monitor Channel 1 output
Output Discharge Function	Enabled for all four buck regulators
Switching Frequency on Channel 1	1 x switching frequency set by the RT pin
Switching Frequency on Channel 3	1 x switching frequency set by the RT pin
SYNC/MODE Pin (Pin 43) Function	Forced PWM/automatic PWM/PSM mode setting with the ability to synchronize to an external clock
Hiccup Protection	Enabled for overcurrent events
Short-Circuit Latch-Off Function	Disabled for output short-circuit events
Overvoltage Latch-Off Function	Disabled for output overvoltage events
Reset Timeout Period	200 ms
Watchdog Timeout Period	1.6 sec
Manual Reset Input Mode	Processor manual reset mode

CADENCE DESIGN SYSTEMS, INC.

CADENCE

THIS DOCUMENT CONTAINS INFORMATION PROPRIETARY
TO CADENCE DESIGN SYSTEMS INC (CADENCE). USE
OR DISCLOSURE WITHOUT THE WRITTEN PERMISSION OF AN
OFFICER OF CADENCE IS EXPRESSLY FORBIDDEN.
COPYRIGHT (C) CADENCE 1988

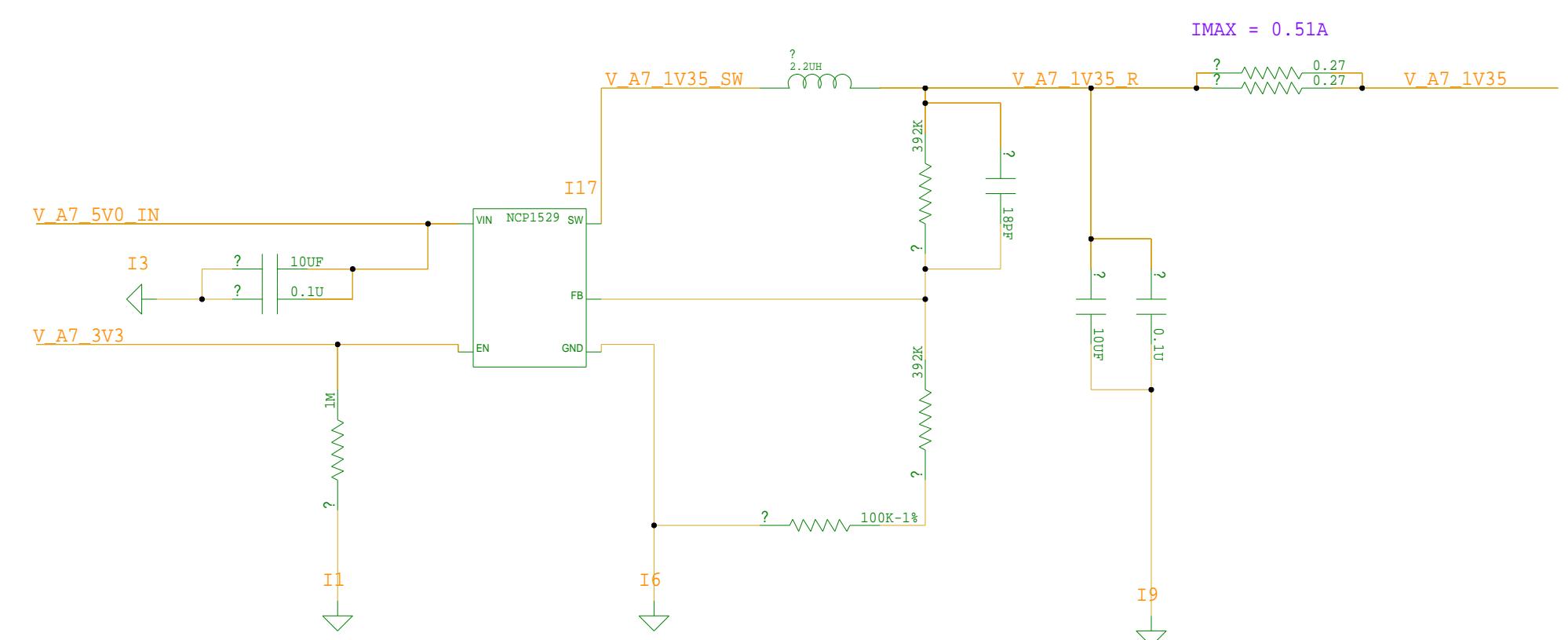
DRAWING TITLE			
SIZE	REV.	DRAWING NO.	
C			
SCALE			SHEET OF
			1

ARTIX-7 POWER (3)

$$V_{out} = V_{FB} \times (1 + R1/R2)$$

- V_{OUT} : Output Voltage (V)
- V_{FB} : Feedback Voltage = 0.6 V
- $R1$: Feedback Resistor from V_{OUT} to FB
- $R2$: Feedback Resistor from FB to GND

4



CADENCE DESIGN SYSTEMS, INC.



THIS DOCUMENT CONTAINS INFORMATION PROPRIETARY
TO CADENCE DESIGN SYSTEMS INC (CADENCE). USE
OR DISCLOSURE WITHOUT THE WRITTEN PERMISSION OF AN
OFFICER OF CADENCE IS EXPRESSLY FORBIDDEN.
COPYRIGHT (C) CADENCE 1988

DRAWING TITLE

SIZE	REV.	DRAWING NO.
C		
SCALE		SHEET OF

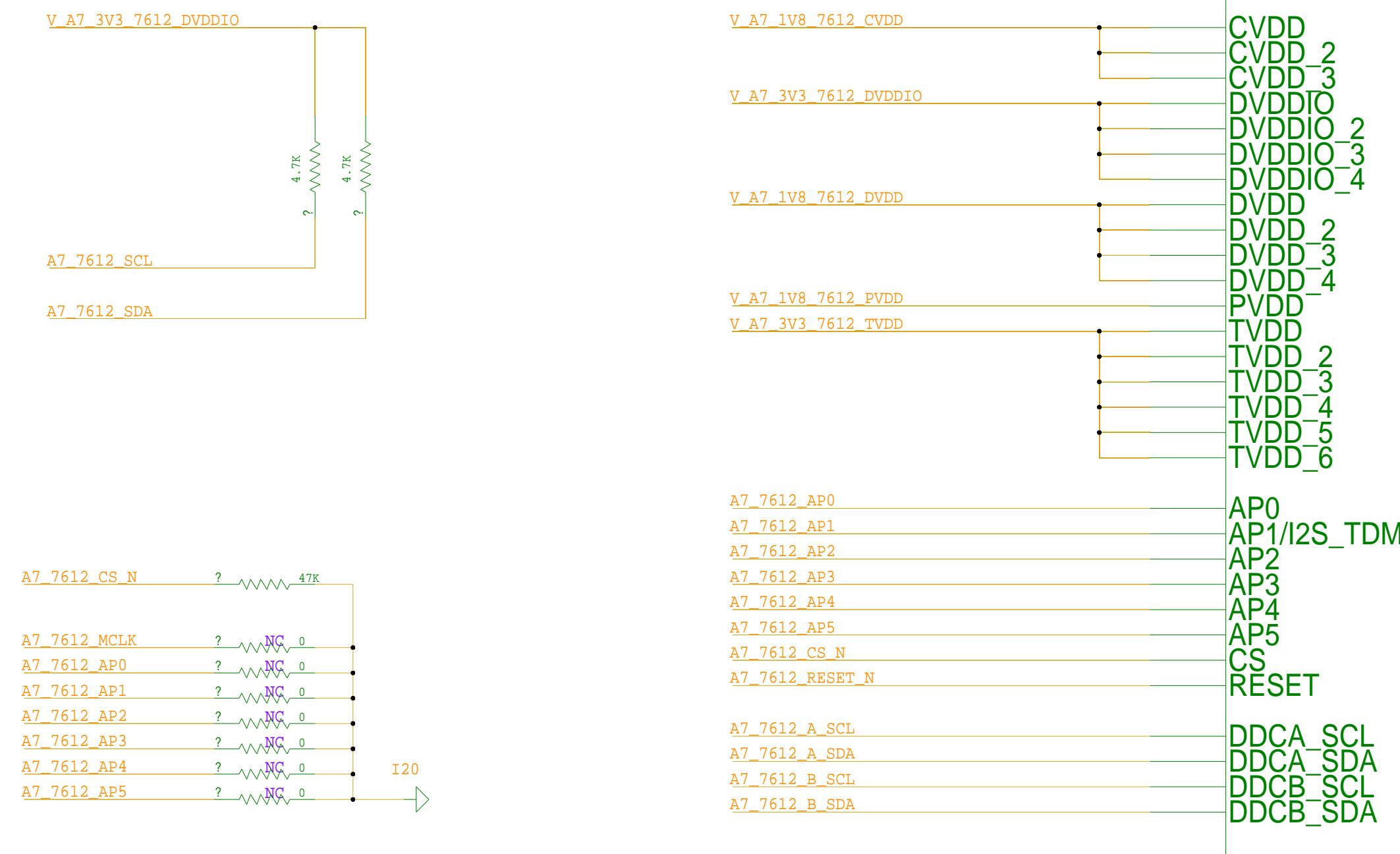
ARTIX-7 HDMI RECEIVER (1)

REVISONS

ZONE LTR

DESCRIPTION

DATE APPR.



DE

XTALP
XTALN
SDA
SCLK/INT2
SCL
RXB_5V
RXA_5V

MCLK/INT2
INT1
HPA_B
HPA_A/INT2

RXB_C+
RXB_C-
RXB_2-
RXB_1-
RXB_0-
RXB_2+
RXB_1+
RXB_0+
RXA_C+
RXA_C-
RXA_2-
RXA_1-
RXA_0-
RXA_2+
RXA_1+
RXA_0+

A7_7612_XTAL_P
A7_7612_XTAL_N
A7_7612_SDA
A7_7612_SCL
V_A7_7612_B_5V
V_A7_7612_A_5V0

A7_7612_MCLK

A7_7612_B_HP
A7_7612_A_HP

A7_7612_B_CLK_P
A7_7612_B_CLK_N
A7_7612_B_DATA2_N

A7_7612_B_DATA1_N
A7_7612_B_DATA0_N
A7_7612_B_DATA2_P

A7_7612_B_DATA1_P
A7_7612_B_CLK_P

A7_7612_A_CLK_P
A7_7612_A_CLK_N

A7_7612_A_DATA2_N

A7_7612_A_DATA1_N
A7_7612_A_CLK_N

A7_7612_A_DATA0_N
A7_7612_A_CLK_P

A7_7612_A_DATA2_P
A7_7612_A_CLK_N

A7_7612_A_DATA1_P
A7_7612_A_CLK_P

A7_7612_A_DATA0_P

CADENCE DESIGN SYSTEMS, INC.

CADENCE

THIS DOCUMENT CONTAINS INFORMATION PROPRIETARY
TO CADENCE DESIGN SYSTEMS INC (CADENCE). USE
OR DISCLOSURE WITHOUT THE WRITTEN PERMISSION OF AN
OFFICER OF CADENCE IS EXPRESSLY FORBIDDEN.
COPYRIGHT (C) CADENCE 1988

DRAWING TITLE

SIZE

C

REV.

?

DRAWING NO.

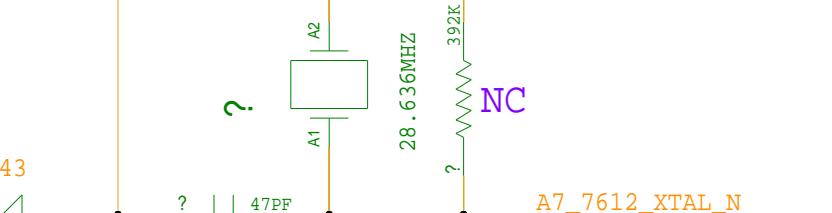
?

SCALE

?

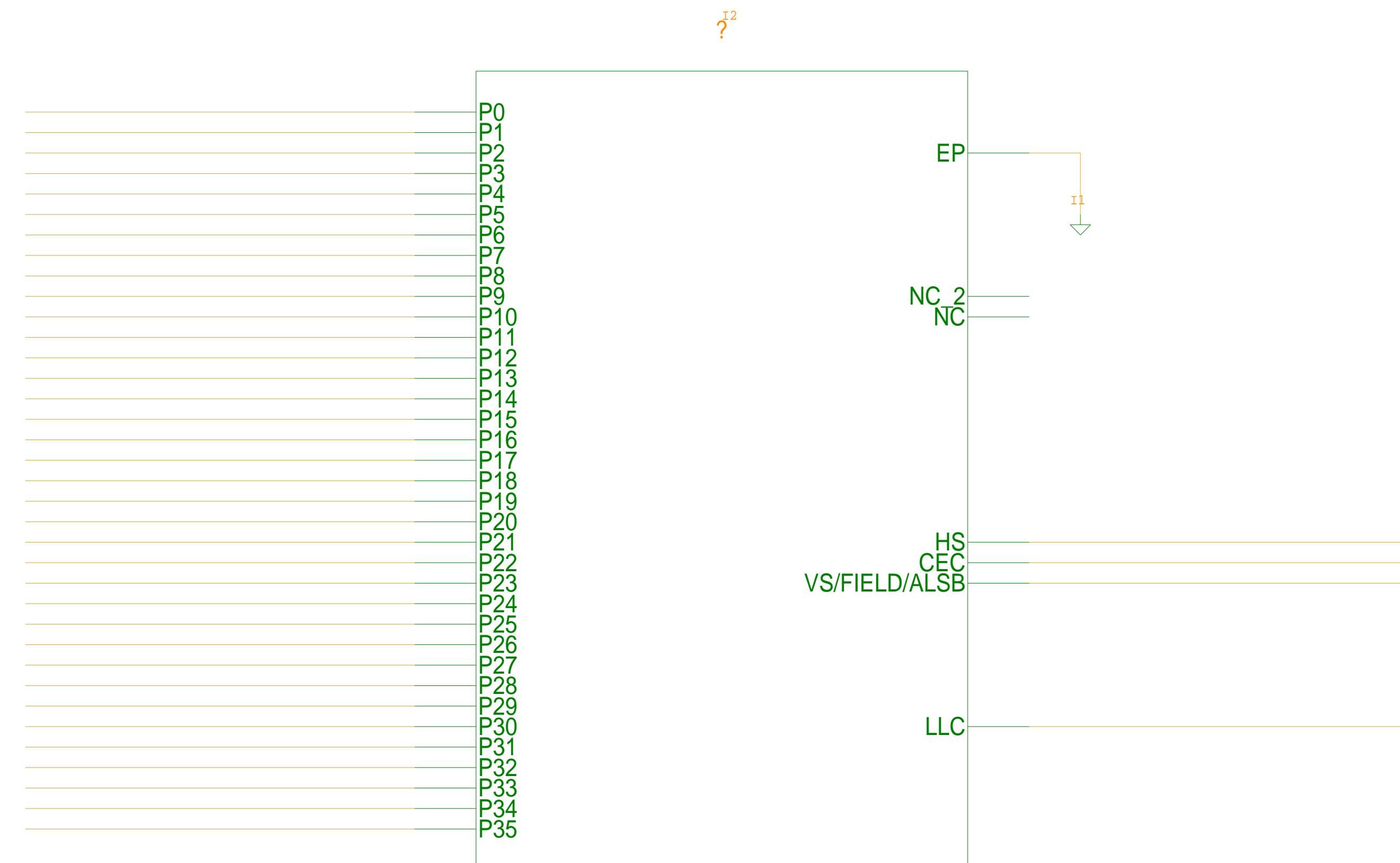
SHEET

OF



ARTIX-7 HDMI RECEIVER (2)

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPR.



CADENCE DESIGN SYSTEMS, INC.



THIS DOCUMENT CONTAINS INFORMATION PROPRIETARY
TO CADENCE DESIGN SYSTEMS INC (CADENCE). USE
OR DISCLOSURE WITHOUT THE WRITTEN PERMISSION OF AN
OFFICER OF CADENCE IS EXPRESSLY FORBIDDEN.
COPYRIGHT (C) CADENCE 1988

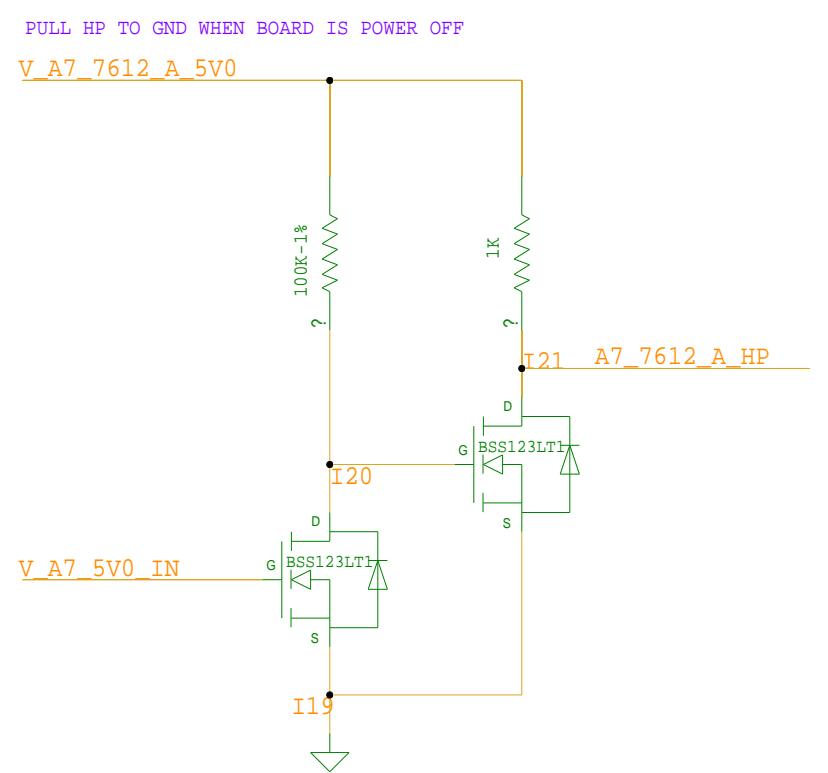
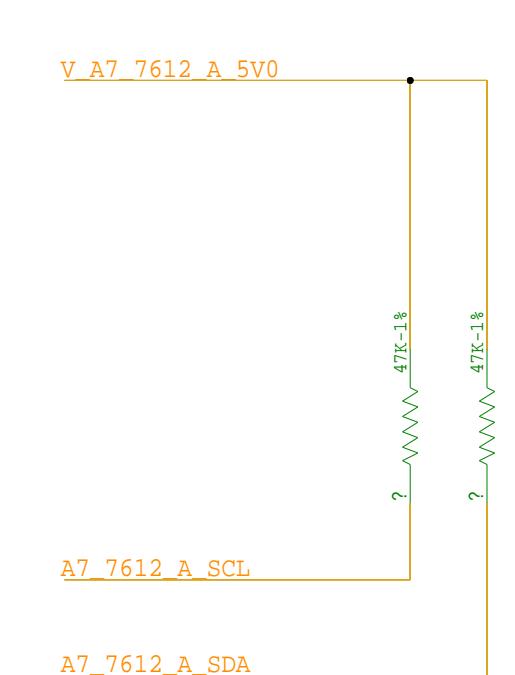
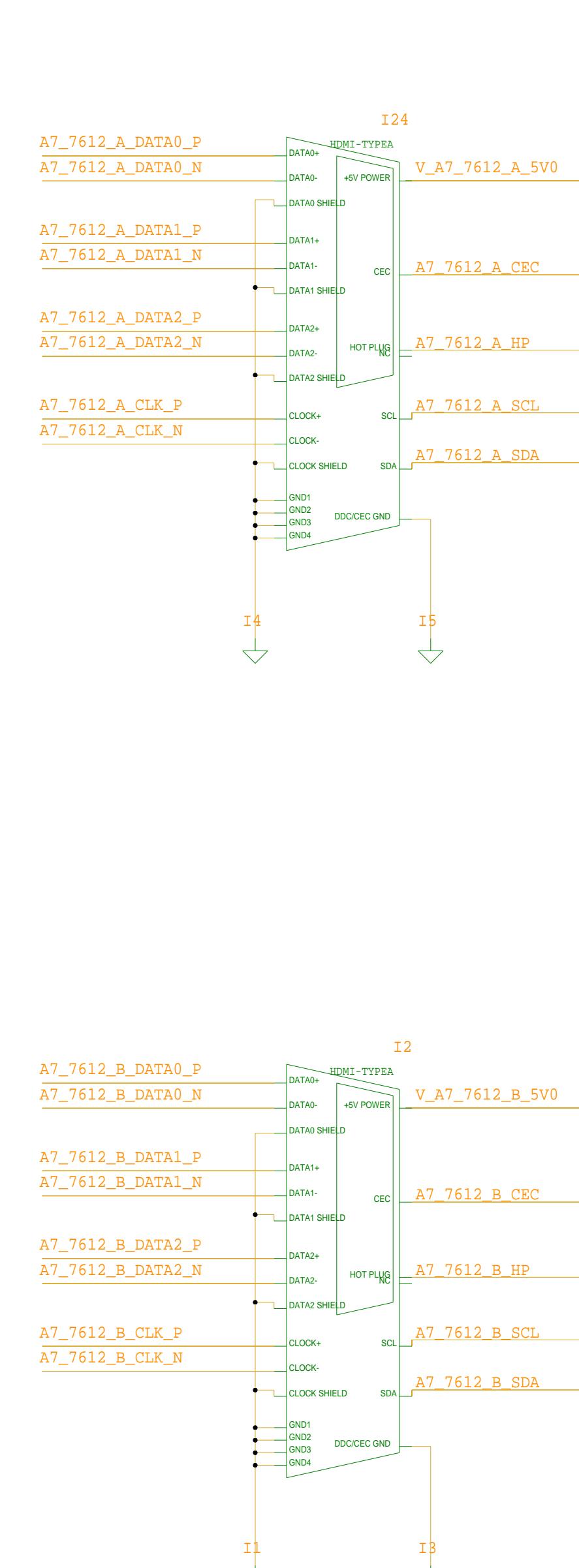
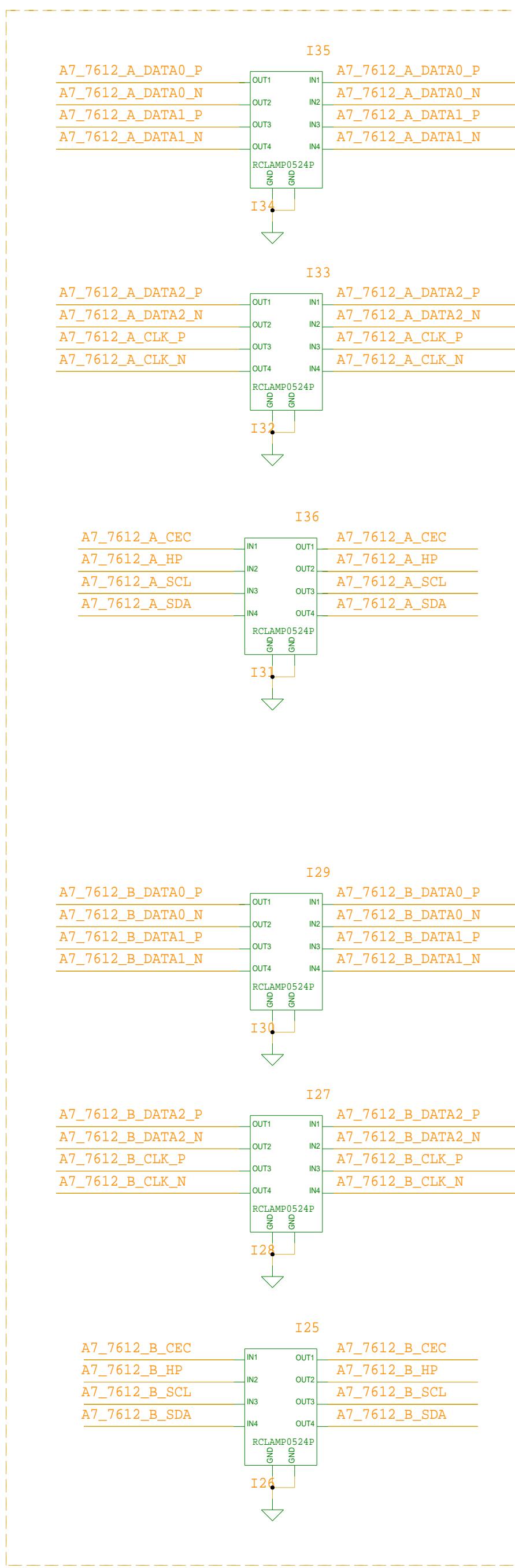
DRAWING TITLE

SIZE REV. DRAWING NO.

SCALE SHEET OF

ARTIX-7 HDMI RECEIVER (3)

CHANGE CONNECTION DUE TO LAYOUT

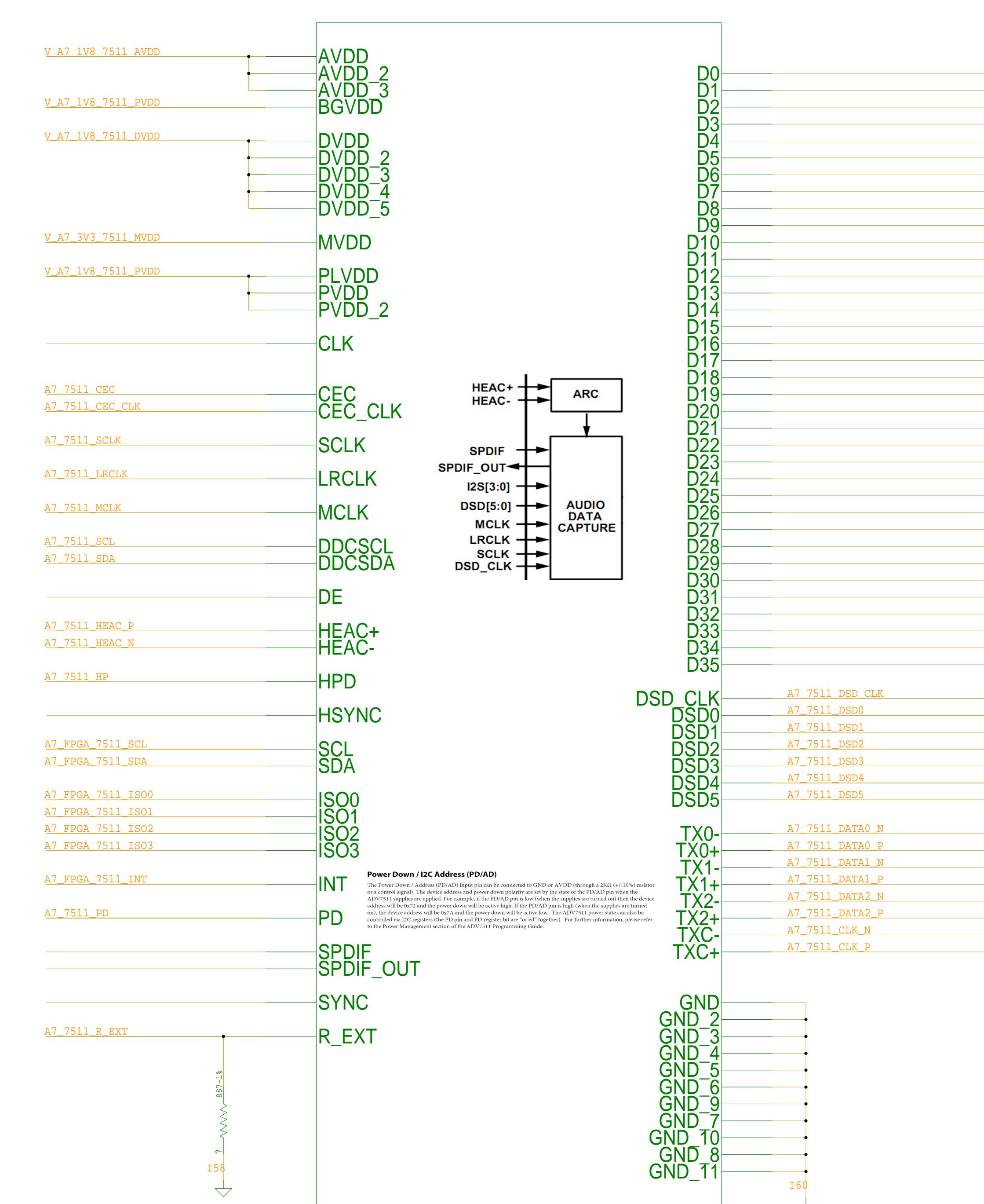


CADENCE DESIGN SYSTEMS, INC.
CADENCE

THIS DOCUMENT CONTAINS INFORMATION PROPRIETARY
TO CADENCE DESIGN SYSTEMS INC (CADENCE). USE
OR DISCLOSURE WITHOUT THE WRITTEN PERMISSION OF AN
OFFICER OF CADENCE IS EXPRESSLY FORBIDDEN.
COPYRIGHT (C) CADENCE 1988

DRAWING TITLE		SIZE		REV.		DRAWING NO.	
SCALE						SHEET	OF

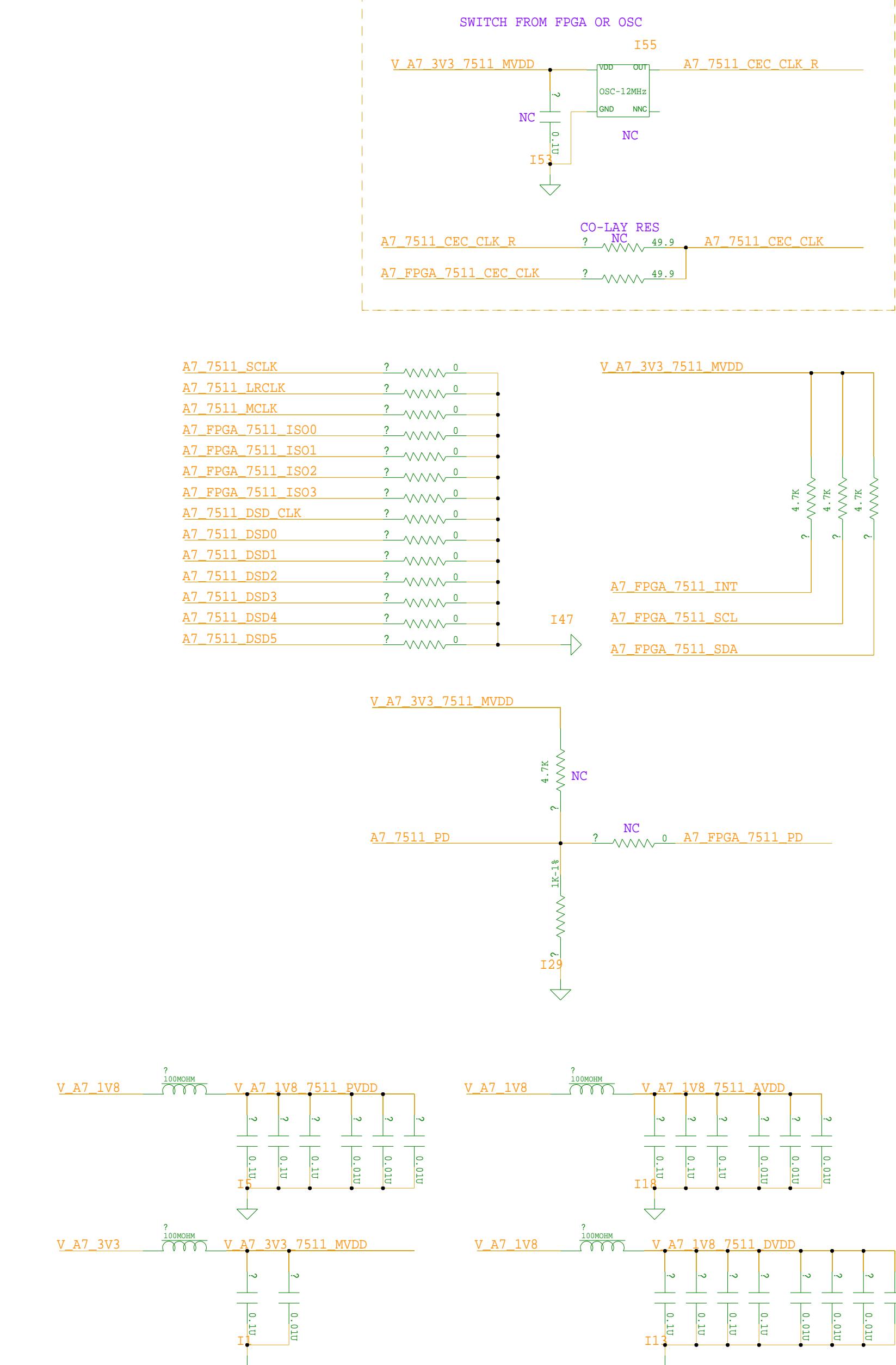
ARTIX-7 HDMI TRANSMITTER (1)



CADENCE DESIGN SYSTEMS, INC.
CADENCE

THIS DOCUMENT CONTAINS INFORMATION PROPRIETARY
TO CADENCE DESIGN SYSTEMS INC (CADENCE). USE
OR DISCLOSURE WITHOUT THE WRITTEN PERMISSION OF AN
OFFICER OF CADENCE IS EXPRESSLY FORBIDDEN.
COPYRIGHT (C) CADENCE 1988

DRAWING TITLE		SIZE		REV.		DRAWING NO.	
		SCALE				SHEET	OF
8	7	6	5	4	3	2	1

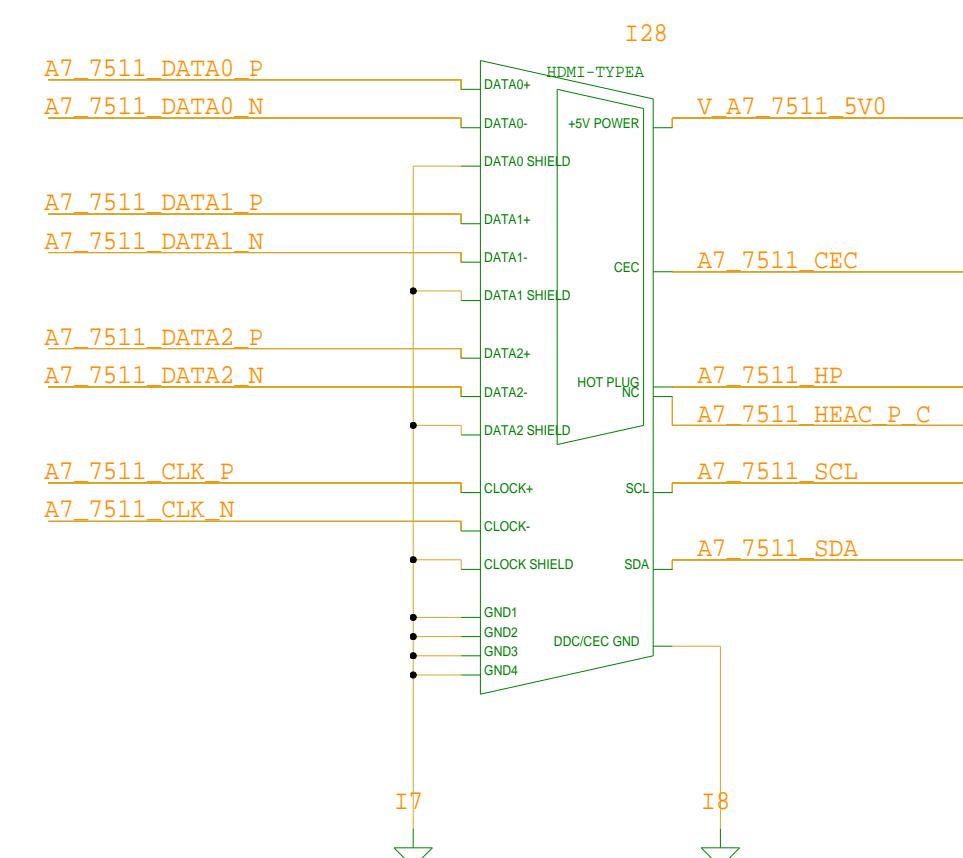
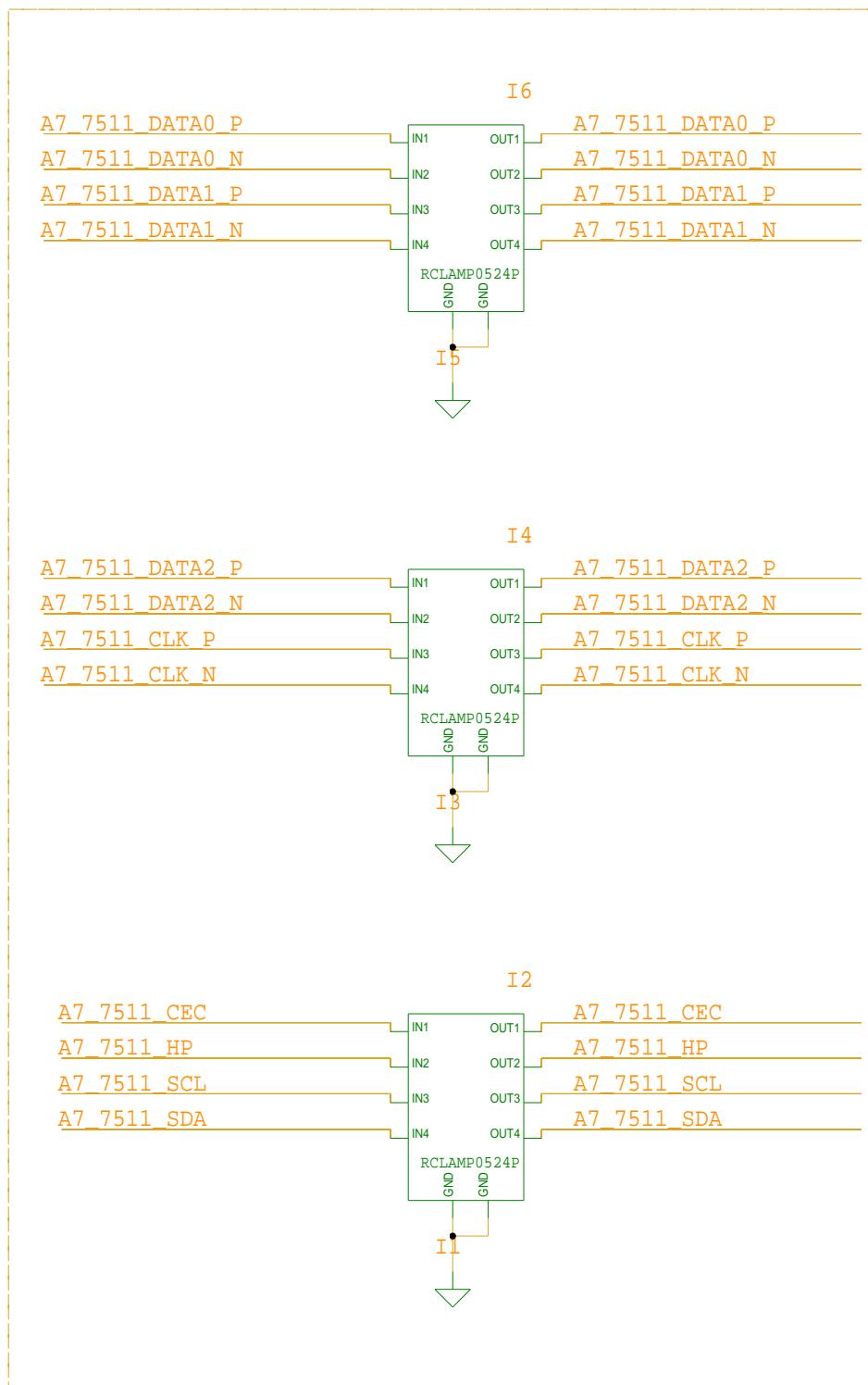


ARTIX-7 HDMI TRANSMITTER (2)

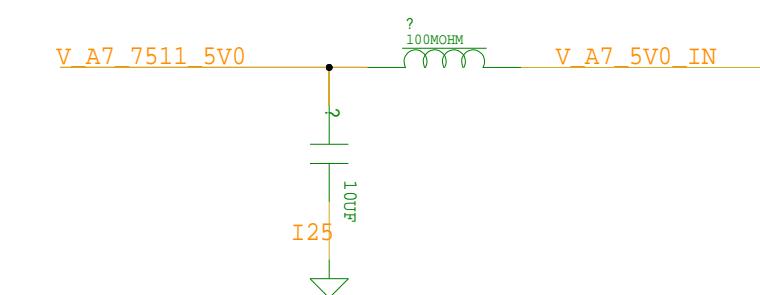
REVISED

ZONE	LTR	DESCRIPTION	DATE	APPR.
------	-----	-------------	------	-------

CHANGE CONNECTION DUE TO LAYOUT



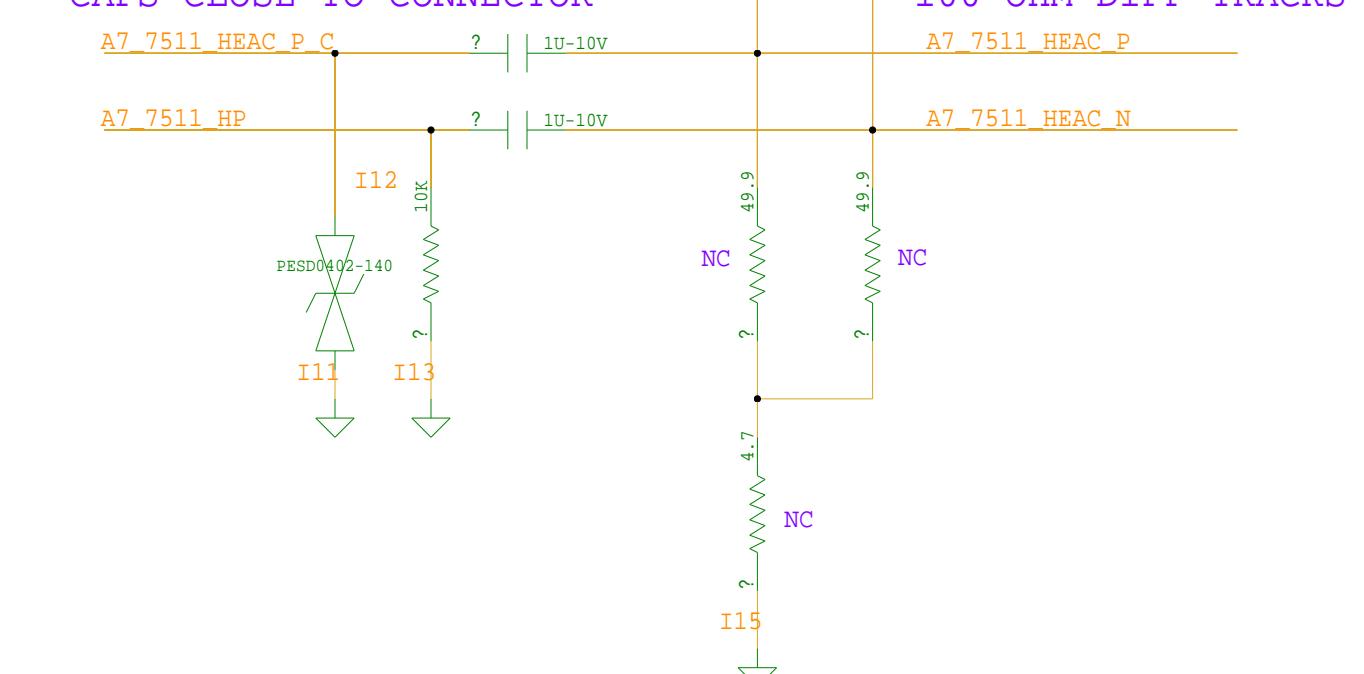
CLOSE TO HDMI CONNECTOR



A7_7511_CEC → IN4148 → V_A7_3V3_7511_MVDD

27.4K

CAPS CLOSE TO CONNECTOR



A7_7511_SCL → 1.8K-1% → V_A7_7511_5V0
A7_7511_SDA → 1.8K-1%

CADENCE DESIGN SYSTEMS, INC.

CADENCE

THIS DOCUMENT CONTAINS INFORMATION PROPRIETARY
TO CADENCE DESIGN SYSTEMS INC (CADENCE). USE
OR DISCLOSURE WITHOUT THE WRITTEN PERMISSION OF AN
OFFICER OF CADENCE IS EXPRESSLY FORBIDDEN.
COPYRIGHT (C) CADENCE 1988

DRAWING TITLE

SIZE

C

REV.

DRAWING NO.

SCALE

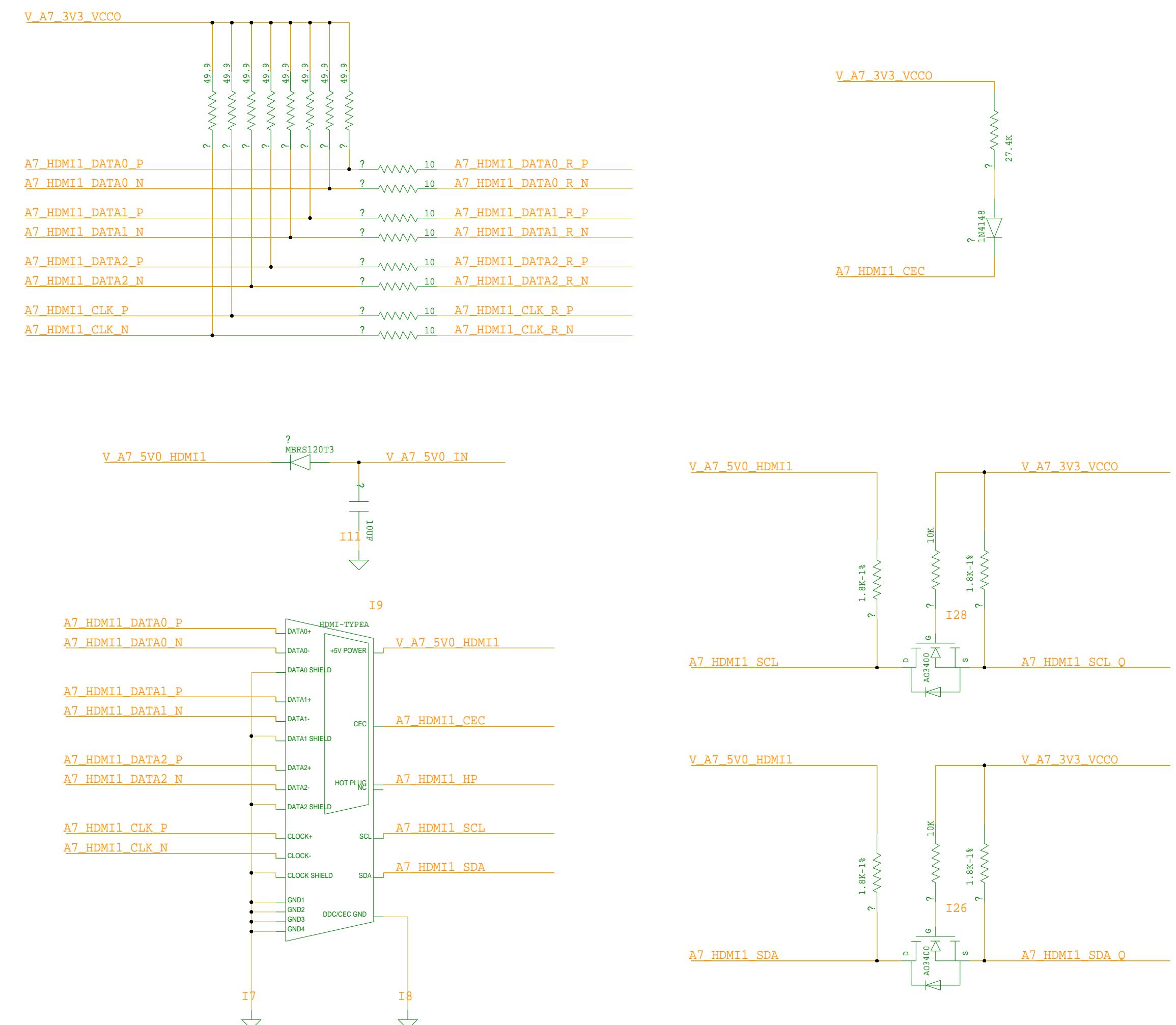
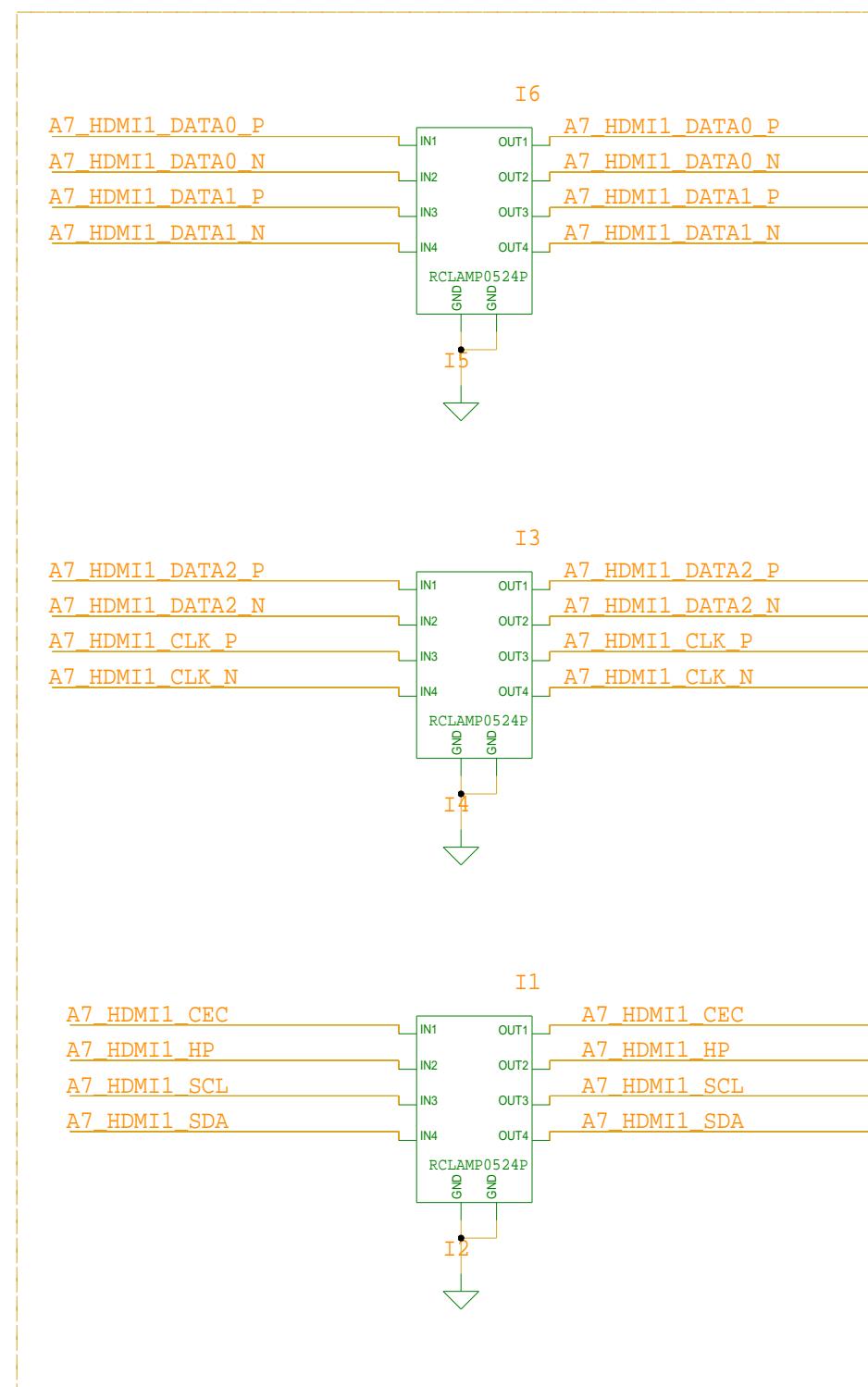
SHEET OF

REVISIONS

ZONE	LTR	DESCRIPTION	DATE	APPR.

ARTIX-7 HDMI INOUT (1)

CHANGE CONNECTION DUE TO LAYOUT



CADENCE DESIGN SYSTEMS, INC.
 CADENCE

THIS DOCUMENT CONTAINS INFORMATION PROPRIETARY
 TO CADENCE DESIGN SYSTEMS INC (CADENCE). USE
 OR DISCLOSURE WITHOUT THE WRITTEN PERMISSION OF AN
 OFFICER OF CADENCE IS EXPRESSLY FORBIDDEN.
 COPYRIGHT (C) CADENCE 1988

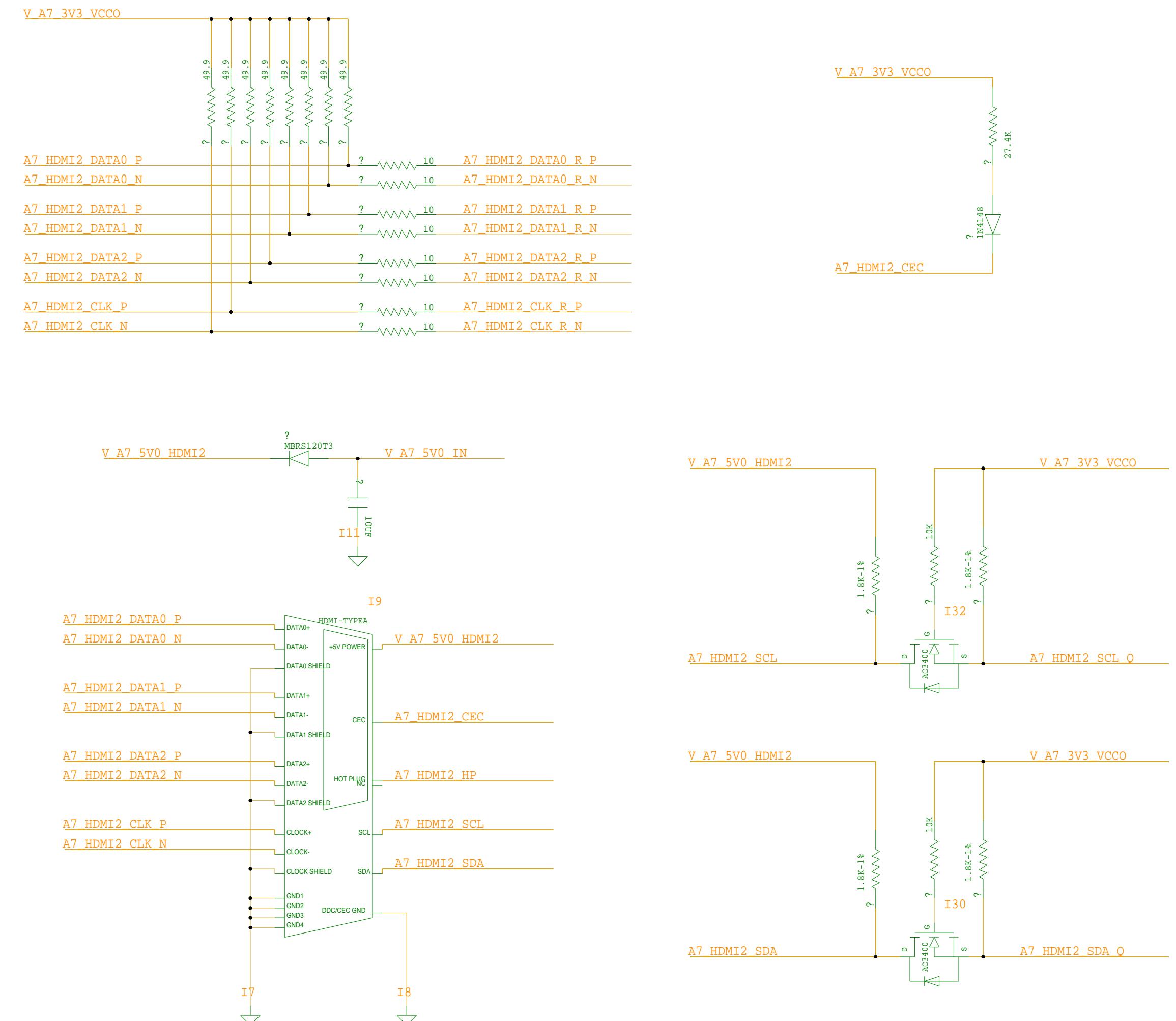
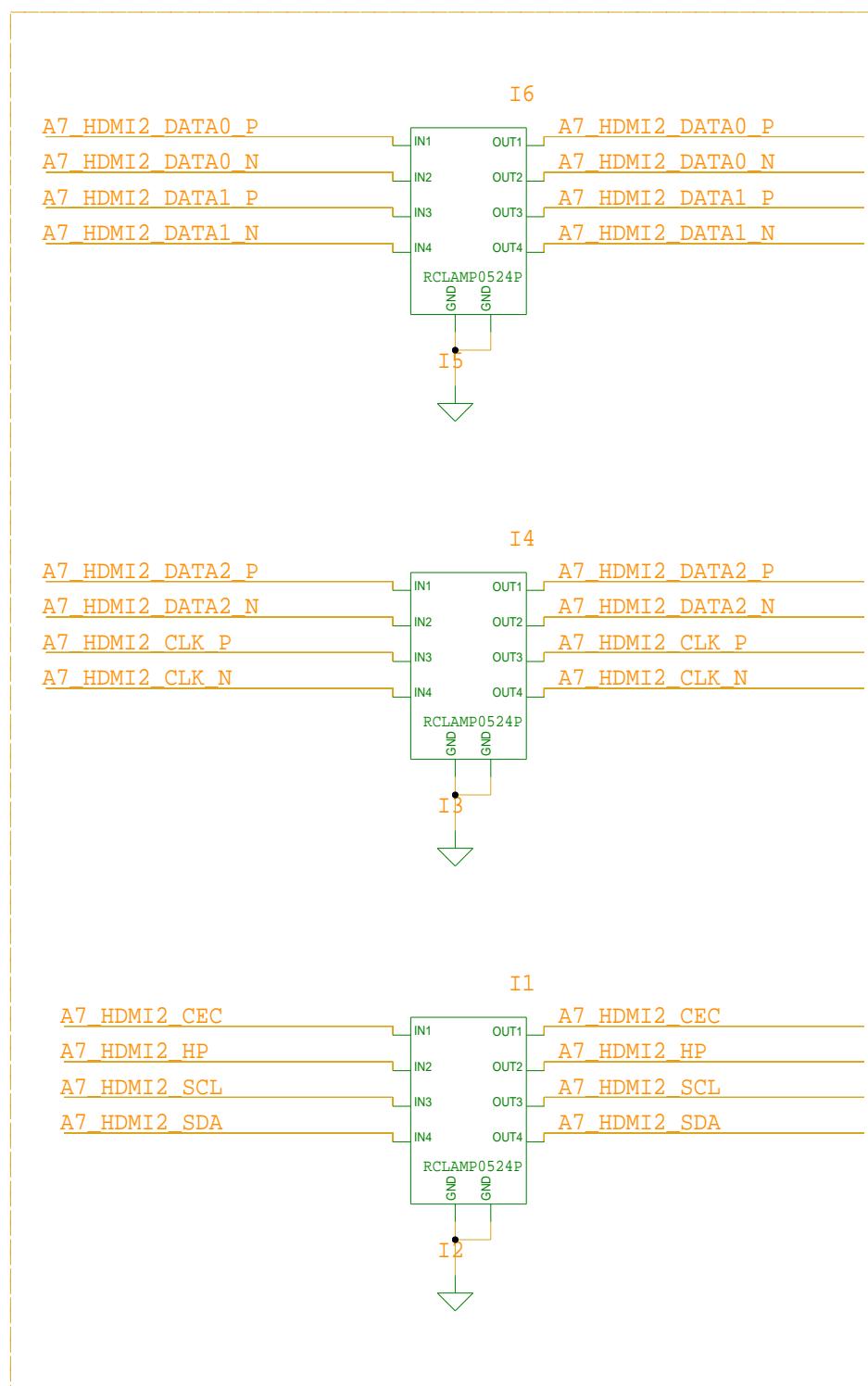
DRAWING TITLE		SIZE		REV.		DRAWING NO.	
SCALE	OF	INCHES	MM	INCHES	MM	INCHES	MM

ARTIX-7 HDMI INOUT (2)

REVISED

ZONE	LTR	DESCRIPTION	DATE	APPR.

CHANGE CONNECTION DUE TO LAYOUT



CADENCE DESIGN SYSTEMS, INC.
CADENCE

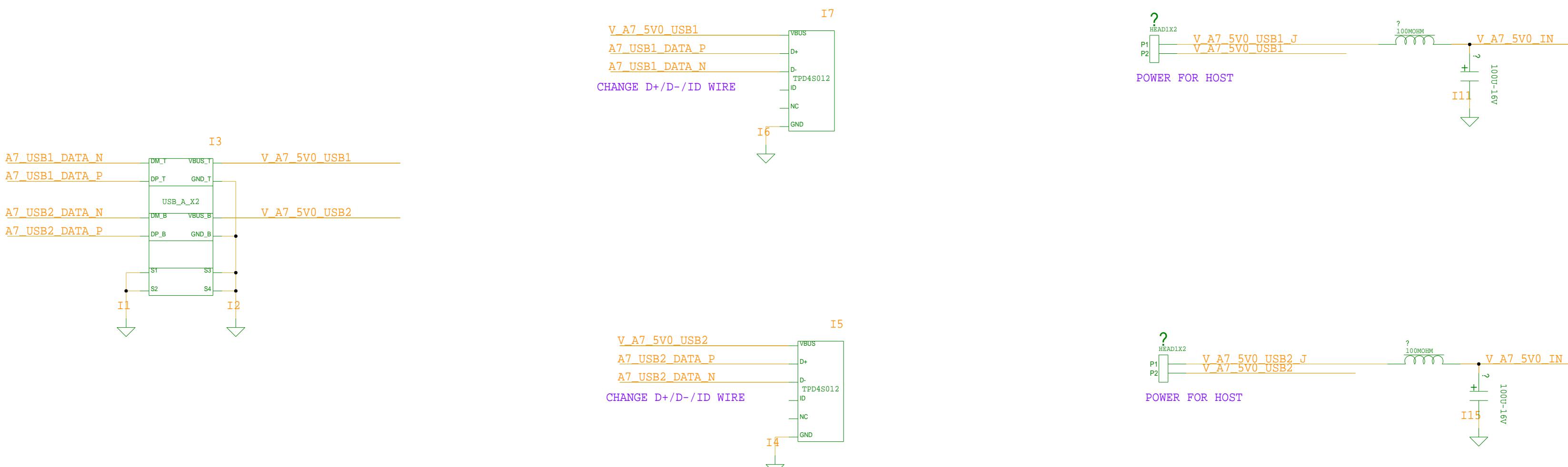
THIS DOCUMENT CONTAINS INFORMATION PROPRIETARY
TO CADENCE DESIGN SYSTEMS INC (CADENCE). USE
OR DISCLOSURE WITHOUT THE WRITTEN PERMISSION OF AN
OFFICER OF CADENCE IS EXPRESSLY FORBIDDEN.
COPYRIGHT (C) CADENCE 1988

DRAWING TITLE		SIZE		REV.		DRAWING NO.	
SCALE	OF	REV.	SIZE	DRAWING NO.	OF	SCALE	OF

ARTIX-7 USB INOUT

REVISIONS

ZONE	LTR	DESCRIPTION	DATE	APPR.



CADENCE DESIGN SYSTEMS, INC.
 CADENCE

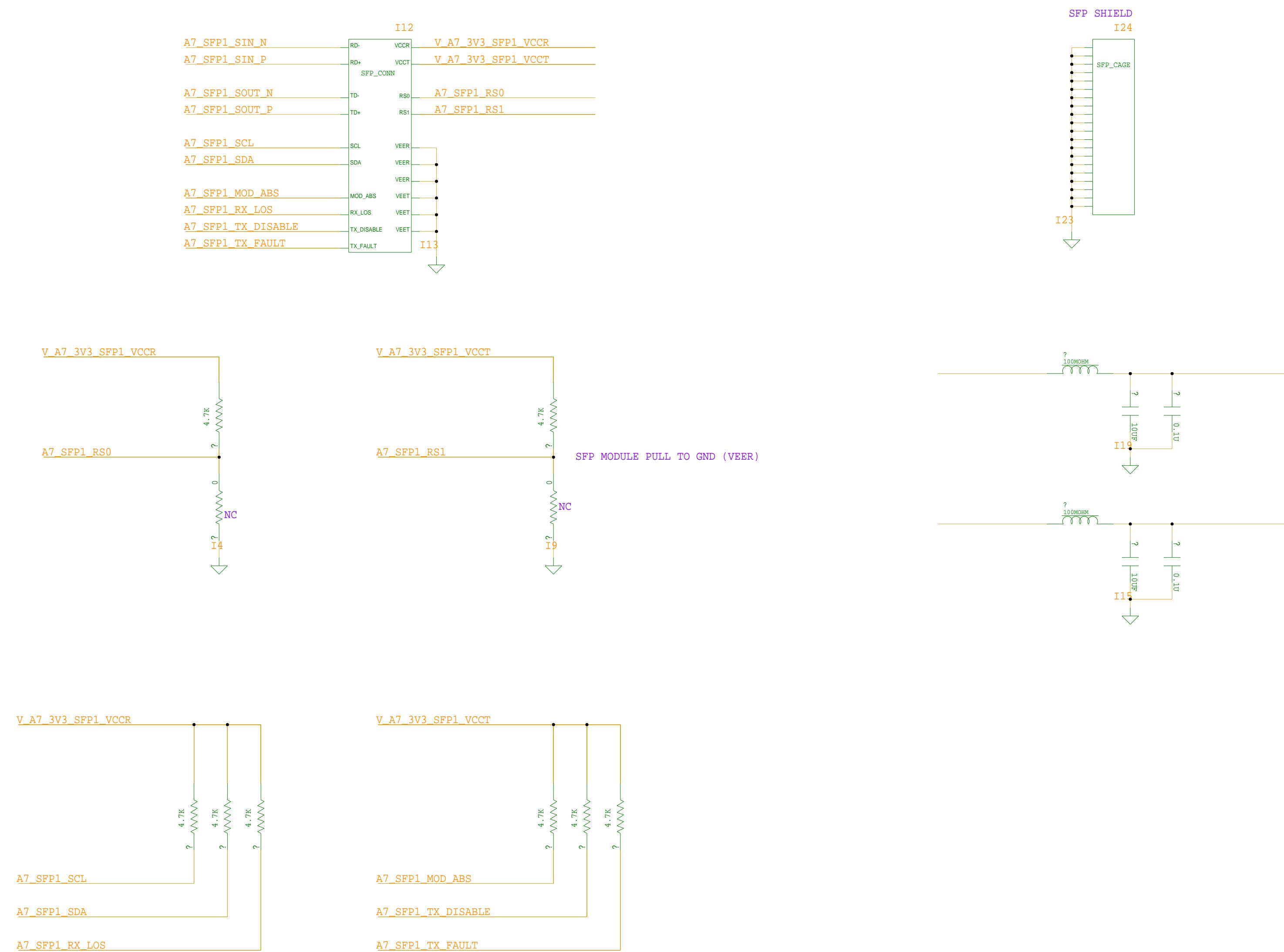
THIS DOCUMENT CONTAINS INFORMATION PROPRIETARY
 TO CADENCE DESIGN SYSTEMS INC (CADENCE). USE
 OR DISCLOSURE WITHOUT THE WRITTEN PERMISSION OF AN
 OFFICER OF CADENCE IS EXPRESSLY FORBIDDEN.
 COPYRIGHT (C) CADENCE 1988

DRAWING TITLE		SIZE		REV.		DRAWING NO.	
		C					
SCALE						SHEET	OF

REVISIONS

ZONE	LTR	DESCRIPTION	DATE	APPR.

ARTIX-7 SFP+/SFP INOUT (1)



CADENCE DESIGN SYSTEMS, INC.
 CADENCE

THIS DOCUMENT CONTAINS INFORMATION PROPRIETARY
 TO CADENCE DESIGN SYSTEMS INC (CADENCE). USE
 OR DISCLOSURE WITHOUT THE WRITTEN PERMISSION OF AN
 OFFICER OF CADENCE IS EXPRESSLY FORBIDDEN.
 COPYRIGHT (C) CADENCE 1988

DRAWING TITLE

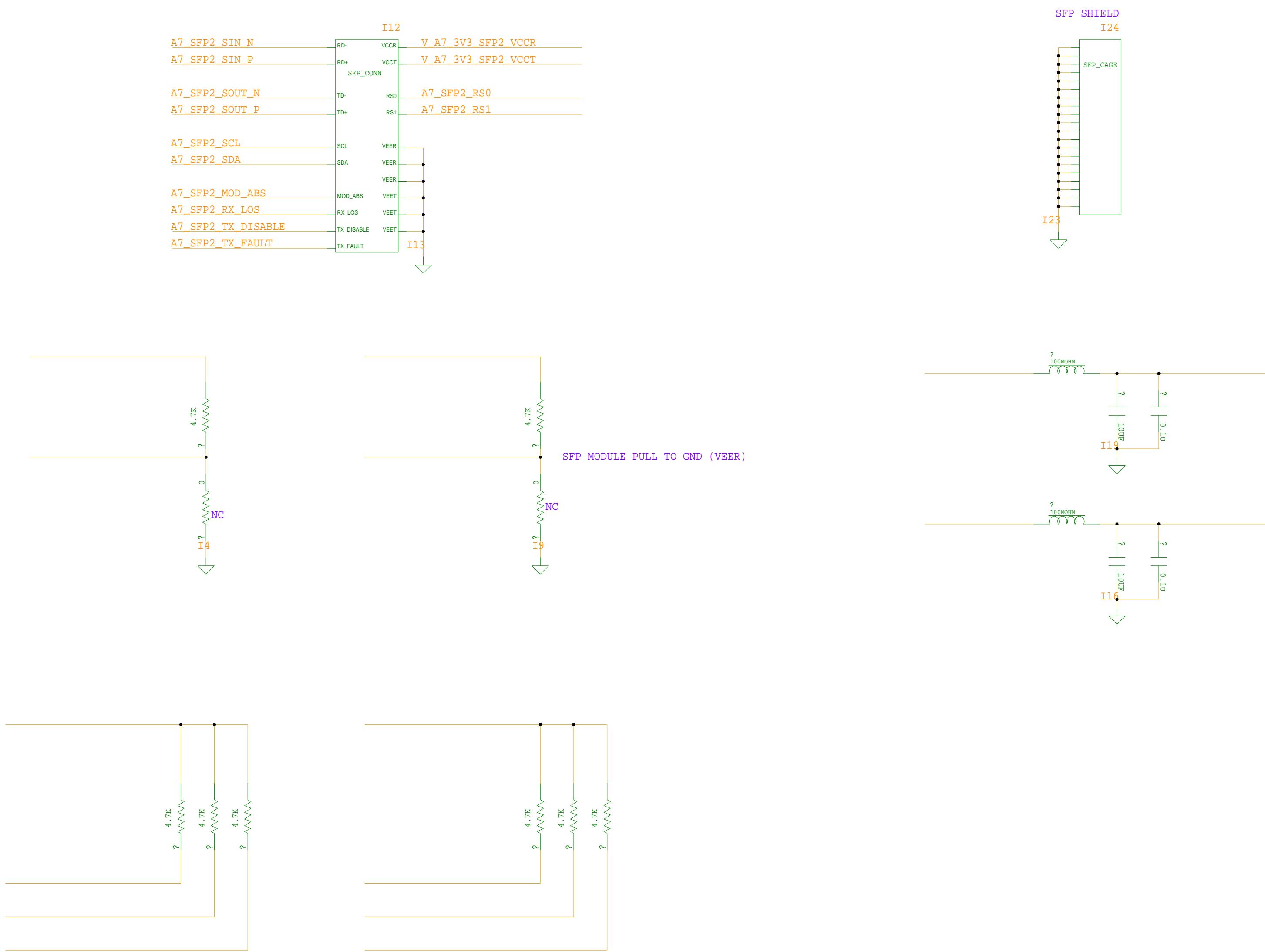
SIZE	REV.	DRAWING NO.

SCALE SHEET OF

REVISIONS

ZONE	LTR	DESCRIPTION	DATE	APPR.

ARTIX-7 SFP+/SFP INOUT (2)



CADENCE DESIGN SYSTEMS, INC.



THIS DOCUMENT CONTAINS INFORMATION PROPRIETARY
TO CADENCE DESIGN SYSTEMS INC (CADENCE). USE
OR DISCLOSURE WITHOUT THE WRITTEN PERMISSION OF AN
OFFICER OF CADENCE IS EXPRESSLY FORBIDDEN.
COPYRIGHT (C) CADENCE 1988

DRAWING TITLE

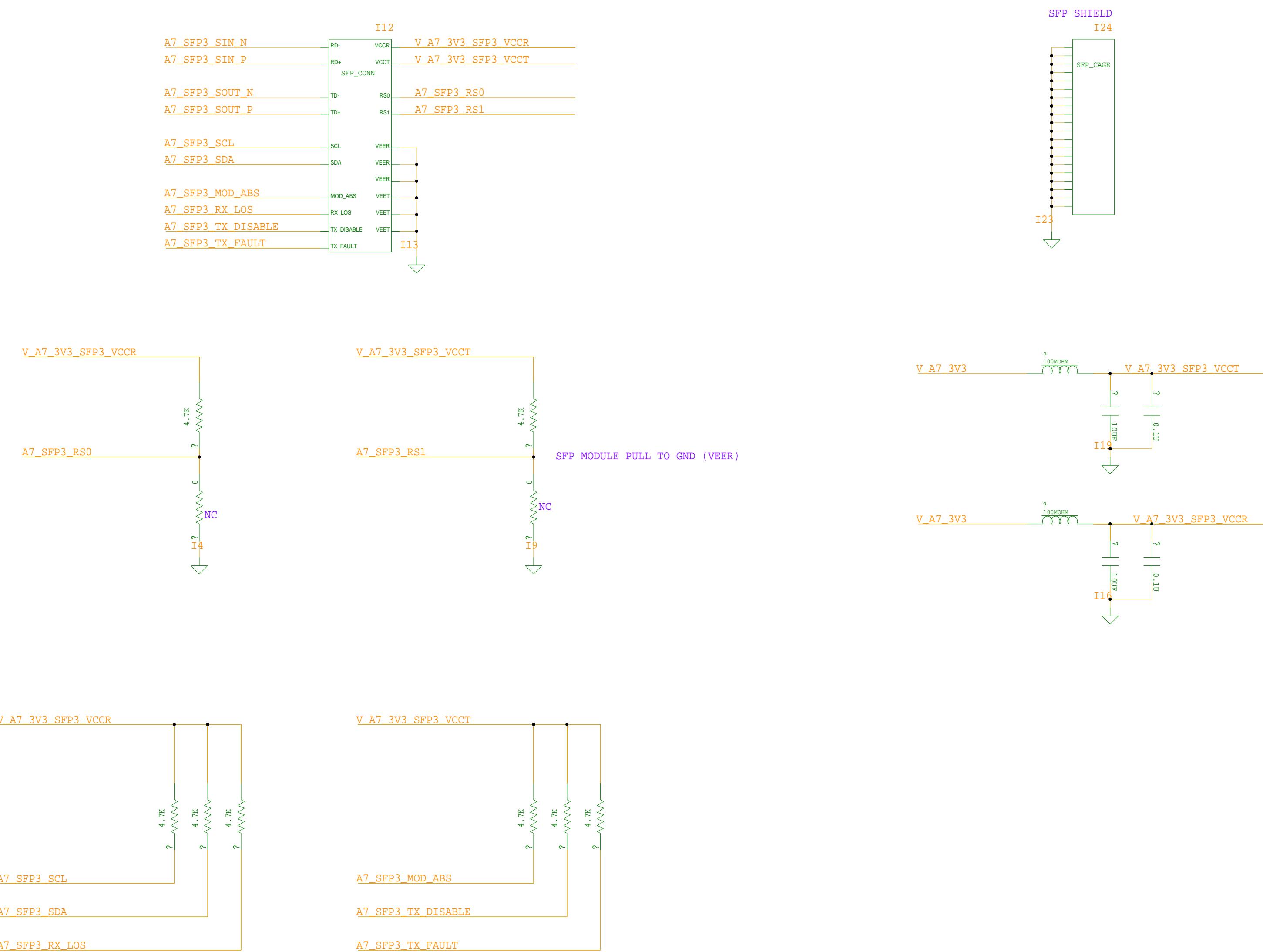
SIZE **C** REV.

SCALE SHEET OF

ARTIX-7 SFP+/SFP INOUT (3)

REVISIONS

ZONE	LTR	DESCRIPTION	DATE	APPR.



CADENCE DESIGN SYSTEMS, INC.
 CADENCE

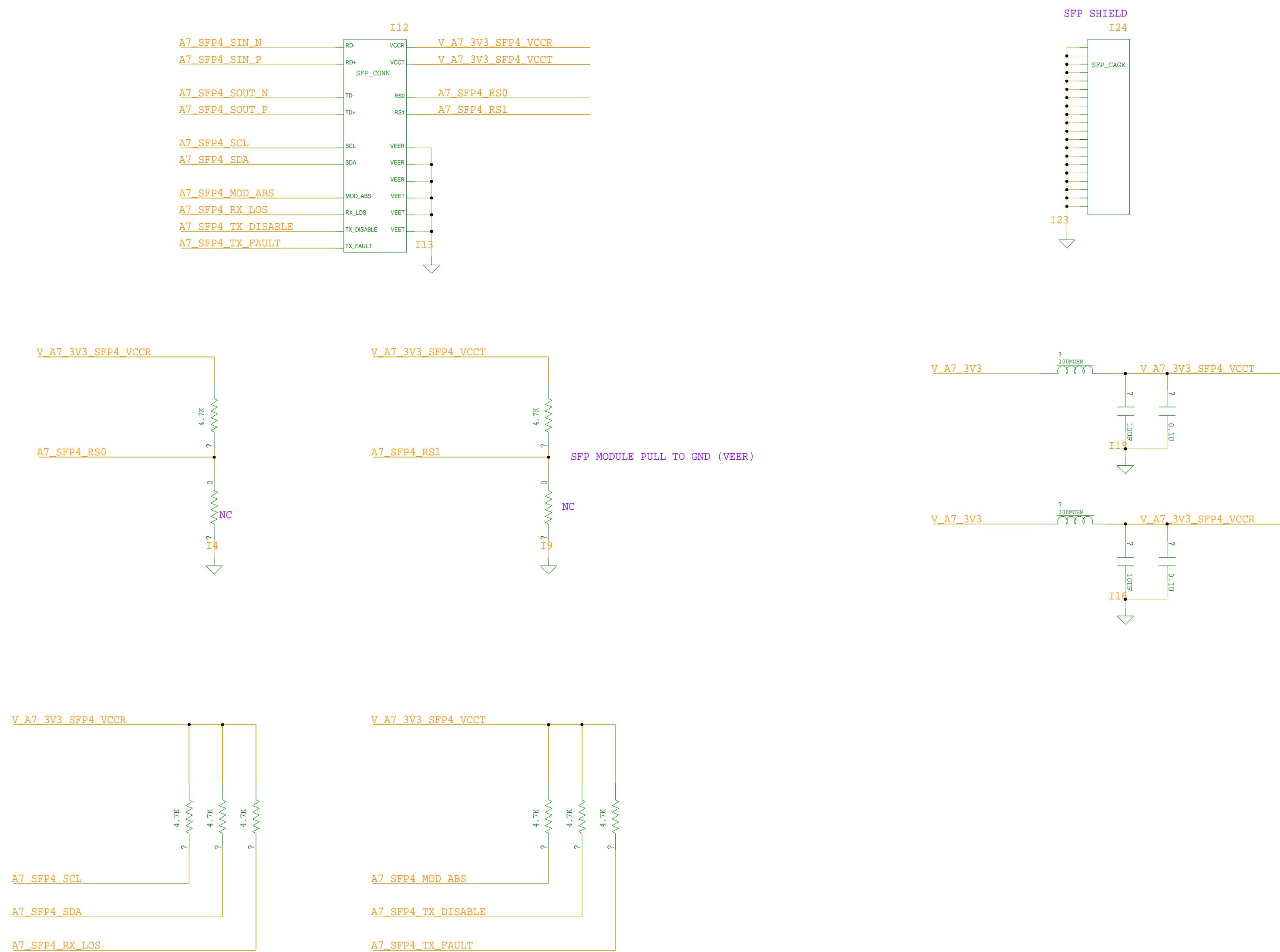
THIS DOCUMENT CONTAINS INFORMATION PROPRIETARY
 TO CADENCE DESIGN SYSTEMS INC (CADENCE). USE
 OR DISCLOSURE WITHOUT THE WRITTEN PERMISSION OF AN
 OFFICER OF CADENCE IS EXPRESSLY FORBIDDEN.
 COPYRIGHT (C) CADENCE 1988

DRAWING TITLE		SIZE		REV.		DRAWING NO.	
SCALE	OF	INCHES	MM	1	2	3	4

REVISIONS

ZONE	LTR	DESCRIPTION	DATE	APPR.

ARTIX-7 SFP+/SFP INOUT (4)



CADENCE DESIGN SYSTEMS, INC.
 CADENCE

THIS DOCUMENT CONTAINS INFORMATION PROPRIETARY
 TO CADENCE DESIGN SYSTEMS INC (CADENCE). USE
 OR DISCLOSURE WITHOUT THE WRITTEN PERMISSION OF AN
 OFFICER OF CADENCE IS EXPRESSLY FORBIDDEN.
 COPYRIGHT (C) CADENCE 1988

DRAWING TITLE		SIZE		REV.		DRAWING NO.	
		C					
SCALE							
SHEET	OF						

ARTIX-7 PCIE X16 CONN

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPR.

F

F

E

E

D

D

C

C

B

B

A

A

CADENCE DESIGN SYSTEMS, INC.
 CADENCE

THIS DOCUMENT CONTAINS INFORMATION PROPRIETARY
TO CADENCE DESIGN SYSTEMS INC (CADENCE). USE
OR DISCLOSURE WITHOUT THE WRITTEN PERMISSION OF AN
OFFICER OF CADENCE IS EXPRESSLY FORBIDDEN.
COPYRIGHT (C) CADENCE 1988

DRAWING TITLE

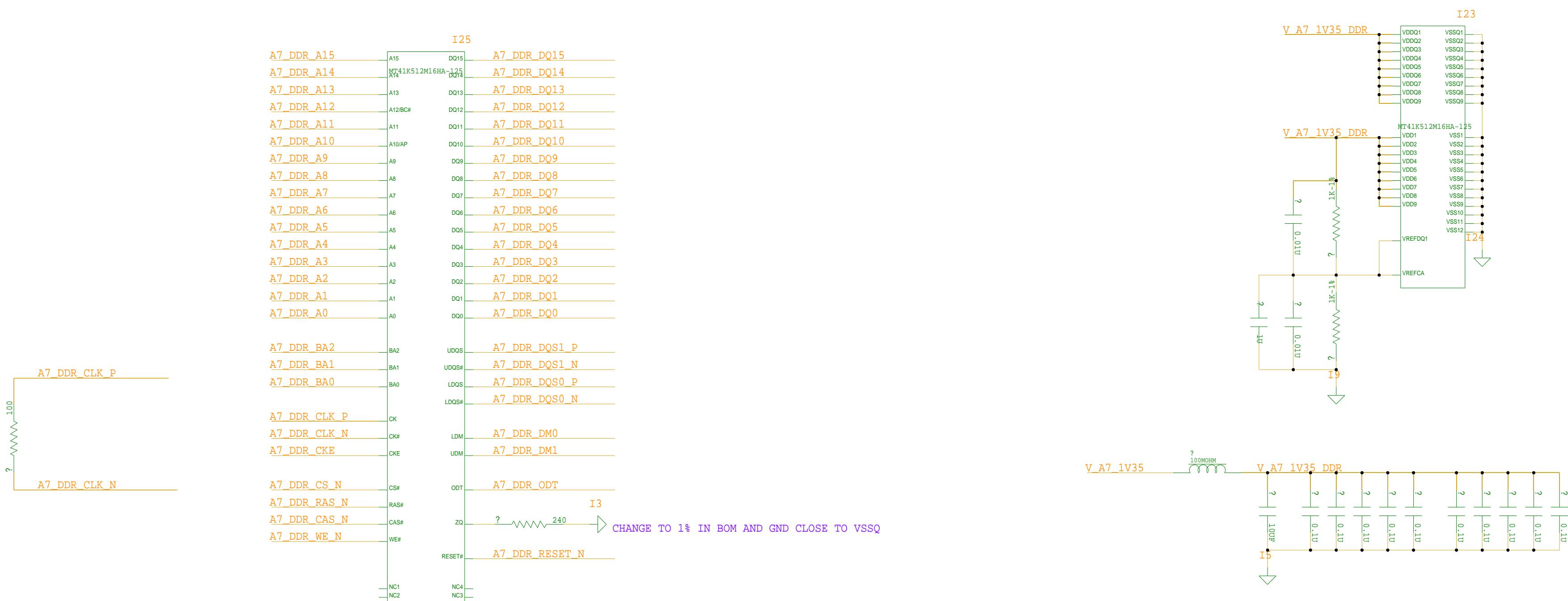
SIZE  REV. DRAWING NO.

SCALE SHEET OF

ARTIX-7 DDR3

REVISIONS

ZONE	LTR	DESCRIPTION	DATE	APPR.

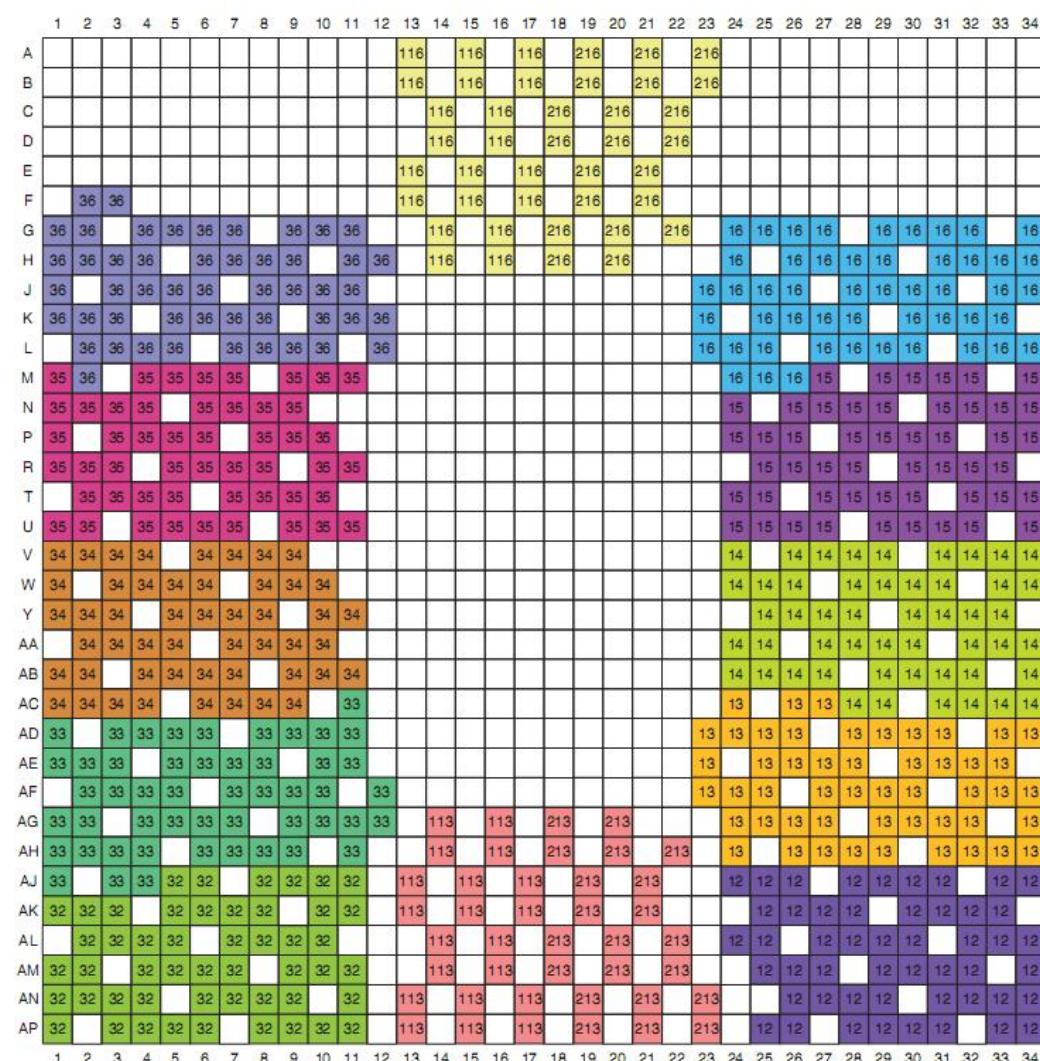


CADENCE DESIGN SYSTEMS, INC.  CADENCE	DRAWING TITLE		
	SIZE 	REV.	DRAWING NO.
THIS DOCUMENT CONTAINS INFORMATION PROPRIETARY TO CADENCE DESIGN SYSTEMS INC (CADENCE). USE OR DISCLOSURE WITHOUT THE WRITTEN PERMISSION OF AN OFFICER OF CADENCE IS EXPRESSLY FORBIDDEN. COPYRIGHT (C) CADENCE 1988		SCALE	SHEET OF

ARTIX-7 PINOUT MAP

REVISIONS

ZONE	LTR	DESCRIPTION	DATE	APPR.



BANK0 : 3.3V CONFIG

BANK36 : 3.3V USB INOUT 1/2 SFP+ MUX

BANK35 : 3.3V NC

BANK34 : 1.35V DDR3

BANK33 : 3.3V NC

BANK32 : 3.3V NC

BANK16 : 3.3V NC

BANK15 : 3.3V HDMI RECEIVER

BANK14 : 3.3V SPI FLASH

BANK13 : 3.3V HDMI INOUT 1/2

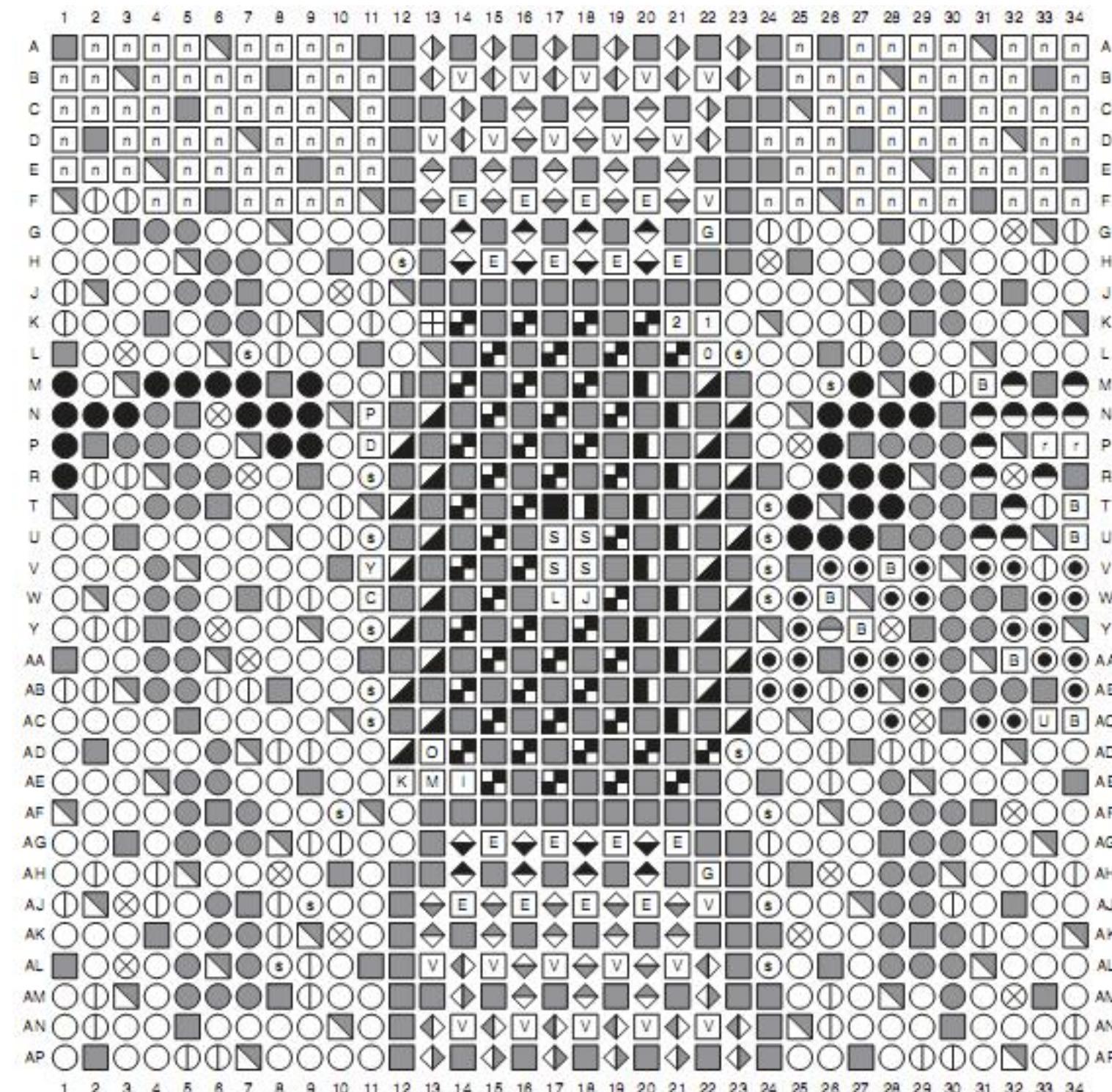
BANK12 : 3.3V HDMI TRANSMITTER

BANK116 : 3.3V PCIE X4

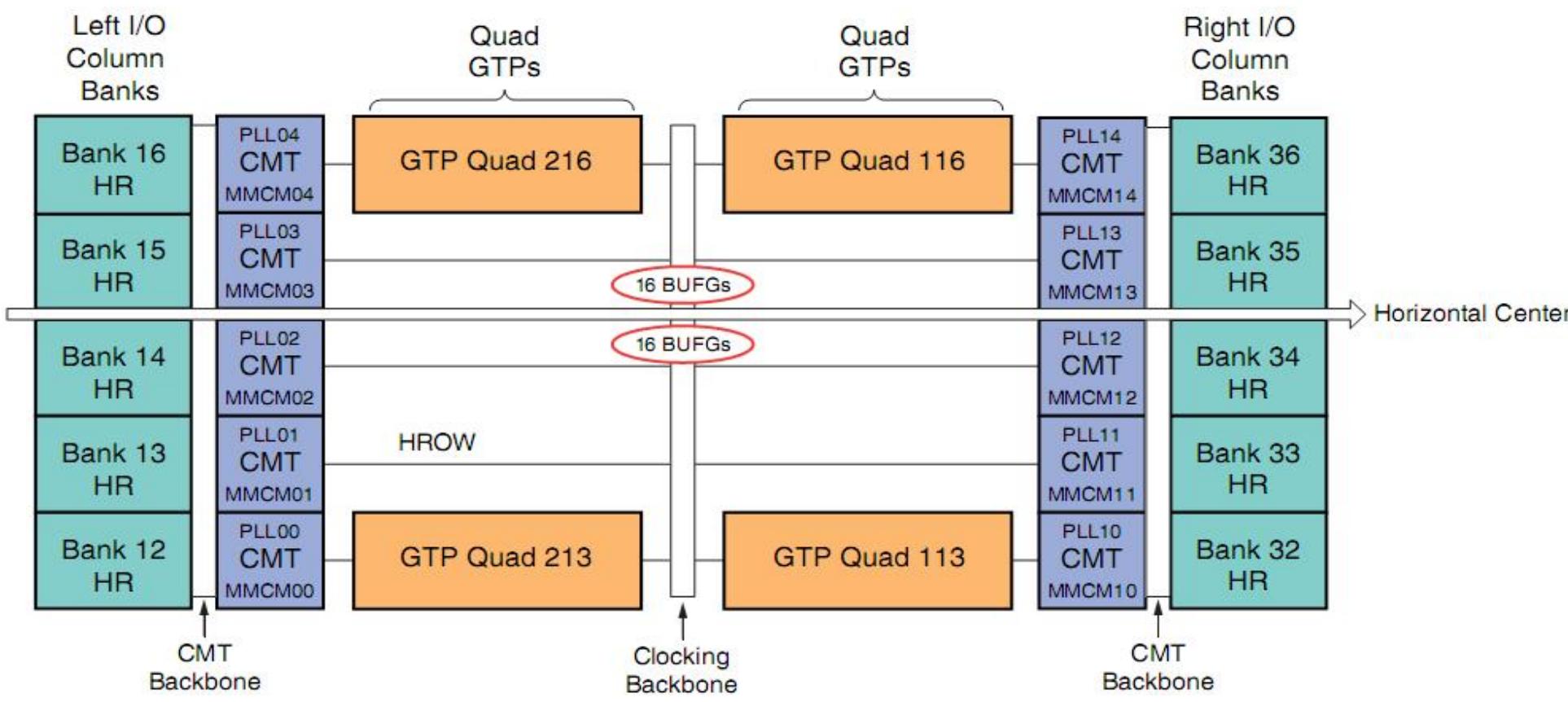
BANK216 : 3.3V SFP+ *4

BANK113 : 3.3V PCIE X4

BANK213 : 3.3V PCIE X4



All HR I/O banks and the GTP Quads are fully bonded out in this package.



User I/O Pins	Transceiver Pins	Dedicated Pins	Other Pins
○ IO_LXXY_# ○ IO_XX_#	E MGTAVCC_G# V MGTAVTT_G# A MGTVCVAUX_G# ◀ MGTAVTTRCAL G MGTREFREF B ADV_B B FCS_B B FOE_B B MOSI B FWE_B B DOUT_CSO_B B CSI_B B PUDC_B U RDWR_B r RSD-RS1 ● ADDP/ADON-AD15P/AD15N ○ EMCCLK	C CCLK_0 V CFGBVS_0 A DONE_0 ◀ MGTAVTTRCAL J DXP_0 L DXN_0 ■ GNDADC_0 Y INIT_B_0 O M0_0 1 M1_0 2 M2_0 P PROGRAM_B_0 K TCK_0 I TDI_0 O TDO_0 M TMS_0 ■ VCCADC_0 □ VCCBATT_0	GND VCCAUX_IO_G# VCCAUX VCCINT VCCO_# VCCBRAM NC
Multi-Function Pins			
	B ADV_B B FCS_B B FOE_B B MOSI B FWE_B B DOUT_CSO_B B CSI_B B PUDC_B U RDWR_B r RSD-RS1 ● ADDP/ADON-AD15P/AD15N ○ EMCCLK	E VRN ○ VRP ○ VREF ● D00-D31 ● A00-A28 ○ DQS ○ MRCC ○ SRCC	

CADENCE DESIGN SYSTEMS, INC.

CADENCE

THIS DOCUMENT CONTAINS INFORMATION PROPRIETARY
TO CADENCE DESIGN SYSTEMS INC (CADENCE). USE
OR DISCLOSURE WITHOUT THE WRITTEN PERMISSION OF AN
OFFICER OF CADENCE IS EXPRESSLY FORBIDDEN.
COPYRIGHT (C) CADENCE 1988

DRAWING TITLE

SIZE

REV.

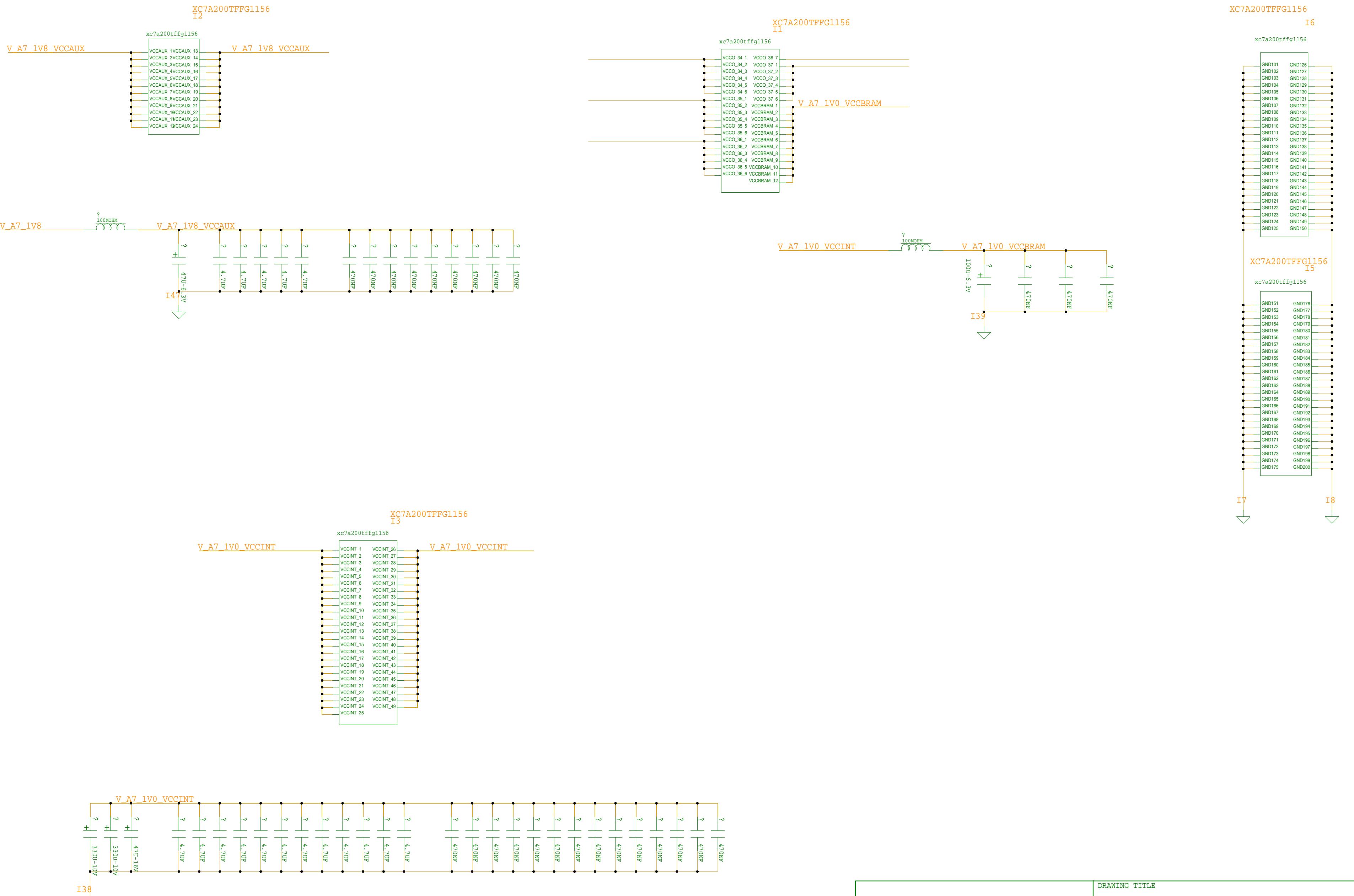
SCALE

SHEET OF

ARTIX-7 BANK POWER (1)

REVISONS

ZONE	LTR	DESCRIPTION	DATE	APPR.



CADENCE DESIGN SYSTEMS, INC.

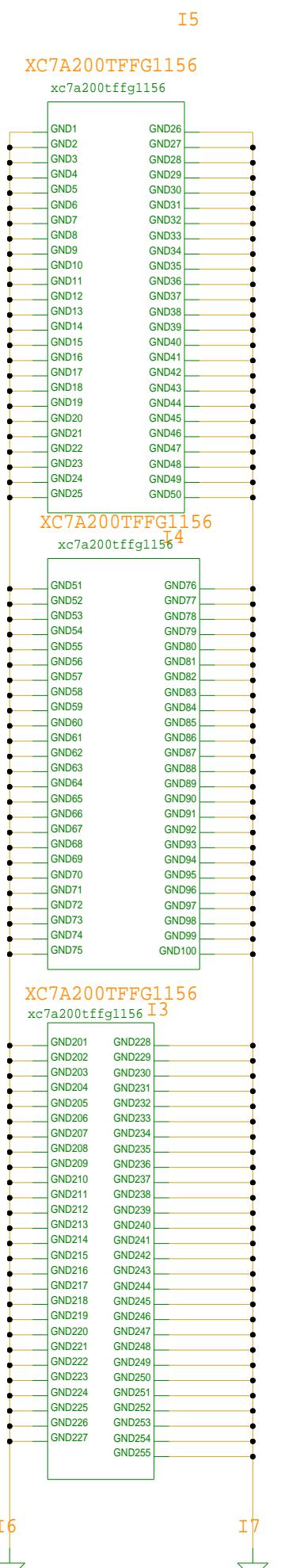
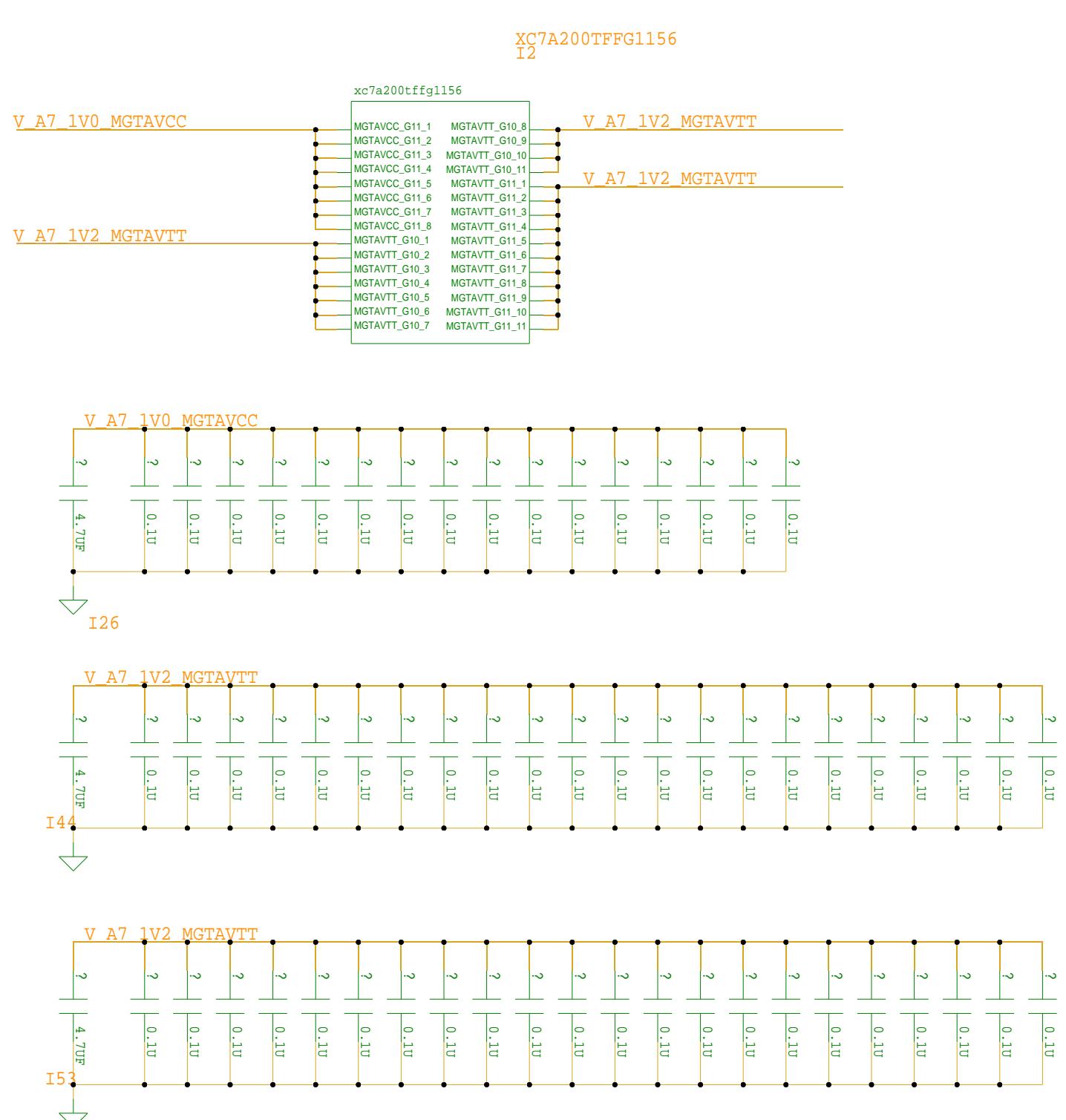
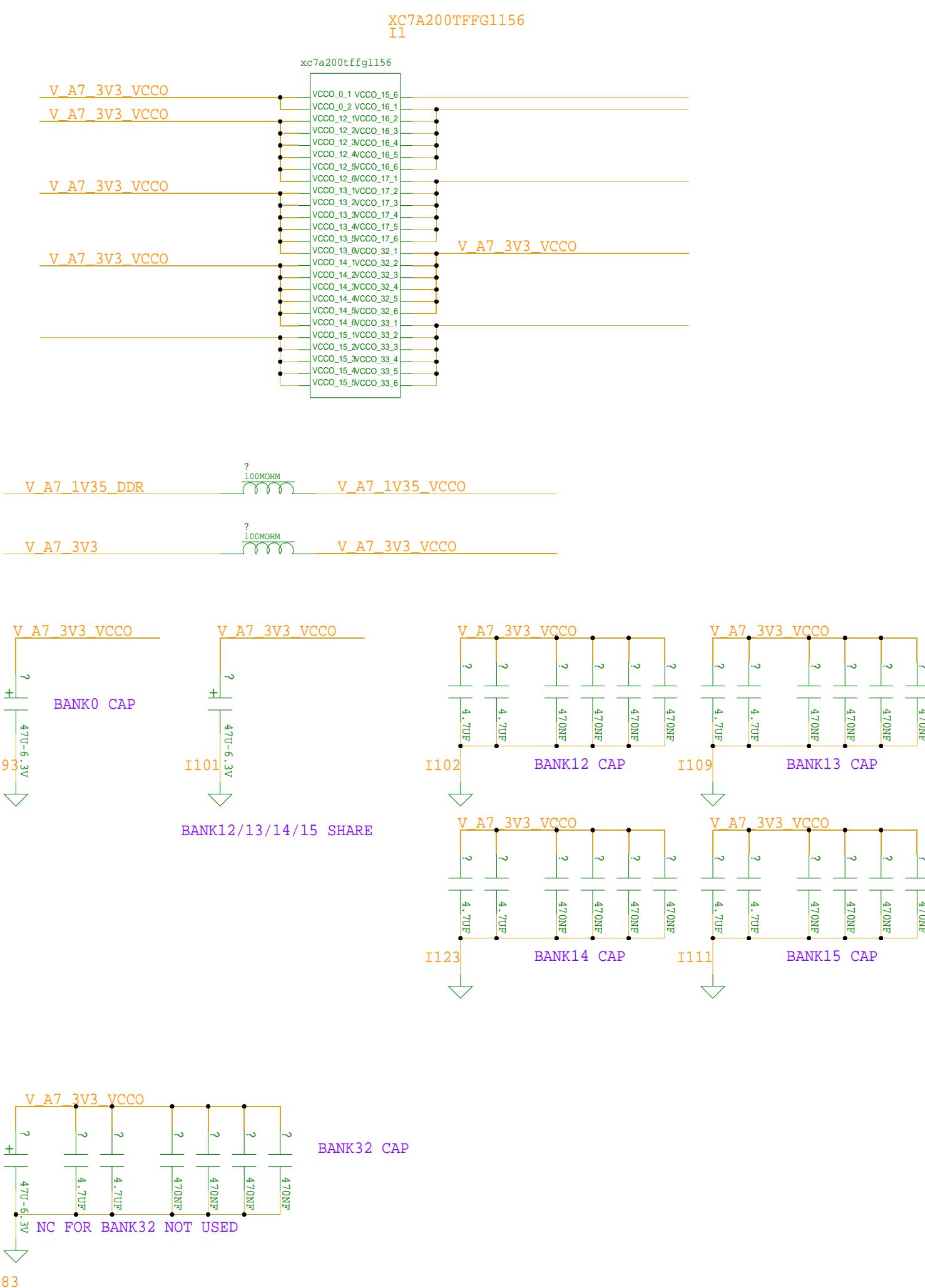


THIS DOCUMENT CONTAINS INFORMATION PROPRIETARY
TO CADENCE DESIGN SYSTEMS INC (CADENCE). USE
OR DISCLOSURE WITHOUT THE WRITTEN PERMISSION OF AN
OFFICER OF CADENCE IS EXPRESSLY FORBIDDEN.
COPYRIGHT (C) CADENCE 1988

DRAWING TITLE		SIZE		DRAWING NO.	
SCALE	REV.				

ARTIX-7 BANK POWER (2)

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPR.



CADENCE DESIGN SYSTEMS, INC.

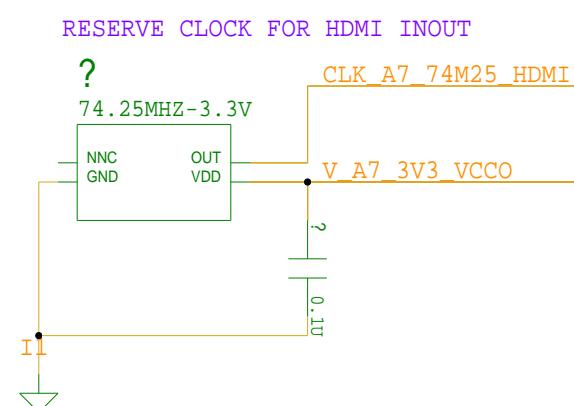
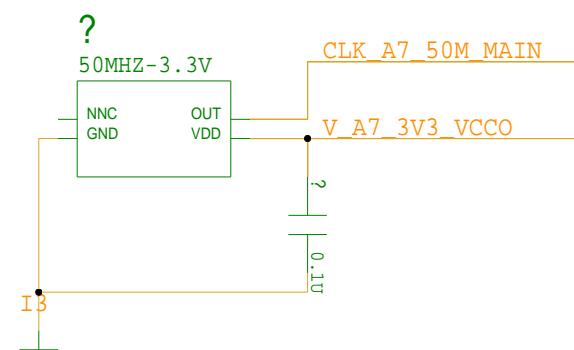


THIS DOCUMENT CONTAINS INFORMATION PROPRIETARY
TO CADENCE DESIGN SYSTEMS INC (CADENCE). USE
OR DISCLOSURE WITHOUT THE WRITTEN PERMISSION OF AN
OFFICER OF CADENCE IS EXPRESSLY FORBIDDEN.
COPYRIGHT (C) CADENCE 1988

DRAWING TITLE		
SIZE	REV.	DRAWING NO.
SCALE		SHEET OF

ARTIX-7 CLOCK

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPR.



CADENCE DESIGN SYSTEMS, INC.
 CADENCE

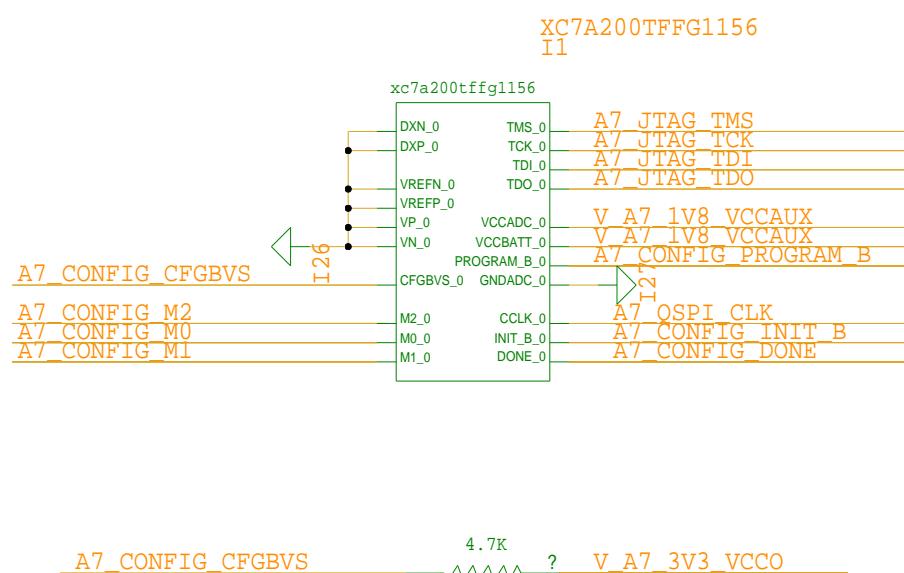
THIS DOCUMENT CONTAINS INFORMATION PROPRIETARY
TO CADENCE DESIGN SYSTEMS INC (CADENCE). USE
OR DISCLOSURE WITHOUT THE WRITTEN PERMISSION OF AN
OFFICER OF CADENCE IS EXPRESSLY FORBIDDEN.
COPYRIGHT (C) CADENCE 1988

DRAWING TITLE			
SIZE	REV.	DRAWING NO.	
C			
SCALE			SHEET OF

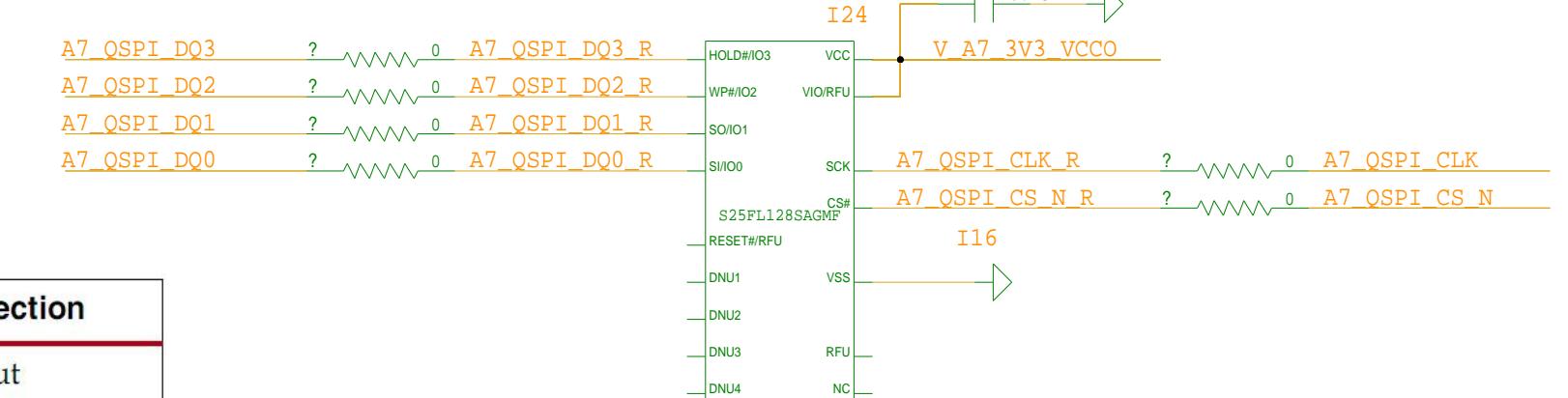
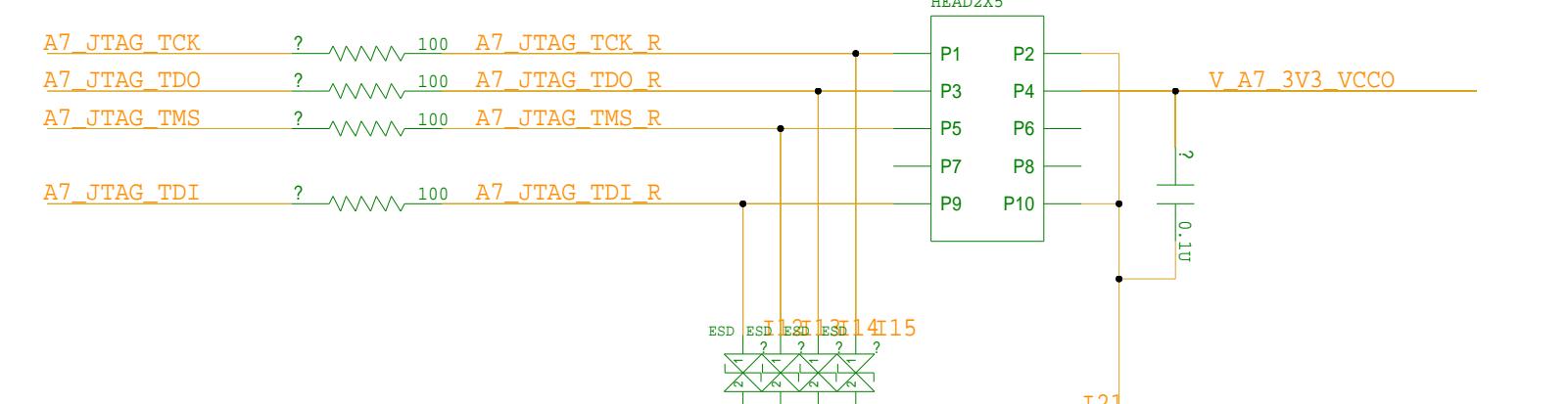
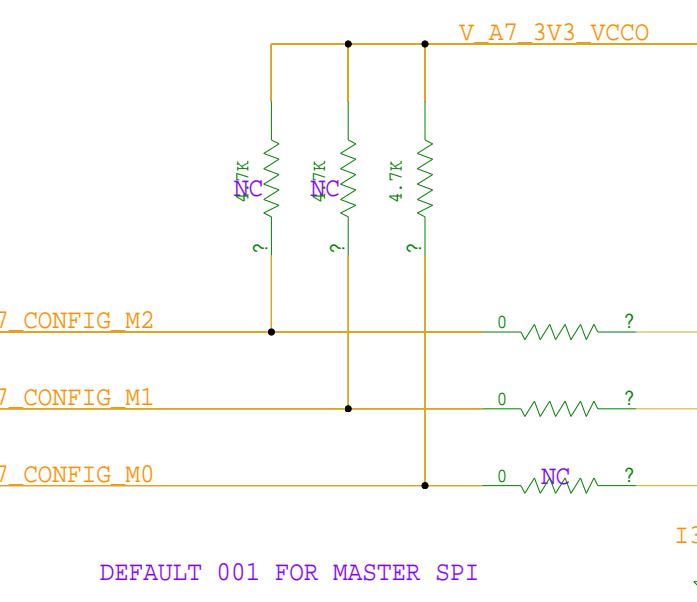
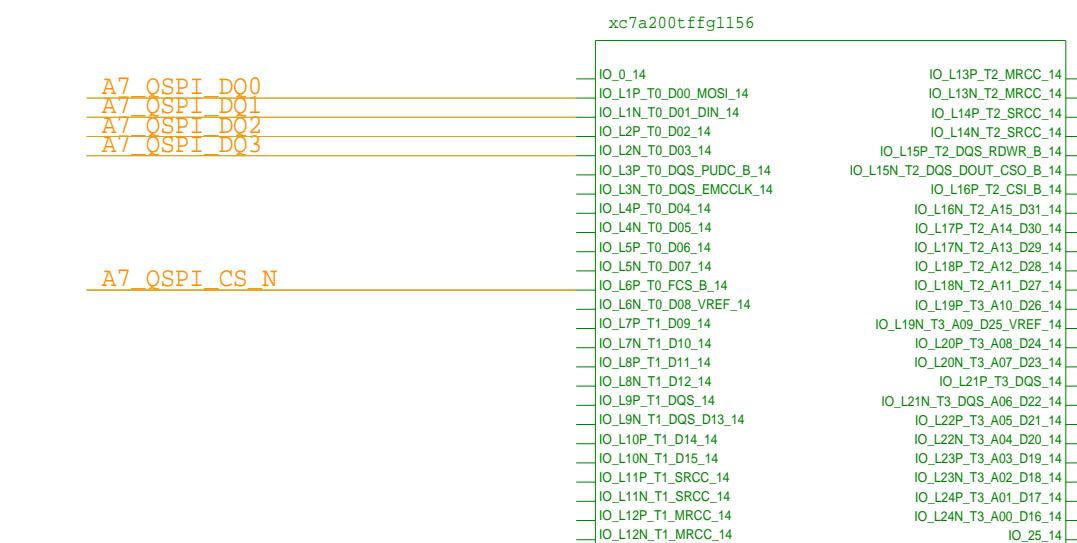
REVISIONS

ZONE	LTR	DESCRIPTION	DATE	APPR.

ARTIX-7 BANK0/14 CONFIG



CFGBVS Pin Connection	Supported Configuration Banks 0/14/15 V _{cco} Supply and I/O Signal Voltages		
	Spartan-7, Artix-7, Kintex-7	Virtex-7 T, XT	Virtex-7 HT
Banks Affected	0, 14, 15	0	none
V _{cco} _0 (3.3V or 2.5V)	3.3V or 2.5V	3.3V or 2.5V	1.8V (no CFGBVS)
GND	1.8V or 1.5V	1.8V or 1.5V	

XC7A200TFFG1156
I25

Configuration Mode	M[2:0]	Bus Width	CCLK Direction
Master Serial	000	x1	Output
Master SPI	001	x1, x2, x4	Output
Master BPI	010	x8, x16	Output
Master SelectMAP	100	x8, x16	Output
JTAG	101	x1	Not Applicable
Slave SelectMAP	110	x8, x16, x32 ⁽¹⁾	Input
Slave Serial ⁽²⁾	111	x1	Input

CADENCE DESIGN SYSTEMS, INC.
CADENCETHIS DOCUMENT CONTAINS INFORMATION PROPRIETARY
TO CADENCE DESIGN SYSTEMS INC (CADENCE). USE
OR DISCLOSURE WITHOUT THE WRITTEN PERMISSION OF AN
OFFICER OF CADENCE IS EXPRESSLY FORBIDDEN.
COPYRIGHT (C) CADENCE 1988

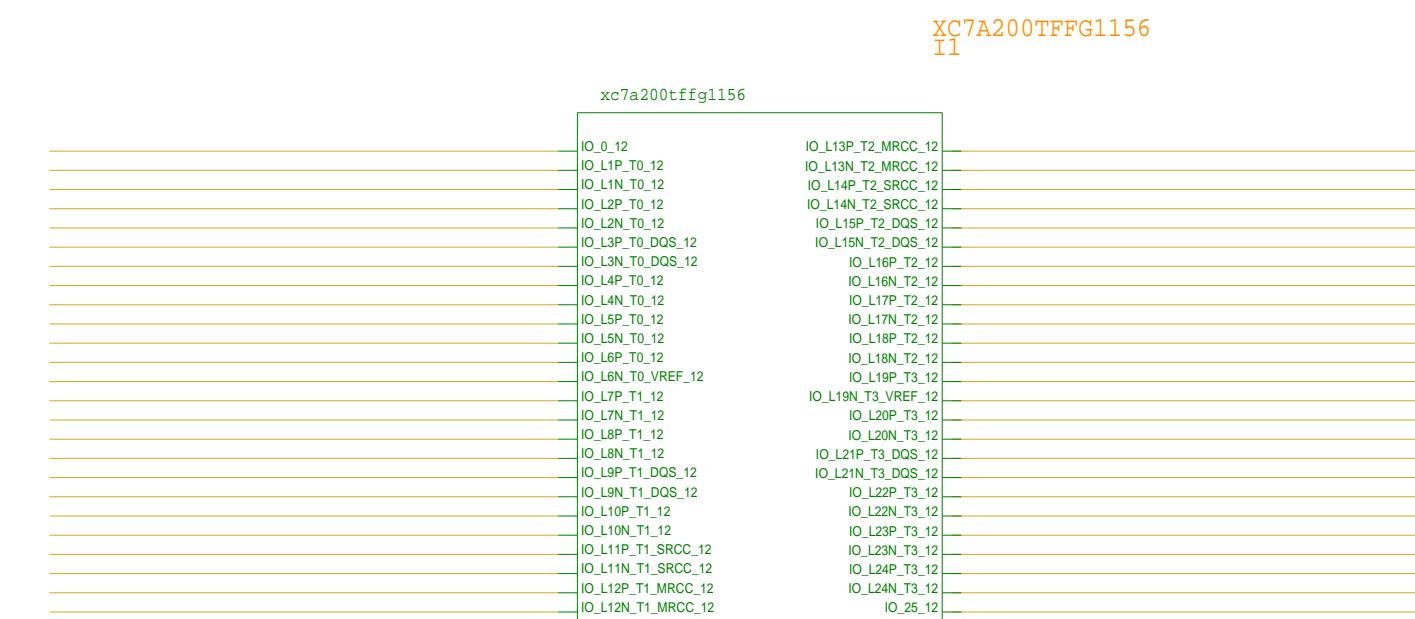
DRAWING TITLE

SIZE	REV.	DRAWING NO.
C		
SCALE		

SHEET OF

ARTIX-7 BANK12

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPR.



CADENCE DESIGN SYSTEMS, INC.
 CADENCE

THIS DOCUMENT CONTAINS INFORMATION PROPRIETARY
TO CADENCE DESIGN SYSTEMS INC (CADENCE). USE
OR DISCLOSURE WITHOUT THE WRITTEN PERMISSION OF AN
OFFICER OF CADENCE IS EXPRESSLY FORBIDDEN.
COPYRIGHT (C) CADENCE 1988

DRAWING TITLE			
SIZE	REV.	DRAWING NO.	
			
SCALE		SHEET	OF