ZYNQ_NvDIMM SCHEMAITC

CETHIK

中电海康集团有限公司

拟制：	审核：	批准：

Title

Size A3	SCHEMATIC CODE TOP	Rev 1.00
	PROJECT NAME ZYNQ_NvDIMM	
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拟制：	审核：	批准：

Title

Size	SCHEMATIC CODE	TITLE	Rev
A3	PROJECT NAME	ZYNQ_NvDIMM	1.00

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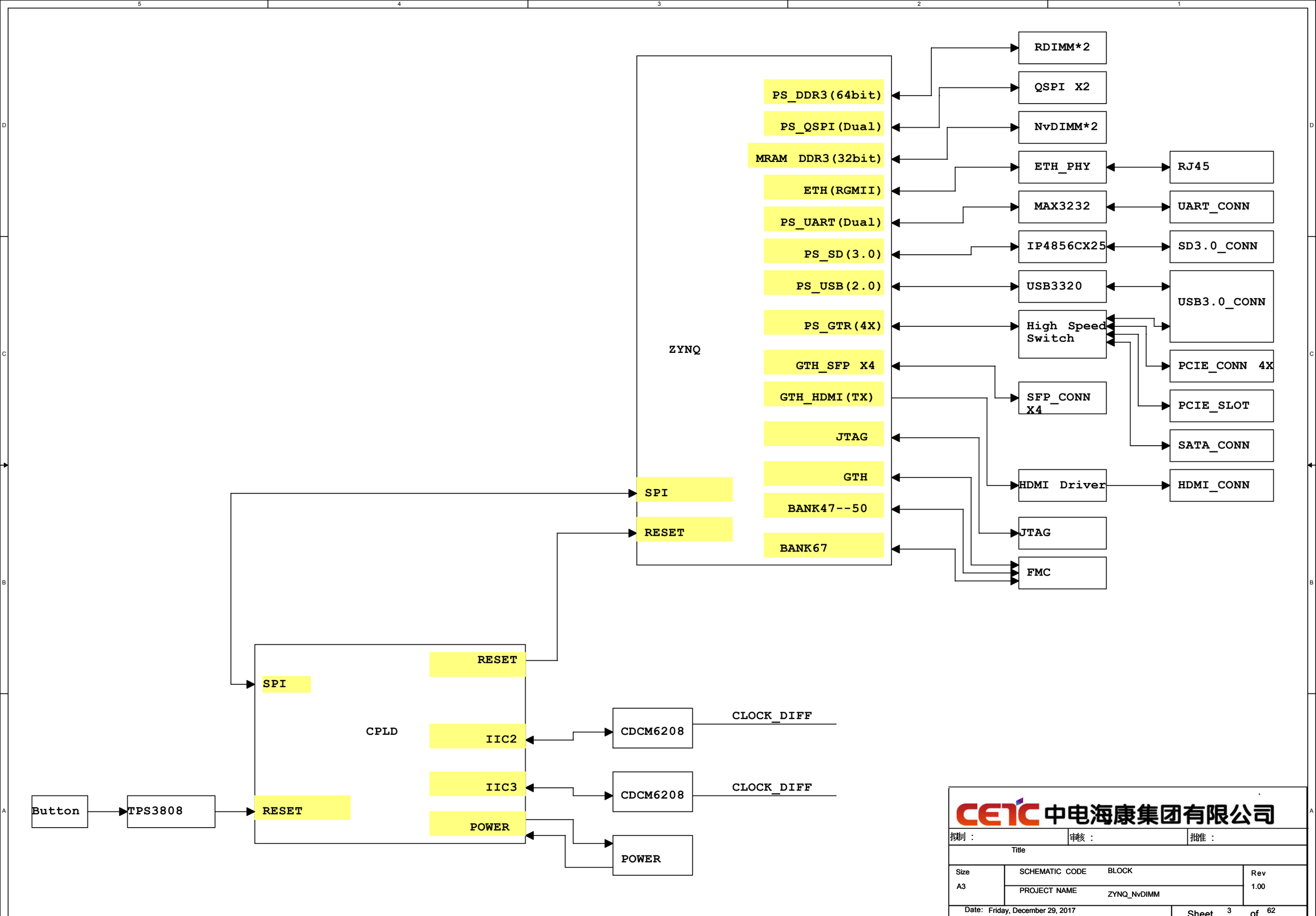

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拟制：	审核：	批准：

Title

Size: A3	SCHEMATIC CODE: BLOCK	Rev: 1.00
	PROJECT NAME: ZYNQ_NvDIMM	
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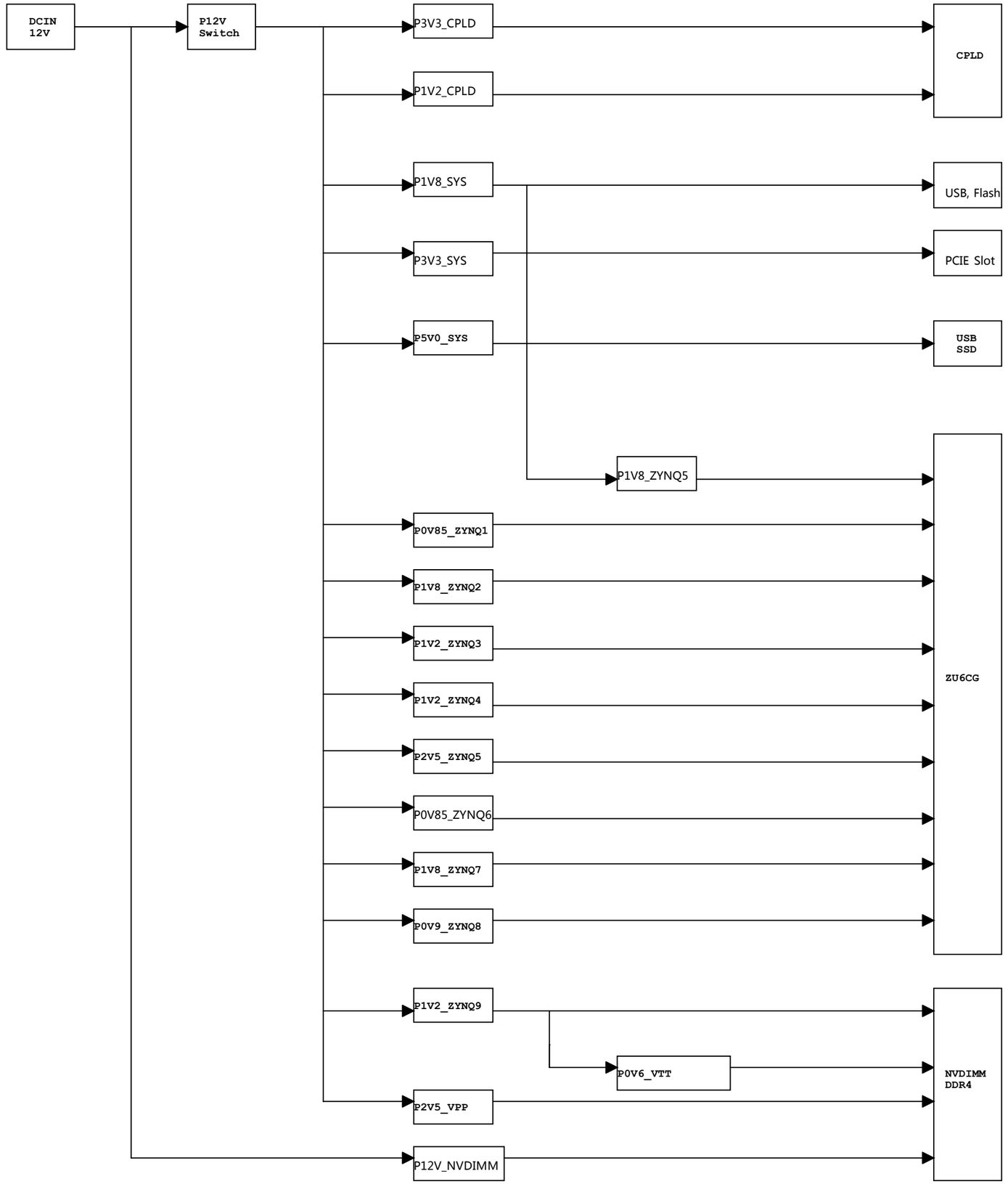

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拟制：	审核：	批准：

Title

Size	SCHEMATIC CODE	POWER_TREE	Rev
A3	PROJECT NAME	ZYNQ_NvDIMM	1.00

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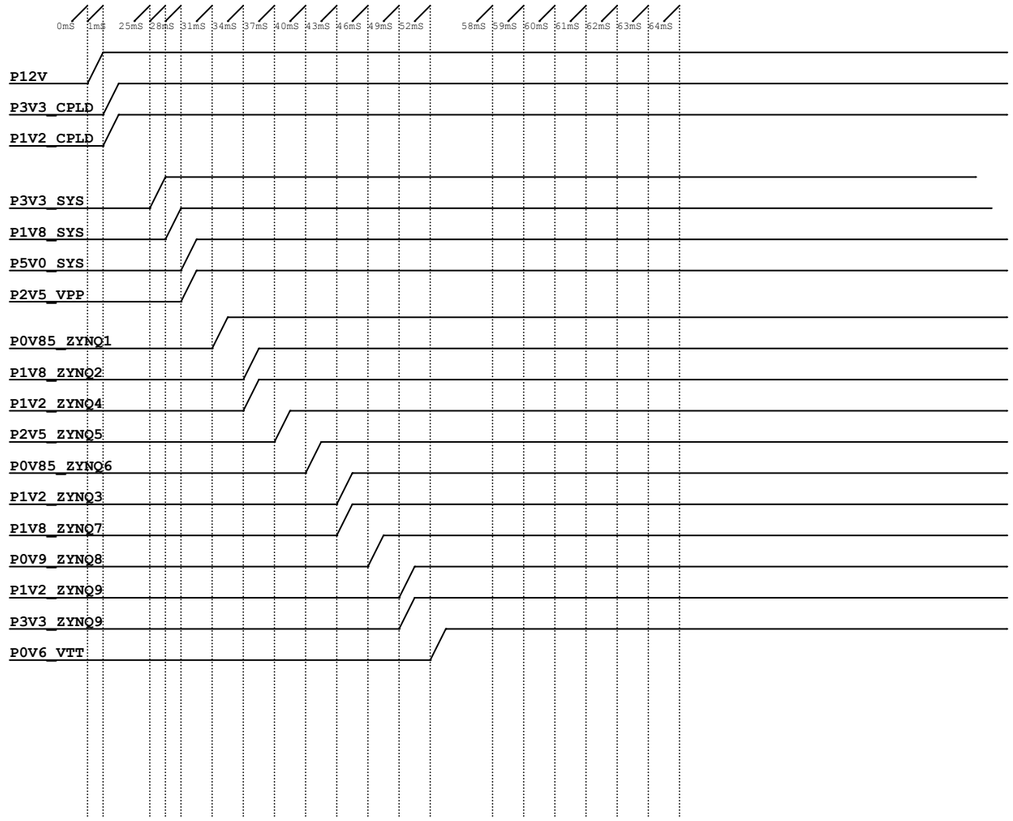

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拟制：	审核：	批准：
Title		
Size: A3	SCHEMATIC CODE: POR_SEQUENCE	Rev: 1.00
	PROJECT NAME: ZYNQ_NvDIMM	
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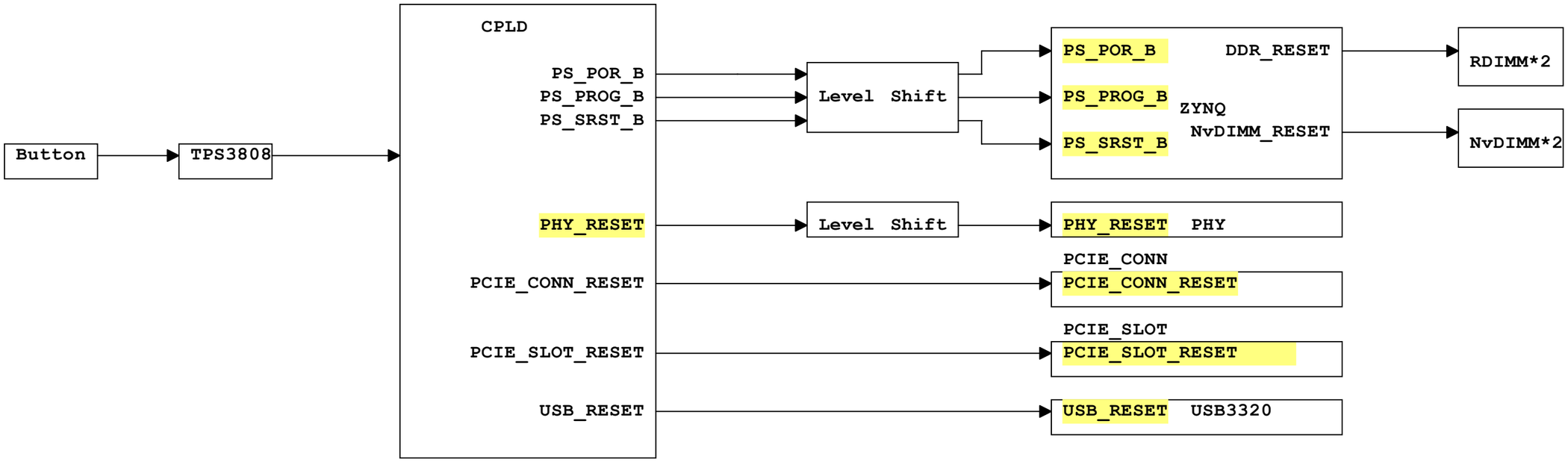

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拟制：	审核：	批准：

Title

Size: A3	SCHEMATIC CODE: RESET	Rev: 1.00
	PROJECT NAME: ZYNQ_NvDIMM	
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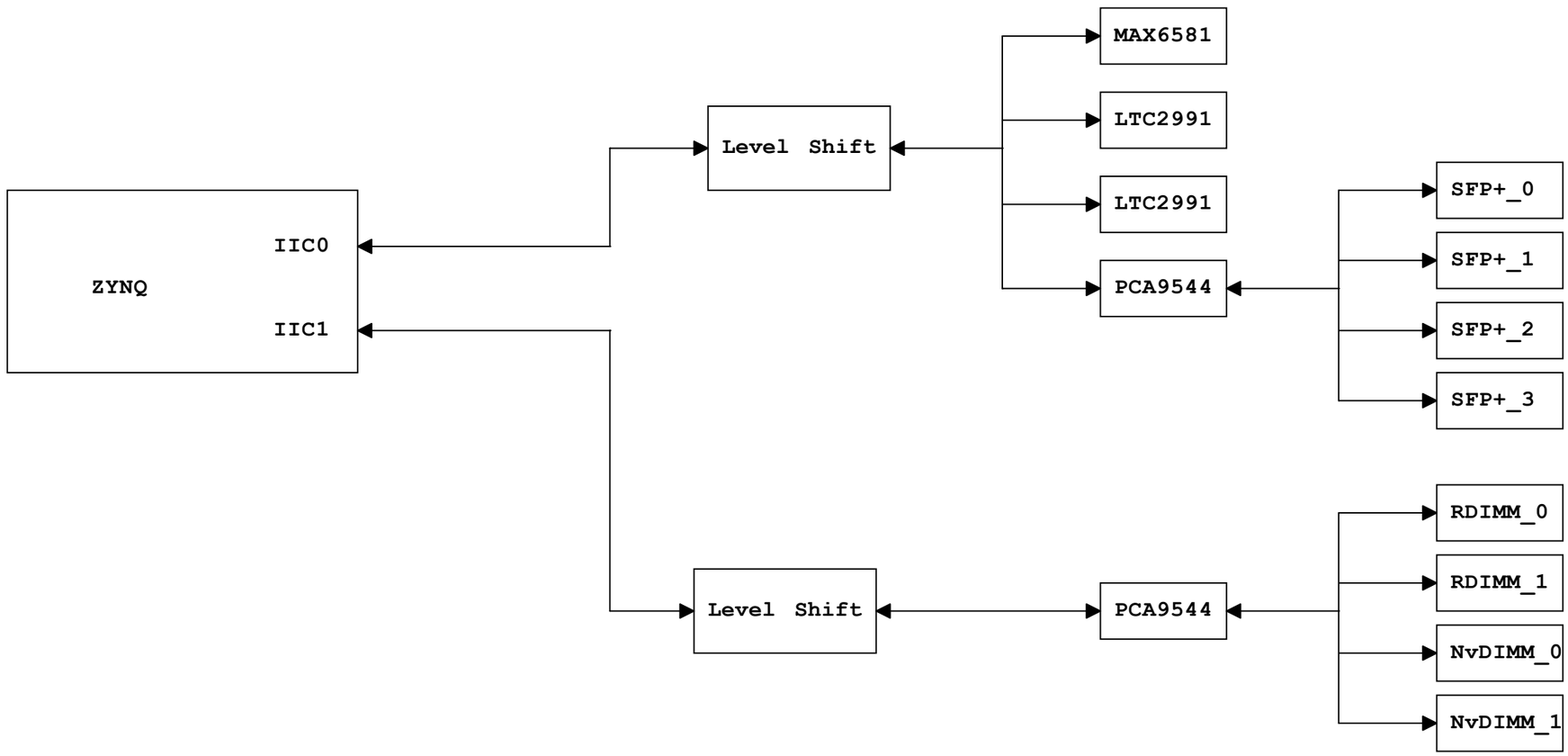

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拟制：	审核：	批准：

Title

Size	SCHEMATIC CODE	IIC_TOPOLOGY	Rev
A3	PROJECT NAME	ZYNQ_NvDIMM	1.00

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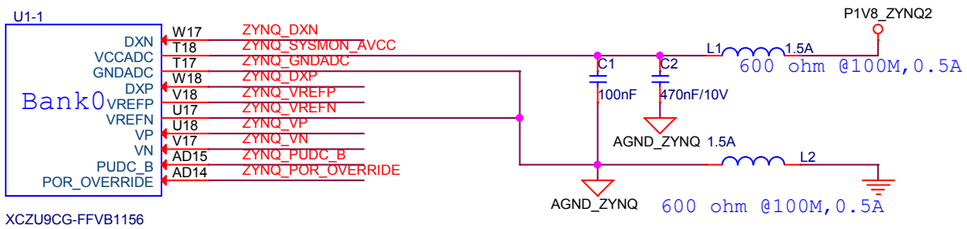

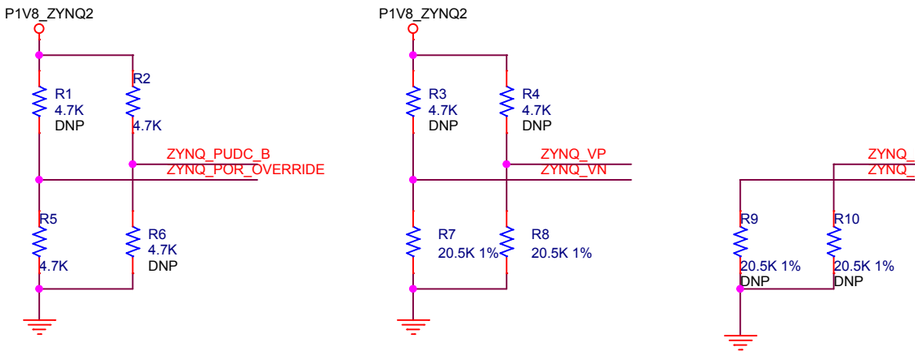

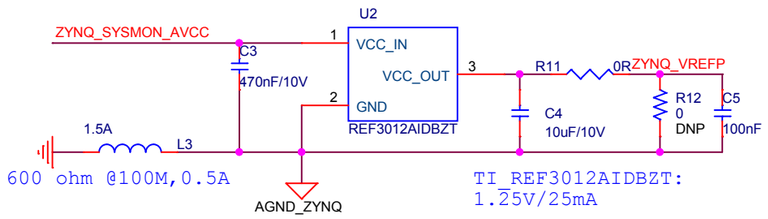

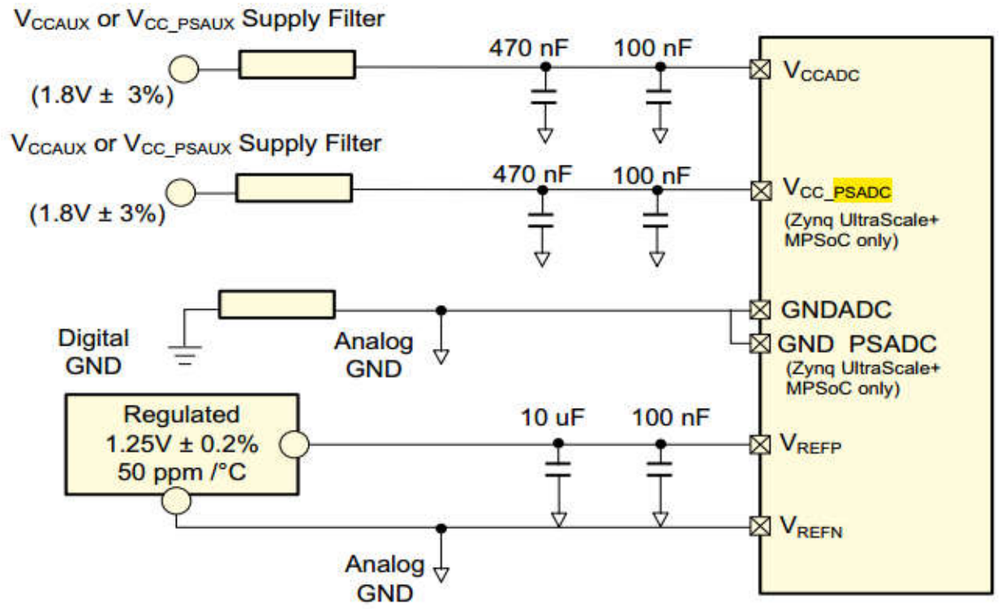

see ug580.p13

PUDC_B:1 = Weak preconfiguration I/O pull-up resistors disabled.PUDC_B is powered by VCCAUX.

POR_OVERRIDE:0 = Standard PL power-on delay time.

VP_VN:This pin should be connected to GNDADC if not used.

DXP_DXN: When not used, tie to GND.

VREFP:Voltage reference input(1.25V).

VREFN:Voltage reference GND.

VCCADC:PL System Monitor supply relative to GNDADC(1.8V).

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拟制：	审核：	批准：

Title

Size	SCHEMATIC CODE	ZYNQ_CONFIG	Rev
A3	PROJECT NAME	ZYNQ_NvDIMM	1.00

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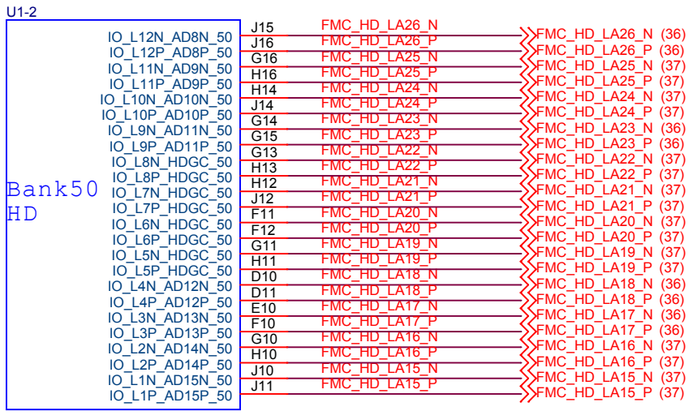

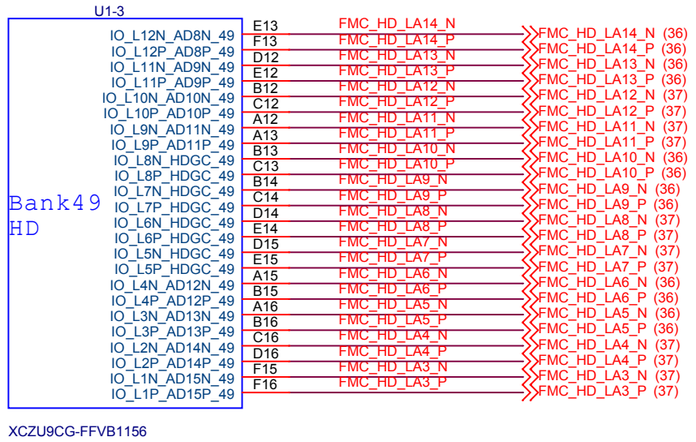

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拟制：	审核：	批准：

Title

Size: A3	SCHEMATIC CODE: ZYNQ_HD_BANK49/50	Rev: 1.00
	PROJECT NAME: ZYNQ_NvDIMM	
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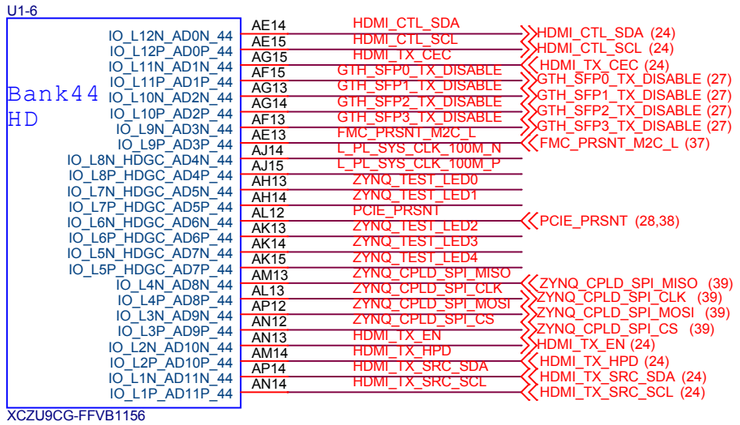

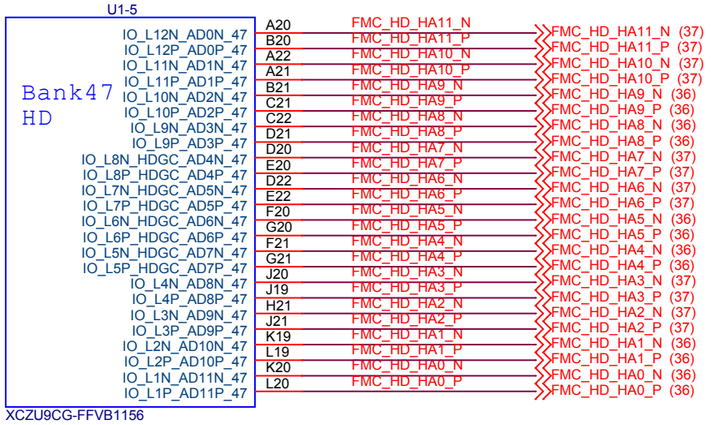

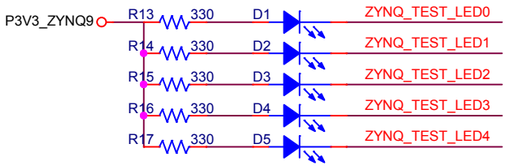

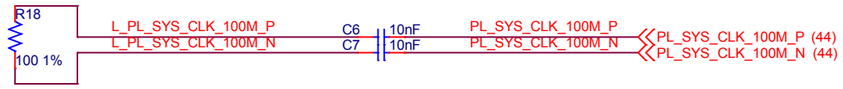

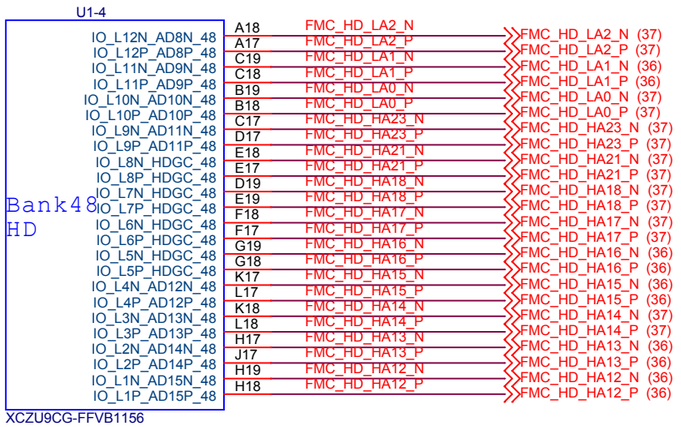

NOTE:
HDGC pins have direct access to the global clock buffers.

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拟制：	审核：	批准：

Title

Size: A3	SCHEMATIC CODE: ZYNQ_HD_BANK44/47/48	Rev: 1.00
	PROJECT NAME: ZYNQ_NvDIMM	
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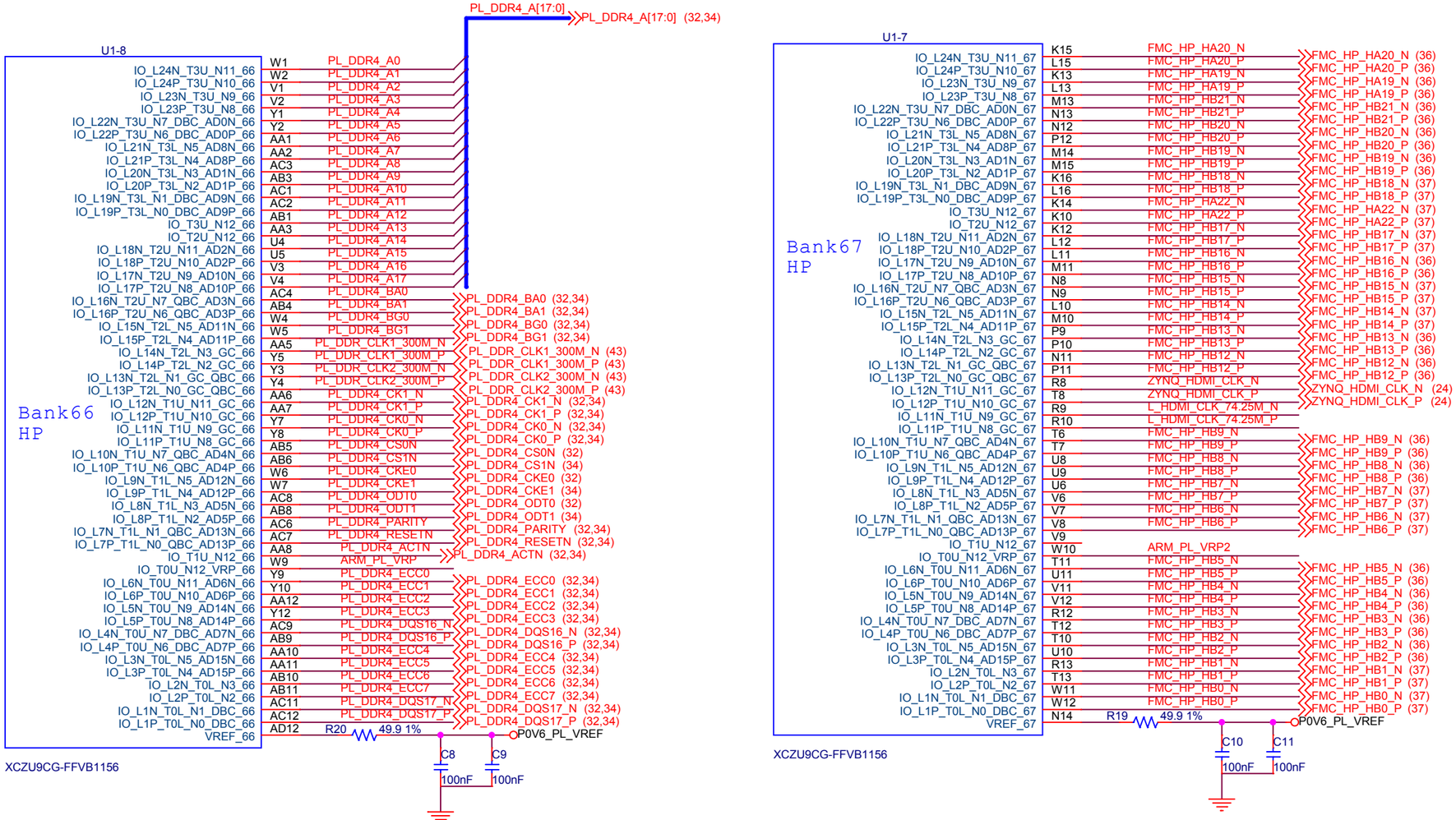

NOTE:
VRP:This pin is for the DCI voltage reference resistor of P
transistor.Digitally controlled impedance (DCI) is only available in HP I/O banks.
DCI uses only one reference resistor per bank, 240Ω to GND on the VRP pin

NOTE:
GC pins have direct access to the global clock buffers and the MMCMs and PLLs
that are in the clock management tile (CMT) adjacent to the same I/O bank.

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拟制：	审核：	批准：

Title

Size	SCHEMATIC CODE	ZYNQ_HP_BANK66/67	Rev
A3	PROJECT NAME	ZYNQ_NvDIMM	1.00

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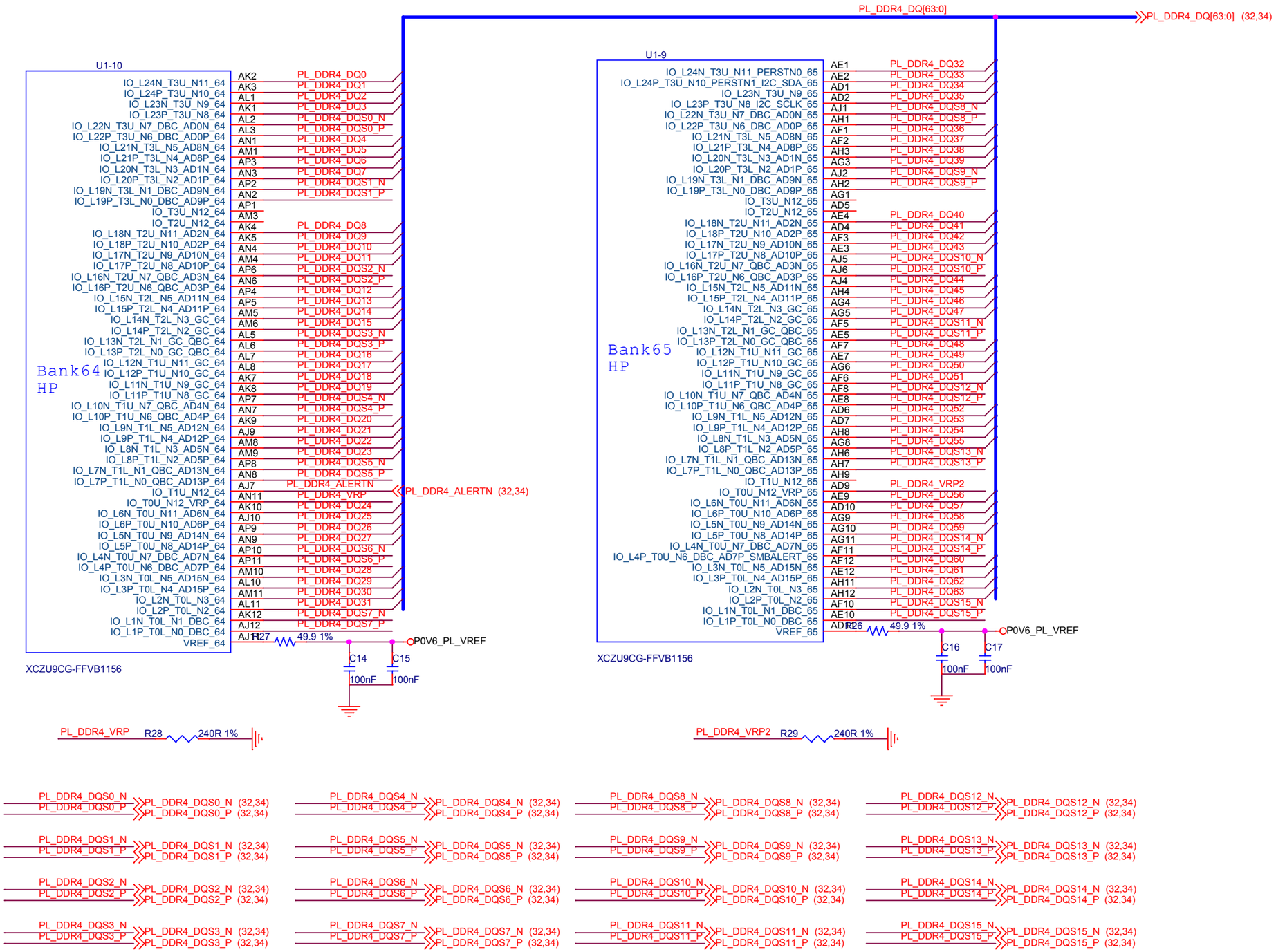

NOTE:
VRP:This pin is for the DCI voltage reference resistor of P
transistor.Digitally controlled impedance (DCI) is only available in HP I/O banks.
DCI uses only one reference resistor per bank, 240Ω to GND on the VRP pin

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拟制：	审核：	批准：

Title

Size	SCHEMATIC CODE	ZYNQ_HP_BANK64/65	Rev
A3	PROJECT NAME	ZYNQ_NvDIMM	1.00
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NOTE:
MGTREFCLK*_P/N:The dedicated differential reference clock input pair MGTREFCLKP/MGTREFCLKN is internally terminated with 100Ω differential impedance.
The common mode voltage for UltraScale+ FPGAs is MGTAVCC, or nominal of 0.9V.
If the reference clock input is not used, leave the reference clock input pins unconnected (both MGTREFCLKP and MGTREFCLKN).(see ug576.p324)

NOTE:
MGTHRXP[3:0]/MGTHRXN[3:0]
If a receiver will never be used under any conditions, connect the associated pin pair to GND.
If a transmitter is not used, leave the associated pin pair unconnected.

NOTE:
Connect the MGTAVTTRCAL pin to the MGTAVTT supply and to a pin on the 100Ω precision external resistor.the trace from the MGTAVTTRCAL pin to the resistor should have the same length and geometry as the trace that connects the other pin of the resistor to the MGTRREF pin.

U1-11

Bank128 GTH

M29	MGTHTXP3_128	MGTHRXP3_128	M33
M30	MGTHTXN3_128	MGTHRXN3_128	M34
P29	MGTHTXP2_128	MGTHRXP2_128	N31
P30	MGTHTXN2_128	MGTHRXN2_128	N32
R31	MGTHTXP1_128	MGTHRXP1_128	P33
R32	MGTHTXN1_128	MGTHRXN1_128	P34
T29	MGTHTXP0_128	MGTHRXP0_128	T33
T30	MGTHTXN0_128	MGTHRXN0_128	T34
N27	MGTREFCLK1P_128		
N28	MGTREFCLK1N_128		
R27	MGTREFCLK0P_128		
R28	MGTREFCLK0N_128		

R30–R37 1K DNP

R38 1K DNP
R39 1K DNP

(24) ZYNQ_HDMI_TX2_P
(24) ZYNQ_HDMI_TX2_N
(24) ZYNQ_HDMI_TX1_P
(24) ZYNQ_HDMI_TX1_N
(24) ZYNQ_HDMI_TX0_P
(24) ZYNQ_HDMI_TX0_N
ZYNQ_HDMI_TX2_P
ZYNQ_HDMI_TX2_N
ZYNQ_HDMI_TX1_P
ZYNQ_HDMI_TX1_N
ZYNQ_HDMI_TX0_P
ZYNQ_HDMI_TX0_N

(43) GTH_HDMI_74.25M_P
(43) GTH_HDMI_74.25M_N
GTH_HDMI_74.25M_P C18 10nF R_GTH_HDMI_74.25M_P
GTH_HDMI_74.25M_N C19 10nF R_GTH_HDMI_74.25M_N

Bank129 GTH

G31	MGTHTXP3_129	MGTHRXP3_129	F33
G32	MGTHTXN3_129	MGTHRXN3_129	F34
H29	MGTHTXP2_129	MGTHRXP2_129	H33
H30	MGTHTXN2_129	MGTHRXN2_129	H34
J31	MGTHTXP1_129	MGTHRXP1_129	K33
J32	MGTHTXN1_129	MGTHRXN1_129	K34
K29	MGTHTXP0_129	MGTHRXP0_129	L31
K30	MGTHTXN0_129	MGTHRXN0_129	L32
J27	MGTHREFCLK1P_129	MGTRREF_L	A29
J28	MGTHREFCLK1N_129	MGTAVTTRCAL_L	A30
E27	MGTHREFCLK0P_129		
E28	MGTHREFCLK0N_129		

(36) GTH1_FMC_C2M_DP03_P
(36) GTH1_FMC_C2M_DP03_N
(36) GTH1_FMC_C2M_DP02_P
(36) GTH1_FMC_C2M_DP02_N
(36) GTH1_FMC_C2M_DP01_P
(36) GTH1_FMC_C2M_DP01_N
(36) GTH1_FMC_C2M_DP00_P
(36) GTH1_FMC_C2M_DP00_N
GTH1_FMC_C2M_DP03_P
GTH1_FMC_C2M_DP03_N
GTH1_FMC_C2M_DP02_P
GTH1_FMC_C2M_DP02_N
GTH1_FMC_C2M_DP01_P
GTH1_FMC_C2M_DP01_N
GTH1_FMC_C2M_DP00_P
GTH1_FMC_C2M_DP00_N

GTH1_FMC_M2C_DP03_P
GTH1_FMC_M2C_DP03_N
GTH1_FMC_M2C_DP02_P
GTH1_FMC_M2C_DP02_N
GTH1_FMC_M2C_DP01_P
GTH1_FMC_M2C_DP01_N
GTH1_FMC_M2C_DP00_P
GTH1_FMC_M2C_DP00_N

GTH1_FMC_M2C_DP03_P (36)
GTH1_FMC_M2C_DP03_N (36)
GTH1_FMC_M2C_DP02_P (36)
GTH1_FMC_M2C_DP02_N (36)
GTH1_FMC_M2C_DP01_P (36)
GTH1_FMC_M2C_DP01_N (36)
GTH1_FMC_M2C_DP00_P (36)
GTH1_FMC_M2C_DP00_N (36)

(36) FMC_GBTCLK1_M2C_P
(36) FMC_GBTCLK1_M2C_N
FMC_GBTCLK1_M2C_P C20 10nF R_FMC_GBTCLK1_M2C_P
FMC_GBTCLK1_M2C_N C21 10nF R_FMC_GBTCLK1_M2C_N

(43) GTH_FMC1_CLK_125M_P
(43) GTH_FMC1_CLK_125M_N
GTH_FMC1_CLK_125M_P C22 10nF R_GTH_FMC1_CLK_125M_P
GTH_FMC1_CLK_125M_N C23 10nF R_GTH_FMC1_CLK_125M_N

R40 100 1% P1V2_ZYNQ3

Note:R386 两侧 需做 等长 处 理

XCZU9CG-FFVB1156

U1-12

Bank130 GTH

A31	MGTHTXP3_130	MGTHRXP3_130	B33
A32	MGTHTXN3_130	MGTHRXN3_130	B34
B29	MGTHTXP2_130	MGTHRXP2_130	C31
B30	MGTHTXN2_130	MGTHRXN2_130	C32
D29	MGTHTXP1_130	MGTHRXP1_130	D33
D30	MGTHTXN1_130	MGTHRXN1_130	D34
F29	MGTHTXP0_130	MGTHRXP0_130	E31
F30	MGTHTXN0_130	MGTHRXN0_130	E32
G27	MGTREFCLK0P_130		
G28	MGTREFCLK0N_130		
E27	MGTREFCLK1P_130		
E28	MGTREFCLK1N_130		

R41–R46 1K DNP

R47 1K DNP
R48 1K DNP

(36) GTH1_FMC_C2M_DP08_P
(36) GTH1_FMC_C2M_DP08_N
GTH1_FMC_C2M_DP08_P
GTH1_FMC_C2M_DP08_N

GTH1_FMC_M2C_DP08_P
GTH1_FMC_M2C_DP08_N

GTH1_FMC_M2C_DP08_P (36)
GTH1_FMC_M2C_DP08_N (36)

(44) GTH_FMC1_CLK_156.25M_P
(44) GTH_FMC1_CLK_156.25M_N
GTH_FMC1_CLK_156.25M_P C24 10nF R_GTH_FMC1_CLK_156.25M_P
GTH_FMC1_CLK_156.25M_N C25 10nF R_GTH_FMC1_CLK_156.25M_N

Bank228 GTH

M6	MGTHTXP3_228	MGTHRXP3_228	L4
M5	MGTHTXN3_228	MGTHRXN3_228	L3
N4	MGTHTXP2_228	MGTHRXP2_228	M2
N3	MGTHTXN2_228	MGTHRXN2_228	M1
P6	MGTHTXP1_228	MGTHRXP1_228	P2
P5	MGTHTXN1_228	MGTHRXN1_228	P1
R4	MGTHTXP0_228	MGTHRXP0_228	T2
R3	MGTHTXN0_228	MGTHRXN0_228	T1
J8	MGTHREFCLK1P_228	MGTRREF_R	A6
J7	MGTHREFCLK1N_228	MGTAVTTRCAL_R	A5
E8	MGTHREFCLK0P_228		
E7	MGTHREFCLK0N_228		

(27) GTH_SFP3_TX_P
(27) GTH_SFP3_TX_N
(27) GTH_SFP2_TX_P
(27) GTH_SFP2_TX_N
(27) GTH_SFP1_TX_P
(27) GTH_SFP1_TX_N
(27) GTH_SFP0_TX_P
(27) GTH_SFP0_TX_N
GTH_SFP3_TX_P
GTH_SFP3_TX_N
GTH_SFP2_TX_P
GTH_SFP2_TX_N
GTH_SFP1_TX_P
GTH_SFP1_TX_N
GTH_SFP0_TX_P
GTH_SFP0_TX_N

GTH_SFP3_RX_P
GTH_SFP3_RX_N
GTH_SFP2_RX_P
GTH_SFP2_RX_N
GTH_SFP1_RX_P
GTH_SFP1_RX_N
GTH_SFP0_RX_P
GTH_SFP0_RX_N

GTH_SFP3_RX_P (27)
GTH_SFP3_RX_N (27)
GTH_SFP2_RX_P (27)
GTH_SFP2_RX_N (27)
GTH_SFP1_RX_P (27)
GTH_SFP1_RX_N (27)
GTH_SFP0_RX_P (27)
GTH_SFP0_RX_N (27)

R49 1K DNP
R51 1K DNP

R50 100 1% P1V2_ZYNQ3

Note:R391 两侧 需做 等长 处 理

(44) GTH_SFP_CLK_156.25M_P
(44) GTH_SFP_CLK_156.25M_N
GTH_SFP_CLK_156.25M_P C26 10nF R_GTH_SFP_CLK_156.25M_P
GTH_SFP_CLK_156.25M_N C27 10nF R_GTH_SFP_CLK_156.25M_N

XCZU9CG-FFVB1156

U1-13

Bank229 GTH

F6	MGTHTXP3_229	MGTHRXP3_229	F2
F5	MGTHTXN3_229	MGTHRXN3_229	F1
G4	MGTHTXP2_229	MGTHRXP2_229	H2
G3	MGTHTXN2_229	MGTHRXN2_229	H1
H6	MGTHTXP1_229	MGTHRXP1_229	J4
H5	MGTHTXN1_229	MGTHRXN1_229	J3
K6	MGTHTXP0_229	MGTHRXP0_229	K2
K5	MGTHTXN0_229	MGTHRXN0_229	K1
E8	MGTHREFCLK1P_229		
E7	MGTHREFCLK1N_229		
G8	MGTHREFCLK0P_229		
G7	MGTHREFCLK0N_229		

(36) GTH2_FMC_C2M_DP07_P
(36) GTH2_FMC_C2M_DP07_N
(36) GTH2_FMC_C2M_DP06_P
(36) GTH2_FMC_C2M_DP06_N
(36) GTH2_FMC_C2M_DP05_P
(36) GTH2_FMC_C2M_DP05_N
(36) GTH2_FMC_C2M_DP04_P
(36) GTH2_FMC_C2M_DP04_N
GTH2_FMC_C2M_DP07_P
GTH2_FMC_C2M_DP07_N
GTH2_FMC_C2M_DP06_P
GTH2_FMC_C2M_DP06_N
GTH2_FMC_C2M_DP05_P
GTH2_FMC_C2M_DP05_N
GTH2_FMC_C2M_DP04_P
GTH2_FMC_C2M_DP04_N

GTH2_FMC_M2C_DP07_P
GTH2_FMC_M2C_DP07_N
GTH2_FMC_M2C_DP06_P
GTH2_FMC_M2C_DP06_N
GTH2_FMC_M2C_DP05_P
GTH2_FMC_M2C_DP05_N
GTH2_FMC_M2C_DP04_P
GTH2_FMC_M2C_DP04_N

GTH2_FMC_M2C_DP07_P (36)
GTH2_FMC_M2C_DP07_N (36)
GTH2_FMC_M2C_DP06_P (36)
GTH2_FMC_M2C_DP06_N (36)
GTH2_FMC_M2C_DP05_P (36)
GTH2_FMC_M2C_DP05_N (36)
GTH2_FMC_M2C_DP04_P (36)
GTH2_FMC_M2C_DP04_N (36)

(36) FMC_GBTCLK0_M2C_P
(36) FMC_GBTCLK0_M2C_N
FMC_GBTCLK0_M2C_P C28 10nF R_FMC_GBTCLK0_M2C_P
FMC_GBTCLK0_M2C_N C29 10nF R_FMC_GBTCLK0_M2C_N

(44) GTH_FMC2_CLK_125M_P
(44) GTH_FMC2_CLK_125M_N
GTH_FMC2_CLK_125M_P C30 10nF R_GTH_FMC2_CLK_125M_P
GTH_FMC2_CLK_125M_N C31 10nF R_GTH_FMC2_CLK_125M_N

Bank230 GTH

A8	MGTHTXP3_230	MGTHRXP3_230	A4
A7	MGTHTXN3_230	MGTHRXN3_230	A3
B6	MGTHTXP2_230	MGTHRXP2_230	B2
B5	MGTHTXN2_230	MGTHRXN2_230	B1
D6	MGTHTXP1_230	MGTHRXP1_230	C4
D5	MGTHTXN1_230	MGTHRXN1_230	C3
E4	MGTHTXP0_230	MGTHRXP0_230	D2
E3	MGTHTXN0_230	MGTHRXN0_230	D1
B10	MGTHREFCLK1P_230		
B9	MGTHREFCLK1N_230		
C8	MGTHREFCLK0P_230		
C7	MGTHREFCLK0N_230		

R52–R57 1K DNP

(36) GTH2_FMC_C2M_DP09_P
(36) GTH2_FMC_C2M_DP09_N
GTH2_FMC_C2M_DP09_P
GTH2_FMC_C2M_DP09_N

GTH2_FMC_M2C_DP09_P
GTH2_FMC_M2C_DP09_N

GTH2_FMC_M2C_DP09_P (36)
GTH2_FMC_M2C_DP09_N (36)

R58 1K DNP
R59 1K DNP

(44) GTH_FMC_CLK_125M_P
(44) GTH_FMC_CLK_125M_N
GTH_FMC_CLK_125M_P C32 10nF R_GTH_FMC_CLK_125M_P
GTH_FMC_CLK_125M_N C33 10nF R_GTH_FMC_CLK_125M_N

XCZU9CG-FFVB1156

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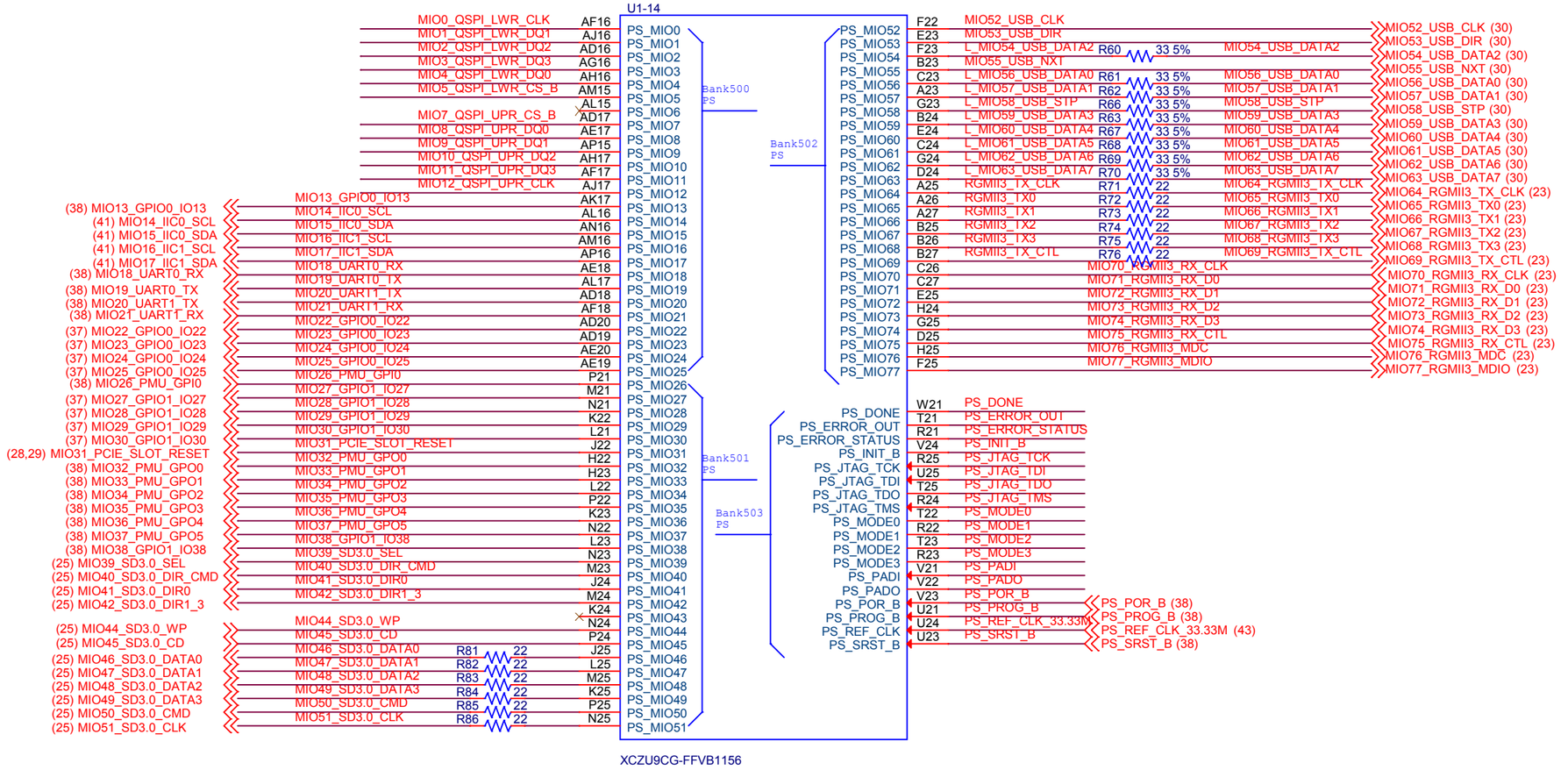
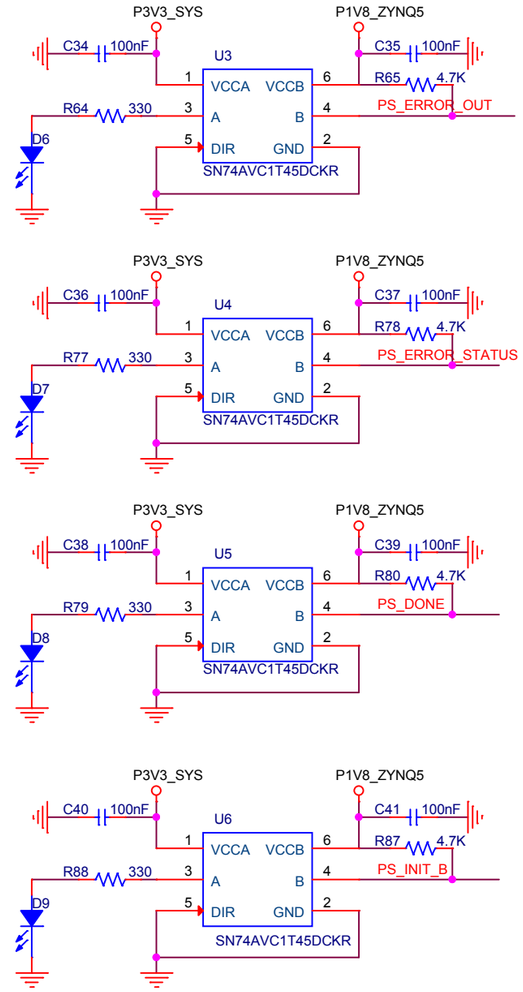
拟制：	审核：	批准：

Title

Size A3	SCHEMATIC CODE ZYNQ_GTH_BANK	Rev 1.00
	PROJECT NAME ZYNQ_NvDIMM	
Date: Friday, December 29, 2017	Sheet 13 of 62	



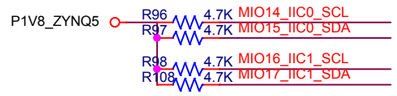
ZYNQ STATUS LED



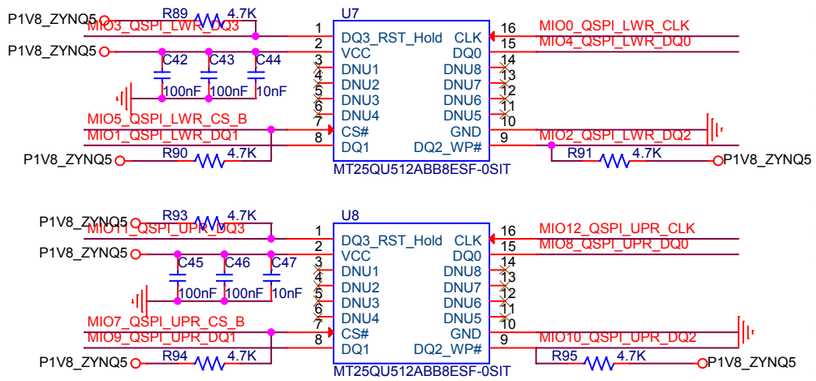
NOTE:SN74AVC1T45
DIR:DIR Input Circuit Referenced to VCCA.
L:B Data --> A Bus;
H:A Data --> B Bus.

PS_INIT_B:
Initialization completion indicator after POR.Requires an external pull-up resistor.

PS DONE:
Requires an external pull-up resistor.



QSPI



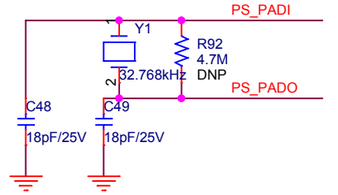
DQ3_RST_HOLD_B:
RESET# or HOLD# signals can share Pin 1 with DQ3
DQ3 must be driven high by the host, or an external pull-up resistor must be placed on the PCB, in order to avoid allowing the HOLD# or RESET# input to float.

Pin 3 = RESET# or DNU, depending on the part number. This signal has an internal pullup resistor and may be left unconnected if not used.

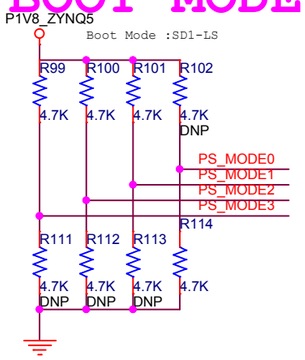
WP#:This signal does not have internal pull-ups, it cannot be left floating and must be driven

CS#: When S# is driven HIGH, the device will enter standby mode, unless an internal PROGRAM, ERASE, or WRITE STATUS REGISTER cycle is in progress

RTC CLK

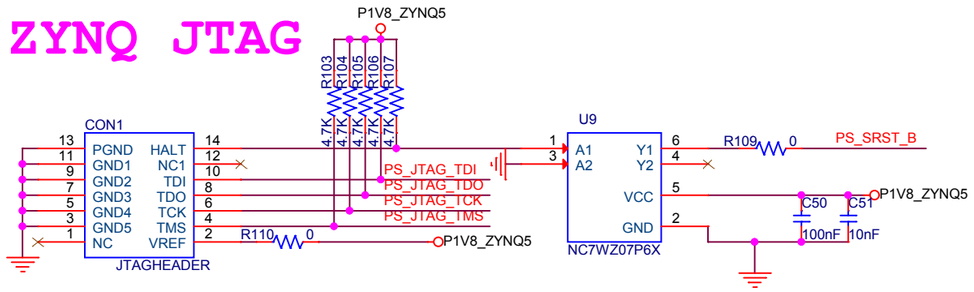


BOOT MODE



Boot Mode	Mode Pin [3:0]	MIO Location
JTAG	0x0	JTAG
QSPI24	0x1	MIO[12:0]
QSPI32	0x2	MIO[12:0]
SD0	0x3	MIO[25:13]
NAND	0x4	MIO[25:9]
SD1	0x5	MIO[51:38]
eMMC_18	0x6	MIO[22:13]
USB0	0x7	MIO[63:52]
PJTAG0	0x8	MIO[29:26]
PJTAG1	0x9	MIO[15:12]
SD1_LS	0xE	MIO[51:39]

ZYNQ JTAG



NC7WZ07P6X Function Table

input	output
A	Y
L	L
H	High Impedance Output State,Open Drain

NOTE:
VCC:1.65V to 5.5V

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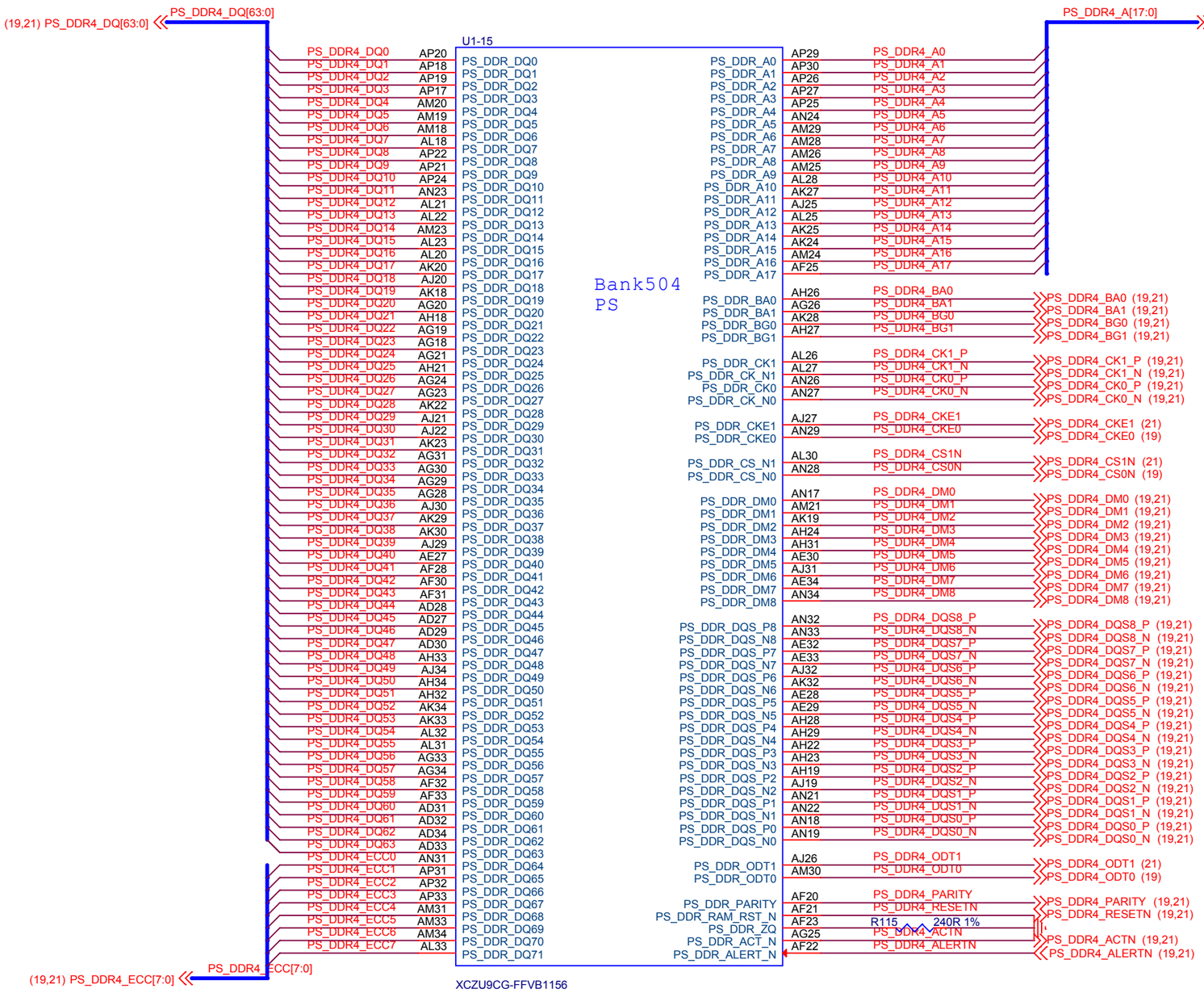
Title		
Size A3	SCHEMATIC CODE ZYNQ_PS_MIO_BANK	Rev 1.00
	PROJECT NAME ZYNQ_NvDIMM	
Date: Friday, December 29, 2017	Sheet 14 of 62	



NOTE:
1、All unused DDR pins can be left unconnected.
2、Connect the PS_DDR_ZQ pin to GND using a 240Ω resistor.
There should be separate 240Ω resistors at the FPGA and at the DRAM.

NOTE:
DDR3/3L Pin Swapping Restrictions
1、Address/command/control bits cannot be swapped.
2、DQ byte lane swapping is allowed.
3、DQ bits swapping within a byte lane is allowed.(see ug1075.p52)

NOTE:
PS_DDR_PARITY:Can be left unconnected for components and UDIMMs.
(see ug1075)

PS_DDR_ALERT_N:Can be left unconnected.

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拟制：	审核：	批准：

Title

Size	SCHEMATIC CODE	ZYNQ_PS_DDR	Rev
A3	PROJECT NAME	ZYNQ_NvDIMM	1.00

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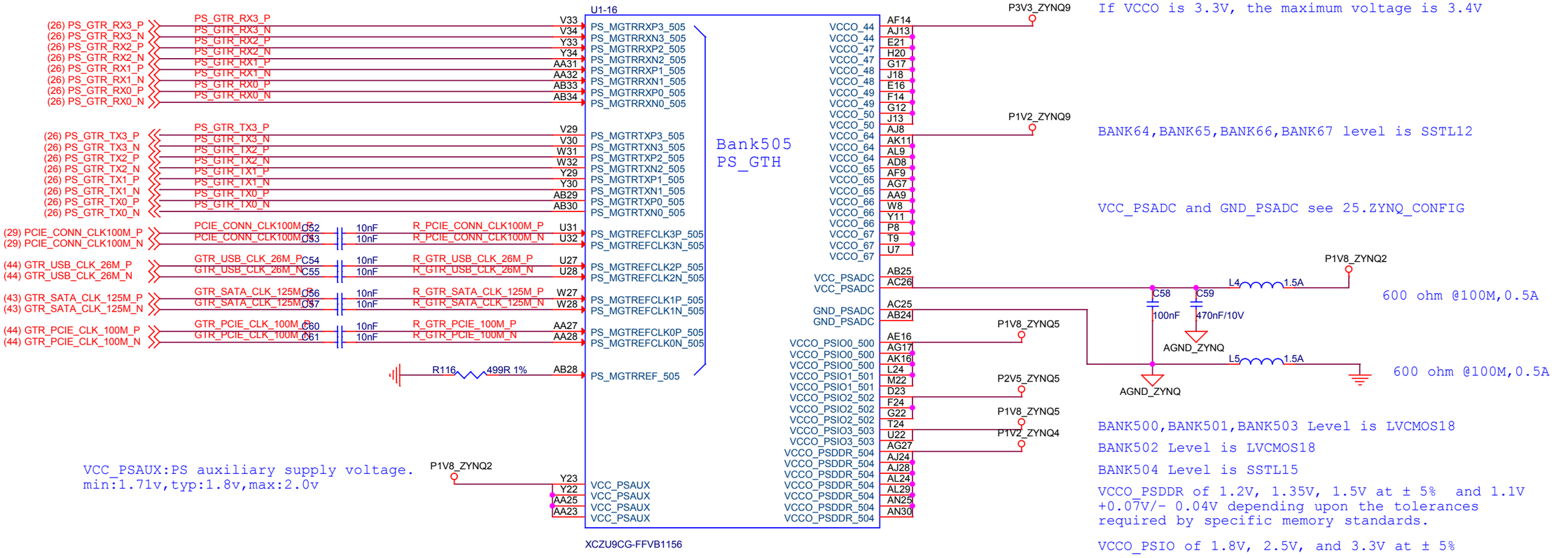

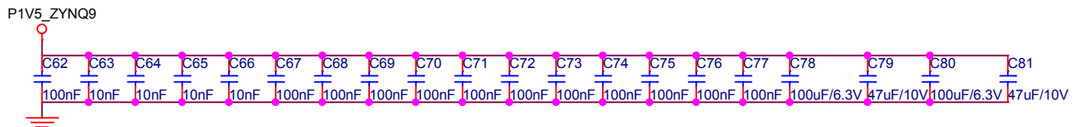

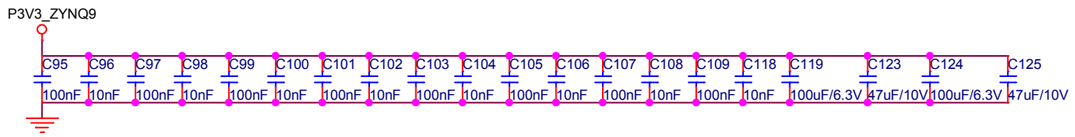

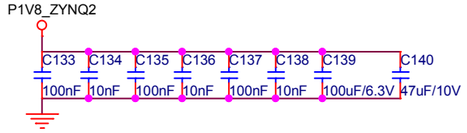

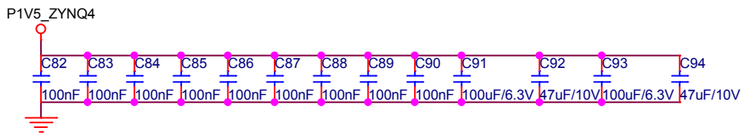

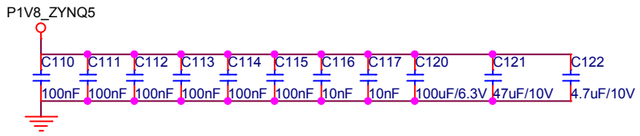

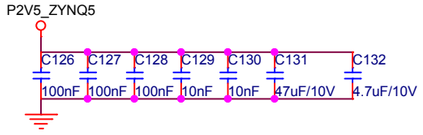

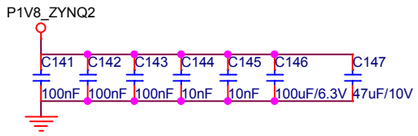

NOTE:
PS_MGTRREF:Connect to a 500Ω 0.5% resistor to this pin with the other terminal of the resistor connected to ground.(see ug583.p176)

PS_MGTRTX[3:0]_P/_N:
If a transmitter is not used, leave the associated pin pair unconnected.(see ug583.p176)

PS_MGTRRX[3:0]_P/_N:
If a transmitter is not used, leave the associated pin pair unconnected.
The recommended value for AC coupling capacitors is 100 nF.(see ug583.p176)

PS_MGTREFCLK[3:0]_P/_N:
Use AC coupling capacitors for connection to oscillator;
For AC coupling capacitors,The recommended value for LVDS is 10 nF.
If the reference clock input is not used, leave the associated pin pair unconnected.(see ug583.p176)

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Title

Size	SCHEMATIC CODE	ZYNQ_PS_GTR_PS_PWR	Rev
A3	PROJECT NAME	ZYNQ_NvDIMM	1.00

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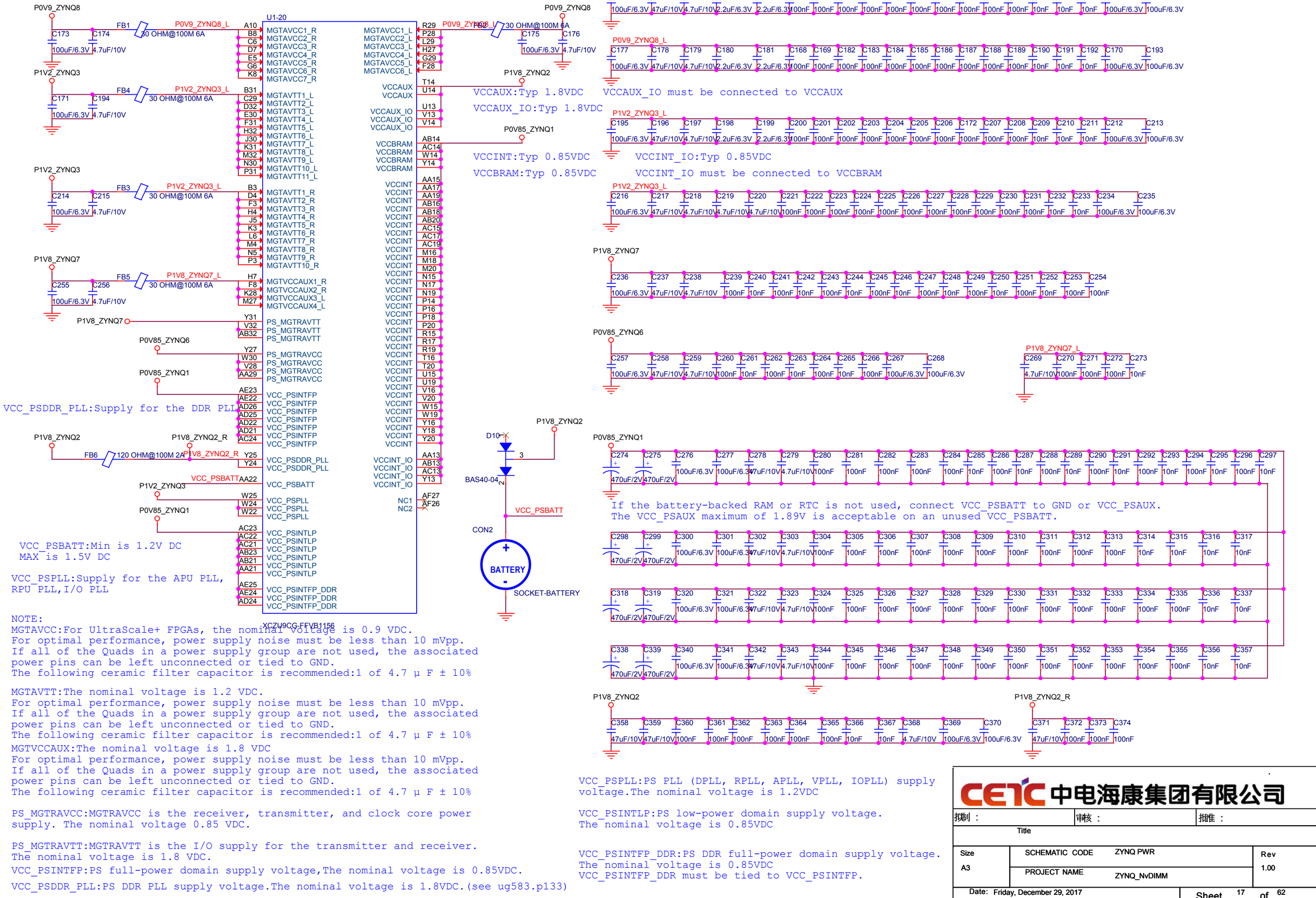

NOTE:
MGTAVCC:For UltraScale+ FPGAs, the nominal voltage is 0.9 VDC.
For optimal performance, power supply noise must be less than 10 mVpp.
If all of the Quads in a power supply group are not used, the associated power pins can be left unconnected or tied to GND.
The following ceramic filter capacitor is recommended:1 of 4.7 μ F ± 10%

MGTAVTT:The nominal voltage is 1.2 VDC.
For optimal performance, power supply noise must be less than 10 mVpp.
If all of the Quads in a power supply group are not used, the associated power pins can be left unconnected or tied to GND.
The following ceramic filter capacitor is recommended:1 of 4.7 μ F ± 10%

MGTVCCAUX:The nominal voltage is 1.8 VDC
For optimal performance, power supply noise must be less than 10 mVpp.
If all of the Quads in a power supply group are not used, the associated power pins can be left unconnected or tied to GND.
The following ceramic filter capacitor is recommended:1 of 4.7 μ F ± 10%

PS_MGTRAVCC:MGTRAVCC is the receiver, transmitter, and clock core power supply. The nominal voltage 0.85 VDC.

PS_MGTRAVTT:MGTRAVTT is the I/O supply for the transmitter and receiver.
The nominal voltage is 1.8 VDC.

VCC_PSINTFP:PS full-power domain supply voltage,The nominal voltage is 0.85VDC.

VCC_PSDDR_PLL:PS DDR PLL supply voltage.The nominal voltage is 1.8VDC.(see ug583.p133)

VCC_PSPLL:PS PLL (DPLL, RPLL, APLL, VPLL, IOPLL) supply voltage.The nominal voltage is 1.2VDC

VCC_PSINTLP:PS low-power domain supply voltage.
The nominal voltage is 0.85VDC

VCC_PSINTFP_DDR:PS DDR full-power domain supply voltage.
The nominal voltage is 0.85VDC
VCC_PSINTFP_DDR must be tied to VCC_PSINTFP.

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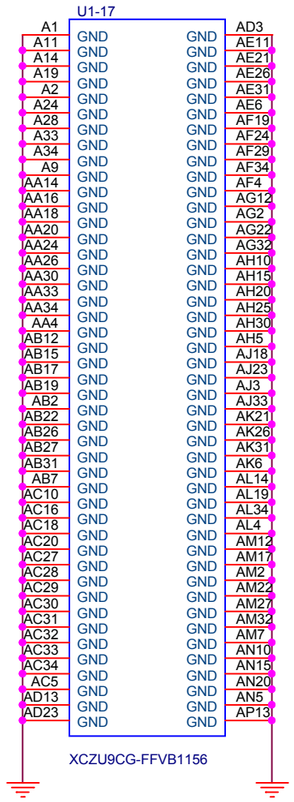
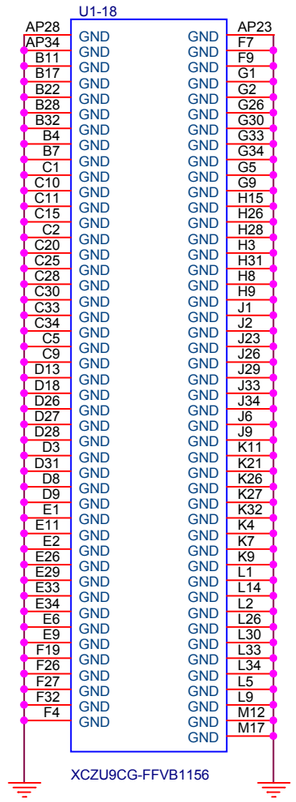
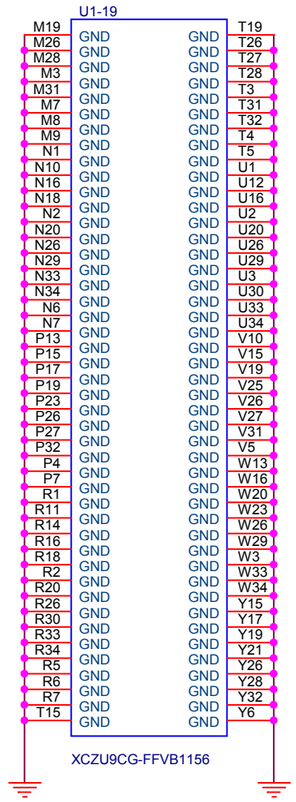
Title

Size	SCHEMATIC CODE	ZYNQ PWR	Rev
A3	PROJECT NAME	ZYNQ_NvDIMM	1.00
Date: Friday, December 29, 2017		Sheet 17 of 62	







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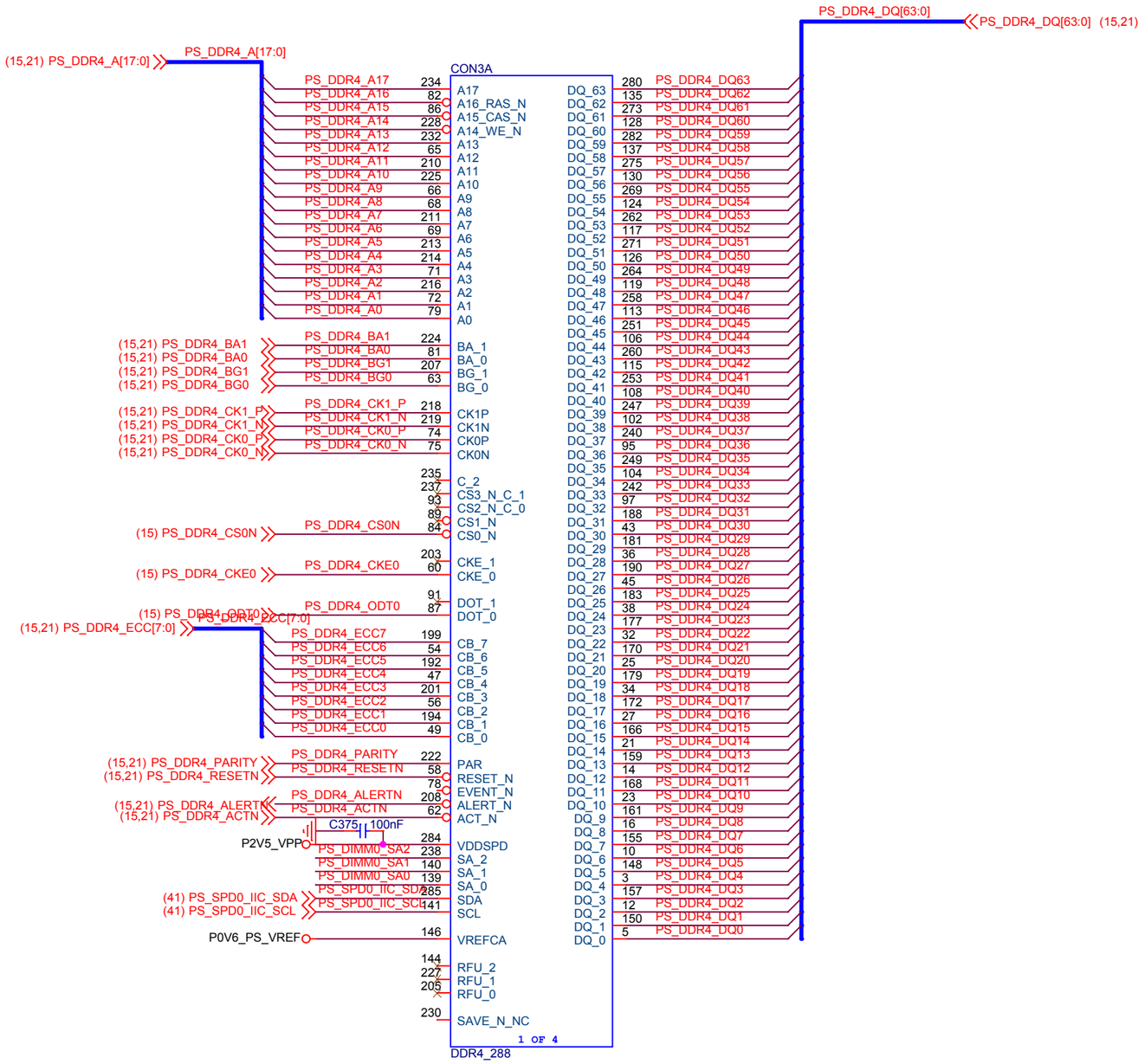
拟制：	审核：	批准：
Title		
Size A3	SCHEMATIC CODE ZYNQ GND	Rev 1.00
	PROJECT NAME ZYNQ_NvDIMM	
Date: Friday, December 29, 2017	Sheet 18 of 62	



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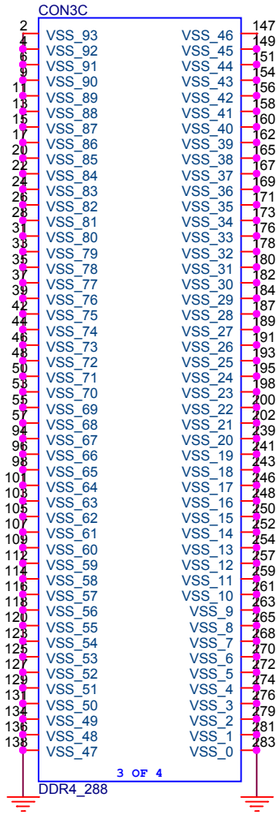
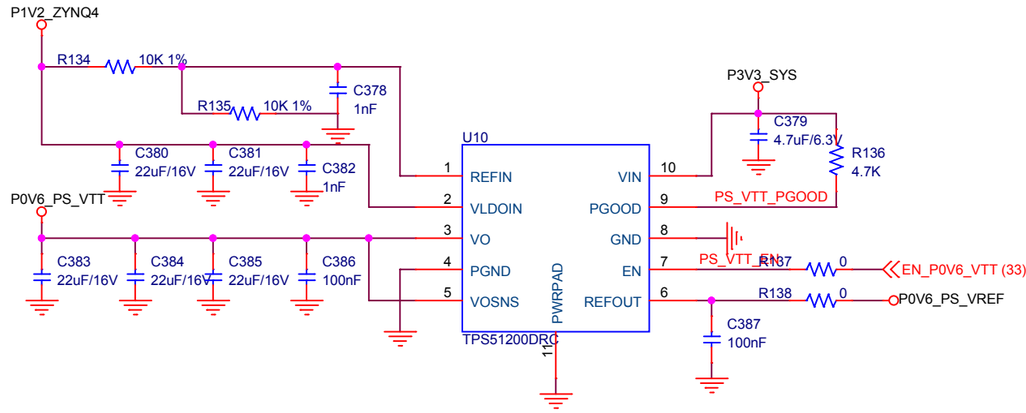
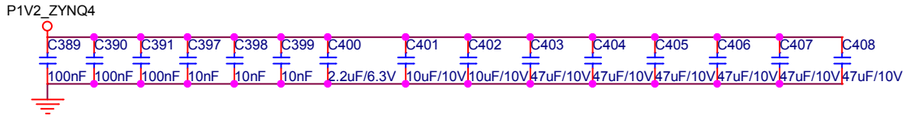
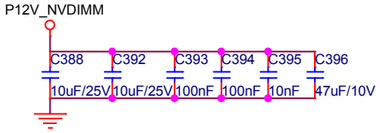
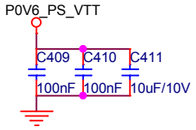
拟制：	审核：	批准：
Title		
Size A3	SCHEMATIC CODE ZYNQ PS DDR4_DIMM0	Rev 1.00
	PROJECT NAME ZYNQ_NvDIMM	
Date: Friday, December 29, 2017	Sheet 19 of 62	

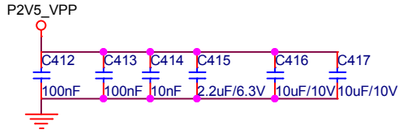












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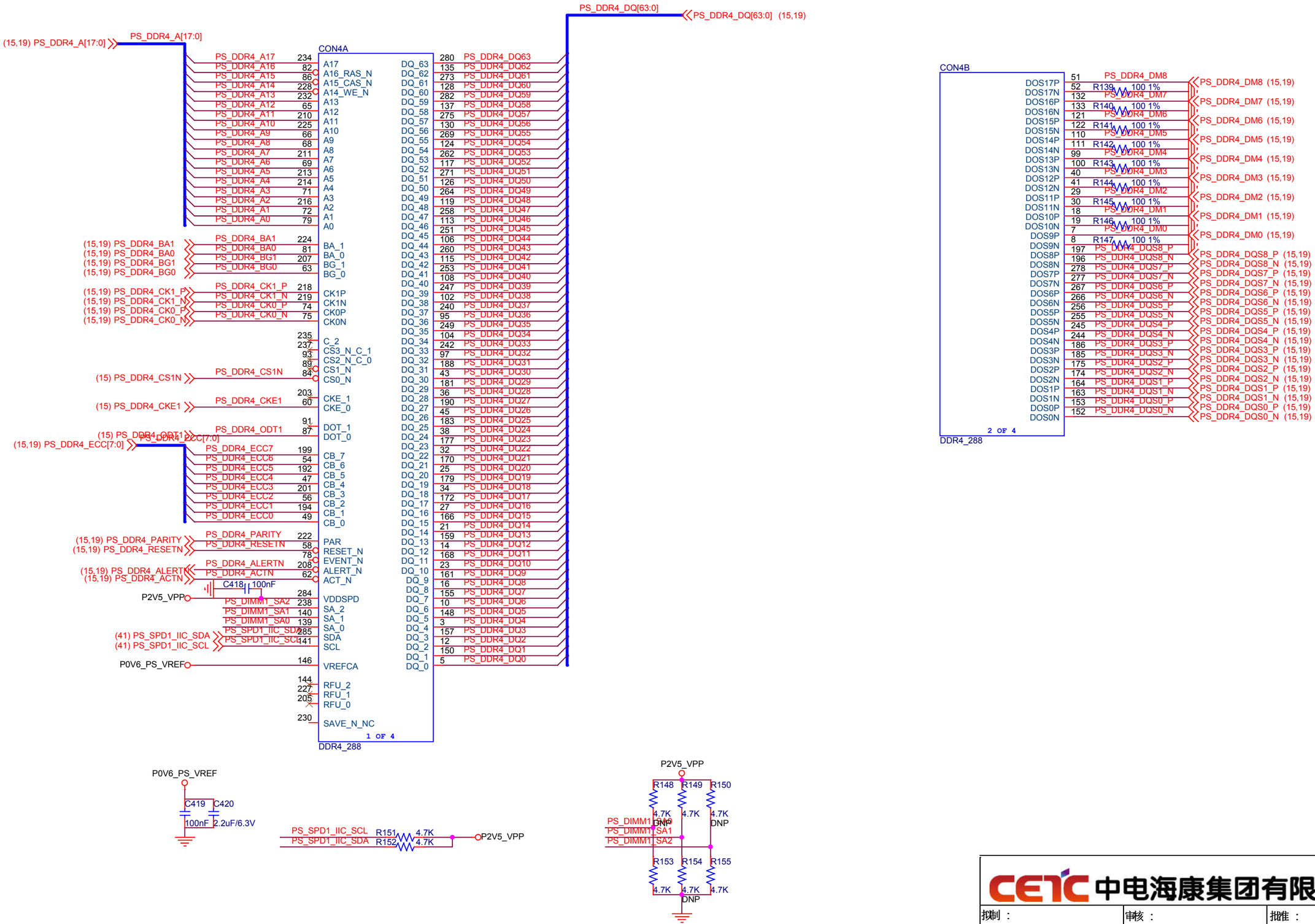
Title

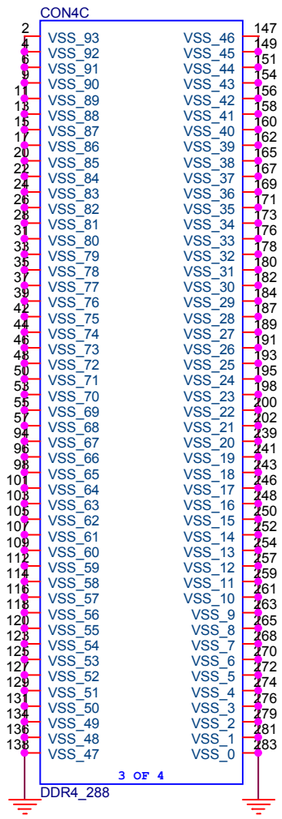
Size A3	SCHEMATIC CODE ZYNQ PS DDR4_DIMM0_POWER	Rev 1.00
	PROJECT NAME ZYNQ_NvDIMM	
Date: Friday, December 29, 2017	Sheet 20 of 62	

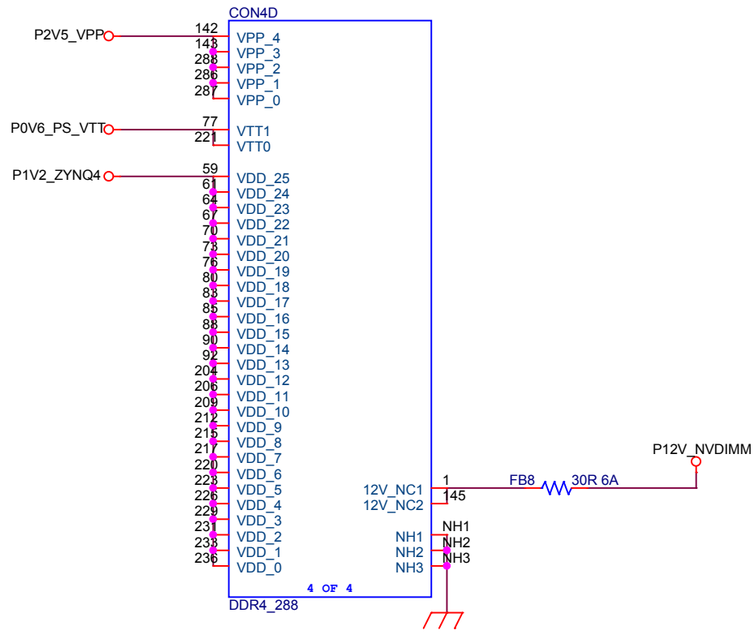


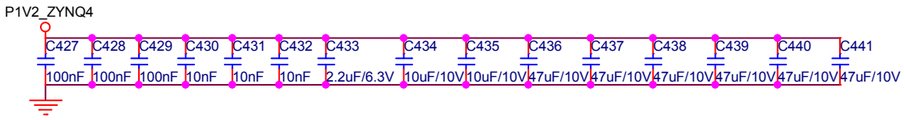
拟制：	审核：	批准：

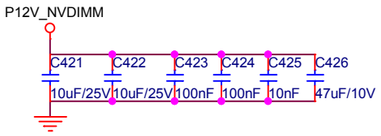
Title

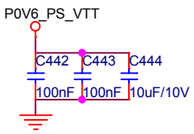
Size A3	SCHEMATIC CODE ZYNQ_PS_DDR4_DIMM1	Rev 1.00
	PROJECT NAME ZYNQ_NvDIMM	
Date: Friday, December 29, 2017	Sheet 21 of 62	

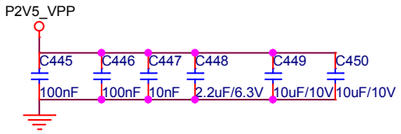












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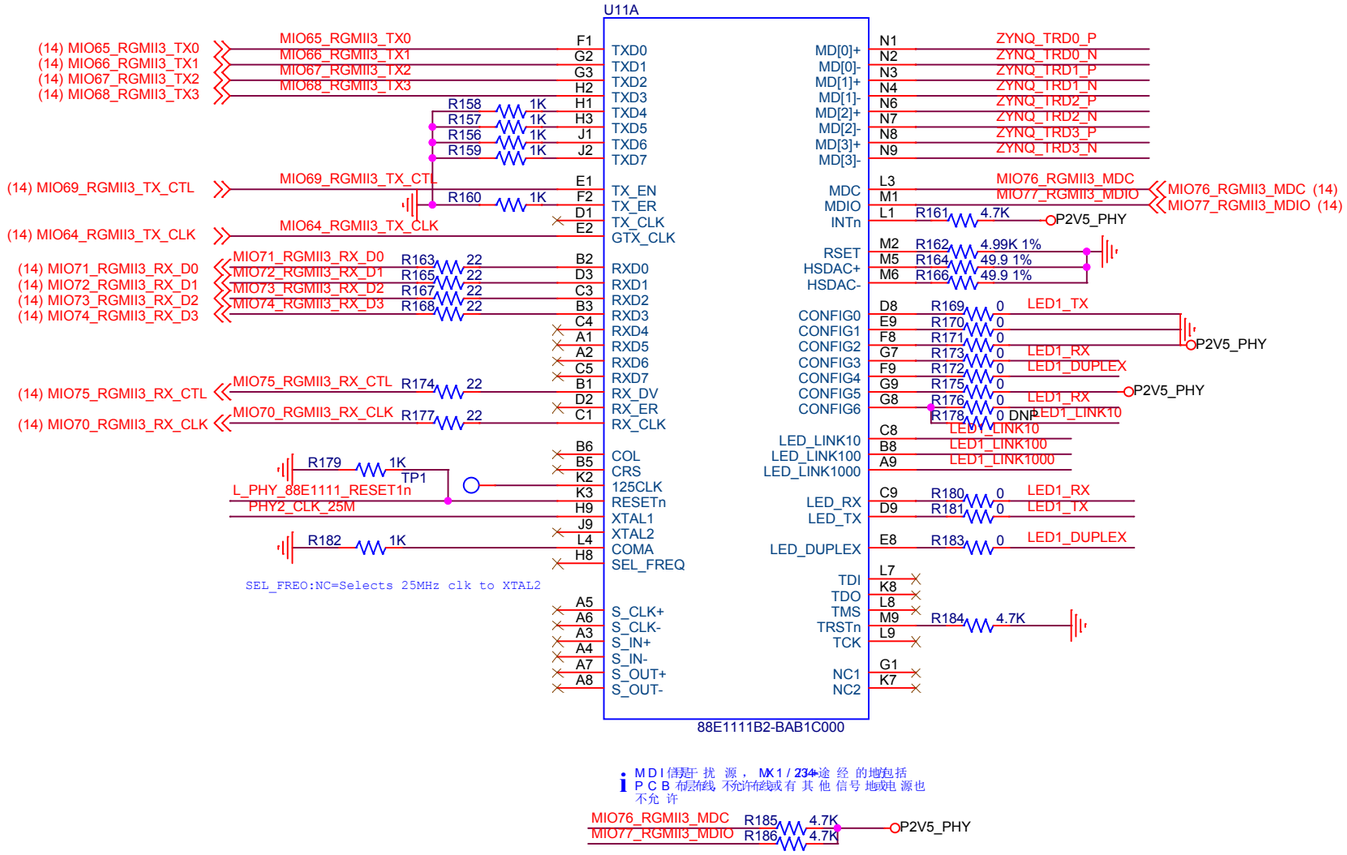
拟制：	审核：	批准：

Title

Size A3	SCHEMATIC CODE ZYNQ_PS_DDR4_DIMM1_POWER	Rev 1.00
	PROJECT NAME ZYNQ_NvDIMM	
Date: Friday, December 29, 2017	Sheet 22 of 62	



Pin	LED Pin Connection	Hardware Configuration Bit Setting	Configuration
CONFIG0	LED_TX	001	PHY Address bit[2:0] = 001
CONFIG1	VSS	000	Enable Pause,PHY Address bit[4:3] = 00
CONFIG2	VDD	111	Auto-Neg, advertise all capabilities, prefer Master
CONFIG3	LED_RX	010	Enable MDI crossover, enable 125CLK
CONFIG4	LED_DUPLEX	011	RGMII to copper
CONFIG5	VDD	111	Disable fiber/copper Auto-detect, Disable sleep
CONFIG6	LED_RX	010	Select MDC/MDIO interface, INT signal active low, 50 ohm termination for fiber

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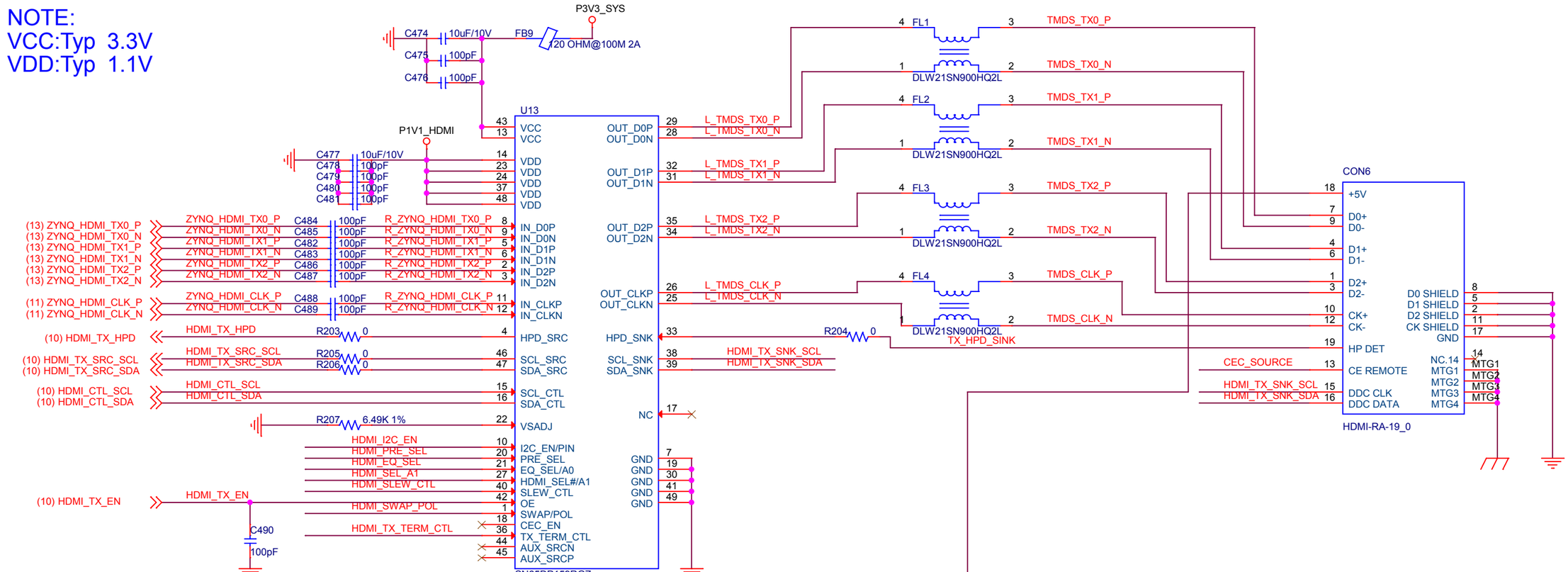
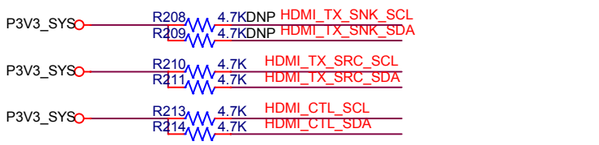
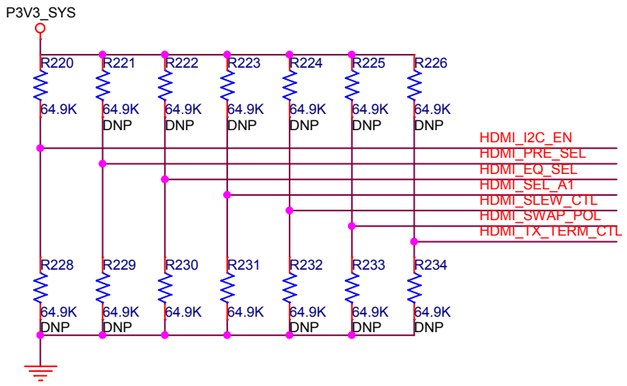
拟制：	审核：	批准：
Title		
Size: A3	SCHEMATIC CODE: ZYNQ ETH PHY	Rev: 1.00
	PROJECT NAME: ZYNQ_NvDIMM	
Date: Friday, December 29, 2017	Sheet 23 of 62	

NOTE:
VCC:Typ 3.3V
VDD:Typ 1.1V







NOTE:
I2C_EN/PIN = High; puts device into I2C control mode

PRE_SEL:PRE_SEL = No Connect: 0 dB

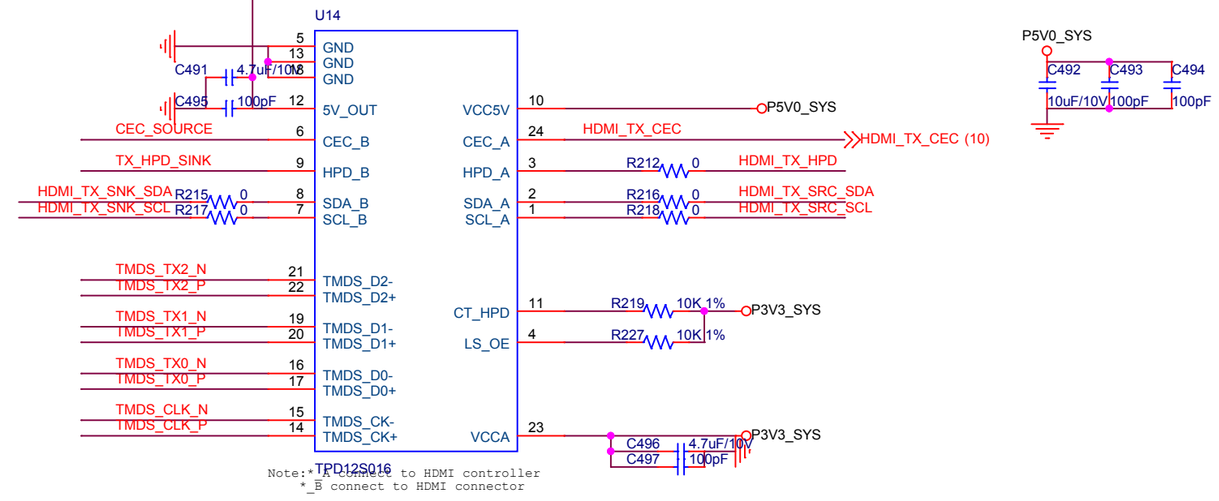
EQ_SEL/A0:When I2C_EN/PIN = High Address bit 1

HDMI_SEL/A1:When I2C_EN/PIN = High Address bit 2
Note: Weak internal pull down

SLEW_CTL:When I2C_EN/PIN = High Slew rate is controlled through I2C

SWAP/POL:SWAP/POL = No Connect normal working

TX_TERM_CTL: If left floating will be in automatic select mode.



NOTE:
HPD_A:Hot plug detect output referenced to VCCA

CEC_A:HDMI controller side CEC signal pin referenced to VCCA.
SCL_A:HDMI controller side SCL signal pin referenced to VCCA.
SDA_A:HDMI controller side SDA signal pin referenced to VCCA.
LS_OE:The OE pin is referenced to VCCA
CT_HPD:The CT_HPD is referenced to VCCA

SCL_B:HDMI connector side SCL signal pin referenced to 5V_OUT supply.
SDA_B:HDMI connector side SDA signal pin referenced to 5V_OUT supply.

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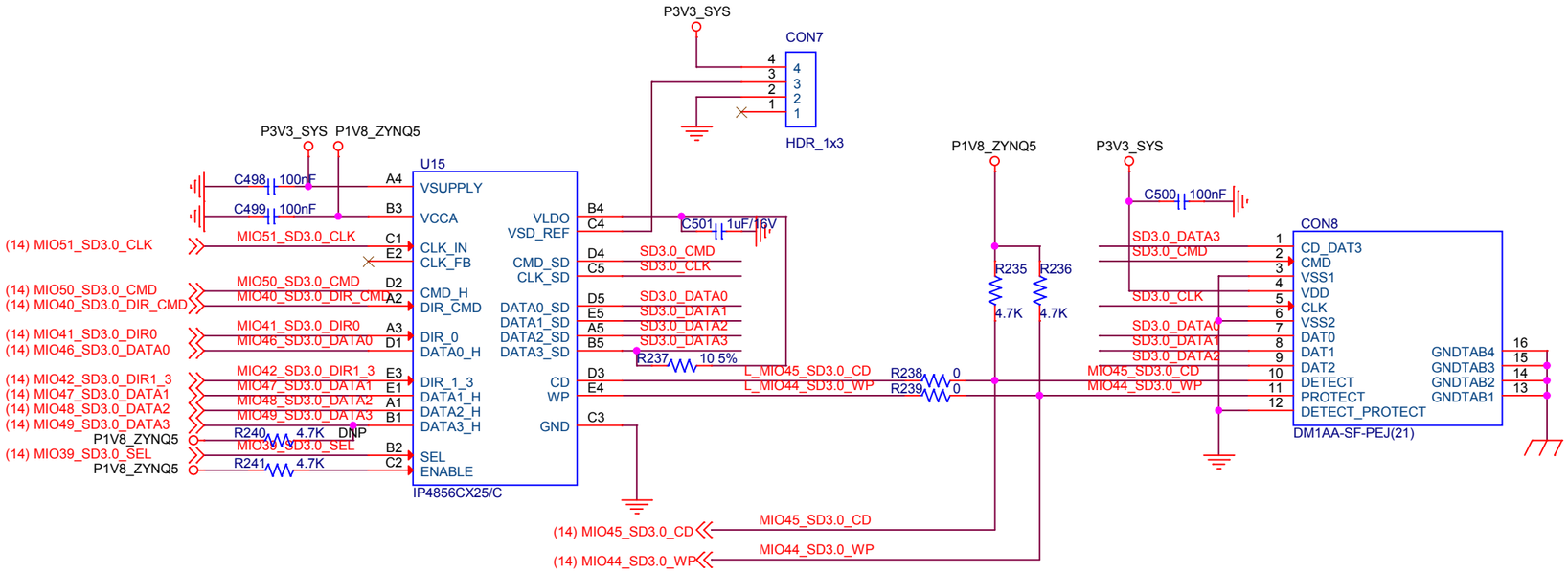
拟制：	审核：	批准：
Title		
Size: A3	SCHEMATIC CODE: ZYNQ HDMI	Rev: 1.00
	PROJECT NAME: ZYNQ_NvDIMM	
Date: Friday, December 29, 2017	Sheet 24 of 62	



NOTE:
It is designed to interface between a memory card operating at 1.8 V or 2.9 V signal levels and a host with a fixed nominal supply voltage of 1.7 V to 3.6 V.The device supports SD 3.0, SDR104, SDR50, DDR50, SDR25, SDR12 and SD 2.0 high-speed (50 MHz) and default-speed (25 MHz) modes.

ZYNQ:Support Transfers the data in SDR104, SDR50, and DDR50 modes.

The bidirectional level translator shifts the data between the I/O supply levels of the host and the memory card. Dedicated direction control signals determine if a command and data signals are transferred from the memory card to the host (card read mode) or from the host to the memory card (card write mode).

I/O function control signal truth table

Control		Host side		Memory card side	
Pin	Level	Pin	Function	Pin	Function
Pin ENABLE = HIGH and VCCA >=1.62 V					
DIR_CMD	H	CMD_H	input	CMD_SD	output
	L	CMD_H	output	CMD_SD	input
DIR_0	H	DATA0_H	input	DATA0_SD	output
	L	DATA0_H	output	DATA0_SD	input
DIR_1_3	H	DATA1_H	input	DATA1_SD	output
		DATA2_H	input	DATA2_SD	output
		DATA3_H	input	DATA3_SD	output
	L	DATA1_H	output	DATA1_SD	input
		DATA2_H	output	DATA2_SD	input
		DATA3_H	output	DATA3_SD	input
-	-	CLK_IN	input	CLK_SD	output
-	-	CLK_FB	output	-	-
Pin ENABLE = LOW or VCCA <= 0.8 V					
DIR_CMD	X	CMD_H	Hi-Z	CMD_SD	Hi-Z
DIR_0	X	DATA0_H	Hi-Z	DATA0_SD	Hi-Z
DIR_1_3	X	DATA1_H	Hi-Z	DATA1_SD	Hi-Z
		DATA2_H	Hi-Z	DATA2_SD	Hi-Z
		DATA3_H	Hi-Z	DATA3_SD	Hi-Z
-	-	CLK_IN	input	CLK_SD	Hi-Z
-	-	CLK_IN	Hi-Z	-	-

SD card side voltage level control signal truth table

Input		Output		
SEL	VSD_REF	VLDO	Pin	Function
H	X	1.8 V	DATA0_SD to DATA3_SD, CLK_SD	low supply voltage level (1.8 V typical)
L	< 1 V	2.9 V	DATA0_SD to DATA3_SD, CLK_SD	high supply voltage level (2.9 V typical)
	> 1.5 V	VSD_REF	DATA0_SD to DATA3_SD, CLK_SD	supply voltage level based on VSD_REF

Pins Write Protect (WP) and Card Detection (CD) might be pulled down by the memory card which has to be detected by the host. Both signals must be HIGH if no card is inserted.So pull-up resistors connected to the host supply VCCA.

VCCA:supply voltage from host side
CMD_H, DATA0_H to DATA3_H and CLK_IN SEL, ENABLE, DIR_0, DIR_1_3 and DIR_CMD
Referenced to VCCA(1.8V)

VSUPPLY:supply voltage(3.3V)

VLDO:internal supply decoupling

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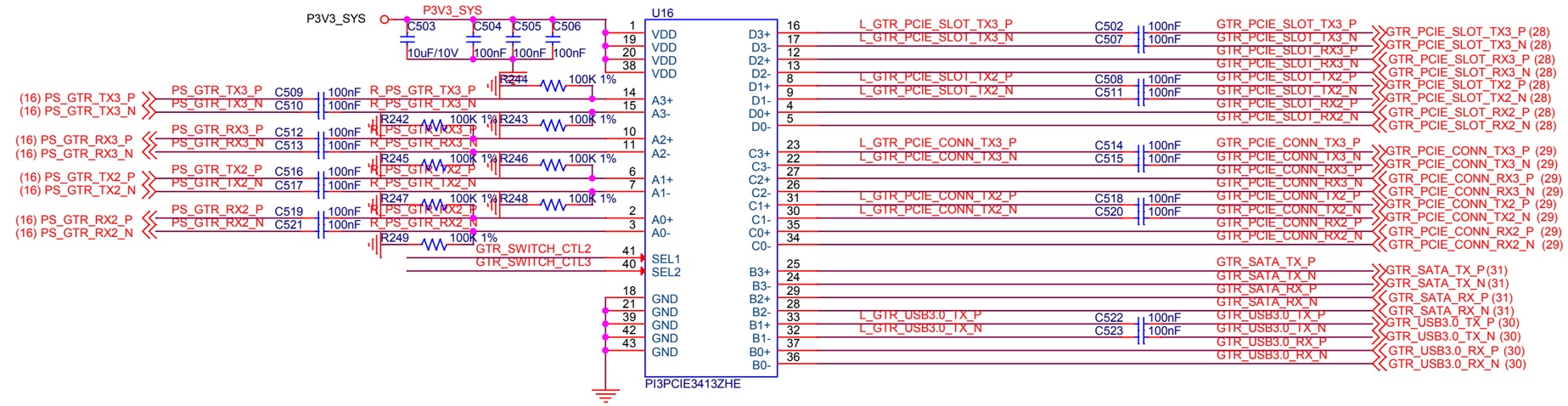
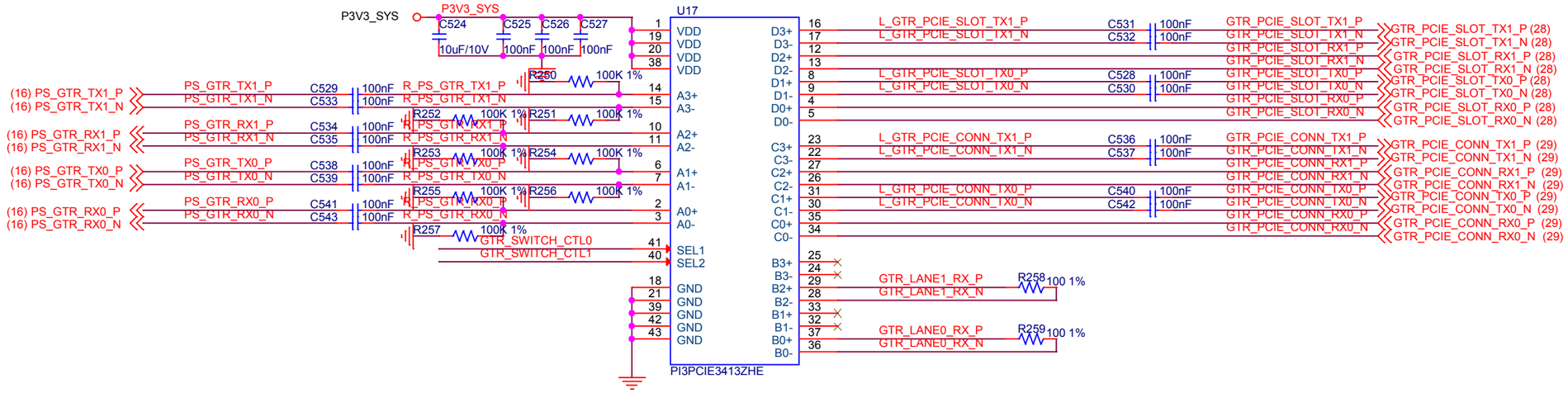
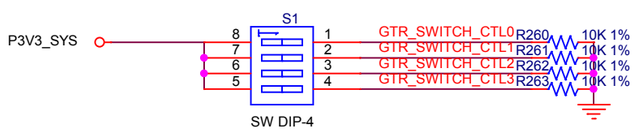
拟制：	审核：	批准：

Title

Size A3	SCHEMATIC CODE ZYNQ SD3.0	Rev 1.00
	PROJECT NAME ZYNQ_NvDIMM	
Date: Friday, December 29, 2017	Sheet 25 of 62	







NOTE:
Supply Voltage 3.3V

SEL1	SEL2	Function
0	0	Power down all switch hi-z
0	1	A<-->B
1	0	A<-->C
1	1	A<-->D

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拟制：	审核：	批准：

Title

Size	SCHEMATIC CODE	ZYNQ GTR SWITCH	Rev
A3	PROJECT NAME	ZYNQ_NvDIMM	1.00

Date: Friday, December 29, 2017 Sheet 26 of 62

C556 1nF/2KV
R292 1M

C557 1nF/2KV
R295 1M

C558 1nF/2KV
R297 1M

C563 1nF/2KV
R307 1M

P3V3_SYS

L10 4.7uH 6A
L11 4.7uH 6A

C544 22uF/16V
C545 100nF
C546 22uF/16V
C547 100nF

CON9

VCCT 16
VCCR 15
VEET 1
VEET 17
VEET 20
VEET
VEER 10
VEER 11
VEER 14
VEER

TD+ 18 GTH_SFP0_TX_P
TD- 19 GTH_SFP0_TX_N
RD+ 13 GTH_SFP0_RX_P
RD- 12 GTH_SFP0_RX_N
TX_FAULT 2 GTH_SFP0_TX_FAULT
TX_DISABLE 3 GTH_SFP0_TX_DISABLE
SDA 4 GTH_SFP0_SDA
SCL 5 GTH_SFP0_SCL
MOD_ABS 6 GTH_SFP0_MOD_ABS
RS0 7 GTH_SFP0_RS0
RS1 9 GTH_SFP0_RS1
RX_LOS 8 GTH_SFP0_RX_LOS

Molex_074441-0001

GTH_SFP0_TX_P (13)
GTH_SFP0_TX_N (13)
GTH_SFP0_RX_P (13)
GTH_SFP0_RX_N (13)

P3V3_SYS
R264 R268 R265 R266 R269 R267 4.7K

TP2
GTH_SFP0_TX_DISABLE (10)
TP3
GTH_SFP0_SDA (41)
GTH_SFP0_SCL (41)
TP4

P3V3_SYS
R270 R271 4.7K
R272 R273 4.7K DNP

P3V3_SYS

L12 4.7uH 6A
L13 4.7uH 6A

C548 22uF/16V
C549 100nF
C550 22uF/16V
C551 100nF

CON10

VCCT 16
VCCR 15
VEET 1
VEET 17
VEET 20
VEET
VEER 10
VEER 11
VEER 14
VEER

TD+ 18 GTH_SFP1_TX_P
TD- 19 GTH_SFP1_TX_N
RD+ 13 GTH_SFP1_RX_P
RD- 12 GTH_SFP1_RX_N
TX_FAULT 2 GTH_SFP1_TX_FAULT
TX_DISABLE 3 GTH_SFP1_TX_DISABLE
SDA 4 GTH_SFP1_SDA
SCL 5 GTH_SFP1_SCL
MOD_ABS 6 GTH_SFP1_MOD_ABS
RS0 7 GTH_SFP1_RS0
RS1 9 GTH_SFP1_RS1
RX_LOS 8 GTH_SFP1_RX_LOS

Molex_074441-0001

GTH_SFP1_TX_P (13)
GTH_SFP1_TX_N (13)
GTH_SFP1_RX_P (13)
GTH_SFP1_RX_N (13)

P3V3_SYS
R274 R275 R276 R277 R278 R279 4.7K

TP5
GTH_SFP1_TX_DISABLE (10)
GTH_SFP1_SDA (41)
GTH_SFP1_SCL (41)
TP6
TP7

P3V3_SYS
R280 R281 4.7K
R282 R285 4.7K DNP

P3V3_SYS

L14 4.7uH 6A
L15 4.7uH 6A

C552 22uF/16V
C553 100nF
C554 22uF/16V
C555 100nF

CON11

VCCT 16
VCCR 15
VEET 1
VEET 17
VEET 20
VEET
VEER 10
VEER 11
VEER 14
VEER

TD+ 18 GTH_SFP2_TX_P
TD- 19 GTH_SFP2_TX_N
RD+ 13 GTH_SFP2_RX_P
RD- 12 GTH_SFP2_RX_N
TX_FAULT 2 GTH_SFP2_TX_FAULT
TX_DISABLE 3 GTH_SFP2_TX_DISABLE
SDA 4 GTH_SFP2_SDA
SCL 5 GTH_SFP2_SCL
MOD_ABS 6 GTH_SFP2_MOD_ABS
RS0 7 GTH_SFP2_RS0
RS1 9 GTH_SFP2_RS1
RX_LOS 8 GTH_SFP2_RX_LOS

Molex_074441-0001

GTH_SFP2_TX_P (13)
GTH_SFP2_TX_N (13)
GTH_SFP2_RX_P (13)
GTH_SFP2_RX_N (13)

P3V3_SYS
R283 R286 R287 R284 R288 R289 4.7K

TP8
GTH_SFP2_TX_DISABLE (10)
GTH_SFP2_SDA (41)
GTH_SFP2_SCL (41)
TP9
TP10

P3V3_SYS
R290 R291 4.7K
R293 R294 4.7K DNP

P3V3_SYS

L16 4.7uH 6A
L17 4.7uH 6A

C559 22uF/16V
C560 100nF
C561 22uF/16V
C562 100nF

CON12

VCCT 16
VCCR 15
VEET 1
VEET 17
VEET 20
VEET
VEER 10
VEER 11
VEER 14
VEER

TD+ 18 GTH_SFP3_TX_P
TD- 19 GTH_SFP3_TX_N
RD+ 13 GTH_SFP3_RX_P
RD- 12 GTH_SFP3_RX_N
TX_FAULT 2 GTH_SFP3_TX_FAULT
TX_DISABLE 3 GTH_SFP3_TX_DISABLE
SDA 4 GTH_SFP3_SDA
SCL 5 GTH_SFP3_SCL
MOD_ABS 6 GTH_SFP3_MOD_ABS
RS0 7 GTH_SFP3_RS0
RS1 9 GTH_SFP3_RS1
RX_LOS 8 GTH_SFP3_RX_LOS

Molex_074441-0001

GTH_SFP3_TX_P (13)
GTH_SFP3_TX_N (13)
GTH_SFP3_RX_P (13)
GTH_SFP3_RX_N (13)

P3V3_SYS
R298 R299 R300 R301 R296 R302 4.7K

TP11
GTH_SFP3_TX_DISABLE (10)
GTH_SFP3_SDA (41)
GTH_SFP3_SCL (41)
TP12
TP13

P3V3_SYS
R303 R304 4.7K
R305 R306 4.7K DNP

CON13 Molex_074754-0410

SHELL1 SHELL2 SHELL3 SHELL4 SHELL5 SHELL6 SHELL7 SHELL8 SHELL9 SHELL10 SHELL11 SHELL12 SHELL13 SHELL14 SHELL15 SHELL16 SHELL17 SHELL18 SHELL19 SHELL20 SHELL21 SHELL22 SHELL23 SHELL24 SHELL25 SHELL26 SHELL27 SHELL28 SHELL29 SHELL30 SHELL31 SHELL32 SHELL33 SHELL34 SHELL35 SHELL36 SHELL37 SHELL38 SHELL39 SHELL40 SHELL41 SHELL42 SHELL43 SHELL44 SHELL45 SHELL46 SHELL47 SHELL48 SHELL49 SHELL50 SHELL51 SHELL52 SHELL53 SHELL54 SHELL55 SHELL56 SHELL57 SHELL58 SHELL59 SHELL60 SHELL61 SHELL62 SHELL63

H1 H2 H3 H4 H5 H6 H7 H8 H9 H10 H11 H12 H13 H14 H15 H16 H17 H18 H19 H20 H21 H22 H23 H24 H25 H26 H27 H28 H29 H30 H31 H32 H33 H34 H35 H36 H37 H38 H39 H40 H41 H42 H43 H44 H45 H46 H47 H48 H49 H50 H51 H52 H53 H54 H55 H56 H57 H58 H59 H60 H61 H62 H63

SFP+ Cage

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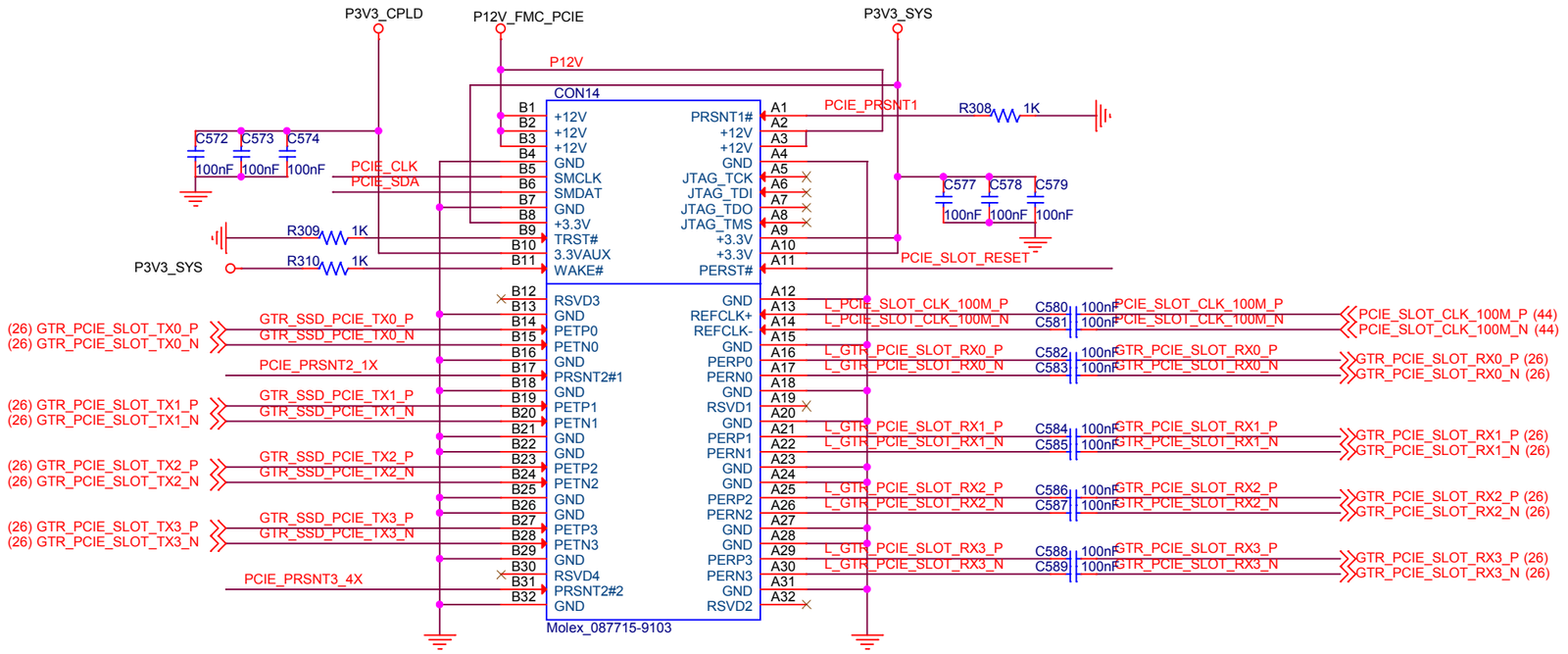
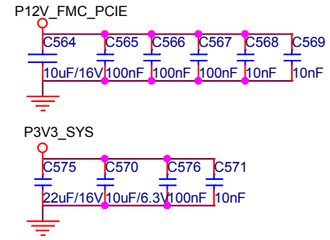
拟制：	审核：	批准：

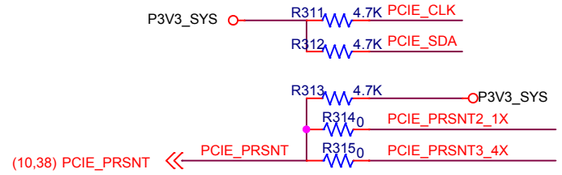
Title

Size	SCHEMATIC CODE	ZYNQ SFP	Rev
A3	PROJECT NAME	ZYNQ_NvDIMM	1.00

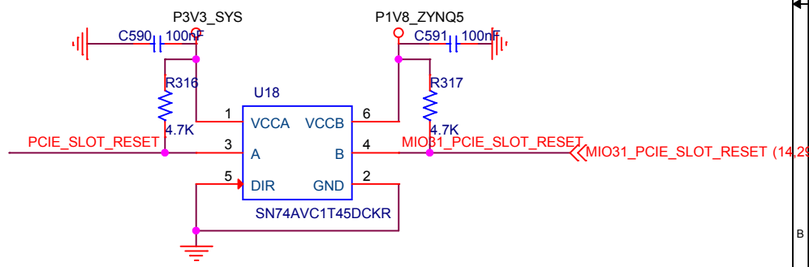
Date: Friday, December 29, 2017 Sheet 27 of 62



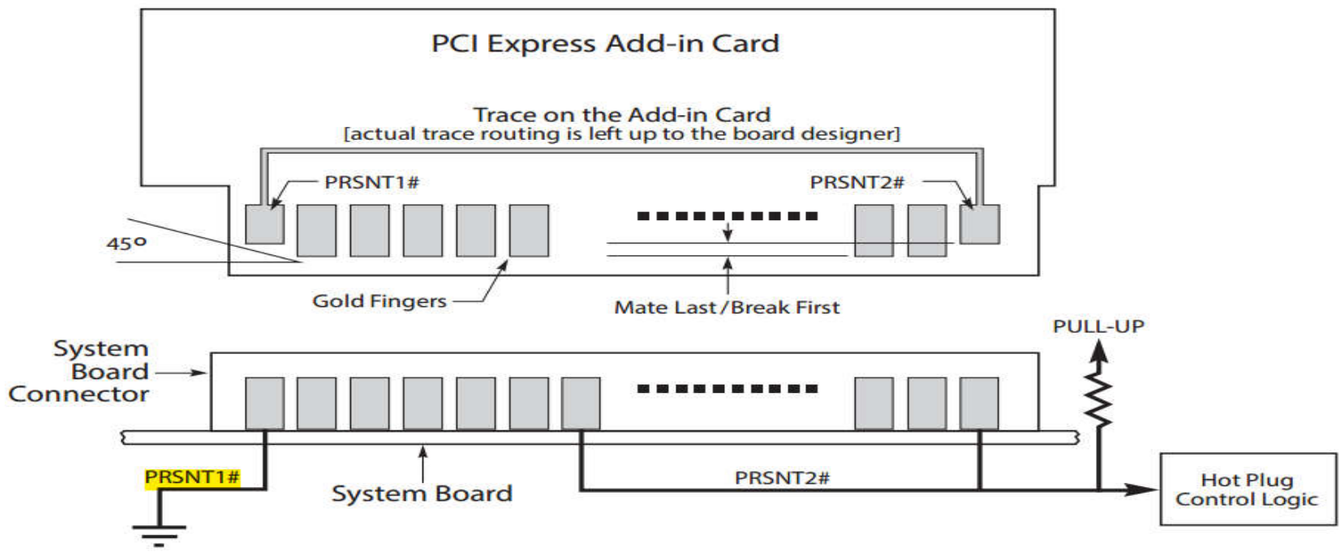




PCIe RST



NOTE:
DIR:DIR Input Circuit Referenced to VCCA.
L:B Data --> A Bus;
H:A Data --> B Bus.



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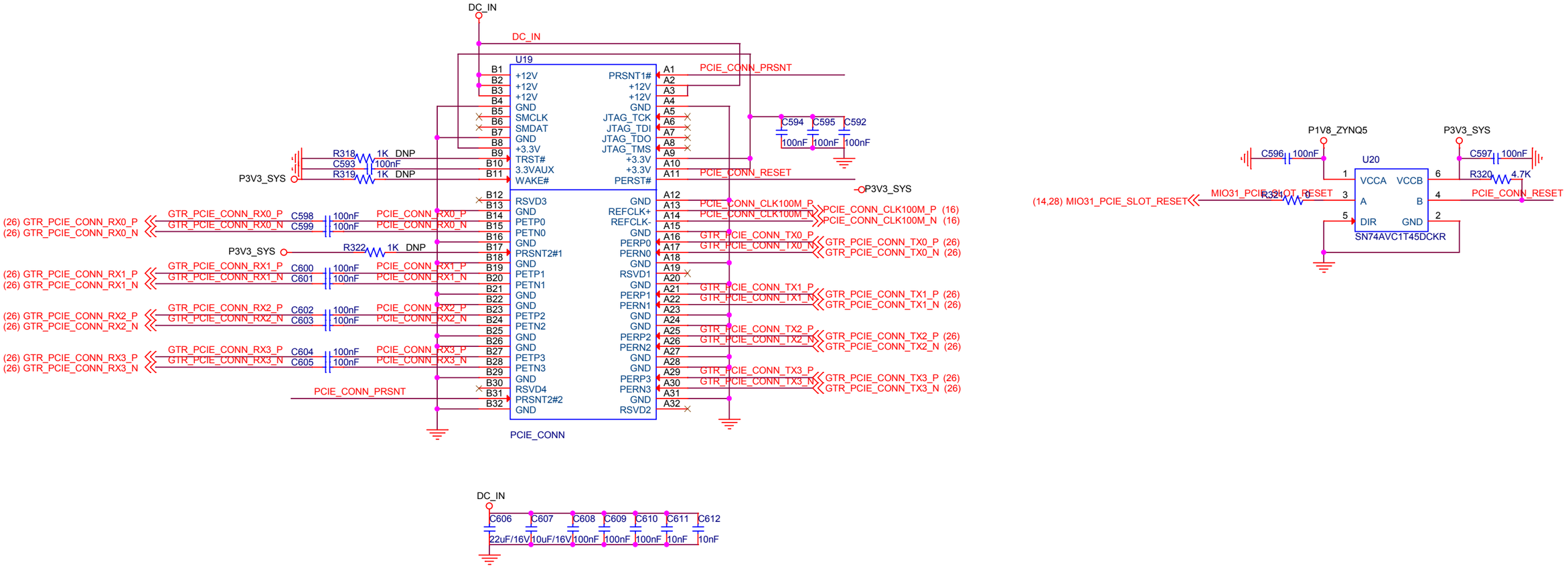
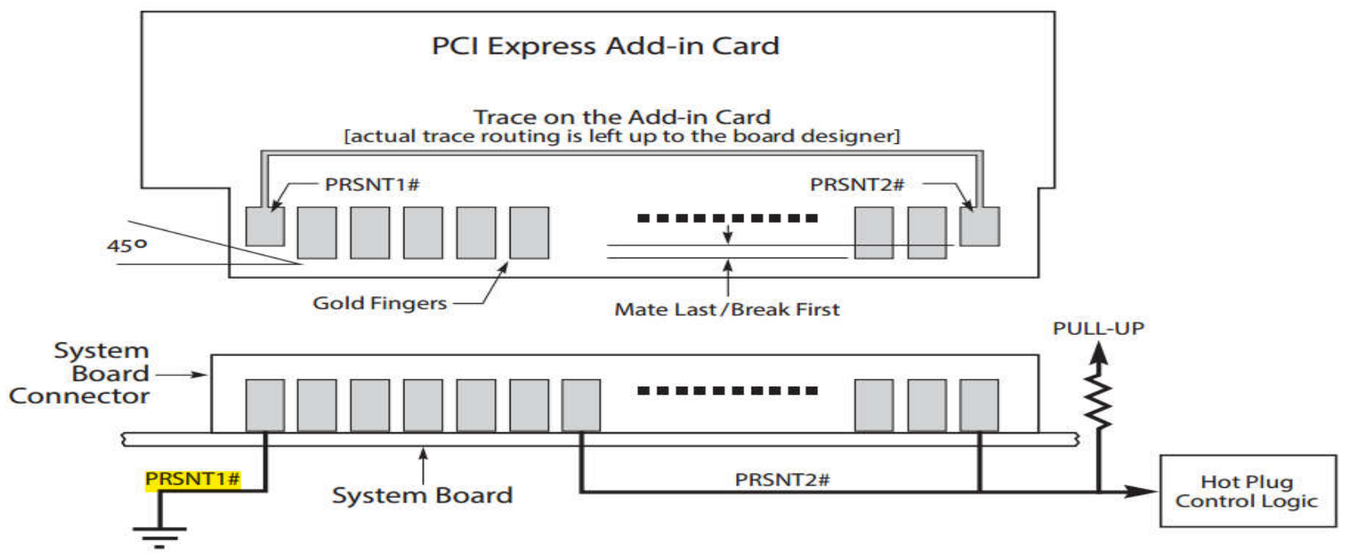
拟制：	审核：	批准：

Title

Size: A3	SCHEMATIC CODE: ZYNQ PCIE SLOT	Rev: 1.00
	PROJECT NAME: ZYNQ_NvDIMM	
Date: Friday, December 29, 2017	Sheet 28 of 62	





拟制：	审核：	批准：
Title		
Size: A3	SCHEMATIC CODE: ZYNQ PCIE CONN	Rev: 1.00
	PROJECT NAME: ZYNQ_NvDIMM	
Date: Friday, December 29, 2017	Sheet 29 of 62	

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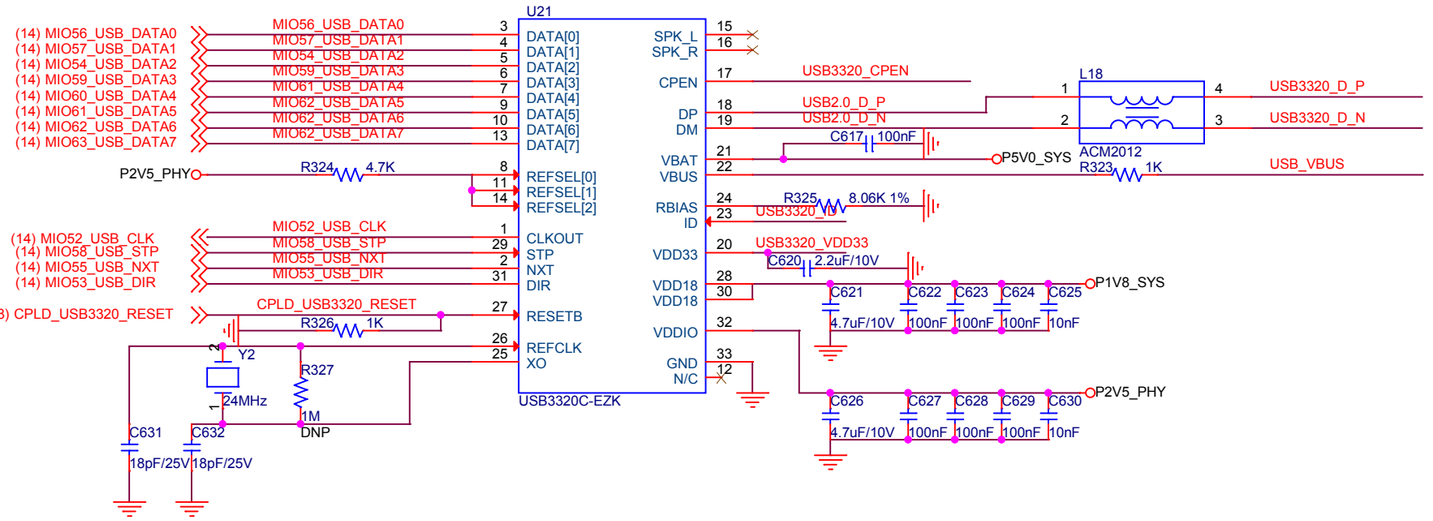

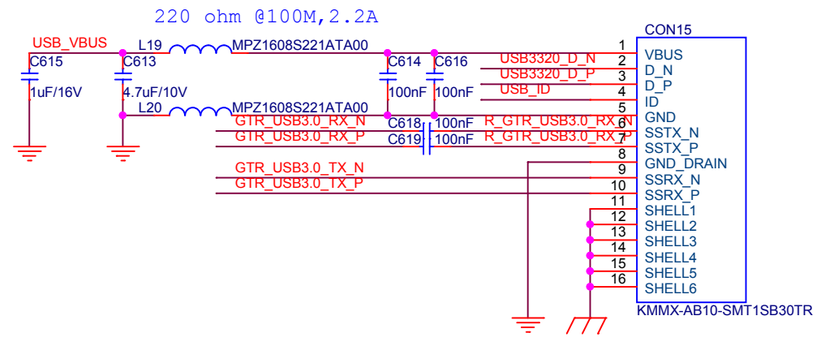

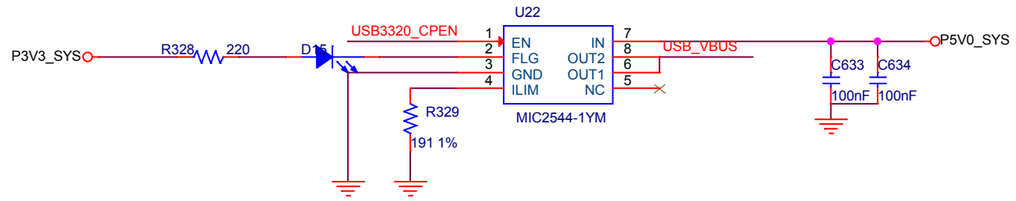

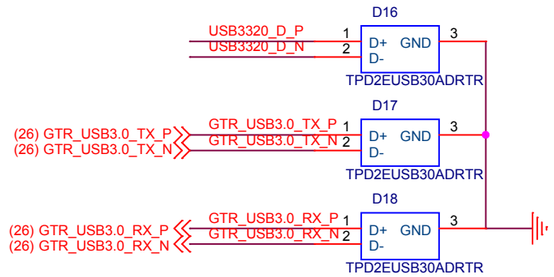

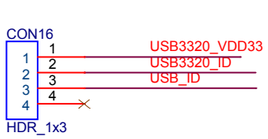

REQUIRED RVBUS RESISTOR VALUE

Configuration Pins			Description
REFSEL[2]	REFSEL[1]	REFSEL[0]	Reference Frequency
0	0	0	52 MHz
0	0	1	38.4MHz
0	1	0	12MHz
0	1	1	27MHz
1	0	0	13MHz
1	0	1	19.2MHz
1	1	0	26MHz
1	1	1	24MHz

REQUIRED RVBUS RESISTOR VALUE

Operating Mode	Rvbus
Device only	10k ± 5%
OTG	1k ± 5%
Host	10k ± 5%

CAPACITANCE VALUES AT VBUS OF USB CONNECTOR

Mode	MIN Value	MAX Value
Host	120uF	--
Device	1uF	10uF
OTG	1uF	6.5uF

VDDIO:
External 1.8V to 3.3V ULPI supply input pin.
This voltage sets the value of VOH for the
ULPI signals. This pad needs to be bypassed
with a 0.1uF capacitor to ground,placed as
close as possible to the USB3320.

VDD18:
External 1.8V Supply input pin. This pad
needs to be bypassed with a 0.1uF capacitor
to ground, placed as close as possible to
the USB3320.

CPEN:
External 5V supply enable. Controls the external
VBUS power switch. CPEN is low on POR.

RBIAS:
This pin requires an 8.06k(± 1%) resistor to ground,
placed as close as possible to the USB3320.
Nominal voltage during ULPI operation is 0.8V.

RESETB,CLKOUT,STP,DIR,NXT,DATA[7:0],REFCLK are referenced to VDDIO

VDD33:
3.3V Regulator Output. A 2.2uF (<1 ohm ESR)
bypass capacitor to ground is required for
regulator stability. The bypass capacitor should
be placed as close as possible to the USB3320.

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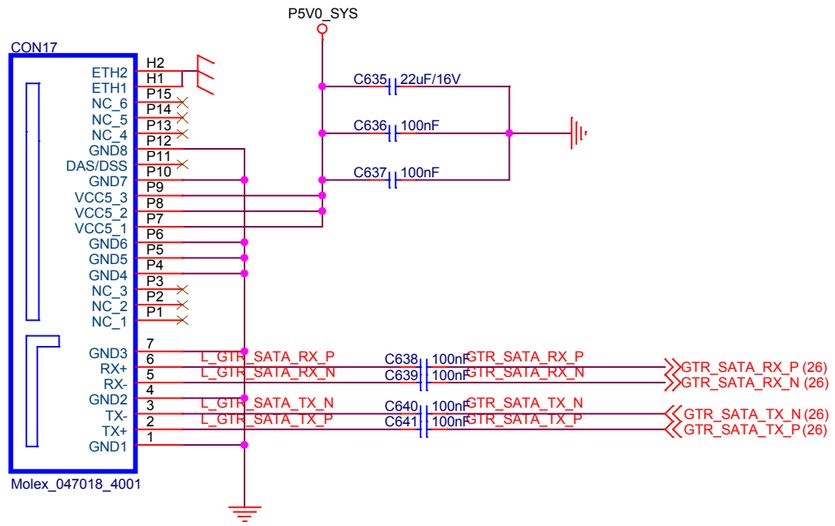
拟制：	审核：	批准：

Title

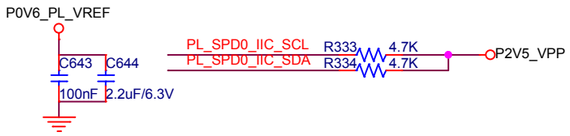
Size: A3	SCHEMATIC CODE: ZYNQ USB2.0/3.0	Rev: 1.00
	PROJECT NAME: ZYNQ_NvDIMM	
Date: Friday, December 29, 2017	Sheet 30 of 62	

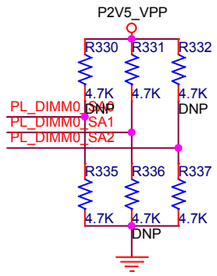


拟制：	审核：	批准：

Title

Size A3	SCHEMATIC CODE ZYNQ SATA	Rev 1.00
	PROJECT NAME ZYNQ_NvDIMM	
Date: Friday, December 29, 2017	Sheet 31 of 62	





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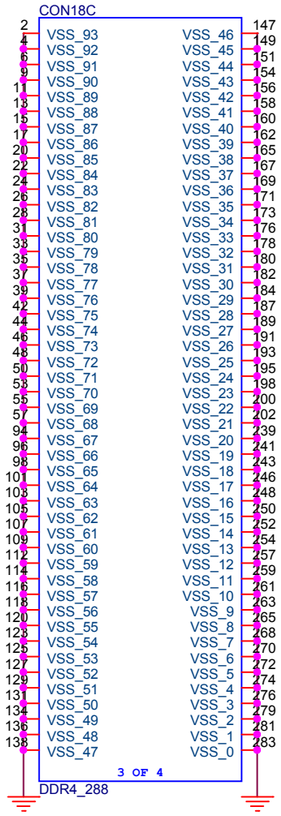
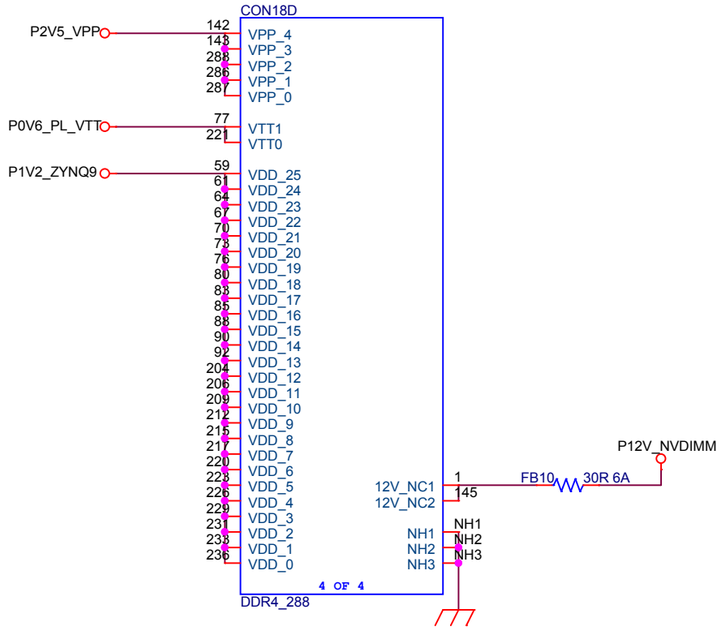
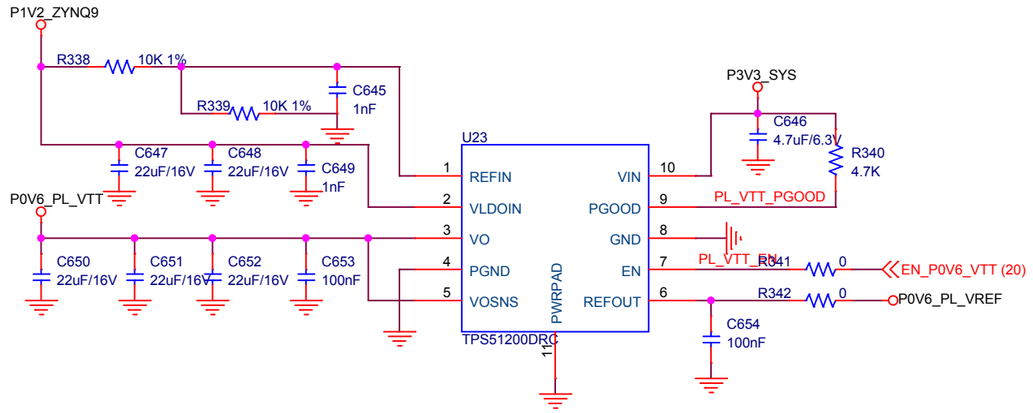
拟制：	审核：	批准：

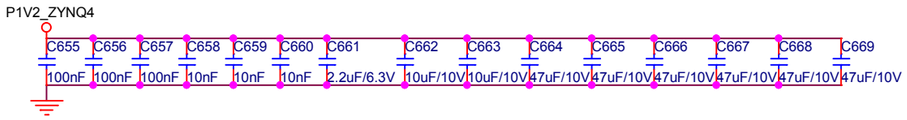
Title

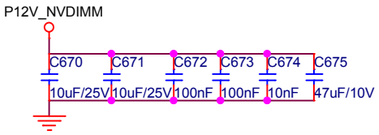
Size A3	SCHEMATIC CODE ZYNQ PL NvDIMM	Rev 1.00
	PROJECT NAME ZYNQ_NvDIMM	
Date: Friday, December 29, 2017	Sheet 32 of 62	

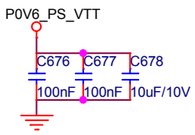


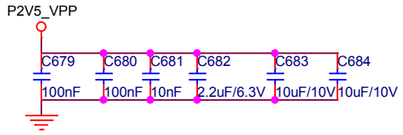












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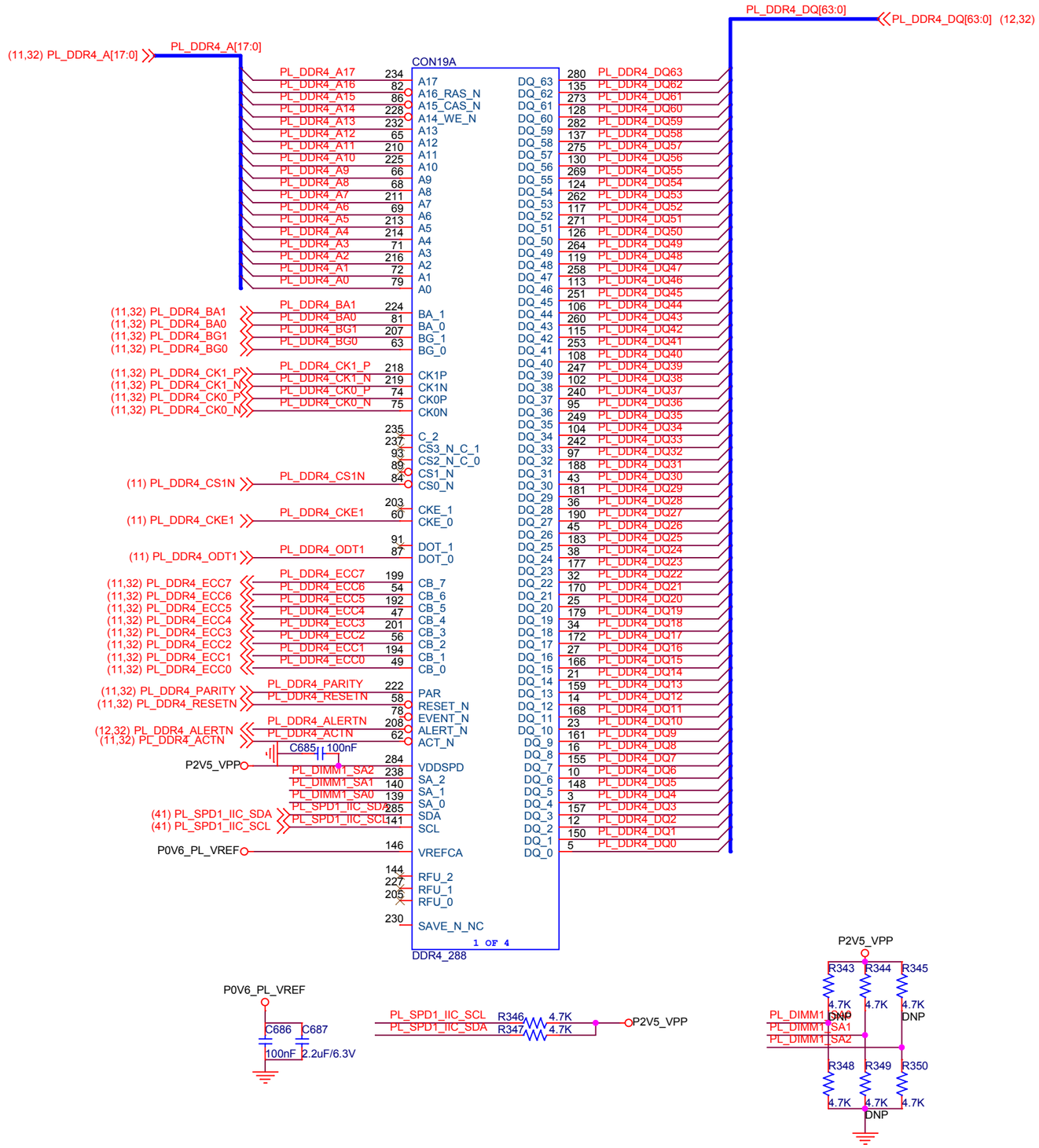
拟制：	审核：	批准：

Title

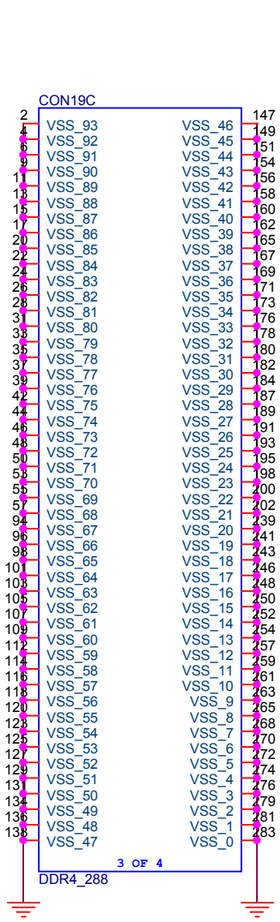
Size A3	SCHEMATIC CODE ZYNQ_PL_NvDIMM_POWER	Rev 1.00
	PROJECT NAME ZYNQ_NvDIMM	
Date: Friday, December 29, 2017	Sheet 33 of 62	

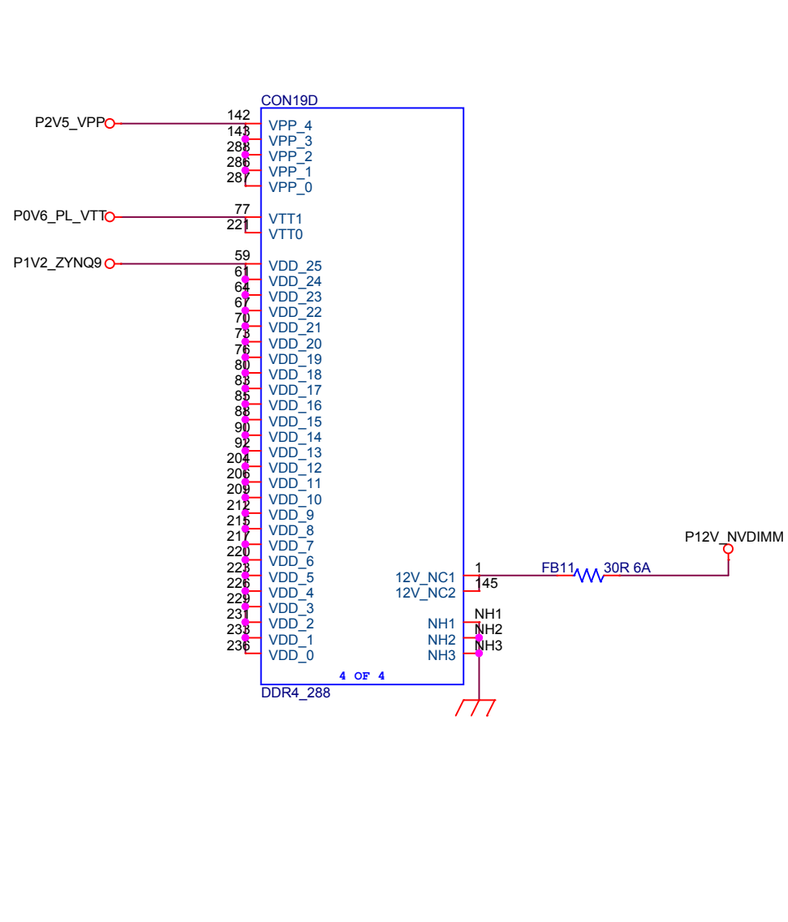


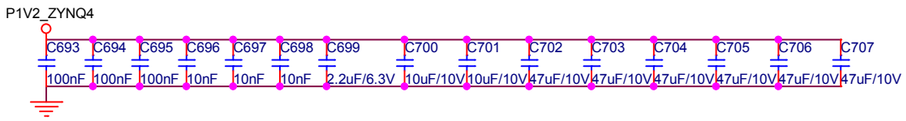
拟制：	审核：	批准：

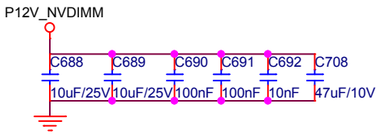
Title

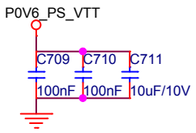
Size A3	SCHEMATIC CODE ZYNQ_PL_DDR4_DIMM	Rev 1.00
	PROJECT NAME ZYNQ_NvDIMM	
Date: Friday, December 29, 2017	Sheet 34 of 62	

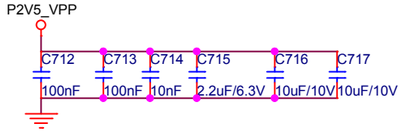












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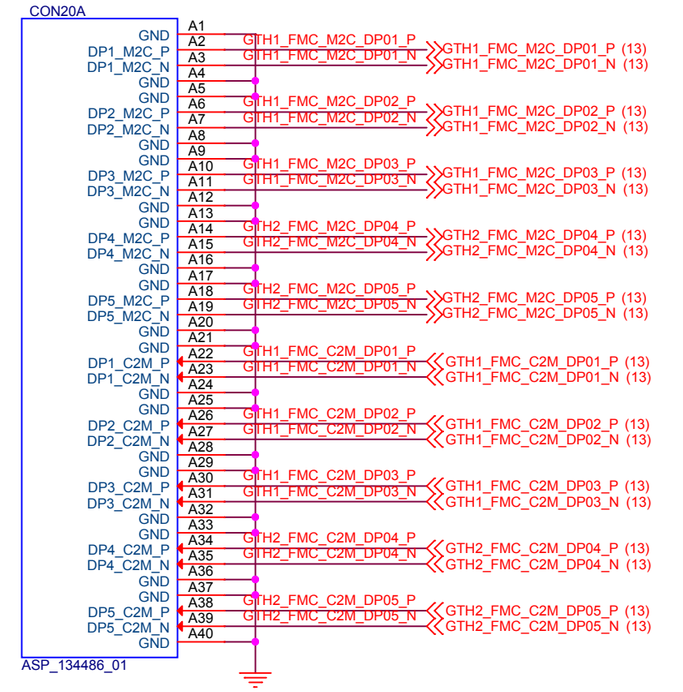
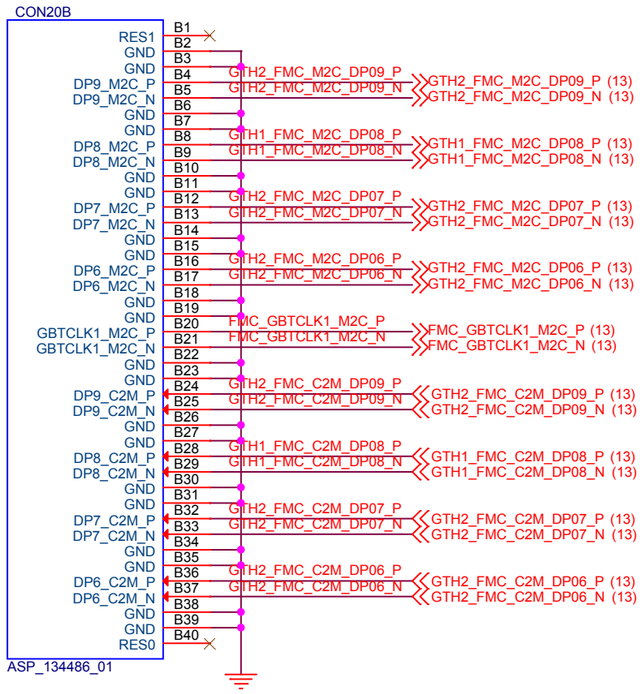
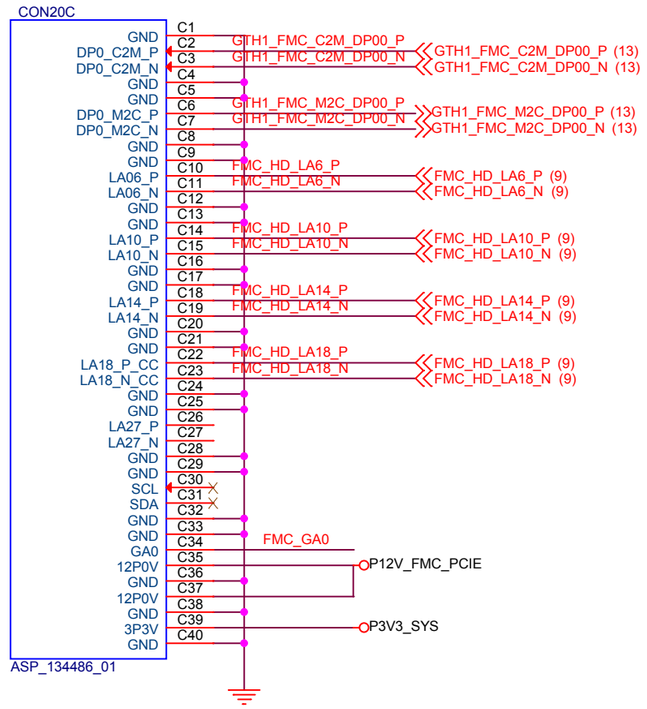
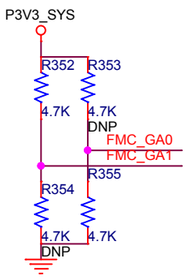
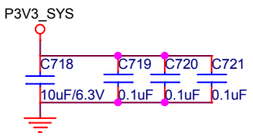
Title		
Size A3	SCHEMATIC CODE ZYNQ_PL_DDR4_DIMM_POWER	Rev 1.00
	PROJECT NAME ZYNQ_NvDIMM	
Date: Friday, December 29, 2017	Sheet 35 of 62	

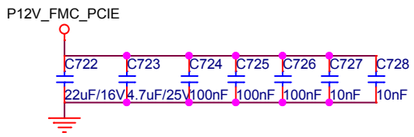


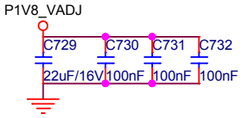












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拟制：	审核：	批准：

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Size	SCHEMATIC CODE	ZYNQ_PL_FMC1	Rev
A3	PROJECT NAME	ZYNQ_NvDIMM	1.00
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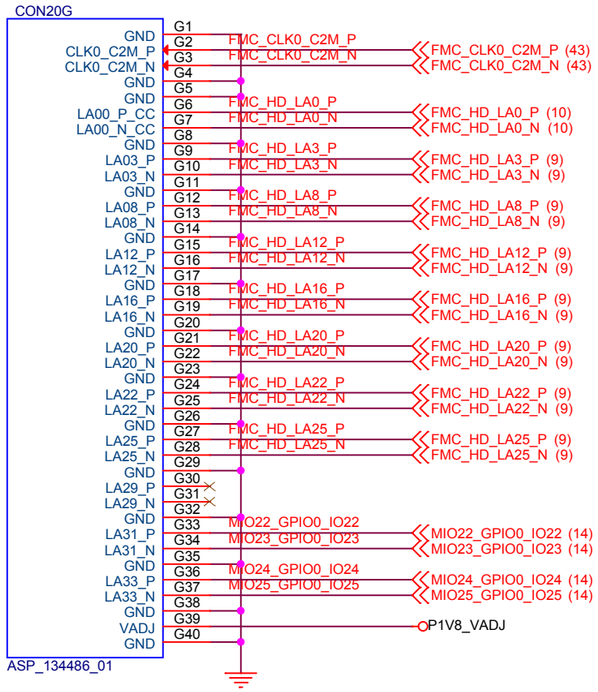

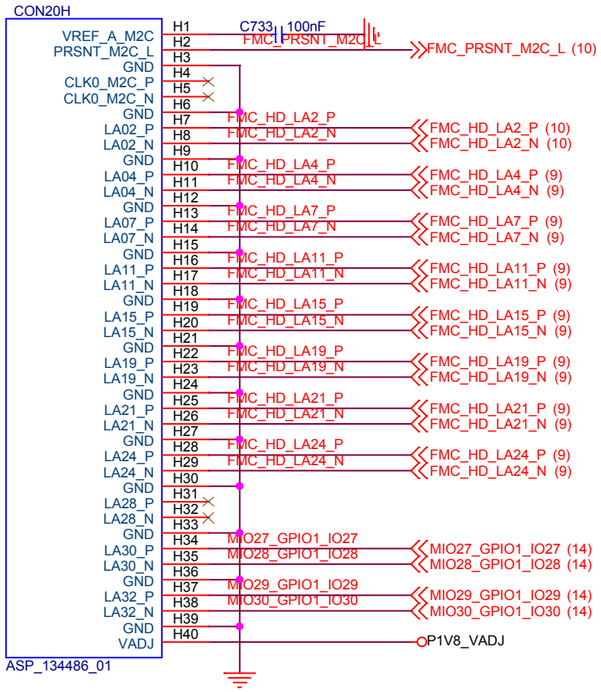

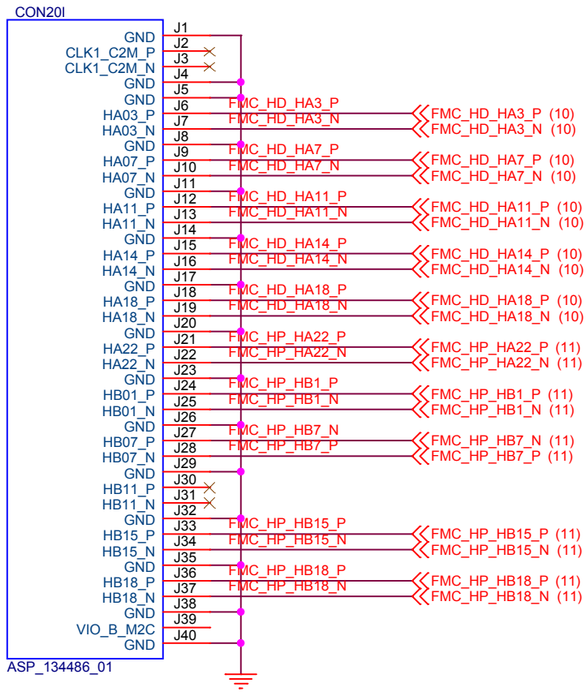

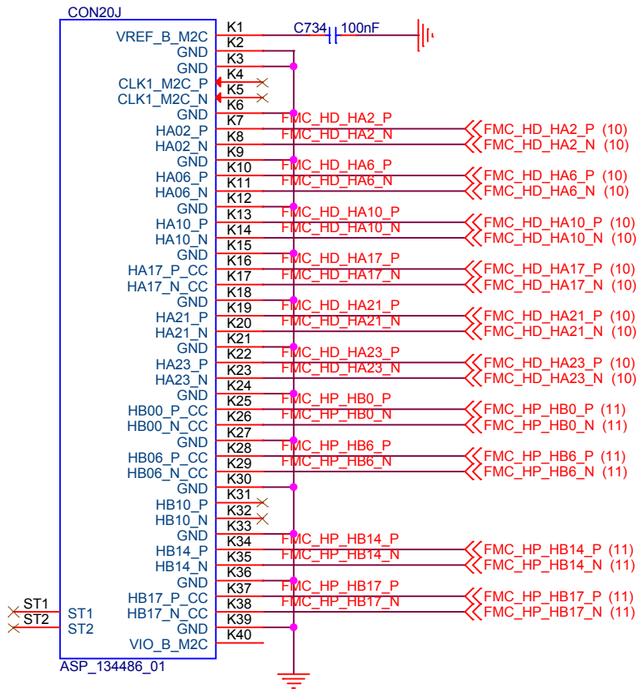

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拟制：	审核：	批准：

Title

Size A3	SCHEMATIC CODE ZYNQ_PL_FMC2	Rev 1.00
	PROJECT NAME ZYNQ_NvDIMM	
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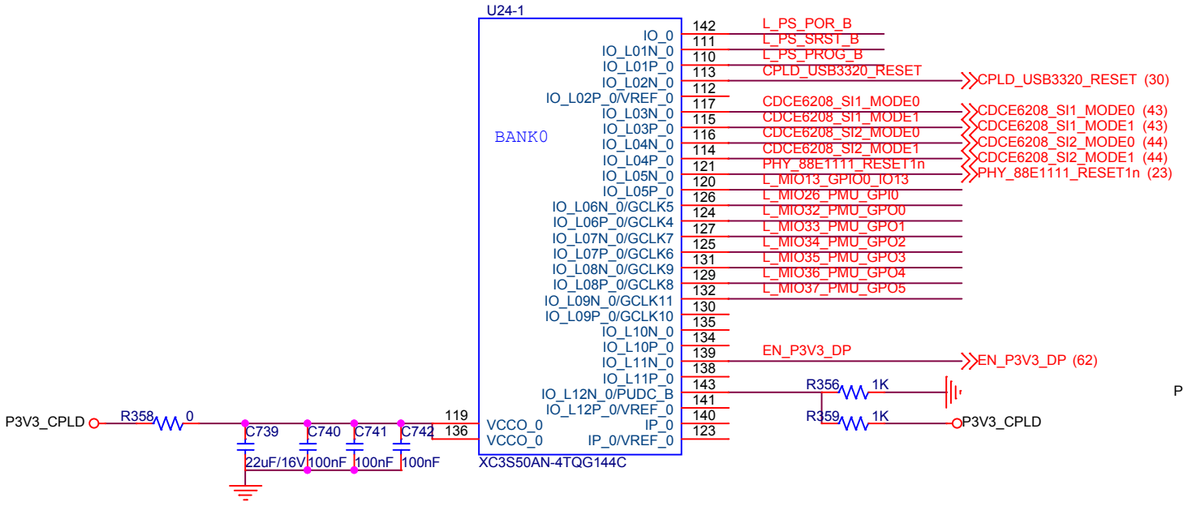
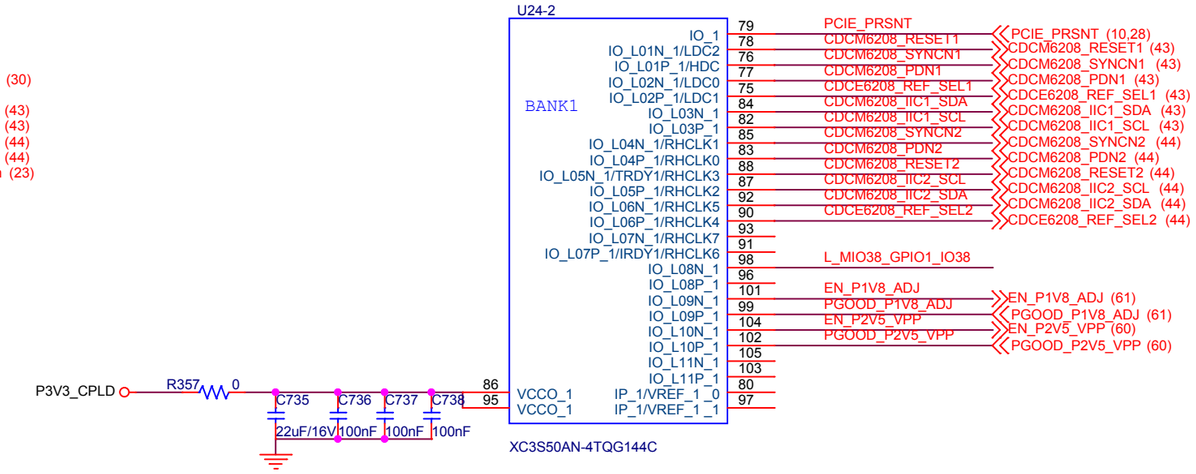
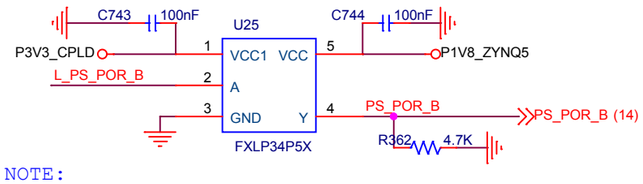
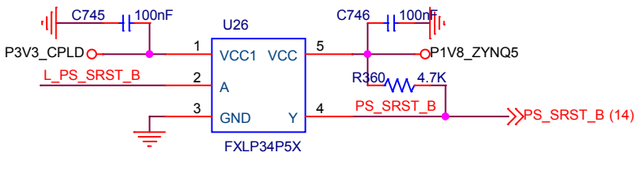


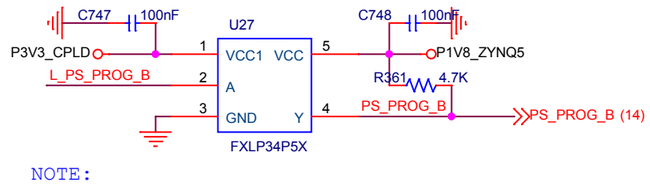




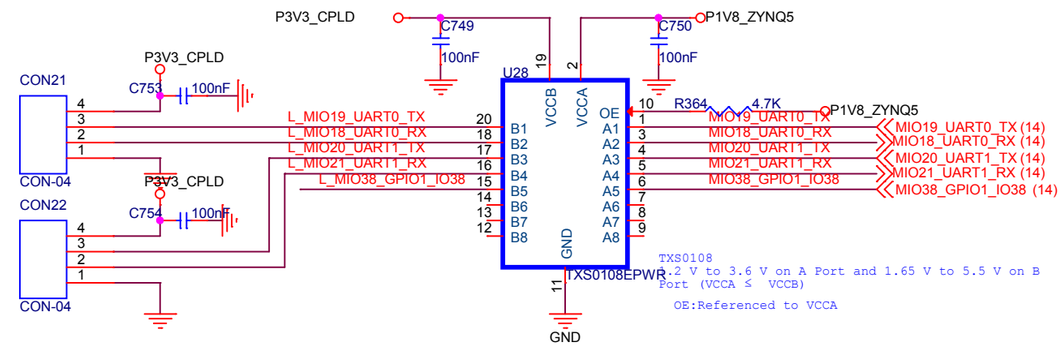
NOTE:
PS_POR_B must be held at 0 until all
PS power supplies meet voltage requirements and
the PS_CLK reference is within specification.

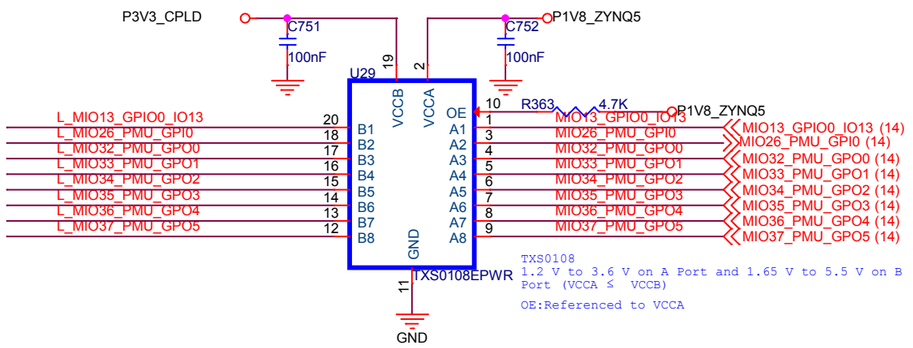


NOTE:
PS_SRST_B:System reset. For use when debugging. When 0,
forces the PS to enter the system reset sequence.



NOTE:
PROG_B signal to reset configuration block. Requires
an external pull-up resistor.





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拟制：	审核：	批准：

Title

Size	SCHEMATIC CODE	CPLD BANK0/1	Rev
A3	PROJECT NAME	ZYNQ_NvDIMM	1.00

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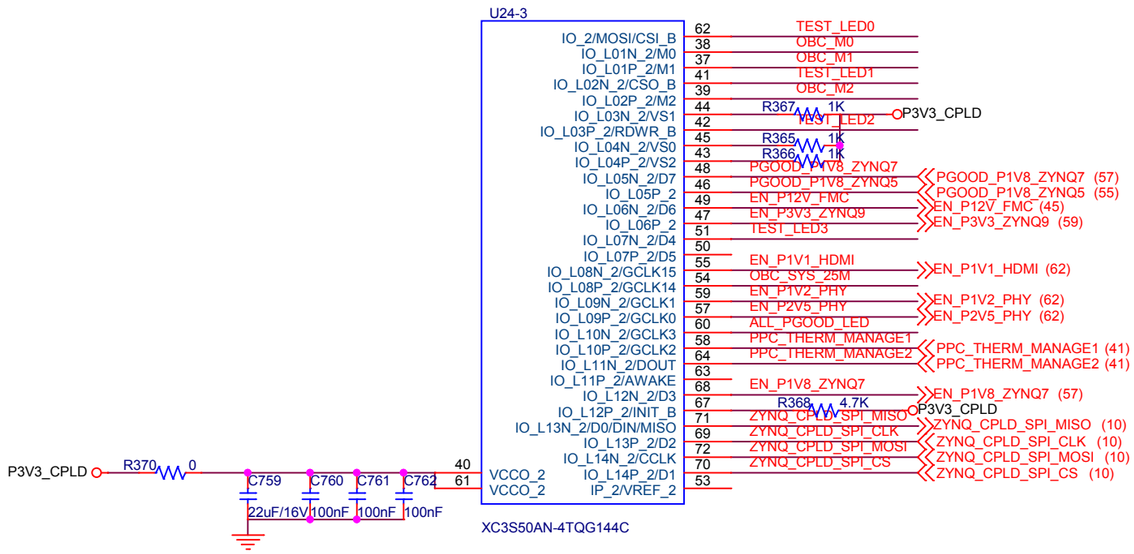
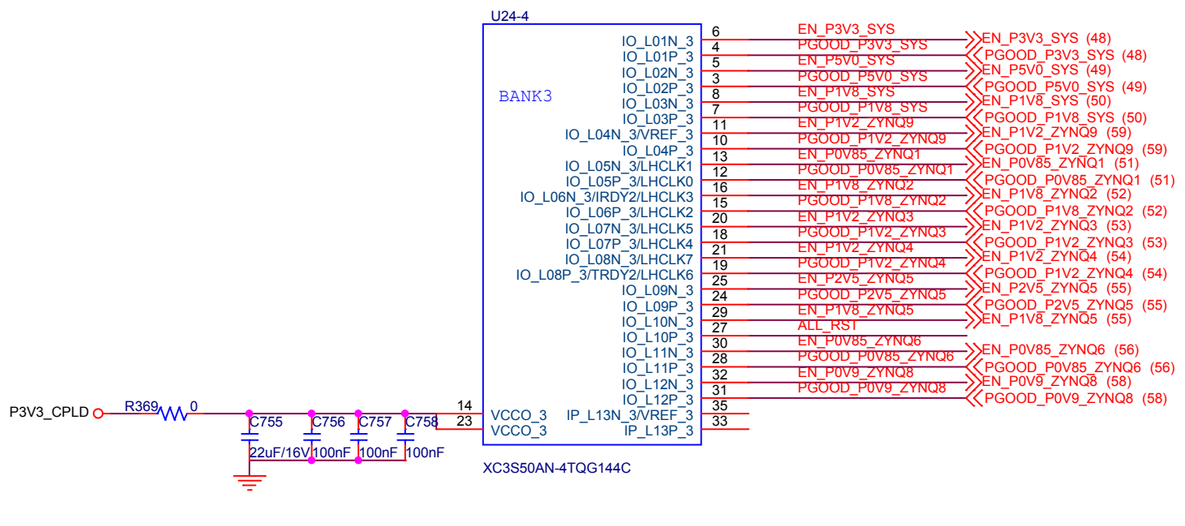
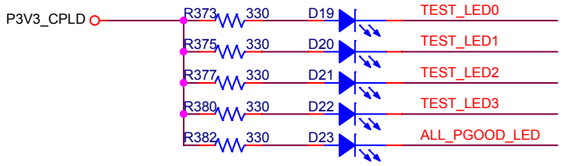
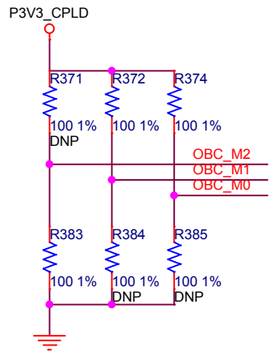
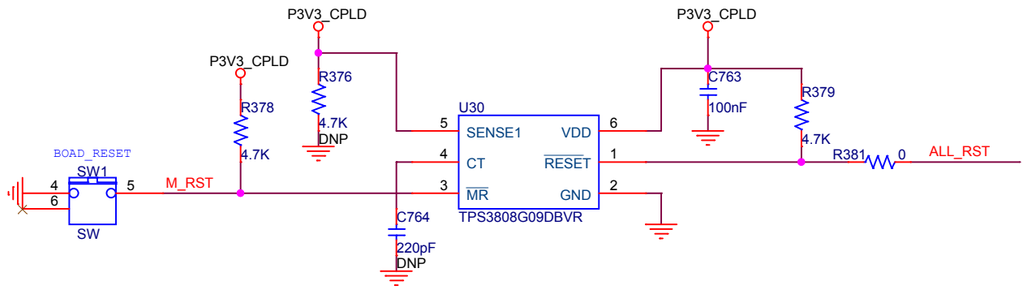


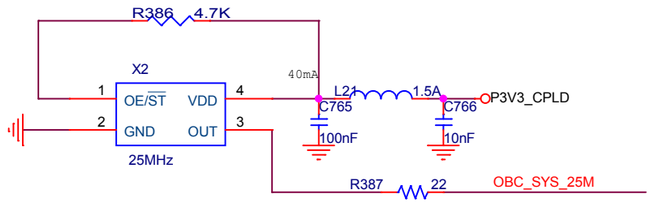








Note:RESET Time Fix 20 ms



拟制：	审核：	批准：
Title		
Size: A3	SCHEMATIC CODE: CPLD BNAK2/3	Rev: 1.00
	PROJECT NAME: ZYNQ_NvDIMM	
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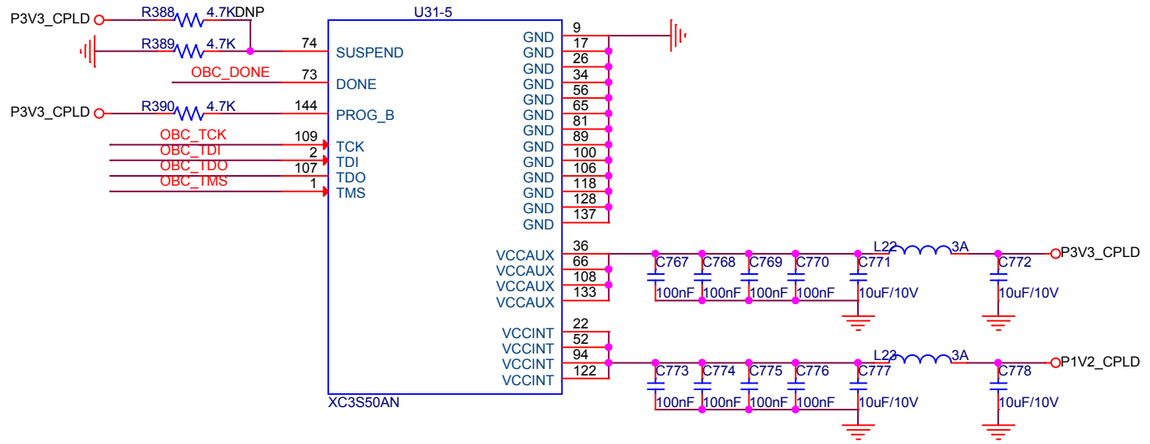

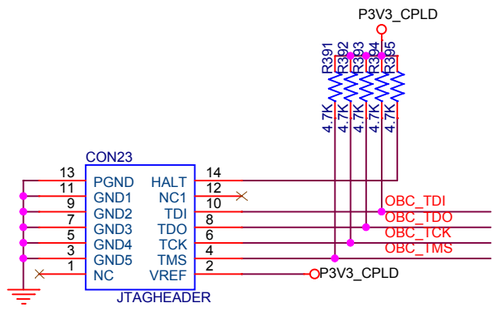

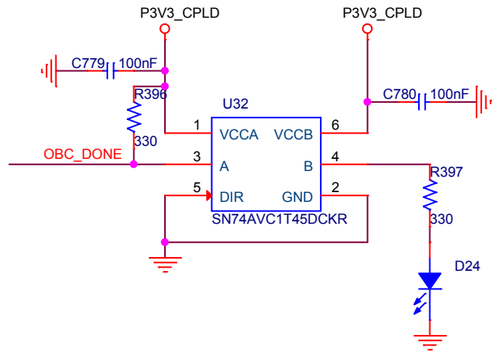

拟制：	审核：	批准：
Title		
Size: A3	SCHEMATIC CODE: CPLD POWER	Rev: 1.00
	PROJECT NAME: ZYNQ_NvDIMM	
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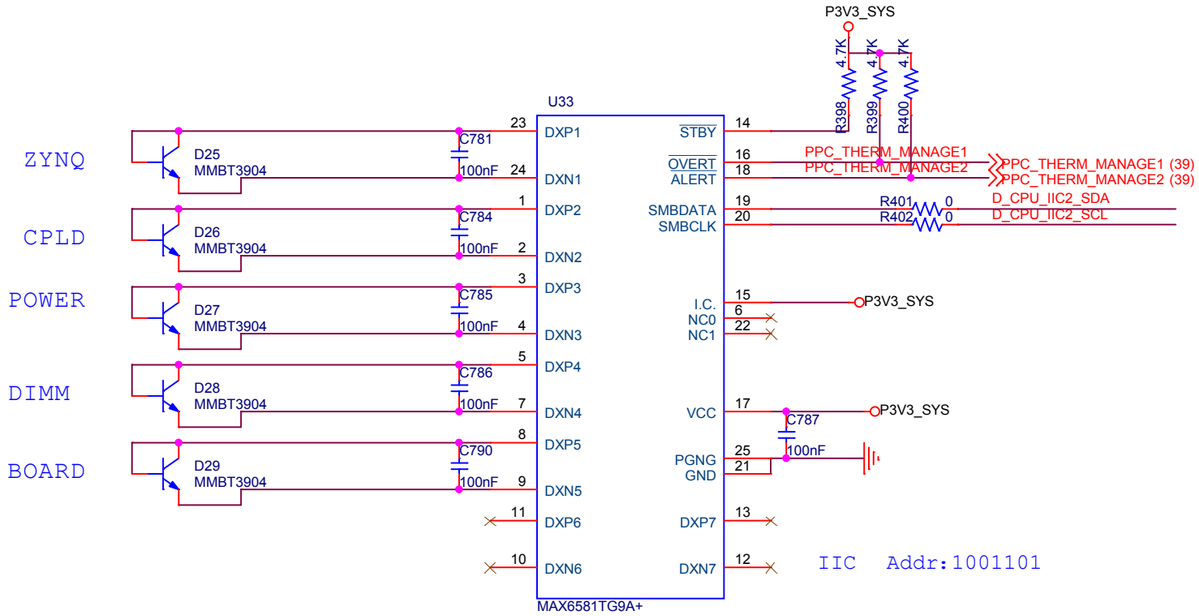

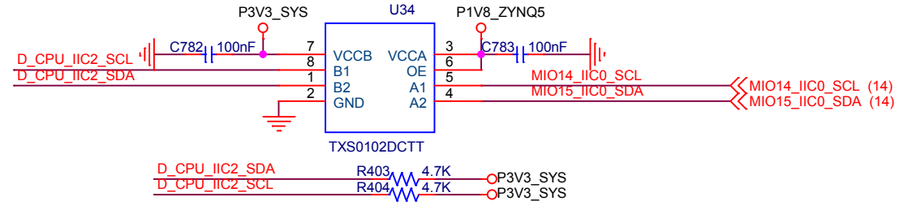

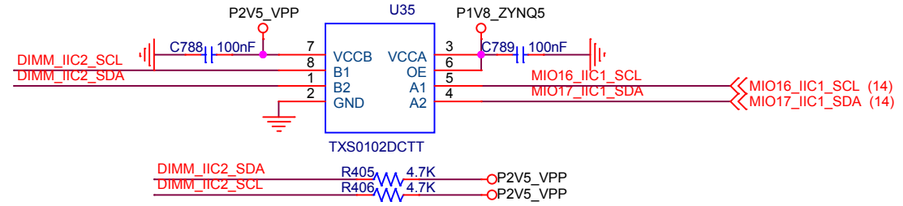

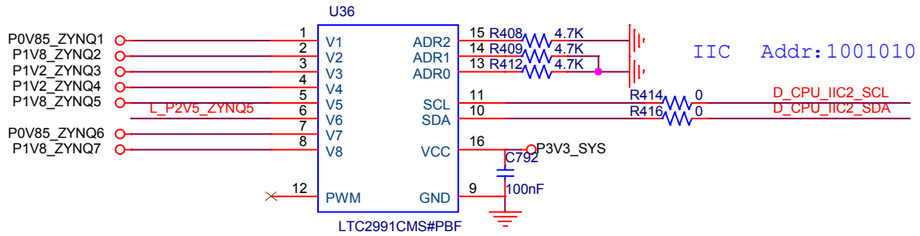

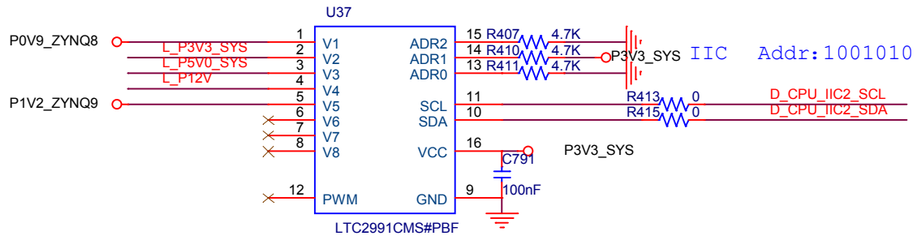

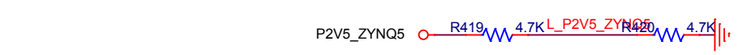

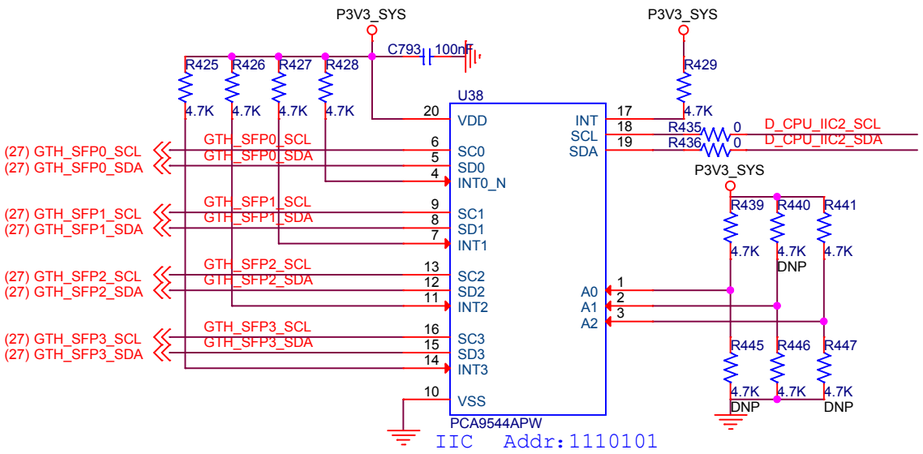

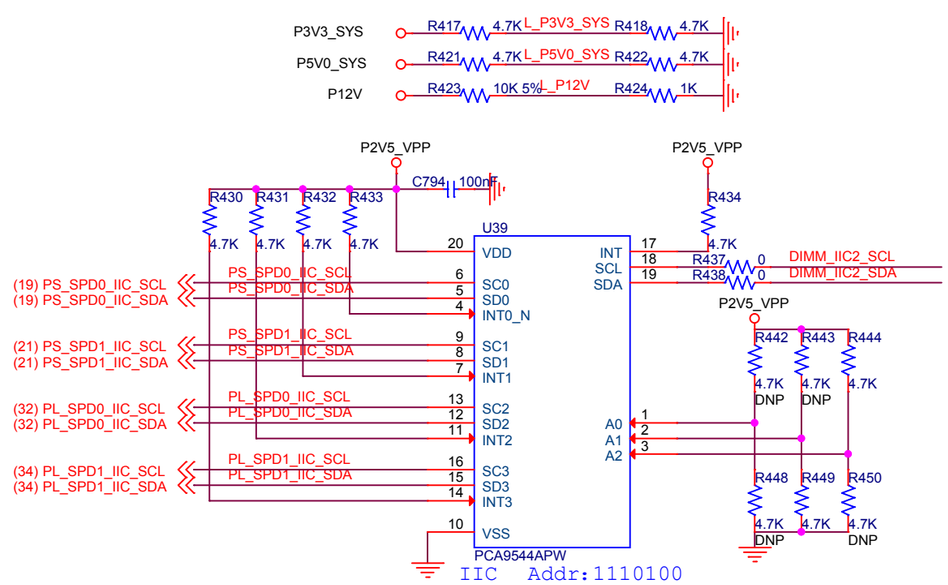

拟制：	审核：	批准：
Title		
Size: A3	SCHEMATIC CODE: Temp&&Voltage Monitor	Rev: 1.00
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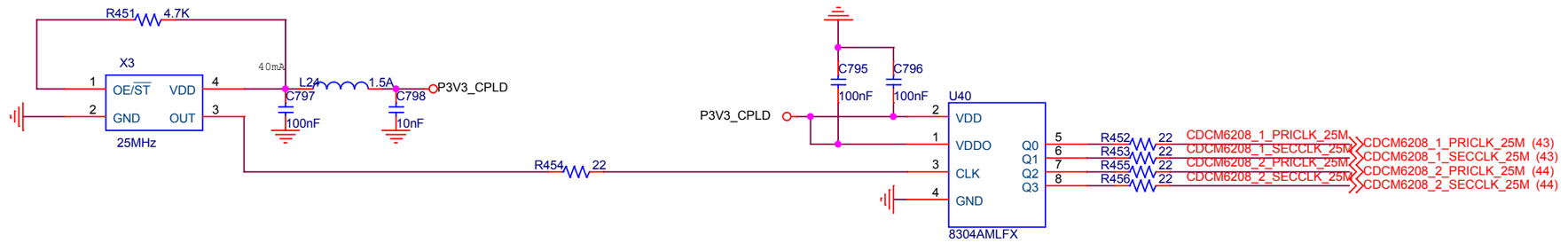

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拟制：	审核：	批准：

Title

Size	SCHEMATIC CODE	CLOCK1	Rev
A3	PROJECT NAME	ZYNQ_NvDIMM	1.00

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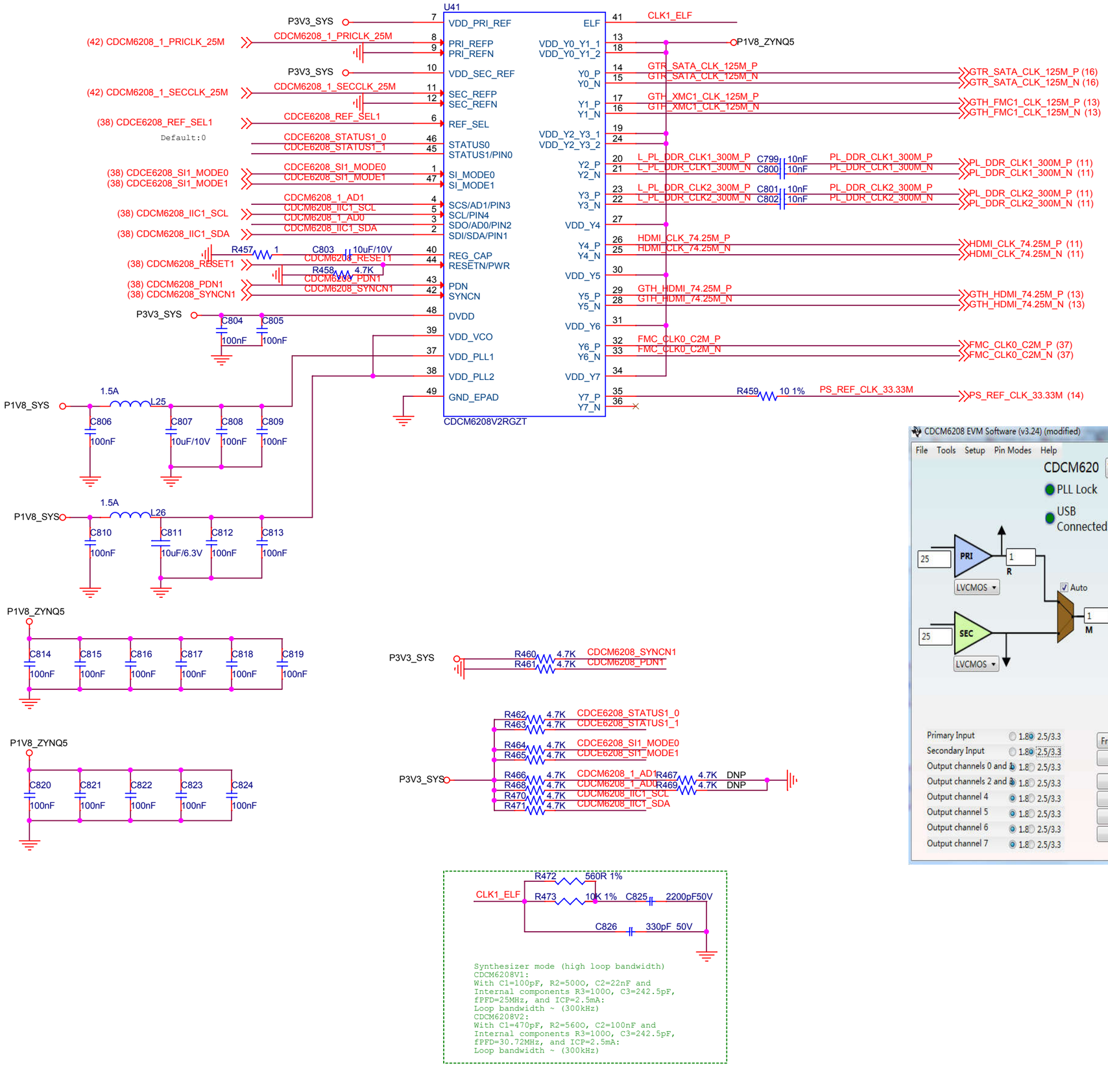

拟制：	审核：	批准：
Title		
Size A3	SCHEMATIC CODE CLOCK2	Rev 1.00
	PROJECT NAME ZYNQ_NvDIMM	
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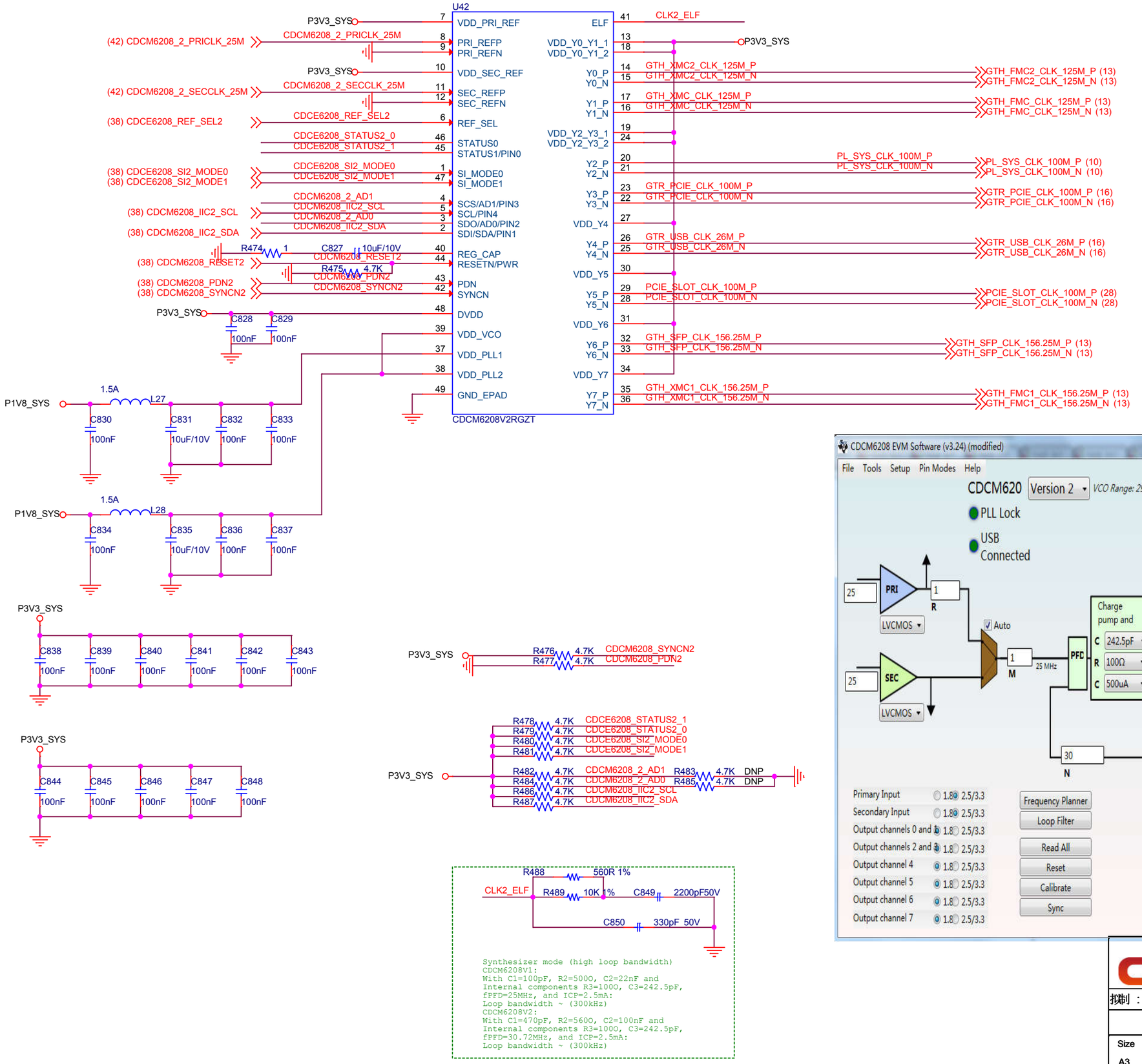

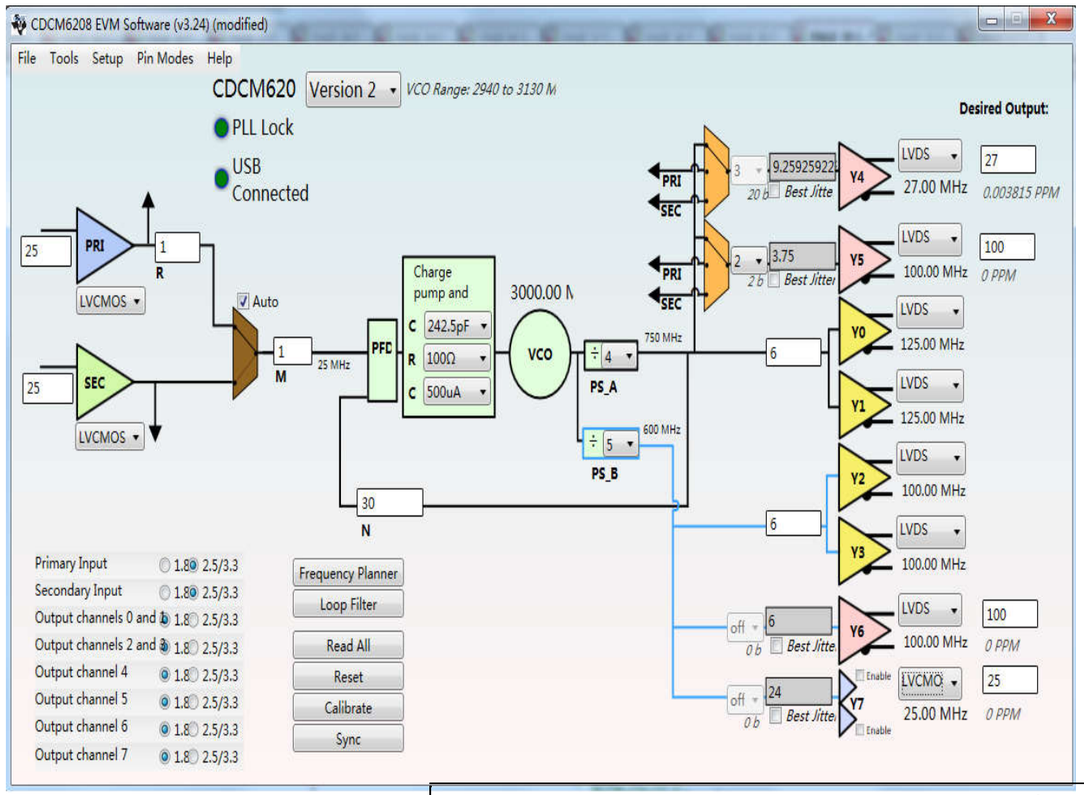

中电海康集团有限公司

拟制：	审核：	批准：

Title

Size	SCHEMATIC CODE	CLOCK3	Rev
A3	PROJECT NAME	ZYNQ_NvDIMM	1.00

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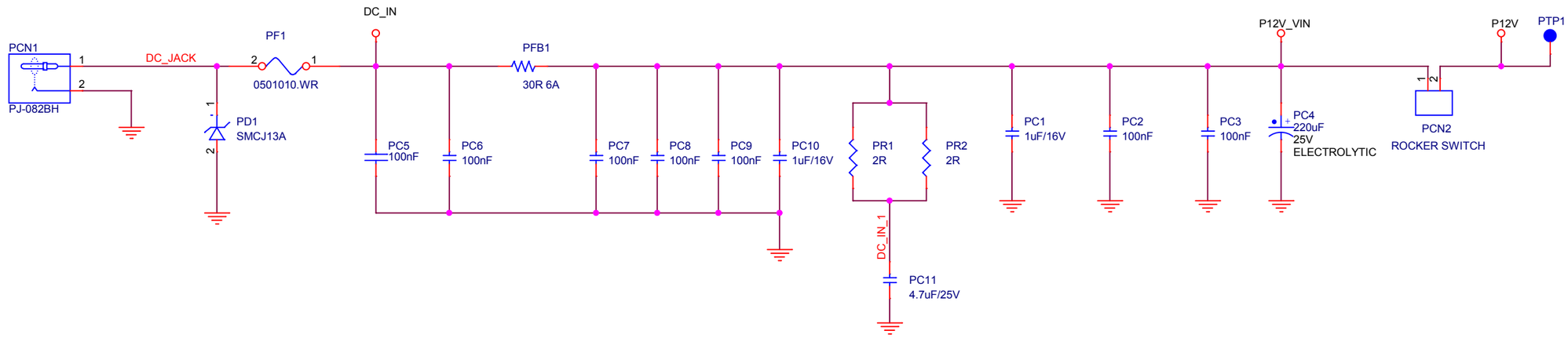

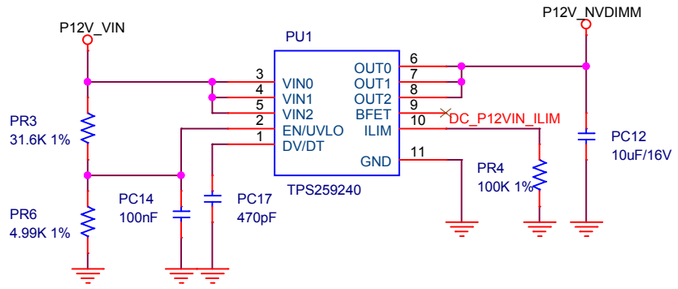

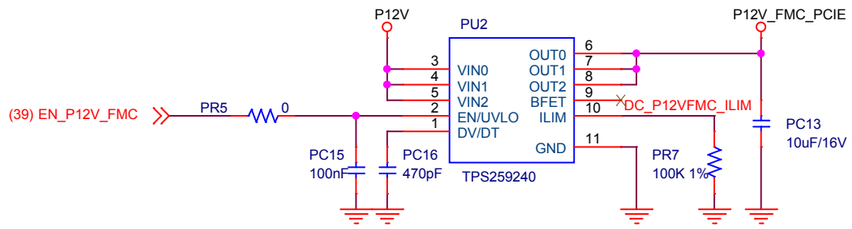

拟制：	审核：	批准：
Title		
Size A3	SCHEMATIC CODE DCIN	Rev 1.00
	PROJECT NAME ZYNQ_NvDIMM	
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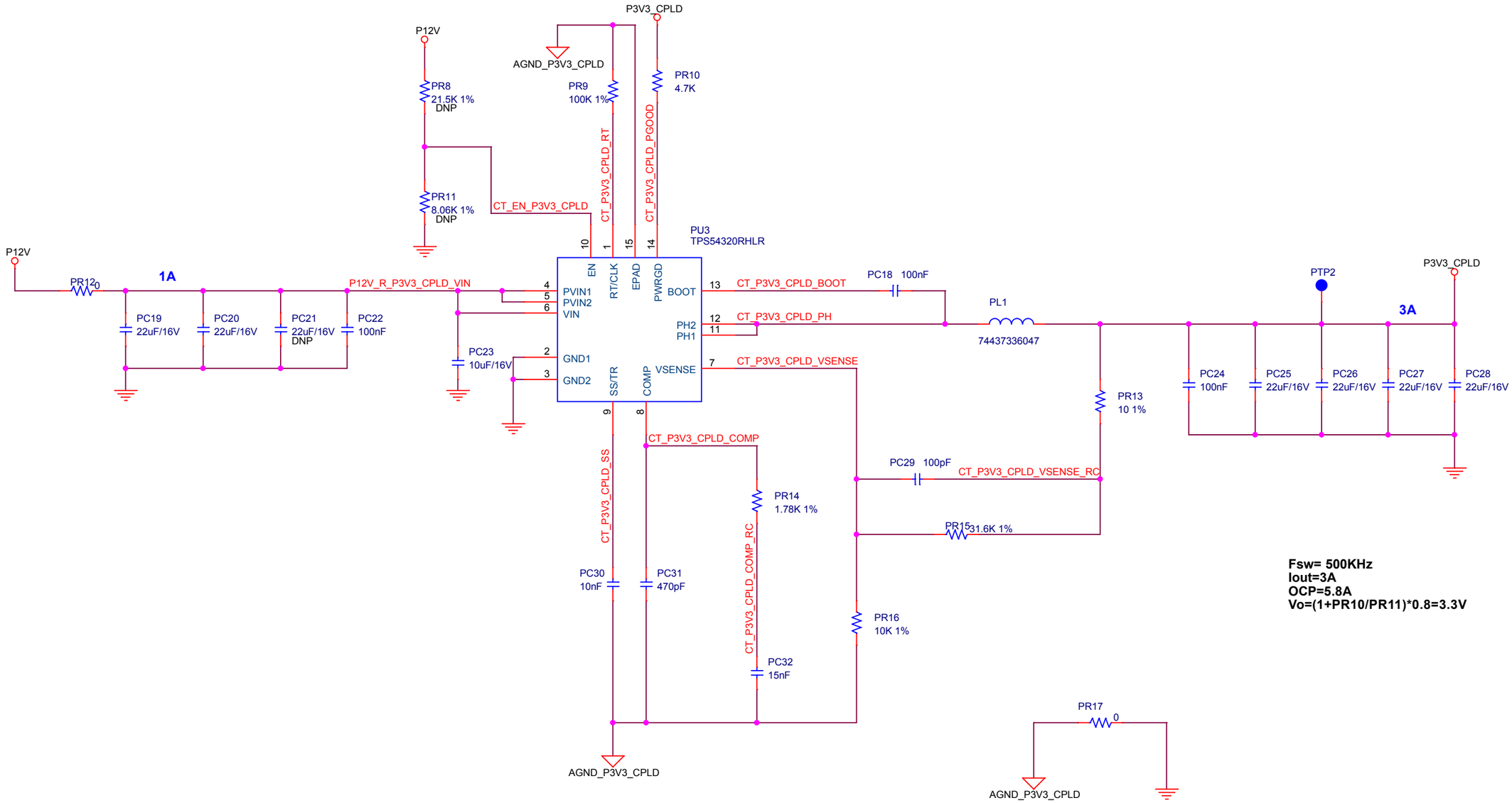

中电海康集团有限公司		
拟制：	审核：	批准：
Title		
Size: A3	SCHEMATIC CODE: P3V3_CPLD	Rev: 1.00
	PROJECT NAME: ZYNQ_NvDIMM	
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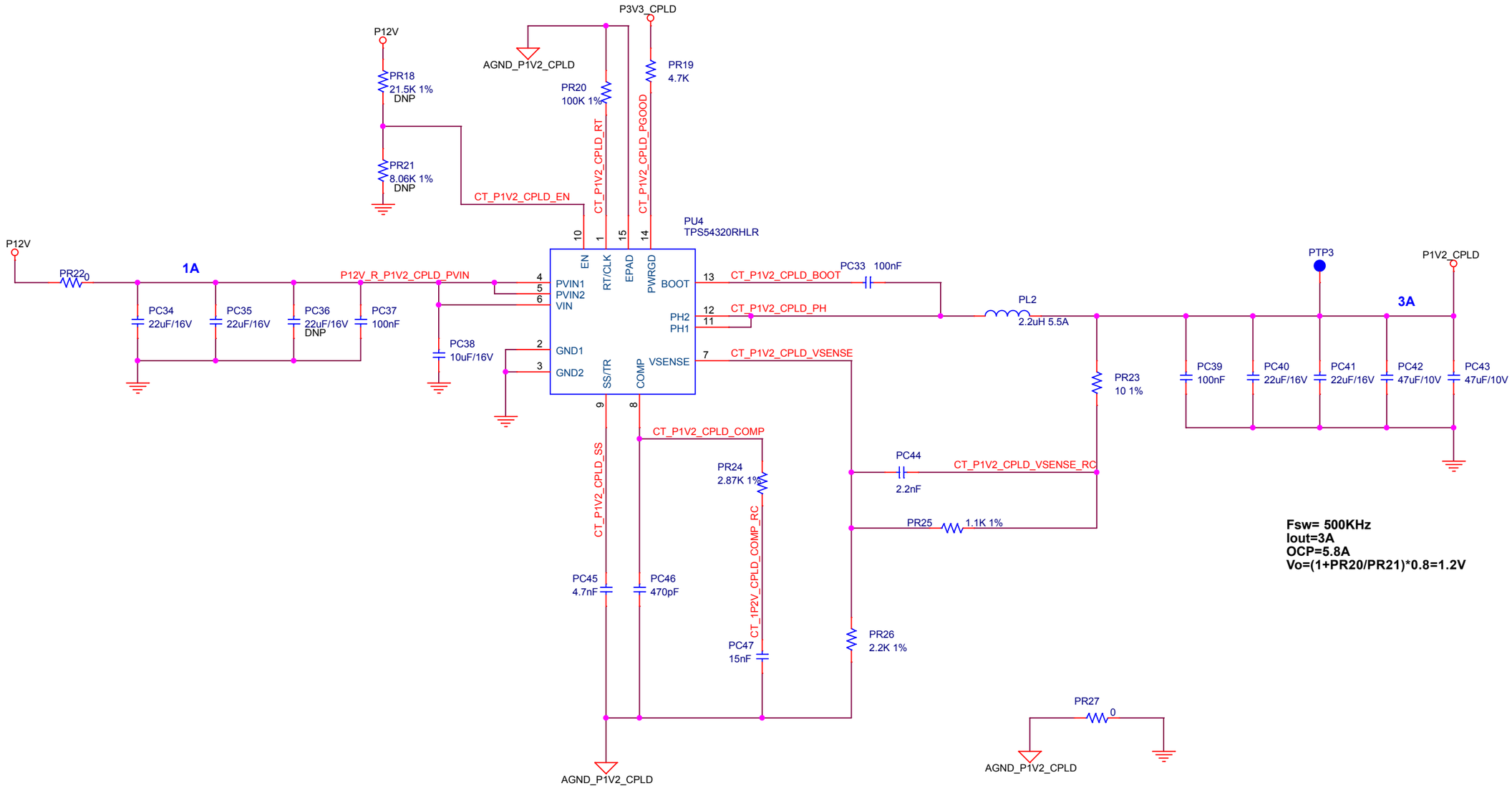

中电海康集团有限公司		
拟制：	审核：	批准：
Title		
Size A3	SCHEMATIC CODE P1V2_CPLD	Rev 1.00
	PROJECT NAME ZYNQ_NvDIMM	
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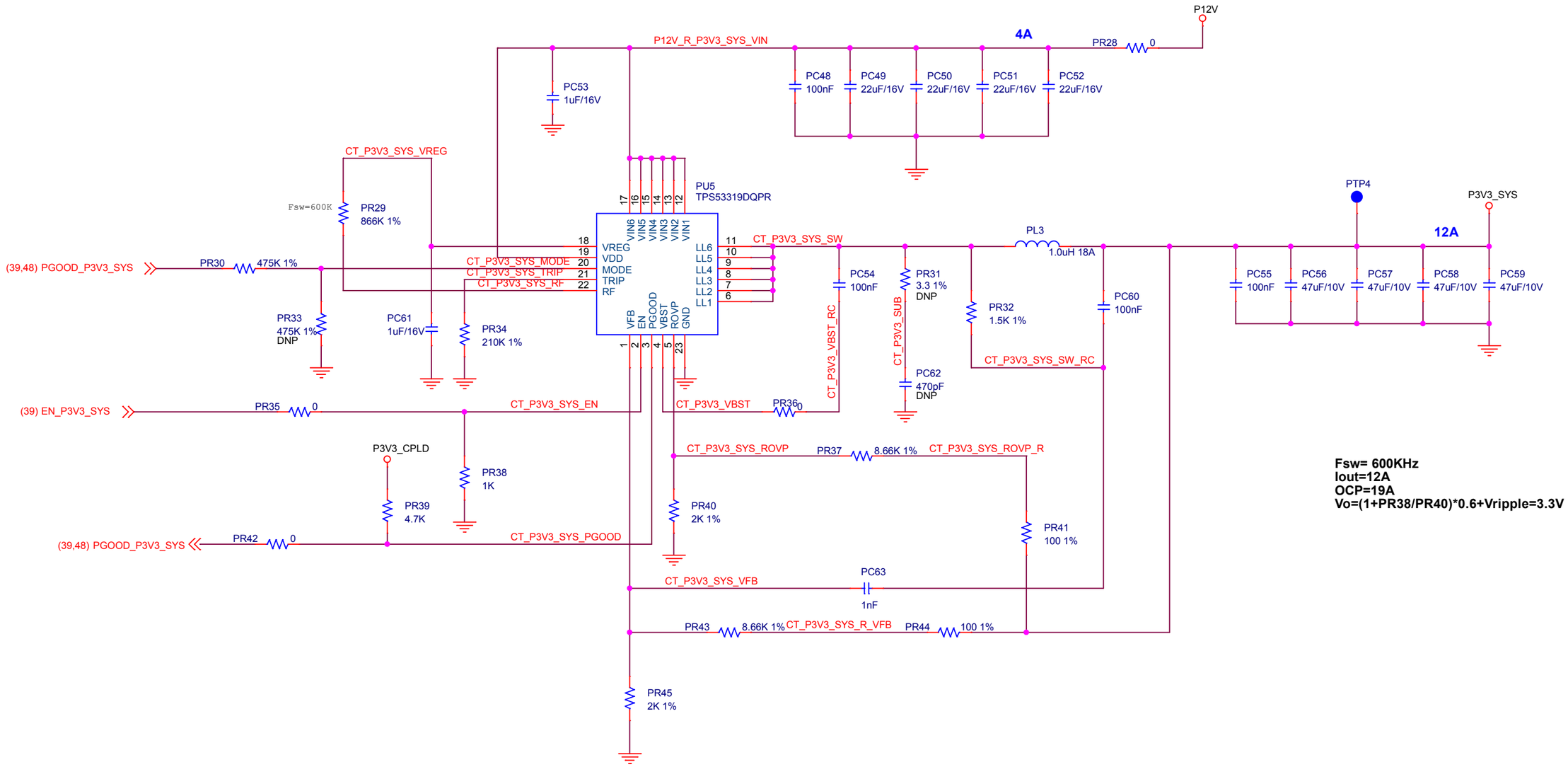

中电海康集团有限公司		
拟制：	审核：	批准：
Title		
Size: A3	SCHEMATIC CODE: P3V3_SYS	Rev: 1.00
	PROJECT NAME: ZYNQ_NvDIMM	
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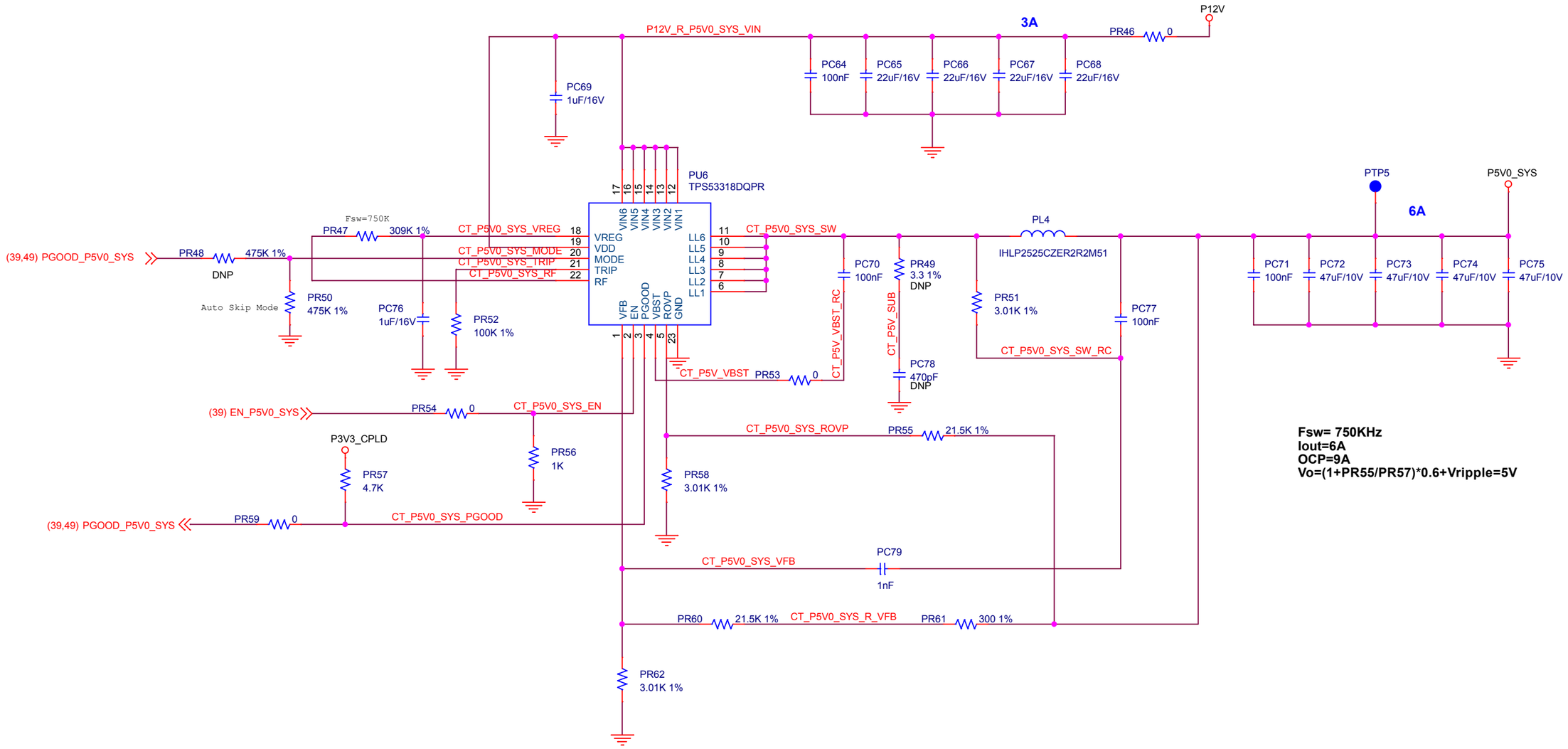

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拟制：	审核：	批准：

Title

Size A3	SCHEMATIC CODE P5V0_SYS	Rev 1.00
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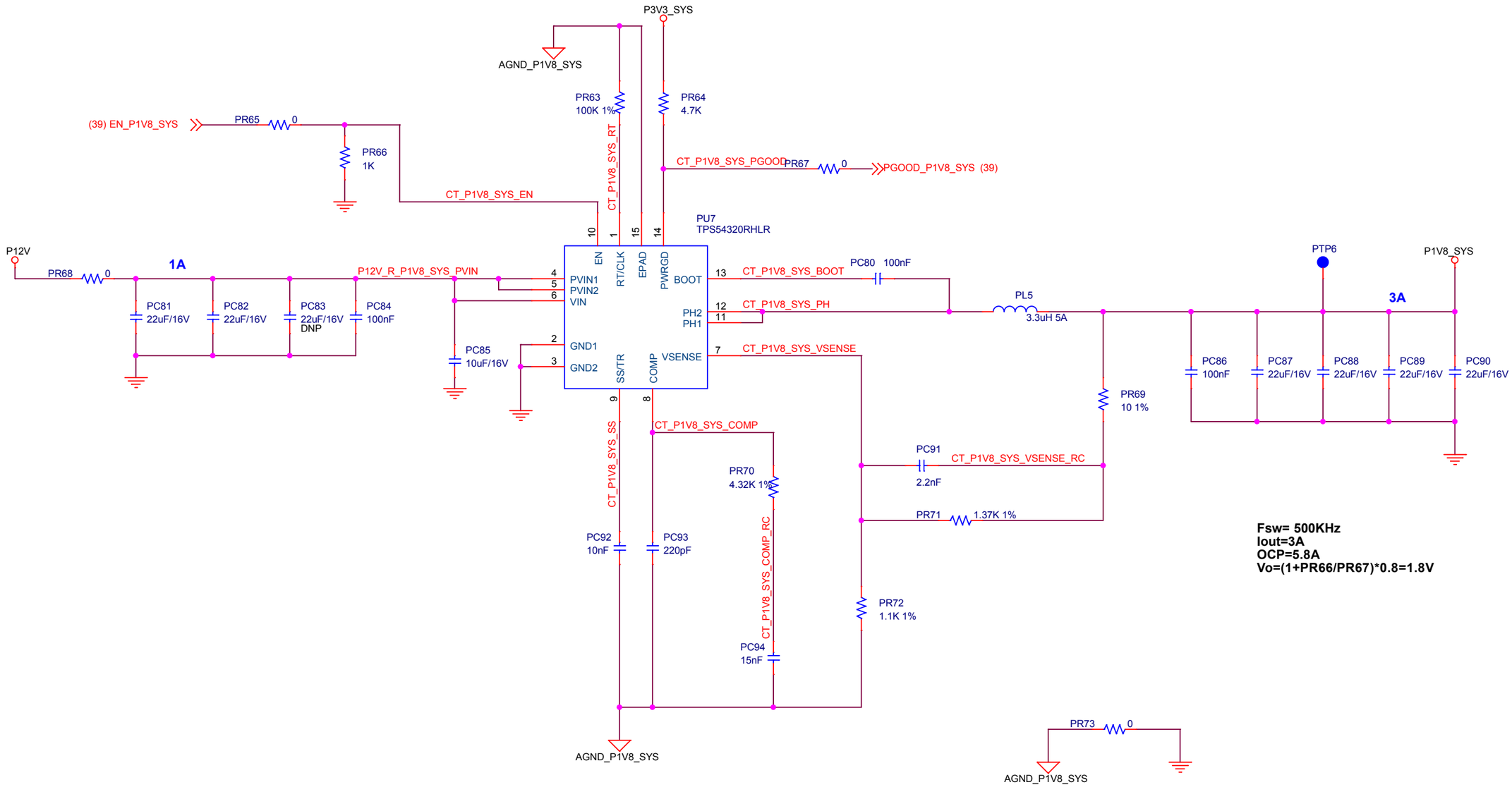

Fsw= 500KHz
Iout=3A
OCP=5.8A
Vo=(1+PR66/PR67)*0.8=1.8V

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拟制：	审核：	批准：

Title

Size: A3	SCHEMATIC CODE: P1V8_SYS	Rev: 1.00
	PROJECT NAME: ZYNQ_NvDIMM	
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(51) CT_P1V8_ZYNQ1_DIFFO
PR74 49.9 1%
PR75 10K 1%
CT_P1V8_ZYNQ1_FB1 (51)
PC96 1nF
PR77 280 1%
CT_P1V8_ZYNQ1_COMP1_RC1
PC102 100pF
CT_P1V8_ZYNQ1_COMP1 (51)
PR78 24K 1%
PC103 1.5nF
PR79 10K 1%
CT_P1V8_ZYNQ1_COMP1_RC2
AGND_P0V85_ZYNQ1

P0V85_ZYNQ1
PR81 49.9 1%
PR82 49.9 1%
CT_VSENSE_P0V85_ZYNQ1_P (51)
CT_VSENSE_P0V85_ZYNQ1_N (51)

P12V
PL7
65nH 30A
P12V_L_P0V85_ZYNQ1_VIN
PC106 22uF/16V
PC107 100nF
PC108 270uF/16V

(51) CT_P1V8_ZYNQ1_FLT
(51) CT_P1V8_ZYNQ1_FB1
(51) CT_P1V8_ZYNQ1_COMP1
(51) CT_VSENSE_P0V85_ZYNQ1_P
(51) CT_VSENSE_P0V85_ZYNQ1_N
(51) CT_P1V8_ZYNQ1_DIFFO
PC116 100nF
AGND_P0V85_ZYNQ1
CT_P1V8_ZYNQ1_CS1_N (51)
CT_P1V8_ZYNQ1_CS1_P (51)
P0V85_ZYNQ1_TSNS1 (51)
PR90 40.2K 1%
CT_P0V85_ZYNQ1_RT
AGND_P0V85_ZYNQ1
PC119 470pF
AGND_P0V85_ZYNQ1
P3V3_SYS
PR92 4.7K

PU9
TPS40428RHAR
41 PAD
40 RT
39 DIFFO1
38 GSNS1
37 VSNS1
36 COMP1
35 FB1
34 FLT1
33 CS1N
32 CS1P
31 TSNS1
1 SYNC
2 PHSET
3 CNTL1
4 CNTL2
5 SMBALERT
6 PMBDATA
7 PMBCLK
8 AGND
9 AVSDATA
10 AVSCLK
30 ISH1
29 PG1
28 PWM1
27 PGND
26 BP3
25 BP5
24 VDD
23 PWM2
22 PG2
21 ISH2
11 ADDR1
12 ADDR0
13 GSNS2
14 VSNS2
15 COMP2
16 FB2
17 FLT2
18 CS2N
19 CS2P
20 TSNS2

CT_P1V8_ZYNQ1_ISH (51)
CT_P0V85_ZYNQ1_PG1
PR93 0
PGOOD_P0V85_ZYNQ1 (39)
TP16
CT_P1V8_ZYNQ1_PWM1 (51)
CT_P1V8_ZYNQ1_BP5 (51)
CT_P0V85_ZYNQ1_BP3
PC126 1uF/16V
PC127 1uF/16V
AGND_P0V85_ZYNQ1
CT_P0V85_ZYNQ1_VDD
PC128 1uF/16V
P12V_L_P0V85_ZYNQ1_VIN
PR97 0
TP17
CT_P1V8_ZYNQ1_PWM2 (51)
PR98 0
CT_P1V8_ZYNQ1_ISH (51)
P0V85_ZYNQ1_TSNS2 (51)
PC137 470pF
AGND_P0V85_ZYNQ1

(39) EN_P0V85_ZYNQ1
PR91 0
PR95 1K
(51) P1V8_ZYNQ1_SMBALERT
(51) P1V8_ZYNQ1_PMBDATA
(51) P1V8_ZYNQ1_PMBCLK
AGND_P0V85_ZYNQ1
CT_P0V85_ZYNQ1_ADDR1
CT_P0V85_ZYNQ1_ADDR0
PR101 16.2K 1%
PR102 25.5K 1%
AGND_P0V85_ZYNQ1
(51) CT_P1V8_ZYNQ1_COMP1
(51) CT_P1V8_ZYNQ1_BP5
(51) CT_P1V8_ZYNQ1_FLT
(51) CT_P1V8_ZYNQ1_CS2_N
(51) CT_P1V8_ZYNQ1_CS2_P
PC141 100nF
AGND_P0V85_ZYNQ1
PR108 0
AGND_P0V85_ZYNQ1

P3V3_SYS
PR109 4.7K
PR110 4.7K
PR111 4.7K
(51) P1V8_ZYNQ1_PMBDATA
(51) P1V8_ZYNQ1_PMBCLK
(51) P1V8_ZYNQ1_SMBALERT

CT_P0V85_ZYNQ1_BST1_RC
PC95 100nF
PR76 0
CT_P0V85_ZYNQ1_BST1
CT_ZYNQ1_BST1_R
P12V_L_P0V85_ZYNQ1_VIN
PC97 3.3nF
PC98 22uF/16V
PC99 22uF/16V
PC100 22uF/16V
PC101 22uF/16V
P5V0_SYS
PR80 1
PC104 1uF/16V

PU8
CSD95378BQ5M
9 BOOT
8 BOOT_R
5 VDD
3 ENABLE
4 PGND1
13 PGND2
7 VIN
6 VSW
10 FCCM
11 TAO/FAULT
12 PWM
2 REFIN
1 IOUT

P0V85_ZYNQ1
PTP7
CT_P0V85_ZYNQ1_SW1
PL6
744308033
25A
PR83 1
PC105 1nF
P5V0_SYS
DNP
PR84 0
PR85 0
PC109 100uF/6.3V
PC110 100uF/6.3V
PC111 100uF/6.3V
PC112 100uF/6.3V
PC113 100uF/6.3V
PC114 100uF/6.3V
PC115 100uF/6.3V
(51) P0V85_ZYNQ1_TSNS1
(51) CT_P1V8_ZYNQT_PWM1
(51) CT_P1V8_ZYNQ1_CS1_N
(51) CT_P1V8_ZYNQ1_CS1_P
PR86 0
PR87 0
PR88 0
CT_ZYNQ1_RFEIN1
CT_ZYNQ1_IOUT1
PR89 121K 1%
PC117 470pF
PC118 100nF

Fsw= 500KHz
Iout=45A
Vo=(1+PR79/PR81)*0.6=0.85V

CT_P0V85_ZYNQ1_BST2_RC
PC120 100nF
PR94 0
CT_P0V85_ZYNQ1_BST2
CT_ZYNQ1_BST2_R
P12V_L_P0V85_ZYNQ1_VIN
PC121 3.3nF
PC122 22uF/16V
PC123 22uF/16V
PC124 22uF/16V
PC125 22uF/16V
P5V0_SYS
PR96 1
PC129 1uF/16V

PU10
CSD95378BQ5M
9 BOOT
8 BOOT_R
5 VDD
3 ENABLE
4 PGND1
13 PGND2
7 VIN
6 VSW
10 FCCM
11 TAO/FAULT
12 PWM
2 REFIN
1 IOUT

P0V85_ZYNQ1
CT_P0V85_ZYNQ1_SW2
PL8
744308033
25A
PR99 1
PC130 1nF
P5V0_SYS
DNP
PR100 0
PR103 0
PC131 100uF/6.3V
PC132 100uF/6.3V
PC133 100uF/6.3V
PC134 100uF/6.3V
PC135 100uF/6.3V
PC136 100uF/6.3V
PC138 100uF/6.3V
(51) P0V85_ZYNQ1_TSNS2
(51) CT_P1V8_ZYNQT_PWM2
(51) CT_P1V8_ZYNQ1_CS2_N
(51) CT_P1V8_ZYNQ1_CS2_P
PR104 0
PR105 0
PR106 0
CT_ZYNQ1_RFEIN2
CT_ZYNQ1_IOUT2
PR107 121K 1%
PC139 470pF
PC140 100nF

P3V3_SYS
PCN3
1 2
3 4
5 6
7 8
9 10
HEADER 2X5
(51) P1V8_ZYNQ1_PMBCLK
P1V8_ZYNQ1_SMBALERT (51)
P1V8_ZYNQ1_PMBDATA (51)

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Title		
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	PROJECT NAME: ZYNQ_NvDIMM	
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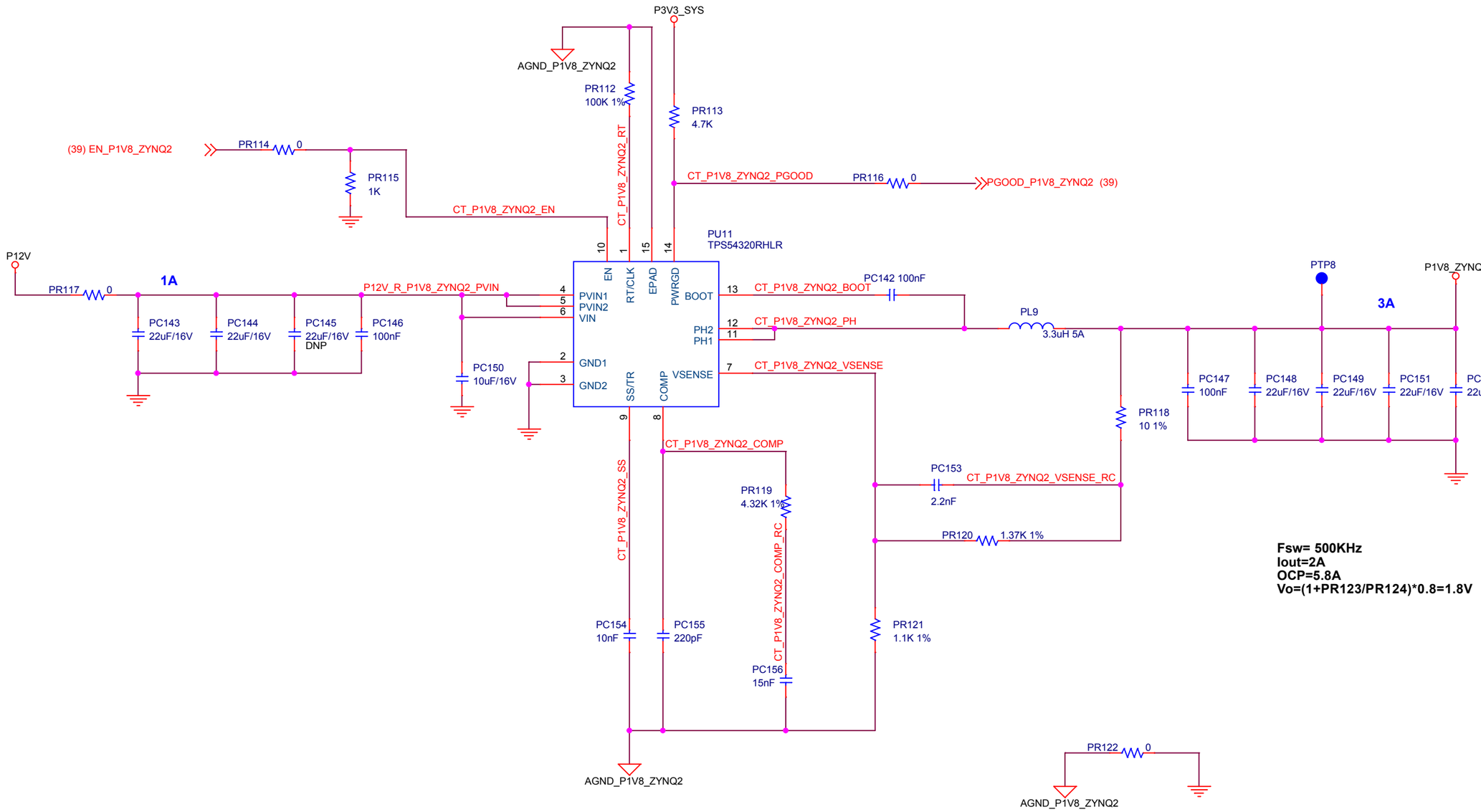

中电海康集团有限公司		
拟制：	审核：	批准：
Title		
Size: A3	SCHEMATIC CODE: P1V8_ZYNQ2	Rev: 1.00
	PROJECT NAME: ZYNQ_NvDIMM	
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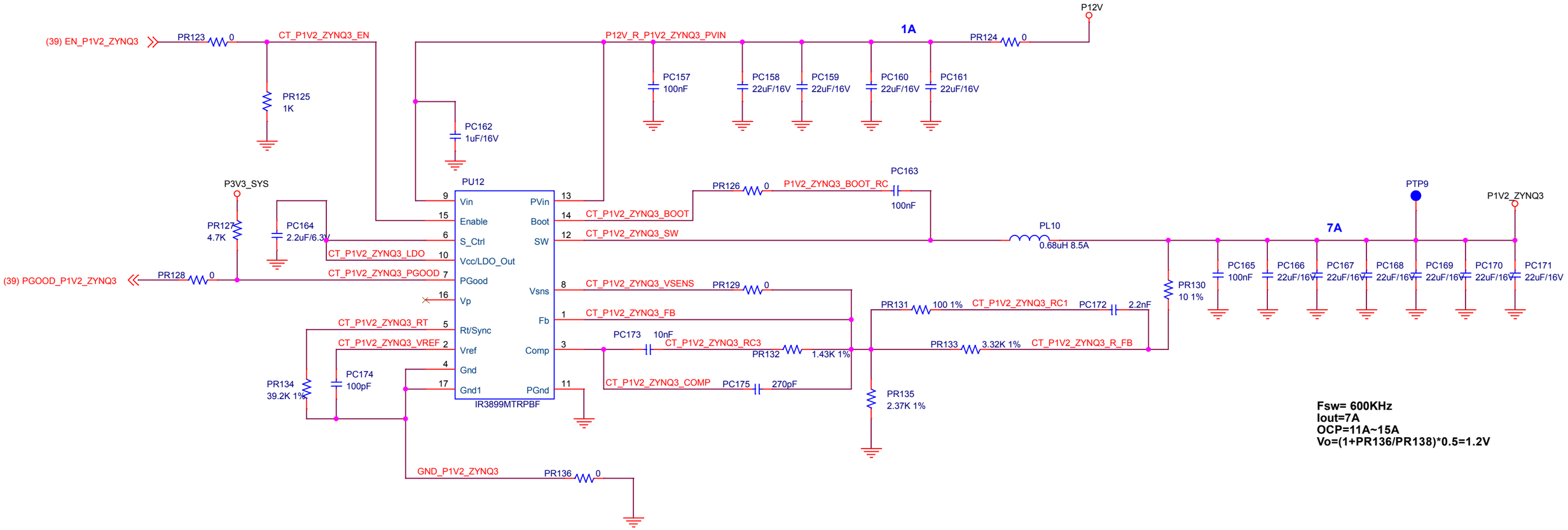

拟制：	审核：	批准：
Title		
Size: A3	SCHEMATIC CODE: P1V2_ZYNQ3	Rev: 1.00
	PROJECT NAME: ZYNQ_NvDIMM	
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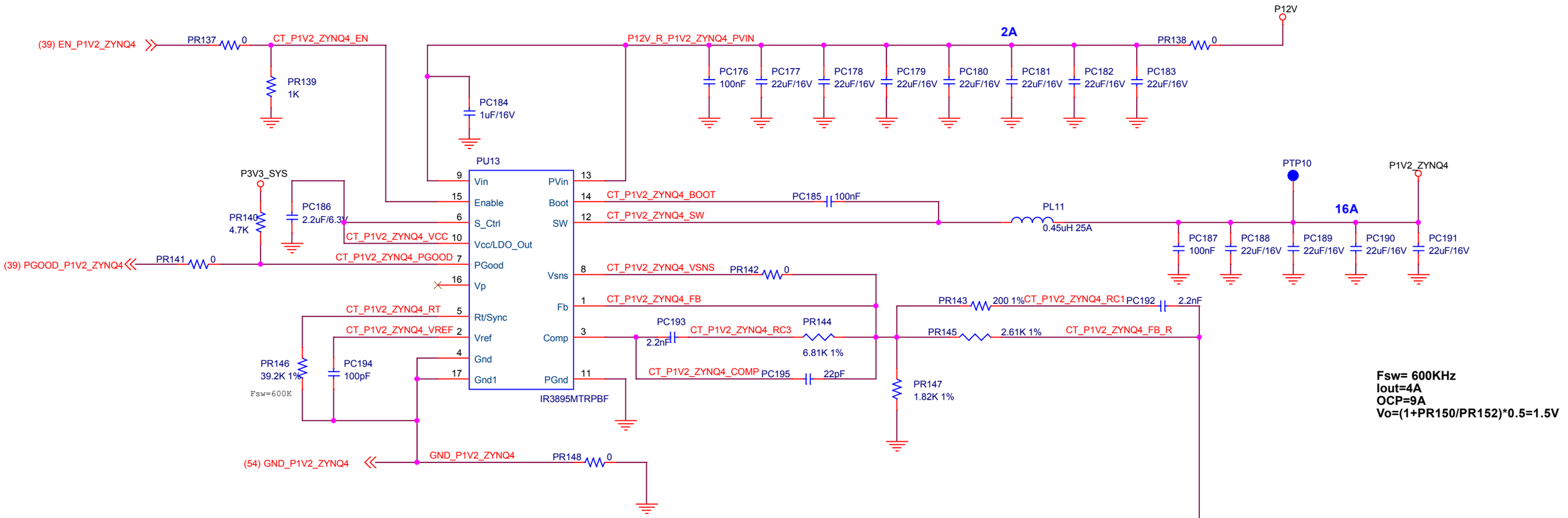

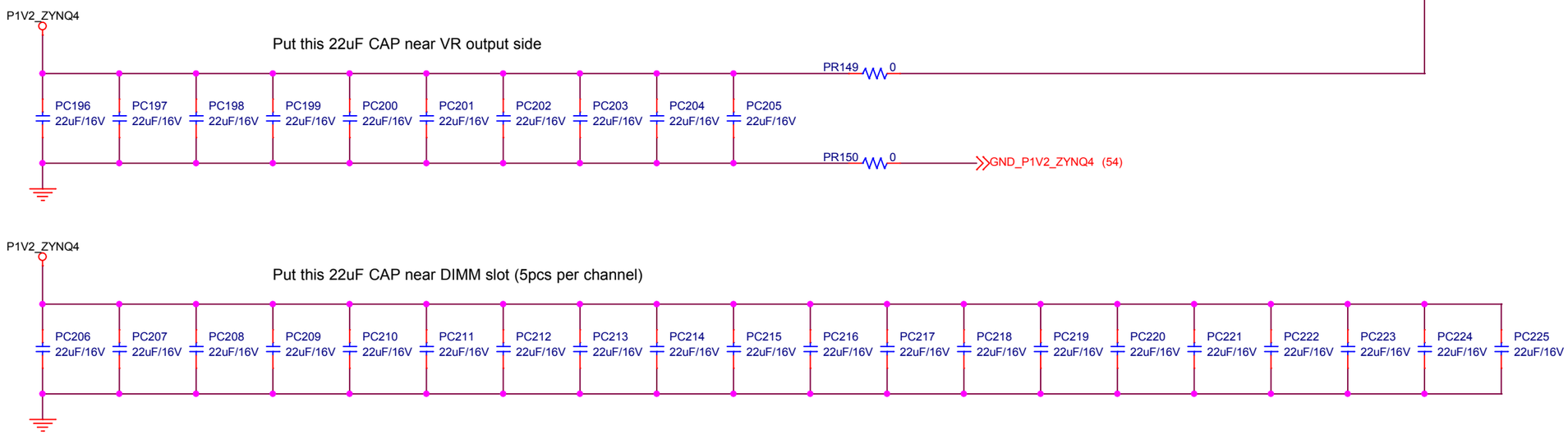

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拟制：	审核：	批准：
Title		
Size: A3	SCHEMATIC CODE: P1V2_ZYNQ4	Rev: 1.00
	PROJECT NAME: ZYNQ_NvDIMM	
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Title		
Size: A3	SCHEMATIC CODE: P2V5_ZYNQ5&P1V8_ZYNQ5	Rev: 1.00
	PROJECT NAME: ZYNQ_NvDIMM	
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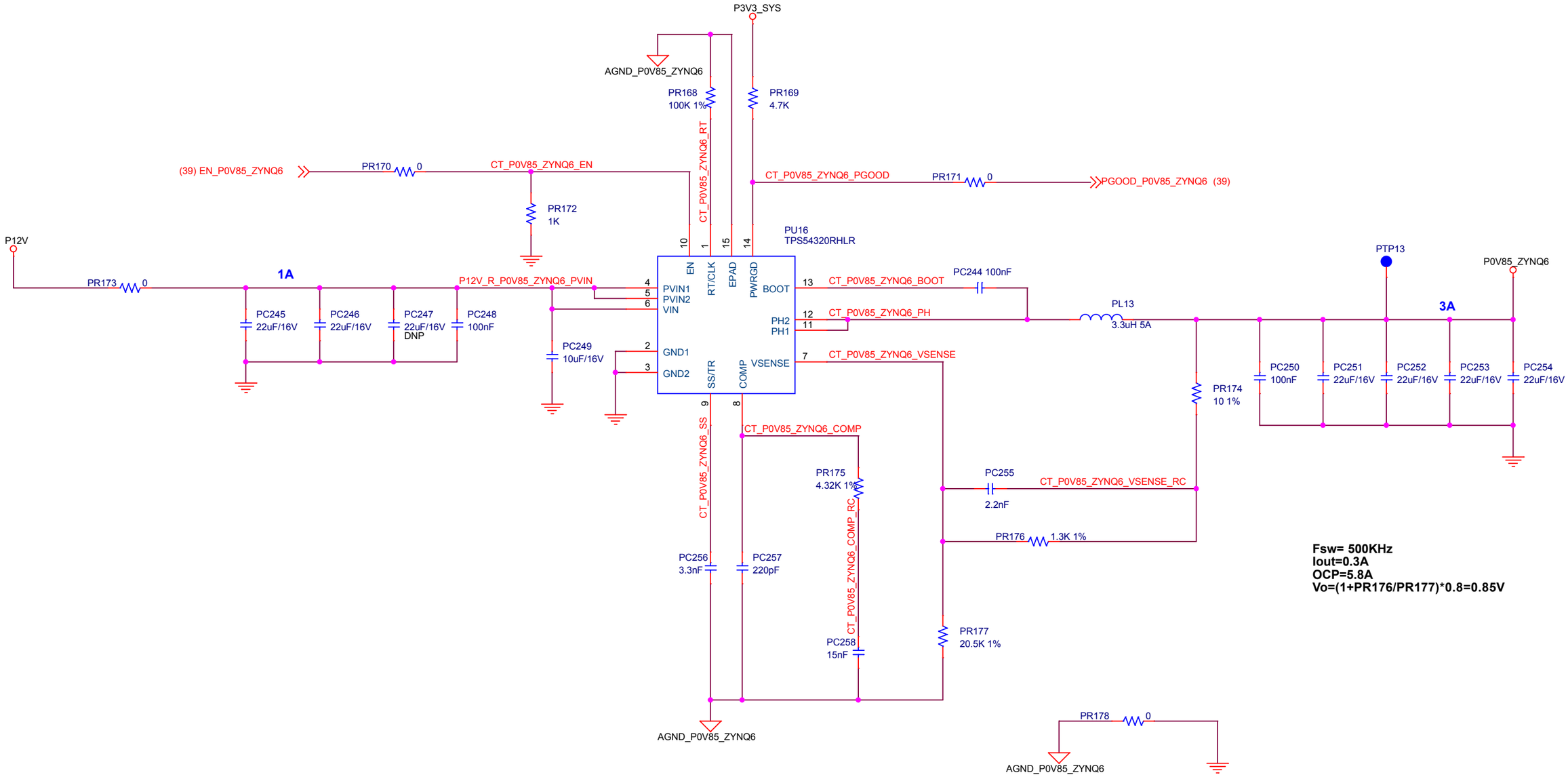

中电海康集团有限公司		
拟制：	审核：	批准：
Title		
Size: A3	SCHEMATIC CODE: P0V85_ZYNQ6	Rev: 1.00
	PROJECT NAME: ZYNQ_NvDIMM	
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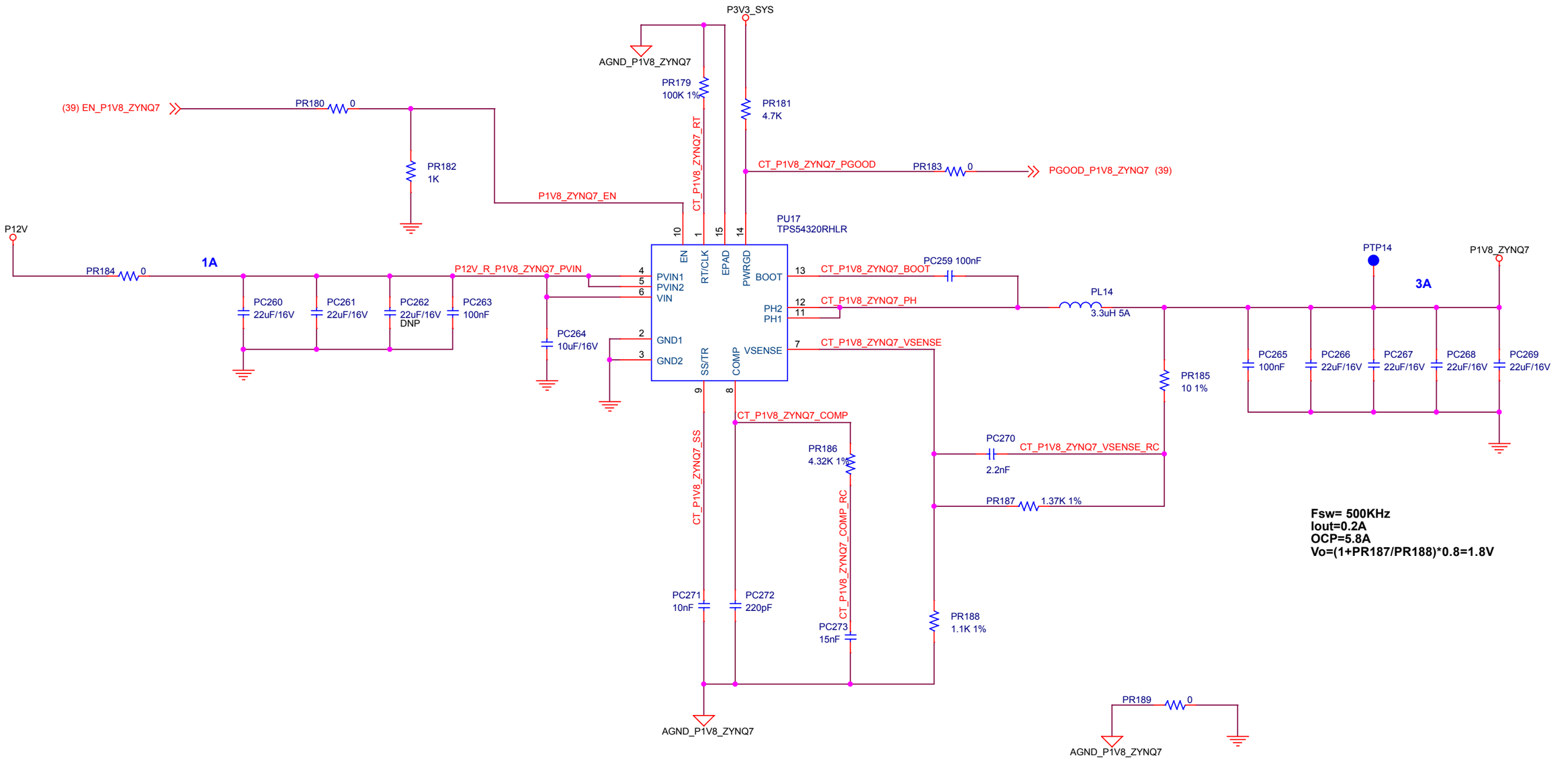

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拟制：	审核：	批准：

Title

Size	SCHEMATIC CODE	P1V8_ZYNQ7	Rev
A3	PROJECT NAME	ZYNQ_NvDIMM	1.00

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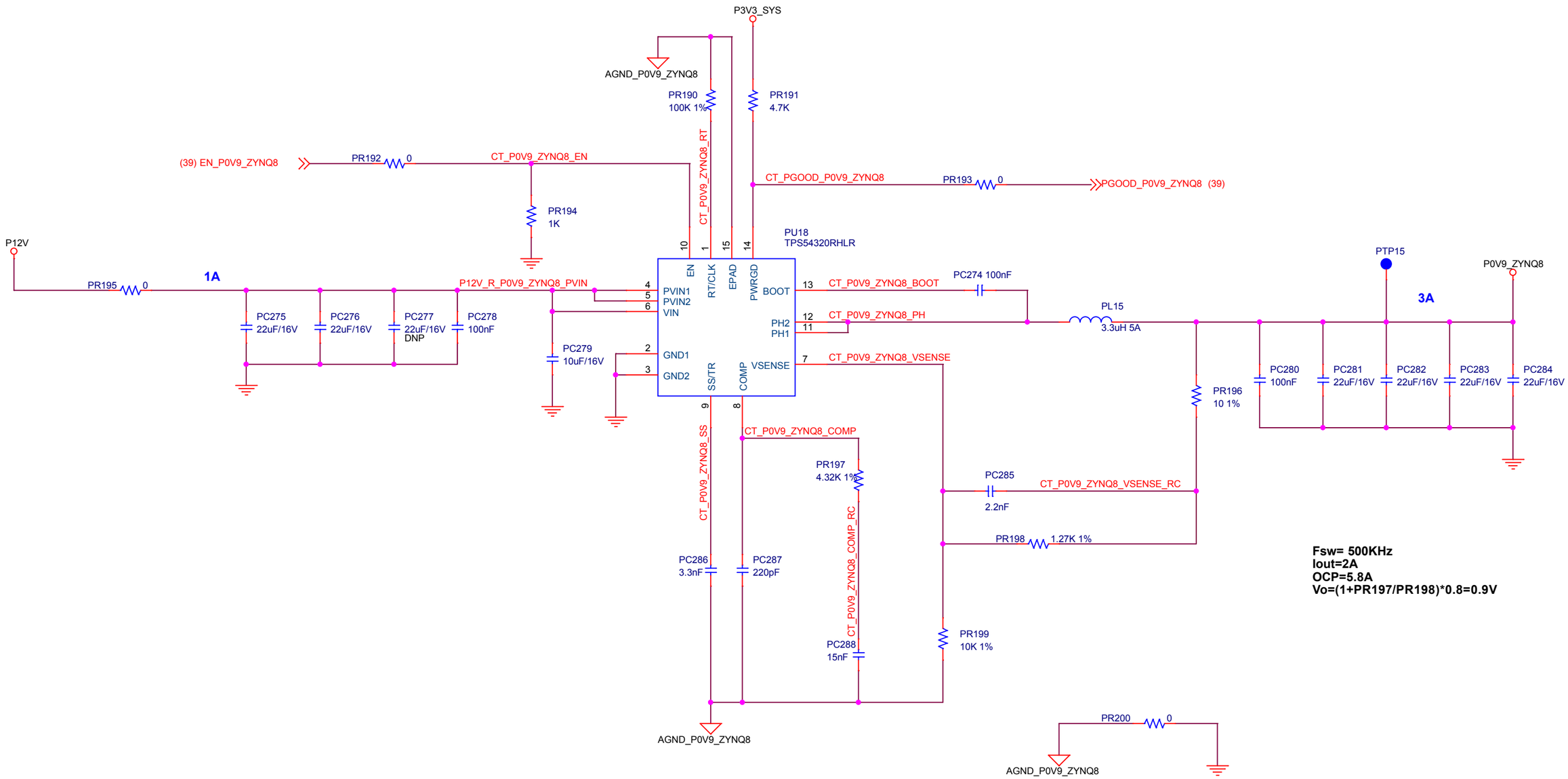

Fsw= 500KHz
Iout=2A
OCP=5.8A
Vo=(1+PR197/PR198)*0.8=0.9V

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拟制：	审核：	批准：

Title

Size: A3	SCHEMATIC CODE: P0V9_ZYNQ8	Rev: 1.00
	PROJECT NAME: ZYNQ_NvDIMM	
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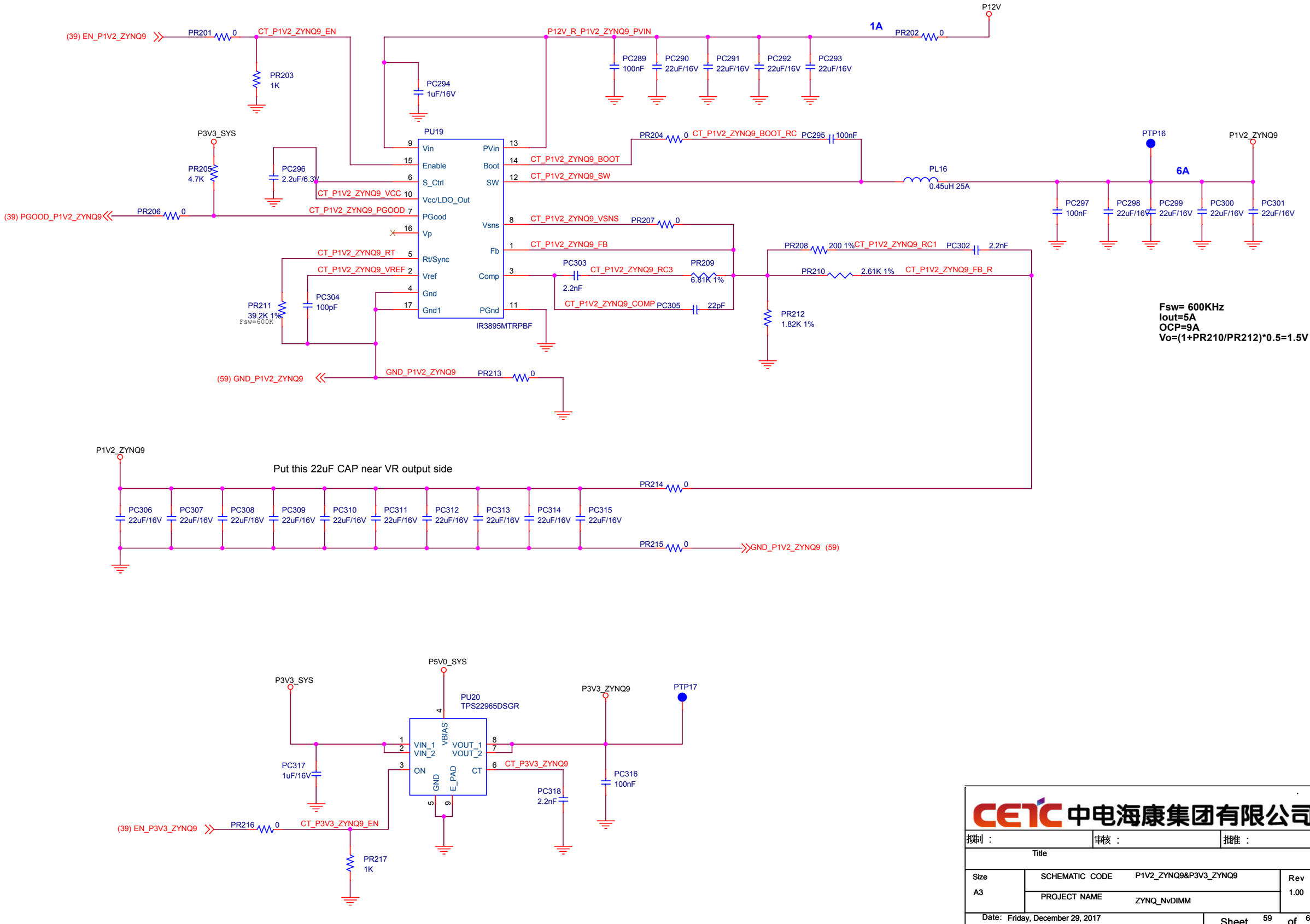

拟制：	审核：	批准：
Title		
Size: A3	SCHEMATIC CODE: P1V2_ZYNQ9&P3V3_ZYNQ9	Rev: 1.00
	PROJECT NAME: ZYNQ_NvDIMM	
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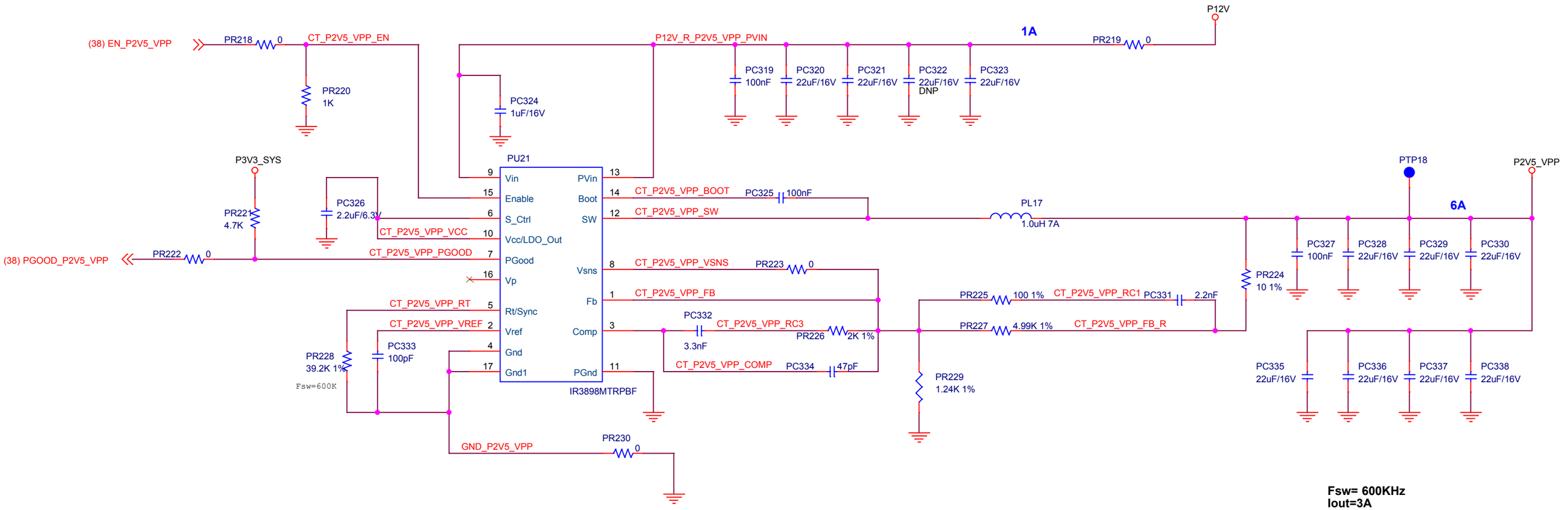

Fsw= 600KHz
Iout=3A
OCP=9A
Vo=(1+PR223/PR224)*0.5=2.5V

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拟制：	审核：	批准：

Title

Size	SCHEMATIC CODE	P2V5_VPP	Rev
A3	PROJECT NAME	ZYNQ_NvDIMM	1.00

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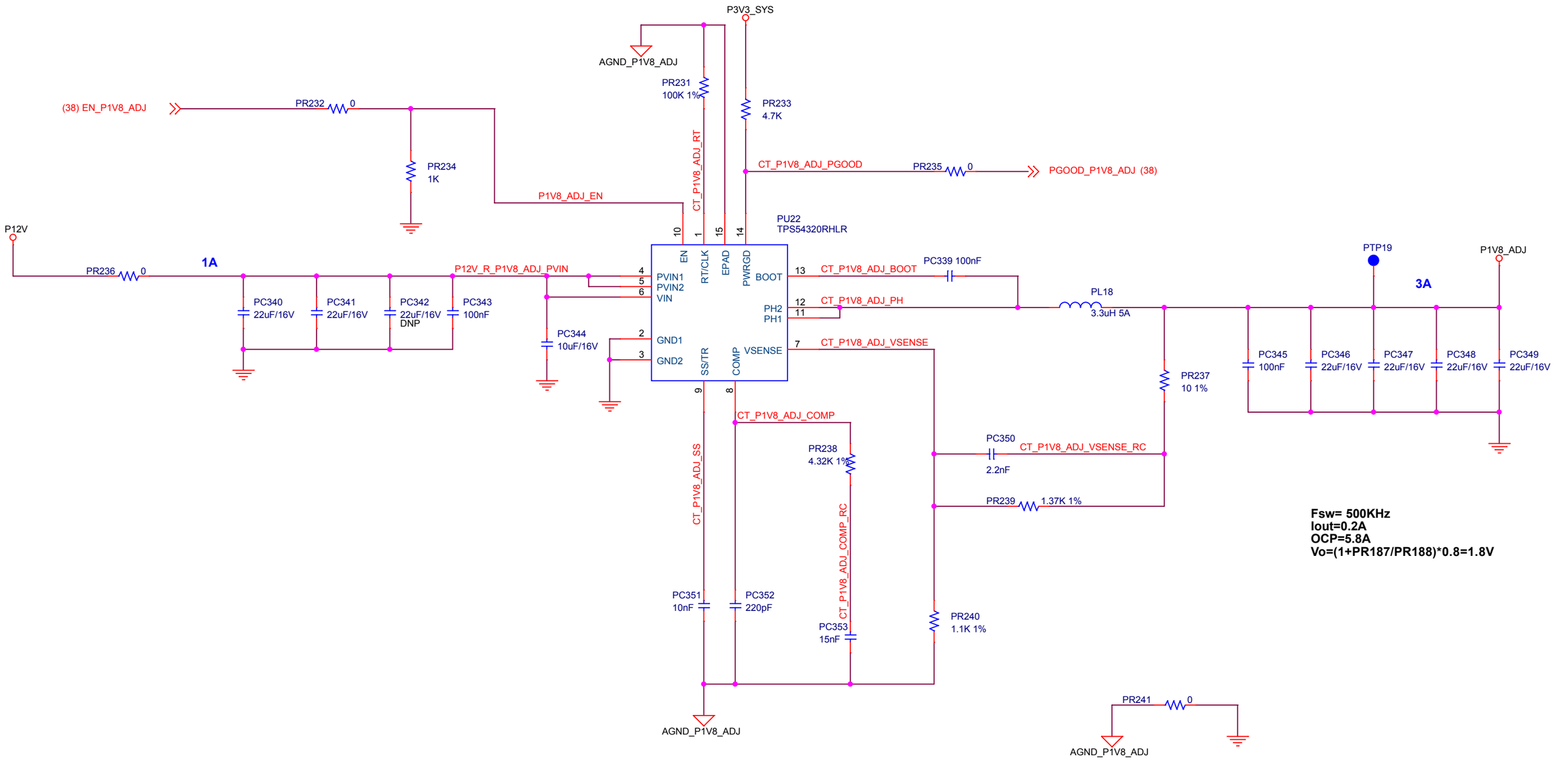

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拟制：	审核：	批准：

Title

Size A3	SCHEMATIC CODE P1V8_ADJ	Rev 1.00
	PROJECT NAME ZYNQ_NvDIMM	
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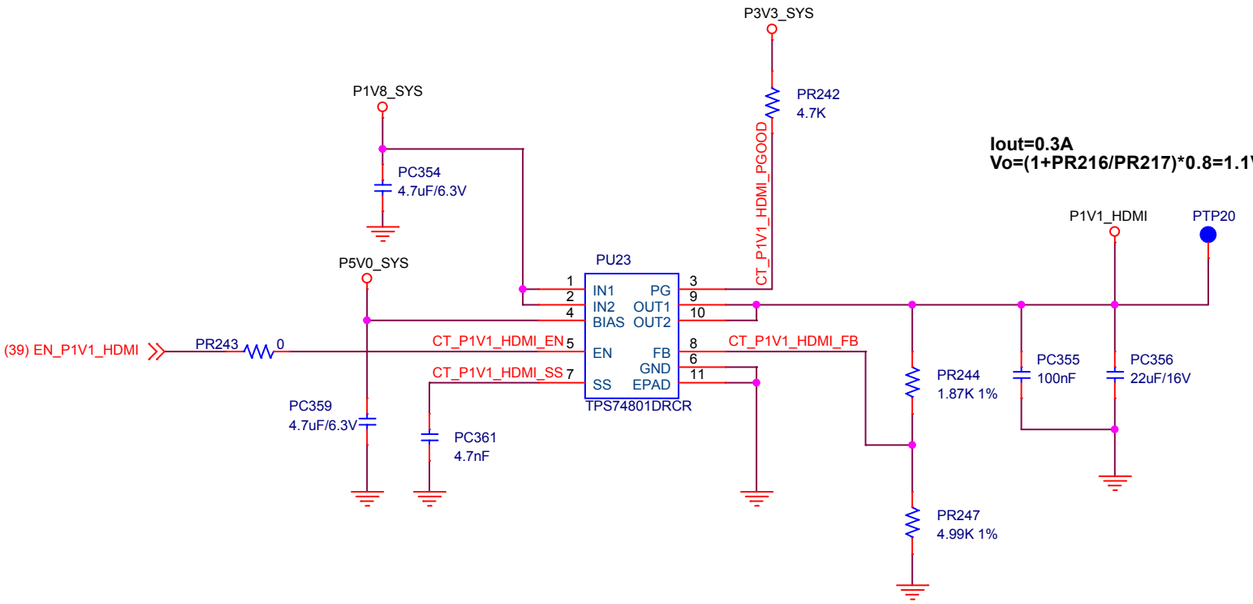

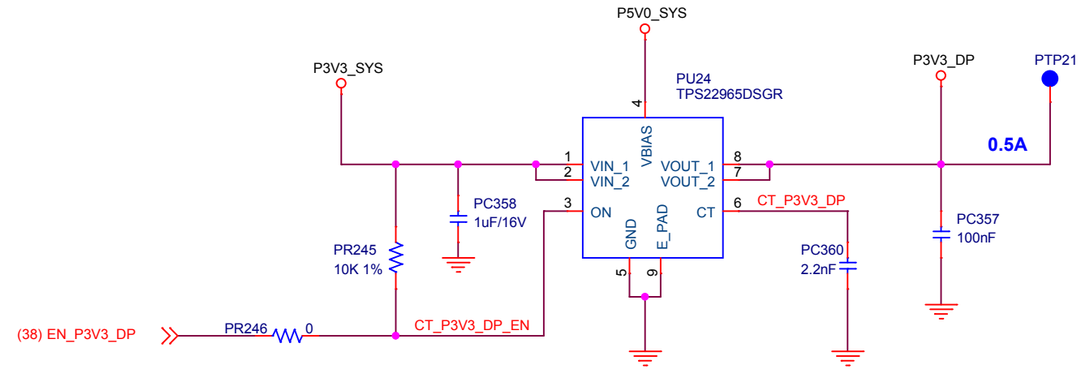

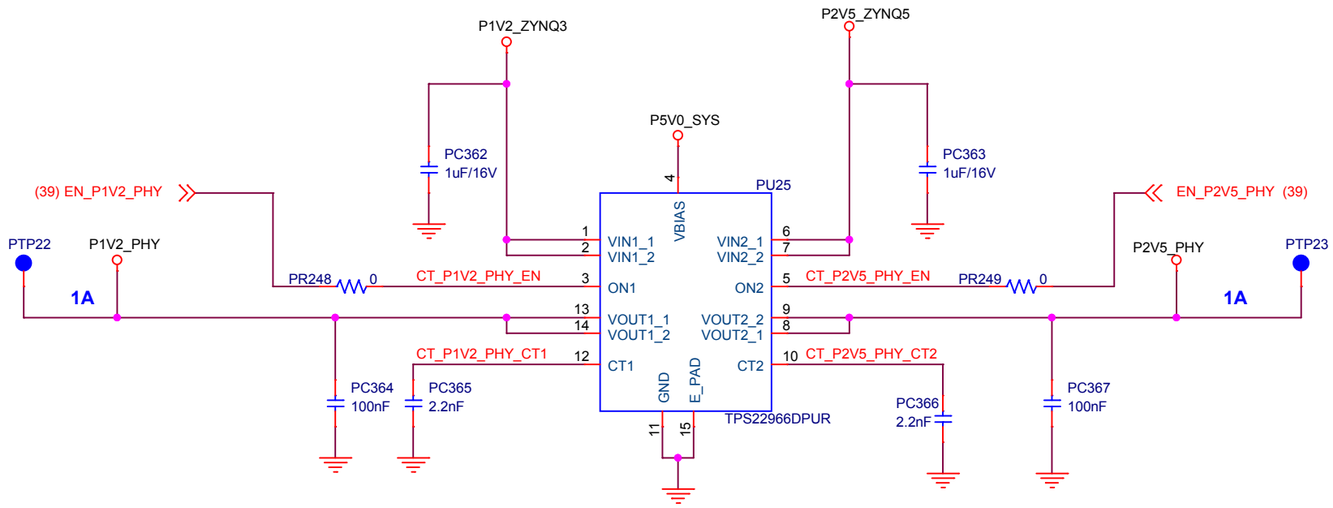

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拟制：	审核：	批准：

Title

Size A3	SCHEMATIC CODE Other Power	Rev 1.00
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