RTL8211DN-VB-GR

INTEGRATED 10/100/1000M ETHERNET TRANSCEIVER

DATASHEET

(CONFIDENTIAL: Development Partners Only)

Rev. 1.4
27 May 2011
Track ID: JATR-2265-11

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USING THIS DOCUMENT

This document is intended for the software engineer’s reference and provides detailed programm information.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide.

REVISION HISTORY

Revision	Release Date	Summary
1.0	2010/04/28	First release.
1.1	2010/08/09	Revised IEEE 802.3az to Draft 3.2. Added section 3.5 UTP/Fiber Auto-Detection to GMII/RGMII Application Diagram, page 4. Revised Table 15 MII/MDI Interface Configuration, page 14. Added section 6.9 Green Ethernet (Gigabit Mode Only), page 16. Added section 6.10.6 Access to Extension Page (ExtPage), page 19. Added section 6.10.7 Access to MDIO Manageable Device (MMD), page 19. Revised Table 22 Page0 Register Mapping and Definitions, page 30. Added section 7.3 MMD Register Mapping and Definition, page 31. Added Table 36 MACR (MMD Access Control Register, Address 0x0D), page 38. Added Table 37 MAADR (MMD Access Address Data Register, Address 0x0E), page 39. Added Table 46, page 42 to Table 51, page 43. Revised section 9.6.5 RGMII Timing Modes, page 59.
1.2	2010/08/13	Revised section 9.6.2 MII Transmission Cycle Timing, page 56. Revised section 9.6.6 SGMII Timing Modes, page 62.
1.3	2010/12/17	Revised Table 39 PHYCR (PHY Specific Control Register, Address 0x10), page 39 (Bit 16.5). Revised Table 53 Power Sequence Parameter, page 51. Revised Table 61 MDC/MDIO Timing, page 55. Revised Table 64 GMII Timing Parameters, page 58.
1.4	2011/05/27	Separated RTL8211D and RTL8211DG versions from RTL8211DN version. Revised section 9.6.2 MII , page 56. Revised section 0 MII Reception Cycle Timing, page 57.

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1. General Description

The Realtek RTL8211DN-VB is a highly integrated Ethernet transceiver that complies with 10Base-T, 100Base-TX, 100Base-FX, 1000Base-T, and 1000Base-X IEEE 802.3 standards. It provides all the necessary physical layer functions to transmit and receive Ethernet packets over CAT 5 UTP cable.

The RTL8211DN uses state-of-the-art DSP technology and an Analog Front End (AFE) to enable high-speed data transmission and reception over UTP cable. Functions such as Crossover Detection & Auto-Correction, polarity correction, adaptive equalization, cross-talk cancellation, echo cancellation, timing recovery, and error correction are implemented in the RTL8211DN to provide robust transmission and reception capabilities at 10Mbps, 100Mbps, or 1000Mbps. The advanced DSP algorithms provide robust communication even in critical environments.

The RTL8211DN supports various interfaces to communicate with the MAC and PHY, including:

? RGMII (Reduced Gigabit Media Independent Interface) for 1000/10Base-T and 100Base-TX

? GMII/MII (Gigabit Media Independent Interface) for 1000/10Base-T and 100Base-TX

? SGMII (Serial Gigabit Media Independent Interface) for 1000Base-T and 100Base-TX

? Supports 1000Base-X and 100Base-FX

The RTL8211DN supports a SerDes interface that can be configured as SGMII, 1000Base-X, and 100Base-FX.

2. Features

1000Base-T/1000Base-X IEEE 802.3ab Compliant

100Base-TX/100Base-FX IEEE 802.3u Compliant

10Base-T IEEE 802.3 Compliant

IEEE 802.3 Compliant GMII/MII

Supports RGMII

Supports IEEE 802.3az-2010 (Energy Efficient Ethernet)

Supports SerDes (SGMII)

Supports UTP or fiber mode output

Supports PHYRSTB core power Turn-Off

Built-in Wake-On-LAN (WOL)

Supports Interrupt function

Supports media converter/interface converter (SGMII to GMII/RGMII or 1000Base-X to 1000Base-T)

Supports Auto-Negotiation

Supports Parallel Detection

JTAG Compliant to IEEE 1149.1

Green Ethernet (Gigabit mode only)

Crossover Detection & Auto-Correction

Automatic polarity correction

Baseline Wander Correction

Supports 120m for CAT.5 cable in 1000Base-T

Supports 3.3V or 2.5V signaling for GMII/RGMII

Supports 25MHz external crystal or OSC

Provides 125MHz clock source for MAC

Provides 4 network status LEDs

Built-in switching regulator

88-pin QFN Package

0.11 μm process with very low power consumption

3. System Applications

MAU (Media Access Unit)

CNR (Communication and Network Riser)

Game Console

Printer and Office Machine

DVD Player and Recorder

Ethernet Hub

Ethernet Switch

In addition, it can be used in any embedded system with an Ethernet MAC that needs a UTP or Fiber physical connection.

3.1. Fiber Application Diagram

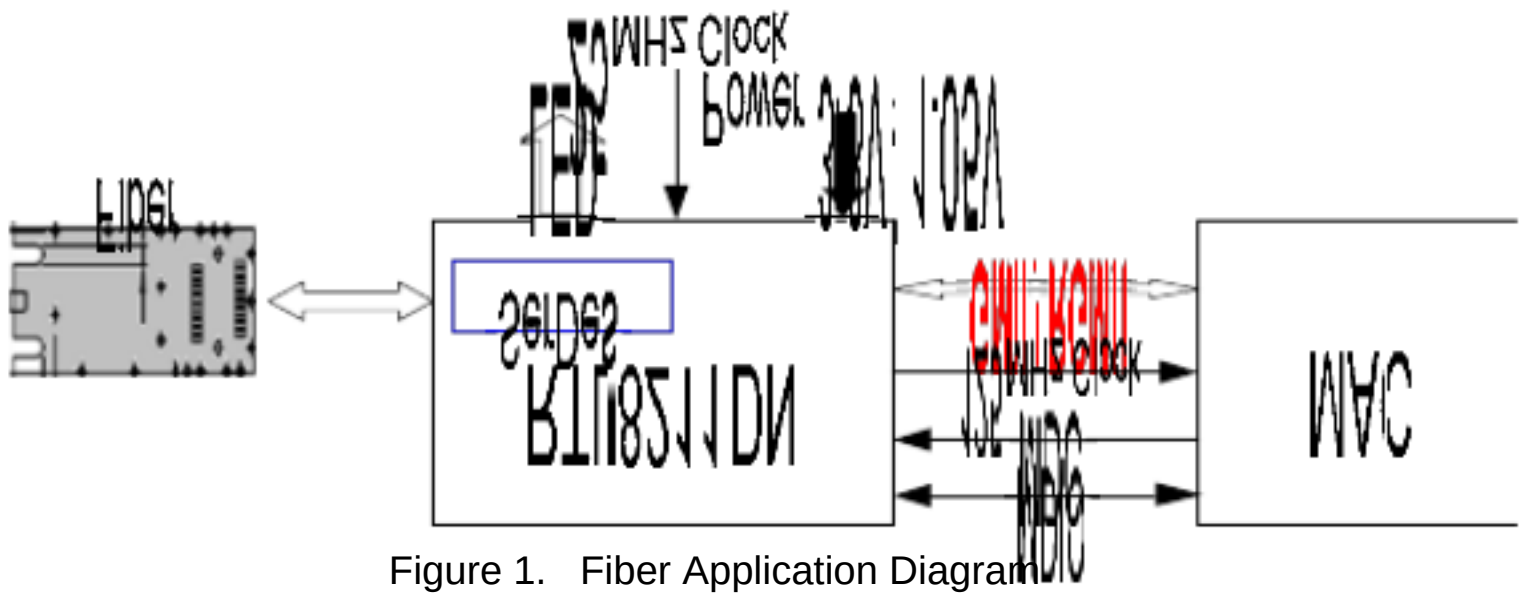


Figure 1. Fiber Application Diagram

3.2. UTP Application Diagram

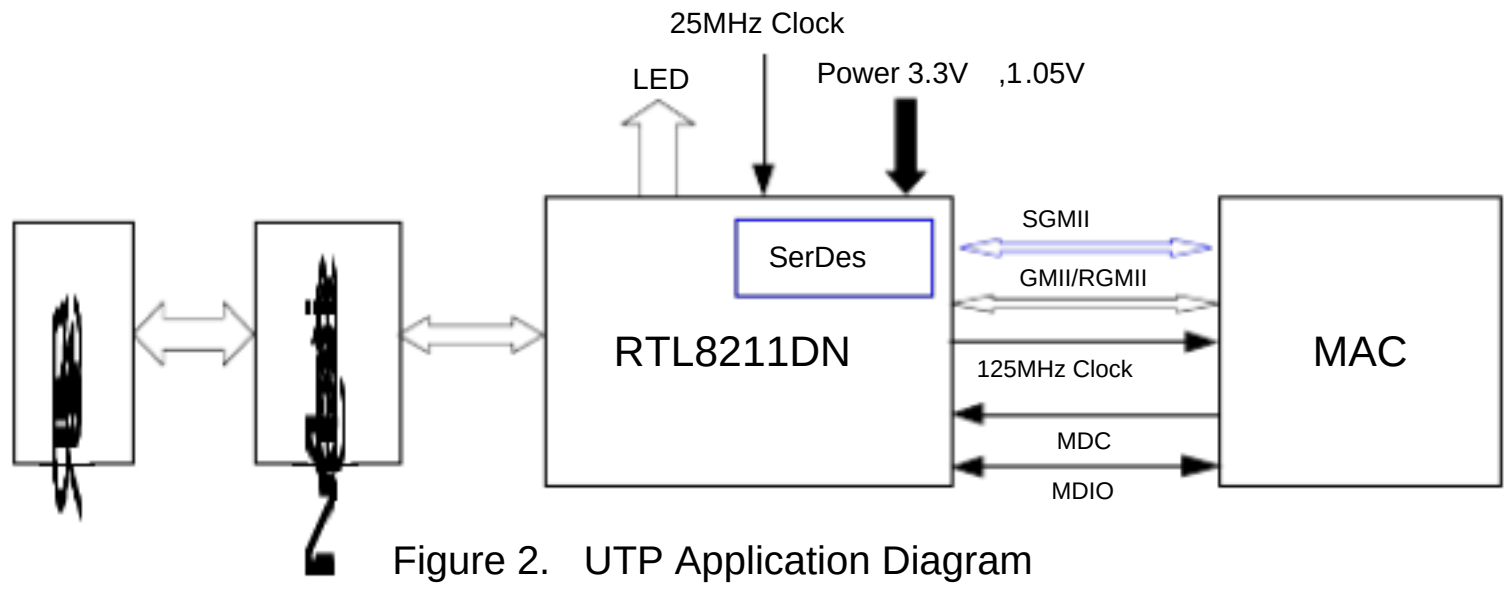


Figure 2. UTP Application Diagram

3.3. Fiber to UTP (Bridge Mode) Application Diagram

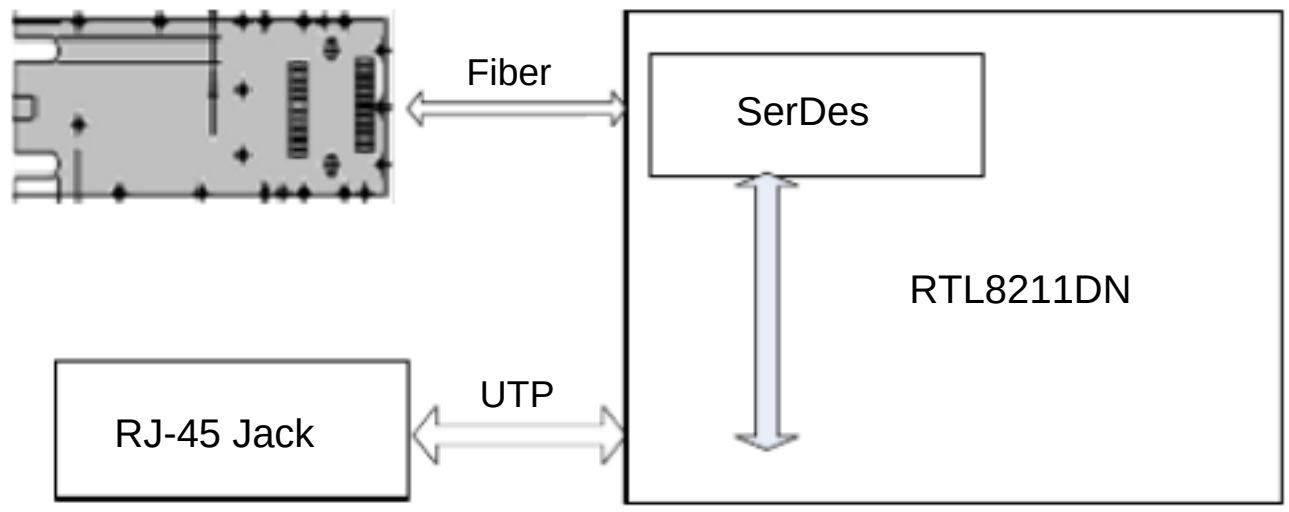


Figure 3. Fiber to UTP (Bridge Mode) Application Diagram

3.4. SGMII to GMII/RGMII (Bridge Mode) Application Diagram

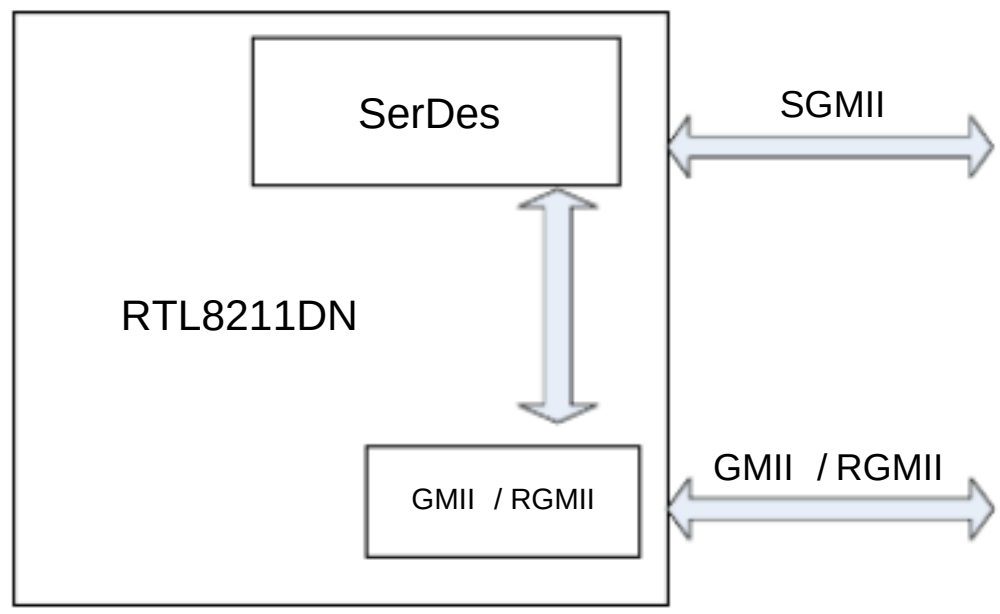


Figure 4. SGMII to GMII/RGMII (Bridge Mode) Application Diagram

3.5. UTP/Fiber Auto-Detection to GMII/RGMII Application Diagram

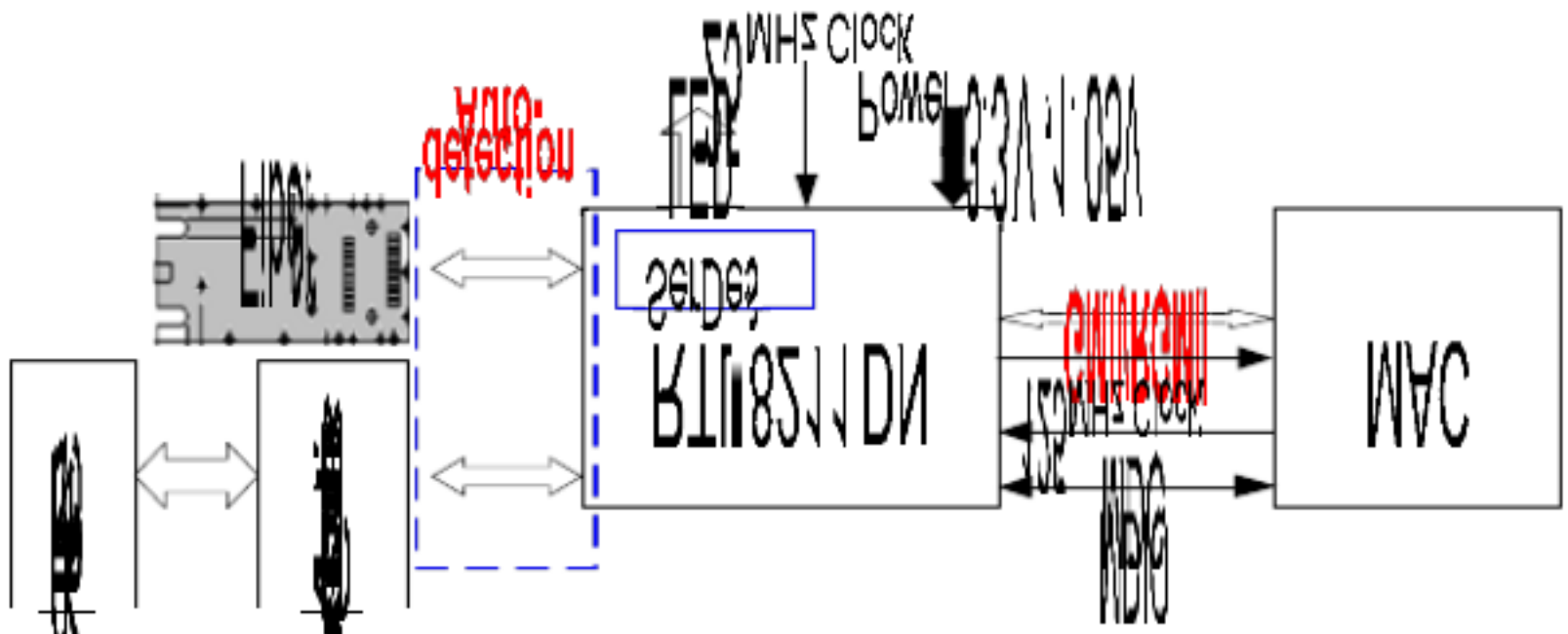


Figure 5. UTP/Fiber Auto-Detection to GMII/RGMII Application Diagram

4. Pin Assignments

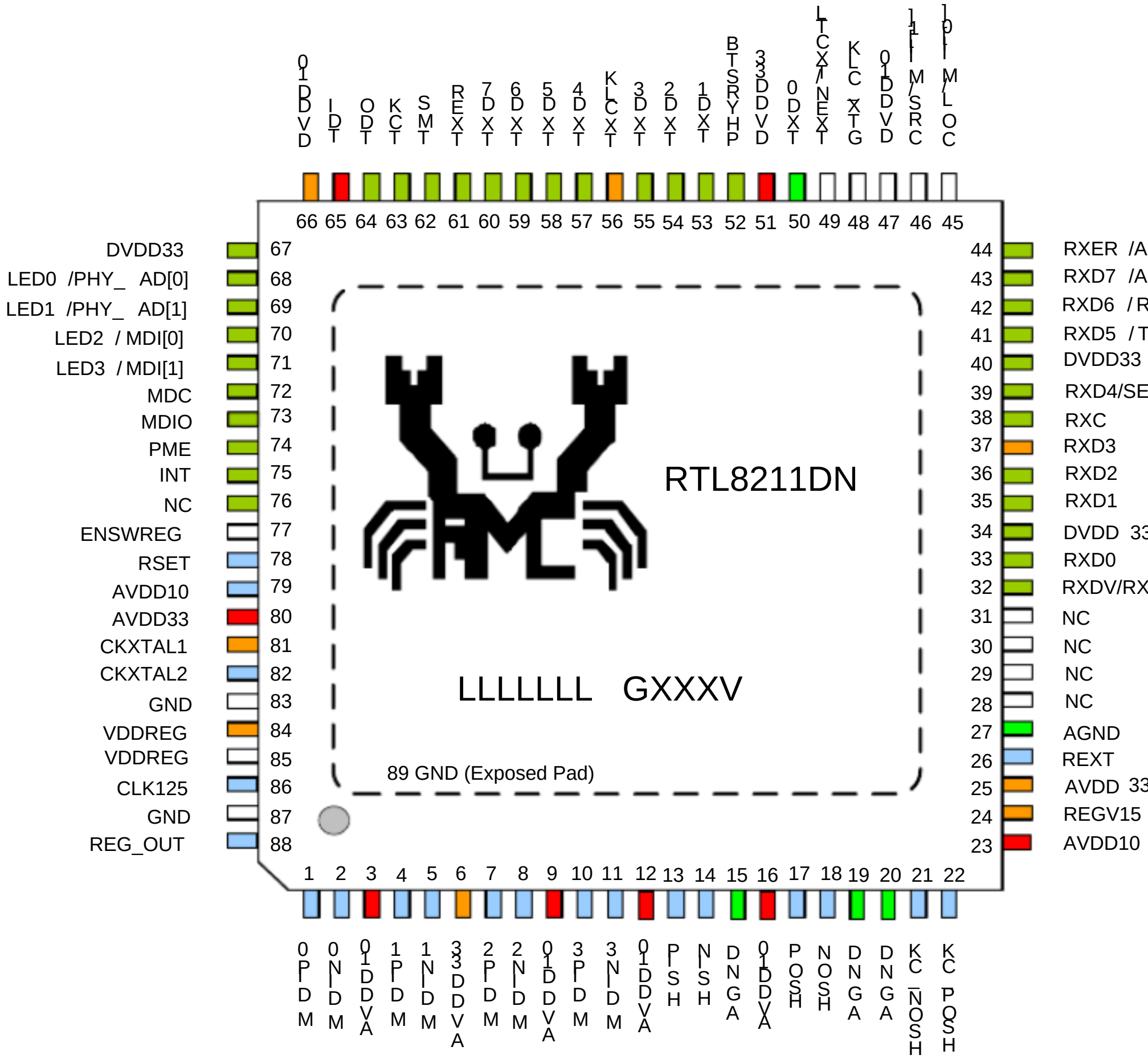


Figure 6. Pin Assignments

4.1. Package Identification

Green package is indicated by the ‘G’ in GXXXV (Figure 6). The version is shown in the location ma ‘V’.

5. Pin Descriptions

Note that some pins have multiple functions. Refer to the Pin Assignments figure for a graphical representation.

I: Input

O: Output

P: Power

PU: Internal Pull up during power on reset

G: Ground

LI: Latched Input during Power up or Reset

IO: Bi-directional input and output

HZ: High impedance during power on reset

PD: Internal Pull down during power on reset

OD: Open Drain

5.1. Transceiver Interface

Table 1. Transceiver Interface

Pin No.	Pin Name	Type	Description
1	MDIP0	IO	In MDI mode, this is the first pair in 1000Base-T, i.e., the BI_DA+/- pair, and is the transmit pair in 10Base-T and 100Base-TX.
2	MDIN0	IO	In MDI crossover mode, this pair acts as the BI_DB+/- pair, and is the receive pair in 10Base-T and 100Base-TX.
4	MDIP1	IO	In MDI mode, this is the second pair in 1000Base-T, i.e., the BI_DB+/- pair, and is the receive pair in 10Base-T and 100Base-TX.
5	MDIN1	IO	In MDI crossover mode, this pair acts as the BI_DA+/- pair, and is the transmit pair in 10Base-T and 100Base-TX.
7	MDIP2	IO	In MDI mode, this is the third pair in 1000Base-T, i.e., the BI_DC+/- pair.
8	MDIN2	IO	In MDI crossover mode, this pair acts as the BI_DD+/- pair.
10	MDIP3	IO	In MDI mode, this is the fourth pair in 1000Base-T, i.e., the BI_DD+/- pair.
11	MDIN3	IO	In MDI crossover mode, this pair acts as the BI_DC+/- pair.

5.2. Clock

Table 2. Clock

Pin No.	Pin Name	Type	Description
81	CKXTAL1	I	25MHz Crystal Input. If a 25MHz oscillator is used, connect CKXTAL1 to the oscillator output.
82	CKXTAL2	O	25MHz Crystal Output. Must be kept floating when an external 25MHz oscillator drives CKXTAL1.
86	CLK125	O/HZ	125MHz Reference Clock Generated from Internal PLL. This clock will be stopped when PHYRSTB is kept low. This pin should be left floating if this function is not used.

5.3. GMII/MII

Table 3. GMII/MII

Pin No.	Pin Name	Type	Description
48	GTX_CLK	I	The transmit reference clock is 125MHz.
56	TXCLK	O	The transmit reference clock is 25MHz or 2.5MHz depending on speed. This clock will be stopped when PHYRSTB is kept low.
50	TXD0	I	Transmit Data. Data is transmitted from MAC to PHY via TXD[7:0].
53	TXD1	I	
54	TXD2	I	
55	TXD3	I	
57	TXD4	I	
58	TXD5	I	
59	TXD6	I	
60	TXD7	I	
49	TXEN	I	Transmit Enable. In RGMII mode, this pin is named TXCTL.
61	TXER	I	Transmit Error. When both TXER and TXEN are asserted, the transmit error symbol is transmitted onto the cable. When TXER is asserted and TXEN is de-asserted, the carrier extension symbol is transmitted onto the cable. Connect this pin to GND if the MAC does not have a TXER pin.
38	RXC	O	The continuous receive reference clock will be 125MHz, 25MHz, or 2.5MHz, and is derived from the received data stream. This clock will be stopped when PHYRSTB is kept low.
33	RXD0	O	Receive Data. Data is transmitted from PHY to MAC via RXD[7:0].
35	RXD1	O	
36	RXD2	O	
37	RXD3	O	
39	RXD4	LI/O/PU	
41	RXD5	LI/O/PD	
42	RXD6	LI/O/PU	
43	RXD7	LI/O/PU	
32	RXDV	O	Receive Data Valid. In RGMII mode, this pin is named RXCTL.
44	RXER	LI/O/PU	Receive Error. When both RXER and RXDV are asserted, an error symbol is received from the cable. When RXER is asserted and RXDV is de-asserted, it means false carrier or carrier extension symbol is detected on the cable.
45	COL	LI/O/PD	Collision In Half Duplex Mode
46	CRS	LI/O/PD	Carrier Sense.

5.4. RGMII

Table 4. RGMII

Pin No.	Pin Name	Type	Description
48	GTX_CLK	I	The transmit reference clock will be 125MHz, 25MHz, or 2.5MHz depending on speed.
50	TXD0	I	Transmit Data. Data is transmitted from MAC to PHY via TXD[3:0].
53	TXD1	I	
54	TXD2	I	
55	TXD3	I	
49	TXCTL	I	Receive Control Signal from the MAC. In GMII/MII mode, this pin is named TXEN.
38	RXC	O	The continuous receive reference clock will be 125MHz, 25MHz, or 2.5MHz, and is derived from the received data stream. This clock will be stopped when PHYRSTB is kept low.
33	RXD0	O	Receive Data. Data is transmitted from PHY to MAC via RXD[3:0].
35	RXD1	O	
36	RXD2	O	
37	RXD3	O	
32	RXCTL	O	Transmit Control Signal to the MAC. In GMII/MII mode, this pin is named RXDV .
41	TXDLY	LI/O/PD	RGMII Transmit Clock Timing Control. 1: Add 2ns delay to TXC for TXD latching
42	RXDLY	LI/O/PU	RGMII Receiver Clock Timing Control. 1: Add 2ns delay to RXC for RXD latching

5.5. SGMII

Table 5. SGMII

Pin No.	Pin Name	Type	Description
13	HSIP	I	SGMII Differential Input: 1.25GHz serial interfaces to receive data from an External device that supports the SGMII interface. The differential pair has an internal 100-ohm termination resistor.
14	HSIN	I	
15, 19, 20, 27	AGND	G	Analog Ground for SGMII Circuits.
17	HSOP	O	SGMII Differential Output: 1.25GHz serial interfaces to transfer data from an External device that supports the SGMII interface. The differential pair has an internal 100-ohm termination resistor.
18	HSON	O	
21	HSON_CK	O	SGMII 625MHz Receive CLK Pair. 625MHz differential serial clock output. The differential pair has an internal 100-ohm termination resistor.
22	HSOP_CK	O	
24	REGV15	P	Internal 1.5V regulator power when fiber mode enabled. AVDD10 power pin when SGMII enabled.
26	REXT	O	Reference. External Resistor Reference. Connect to 12k-ohm resistor.

5.6. Management Interface

Table 6. Management Interface

Pin No.	Pin Name	Type	Description
72	MDC	I	Management Data Clock.
73	MDIO	IO	Input/Output of Management Data.
74	PME	O/OD	Power Management Event (Supports 3.3V and 5V Pull Up). Set low if receives magic packet or wake up frame; active low. The pin should be left floating if does not use this function.
64	TDO	O	Test Data In for JTAG Interface.
65	TDI	I/PU	Test Data Out for JTAG Interface.
62	TMS	I/PU	Test Mode State for JTAG Interface.
63	TCK	I/PD	Test Clock for JTAG Interface.
75 INT		O/OD	Interrupt. Set low if status changes; Active Low. The pin should be left floating if this function not used.

5.7. Reset

Table 7. Reset

Pin No.	Pin Name	Type	Description
52	PHYRSTB	I/PU	Hardware Reset. Active low. For a complete PHY reset, this pin must be asserted low for at least 10ms. All registers will be cleared after a hardware reset.

5.8. Mode Selection

Table 8. Mode Selection

Pin No.	Pin Name	Type	Description
68	PHY_AD[0]	LI/O/PU	PHY Address Configuration.
69	PHY_AD[1]	LI/O/PD	
43	AN[0]	LI/O/PU	NWay Configuration.
44	AN[1]	LI/O/PU	
45	MII[0]	LI/O/PD	MDI and Interface (SGMII/GMII/MII/RGMII) Configuration.
46	MII[1]	LI/O/PD	
70	MDI[0]	LI/O/PU	
71	MDI[1]	LI/O/PD	
39	SELRGV	LI/O/PU	Pull Up for 3.3V GMII/RGMII. Pull Down for 2.5V GMII/RGMII.

Note: See section 6.7 Hardware Configuration, page 13 for details.

5.9. LED Indication

Table 9. LED Indication

Pin No.	Pin Name	Type	Description
68	LED0	LI/O/PU	Active
69	LED1	LI/O/PD	LED 10/100/1000
70	LED2	LI/O/PU	LED 10/100/1000+Active
71	LED3	LI/O/PD	LED100/1000 (Fiber mode only) + Activity (Fiber only)

Note: See section 6.13 LED Configuration, page 27 for details.

5.10. Regulator and Reference

Table 10. Regulator and Reference

Pin No.	Pin Name	Type	Description
78	RSET	O	External Resistor Reference. Connect to 2.49k-ohm resistor
84, 85	VDDREG	P	3.3V Analog Power Supply for Switching Regulator.
88	REG_OUT	O	Switching Regulator 1.05V Output. Connect to a 4.7 μH inductor.
3	AVDD10	P	Feedback Pin for Switching Regulator.
77	ENSWREG	I	3.3V: Enable switching regulator. 0V: Disable switching regulator.

5.11. Power and Ground

Table 11. Power and Ground

Pin No.	Pin Name	Type	Description
34, 40, 51, 67	DVDD33	P	Digital Power. 3.3V.
34, 40	DVDD33	P	GMII/RGMII Power Pins. For 3.3 or 2.5V GMII/RGMII I/O.
47, 66	DVDD10	P	Digital Power. 1.05V.
6, 25, 80	AVDD33	P	Analog Power. 3.3V.
3, 9, 12, 16, 23, 79	AVDD10	P	Analog Power. 1.05V.
83, 87	GND	G	Ground. Exposed Pad (E-Pad) Digital Ground (see section 10, page 64).

5.12. Not Connected

Table 12. Not Connected

Pin No.	Pin Name	Type	Description
28, 29, 30, 31, 76	NC	-	Not Connected.

6. Function Description

6.1. 1000Base-T Transmitter

The 1000Base-TX transmit function performs 8B/10B coding, scrambling, and 4D-PAM5 encoding. These code groups are passed through a waveform-shaping filter to minimize EMI effects, and are transmitted onto 4-pair CAT5 cable at 125Mbps through a D/A converter.

6.2. 1000Base-T Receiver

Input signals from the media pass through the sophisticated on-chip hybrid circuit to subtract the transmitted signal from the input signal for effective reduction of near-end echo. Afterwards, the received signal is processed with state-of-the-art technology, e.g., adaptive equalization, BLW (Baseline Wander) correction, cross-talk cancellation, echo cancellation, timing recovery, error correction, and 4D-PAM5 decoding. The 8-bit-wide data is recovered and sent to the GMII/MII/RGMII/SGMII interface at a clock speed of 125MHz. The Rx MAC retrieves the packet data from the internal receive GMII/MII/RGMII/SGMII interface and sends it to the packet buffer manager.

6.3. Energy Efficient Ethernet (EEE)

The RTL8211DN supports IEEE 802.3az-2010, also known as Energy Efficient Ethernet (EEE), at 10Mbps, 100Mbps, and 1000Mbps. It provides a protocol to coordinate transitions to/from a lower power consumption level (Low Power Idle mode) based on link utilization. When no packets are being transmitted, the system goes to Low Power Idle mode to save power. Once packets need to be transmitted, the system returns to normal mode, and does this without changing the link status and without dropping/corrupting frames.

To save power, when the system is in Low Power Idle mode, most of the circuits are disabled, however, the transition time to/from Low Power Idle mode is kept small enough to be transparent to upper layer protocols and applications.

EEE also specifies a negotiation method to enable link partners to determine whether EEE is supported and to select the best set of parameters common to both devices.

Refer to http://www.ieee802.org/3/az/index.html for more details.

6.4. Wake-On-LAN (WOL)

The RTL8211DN can monitor the network for a Wakeup Frame or a Magic Packet, and notify the system via the PME (Power Management Event) pin when such a packet or event occurs. The system can then be restored to a normal state to process incoming jobs. The PME pin needs to be connected with a 4.7k-ohm resistor and pulled up to 3.3V or 5V. When the Wakeup Frame or a Magic Packet is sent to the PHY, the PME pin will be set low to notify the system to wake up. Refer to the WOL application note for details.

Magic Packet Wakeup occurs only when the following conditions are met:

? The destination address of the received Magic Packet is acceptable to the RTL8211DN, e.g., a broadcast, multicast, or unicast packet addressed to the current RTL8211DN.

? The received Magic Packet does not contain a CRC error.

? The Magic Packet pattern matches; i.e., 6 * FFh + MISC (can be none) + 16 * DID (Destination ID) in any part of a valid Ethernet packet.

A Wakeup Frame event occurs only when the following conditions are met:

? The destination address of the received Wakeup Frame is acceptable to the RTL8211DN, e.g., a broadcast, multicast, or unicast address to the current RTL8211DN.

? The received Wakeup Frame does not contain a CRC error.

? The 16-bit CRC* of the received Wakeup Frame matches the 16-bit CRC of the sample Wakeup Frame pattern given by the local machine ’s OS. Or, the RTL8211DN is configured to allow direct packet wakeup, e.g., a broadcast, multicast, or unicast network packet.

Note1: 16-bit CRC: The RTL8211DN supports eight long Wake-Up frames (covering 128 mask bytes from offset 0 to 127 of any incoming network packet). CRC16 polynomial = $x^{16} + x^{12} + x^5 + 1$.

6.5. MDI Interface

This interface consists of four signal pairs; MDI0, MDI1, MDI2, and MDI3. Each signal pair consists of two bi-directional pins that can transmit and receive at the same time. The MDI interface has internal termination resistors, and therefore reduces BOM cost and PCB complexity. For 1000Base-T, all four pairs are used in both directions at the same time. For 10/100 links and during auto-negotiation, only pairs A and B are used.

6.6. SerDes (SGMII) Interface

The RTL8211DN supports one SerDes interface for 1000/100Base-X application. The SerDes interface can be enabled/disabled by pin strapping MDI[1:0] and MII[1:0]. These pins must be connected to 3.3V via a 4.7K-ohm resistor for SerDes operation.

Table 15, page 14 shows the SerDes interface configuration options. The application diagram is shown in Figure 7. When SerDes is selected in MDI mode, SGMII cannot be selected as PHY and MAC interface.

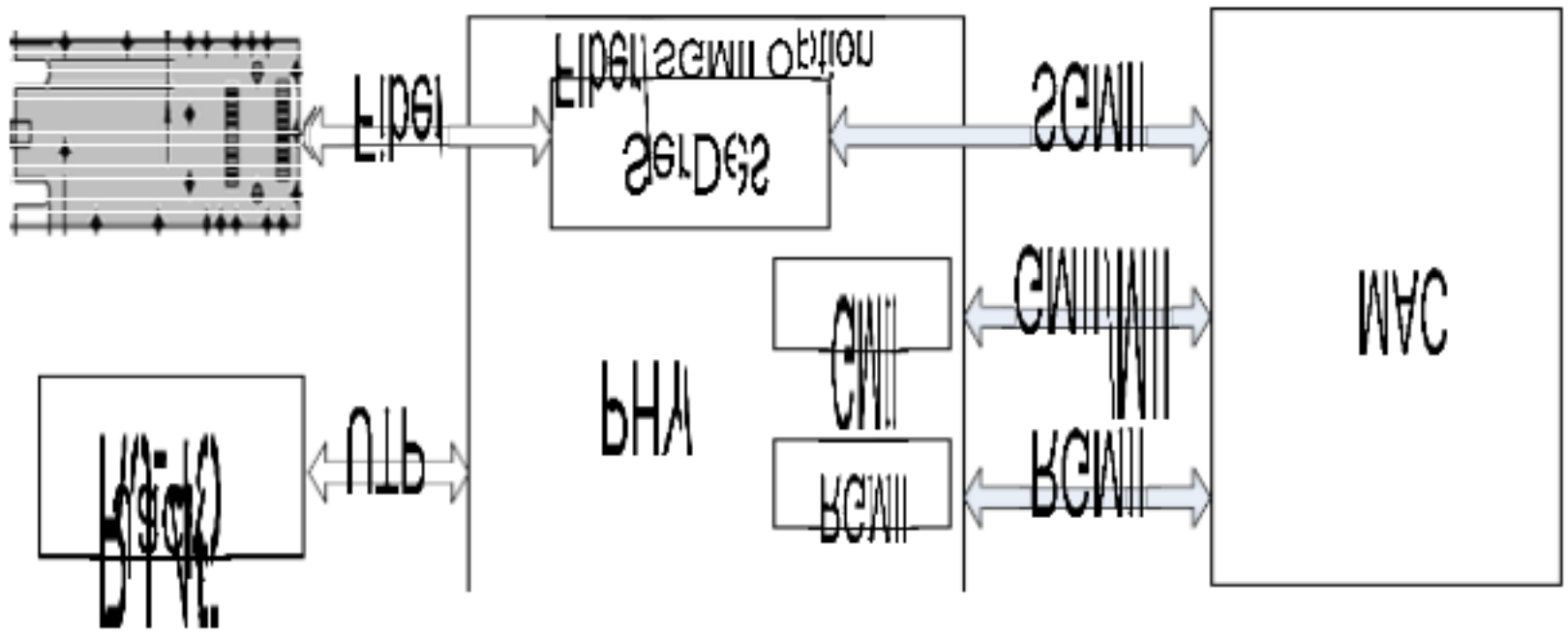


Figure 7. PHY Application

6.7. Hardware Configuration

The operation speed, interface mode, and PHY address can be set by the CONFIG pins. The respective value mapping of CONFIG with the configurable vector is listed in Table 13. To set the CONFIG pins, an external pull-high or pull-low resistor is required.

Table 13. CONFIG Pins vs. Configuration Register

RTL8211DN Pin	Pin Name
LED0	PHY_AD[0]
LED1	PHY_AD[1]
LED2	MDI[0]
LED3	MDI[1]
RXD7	AN[0]
RXER	AN[1]
COL	MII[0]
CRS	MII[1]
RXD6	RX Delay
RXD5	TX Delay

Table 14. Configuration Register Definition (PHY AD and NWay)

Configuration	Description
PHYAD[1:0] PHY Address.	PHYAD sets the PHY address for the device. Note: PHYAD[1:0]=00 can support all PHY addresses. It can automatically remember the first non-zero PHY address sent by the MAC.
AN[1:0]	Auto-Negotiation (NWay) Configuration. AN[1:0] controls the setting of Auto-Negotiation speed and duplex settings. 00: 10Base-T Full/Half Duplex 01: 100Base-TX Half Duplex; 10Base-T Full/Half Duplex 10: 100Base-TX Full/Half Duplex; 10Base-T Full/Half Duplex 11: NWay. Advertise all capabilities (10/1000Base-T; 100Base-TX Full/Half Duplex)

For the interface configuration, MDI CONFIG pins and MII CONFIG pins can be easily set via an external resistor. The various settings are shown below:

CFG_MDI[1:0]

{0, 0}: Use fiber as MDI, with GMII, RGMII as MII options

{0, 1}: Use UTP as MDI, with GMII, RGMII, SGMII as MII options

{1, 0}: Auto-sense UTP/fiber as MDI, with GMII/RGMII as MII options

{1, 1}: Operate as interface converter at MAC site

CFG_MII[1:0]

{0, 0}: Use GMII as MII, with UTP/fiber/auto-sensing as MDI options

{0, 1}: Use RGMII as MII, with UTP/fiber/auto-sensing as MDI options

{1, 0}: Use SGMII as MII, with UTP as MDI

{1, 1}: Operate as media converter. Convert packets between UTP and fiber

Table 15. MII/MDI Interface Configuration

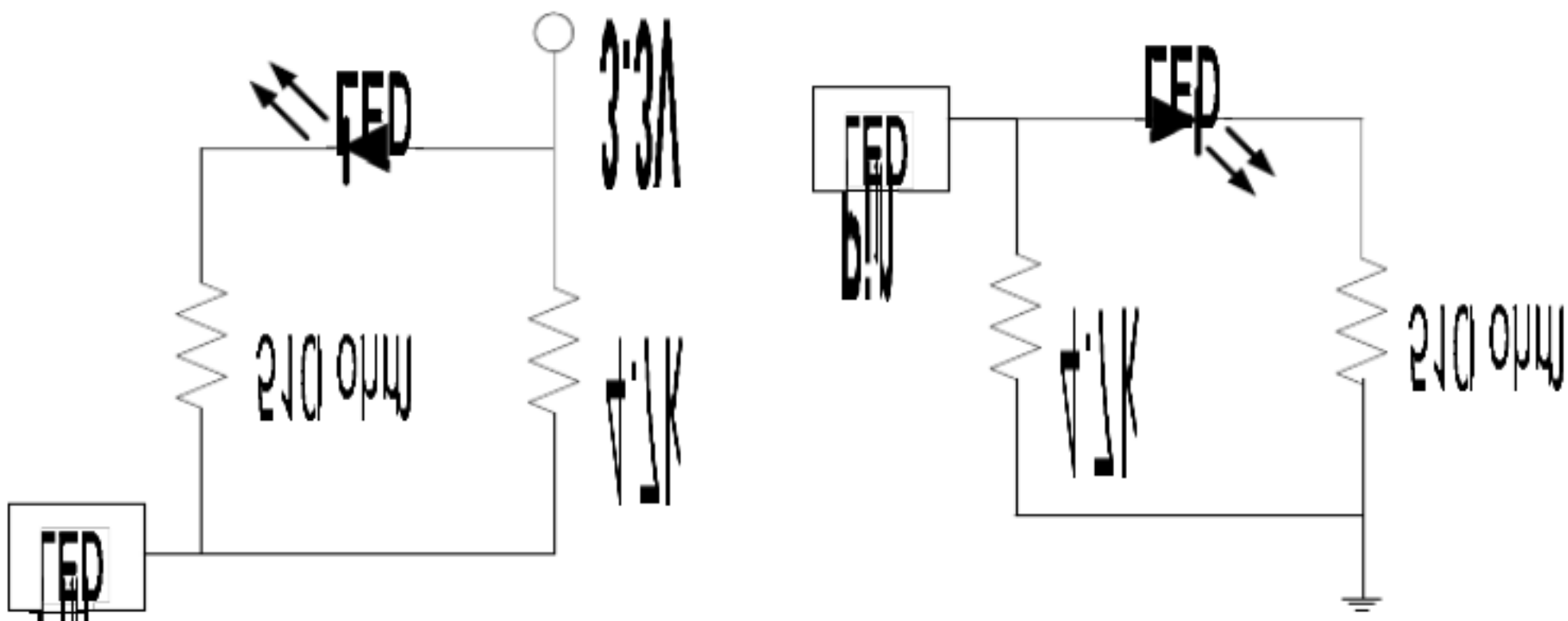
	MDI[0,0]	MDI[0,1]	MDI[1,0]	MDI[1,1]
MII[0,0] Fiber<->GMII		UTP<->GMII	UTP/Fiber<->GMII SGMII<->GMII	
MII[0,1] Fiber<->RGMII		UTP<->RGMII UTP/Fiber<->RGMII SGMII<->RGMII		
MII[1,0] UTP<->SGMII	Not Valid Setting		Not Valid Setting	
MII[1,1]		UTP<->Fiber		

Note: The RTL8211DN default setting is UTP<->GMII mode {MDI[0,1] MII[0,0]}. UTP/Fiber = media detection.

6.8. LED and PHY Address Configuration

In order to reduce the pin count on the RTL8211DN, the LED pins are duplexed with the PHY address pins. As the PHYAD strap options share the LED output pins, the external combinations required for strapping and LED usage must be considered in order to avoid contention. Specifically, when the LED outputs are used to drive LEDs directly, the active state of each output driver is dependent on the logic level sampled by the corresponding PHYAD input upon power-up/reset.

For example, as Figure 8 (left-side) shows, if a given PHYAD input is resistively pulled high then the corresponding output will be configured as an active low driver. On the right side, we can see that if a given PHYAD input is resistively pulled low then the corresponding output will be configured as an active high driver. The PHY address configuration pins should not be connected to GND or VCC directly, but must be pulled high or low through a resistor (e.g., 4.7K Ω). If no LED indications are needed, the components of the LED path (LED+510Ω) can be removed.



PHY Address[:]=Logical 1
RXDLY=Logical 1
LED Indication=Active low

PHY Address[:]=Logical 0
RXDLY=Logical 0
LED Indication=Active High

Figure 8. LED and PHY Address Configuration

6.9. Green Ethernet (Gigabit Mode Only)

6.9.1. Cable Length Power Saving

In Gigabit mode the RTL8211DN provides dynamic detection of cable length and dynamic adjustment of power required for the detected cable length. This feature provides high performance with minimum power consumption.

6.9.2. Register Setting

Follow the register settings below to enable Green Ethernet:

Write Reg31, Data=0x0003 (page3)

Write Reg25, Data=0x3247

Write Reg31, Data=0x0005 (page5)

Write Reg1, Data=0x0240

Write Reg31, Data=0x0000 (page0)

Follow the register settings below to disable Green Ethernet:

Write Reg31, Data=0x0003 (page3)

Write Reg25, Data=0x3246

Write Reg31, Data=0x0000 (page0)

6.10. MAC/PHY Interface

The RTL8211DN supports industry standards and is suitable for most off-the-shelf MACs with GMII/MII/RGMII/SGMII interfaces.

6.10.1. MII

In 100Base-TX and 10Base-T modes (MII mode is selected), TXC and RXC sources are 25MHz and 2.5MHz respectively. TXC and RXC will always be generated by the PHY. TXD[3:0] and RXD[3:0] signals are used for date transitions.

6.10.2. GMII

In 1000Base-T mode (GMII interface is selected), a 125MHz transmit clock is expected on GTX_CLK. TXCLK sources 25MHz or 2.5MHz clock depending on the link speed. RXCLK sources the 125MHz receive clock.

6.10.3. RGMII

In 1000Base-T mode (RGMII interface is selected), TXC and RXC sources are 125MHz. TXC will always be generated by the MAC and RXC will always be generated by the PHY. TXD[3:0] and RXD[3:0] signals are used for date transitions on rising and falling edges of the clock.

6.10.4. SGMII

The Serial Gigabit Media Independent Interface (SGMII) is a follow-on from MII, a standard interface used to connect a MAC-block to a PHY. It is used for Gigabit Ethernet (Ethernet/Fast Ethernet uses MII). It differs from GMII/MII by its low-power requirements and low-pin-count serial interface (commonly referred to as SerDes). To carry frame data and link rate information between a 10/100/1000 PHY and an Ethernet MAC, SGMII uses a differential pair for data signals and for clocking signals, with both being present in each direction (i.e., transmit and receive). The data signals operate at 1.25G/baud and the clocks operate at 625MHz (a DDR interface). Due to the high speed of operation, the use of differential pairs provides signal integrity while minimizing system noise.

6.10.5. Management Interface

The management interface provides access to the internal registers through the MDC and MDIO pins as described in IEEE 802.3u section 22. The MDC signal, provided by the MAC, is the management data clock referenced to the MDIO signal. The MDIO is the management data input/output and is a bi-directional signal that runs synchronously to MDC. The MDIO pin needs a 1.5k-ohm pull-up resistor to maintain the MDIO high during idle and turnaround.

Preamble suppression is the default setting of the RTL8211DN after power-on. However, there still must be at least one idle bit between operations.

Up to 32 bits, the RTL8211DN can share the same MDIO line. In switch/router applications, each port should be assigned a unique address during the hardware reset sequence, and it can only be addressed via that unique PHY address. For detailed information on the RTL8211DN management registers, see section 7 Register Descriptions, page 30.

Table 16. Management Frame Format

	Management Frame Fields							
	Preamble	ST	OP	PHYAD	REGAD	TA	DATA	IDLE
Read 1 ···	1	01	10	AAAAA	RRRRR	Z0	DDDDDDDDDDDDDDDD	Z
Write 1 ···	1	01	01	AAAAA	RRRRR	10	DDDDDDDDDDDDDDDD	Z

Table 17. Management Frame Description

Name	Description
Preamble	32 Contiguous Logical 1 ’s Sent by the MAC on MDIO, along with 32 Corresponding Cycles on MDC. This provides synchronization for the PHY.
ST	Start of Frame. Indicated by a 01 pattern.
OP Operation	Code. Read: 10 Write: 01
PHYAD PHY	Address. Up to 4 PHYs can be connected to one MAC. This 2-bit field selects which PHY the frame is directed to.
REGAD Register	Address. This is a 5-bit field that sets which of the 32 registers of the PHY this operation refers to.
TA Turnaround.	This is a 2-bit-time spacing between the register address and the data field of a frame to avoid contention during a read transaction. For a read transaction, both the STA and the PHY remain in a high-impedance state for the first bit time of the turnaround. The PHY drives a zero bit during the second bit time of the turnaround of a read transaction.
DATA Data.	These are the 16 bits of data.
IDLE Idle	Condition. Not truly part of the management frame. This is a high impedance state. Electrically, the PHY resistor will pull the MDIO line to a logical ‘1’.

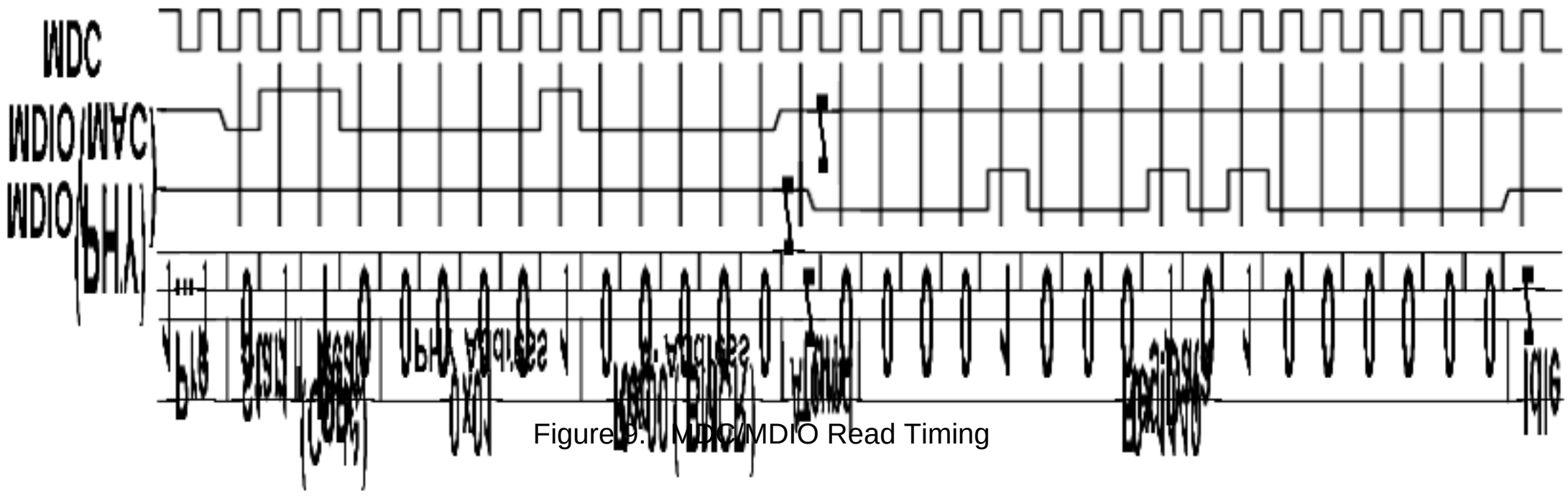


Figure 9. MDC/MDIO Read Timing

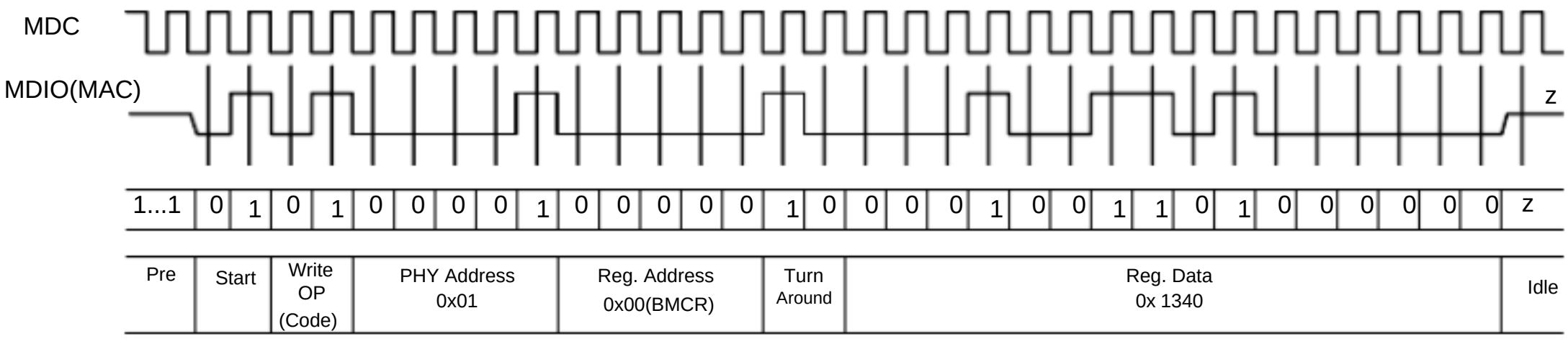


Figure 10. MDC/MDIO Write Timing

6.10.6. Access to Extension Page (ExtPage)

Set MDIO commands as shown below to switch to the Extension Page (ExtPage) 0xXY (in Hex).

1. Write Register 31 Data=0x0007 (set to Extension Page)

2. Write Register 30 Data=0x00XY (Extension Page XY)

3. Write the target Register Data

4. Write Register 31 Data=0x0000 (switch to Page 0)

6.10.7. Access to MDIO Manageable Device (MMD)

The MDIO Manageable Device (MMD) is an extension to the management interface that provides the ability to access more device registers while still retaining logical compatibility with the MDIO interface, defined in section 7.1 Page0 Register Mapping and Definitions, page 30. Access to MMD configuration is provided via Registers 13 and 14.

MMD Read/Write Operation

1. Write Function field to 00 (address mode) and DEVAD field to the device address value for the desired MMD (Register 13).

2. Write the desired address value to the MMD ’s address register (Register 14).

3. Write Function field to 01 (data mode; no post increment) and DEVAD field to the same device address for the desired MMD (Register 13).

4. Read: Go to step 5. Write: Go to step 6.

5. Read the content of the selected register in MMD (Register 14).

6. Write the content of the selected register in MMD (Register 14).

6.11. Auto-Negotiation

Auto-Negotiation is a mechanism to determine the fastest connection between two link partners. For copper media applications, it was introduced in IEEE 802.3u for Ethernet and Fast Ethernet, and then in IEEE 802.3ab to address extended functions for Gigabit Ethernet. It performs the following:

? Auto-Negotiation Priority Resolution

? Auto-Negotiation Master/Slave Resolution

? Auto-Negotiation PAUSE/ASYMMETRIC PAUSE Resolution

? Crossover Detection & Auto-Correction Resolution

Upon de-assertion of a hardware reset, the RTL8211D can be configured to have auto-negotiation enabled, or be set to operate in 10Base-T, 100Base-TX, or 1000Base-T mode via the CONFIG pins (see section 6.7 Hardware Configuration, page 13).

The auto-negotiation process is initiated automatically upon any of the following:

? Power-up

? Hardware reset

? Software reset (register 0.15)

? Restart auto-negotiation (register 0.9)

? Transition from power down to power up (register 0.11)

? Entering the link fail state

Table 18. 1000Base-T and Next Page Bit Assignments

Bit	Name	Bit Description	Register Location
Base Page			
D15 NP		Next Page. 1: Indicates that Next Page follows 0: Indicates that no Next Page follows	-
D14 Ack		Acknowledge. 1: Indicates that a device has successfully received its link partner Link Code Word (LCW)	- ’s
D13 RF		Remote Fault. 1: Indicates to its link partner that a device has encountered a fault condition	-
D[12:5] A[7:0]		Technology Ability Field. Indicates to its link partner the supported technologies specific to the selector field value.	Register 4.[12:5] Table 29, page 35.
D[4:0] S[4:0]		Selector Field. Always 00001. Indicates to its link partner that it is an IEEE Std 802.3 device.	Register 4.[4:0] Table 29, page 35.
PAGE 0 (Message Next Page)			
M15 NP		Next Page. 1: Indicates that Next Page follows 0: Indicates that no Next Page follows	-
M14 Ack		Acknowledge. 1: Indicates that a device has successfully received its link partner Link Code Word (LCW)	- ’s
M13 MP		Message Page. 1: Indicates to its link partner that this is a message page, not an unformatted page	-
M12 Ack2		Acknowledge 2. 1: Indicates to its link partner that a device has the ability to comply with the message	-
M11 T		Toggle. Used by the NWay arbitration function to ensure synchronization with its link partner during Next Page exchange.	-
M[10:0]	-	1000Base-T Message Code. Always 8.	-
PAGE 1 (Unformatted Next Page)			
U15 NP		Next Page. 1: Indicates that Next Page follows 0: Indicates that no Next Page follows	-
U14 Ack		Acknowledge. 1: Indicates that a device has successfully received its link partner Link Code Word (LCW)	- ’s
U13 MP		Message Page. 1: Indicates to its link partner that this is a message page, not an unformatted page	-

Bit	Name	Bit Description	Register Location
U12 Ack2		Acknowledge 2. 1: Indicates to its link partner that a device has the ability to comply with the message	-
U11 T		Toggle. Used by the NWay arbitration function to ensure synchronization with its link partner during Next Page exchange.	-
U[10:5]	-	Reserved. Transmit as 0	-
U4	-	1000Base-T Half Duplex. 1: Half duplex 0: No half duplex	-
U3	-	1000Base-T Full Duplex. 1: Full duplex 0: No full duplex	-
U2	-	1000Base-T Port Type Bit. 1: Multi-port device 0: Single-port device	Register 9.10 (GBCR) Table 34, page 37.
U1	-	1000Base-T Master-Slave Manual Configuration Value. 1: Master 0: Slave This bit is ignored if bit 9.12=0	Register 9.11 (GBCR) Table 34, page 37.
U0	-	1000Base-T Master-Slave Manual Configuration Enable. 1: Manual Configuration Enable This bit is intended to be used for manual selection in Master-Slave mode, and is to be used in conjunction with bit 9.11	Register 9.12 (GBCR) Table 34, page 37.
PAGE 2 (Unformatted Next Page)			
U15 NP		Next Page. 1: Indicates that Next Page follows 0: Indicates that no Next Page follows	-
U14 Ack		Acknowledge. 1: Indicates that a device has successfully received its link partner Link Code Word (LCW)	- ’s
U13 MP		MessagePage. 1: Indicates to its link partner that this is a message page, not an unformatted page.	-
U12 Ack2		Acknowledge 2. 1: Indicates to its link partner that a device has the ability to comply with the message	-
U11 T		Toggle. Used by the NWay arbitration function to ensure synchronization with its link partner during Next Page exchange.	-
U[10:0]	-	1000Base-T Master-Slave Seed Bit[10:0]	Master-Slave Seed Value SB[10:0]

6.11.1. Auto-Negotiation Priority Resolution

Upon the start of auto-negotiation, to advertise its capabilities each station transmits a 16-bit packet called a Link Code Word (LCW), within a burst of 17 to 33 Fast Link Pulses (FLP). A device capable of auto-negotiation transmits and receives the FLPs. The receiver must identify three identical LCWs before the information is authenticated and used in the arbitration process. The devices decode the base LCW and select capabilities with the highest common denominator supported by both devices.

To advertise 1000Base-T capability, both link partners, sharing the same link medium, should engage in Next Page (1000Base-T Message Page, Unformatted Page 1, and Unformatted Page 2) exchange.

Auto-negotiation ensures that the highest priority protocol will be selected as the link speed based on the following priorities advertised through the Link Code Word (LCW) exchange. Refer to IEEE 802.3 Clause 28 for detailed information.

1. 1000Base-T Full Duplex (highest priority)

2. 1000Base-T Half Duplex

3. 100Base-Tx Full Duplex

4. 100Base-Tx Half Duplex

5. 10Base-T Full Duplex

6. 10Base-T Half Duplex (lowest priority)

6.11.2. Auto-Negotiation Master/Slave Resolution

To establish a valid 1000Base-T link, the Master/Slave mode of both link partners should be resolved through the auto-negotiation process:

Master Priority:

Multi-port > Single port

Manual > Non-manual

Determination of Master/Slave configuration from LCW:

Manual_MASTER=U0*U1

Manual_SLAVE=U0*!U1

Single-port device=!U0*!U2

Multi-port device=!U0*U2
Where: U0 is bit 0 of the Unformatted Page 1
U1 is bit 1 of the Unformatted Page 1
U2 is bit 2 of the Unformatted Page 1

Where there are two stations with the same configuration, the one with higher Master-Slave seed SB[10:0] in the unformatted page 2 shall become Master.

Master-Slave configuration process resolution:

Successful: Bit 10.15 Master-Slave Configuration Fault is set to logical 0, and bit 10.14 is set to logical 1 for Master resolution, or set to logical 0 for Slave resolution.

Unsuccessful: Auto-Negotiation restarts.

Fault Detect: Bit 10.15 is set to logical 1 to indicate that a configuration fault has been detected. Auto-Negotiation restarts automatically. This happens when both stations are set to manual Master mode or manual Slave mode, or after seven attempts to configure the Master-Slave relationship through the seed method has failed.

6.11.3. Auto-Negotiation PAUSE/ASYMMETRIC PAUSE Resolution

Auto-negotiation is also used to determine the flow control capability between link partners. Flow control is a mechanism that can force a busy transmitting link partner to stop transmitting in a full duplex environment by sending special MAC control frames. In IEEE 802.3u, a PAUSE control frame had already been defined, however, in IEEE 802.3ab, a new ASY-PAUSE control frame was defined; if the MAC can only generate PAUSE frames but is not able to respond to PAUSE frames generated by the link partner, then it is called ASYMMETRIC PAUSE.

PAUSE/ASYMMETRIC PAUSE capability can be configured by setting the ANAR bits 10 and 11 (Table 29, page 35). Link partner PAUSE capabilities can be determined from ANLPAR bits 10 and 11 (Table 30, page 35). A PHY layer device such as the RTL8211DN is not directly involved in PAUSE resolution, but simply advertises and reports PAUSE capabilities during the Auto-Negotiation process. The MAC is responsible for final PAUSE/ASYMMETRIC PAUSE resolution after a link is established, and is responsible for correct flow control actions thereafter.

6.12. Crossover Detection and Auto-Correction

Ethernet needs a crossover mechanism between both link partners to cross the transmit signal to the receiver when the medium is twisted-pair cable. Crossover Detection & Auto-Correction Configuration eliminates the need for crossover cables between devices, such as two PC ’s connected to ea CAT.5 Ethernet cable. The basic concept is to assume the initial default setting is MDI mode, and then check the link status. If no link is established after a certain time, change to MDI Crossover mode and repeat the process until a link is established. An 11-bit pseudo-random timer is applied to decide the mode change time interval.

Crossover Detection & Auto-Correction is not a part of the Auto-Negotiation process, but it utilizes the process to exchange MDI/MDI Crossover configuration. If the RTL8211DN is configured to only operate in 100Base-TX or only in 10Base-T mode, then Auto-Negotiation is disabled only if the Crossover Detection & Auto-Correction function is also disabled. If Crossover Detection & Auto-Correction are enabled, then Auto-Negotiation is enabled and the RTL8211DN advertises only 100Base-TX mode or 10Base-T mode. If the speed of operation is configured manually and Auto-Negotiation is still enabled because the Crossover Detection & Auto-Correction function is enabled, then the duplex advertised is as follows:

1. If CONFIG is set to half duplex, then only half duplex is advertised.

2. If CONFIG is set to full duplex, then both full and half duplex are advertised.

If the user wishes to advertise only full duplex at a particular speed with the Crossover Detection & Auto-Correction function enabled, then Auto-Negotiation should be enabled (register 0.12) with the appropriate advertising capabilities set in registers 4 or 9. The Crossover Detection & Auto-Correction function may be enabled/disabled by setting (register 16.6) manually.

After initial configuration following a hardware reset, Auto-Negotiation can be enabled and disabled via register 0.12, speed via registers 0.13, 0.6, and duplex via register 0.8. The abilities that are advertised can be changed via registers 4 and 9. Changes to registers 0.12, 0.13, 0.6, and 0.8 do not take effect unless at least one of the following events occurs:

? Software reset (register 0.15)

? Restart of Auto-Negotiation (register 0.9)

? Transition from power-down to power-up (register 0.11)

Registers 4 and 9 are internally latched once each time Auto-Negotiation enters the ABILITY DETECT state in the arbitration state machine (IEEE 802.3). Hence a write into register 4 or 9 has no effect once the RTL8211DN begins to transmit Fast Link Pulses.

Register 7 is treated in a similar manner as 4 and 9 during additional Next Page exchanges. Once the RTL8211DN completes Auto-Negotiation, it updates the various statuses in registers 1, 5, 6, and 10. The speed, duplex, page received, and Auto-Negotiation completed statuses are also available in registers 17 and 19.

6.13. LED Configuration

The RTL8211DN support four LED pins, suitable for multiple types of applications that can directly drive the LEDs. The output of these pins is determined by setting the corresponding bits in extension Page44 Register 28. The functionality of the RTL8211DN LEDs is shown in Table 19.

Table 19. LED Default Definitions

Pin	Description
LED0 Blinking	Transmitting or Receiving
LED1	Low=Link Up (Any speed) High=Link Down (Any speed)
LED2	Low=Link Up (Any speed) High=Link Down (Any speed) Blinking=Transmitting or Receiving
LED3	Low=Link Up (Fiber mode) High=Link Down (Fiber mode) Blinking=Transmitting or Receiving (Fiber mode)

Note: When in EEE mode, blinking duration is 400ms ON and 2 seconds OFF.

The RTL8211DN LED pins can be customized from extension Page44 Register 28 and Register 26. To change the register page, see note (below) and Table 20. There are 24 configuration types (see Table 21, page 28).

Note: To switch to extension Page44, Write Register 31 Data= 0x0007 (set to extension page). Write Register 30 Data=0x002c (extension Page44). After LED setting, switch to the PHY's Page0 (Register 31 Data=0000).

Table 20. LED Register Table

	LINK Speed				Active (Tx/Rx)
	10Mbps	100Mbps	1000Mbps	Fiber	
LED0	Reg28 Bit0	Reg28 Bit1	Reg28 Bit2	Reg28 Bit3	Reg26 Bit4
LED1	Reg28 Bit4	Reg28 Bit5	Reg28 Bit6	Reg28 Bit7	Reg26 Bit5
LED2	Reg28 Bit8	Reg28 Bit9	Reg28 Bit10	Reg28 Bit11	Reg26 Bit6
LED3	Reg28 Bit12	Reg28 Bit13	Reg28 Bit14	Reg28 Bit15	Reg26 Bit7

Table 21. LED Configuration Table

Pin	LINK Bit				Active (Tx/Rx) Bit	Description
	10	100	1000	Fiber		
LED	0 0 0 0				0	N/A (LED Always Dark)
	0 0 0 0				1	Active
	1 0 0 0				0	Link 10
	1 0 0 0				1	Link 10+Active
	0 1 0 0				0	Link 100
	0 1 0 0				1	Link 100+Active
	1 1 0 0				0	Link 10/100
	1 1 0 0				1	Link 100/100+Active
	0 0 1 0				0	Link 1000
	0 0 1 0				1	Link 1000+Active
	1 0 1 0				0	Link 10/1000
	1 0 1 0				1	Link 10/1000+Active
	0 1 1 0				0	Link 100/1000
	0 1 1 0				1	Link 100/1000+Active
	1 1 1 0				0	Link 10/100/1000
	1 1 1 0				1	Link 10/100/1000+Active
	0 0 0 1				1	Fiber Active
	0 0 0 1				0	N/A (LED Always Dark)
	1 0 0 1				1	Fiber Link/Fiber Active
	1 0 0 1				0	Fiber Link
	0 1 0 1				0	Fiber Link
	0 1 0 1				1	Fiber Link/Fiber TX
	1 1 0 1				0	Fiber Link
	1 1 0 1				1	Fiber Link/Fiber RX

6.14. Polarity Correction

The RTL8211DN automatically corrects polarity errors on the receive pairs in 1000Base-T and 10Base-T modes. In 100Base-TX mode polarity is irrelevant. In 1000Base-T mode, receive polarity errors are automatically corrected based on the sequence of idle symbols. Once the descrambler is locked, the polarity is also locked on all pairs. The polarity becomes unlocked only when the receiver loses lock. In 10Base-T mode, polarity errors are corrected based on the detection of validly spaced link pulses. The detection begins during the MDI crossover detection phase and locks when the 10Base-T link is up. The polarity becomes unlocked when the link is down.

6.15. Power

The RTL8211DN implements a switching regulator to generate operating power. The system vendor needs to supply a 3.3V, 1A steady power source. The RTL8211DN converts the 3.3V steady power source to 1.05V via a switching regulator.

Another possible implementation is to use an external regulator to generate 1.0V. Be sure that the regulator meets the required current rate.

The RTL8211DN implements an option for the (R)GMII power pins. The standard I/O voltage of the (R)GMII interface is 3.3V, with support for 2.5V to lower EMI. The 2.5V power source for (R)GMII is from an external regulator.

7. Register Descriptions

7.1. Page0 Register Mapping and Definitions

Table 22. Page0 Register Mapping and Definitions

Offset	Access	Name	Description
0	RW	BMCR	Basic Mode Control Register.
1	RO	BMSR	Basic Mode Status Register.
2	RO	PHYID1	PHY Identifier Register 1.
3	RO	PHYID2	PHY Identifier Register 2.
4 RW		ANAR	Auto-Negotiation Advertising Register.
5	RW	ANLPAR	Auto-Negotiation Link Partner Ability Register.
6	RW	ANER	Auto-Negotiation Expansion Register.
7 RW		ANNPTR Auto-Negotiation	Next Page Transmit Register.
8 RW		ANNPRR Auto-Negotiation	Next Page Receive Register.
9	RW	GBCR	1000Base-T Control Register.
10	RO	GBSR	1000Base-T Status Register.
11~12 RW		RSVD	Reserved.
13	WO	MACR	MMD Access Control Register.
14	RW	MAADR	MMD Access Address Data Register.
15	RO	GBESR	1000Base-T Extended Status Register.
16	RW	PHYCR	PHY Specific Control Register.
17	RO	PHYSR	PHY Specific Status Register.
18	RW	INER	Interrupt Enable Register.
19	RO	INSR	Interrupt Status Register.
24	RO	RXERC	Receive Error Counter.
25~30 RW		RSVD	Reserved.
31	RW	PAGSEL	Page Select Register.

Note: To switch to extension Page44, set Register 31 Data=0x0007 (set to extension page). Set Register 30 Data=0x002c (extension Page44). After setting, switch to PHY's Page0 (Register 31 Data=0000).

7.2. Extension Page Register Mapping and Definition

Table 23. Extension Page Register Mapping and Definition

ExtPage	Offset	Access	Name	Description
140 22	RW		SDSR	SerDesRegister.

7.3. MMD Register Mapping and Definition

Table 24. MMD Register Mapping and Definition

Device	Offset	Access	Name	Description
3	0	RW	PC1R	PCS Control 1 Register.
3	1	RW	PS1R	PCS Status 1 Register.
3	20	RO	EEECR	EEE Capability Register.
3	22	RC	EEEWER	EEE Wake Error Register.
7 60		RW	EEEAR	EEE Advertisement Register.
7	61	RO	EEELPAR	EEE Link Partner Ability Register.

7.4. Register Table

7.4.1. BMCR (Basic Mode Control Register, Address 0x00)

Table 25. BMCR (Basic Mode Control Register, Address 0x00)

Bit	Name	RW	Default	Description
0.15	Reset	RW, SC[1]	0	Reset. 1: PHY reset 0: Normal operation Register 0 (BMCR) and register 1 (BMSR) will return to default values after a software reset (set Bit15 to 1). This action may change the internal PHY state and the state of the physical link associated with the PHY.
0.14	Loopback	RW	0	Loopback Mode for 10M &100M. 1: Enable PCS loopback mode 0: Disable PCS loopback mode
0.13	Speed[0]	RW	0	Speed Select Bit 0. In forced mode, i.e., when Auto-Negotiation is disabled, bits 6 and 13 determine device speed selection.
0.12	ANE	RW	1	Auto-Negotiation Enable Bit. 1: Enable Auto-Negotiation 0: Disable Auto-Negotiation
0.11	PWD	RW	0	Power Down. 1: Power down (only Management Interface and logic active, link is down) 0: Normal operation

Speed[1]	Speed[0]	Speed Enabled
1	1	Reserved
1	0	Reserved
0	1	100Mbps
0	0	10Mbps

Bit	Name	RW	Default	Description
0.10	Isolate	RW	0	Isolate. 1: RGMII/GMII interface is isolated; the serial management interface (MDC, MDIO) is still active. When this bit is asserted, the RTL8211DN ignores TXD[7:0], and TXCLT inputs, and presents a high impedance on TXC, RXC, RXCLT, RXD[7:0]. 0: Normal operation
0.9	Restart_AN	RW, SC	0	RestartAuto-Negotiation. 1: Restart Auto-Negotiation 0: Normal operation
0.8	Duplex	RW	1	Duplex Mode. 1: Full Duplex operation 0: Half Duplex operation This bit is valid only in force mode, i.e., NWay is disabled.
0.7	Collision Test	RW	0	Collision Test. 1: Collision test enabled 0: Normal operation
0.6	Speed[1]	RW	1	Speed Select bit 1. Refer to bit 0.13.
0.5:0	RSVD	RO	000000	Reserved.

Note 1: SC: Self-cleared

Note 2: The power-on duplex, speed, and ANE values take on the values set by external pins AN[3:0] on hardware reset only. A write to these registers has no effect unless any one of the following also occurs: Software reset (0.15) is asserted, Restart_AN (0.9) is asserted, or PWD (0.11) transitions from power down to normal operation.

Note 3: When the RTL8211DN is switched from power down to normal operation, a software reset and restart auto-negotiation are performed even if bits Reset (0.15) and Restart_AN (0.9) are not set by the user.

Note 4: Auto-Negotiation is enabled when speed is set to 1000Base-T. Crossover Detection & Auto-Correction takes precedence over Auto-Negotiation disable (0.12=0). If ANE is disabled, speed and duplex capabilities are advertised by 0.13, 0.6, and 0.8. Otherwise, register 4.8:5 and 9.9:8 take effect.

Note 5: Auto-Negotiation automatically restarts after hardware or software reset regardless of whether or not the restart bit (0.9) is set.

7.4.2. BMSR (Basic Mode Status Register, Address 0x01)

Table 26. BMSR (Basic Mode Status Register, Address 0x01)

Bit	Name	RW	Default	Description
1.15	100Base-T4	RO	0	100Base-T4 Capability. The RTL8211DN does not support 100Base-T4 mode. This bit should always be 0.
1.14	100Base-TX (Full)	RO	1	100Base-TX Full Duplex Capability. 1: Device is able to perform 100Base-TX in full duplex mode 0: Device is not able to perform 100Base-TX in full duplex mode
1.13	100Base-TX (Half)	RO	1	100Base-TX Half Duplex Capability. 1: Device is able to perform 100Base-TX in half duplex mode 0: Device is not able to perform 100Base-TX in half duplex mode
1.12	10Base-T (Full)	RO	1	10Base-T Full Duplex Capability. 1: Device is able to perform 10Base-T in full duplex mode. 0: Device is not able to perform 10Base-T in full duplex mode.
1.11	10Base-T (Half)	RO	1	10Base-T Half Duplex Capability. 1: Device is able to perform 10Base-T in half duplex mode 0: Device is not able to perform 10Base-T in half duplex mode
1.10	100Base-T2 (Full)	RO	0	100Base-T2 Full Duplex Capability. The RTL8211DN does not support 100Base-T2 mode and this bit should always be 0.
1.9	100Base-T2 (Half)	RO	0	100Base-T2 Half Duplex Capability. The RTL8211DN does not support 100Base-T2 mode. This bit should always be 0.
1.8	1000Base-T Extended Status	RO	1	1000Base-T Extended Status Register. 1: Device supports Extended Status Register 0x0F (15) 0: Device does not support Extended Status Register 0x0F This register is read-only and is always set to 1.
1.7	RSVD	RO	0	Reserved.
1.6	Preamble Suppression	RO	1	Preamble Suppression Capability (Permanently On). The RTL8211DN always accepts transactions with preamble suppressed.
1.5	Auto-Negotiation Complete	RO	0	Auto-Negotiation Complete. 1: Auto-Negotiation process complete, and contents of registers 5, 6, 8, and 10 are valid 0: Auto-Negotiation process not complete
1.4	Remote Fault	RC*	0	Remote Fault. 1: Remote fault condition detected (cleared on read or by reset). Indication or notification of remote fault from Link Partner 0: No remote fault condition detected
1.3	Auto-Negotiation Ability	RO	1	Auto Configured Link. 1: Device is able to perform Auto-Negotiation 0: Device is not able to perform Auto-Negotiation

Bit	Name	RW	Default	Description
1.2	Link Status	RO	0	Link Status. 1: Linked 0: Not Linked This register indicates whether the link was lost since the last read. For the current link status, either read this register twice or read register bit 17.10 Link Real Time.
1.1	Jabber Detect	RC	0	Jabber Detect. 1: Jabber condition detected 0: No Jabber occurred
1.0	Extended Capability	RO	1	1: Extended register capabilities, always 1

Note: RC: Read-cleared after read.

7.4.3. PHYID1 (PHY Identifier Register 1, Address 0x02)

Table 27. PHYID1 (PHY Identifier Register 1, Address 0x02)

Bit	Name	RW	Default	Description
2.15:0	OUI_MSB	RO	0000000000011100	Organizationally Unique Identifier Bit 3:18. Always 0000000000011100.

Note: Realtek OUI is 0x000732.

7.4.4. PHYID2 (PHY Identifier Register 2, Address 0x03)

Table 28. PHYID2 (PHY Identifier Register 2, Address 0x03)

Bit	Name	RW	Default	Description
3.15:10	OUI_LSB	RO	110010	Organizationally Unique Identifier Bit 19:24. Always 110010.
3.9:4	Model Number	RO	010001	Manufacture ’s Model Number
3.3:0	Revision Number	RO	0100	Revision Number

7.4.5. ANAR (Auto-Negotiation Advertising Register, Address 0x04)

Table 29. ANAR (Auto-Negotiation Advertising Register, Address 0x04)

Bit	Name	RW	Default	Description
4.15	NextPage	RW	0	1: Additional next pages exchange desired 0: No additional next pages exchange desired
4.14	RSVD	RO	0	Reserved.
4.13	Remote Fault	RW	0	1: Set Remote Fault bit 0: No remote fault detected
4.12	RSVD	RO	0	Reserved.
4.11	Asymmetric PAUSE	RW	0	1: Advertise support for asymmetric pause 0: No support for asymmetric pause
4.10	PAUSE	RW	0	1: Advertise support of pause frames 0: No support of pause frames
4.9	100Base-T4	RO	1	1: 100Base-T4 support 0: 100Base-T4 not supported
4.8	100Base-TX (Full)	RW	1	1: Advertise support of 100Base-TX full-duplex mode 0: Not advertised
4.7	100Base-TX (Half)	RW	1	1: Advertise support of 100Base-TX half-duplex mode 0: Not advertised
4.6	10Base-T (Full)	RW	1	1: Advertise support of 10Base-TX full-duplex mode 0: Not advertised
4.5	10Base-T (Half)	RW	1	1: Advertise support of 10Base-TX full-duplex mode 0: Not advertised
4.4:0	Selector Field	RO	00001	Indicates the RTL8211DN supports IEEE 802.3

Note 1: The setting of Register 4 has no effect unless NWay is restarted or the link goes down.
Note 2: If 1000Base-T is advertised, then the required next pages are automatically transmitted. Register 4.15 should be set to 0 if no additional next pages are needed.

7.4.6. ANLPAR (Auto-Negotiation Link Partner Ability Register, Address 0x05)

Table 30. ANLPAR (Auto-Negotiation Link Partner Ability Register, Address 0x05)

Bit	Name	RW	Default	Description
5.15	Next Page	RO	0	Next Page Indication. Received Code Word Bit 15.
5.14	ACK	RO	0	Acknowledge. Received Code Word Bit 14.
5.13	Remote Fault	RO	0	Remote Fault indicated by Link Partner. Received Code Word Bit 13.
5.12:5	Technology Ability Field	RO	00000000	Received Code Word Bit 12:5.
5.4:0	Selector Field	RO	00000	Received Code Word Bit 4:0.

Note: Register 5 is not valid until the Auto-Negotiation complete bit 1.5 indicates completed.

7.4.7. ANER (Auto-Negotiation Expansion Register, Address 0x06)

Table 31. ANER (Auto-Negotiation Expansion Register, Address 0x06)

Bit	Name	RW	Default	Description
6.15:5	RSVD	RO	0x000	Reserved.
6.4	Parallel Detection Fault	RC	0	1: A fault has been detected via the Parallel Detection function 0: A fault has not been detected via the Parallel Detection function
6.3	Link Partner Next Pageable	RO	0	1: Link Partner supports Next Page exchange 0: Link Partner does not support Next Page exchange
6.2	Local Next Pageable	RO	1	1: Local Device is able to send Next Page Always 1.
6.1	Page Received	RC	0	1: A New Page (new LCW) has been received 0: A New Page has not been received
6.0	Link Partner Auto-Negotiation Capable	RO	0	1: Link Partner supports Auto-Negotiation 0: Link Partner does not support Auto-Negotiation

Note: Register 6 is not valid until the Auto-Negotiation complete bit 1.5 indicates completed.

7.4.8. ANNPTR (Auto-Negotiation Next Page Transmit Register, Address 0x07)

Table 32. ANNPTR (Auto-Negotiation Next Page Transmit Register, Address 0x07)

Bit	Name	RW	Default	Description
7.15	Next Page	RW	0	Next Page Indication. 0: No more next pages to send 1: More next pages to send Transmit Code Word Bit 15.
7.14	RSVD	RO	0	Transmit Code Word Bit 14.
7.13	Message Page	RW	1	Message Page. 0: Unformatted Page 1: Message Page Transmit Code Word Bit 13.
7.12	Acknowledge 2	RW	0	Acknowledge2. 0: Local device has no ability to comply with the message received 1: Local device has the ability to comply with the message received Transmit Code Word Bit 12.
7.11	Toggle	RO	0	Toggle Bit. Transmit Code Word Bit 11.
7.10:0	Message/ Unformatted Field	RW	0x001	Content of Message/Unformatted Page. Transmit Code Word Bit 10:0.

7.4.9. ANNPRR (Auto-Negotiation Next Page Receive Register, Address 0x08)

Table 33. ANNPRR (Auto-Negotiation Next Page Receive Register, Address 0x08)

Bit	Name	RW	Default	Description
8.15	Next Page	RO	0	Received Link Code Word Bit 15.
8.14	Acknowledge	RO	0	Received Link Code Word Bit 14.
8.13	Message Page	RO	0	Received Link Code Word Bit 13.
8.12	Acknowledge 2	RO	0	Received Link Code Word Bit 12.
8.11	Toggle	RO	0	Received Link Code Word Bit 11.
8.10:0	Message/Unformatted Field	RO	0x00	Received Link Code Word Bit 10:0.

Note: Register 8 is not valid until the Auto-Negotiation complete bit 1.5 indicates completed.

7.4.10. GBCR (1000Base-T Control Register, Address 0x09)

Table 34. GBCR (1000Base-T Control Register, Address 0x09)

Bit	Name	RW	Default	Description
9.15:13	Test Mode	RW	0	Test Mode Select. 000: Normal Mode 001: Test Mode 1 - Transmit Jitter Test 010: Test Mode 2 - Transmit Jitter Test (MASTER mode) 011: Test Mode 3 - Transmit Jitter Test (SLAVE mode) 100: Test Mode 4 - Transmit Distortion Test 101, 110, 111: Reserved
9.12	MASTER/SLAVE Manual Configuration Enable	RW	0	Enable Manual Master/Slave Configuration. 1: Manual MASTER/SLAVE configuration 0: Automatic MASTER/SLAVE
9.11	MASTER/SLAVE Configuration Value	RW	0	Advertise Master/Slave Configuration Value. 1: Manual configuration as MASTER 0: Manual configuration as SLAVE
9.10	Port Type	RW	0	Advertise Device Type Preference. 1: Prefer multi-port device (MASTER) 0: Prefer single-port device (SLAVE)
9.9	1000Base-T Full Duplex	RW	1	Advertise 1000Base-T Full Duplex Capability. 1: Advertise 0: Do not advertise
9.8	RSVD	RW	1	Reserved.
9.7:0	RSVD	RO	0	Reserved.

Note 1: Values set in register 9.12:9 have no effect unless Auto-Negotiation is restarted (Reg0.9) or the link goes down.
Note 2: Bits 9.11 and 9.10 are ignored when bit 9.12=0.

7.4.11. GBSR (1000Base-T Status Register, Address 0x0A)

Table 35. GBSR (1000Base-T Status Register, Address 0x0A)

Bit	Name	RW	Default	Description
10.15	MASTER/SLAVE Configuration Fault	RO, RC	0	Master/Slave Manual Configuration Fault Detected. 1: MASTER/SLAVE configuration fault detected 0: No MASTER/SLAVE configuration fault detected
10.14	MASTER/SLAVE Configuration Resolution	RO	0	Master/Slave Configuration Result. 1: Local PHY configuration resolved to MASTER 0: Local PHY configuration resolved to SLAVE
10.13	Local Receiver Status	RO	0	Local Receiver Status. 1: Local Receiver OK 0: Local Receiver Not OK
10.12	Remote Receiver Status	RO	0	Remote Receiver Status. 1: Remote Receiver OK 0: Remote Receiver Not OK
10.11	Link Partner 1000Base-T Full Duplex Capability	RO	0	Link Partner 1000Base-T Full Duplex Capability. 1: Link Partner is capable of 1000Base-T full duplex 0: Link Partner is not capable of 1000Base-T full duplex
10.10	Link Partner 1000Base-T Half Duplex Capability	RO	0	Link Partner 1000Base-T Half Duplex Capability. 1: Link Partner is capable of 1000Base-T half duplex 0: Link Partner is not capable of 1000Base-T half duplex
10.9:8	RSVD	RO	00	Reserved.
10.7:0	Idle Error Count	RO, RC	0x00	MSB of Idle Error Counter. The counter stops automatically when it reaches 0xff.

Note 1: Values set in register 10.11:10 are not valid until register 6.1 is set to 1.

Note 2: Register 10 is not valid until the Auto-Negotiation complete bit 1.5 indicates completed.

7.4.12. MACR (MMD Access Control Register, Address 0x0D)

Table 36. MACR (MMD Access Control Register, Address 0x0D)

Bit	Name	RW	Default	Description
13.15:14	Function	WO	0 00:	Address 01: Data with no post increment 10: Data with post increment on reads and writes 11: Data with post increment on writes only
13.13:5	RSVD	RO	000000000	Reserved.
13.4:0	DEVAD	WO	0	Device Address.

Note 1: This register is used in conjunction with the MAADR (Register 14) to provide access to the MMD address space.

Note 2: If the MAADR accesses for address (Function=00), then it is directed to the address register within the MMD associated with the value in the DEVAD field.

Note 3: If the MAADR accesses for data (Function≠00), both the DEVAD field and MMD s address register direct the MAADR data accesses to the appropriate registers within the MMD.

7.4.13. MAADR (MMD Access Address Data Register, Address 0x0E)

Table 37. MAADR (MMD Access Address Data Register, Address 0x0E)

Bit	Name	RW	Default	Description
14.15:0	Address Data	RW	0x0000	13.15:14 = 00 ? MMD DEV AD’s address register 13.15:14 = 01, 10, or 11 ? MMD DEV AD’s data register as indicated by the contents of its address register

Note: This register is used in conjunction with the MACR (Register 13) to provide access to the MMD address space.

7.4.14. GBESR (1000Base-T Extended Status Register, Address 0x0F)

Table 38. GBESR (1000Base-T Extended Status Register, Address 0x0F)

Bit	Name	RW	Default	Description
15.15	1000Base-X FD	RO	0	0: Not 1000Base-X full duplex capable
15.14	1000Base-X HD	RO	0	0: Not 1000Base-X half duplex capable
15.13	1000Base-T FD	RO	1	1: 1000Base-T full duplex capable
15.12	1000Base-T HD	RO	1	1: 1000Base-T half duplex capable
15.11:0	RSVD	RO	0x000	Reserved.

7.4.15. PHYCR (PHY Specific Control Register, Address 0x10)

Table 39. PHYCR (PHY Specific Control Register, Address 0x10)

Bit	Name	RW	Default	Description
16.15	Disable RXC	RW	0	Disable RXC Clock Output.
16.14:12	Select FPR Fail	RW	000	Select Signal for ‘LPRFAIL’ (10M Link Pulse Receive Status).
16.11	Assert CRS on Transmit	RW	1	1: Assert CRS on transmit 0: Never assert CRS on transmit
16.10	Force Link Good	RW	0	1: Force link good 0: Normal operation
16.9:8	RSVD	RW	01	Reserved.
16.7	RSVD	RW	0	Reserved.
16.6	Enable Crossover	RW	1	1: Enable Auto-crossover mechanism
16.5	MDI Mode	RW	1	Used to Determine MDI/MDIX Mode when Disable Auto-Crossover. 0: MDI mode 1: MDIX mode
16.4	Disable CLK125	RW	0	1: CLK125 remains at logic Low 0: CLK125 Toggling Enabled
16.3:1	RSVD	RW	111	Reserved.
16.0	Disable Jabber	RW	0	1: Disable jabber function 0: Enable jabber function

7.4.16. PHYSR (PHY Specific Status Register, Address 0x11)

Table 40. PHYSR (PHY Specific Status Register, Address 0x11)

Bit	Name	RW	Default	Description
17.15:14	Speed	RO	01	Link Speed. 11: Reserved 10: 1000Mbps 01: 100Mbps 00: 10Mbps
17.13	Duplex	RO	0	Full/Half Duplex Mode. 1: Full duplex 0: Half duplex
17.12	Page Received	RC	0	New Page Received. 1: Page received 0: Page not received
17.11	Speed and Duplex Resolved	RO	0	Speed and Duplex Mode Resolved. 1: Resolved 0: Not resolved
17.10	Link (Real Time)	RO	0	Real Time Link Status. 1: Link OK 0: Link not OK
17.9:7	RSVD	RO	000	Reserved.
17.6	MDI Crossover Status	RO	0	MDI/MDI Crossover Status. 1: MDI Crossover 0: MDI
17.5:1	RSVD	RW	01110	Reserved.
17.0	Jabber (Real Time)	RO	0	Real Time Jabber Indication. 1: Jabber Indication 0: No jabber Indication

7.4.17. INER (Interrupt Enable Register, Address 0x12)

Table 41. INER (Interrupt Enable Register, Address 0x12)

Bit	Name	RW	Default	Description
18.15	Auto-Negotiation Error Interrupt	RW	1	1: Interrupt enable 0: Interrupt disable
18.14	Speed Change Interrupt	RW	1	1: Interrupt enable 0: Interrupt disable
18.13	Duplex Mode Change Interrupt	RW	1	1: Interrupt enable 0: Interrupt disable
18.12	Page Received Interrupt	RW	1	1: Interrupt enable 0: Interrupt disable
18.11	Auto-Negotiation Completed Interrupt	RW	1	1: Interrupt enable 0: Interrupt disable
18.10	Link Status Change Interrupt	RW	1	1: Interrupt enable 0: Interrupt disable
18.9	Symbol Error Interrupt	RW	1	1: Interrupt enable 0: Interrupt disable
18.8	False Carrier Interrupt	RW	1	1: Interrupt enable 0: Interrupt disable
18.7	RSVD	RW	1	Reserved.
18.6	MDI Crossover Change Interrupt	RW	1	1: Interrupt enable 0: Interrupt disable
18.5:2	RSVD	RW	1	Reserved.
18.1	Polarity Change Interrupt	RW	1	1: Interrupt enable 0: Interrupt disable
18.0	Jabber Interrupt	RW	1	1: Interrupt enable 0: Interrupt disable

7.4.18. INSR (Interrupt Status Register, Address 0x13)

Table 42. INSR (Interrupt Status Register, Address 0x13)

Bit	Name	RW	Default	Description
19.15	Auto-Negotiation Error	RC	0	1: Auto-Negotiation Error 0: No Auto-Negotiation Error
19.14	Speed Change	RC	0	1: Link speed changed 0: Link speed not changed
19.13	Duplex Mode Change	RC	0	1: Duplex mode changed 0: Duplex mode not changed
19.12	Page Received	RC	0	1: Page (a new LCW) received 0: Page not received
19.11	Auto-Negotiation Completed	RC	0	1: Auto-Negotiation completed 0: Auto-Negotiation not completed
19.10	Link Status Change	RC	0	1: Link status changed 0: Link status not changed
19.9	Symbol Error	RC	0	1: Symbol error detected 0: No symbol error detected
19.8	False Carrier	RC	0	1: False carrier 0: No false carrier detected
19.7 RSVD		RC	0	Reserved.
19.6	MDI Crossover Change	RC	0	1: Crossover status changed 0: Crossover status not changed
19.5:2 RSVD		RC	0000	Reserved.
19.1	Polarity Change	RC	0	1: Polarity Changed 0: Polarity not changed Note: This bit is valid only when 1000Base-T is enabled.
19.0	Jabber	RC	0	1: Jabber detected 0: No jabber detected

7.4.19. RXERC (Receive Error Counter, Address 0x18)

Table 43. RXERC (Receive Error Counter, Address 0x18)

Bit	Name	RW	Default	Description
24.15:0	Receive Error Count	RC	0x0000	Receive Error Count.

Note: The RXERC register is read-cleared after a read.

7.4.20. PAGSEL (Page Select Register, Address 0x1F)

Table 44. PAGSEL (Page Select Register, Address 0x1F)

Bit	Name	RW	Default	Description
31.15:3	RSVD	RW	0	Reserved.
31.2:0	Pagesel	RW	000	Page Select Signal. 000: Page 0 (default page) 001: Page 1 010: Page 2 011: Page 3 100: Page 4 101: Page 5 110: Page 6 111: Extension page

7.4.21. SDSR (SerDes Register, ExtPage 140, Address 0x16)

Table 45. SDSR (SerDes Register, ExtPage 140, Address 0x16)

Bit	Name	RW	Default	Description
22.13:12	SerDes Speed	RW	0	Bridge Mode Speed Select for SGMII Mode. 00: 10Mbps 01: 100Mbps 10: 1000Mbps

7.4.22. PC1R (PCS Control 1 Register, MMD Device 3, Address 0x00)

Table 46. PC1R (PCS Control 1 Register, MMD Device 3, Address 0x00)

Bit	Name	RW	Default	Description
3.0.15:11	RSVD	RW	0	Reserved.
3.0.10	Clock Stop Enable	RW	0	1: PHY stops RXC in LPI 0: RXC not stoppable
3.0.9:0	RSVD	RW	0	Reserved.

7.4.23. PS1R (PCS Status1 Register, MMD Device 3, Address 0x01)

Table 47. PS1R (PCS Status 1 Register, MMD Device 3, Address 0x01)

Bit	Name	RW	Default	Description
3.1.15:12	RSVD	RO	0	Reserved.
3.1.11	TX LPI received	RO, LH	0	1: TX PCS has received LPI 0: LPI not received
3.1.10	RX LPI received	RO, LH	0	1: RX PCS has received LPI 0: LPI not received
3.19	TX LPI indication	RO	0	1: TX PCS is currently receiving LPI 0: TX PCS is not currently receiving LPI
3.1.8	RX LPI indication	RO	0	1: RX PCS is currently receiving LPI 0: RX PCS is not currently receiving LPI
3.1.7:0	RSVD	RO	0	Reserved

7.4.24. EEECR (EEE Capability Register, MMD Device 3, Address 0x14)

Table 48. EEECR (EEE Capability Register, MMD Device 3, Address 0x14)

Bit	Name	RW	Default	Description
3.20.15:3	RSVD	RO	0	Reserved.
3.20.2	1000BASE-T EEE	RO	1	1: EEE is supported for 1000Base-T EEE 0: EEE is not supported for 1000Base-T EEE
3.20.1	100BASE-TX EEE	RO	1	1: EEE is supported for 100Base-TX EEE 0: EEE is not supported for 100Base-TX EEE
3.20.0	RSVD	RO	0	Reserved.

7.4.25. EEEWER (EEE Wake Error Register, MMD Device 3, Address 0x16)

Table 49. EEEWER (EEE Wake Error Register, MMD Device 3, Address 0x16)

Bit	Name	RW	Default	Description
3.22.15:0	EEE Wake Error Counter	RC	0	Used by PHY types that support EEE to count wake time faults where the PHY fails to complete its normal wake sequence within the time required for the specific PHY type.

7.4.26. EEEAR (EEE Advertisement Register, MMD Device 7, Address 0x3c)

Table 50. EEEAR (EEE Advertisement Register, MMD Device 7, Address 0x3c)

Bit	Name	RW	Default	Description
7.60.15:3	RSVD	RW	0	Reserved.
7.60.2	1000BASE-T EEE	RW	1	Advertise 1000Base-T EEE Capability. 1: Advertise 0: Do not advertise
7.60.1	100BASE-TX EEE	RW	1	Advertise 100Base-TX EEE Capability. 1: Advertise 0: Do not advertise
7.60.0	RSVD	RW	0	Reserved.

7.4.27. EEELPAR (EEE Link Partner Ability Register, MMD Device 7, Address 0x3d)

Table 51. EEELPAR (EEE Link Partner Ability Register, MMD Device 7, Address 0x3d)

Bit	Name	RW	Default	Description
7.61.15:3	RSVD	RO	0	Reserved.
7.61.2	LP 1000BASE-T EEE	RO	0	1: Link Partner is capable of 1000Base-T EEE 0: Link Partner is not capable of 1000Base-T EEE
7.61.1	LP 100BASE-TX EEE	RO	0	1: Link Partner is capable of 100Base-TX EEE 0: Link Partner is not capable of 100Base-TX EEE
7.61.0	RSVD	RO	0	Reserved.

8. Switching Regulator

The RTL8211DN incorporates a state-of-the-art switching regulator that requires a well-designed PCB layout in order to achieve good power efficiency and lower the output voltage ripple and input overshoot. The 1.05V switching regulator output pin (REG_OUT) should be connected only to DVDD10 and AVDD10 (do not provide this power source to other devices).

8.1. PCB Layout

? The input 3.3V power trace connected to VDDREG must be wider than 40mils

? The bulk de-coupling capacitors (Cin1 and Cin2) must be placed within 200mils (0.5cm) of VDDREG to prevent input voltage overshoot

? The output power trace out of REG_OUT must be wider than 60mils

? Lx (4.7 μ H) must be kept within 200mils (0.5cm) of REGOUT

? Cout1 and Cout2 must be kept within 200mils (0.5cm) of Lx to ensure stable output power and better power efficiency

? For switching regulator stability, the capacitor Cout1 and Cout2 must be a ceramic (X5R) capacitor. Cin1 and Cin2 are recommended to be ceramic capacitors

? Place Lx and Cin1 on the same layer as the RTL8211DN. Do not use vias on VDDREG and REG_OUT traces

Note: Violation of the above rules will damage the IC.

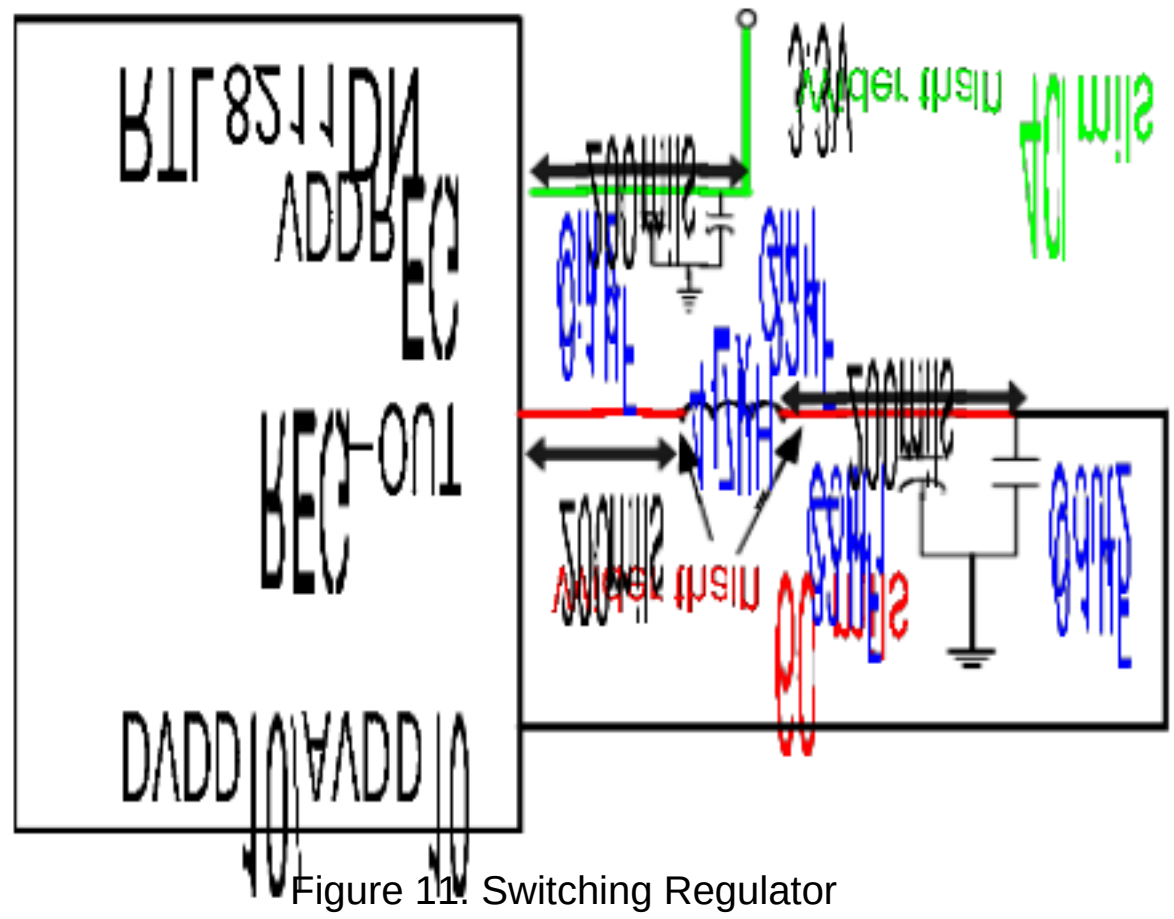


Figure 11. Switching Regulator

8.2. Inductor and Capacitor Parts List

Table 52. Inductor and Capacitor Parts List

Inductor Type	Inductance	ESR at 1MHz (m ?)	Max I (mA)
4R7GTSD32 4.7 µ H		712	1100

Note 1: The ESR is equivalent to RDC or DCR. Lower ESR inductor values will promote a higher-efficiency switching regulator.

Note 2: The power inductor used by the switching regulator should be able to withstand 600mA of current.

Note 3: Typically, if the power inductors ESR at 1MHž is below 0.3, the switching regulator efficiency will be above 75%. However the actual switching regulator efficiency should be measured according to the method described in section 8.4 Efficiency Measurement, page 50.

Note 4: If the inductor does not meet this requirement, it may damage the switching regulator. Refer to the RTL8211D_DG_DN inductor Approved Vendor List (AVL) for details.

Capacitor Type	Capacitance	ESR at 1MHz (m ?)
22 µ F 1210 X5R	22.15 µ F	24.90

Note: Cout1 and Cin1 must be X5R ceramic. Capacitors Cout2 and Cin2 are suggested to be ceramic, as lower ESR values will yield lower output voltage ripple.

8.3. Measurement Criteria

In order for the switching regulator to operate properly, the input and output voltage measurement criteria must be met. From the input side, the voltage overshoot cannot exceed 4V; otherwise the chip may be damaged. Note that the voltage signal must be measured directly at VDDREG, not at the capacitor. In order to reduce the input voltage overshoot, Cin1 and Cin2 must be placed close (< 200mils) to VDDREG. The following figures show what a good input voltage and a bad one look like.

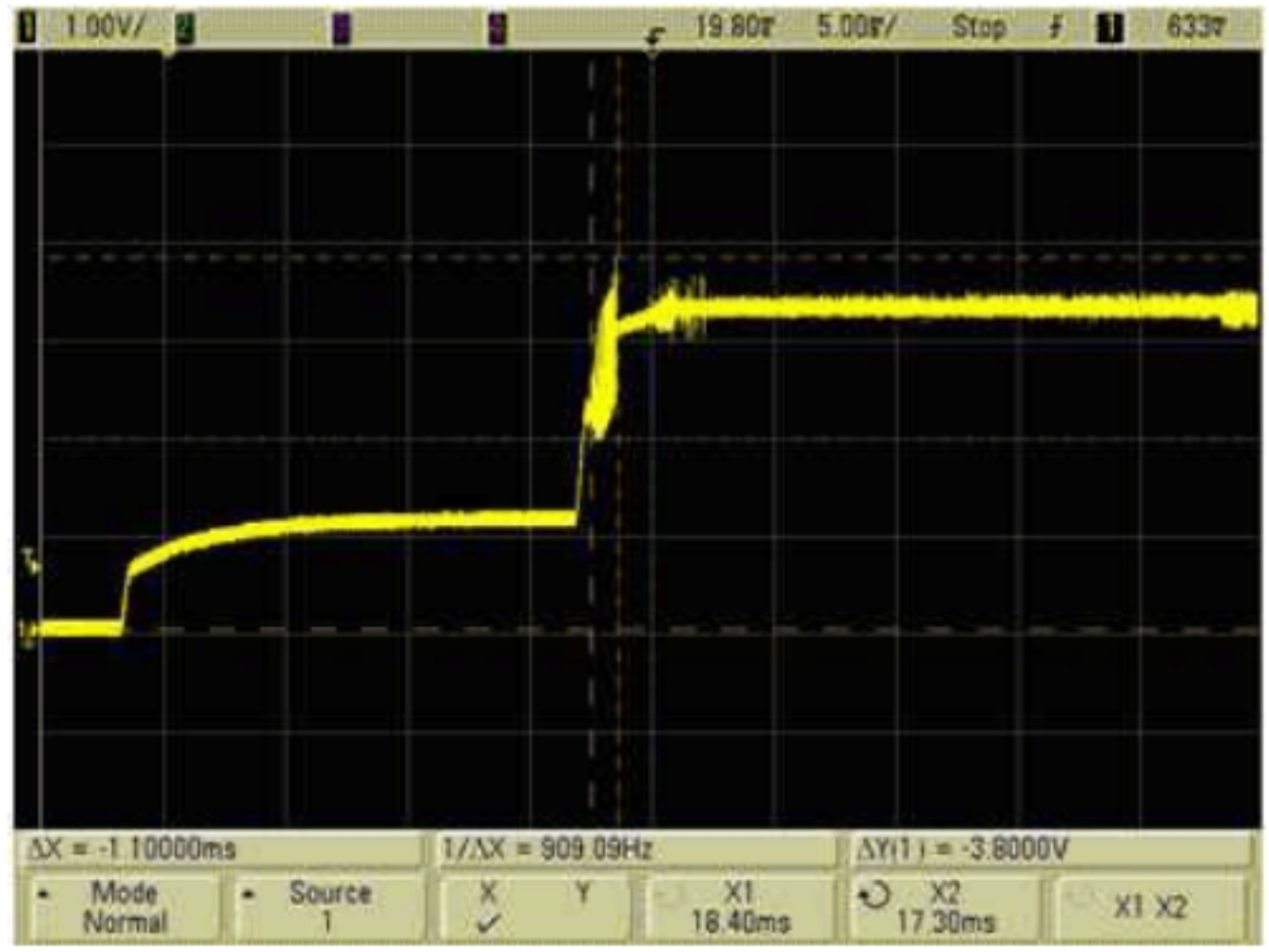


Figure 12. Input Voltage Overshoot <4V (Good)

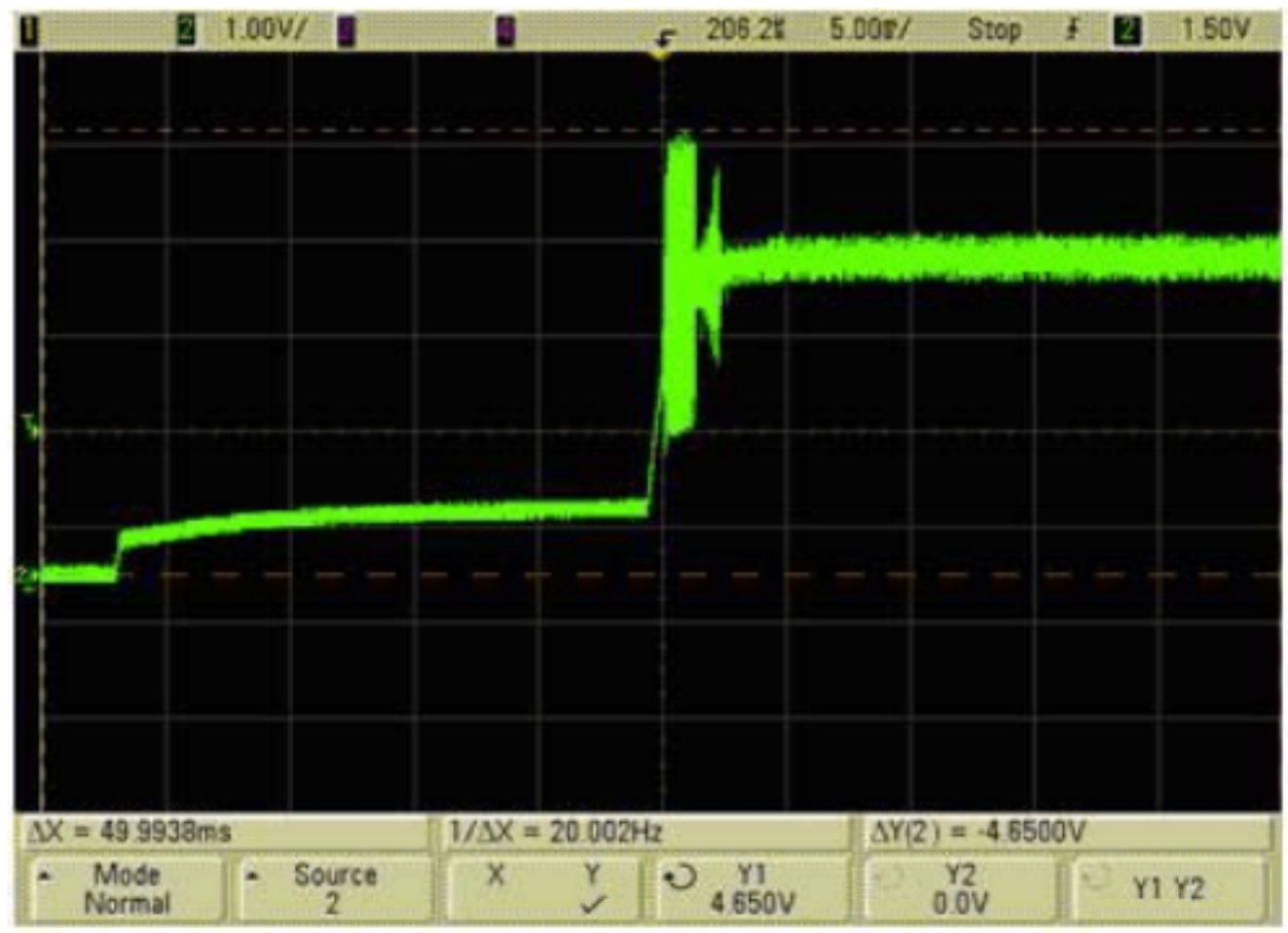


Figure 13. Input Voltage Overshoot >4V (Bad)

From the output side measured at REG_OUT, the voltage ripple must be within 100mV. Choosing different types and values of output capacitor (Cout1, Cout2) and power inductor (Lx) will seriously affect the efficiency and output voltage ripple of switching regulators. The following figures show the effects of different types of capacitors on the switching regulator ’s output voltage.

The blue square wave signal (top row) is measured at the output of REG_OUT before the power inductor (Lx). The yellow signal (second row) is measured after the power inductor (Lx), and shows there is a voltage ripple. The green signal (lower row) is the current. Data in the following figures was measured at 1000Mbps speed.

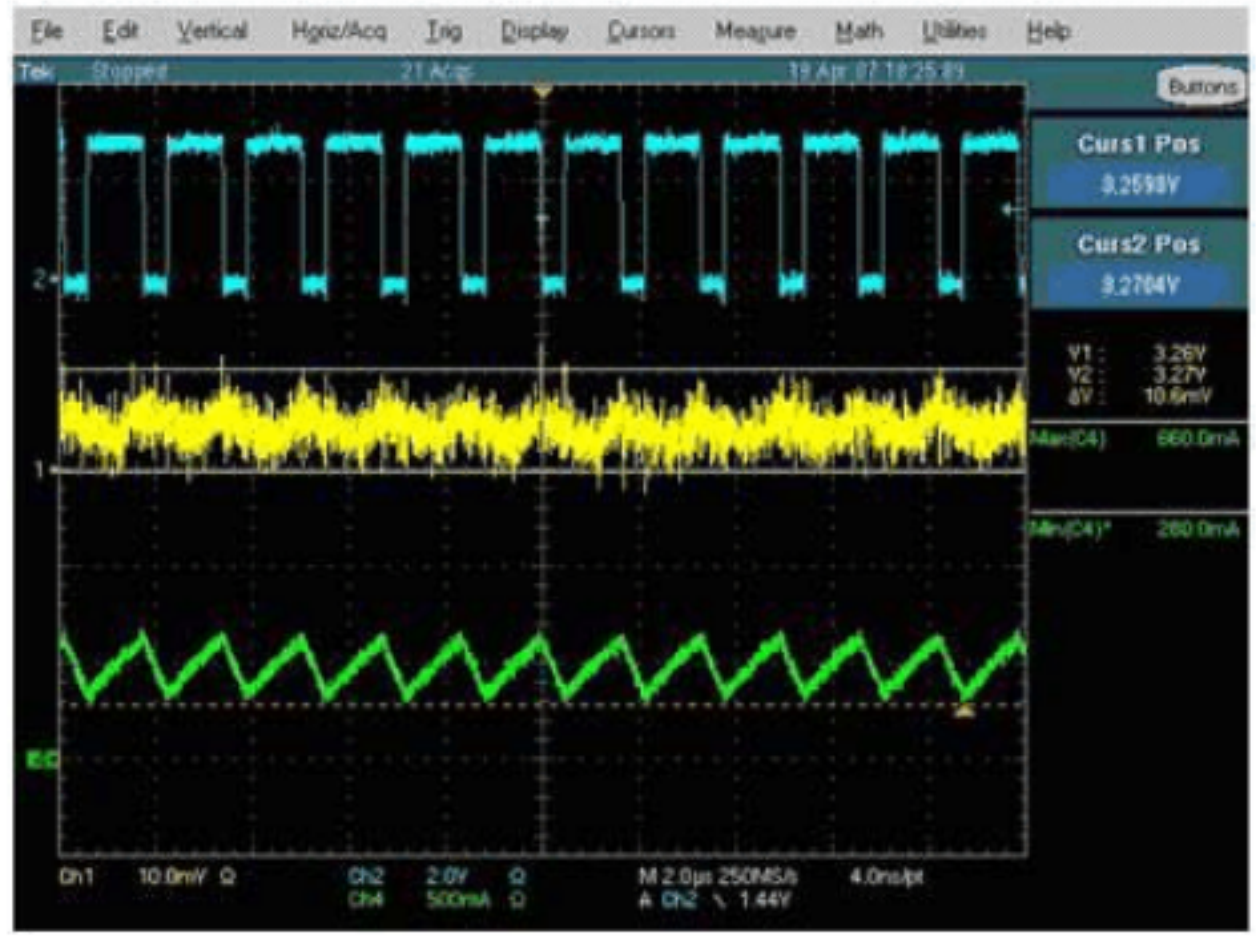


Figure 14. Ceramic 22 µ F 1210(X5R) (Good)

Figure 15. Ceramic 22 µ F 0805(Y5V) (Bad)

A ceramic 22 μ F (X5R) will have a lower voltage ripple compared to the electrolytic 100 choosing a proper output capacitor is to choose the lowest ESR to reduce the output voltage ripple. Choosing a ceramic 22 μ F 0805 (Y5V) in this case will cause malfunction of the switching regulator.

Figure 16. Electrolytic 100 μ F (Ripple Too High)

The following figures show how different inductors affect the REG_OUT output waveform. The typical waveform should look like Figure 17, which has a square waveform with a dip at the falling edge and the rising edge. If the inductor is not carefully chosen, the waveform may look like Figure 18, where the waveform looks like a distorted square. This will cause insufficient current supply and will undermine the stability of the system at gigabit speed. Data in the following figures was measured at gigabit speed.

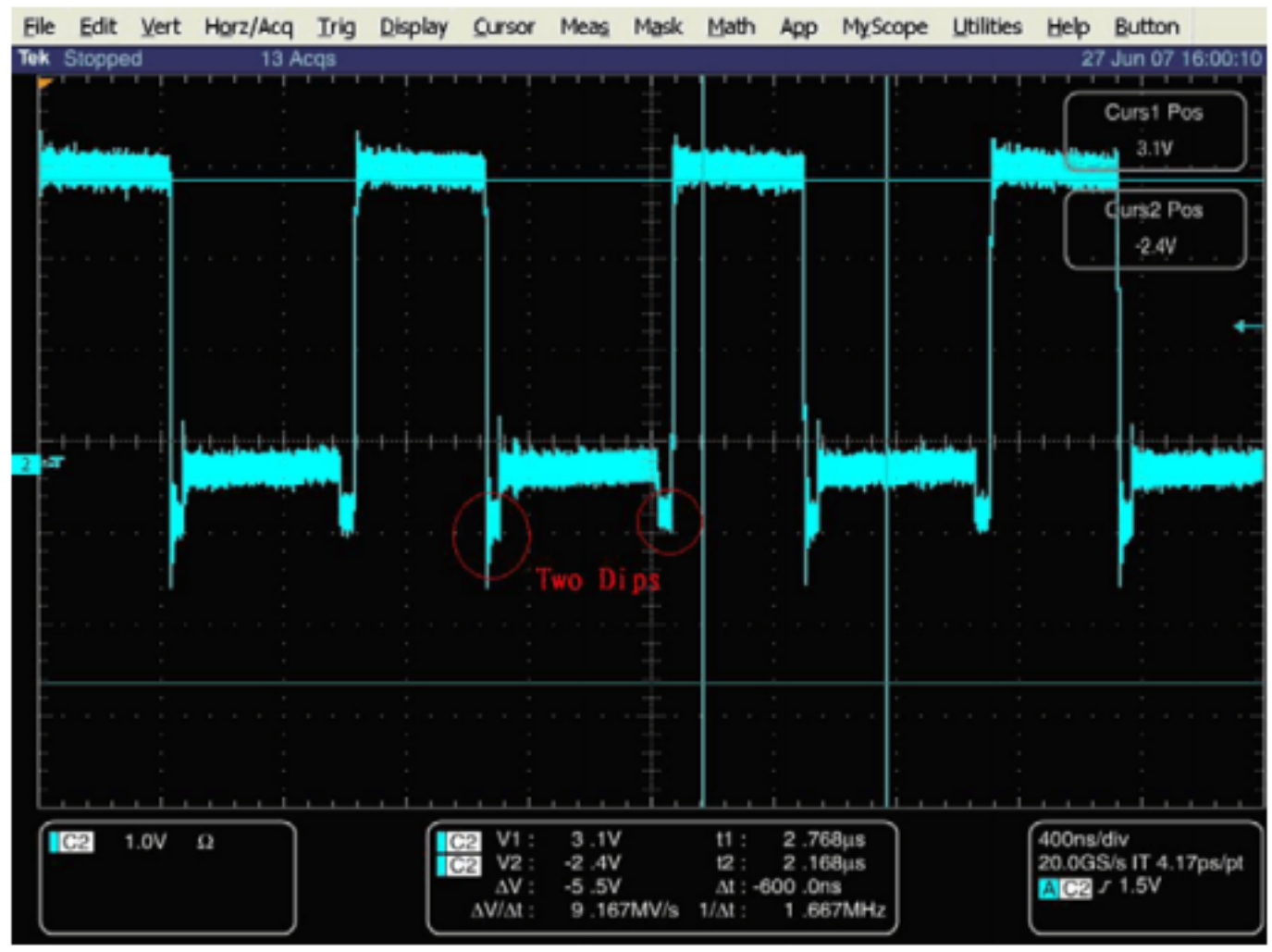


Figure 17. 4R7GTSD32 (Good)

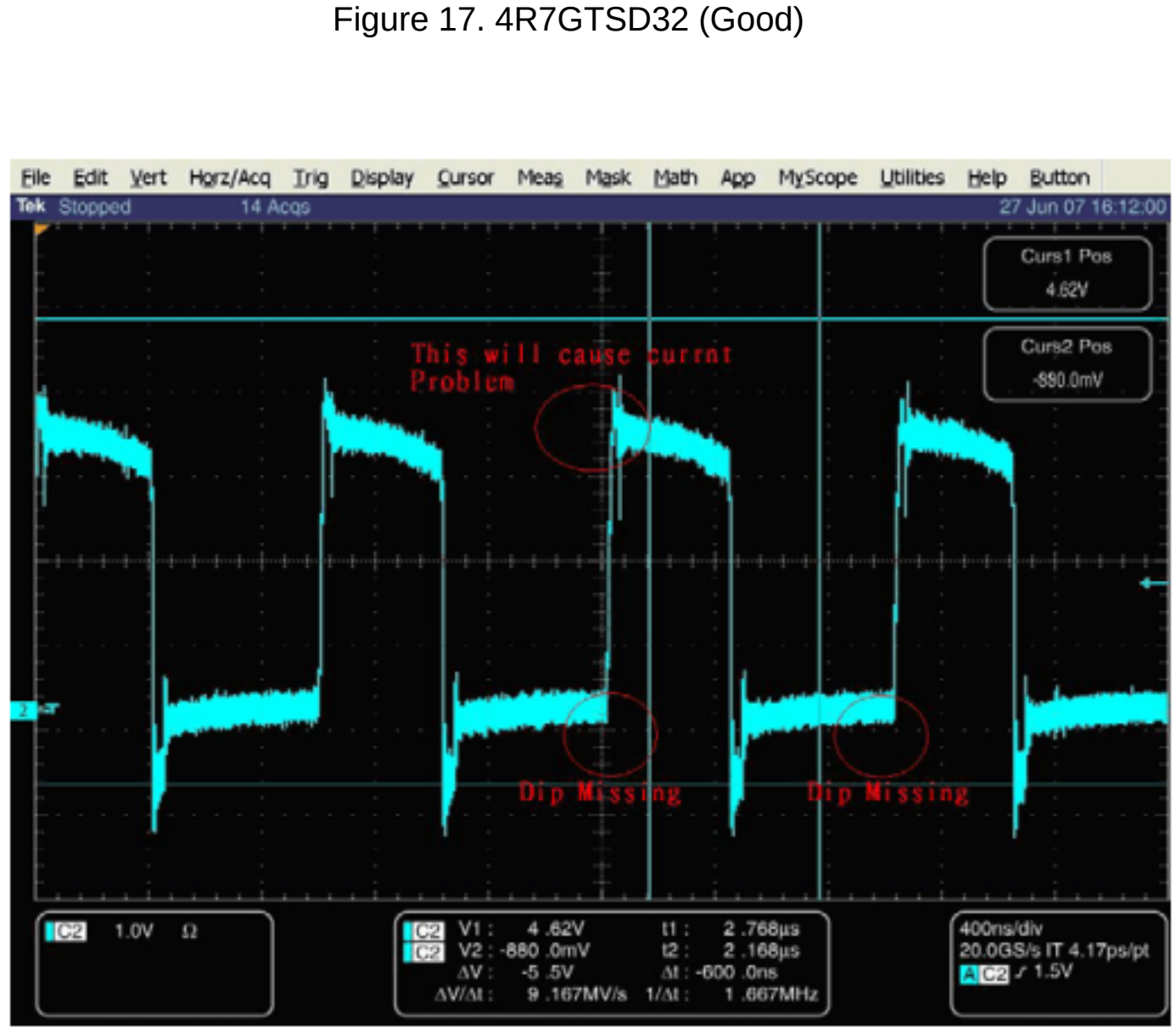


Figure 18. 1 µH Bead (Bad)

8.4. Efficiency Measurement

The efficiency of the switching regulator is designed to be above 75% in gigabit traffic mode. It is very important to choose a suitable inductor before Gerber certification, as the Inductor ESR value will affect the efficiency of the switching regulator. An inductor with a lower ESR value will result in a higher-efficiency switching regulator.

The efficiency of the switching regulator is easily measured using the following method.

Figure 19 shows two checkpoints, checkpoint A (CP_A) and checkpoint B (CP_B). The switching regulator input current (Icpa) should be measured at CP_A, and the switching regulator output current (Icpb) should be measured at CP_B.

To determine efficiency, apply the following formula:

Efficiency = Vcpb*Icpb / Vcpa*Icpa

Where Vcpb is 1.05V; Vcpa is 3.3V. The measurements should be performed in gigabit traffic mode.

For example: The inductor used in the evaluation board is a GOTREND GTSD32-4R7M:

? The ESR value @ 1MHz is approximately 0.712ohm

? The measured Icpa is 160mA at CP_A

? The measured Icpb is 400mA at CP_B

These values are measured in gigabit traffic mode, so the efficiency of the GOTREND GTSD32-4R7M can be calculated as follows:

Efficiency = (1.05V*400mA) / (3.3V*160mA) = 0.80 = 80%.

We strongly recommend that the efficiency should be measured when choosing an inductor for the switching regulator, and that the inductor should yield an efficiency rating higher than 75%. If the efficiency does not meet this requirement, there may be risk to the switching regulator reliability over the long term.

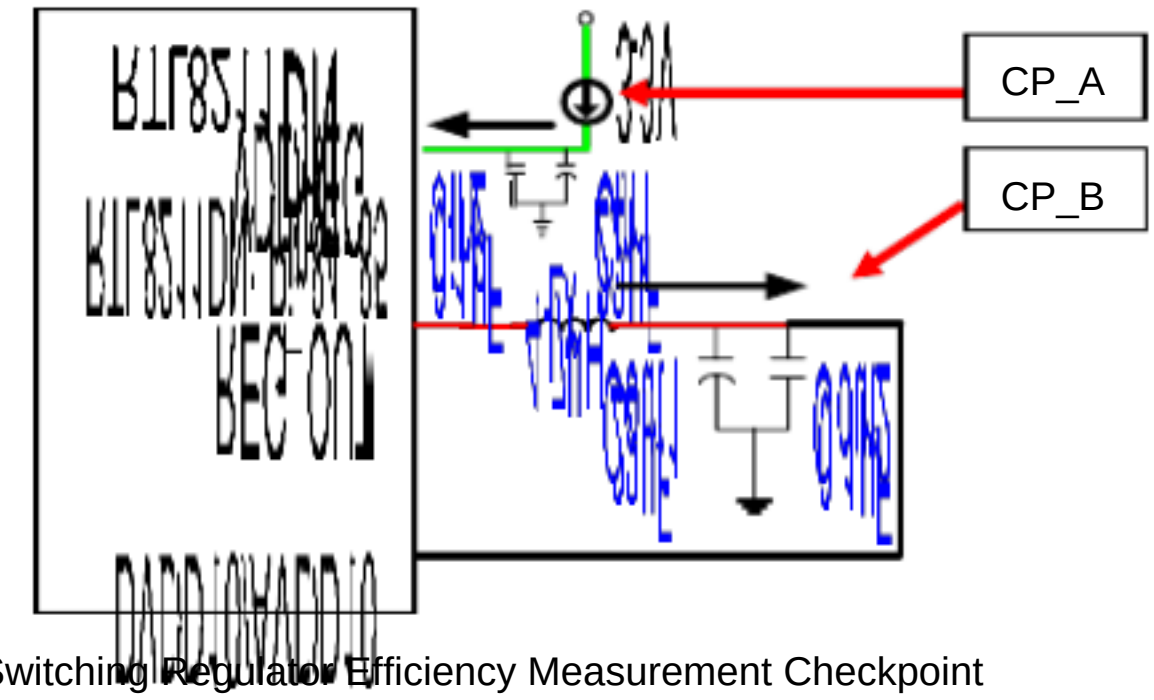


Figure 19. Switching Regulator Efficiency Measurement Checkpoint

8.5. Power Sequence

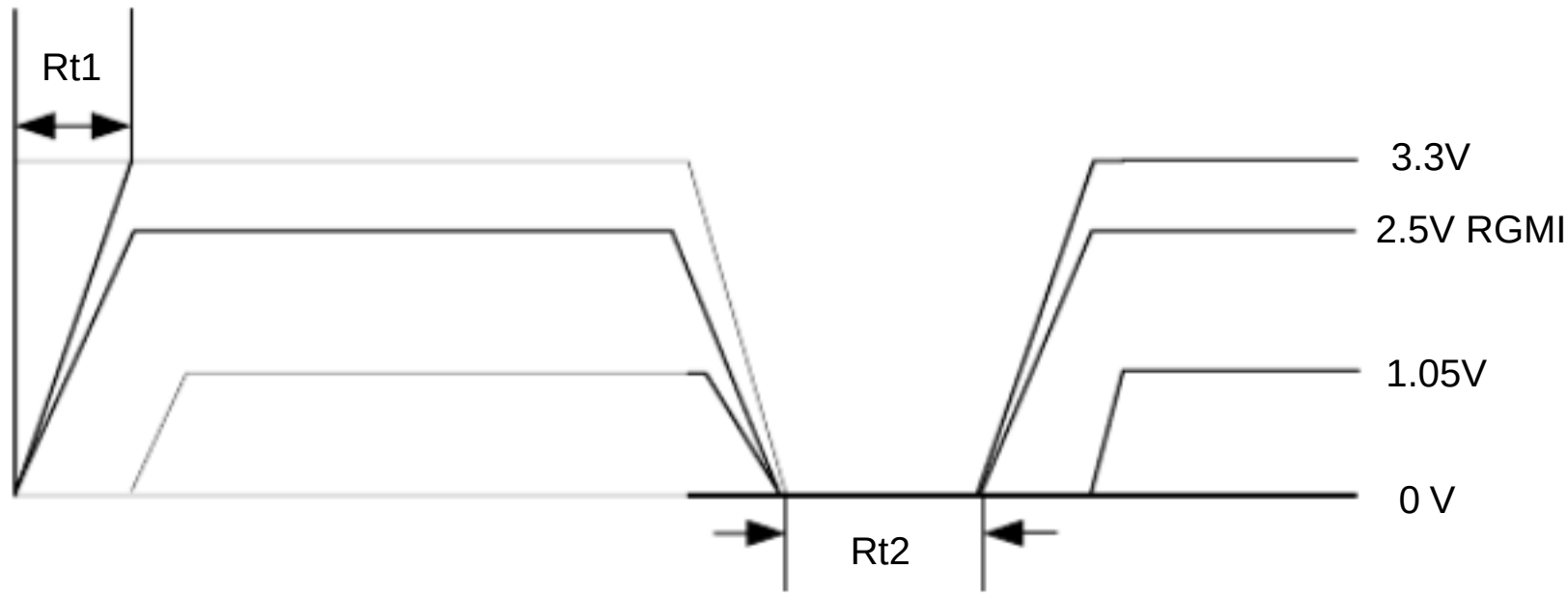


Figure 20. Power Sequence

Table 53. Power Sequence Parameter

Symbol	Description	Min	Typical	Max	Units
Rt1 3.3V	Rise Time	1	-	100	ms
Rt1	2.5V RGMII Rise Time	-	-	100	ms
Rt2 3.3V	Off Time	100	-	-	ms

Note 1: The RTL8211DN does not support fast 3.3V rising. The 3.3V rise time must be controlled over 1ms. If the rise time is too short, it will induce a peak voltage in VDDREG which may cause permanent damage to the switching regulator.

Note 2: If there is any action that involves consecutive ON/OFF toggling of the switching-regulator source (3.3V), the design must make sure the OFF state of both the switching-regulator source (3.3V) and output (1.05V) reach 0V, and the time period between the consecutive ON/OFF toggling action is longer than 100ms.

Note 3: The RTL8211DN requires 30ms for power on reset, after which it can access the PHY register from MDC/MDIO. Refer to the power sequence application note for details.

Note 4: When using an external oscillator or clock source, on stopping the clock source the RTL8211DN must also be powered off.

9. Characteristics

9.1. Absolute Maximum Ratings

WARNING: Absolute maximum ratings are limits beyond which permanent damage may be caused to the device, or device reliability will be affected. All voltages are specified reference to GND unless otherwise specified.

Table 54. Absolute Maximum Ratings

Symbol	Description	Minimum	Maximum	Unit
VDD33, AVDD33	Supply Voltage 3.3V	-0.4	3.7	V
AVDD10, DVDD10	Supply Voltage 1.05V	-0.1	1.26	V
VDD25 (RGMII 2.5V)	Supply Voltage 2.5V	-0.2	2.8	V
DCinput	Input Voltage	-0.5	Corresponding Supply Voltage + 0.5	V
DCoutput	Output Voltage	-0.3	Corresponding Supply Voltage + 0.5	V
NA Storage	Temperature	-55	+125	℃

Note: Refer to the most updated schematic circuit for correct configuration.

9.2. Recommended Operating Conditions

Table 55. Recommended Operating Conditions

Description	Pins	Minimum	Typical	Maximum	Unit
Supply Voltage VDD	DVDD33, AVDD33	2.97	3.3	3.63	V
	AVDD10, DVDD10	0.95	1.05	1.09	V
	2.5V GMII/RGMII	2.37	2.5	2.8	V
Ambient Operating Temperature T_A	-	0	-	70	℃
Maximum Junction Temperature	-	-	-	125	℃

9.3. Crystal Requirements

Table 56. Crystal Requirements

Symbol	Description/Condition	Minimum	Typical	Maximum	Unit
F_{ref}	Parallel Resonant Crystal Reference Frequency, Fundamental Mode, AT-Cut Type.	- 25		-	MHz
F_{ref} Stability	Parallel Resonant Crystal Frequency Stability, Fundamental Mode, AT-Cut Type. T_a=0 ℃~70 ℃.	-30 -		+30	ppm
F_{ref} Tolerance	Parallel Resonant Crystal Frequency Tolerance, Fundamental Mode, AT-Cut Type. T_a=25 ℃.	-50 -		+50	ppm
F_{ref} Duty Cycle	Reference Clock Input Duty Cycle.	45	-	55	%
ESR	Equivalent Series Resistance.	-	-	30	?
DL	Drive Level.	-	-	0.5	mW
Jitter	Broadband Peak-to-Peak Jitter[1, 2]		-	500	ps

Note 1: 25KHz to 25MHz RMS < 3ps.

Note 2: Broadband RMS < 9ps.

9.4. Oscillator/External Clock Requirements

Table 57. Oscillator/External Clock Requirements

Parameter	Condition	Minimum	Typical	Maximum	Unit
Frequency -		-	25	-	MHz
Frequency Stability	Ta = 0 ° C~70 ° C	-30	-	30	ppm
Frequency Tolerance	Ta = 25 ° C	-50	-	50	ppm
Duty Cycle	-	45	-	55	%
Broadband Peak-to-Peak Jitter[1, 2] -		-	-	500	ps
Vpeak-to-peak -		3.15	3.3	3.45	V
Rise Time (10%~90%)	-	-	-	10	ns
Fall Time (10%~90%)	-	-	-	10	ns
Operating Temperature Range	-	0	-	70	° C

Note 1: 25KHz to 25MHz RMS < 3ps.

Note 2: Broadband RMS < 9ps.

9.5. DC Characteristics

Table 58. DC Characteristics

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
VDD33, AVDD33	3.3V Supply Voltage	-	2.97	3.3	3.63	V
RGMII I/O	2.5V GMII/RGMII Supply V oltage	-	2.37	2.5	2.8	V
DVDD10, AVDD10	1.05V Supply Voltage	-	0.98	1.05	1.09	V
Voh (3.3V)	Minimum High Level Output V oltage	-	0.9*VDD33	-	VDD33	V
Voh (2.5V)	Minimum High Level Output V oltage	-	0.9*VDD25	-	VDD25	V
Vol (3.3V)	Maximum Low Level Output V oltage	-	0	-	0.1*VDD33	V
Vol (2.5V)	Maximum Low Level Output V oltage	-	0	-	0.1*VDD25	V
Vih	Minimum High Level Input V oltage	-	1.8	-	-	V
Vil	Maximum Low Level Input V oltage	-	-	-	0.9	V
Iin	Input Current	Vin=VDD33 or GND	0	-	0.5	μ A

9.5.1. SGMII DC Characteristics

Table 59. Differential Transmitter Output DC Characteristics

Symbol	Parameter	Minimum	Typical	Maximum	Units
V_{oh} Output	Voltage High	-	-	1000	mV
V_{ol} Output	Voltage Low	500	-	-	mV
V_{ring} Output	Ringing	-	-	10 %	
$\|V_{od}\|$	Output Differential Voltage	400	-	500	mV
V_{cm} Output	Offset Voltage	-	775	-	mV
R_o	Output Impedance (Single-End)	40	50	60	ohm
ΔR_o	Mismatch in a Pair	-	-	10	%
$\Delta\|V_{od}\|$	Change in Vod between ‘0’ and ‘1’	-	-	25	mV
ΔV_{od}	Change in Vos between ‘0’ and ‘1’	-	-	25	mV
I_{sa}, I_{sb}	Output Current on Short to GND	-	-	40	mA
I_{sab}	Output Current when a/b are Shorted	-	-	12	mA
I_{xa}, I_{xb}	Power Off Leakage Current	-	-	10	mA

Table 60. Differential Receiver Input DC Characteristics

Symbol	Parameter	Minimum	Typical	Maximum	Units
V_i Input	Voltage Range	250	-	1000	mV
V_{idth} Input	Differential Threshold	-150	-	150	mV
V_{hyst}	Input Differential Hysteresis	25	-	-	mV
R_{in}	Receiver Differential Input Impedance	80	100	120	ohm

9.6. AC Characteristics

9.6.1. MDC/MDIO Timing

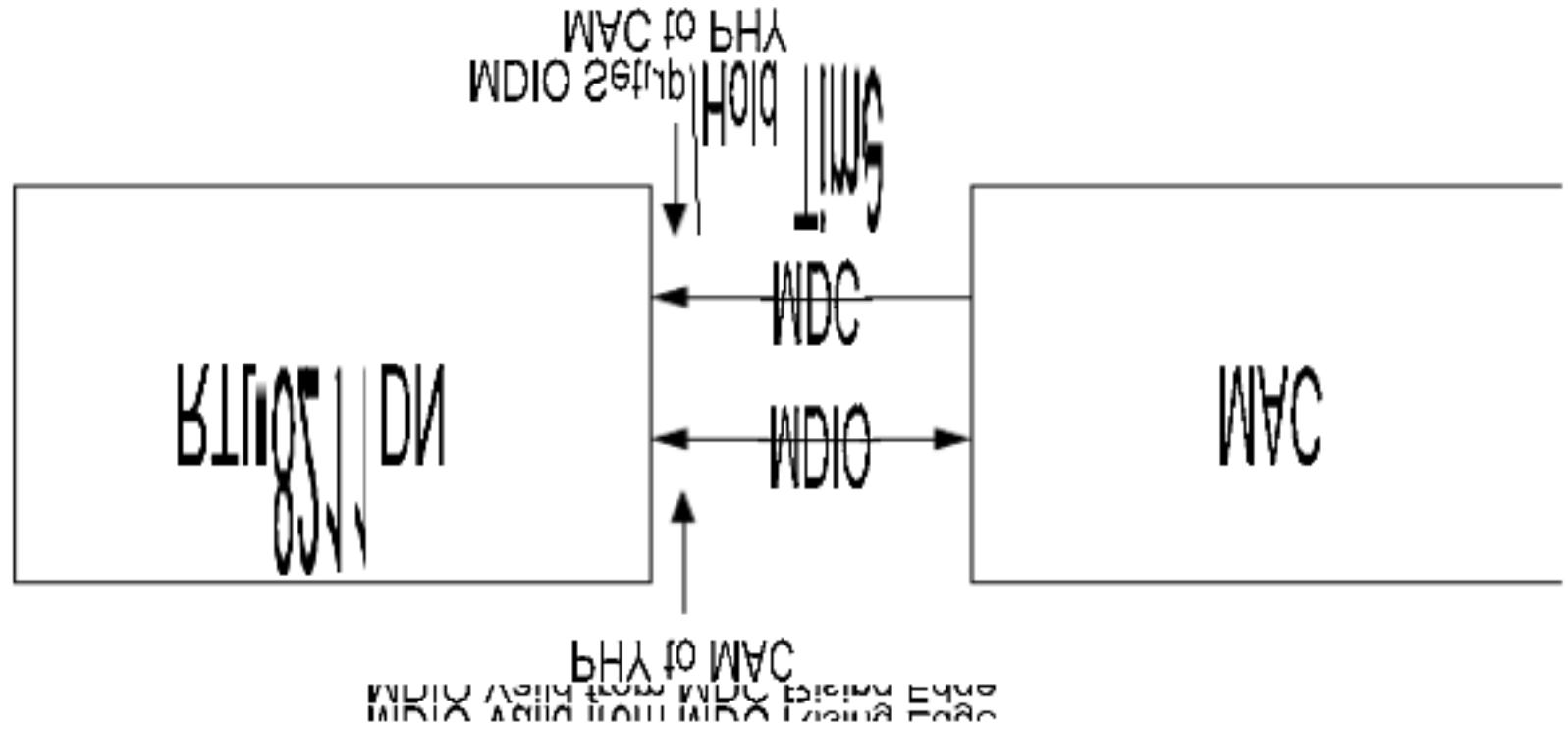


Figure 21. MDC/MDIO Interface Setup, Hold Time, and Valid from MDC Rising Edge Time Definitions

MDC/MDIO Timing – Management Port

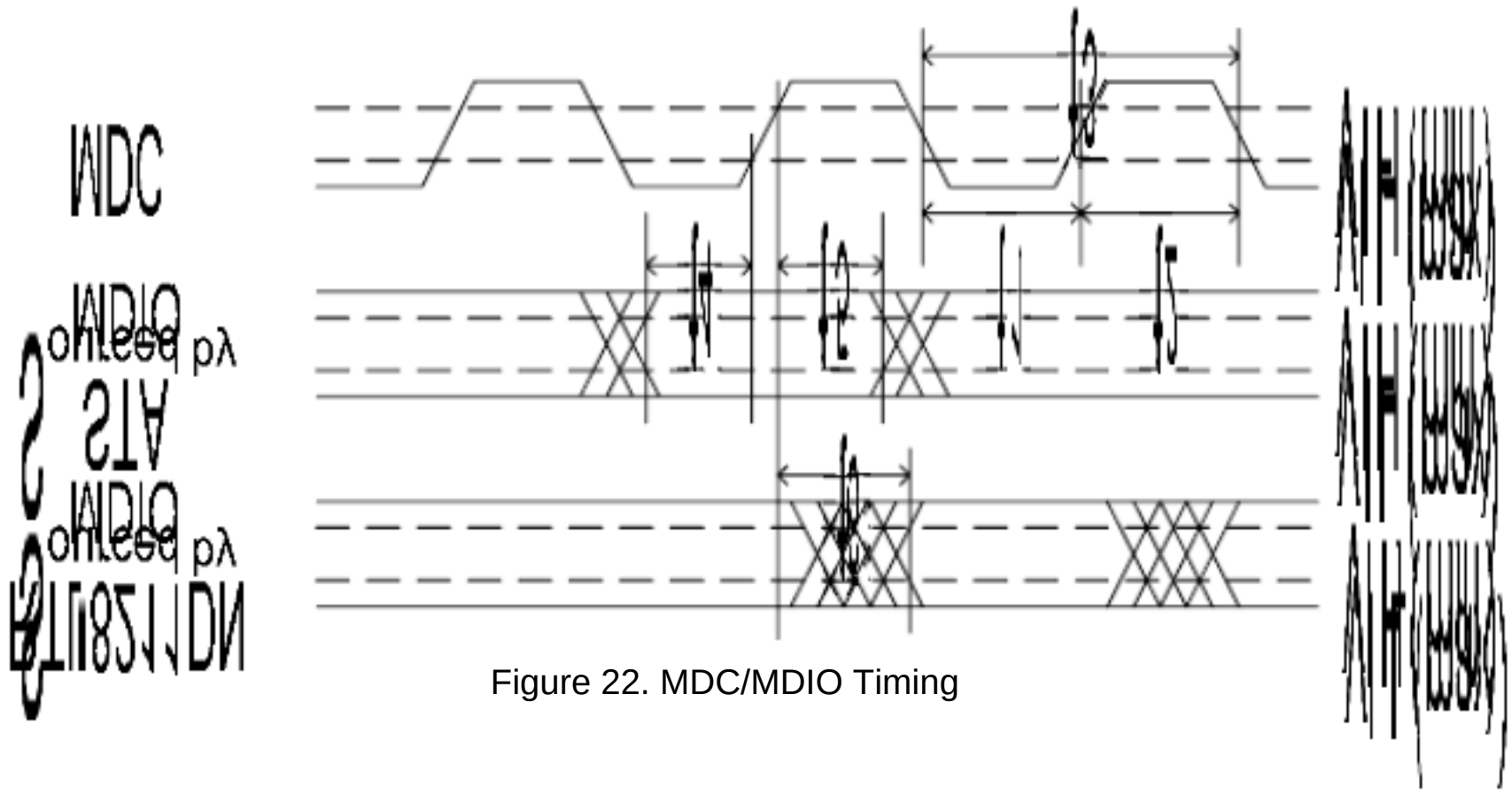


Figure 22. MDC/MDIO Timing

Table 61. MDC/MDIO Timing

Symbol	Description	Minimum	Maximum	Unit
t_1	MDC High Pulse Width	160	-	ns
t_2	MDC Low Pulse Width	160	-	ns
t_3	MDC Period	400	-	ns
t_4	MDIO Setup to MDC Rising Edge	10	-	ns
t_5	MDIO Hold Time from MDC Rising Edge	10	-	ns
t_6	MDIO Valid from MDC Rising Edge	0	300	ns

9.6.2. MII Transmission Cycle Timing

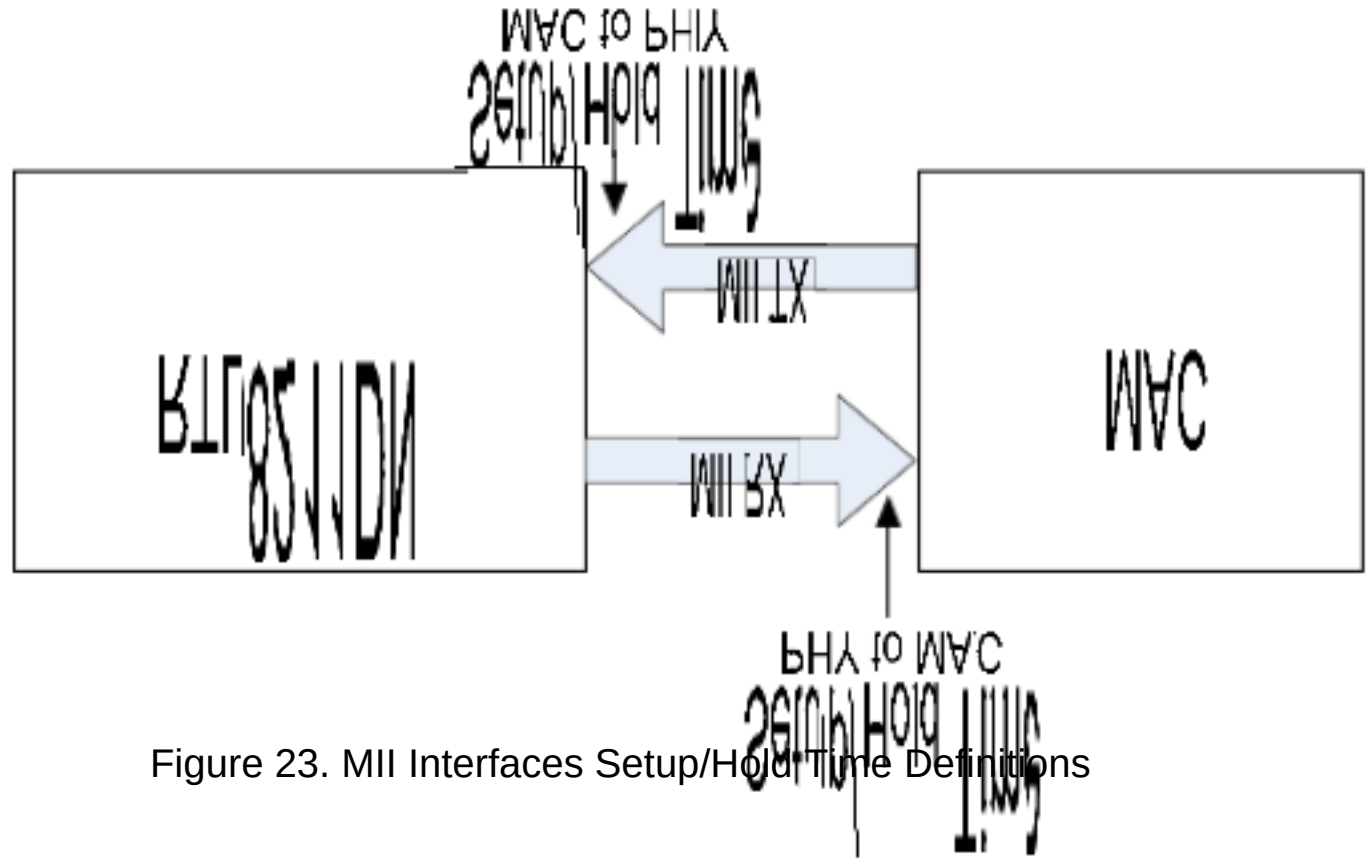


Figure 23. MII Interfaces Setup/Hold Time Definitions

Figure 24 shows an example of a packet transfer from MAC to PHY on the MII interface.

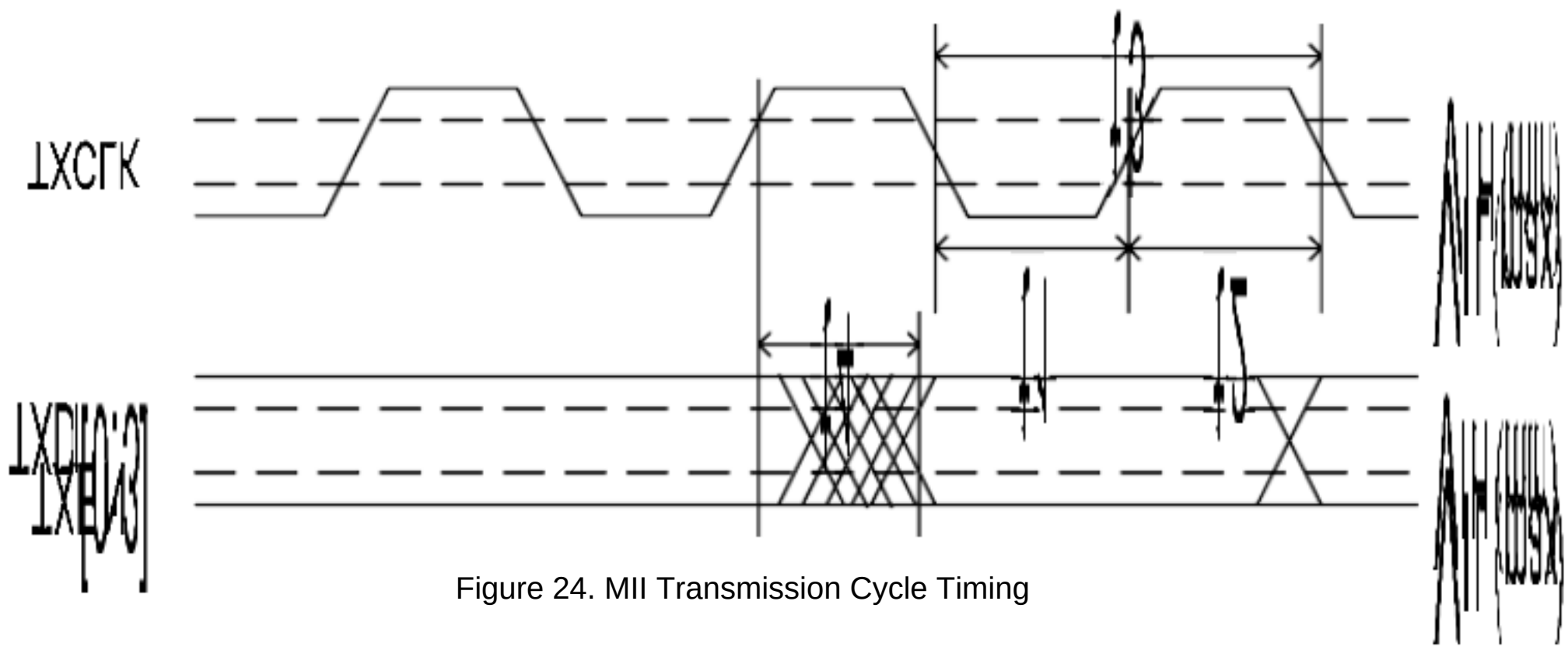


Figure 24. MII Transmission Cycle Timing

Table 62. MII Transmit Timing Parameters

Symbol	Description		Minimum	Typical	Maximum	Unit
t_1, t_2	TXCLK Duty Cycle	100Mbps	40	50	60	%
		10Mbps	40	50	60	%
t_3	TXCLK Period	100Mbps	-	40	-	ns
		10Mbps	-	400	-	ns
t_4	TXEN, TXD[0:3] Hold After TXCLK Rising Edge	100Mbps	0		-	25	ns
		10Mbps	0		-	25	ns

9.6.3. MII Reception Cycle Timing

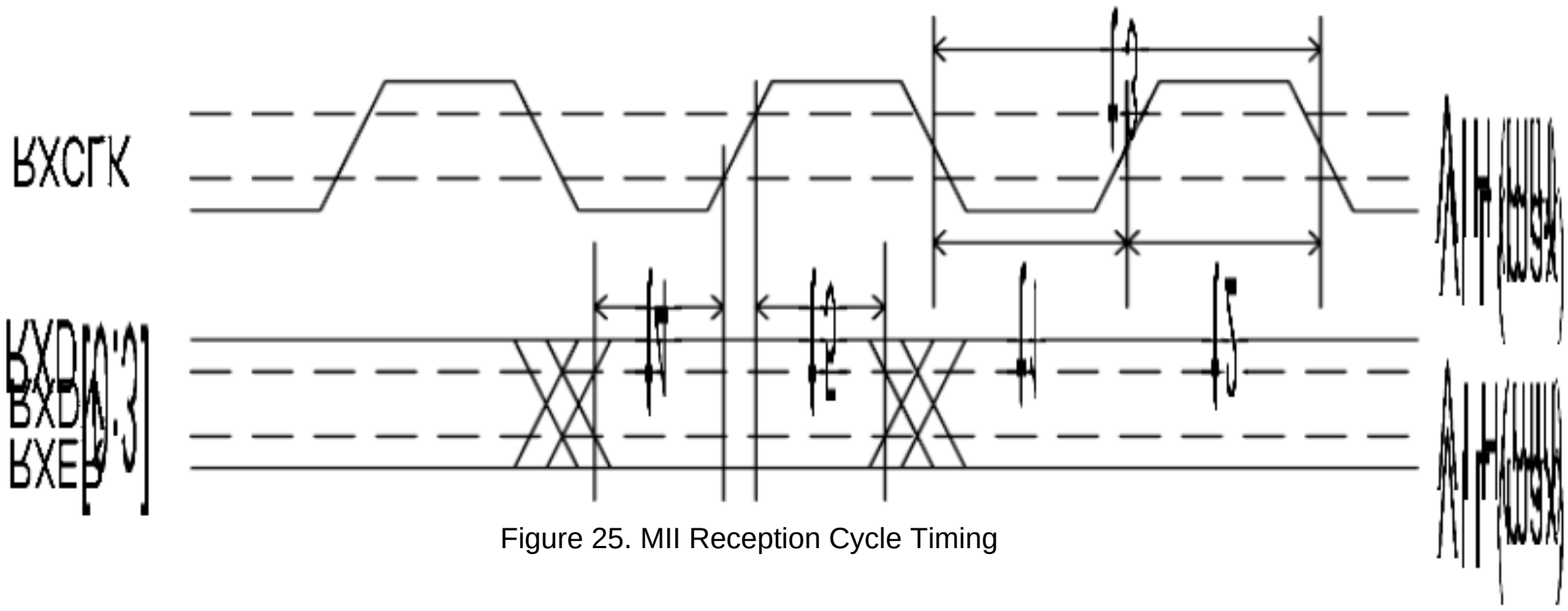


Figure 25. MII Reception Cycle Timing

Table 63. MII Receive Timing Parameters

Symbol	Description		Minimum	Typical	Maximum	Unit
t_1, t_2	RXCLK Duty Cycle	100Mbps	40	50	60	%
		10Mbps	40	50	60	%
t_3	RXCLK Period	100Mbps	-	40	-	ns
		10Mbps	-	400	-	ns
t_4	RXER, RXDV , RXD[0:3] Setup to RXCLK Rising Edge	100Mbps	10		-	-	ns
		10Mbps	10		-	-	ns
t_5	RXER, RXDV , RXD[0:3] Hold After RXCLK Rising Edge	100Mbps	10		-	-	ns
		10Mbps	10		-	-	ns

9.6.4. GMII Timing Modes

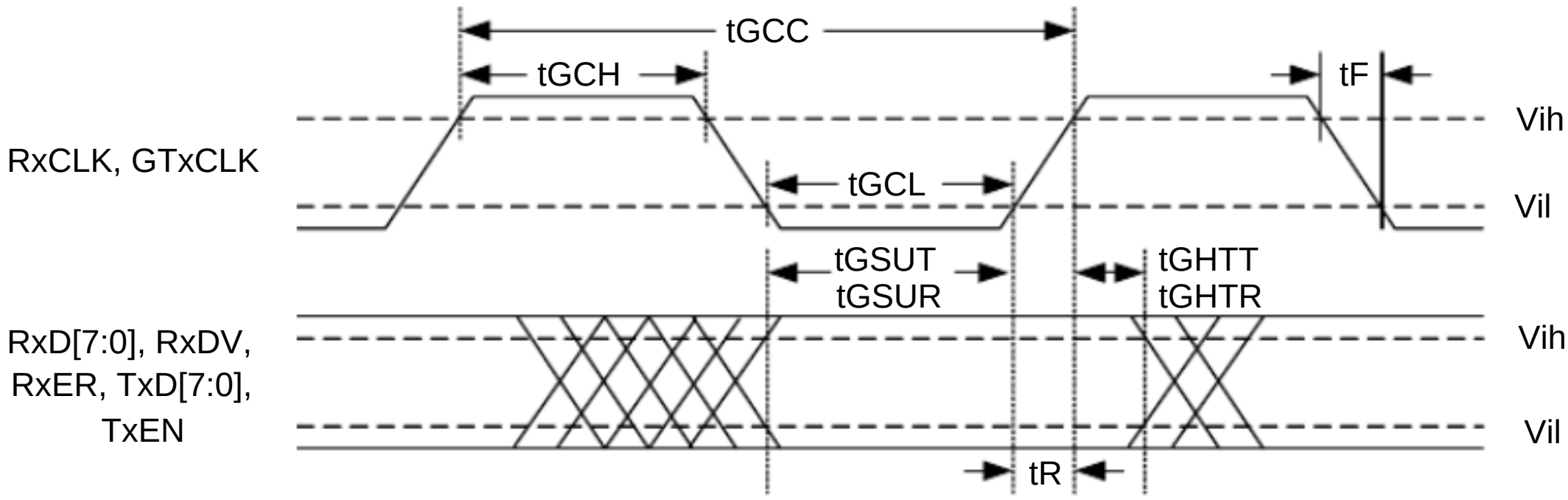
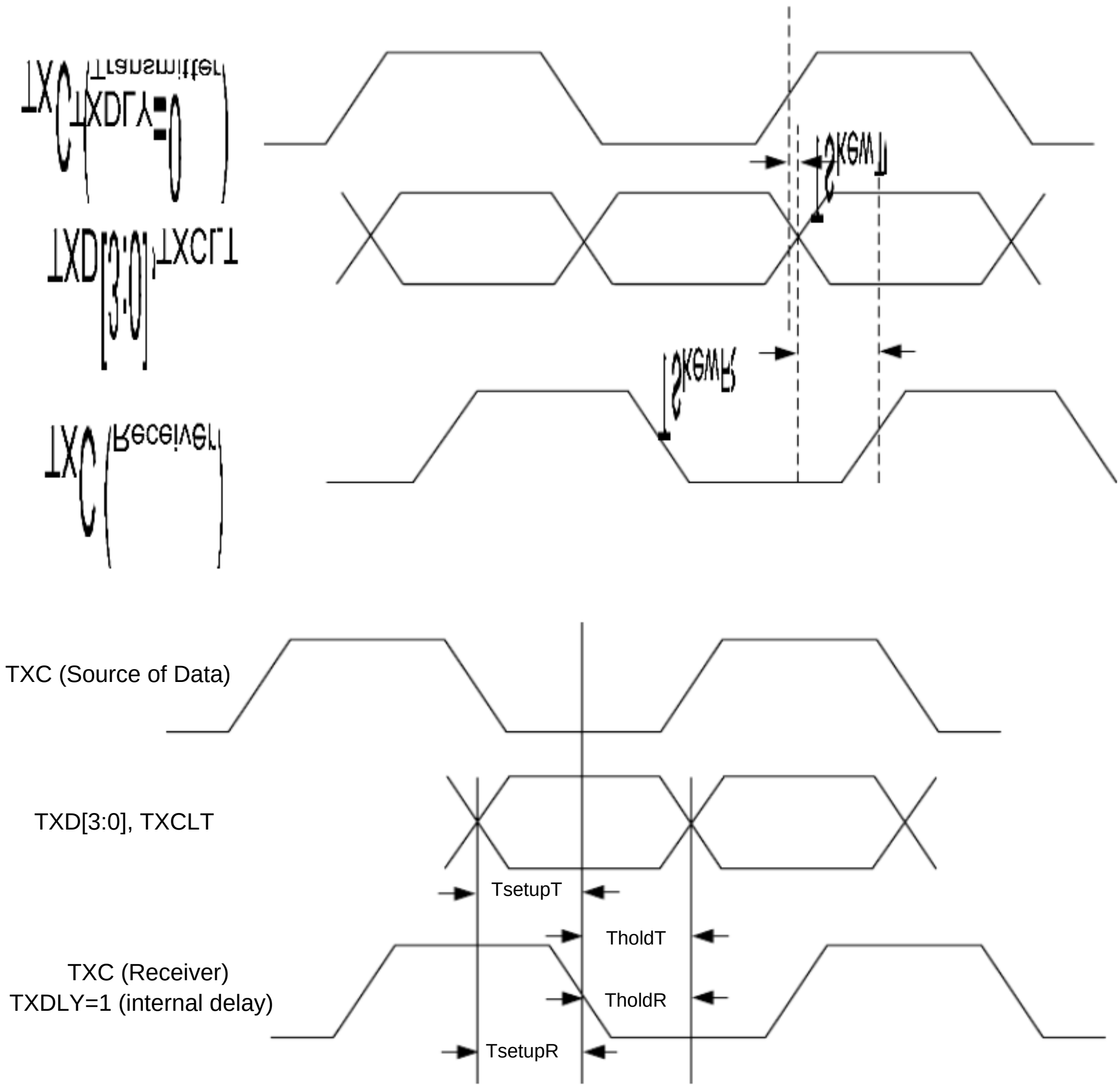


Figure 26. GMII Timing

Table 64. GMII Timing Parameters

Symbol	Description	Min	Typical	Max	Units
tGCC RxCLK	Cycle Time	7.5	8	8.5	ns
tGCH	GTxCLK, RxCLK High Time	2.5	-	-	ns
tGCL	GTxCLK, RxCLK Low Time	2.5	-	-	ns
tR	GTxCLK, RxCLK Rise Time	-	-	1	ns
tF	GTxCLK, RxCLK Fall Time	-	-	1	ns
tGSUT	RxD, RxDV, RxER Setup to ↑of RxCLK	2.5 -		-	ns
tGHTT	RxD, RxDV, RxER Hold from ↑of RxCLK	0.5 -		-	ns
tGSUR	TxD, TxEN Setup to ↑of GTxCLK	2 - -			ns
tGHTR	TxD, TxEN Hold from ↑of GTxCLK	0 - -			ns

9.6.5. RGMII Timing Modes



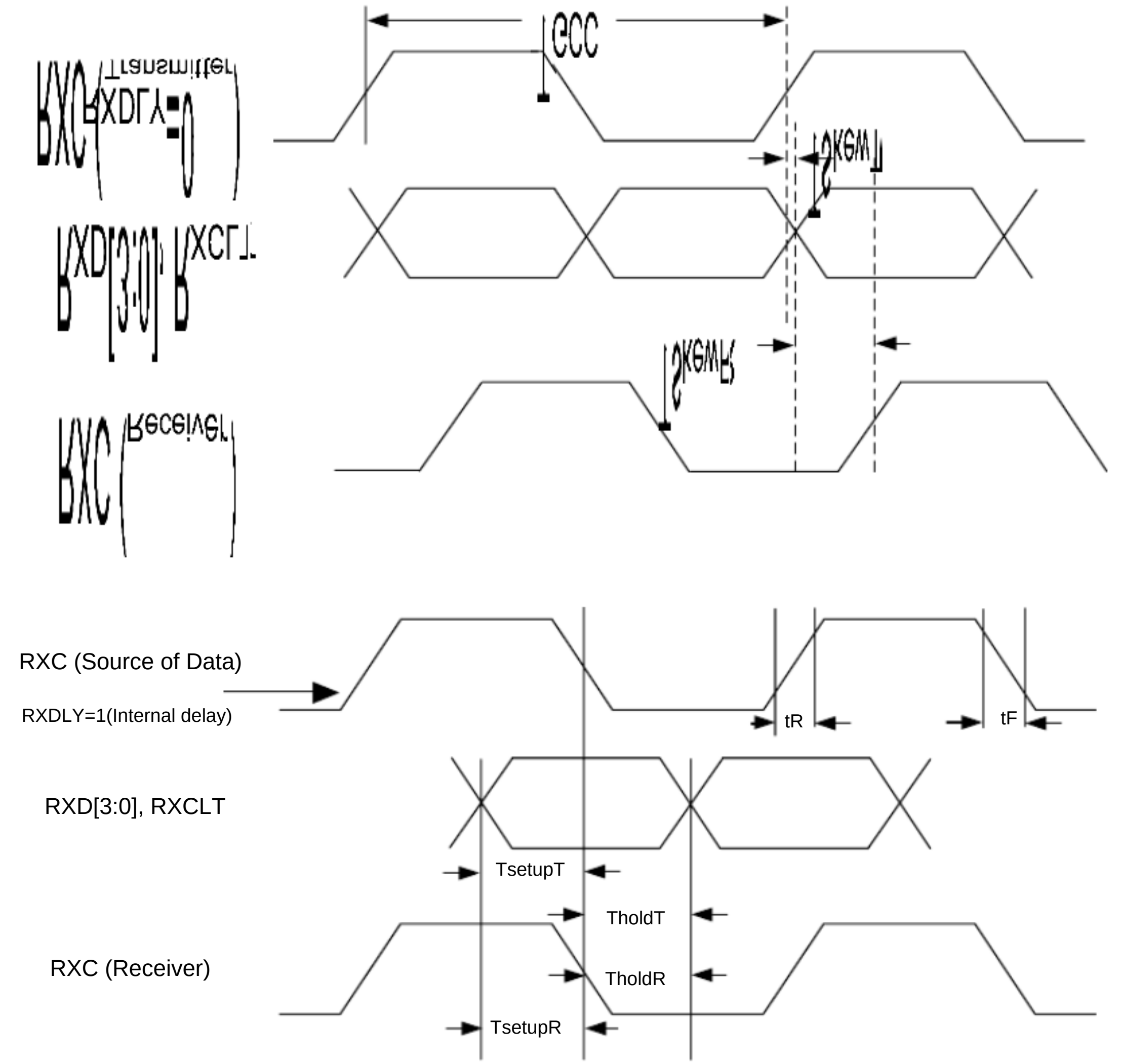


Figure 27. RGMII Timing Modes

Table 65. RGMII Timing Parameters

Symbol	Description	Min	Typical	Max	Units
TGCC	Clock Cycle Duration (1000Mbps)	7.2	8	8.8	ns
	Clock Cycle Duration (100Mbps)	36	40	44	ns
	Clock Cycle Duration (10Mbps)	360	400	440	ns
Duty_G	Duty Cycle for Gigabit	45	50	55	%
Duty_T	Duty Cycle for 10/100T	40	50	60	%
tR	RXC Rise Time (20%~80%)	-	-	0.75	ns
tF	RXC Fall Time (20%~80%)	-	-	0.75	ns
TsetupT	Data to Clock Output Setup (at Transmitter Integrated Delay)	1.2	2	-	ns
TholdT	Data to Clock Output Hold (at Transmitter Integrated Delay)	1.2	2	-	ns
TsetupR	Data to Clock Input Setup (at Receiver Integrated Delay)	1.0	2	-	ns
TholdR	Data to Clock Input Hold (at Receiver Integrated Delay)	1.0	2	-	ns
TskewT	Data to Clock Output Skew (at Transmitter)	-0.5	0	0.5	ns
TskewR	Data to Clock Input Skew (at Receiver). This implies that PC board design will require clocks to be routed such that an additional trace delay of greater than 1.5ns and less than 2.0ns will be added to the associated clock signal	1 1.8		2.6	ns

9.6.6. SGMII Timing Modes

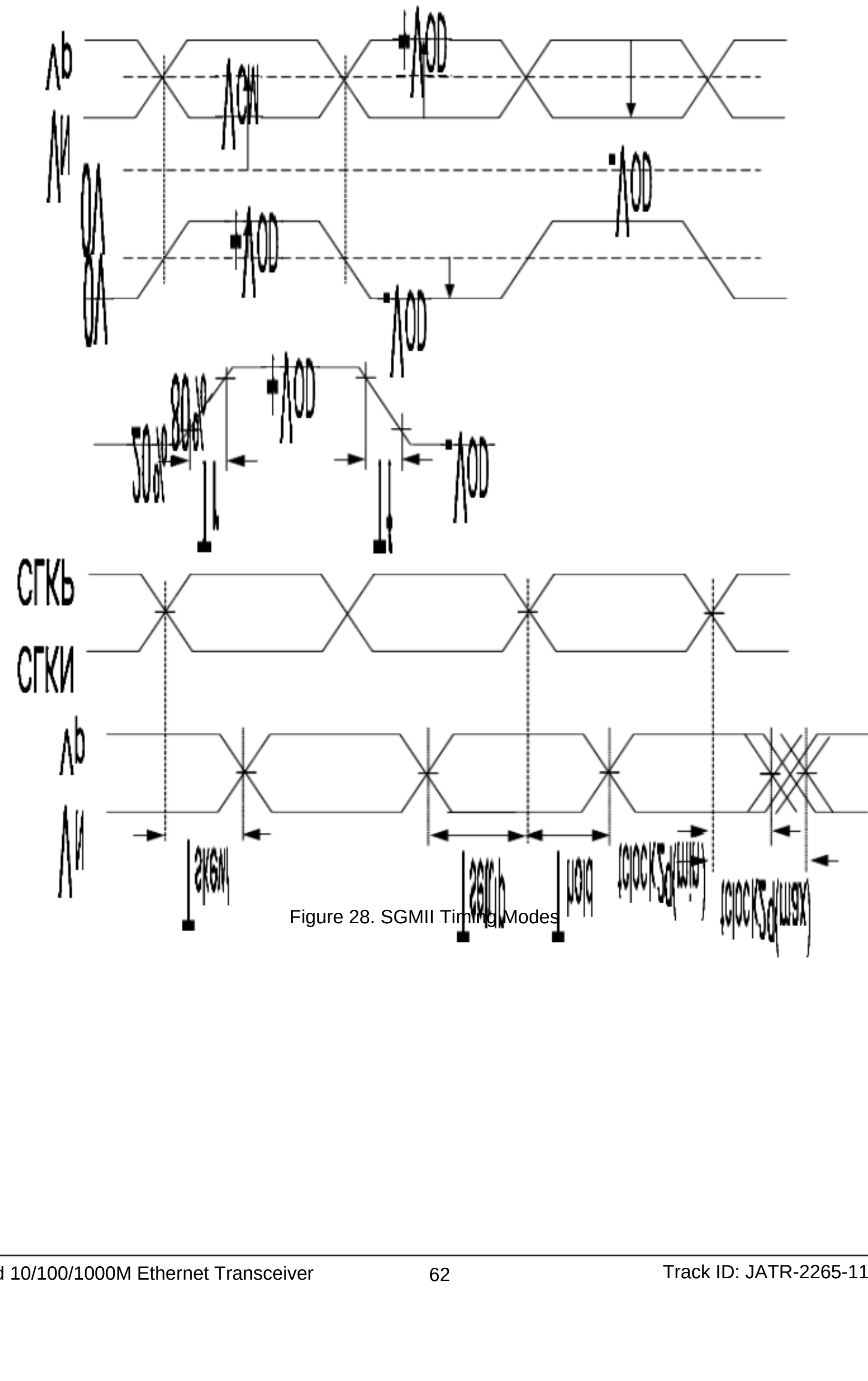


Figure 28. SGMII Timing Modes

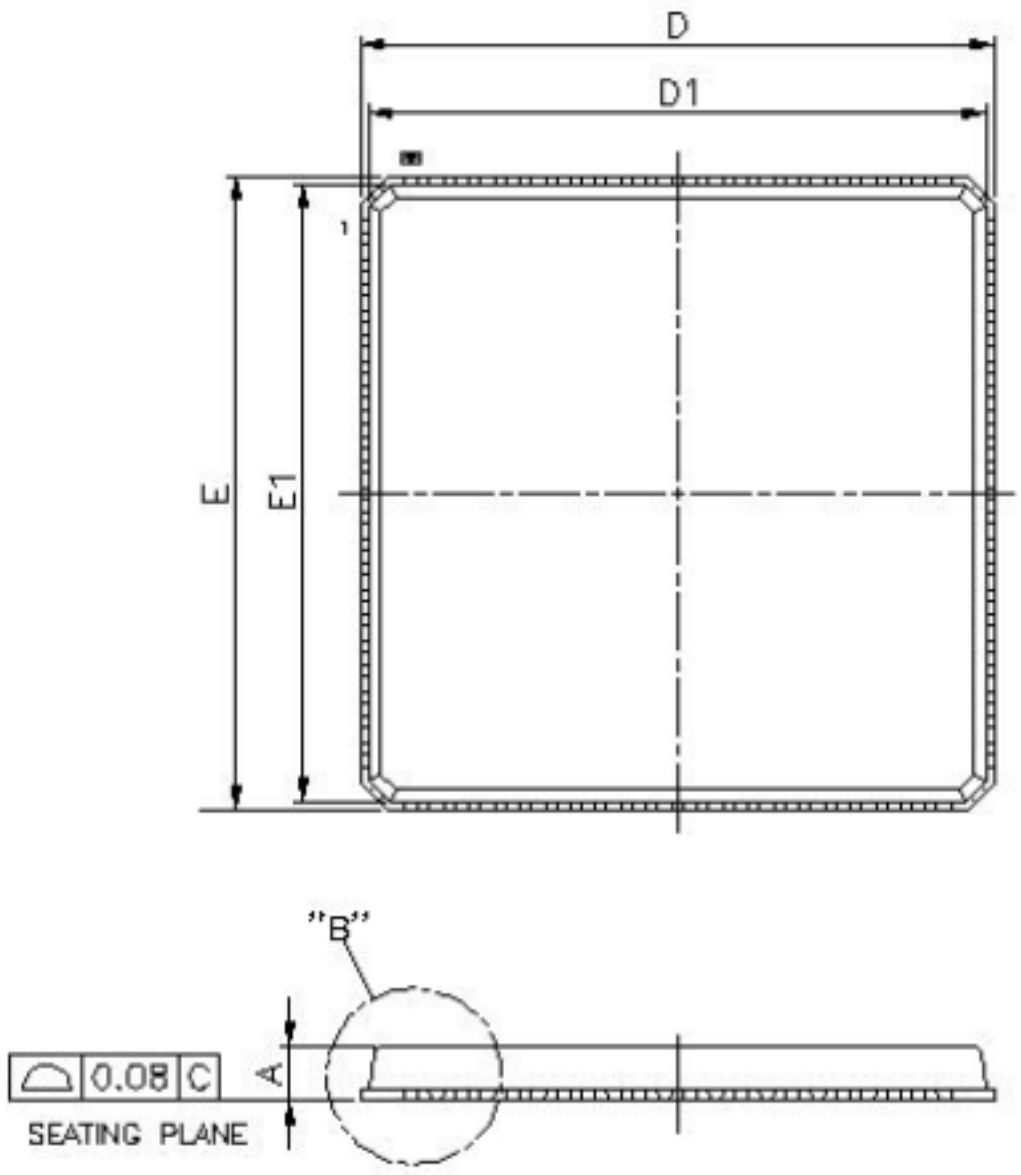
Table 66. Differential Transmitter Output AC Timing

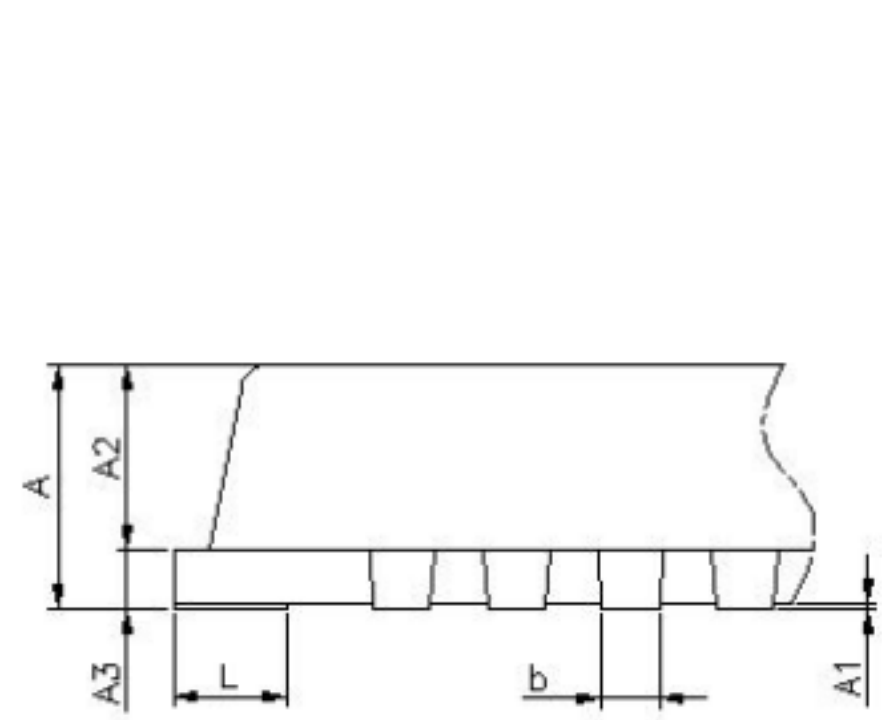
Symbol	Parameter	Min	Typical	Max	Units	Note
clock	Clock Signal Duty Cycle @ 625MHz	48	-	52	%	-
Tf V	$_{OD}$ Fall Time (20%~80%)	80	-	120	ps	-
Tr V	$_{OD}$ Rise Time (20%~80%)	80	-	120	ps	-
T_{skew}	Skew between Two Members of a Differential Pair	- -		15	ps	-
$t_{clock2q}$	Clock to Data Relationship: From either edge of the clock to valid data	250 - 550			ps	-
-	Effective Clock Period	-	800	-	ps	-
-	Cycle to Cycle Clock Jitter -		-	100	ps	peak-to-peak
-	Imperfect Duty Cycle	- -		30	ps	peak-to-peak
-	Data Dependent Skew	-	-	70	ps	peak-to-peak
-	Static Package Skew	-	-	100	ps	peak-to-peak
- Remaining	Window	500	-	-	ps	peak-to-peak

Table 67. Differential Receiver Input AC Timing

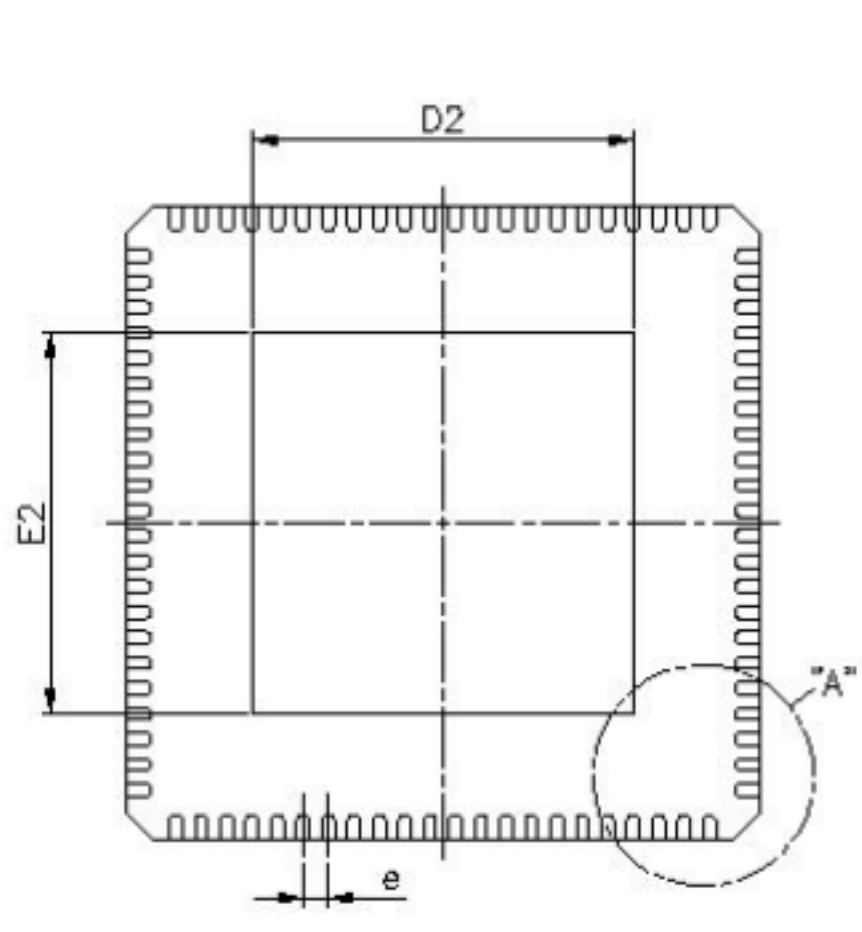
Symbol	Parameter	Min	Typical	Max	Units	Note
T_{setup}	Setup Time (20%~80%)	250 - 550			ps	-
T_{hold}	Hold Time (20%~80%)	250 - 550			ps	-
- Driver	Window	500	-	-	ps	peak-to-peak
-	Static Package Skew	100	-	-	ps	peak-to-peak
- Remaining	Window	200	-	-	ps	peak-to-peak

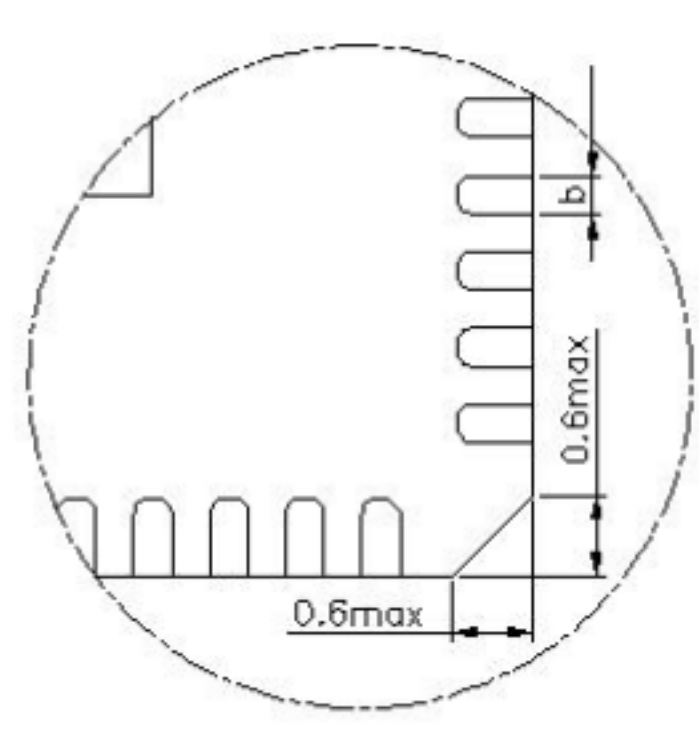
10. Mechanical Dimensions





DETAIL : "B"





DETAIL : "A"

10.1. Mechanical Dimensions Notes

Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A 0.75		0.85	1.00	0.030	0.034	0.039
A_1 0.00		0.02	0.05	0.000	0.001	0.002
A_2 0.55		0.65	0.80	0.022	0.026	0.032
A_3 0.20REF				0.008REF		
b	0.15 0.22		0.25 0.006 0.08 0.010			
D/E 10.00BSC				0.394BSC		
D_1/E_1 9.75BSC				0.384BSC		
D_2/E_2 5.75 6.0			6.25	0.226	0.236	0.246
e 0.40BSC				0.016BSC		
L 0.30		0.40	0.50	0.012	0.016	0.020

Note 1: CONTROLLING DIMENSION: MILLIMETER (mm).

Note 2: REFERENCE DOCUMENT: JEDEC MO-220.

11. Ordering Information

Table 68. Ordering Information

Part Number	Package	Status
RTL8211DN-VB-GR	88-Pin QFN with ‘Green’ Package	Mass Production

Note: See page 5 for package identification.

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Headquarters
No. 2, Innovation Road II
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