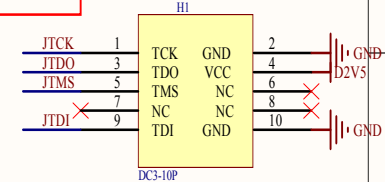


VIP Board Mini V2.5

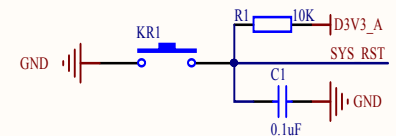
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JTAG



RESET



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EP4CE6/10 FPGA_Core

PIN IO * 130

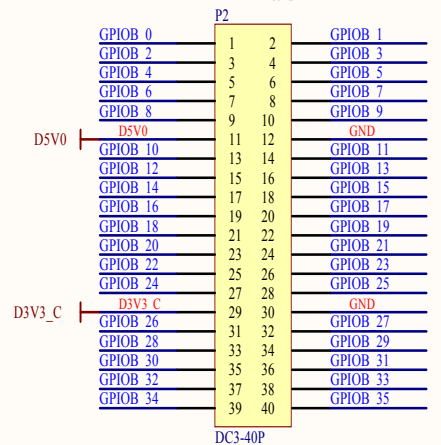
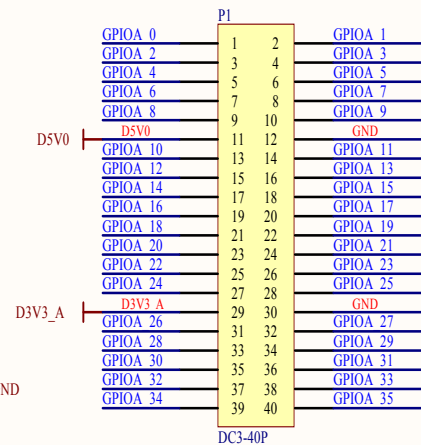
PIN CLK * 6

PIN JTAG * 5

PIN 3.3V * 4

PIN 2.5V * 1

PIN GND * 8



FPGA Core Interface

Size	Number	Revision
A4	Made By CrazyBingo	crazyfpga.com
Date:	2017/5/6	Sheet of
File:	E:\CrazyBingo Information\01 FPGA Core.SchDoc Drawn By:	

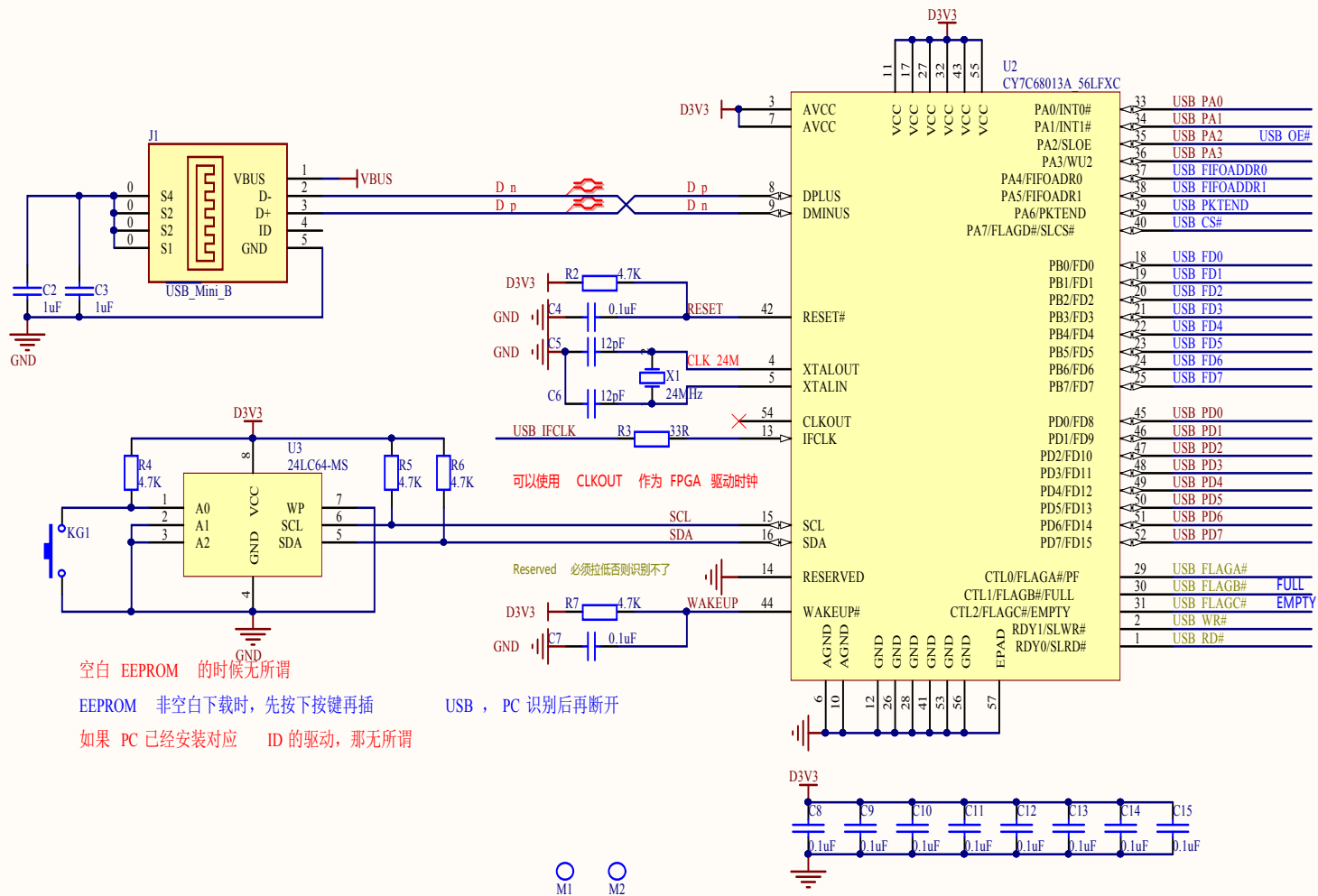
以 I 开头的表示输入型引脚，也是时钟输入引脚，这些引脚只能做输入。后面跟的是

以 IO 开头的表示输入输出型引脚，后面跟的是

FPGA 具体管脚

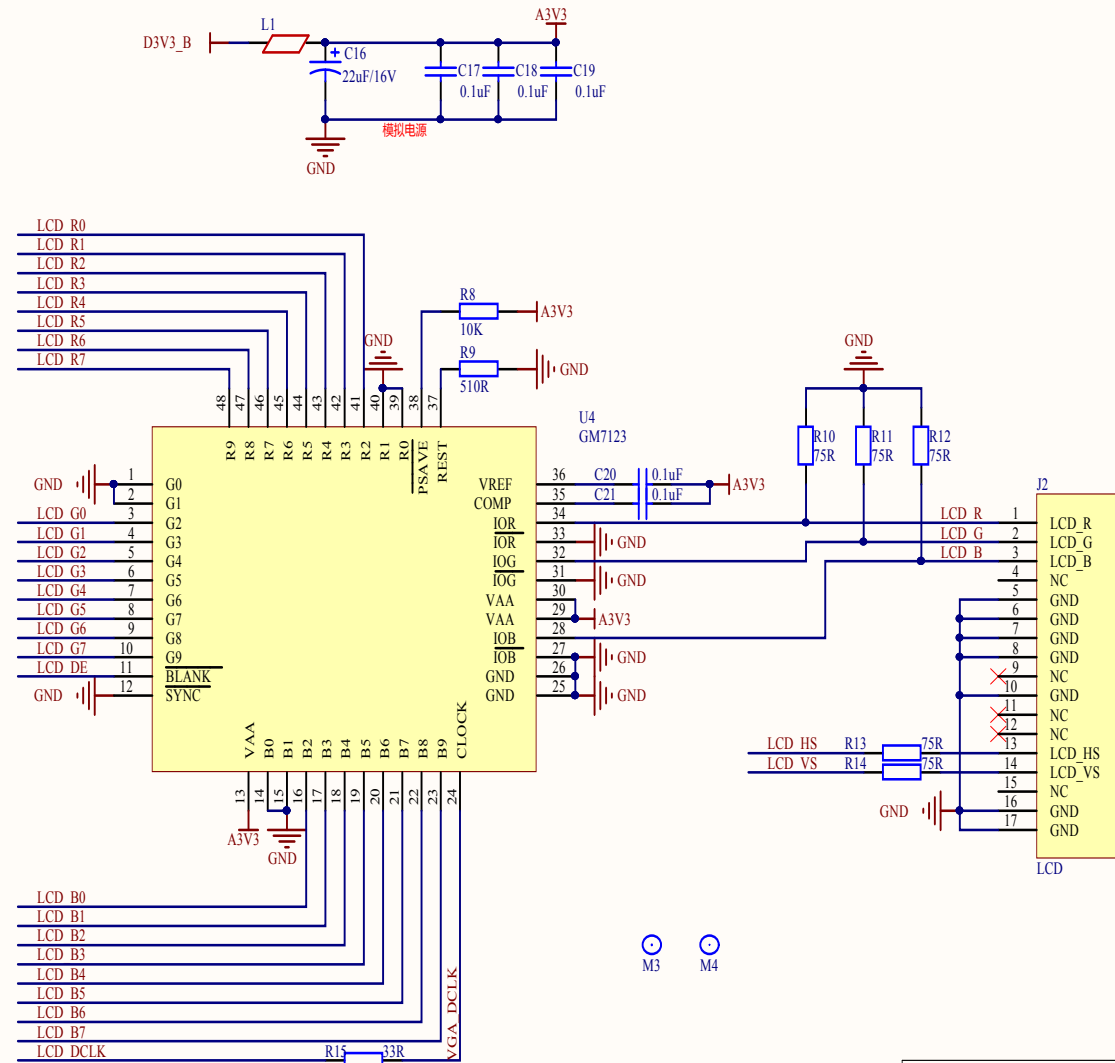
FPGA 具体管脚

VIP_USB2.0 Card V1.0

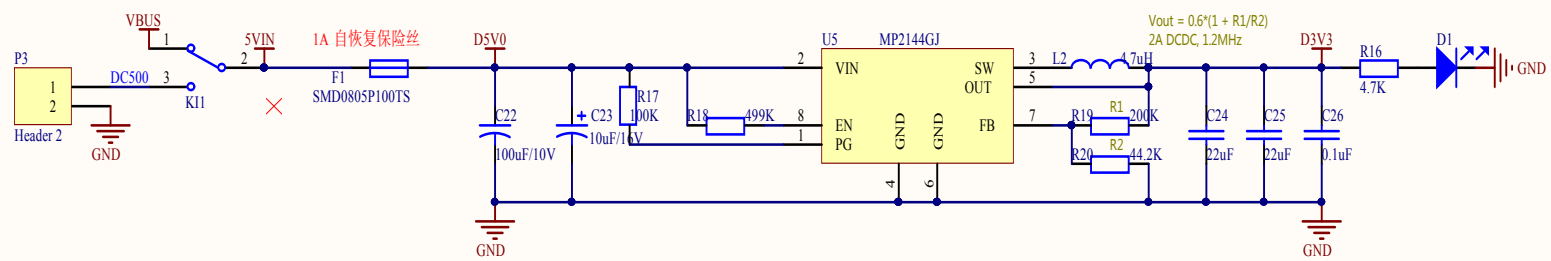


Title			USB2.0 Module		
Size	Number				Revision
A4	Made By CrazyBingo				crazyfpga.com
Date:	2017/5/6		Sheet of		
File:	E:\CrazyBingo Information\02 USB2.0 Module\		Download By:		

ADV7123/GM7123---VGA

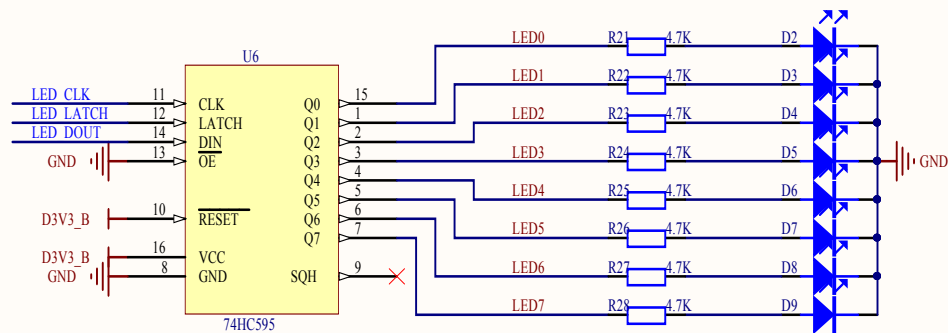


Title		
VGA_RGB888		
Size	Number	Revision
A4	Made By CrazyBingo	crazyfpga.com
Date:	2017/5/6	Sheet of
File:	E:\CrazyBingo Information\03 VGA_RGB888.Sch	
Drawn By:		

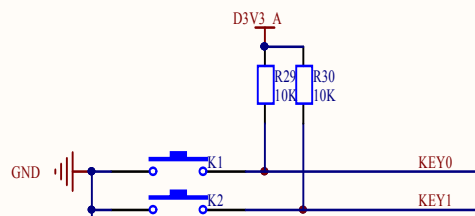


Title			Source		
Size	Number			Revision	
A4	Made By CrazyBingo			crazyfpga.com	
Date:	2017/5/6			Sheet of	
File:	E:\CrazyBingo Information\...\04 Source.SchDoc			Drawn By:	

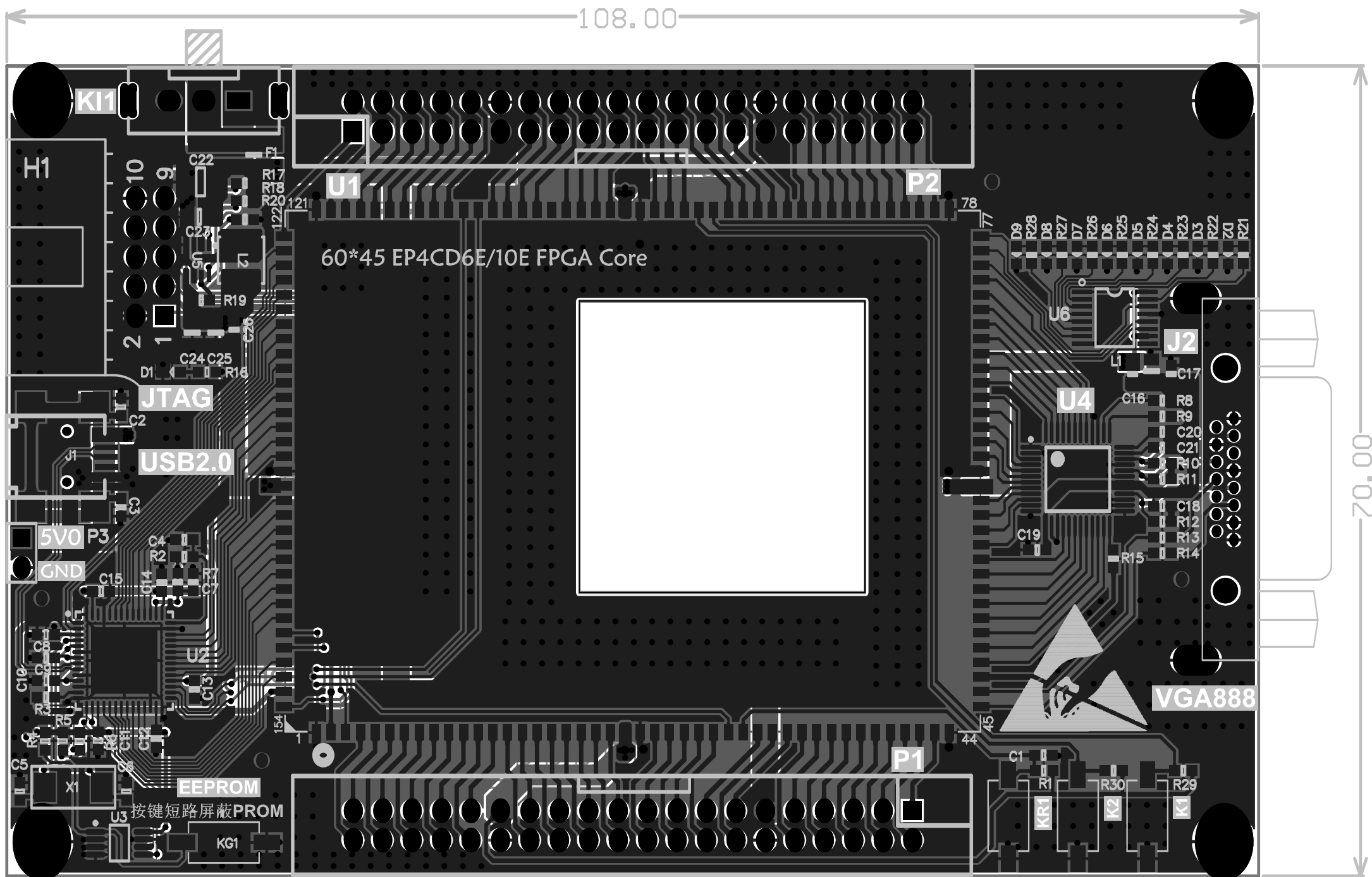
LED



独立按键



Title			User Interface		
Size	Number			Revision	
A4	Made By CrazyBingo			<u>crazyfpga.com</u>	
Date:	2017/5/6		Sheet of		
File:	E:\CrazyBingo Information\05 User Interface.SchDdDrawn By:				



中间keep out layer镂空