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## REVISIONS

ZONE	LTR	DESCRIPTION	DATE	APPR.

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SIZE **C** REV. DRAWING NO.

SCALE SHEET OF

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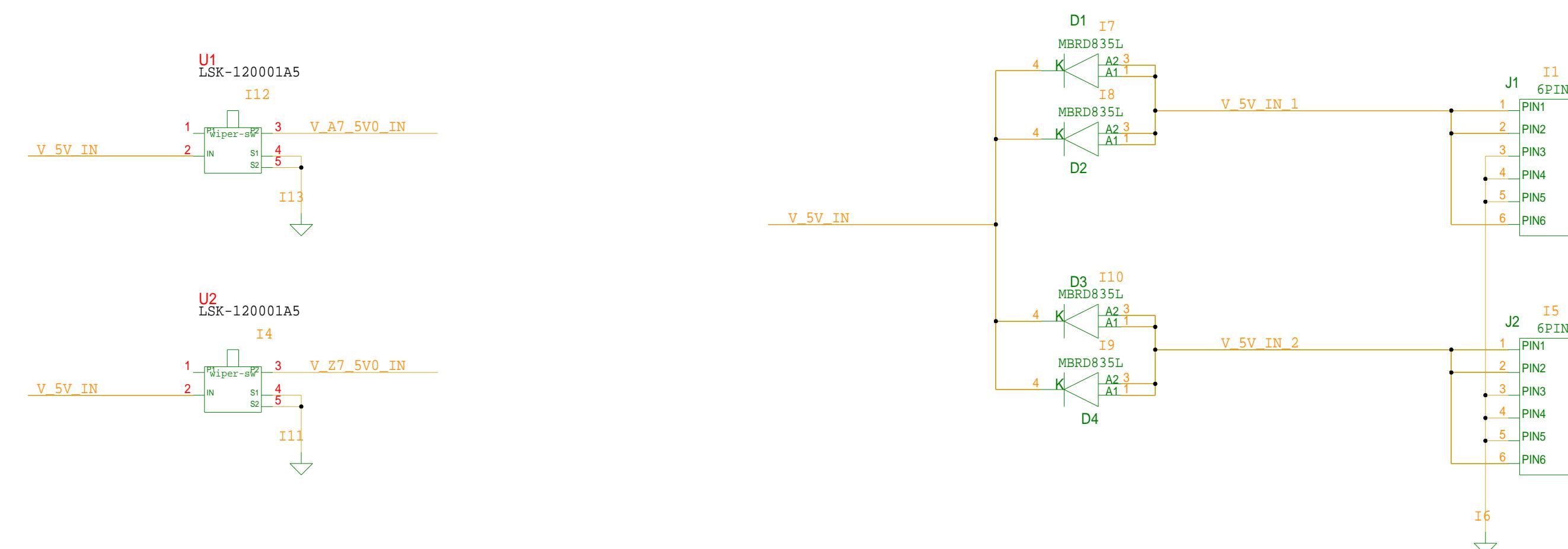
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# MAIN POWER

## REVISIONS

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SIZE **C** REV. DRAWING NO.

SCALE SHEET OF

# ARTIX-7 INDEX

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPR.

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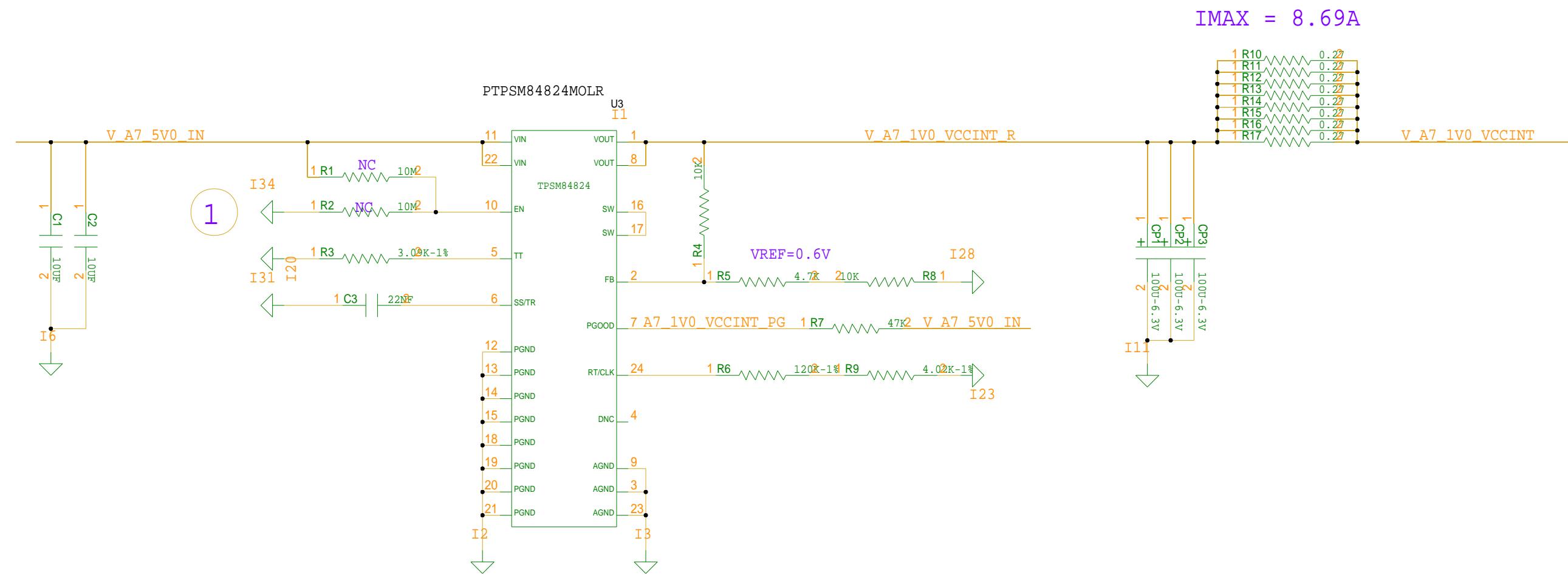
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SIZE	REV.	DRAWING NO.
		
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## REVISED

ZONE	LTR	DESCRIPTION	DATE	APPR.

## ARTIX-7 POWER (1)



SS/TR	6	I	Soft-start and tracking pin. Connecting an external capacitor to this pin adjusts the output voltage soft-start ramp slower than its 1.2 ms default setting. A voltage applied to this pin allows for tracking and sequencing control.
-------	---	---	--

Table 9. Soft-Start Capacitor Values and Soft-Start Time

C <sub>ss</sub> (nF)	open	10	15	22	47
SS Time (ms)	1.2	2.4	3	3.8	6.8

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## ARTIX-7 POWER (2)

$$V_{OUT} = V_{REF} \times (1 + (R_{TOP}/R_{BOT}))$$

$$R_{RT} (\text{k}\Omega) = [14,822/f_{SW} (\text{kHz})]^{1.08}$$

$$V_{IN\_STARTUP} = (0.8 \text{ nA} + (0.8 \text{ V}/R_{BOT\_EN})) \times \left( R_{TOP\_EN} + \frac{R_{BOT\_EN} \times 1 \text{ M}\Omega}{R_{BOT\_EN} + 1 \text{ M}\Omega} \right)$$

where:

$R_{TOP\_EN}$  is the resistor from V<sub>IN</sub> to EN

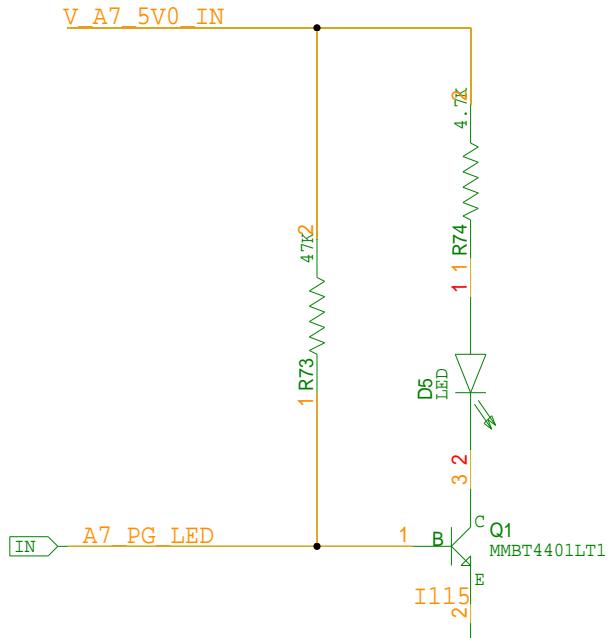
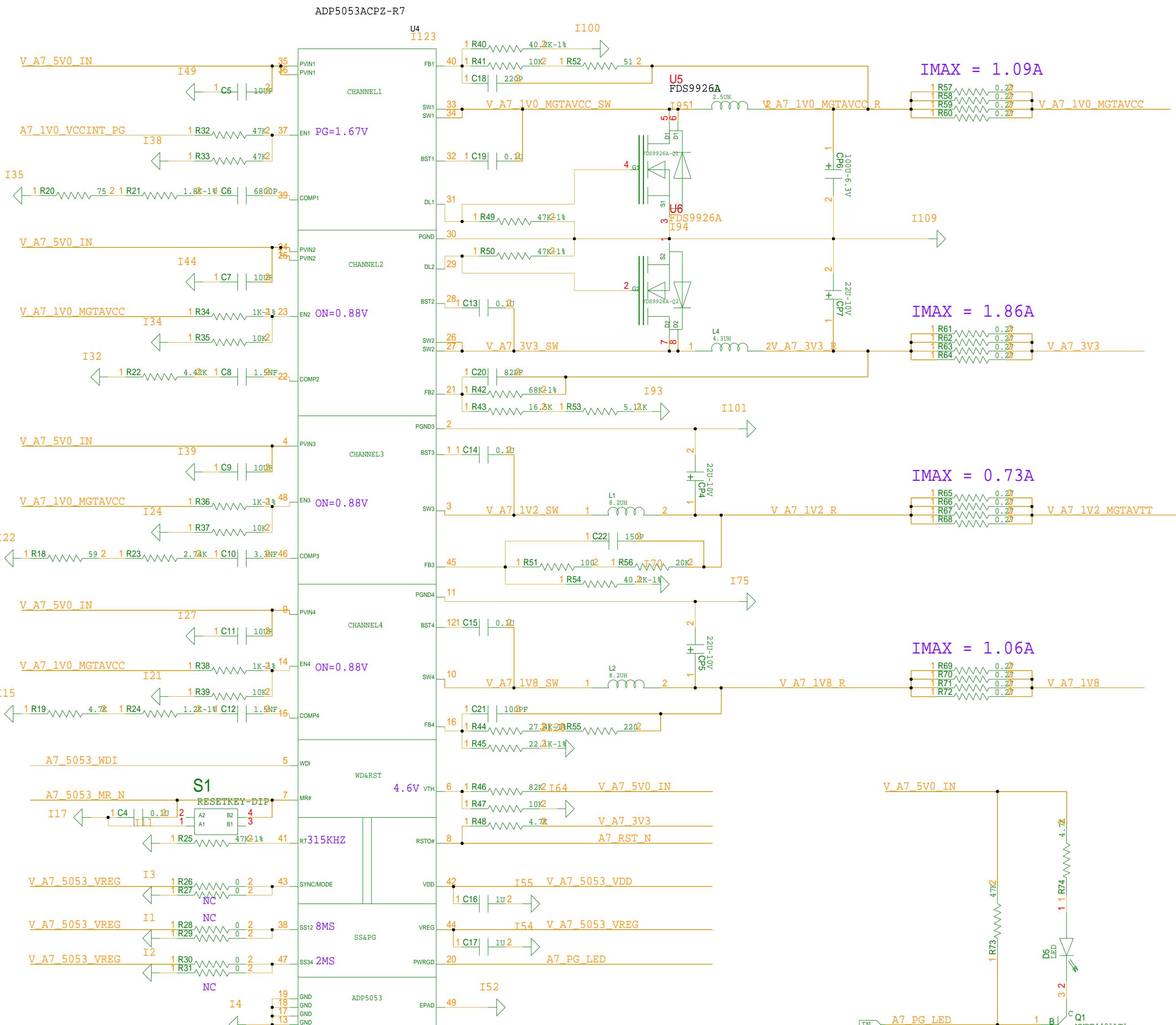
$R_{BOT\_EN}$  is the resistor from EN to ground

**Table 9.** Soft Start Time Set by the SS12 and SS34 Pin

R <sub>TOP</sub> (kΩ)	R <sub>BOT</sub> (kΩ)	Soft Start Time			
		Channel 1	Channel 2	Channel 3	Channel 4
0	N/A <sup>1</sup>	2 ms	2 ms	2 ms	2 ms
100	600	2 ms	Parallel	2 ms	4 ms
200	500	2 ms	8 ms	2 ms	8 ms
300	400	4 ms	2 ms	4 ms	2 ms
400	300	4 ms	4 ms	4 ms	4 ms
500	200	8 ms	2 ms	4 ms	8 ms
600	100	8 ms	Parallel	8 ms	2 ms
N/A <sup>1</sup>	0	8 ms	8 ms	8 ms	8 ms

**Table 16. Factory Default Options**

Option	Default Value
Channel 1 Output Voltage	0.8 V adjustable output
Channel 2 Output Voltage	0.8 V adjustable output
Channel 3 Output Voltage	0.8 V adjustable output
Channel 4 Output Voltage	0.8 V adjustable output
PWRGD Pin (Pin 20) Output	Monitor Channel 1 output
Output Discharge Function	Enabled for all four buck regulators
Switching Frequency on Channel 1	1 × switching frequency set by the RT pin
Switching Frequency on Channel 3	1 × switching frequency set by the RT pin
SYNC/MODE Pin (Pin 43) Function	Forced PWM/automatic PWM/PSM mode setting with the ability to synchronize to an external clock
Hiccup Protection	Enabled for overcurrent events
Short-Circuit Latch-Off Function	Disabled for output short-circuit events
Oversupply Latch-Off Function	Disabled for output oversupply events
Reset Timeout Period	200 ms
Watchdog Timeout Period	1.6 sec
Manual Reset Input Mode	Processor manual reset mode



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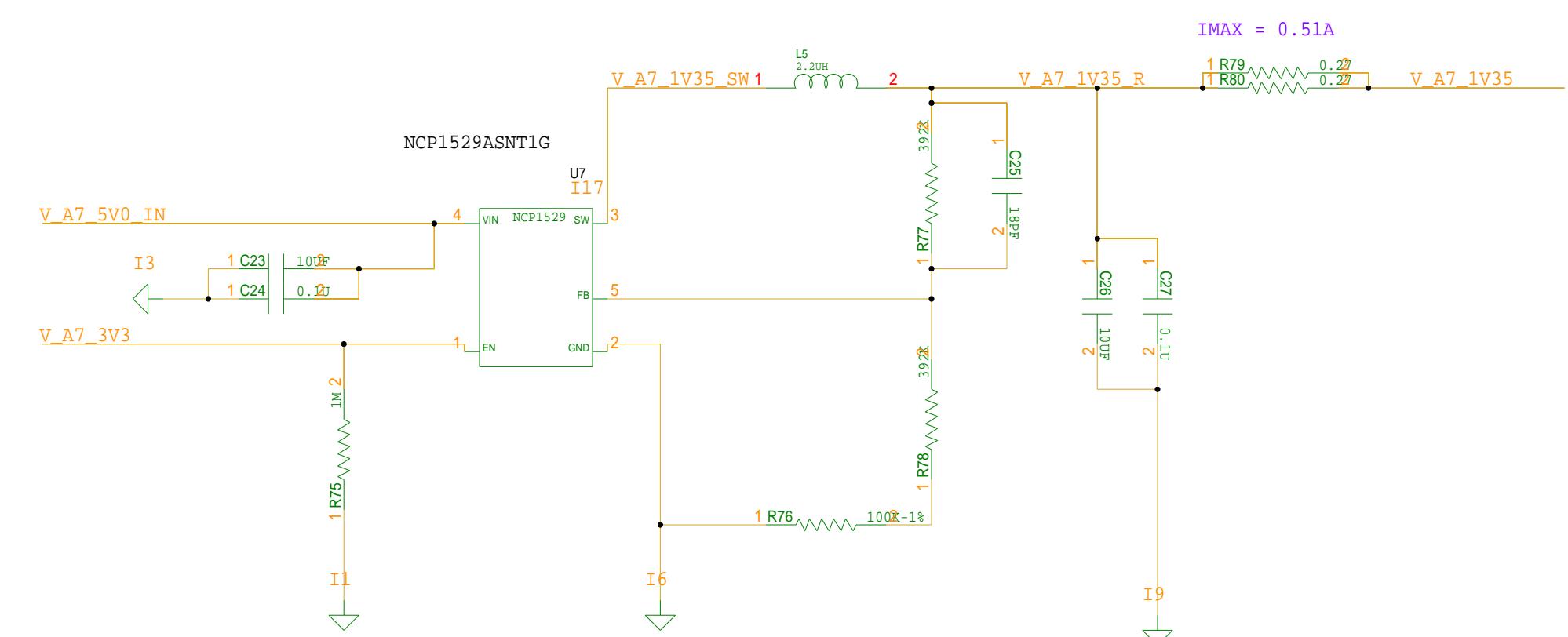
# ARTIX-7 POWER (3)

REVISED		DESCRIPTION		DATE	APPR.
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$$V_{out} = V_{FB} \times (1 + R1/R2)$$

- $V_{OUT}$ : Output Voltage (V)
- $V_{FB}$ : Feedback Voltage = 0.6 V
- $R1$ : Feedback Resistor from  $V_{OUT}$  to FB
- $R2$ : Feedback Resistor from FB to GND

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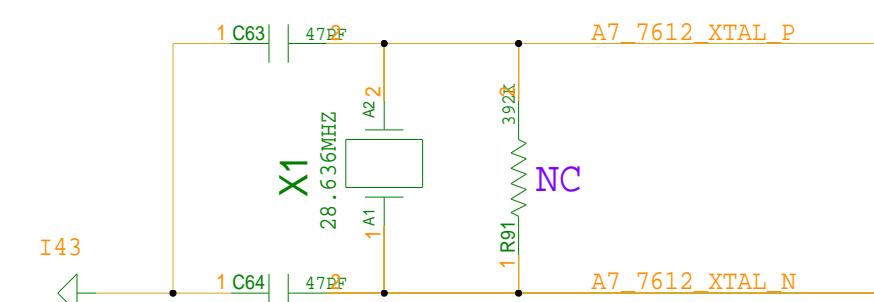
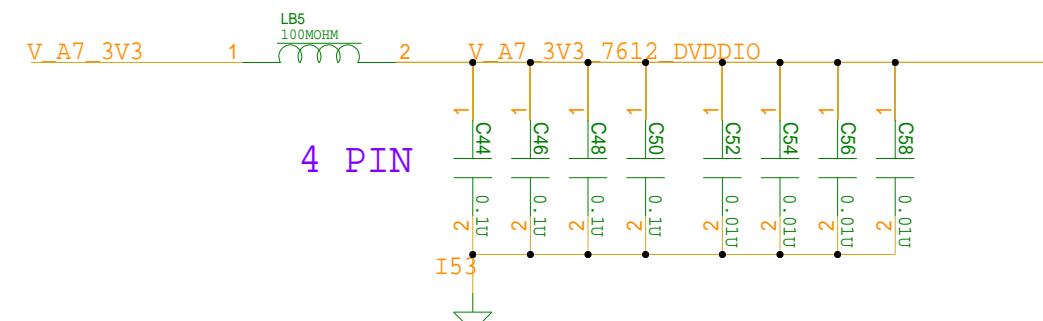
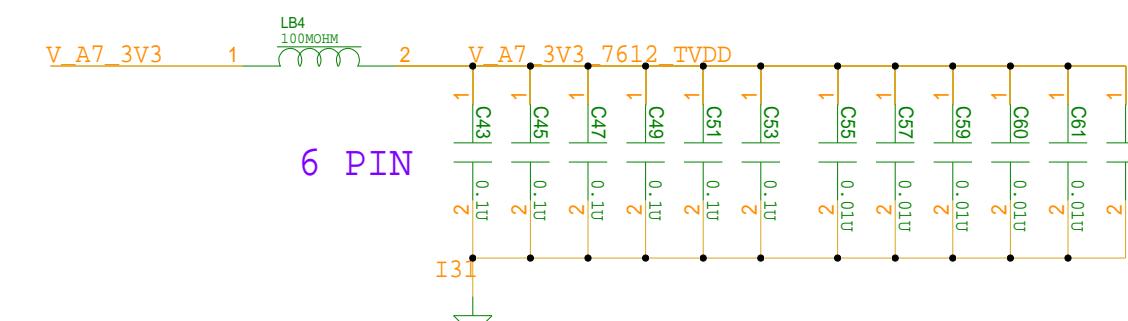
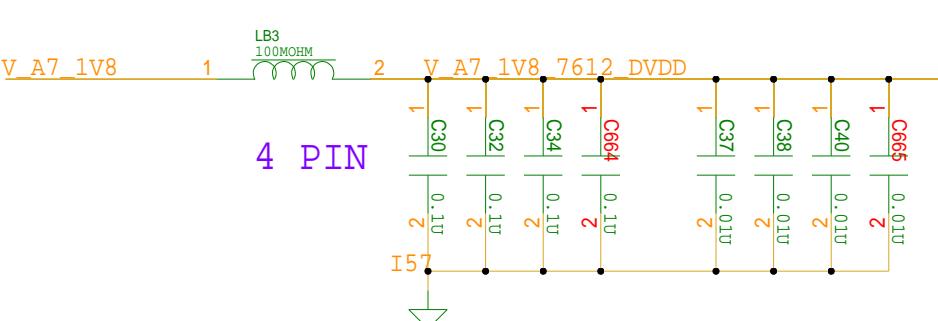
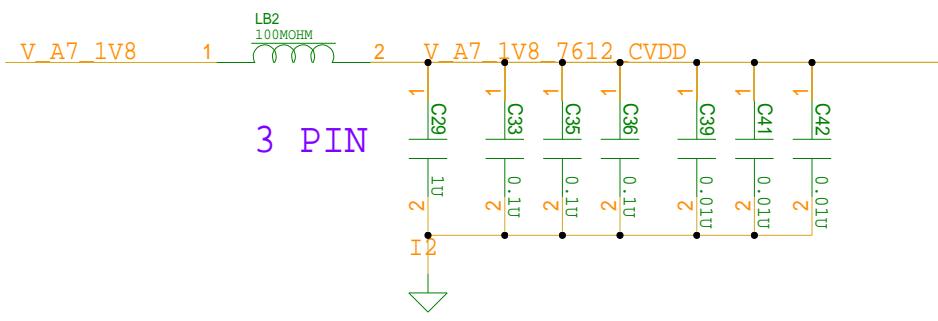
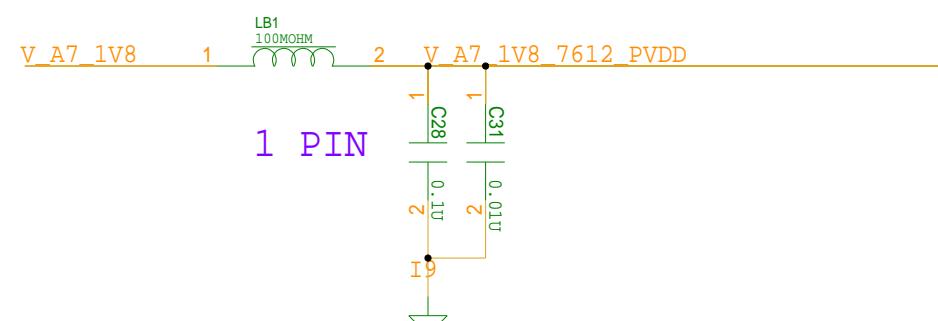
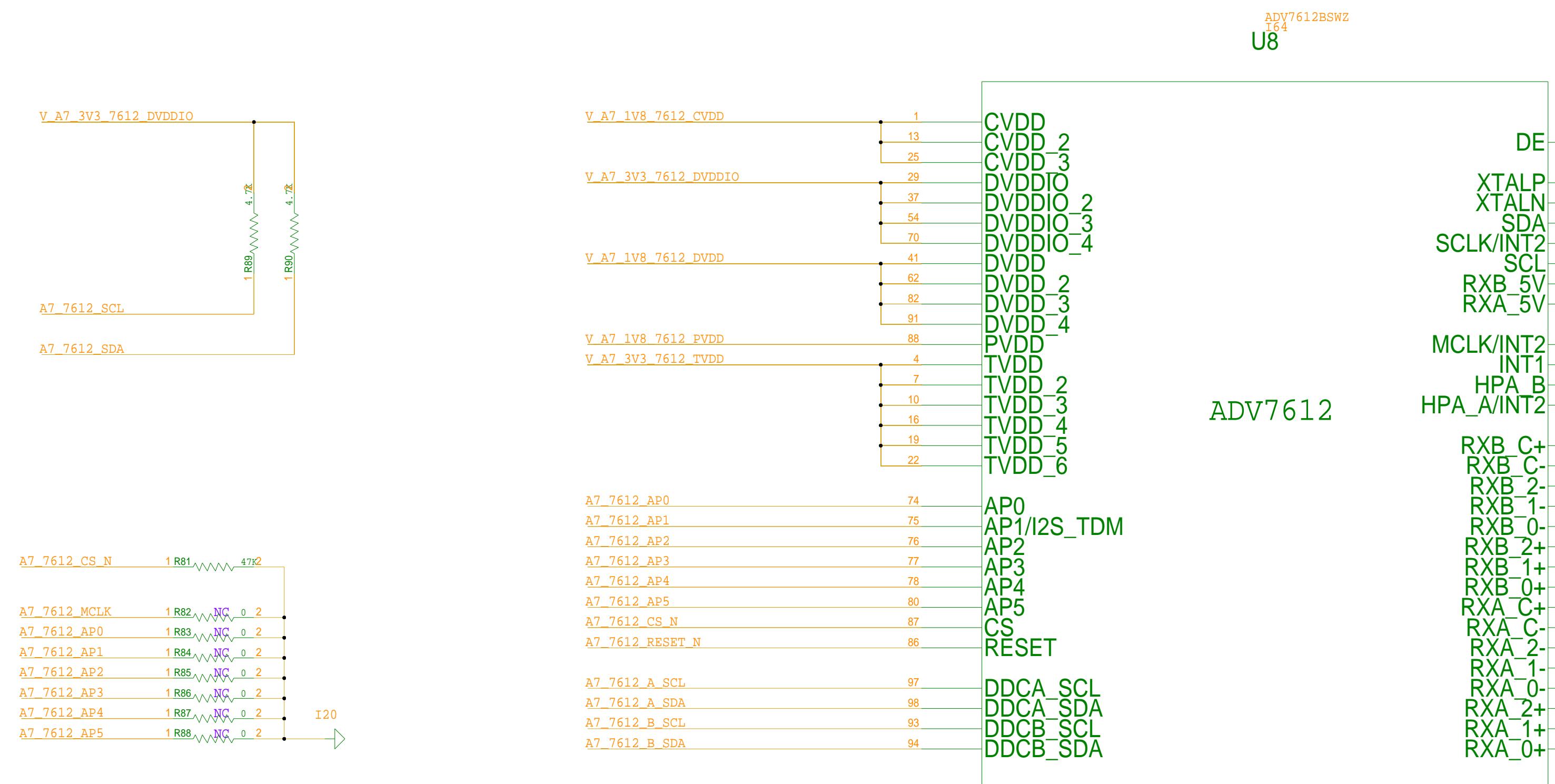
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# ARTIX-7 HDMI RECEIVER (1)

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SCALE SHEET OF

# ARTIX-7 HDMI RECEIVER (2)

REVISIONS				
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A7_7612_P4	65	P4
A7_7612_P5	64	P5
A7_7612_P6	63	P6
A7_7612_P7	61	P7
A7_7612_P8	60	P8
A7_7612_P9	59	P9
A7_7612_P10	58	P10
A7_7612_P11	57	P11
A7_7612_P12	56	P12
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A7_7612_P31	32	P31
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A7_7612_P35	27	P35



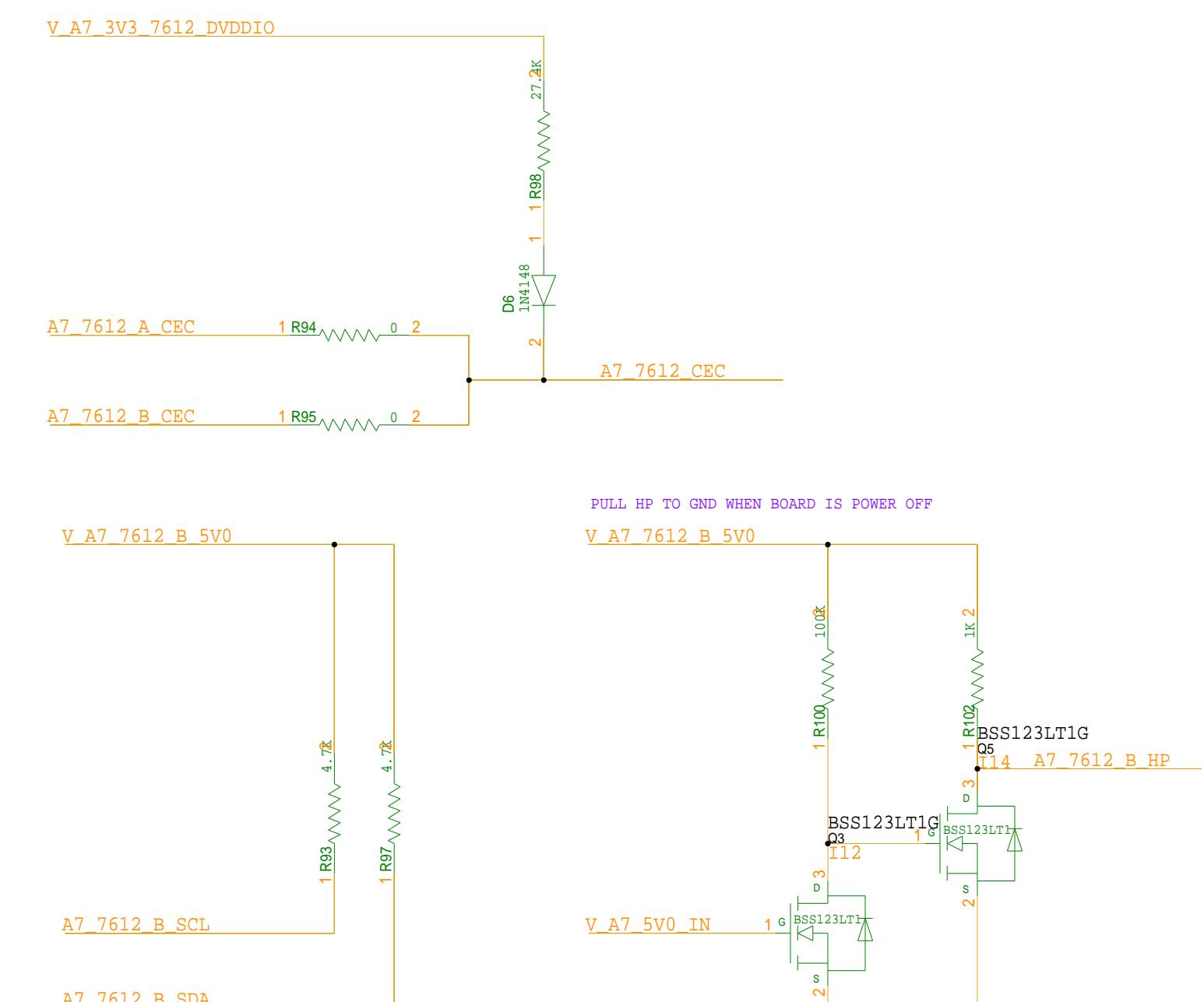
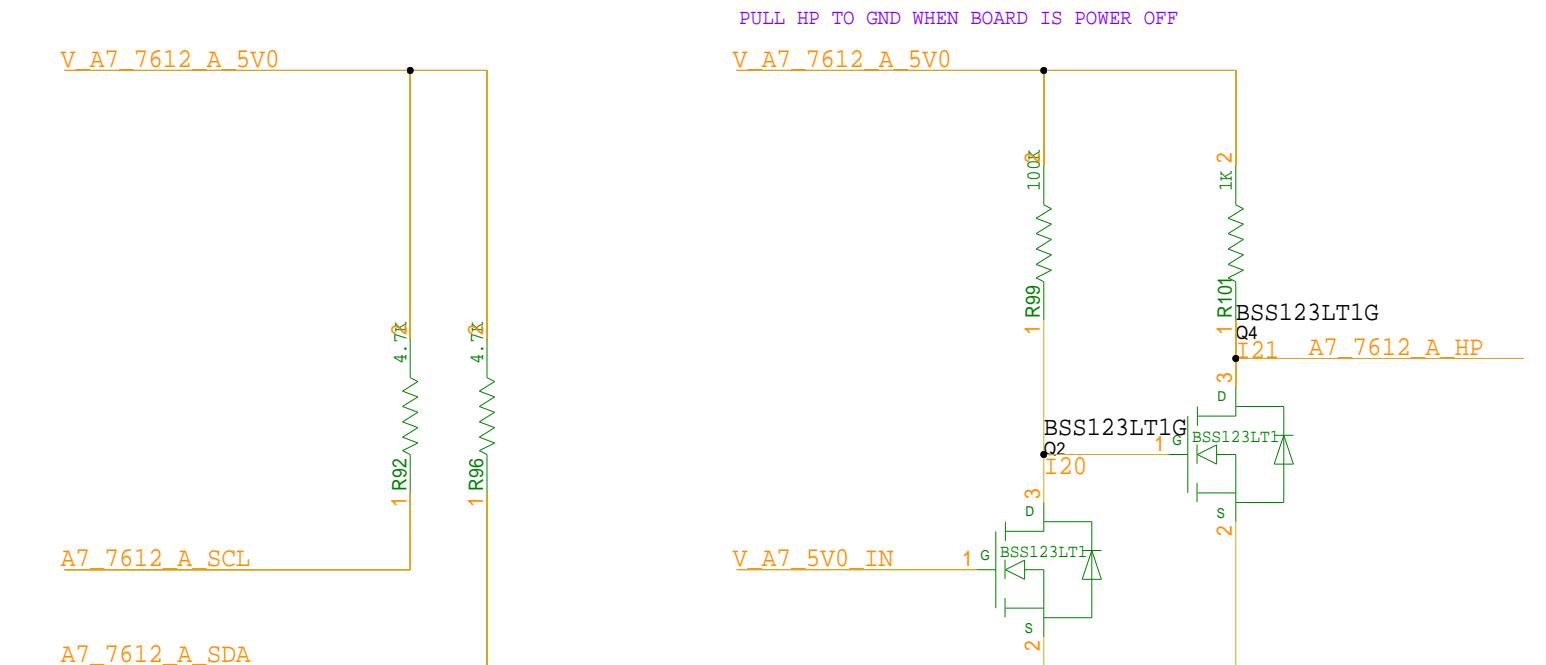
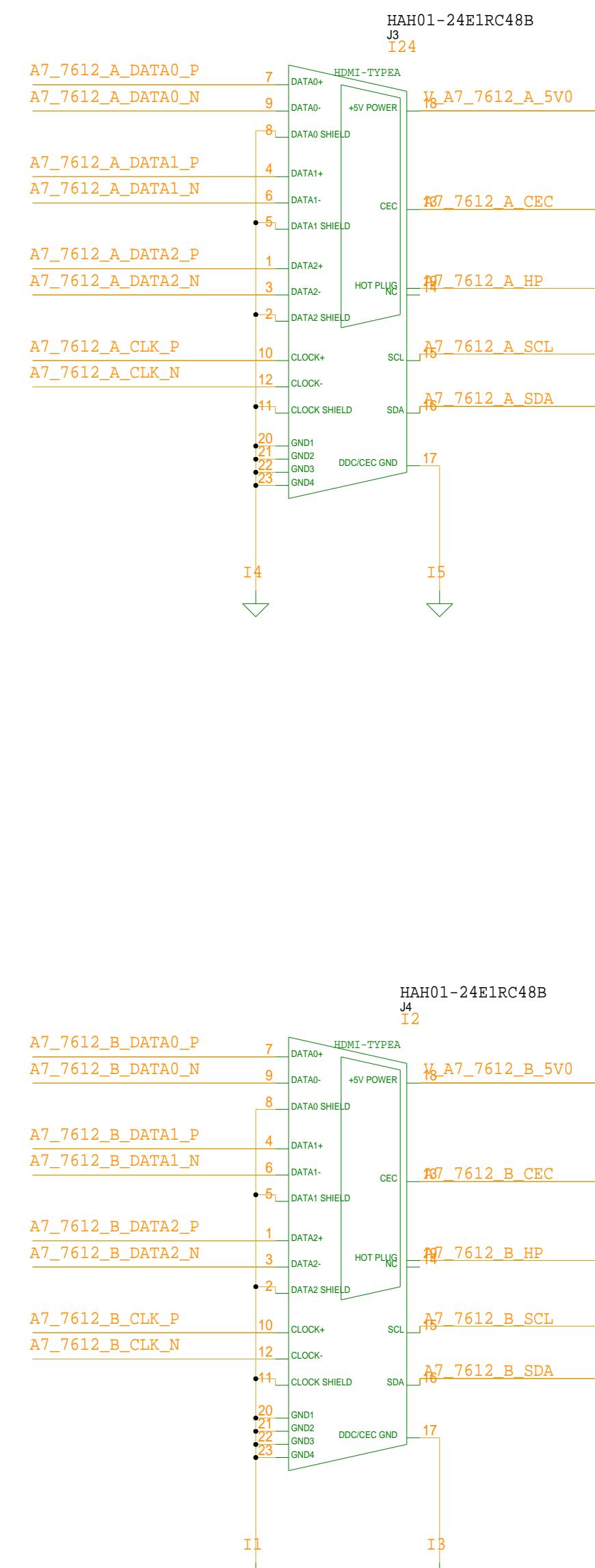
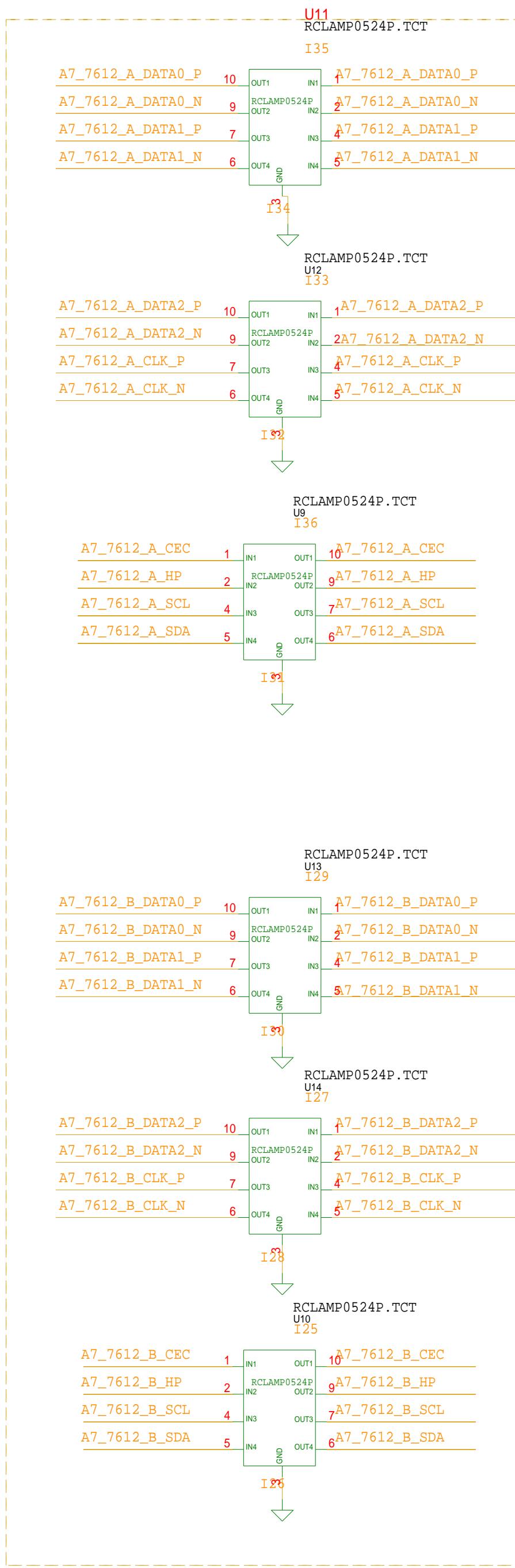
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# ARTIX-7 HDMI RECEIVER (3)

CHANGE CONNECTION DUE TO LAYOUT



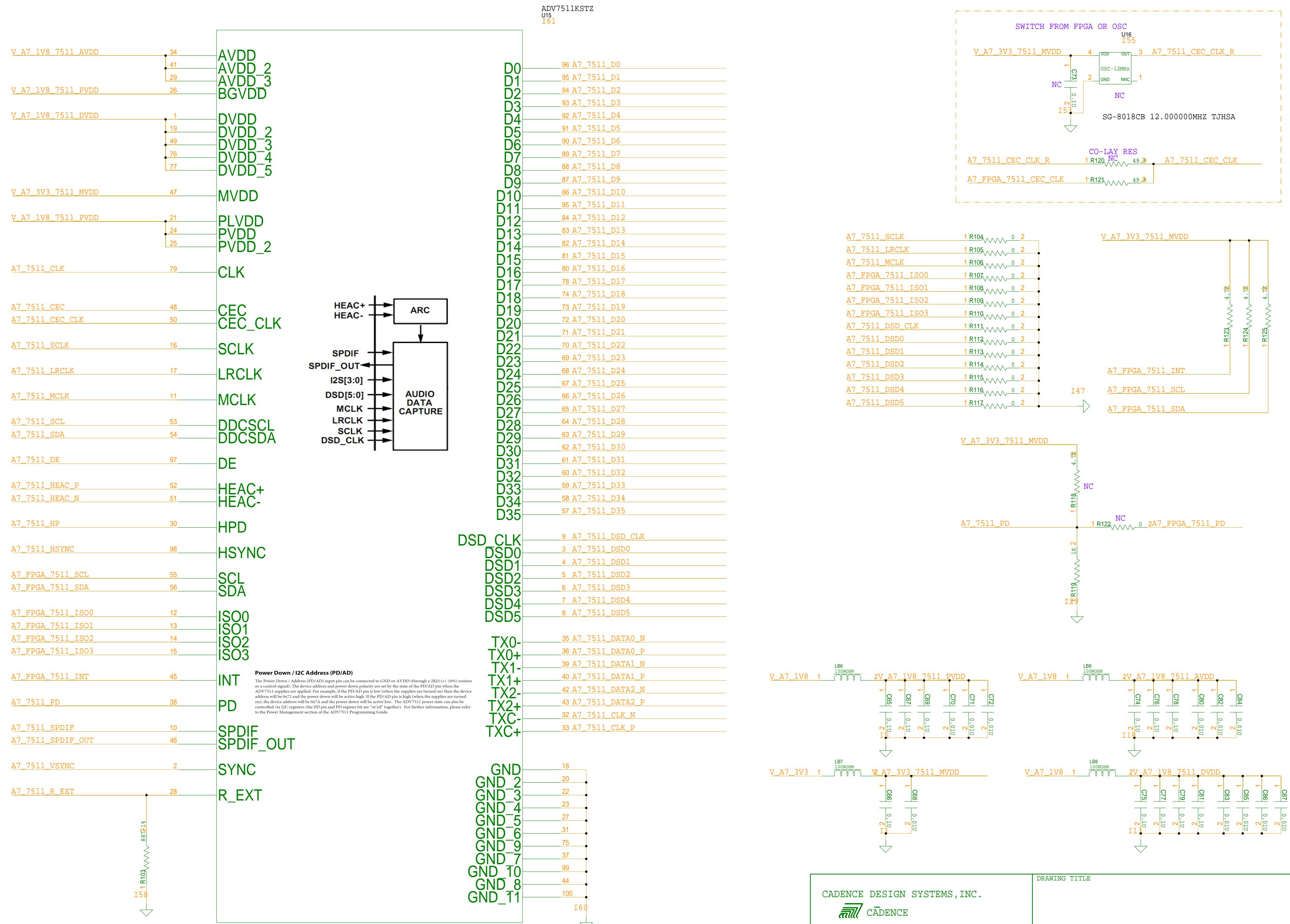
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SIZE	REV.	SCALE	HEET
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# ARTIX-7 HDMI TRANSMITTER (1)

8	7	6	5	4	3	2	1
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ZONE		LTR		DESCRIPTION		DATE	APPR.



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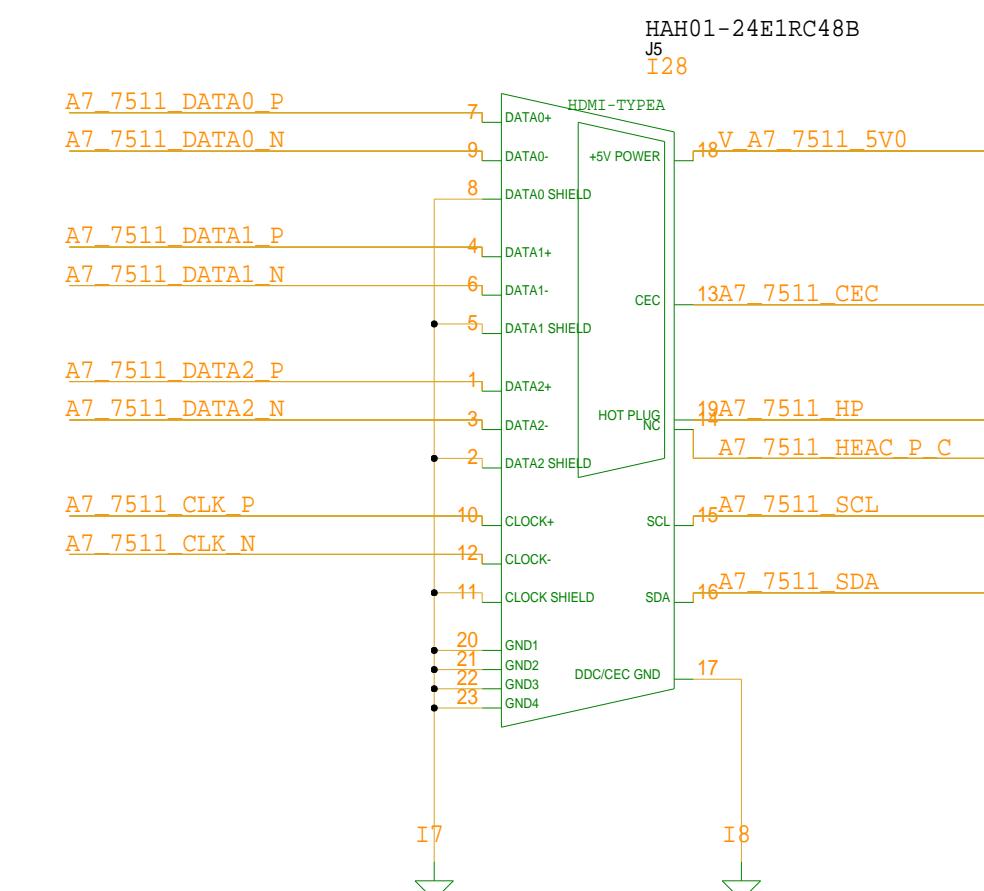
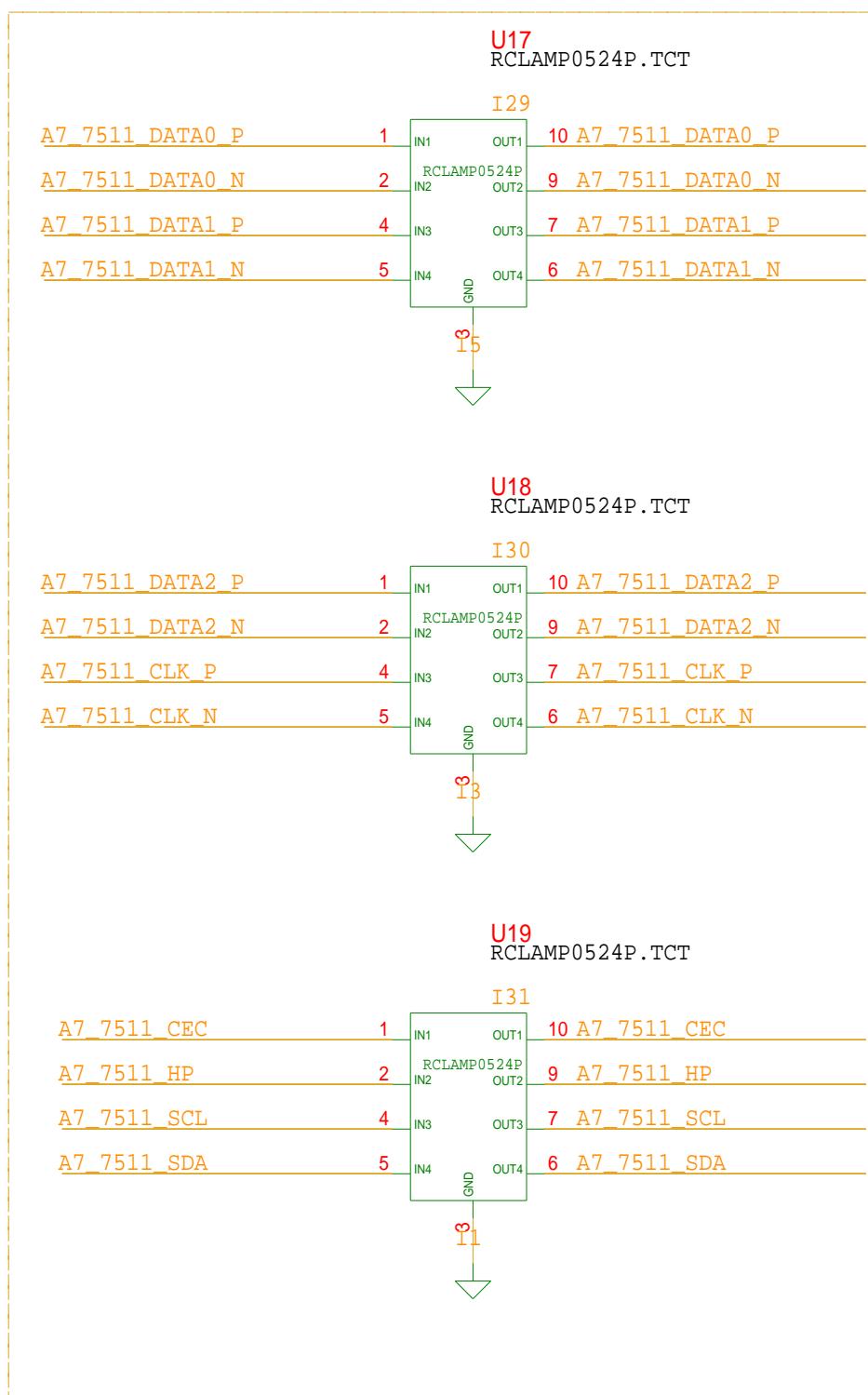
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# ARTIX-7 HDMI TRANSMITTER (2)

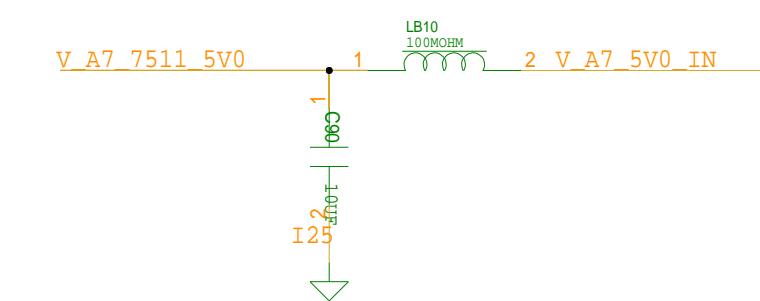
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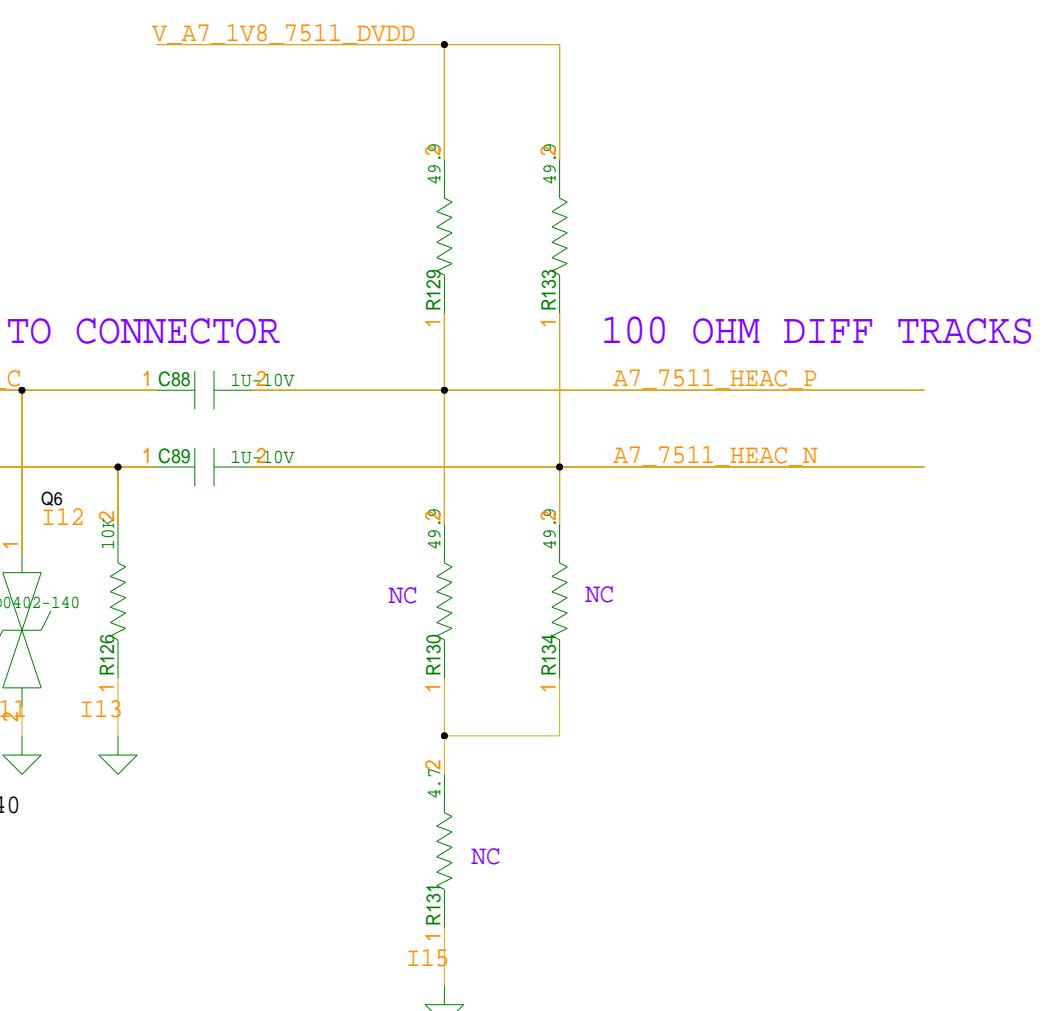
CHANGE CONNECTION DUE TO LAYOUT



CLOSE TO HDMI CONNECTOR



A7\_7511\_CEC → D7 IN4148 → 1 R132 → 27.2k V\_A7\_3V3\_7511\_MVDD



CAPS CLOSE TO CONNECTOR

A7\_7511\_HEAC\_P\_C → 1 C88 → 1U20V → A7\_7511\_HEAC\_P

A7\_7511\_HP → 1 C89 → 1U20V → A7\_7511\_HEAC\_N

NC → 1 R130 → 4.7Ω → 1 R131 → NC

NC → 1 R132 → 4.7Ω → 1 R133 → NC

PESD0402-140 → 1 R120 → 10Ω → 1 R112 → 1 R113 → NC

1 R129 → 4.7Ω → 1 R134 → NC

1 R131 → 4.7Ω → 1 R135 → NC

1 R132 → 4.7Ω → 1 R136 → NC

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1 R241 → 4.7Ω → 1 R245

## ARTIX-7 HDMI INOUT (1)

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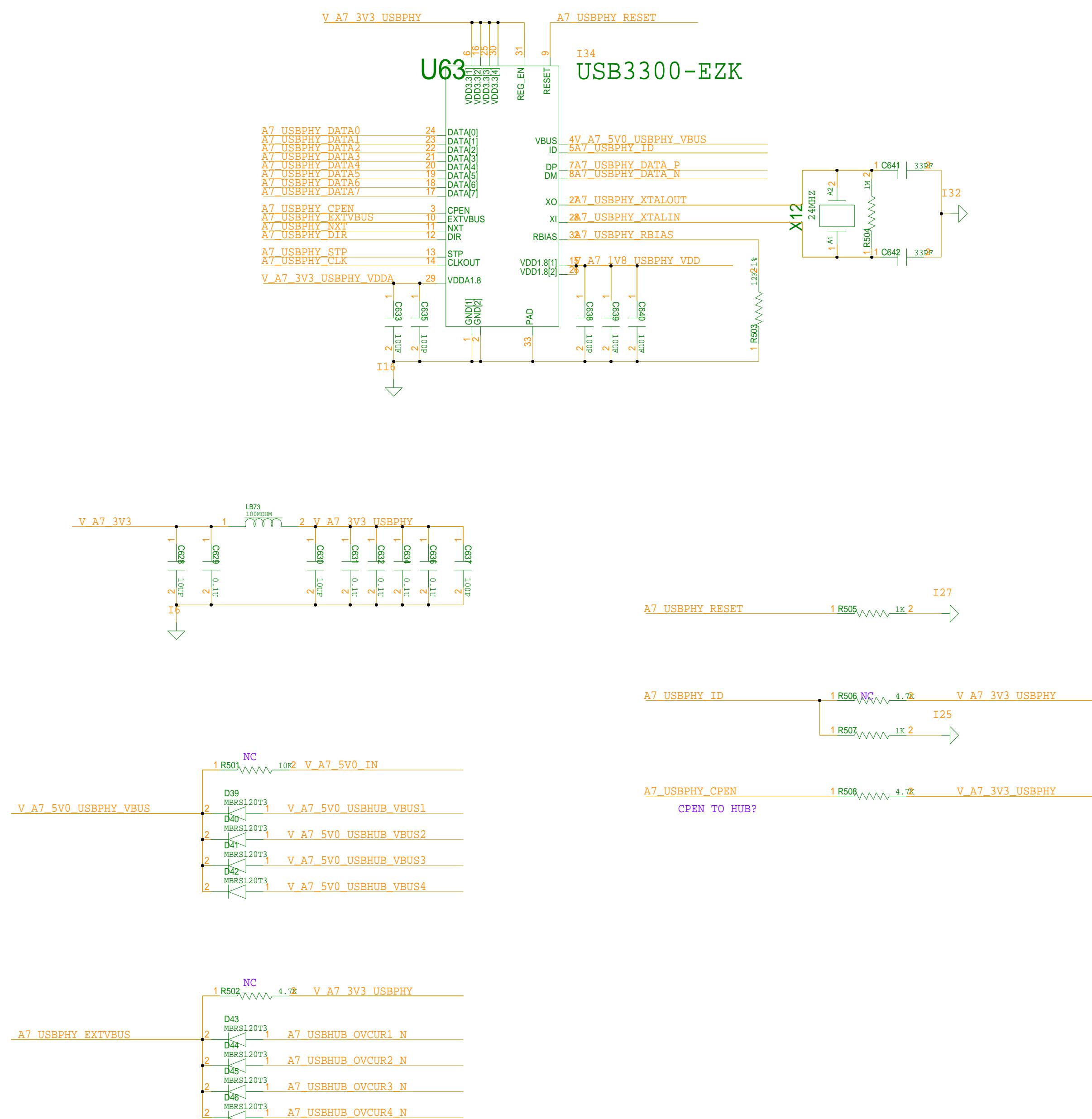
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# ARTIX-7 USB PHY (1)

## REVOLUTIONS

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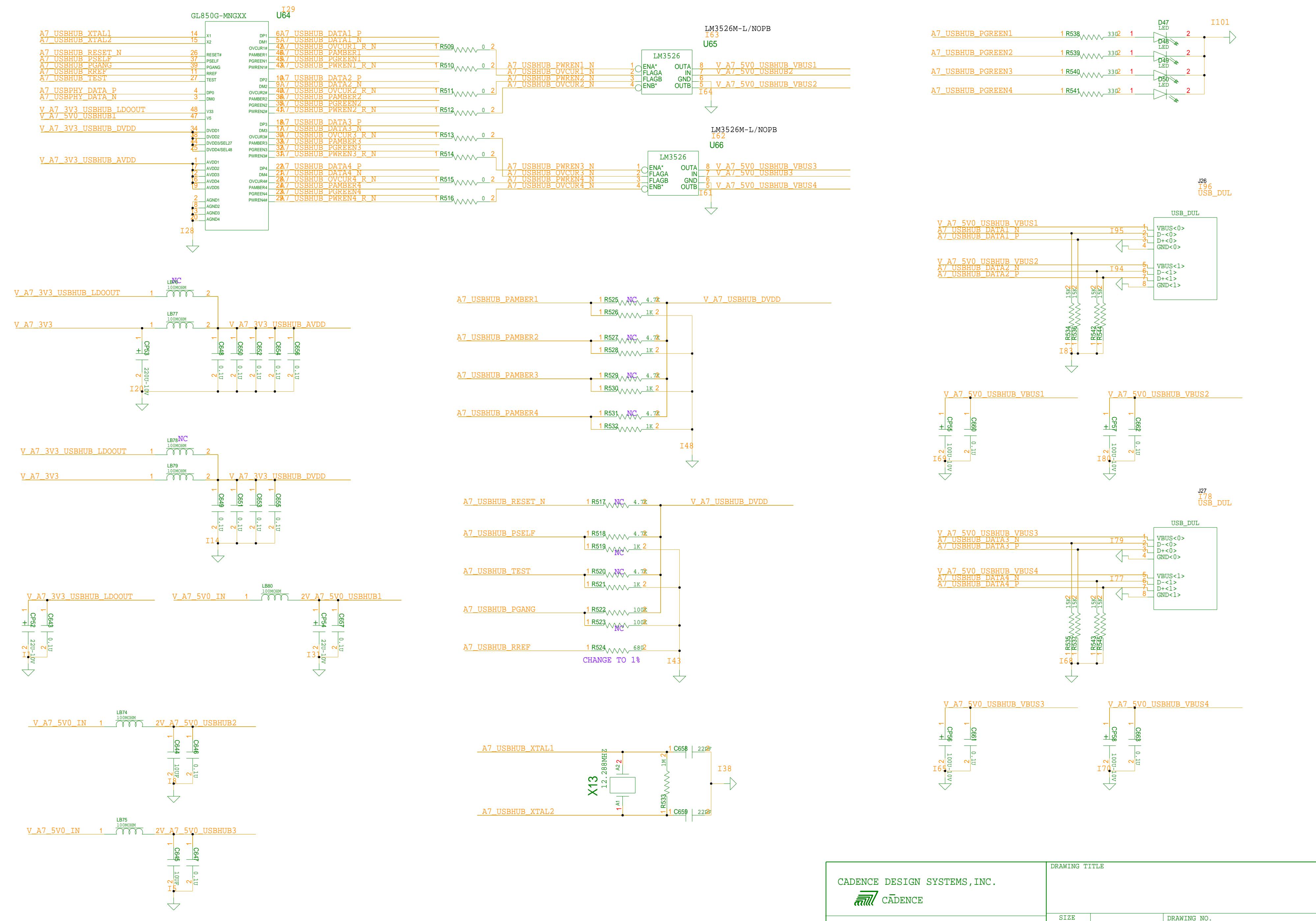
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SCALE	SHEET	OF	REV.	SCALE	SHEET	OF	

# ARTIX-7 USB PHY (2)

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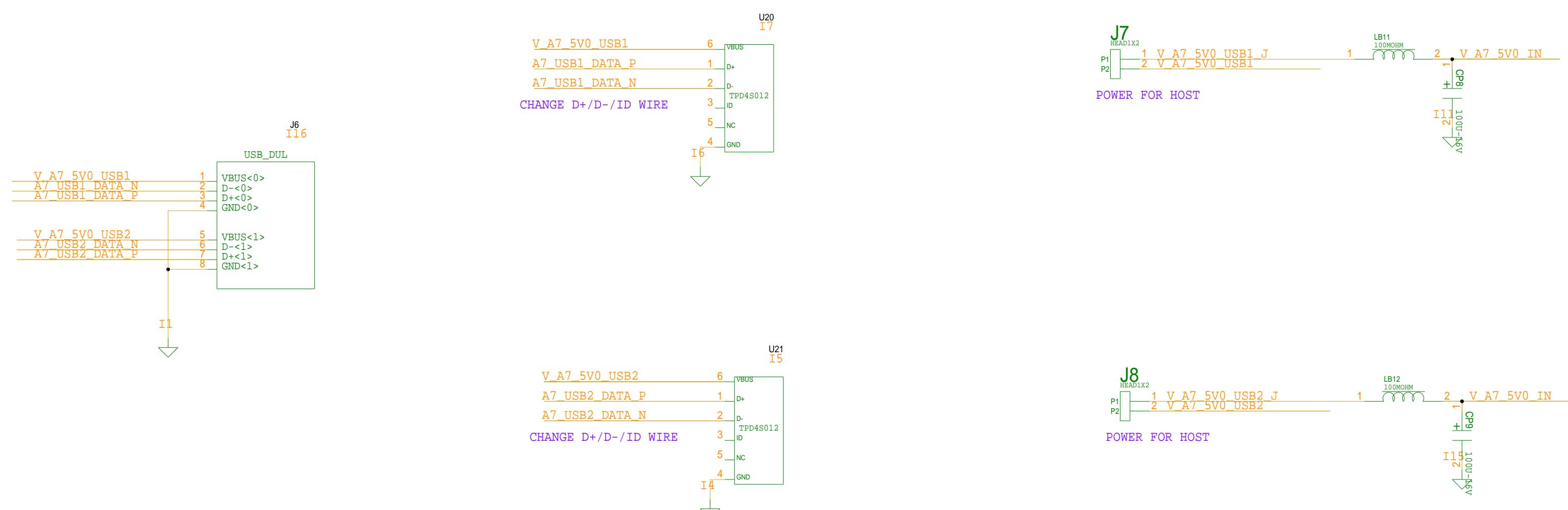
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# ARTIX-7 USB INOUT

## REVOLUTIONS

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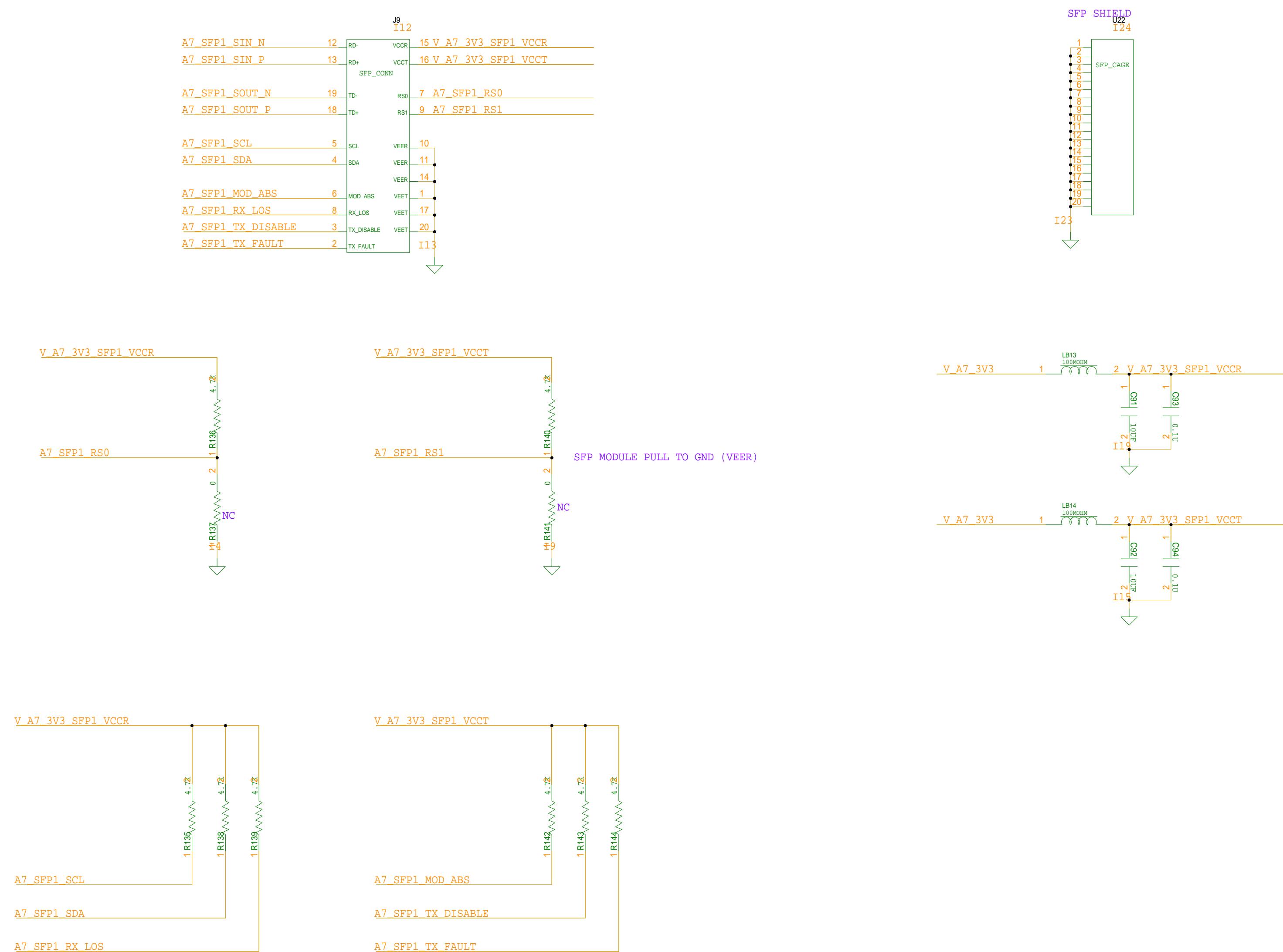
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ZONE	LTR	DESCRIPTION	DATE	APPR.

## ARTIX-7 SFP+/SFP INOUT (1)



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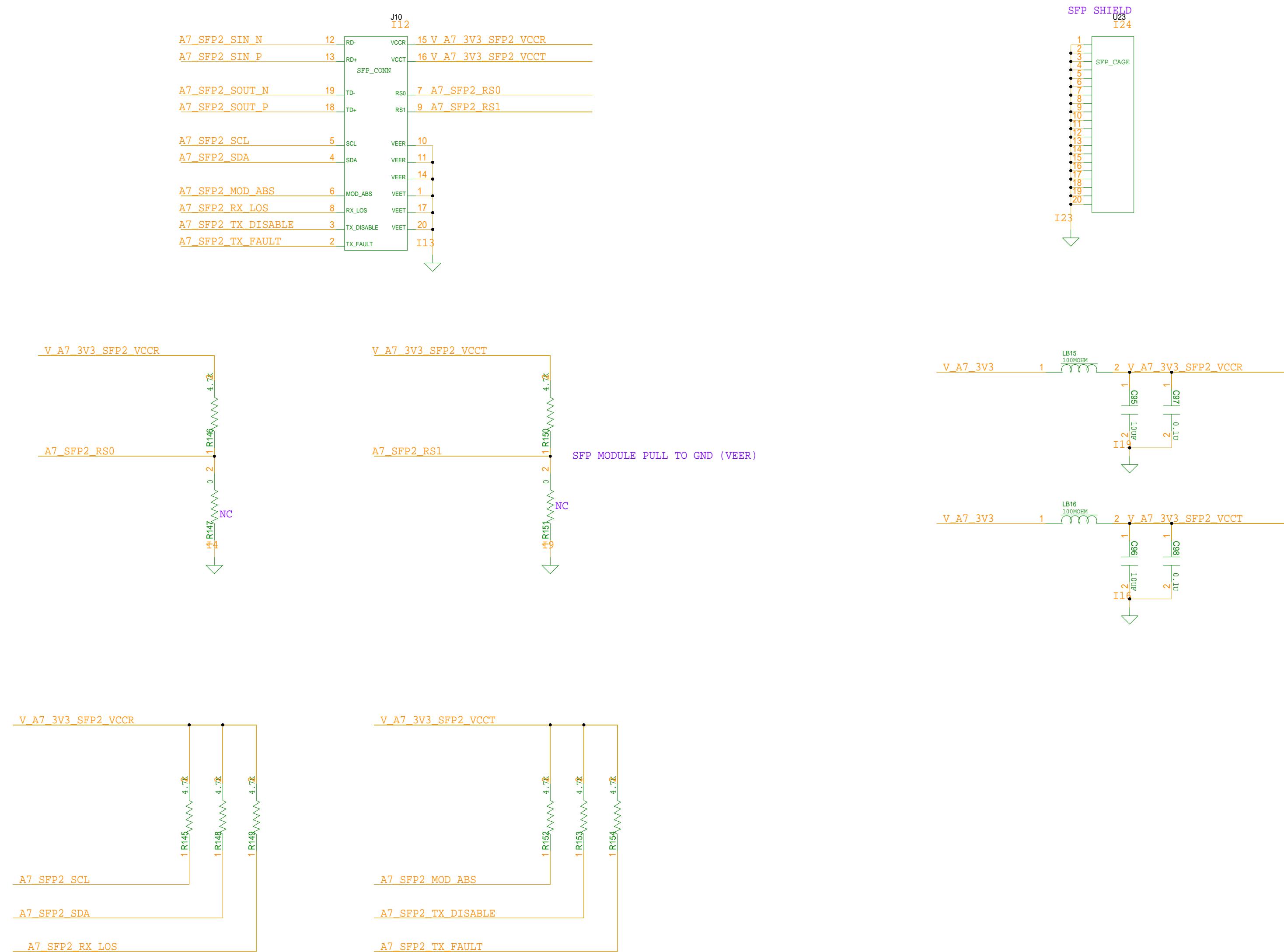
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## ARTIX-7 SFP+/SFP INOUT (2)



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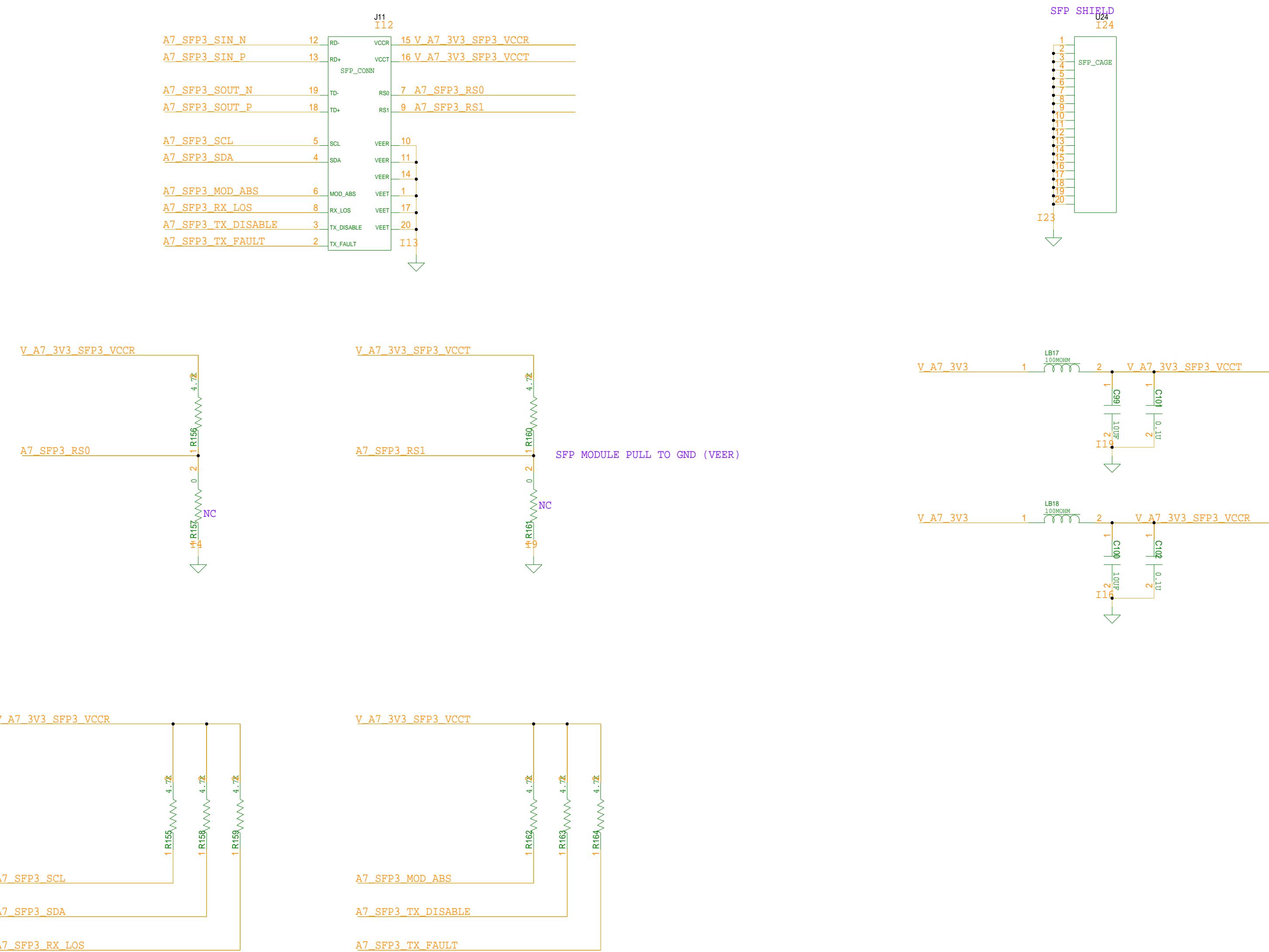
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# ARTIX-7 SFP+/SFP INOUT (3)

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ZONE	LTR	DESCRIPTION	DATE	APPR.

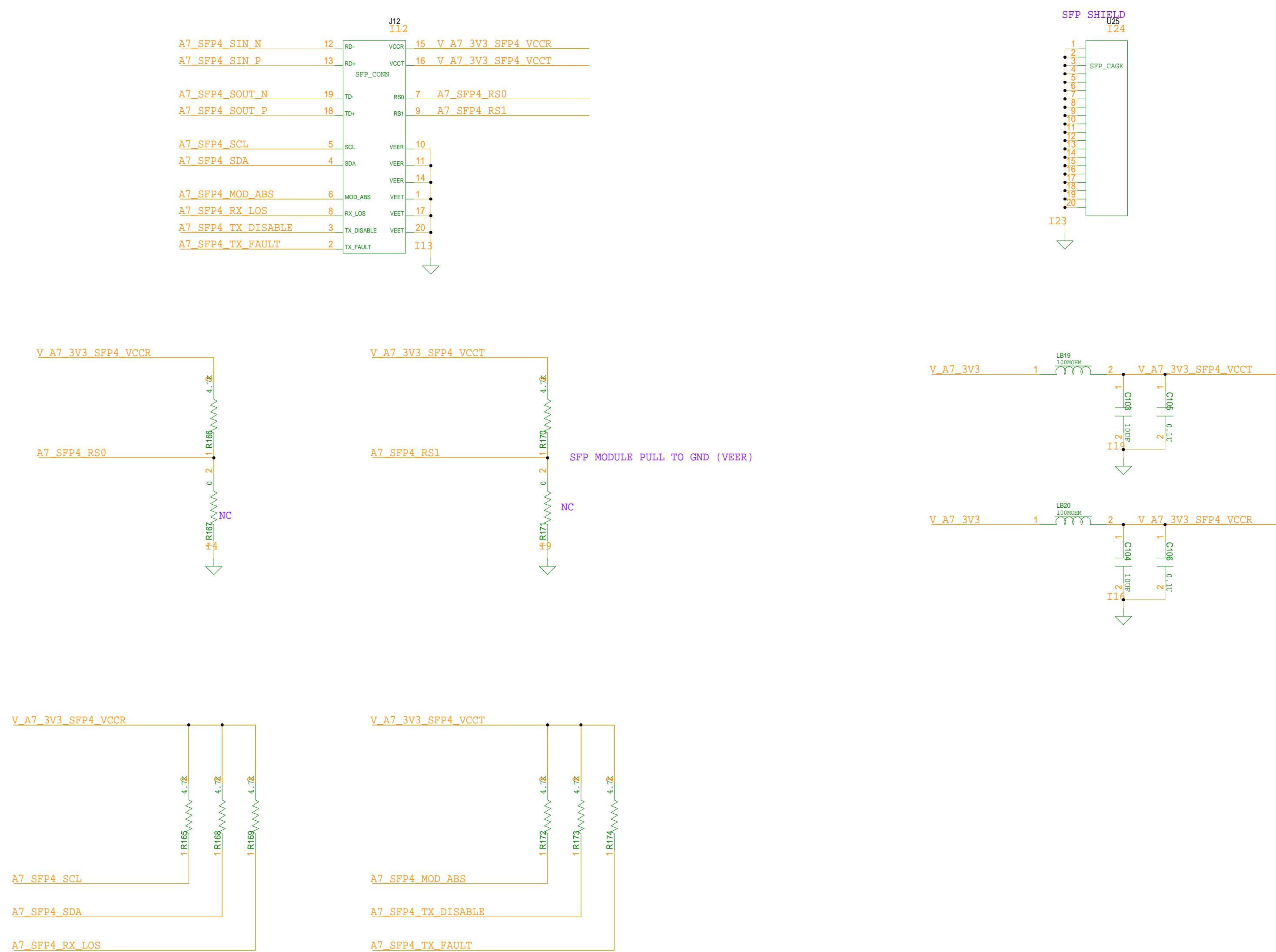


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## REVISIONS

ZONE	LTR	DESCRIPTION	DATE	APPR.

## ARTIX-7 SFP+/SFP INOUT (4)



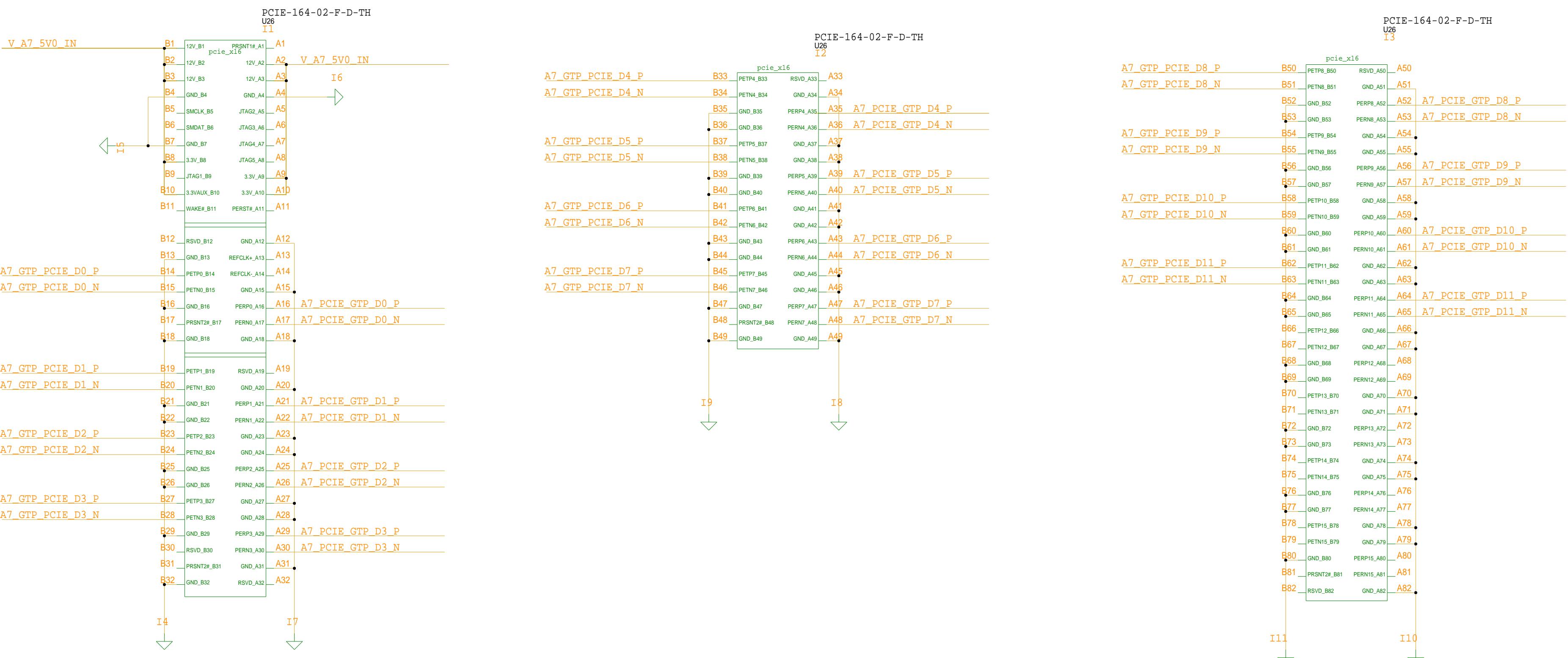
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# ARTIX-7 PCIE X16 CONN

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ZONE	LTR	DESCRIPTION	DATE	APPR.



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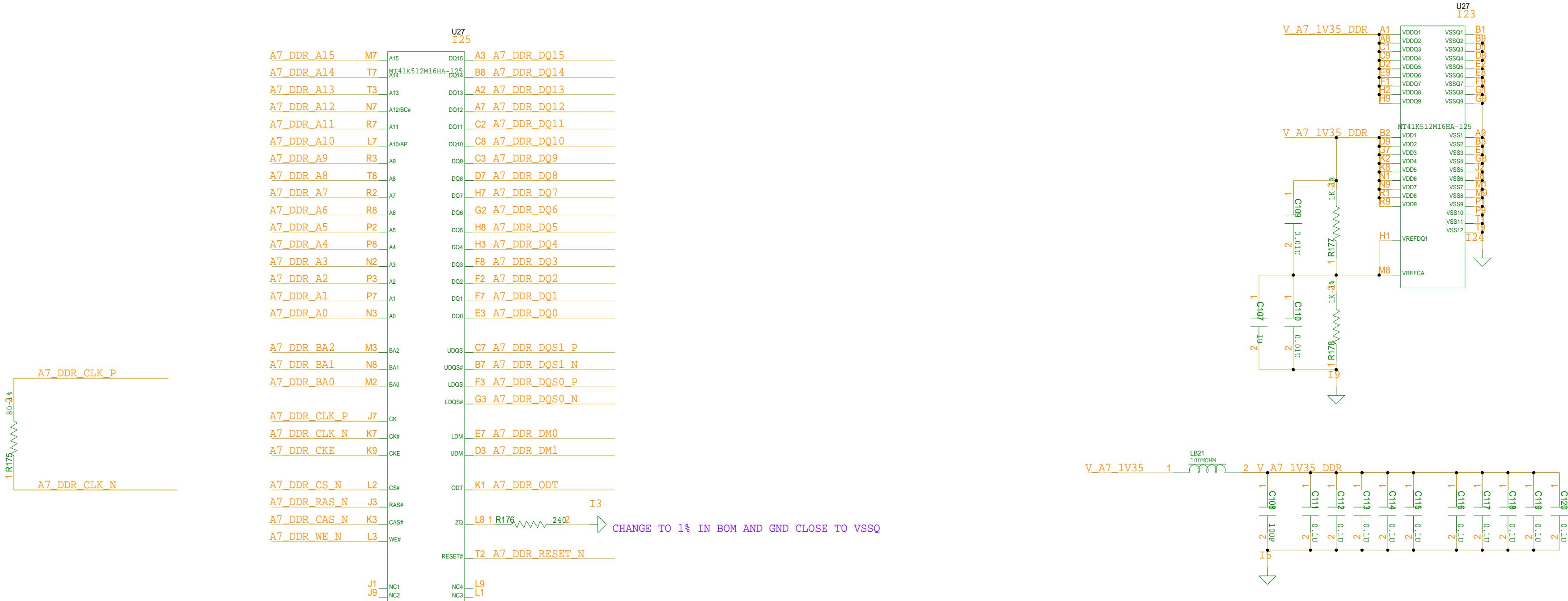
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SIZE	REV.	DRAWING NO.
SCALE		SHEET OF

# ARTIX-7 DDR3

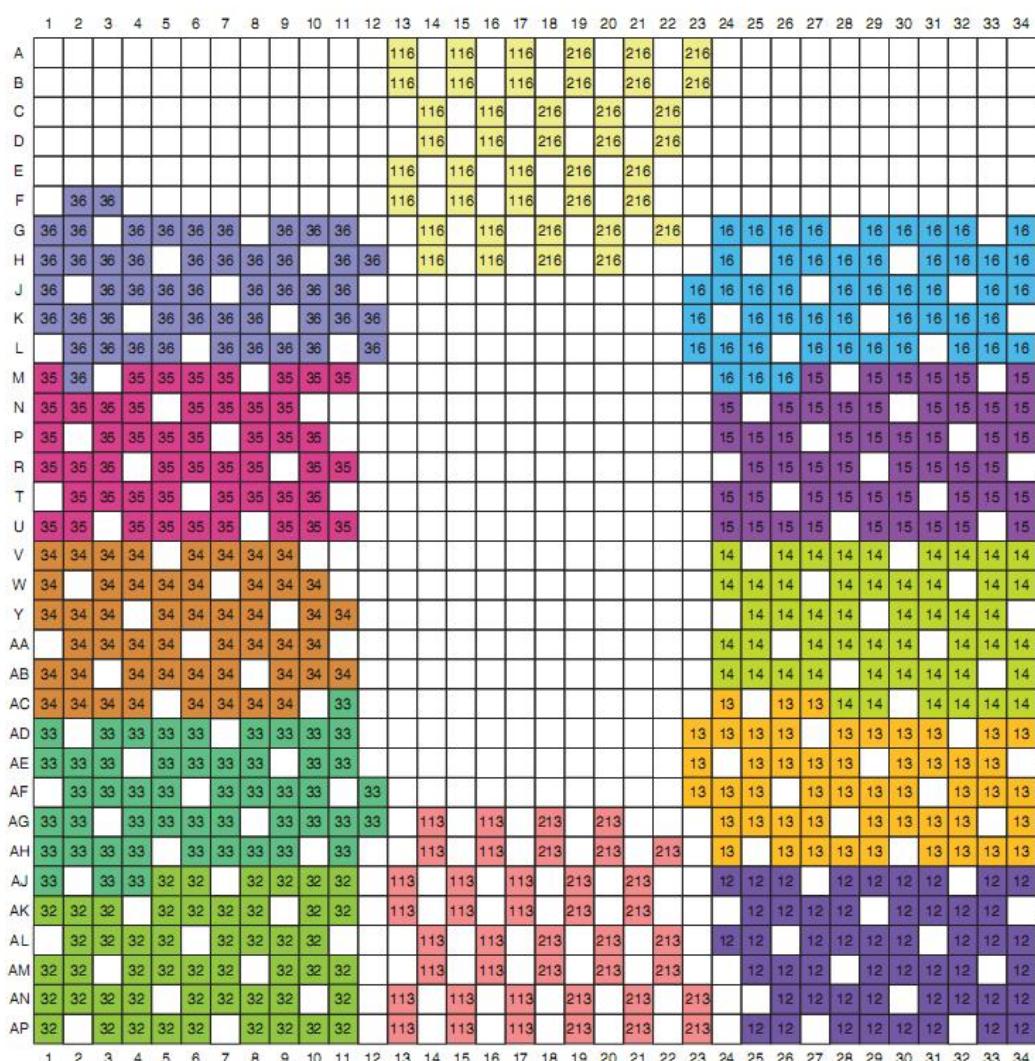
## REVISIONS

ZONE	LTR	DESCRIPTION	DATE	APPR.



ZONE	LTR	DESCRIPTION	DATE	APPR.

# ARTIX-7 PINOUT MAP



BANK0 : 3.3V CONFIG

BANK36 : 3.3V USB INOUT 1/2 SFP+ MUX

BANK35 : 3.3V NC

BANK34 : 1.35V DDR3

BANK33 : 3.3V USB PHY

BANK32 : 3.3V NC

BANK16 : 3.3V NC

BANK15 : 3.3V HDMI RECEIVER

BANK14 : 3.3V SPI FLASH

BANK13 : 3.3V HDMI INOUT 1/2

BANK12 : 3.3V HDMI TRANSMITTER

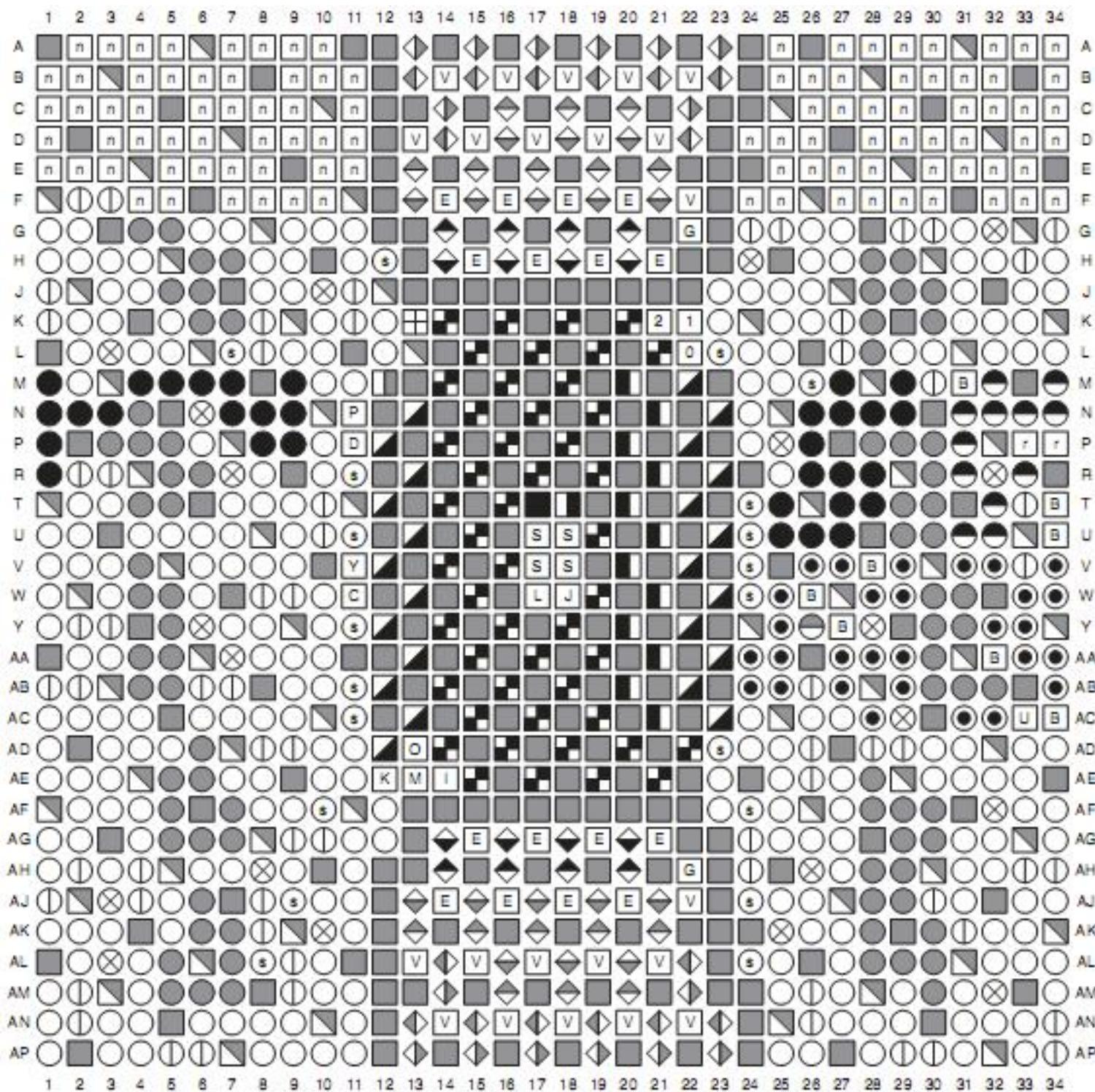
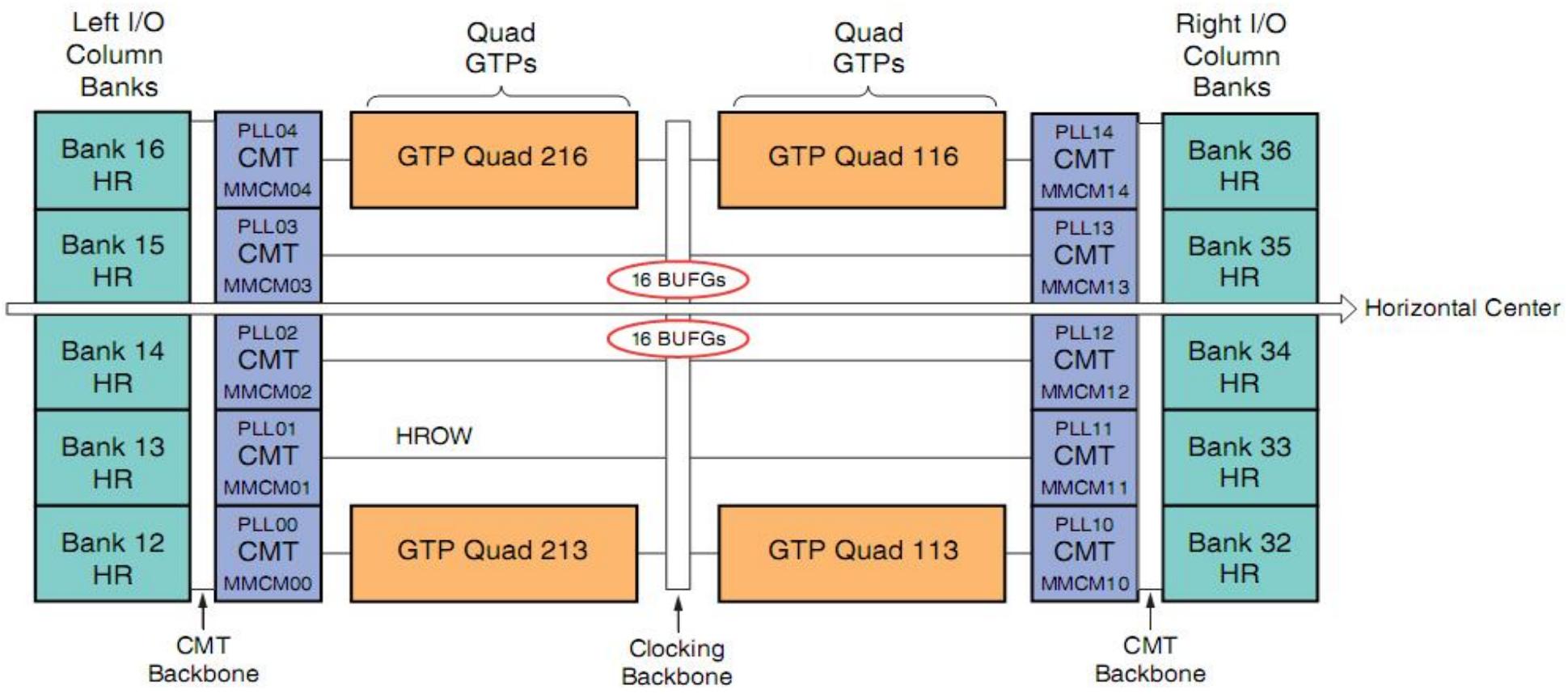
BANK116 : 3.3V PCIE X4

BANK216 : 3.3V SFP+ \*4

BANK113 : 3.3V PCIE X4

BANK213 : 3.3V PCIE X4

All HR I/O banks and the GTP Quads are fully bonded out in this package.



User I/O Pins	Transceiver Pins	Dedicated Pins	Other Pins
○ IO_LXXY_# ● IO_XX_#	E MGTAVCC_G# V MGTAVTT_G# A MGTVCVAUX_G# ◀ MGTAVTTRCAL G MGTREFREF B ADV_B B FCS_B B FOE_B B MOSI B FWE_B B DOUT_CSO_B B CSI_B B PUDC_B U RDWR_B r RSD-RS1 ● ADDP/ADON-AD15P/AD15N ● EMCCLK	C CCLK_0 V CFGBVS_0 A DONE_0 ◀ MGTAVTTRCAL J DXP_0 L DXN_0 ■ GNDADC_0 Y INIT_B_0 O M0_0 1 M1_0 2 M2_0 P PROGRAM_B_0 K TCK_0 I TDI_0 O TDO_0 M TMS_0 ■ VCCADC_0 ■ VCCBATT_0	GND VCCAUX_IO_G# VCCAUX VCCINT VCCO_# VCCBRAM NC
<b>Multi-Function Pins</b>			
	B ADV_B B FCS_B B FOE_B B MOSI B FWE_B B DOUT_CSO_B B CSI_B B PUDC_B U RDWR_B r RSD-RS1 ● ADDP/ADON-AD15P/AD15N ● EMCCLK	E VRN ○ VRP ○ VREF ● D00-D31 ● A00-A28 ○ DQS ○ MRCC ● SRCC	

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SCALE		SHEET OF

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DESCRIPTION	DATE	APPR.



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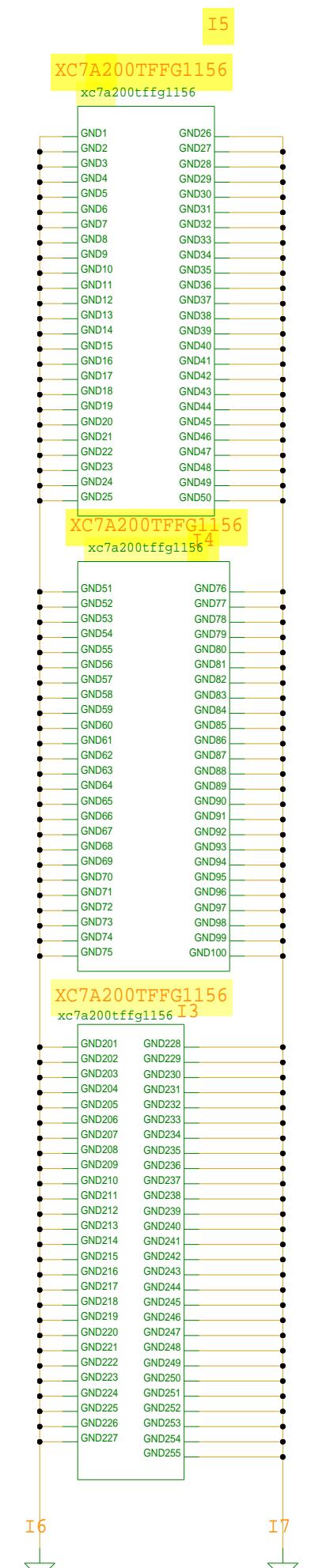
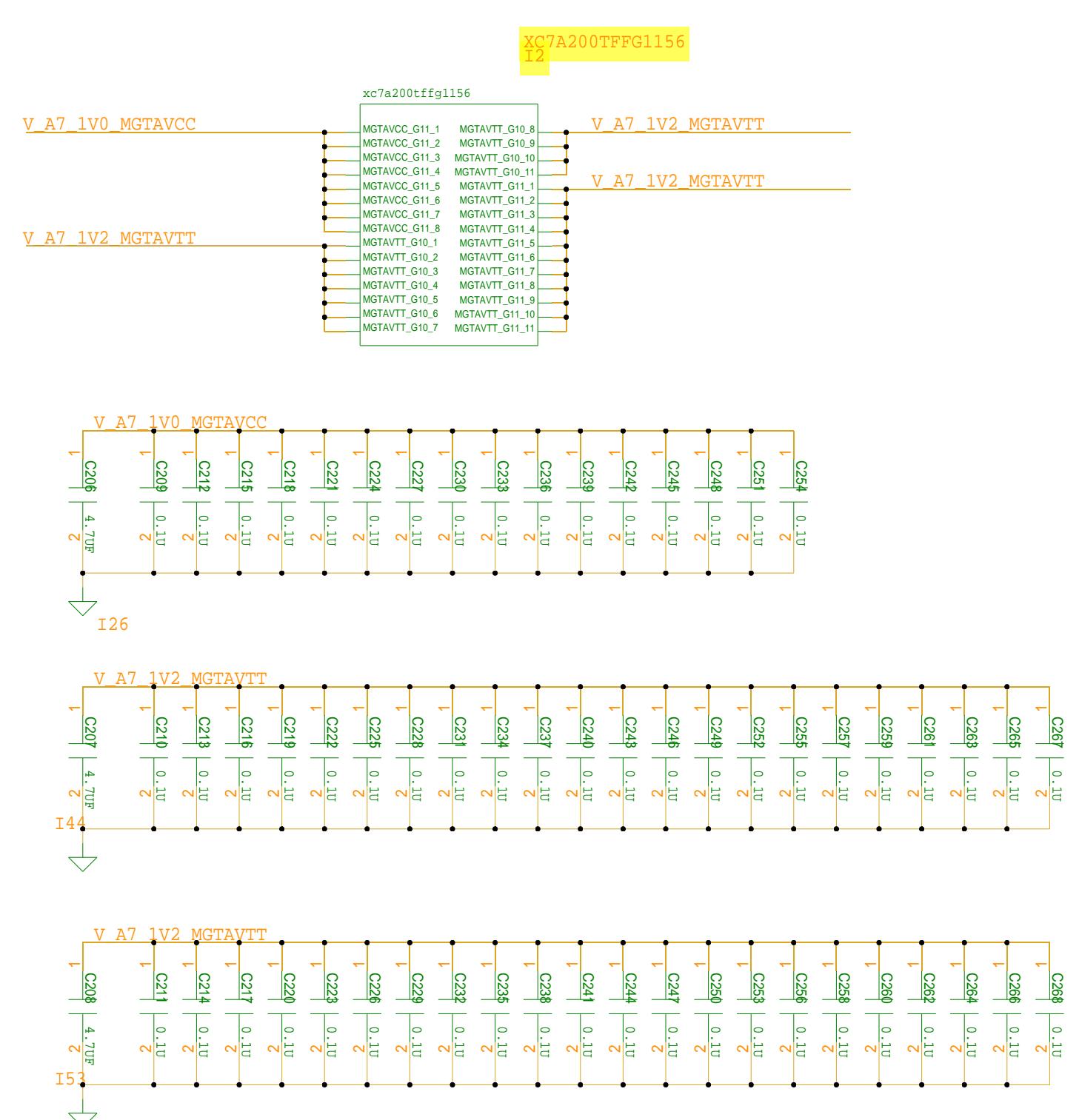
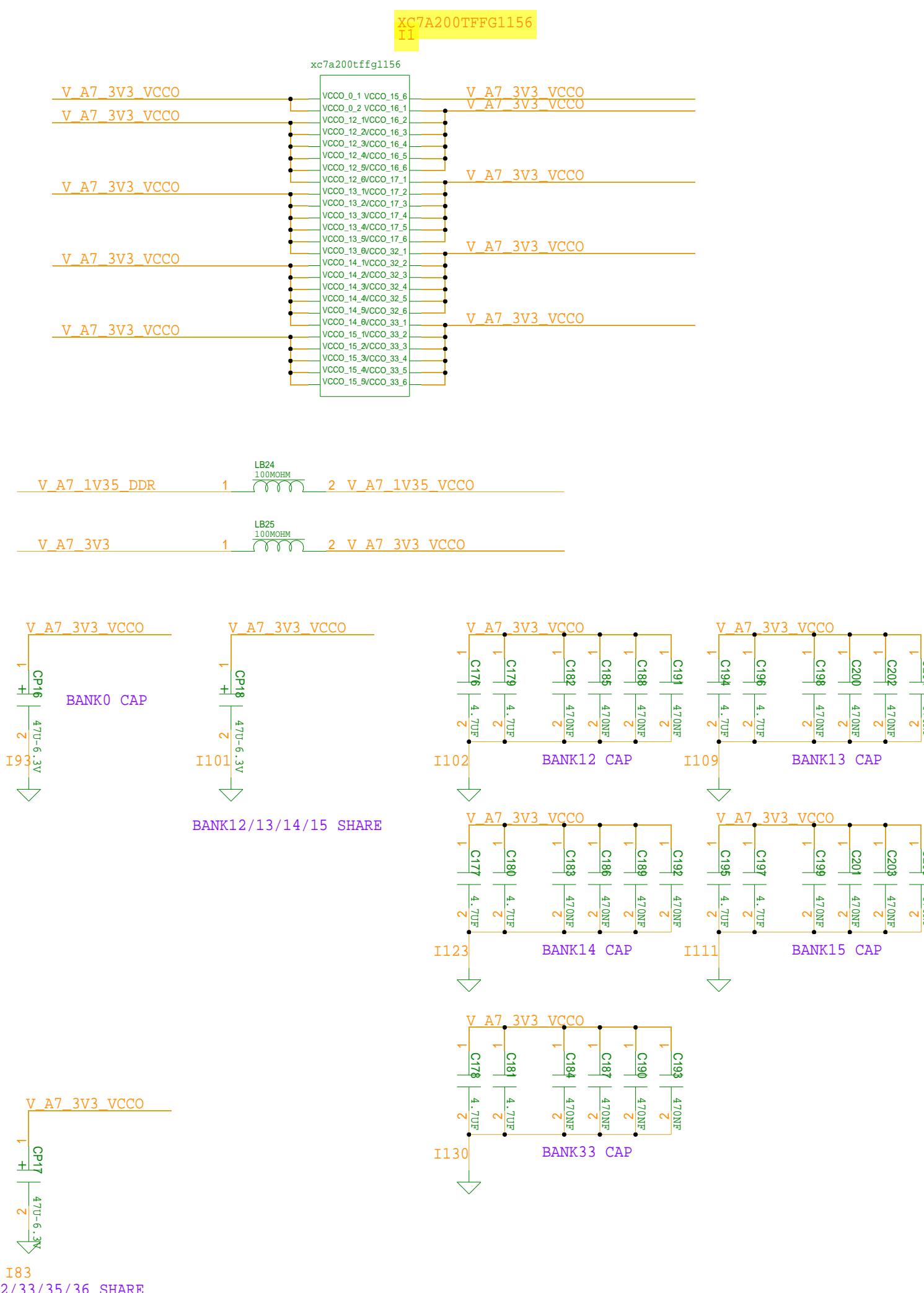
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DRAWING NO.

SHEET OF

# ARTIX-7 BANK POWER (2)

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ZONE	LTR	DESCRIPTION		DATE	APPR.		



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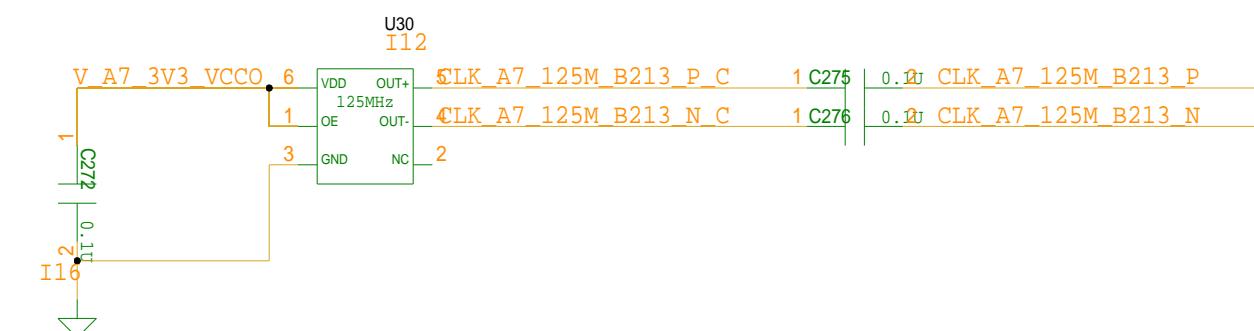
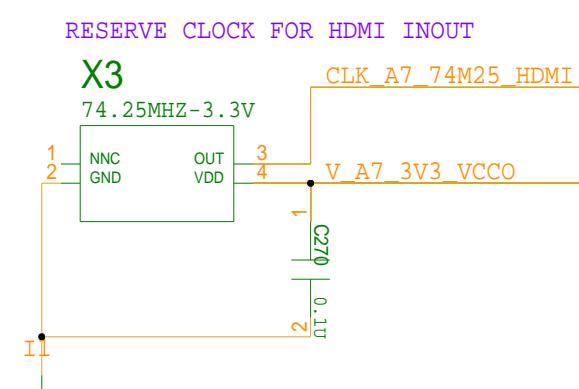
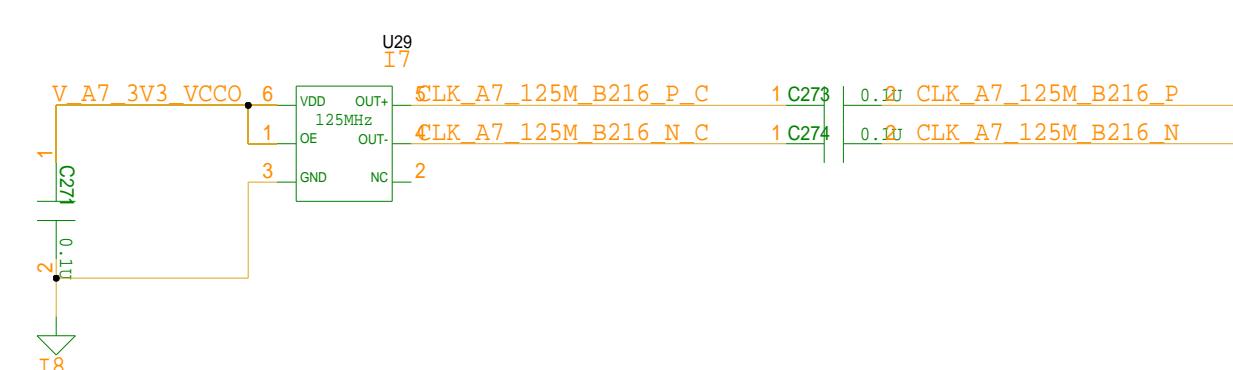
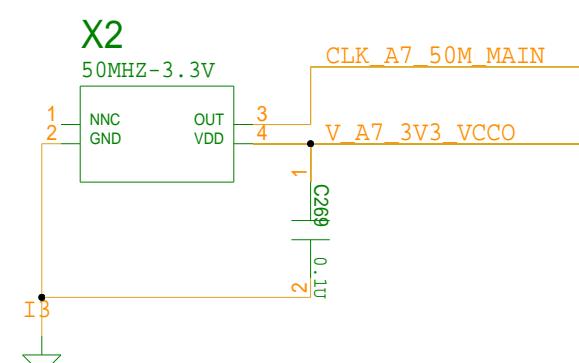
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		SCALE	OF				
8	7	6	5	4	3	2	1

# ARTIX-7 CLOCK

## REVOLUTIONS

ZONE	LTR	DESCRIPTION	DATE	APPR.



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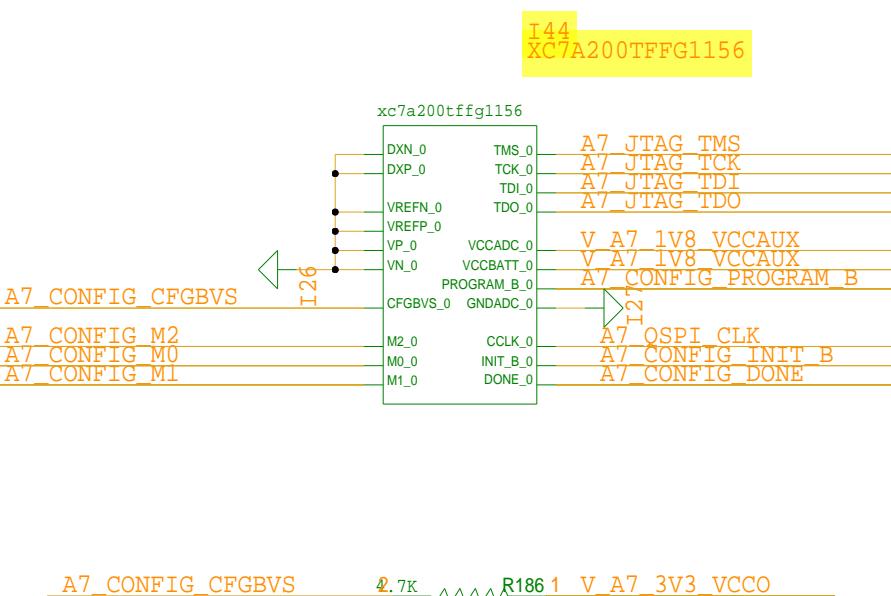
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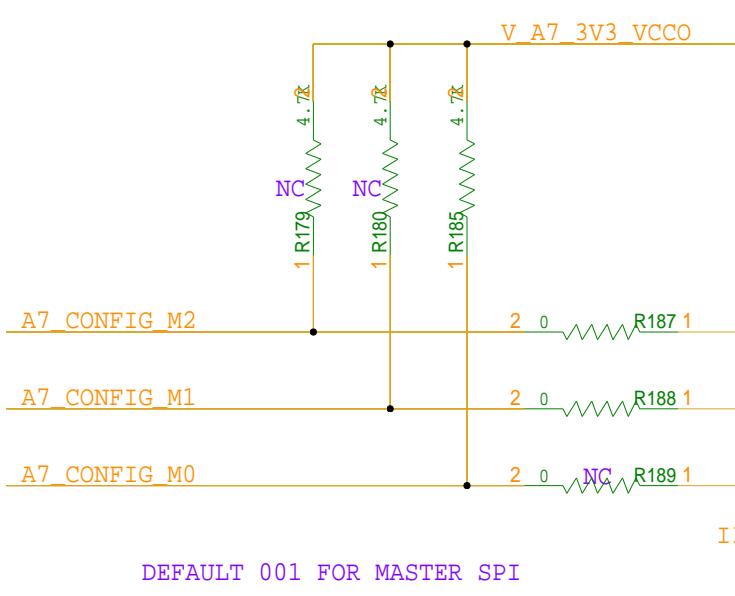
	DESCRIPTION	DATE	APPR.
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ARTIX-7 BANK0 / 14 CONFIG

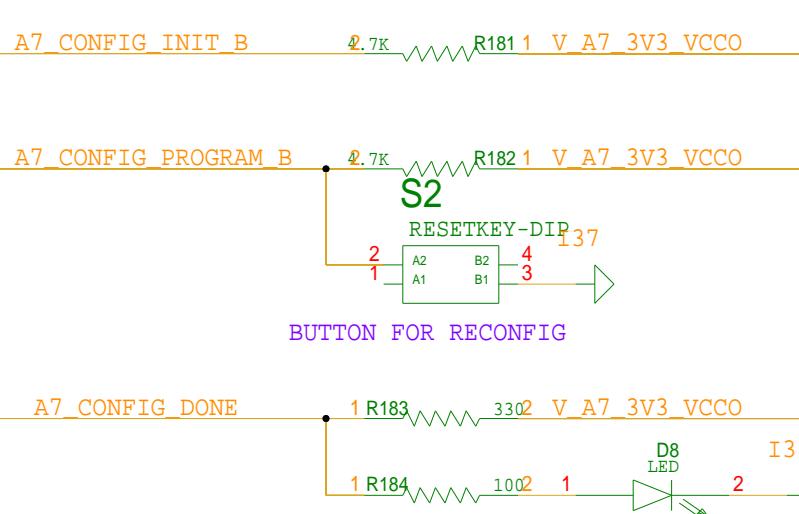


BANK0/14/15 SHOULD BE 3.3V/2.5V

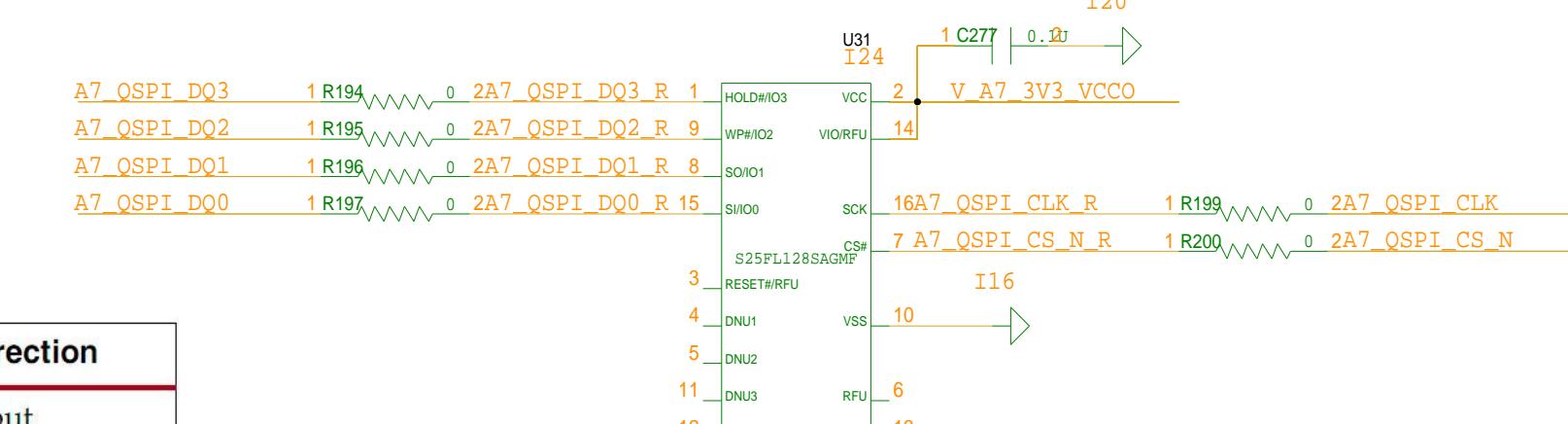
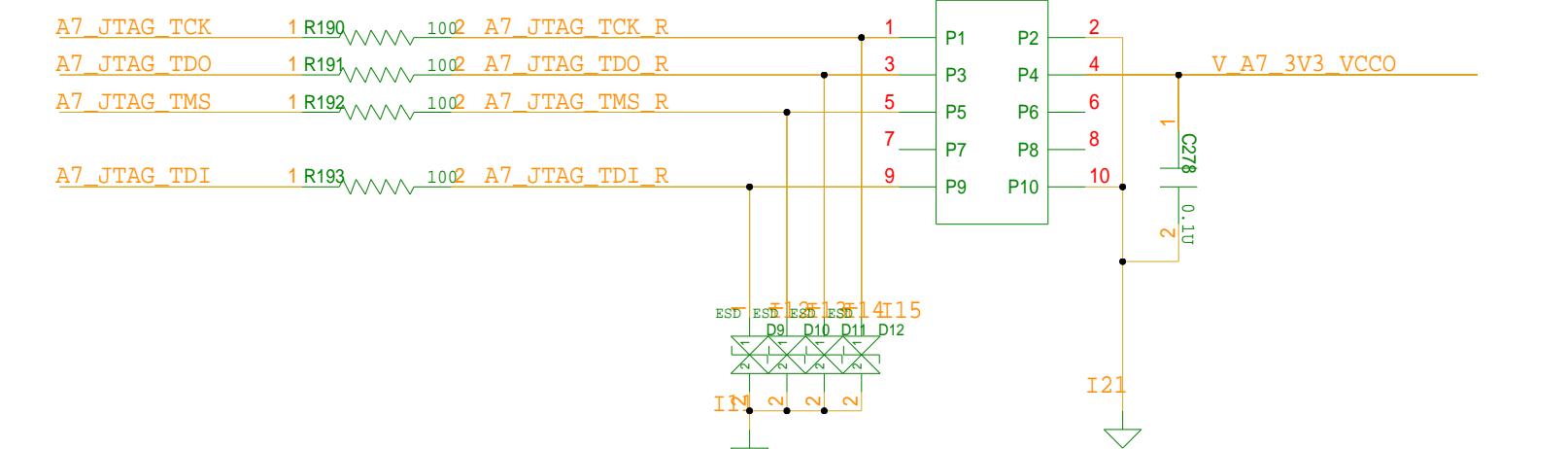
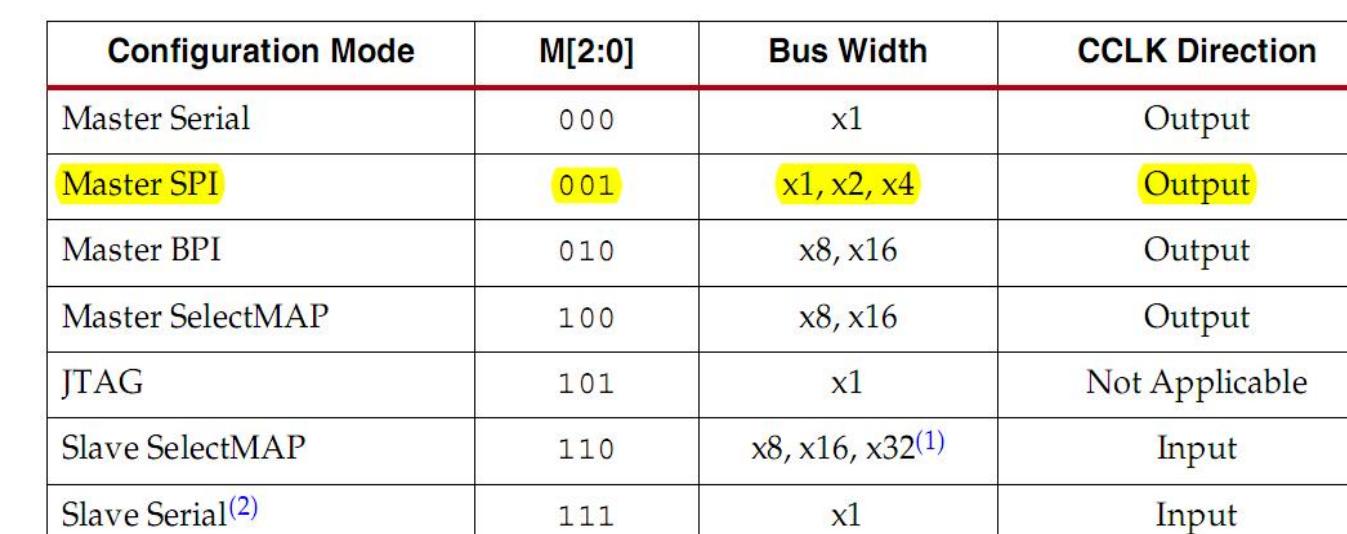
CFGBVS Pin Connection	Supported Configuration Banks 0/14/15 V <sub>CCO</sub> Supply and I/O Signal Voltages		
	Spartan-7, Artix-7, Kintex-7	Virtex-7 T, XT	Virtex-7 HT
Banks Affected	0, 14, 15	0	none
V <sub>CCO</sub> _0 (3.3V or 2.5V)	3.3V or 2.5V	3.3V or 2.5V	1.8V (no CFGBVS)
GND	1.8V or 1.5V	1.8V or 1.5V	



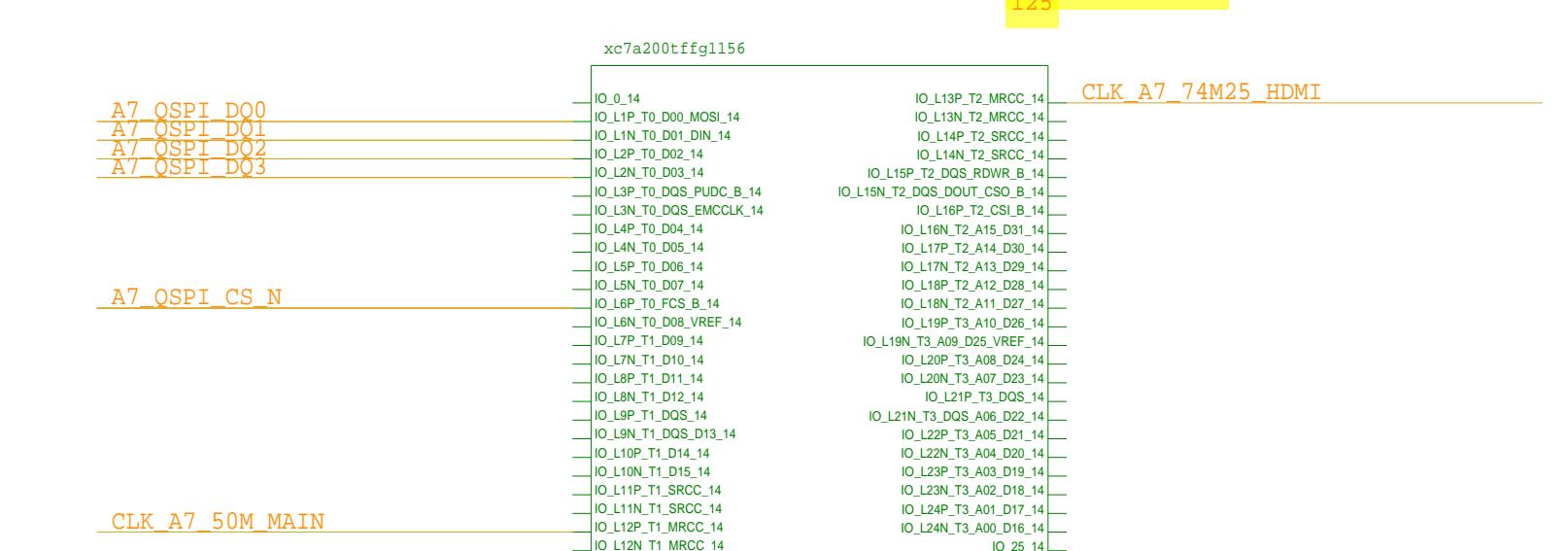
DEFAULT 001 FOR MASTER SPI  
101 FOR JTAG(ONLY)  
111 FOR SLAVE SERIAL



LED INDICATE CONFIG DONGLE



A7 OSPI CS N R7K B1981 V A7 3V3 VCCO



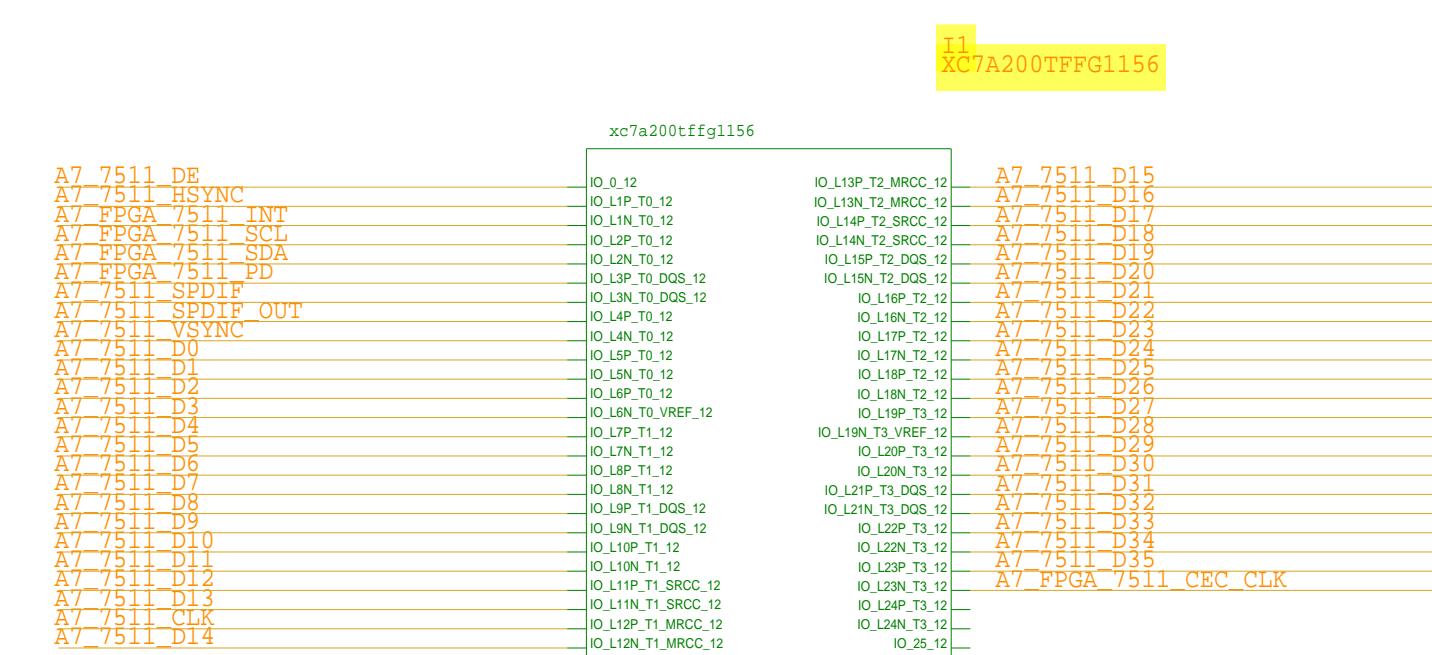
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	SCALE		SHEET	OF

# ARTIX-7 BANK12

REVISED		DESCRIPTION		DATE	APPR.



OD CONFIG AS BELOW:

A7\_FPGA\_7511\_SCL

A7\_FPGA\_7511\_SDA

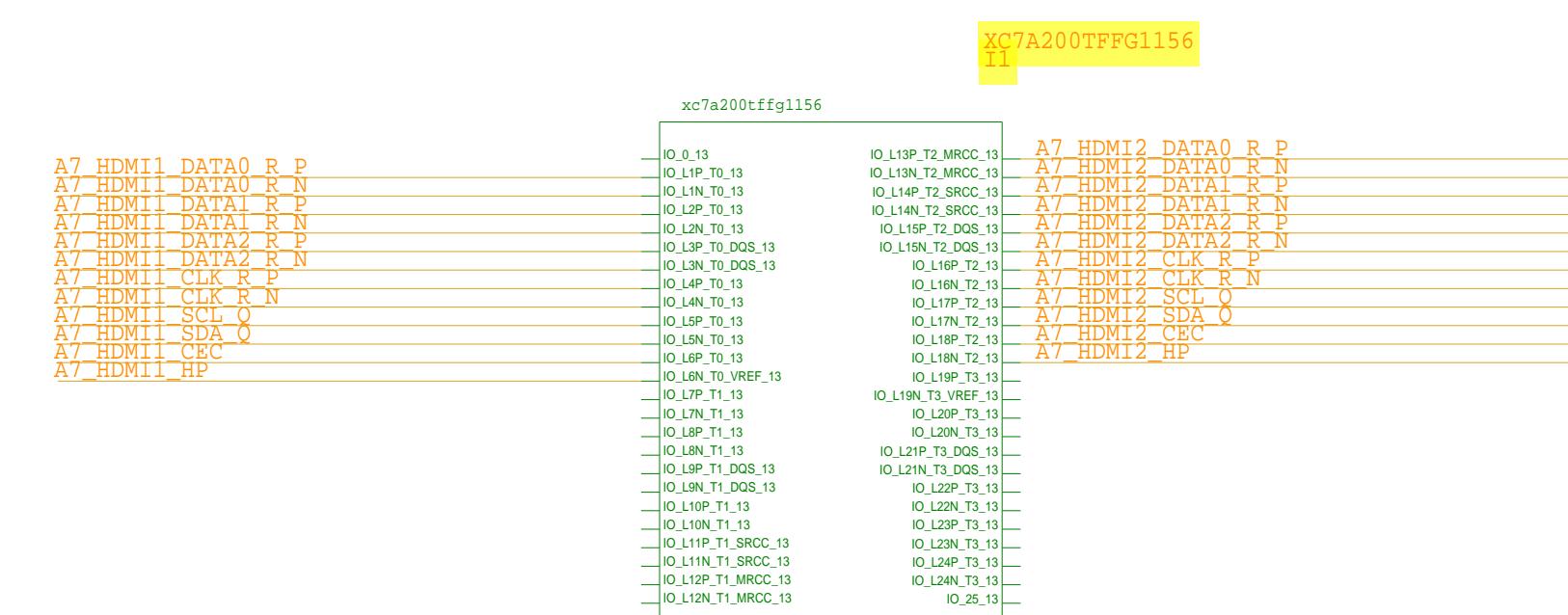
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SCALE	REV.	SIZE		DRAWING NO.	

# ARTIX-7 BANK13

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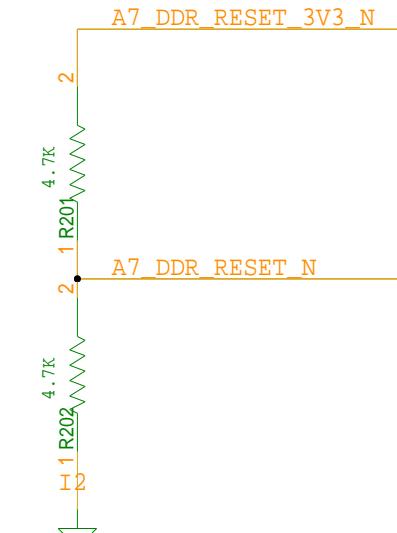
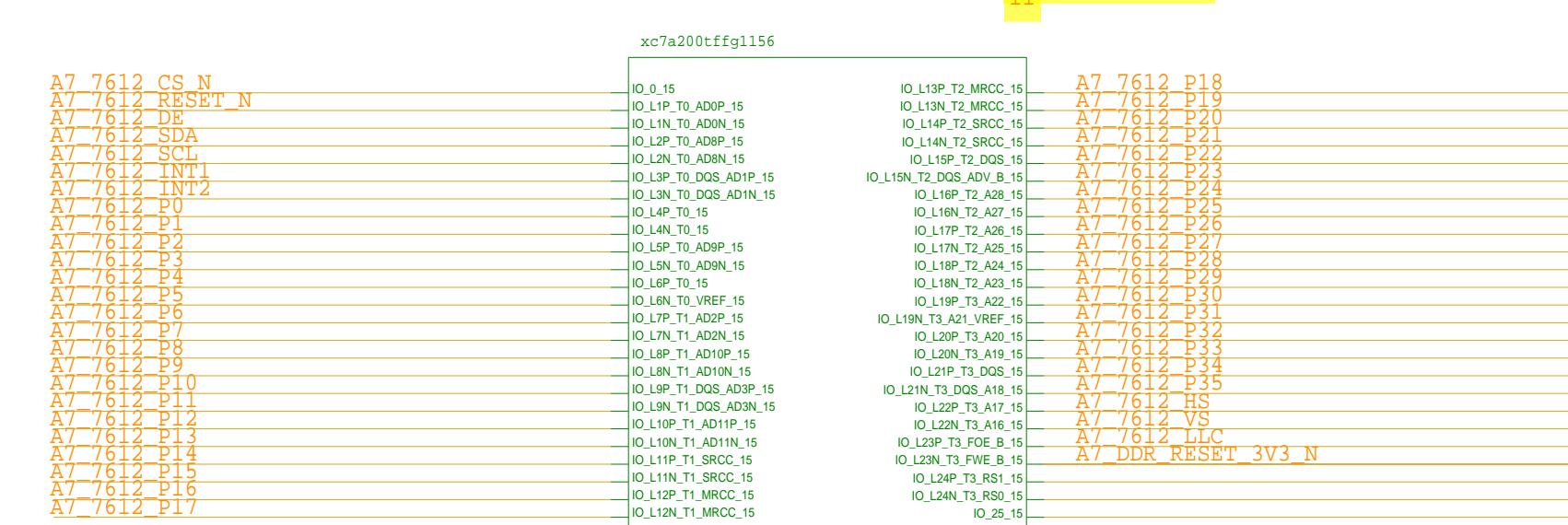
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SCALE SHEET OF

# ARTIX-7 BANK15

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# ARTIX-7 BANK32

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IO_0_32	IO_L13P_T2_MRCC_32
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IO_L2N_T0_32	IO_L15P_T2_DOS_32
IO_L3P_T0_DQS_32	IO_L15N_T2_DQS_32
IO_L3N_T0_DQS_32	IO_L16P_T2_32
IO_L4P_T0_32	IO_L16N_T2_32
IO_L4N_T0_32	IO_L17P_T2_32
IO_L5P_T0_32	IO_L17N_T2_32
IO_L5N_T0_32	IO_L18P_T2_32
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IO_L9P_T1_DQS_32	IO_L21N_T3_DQS_32
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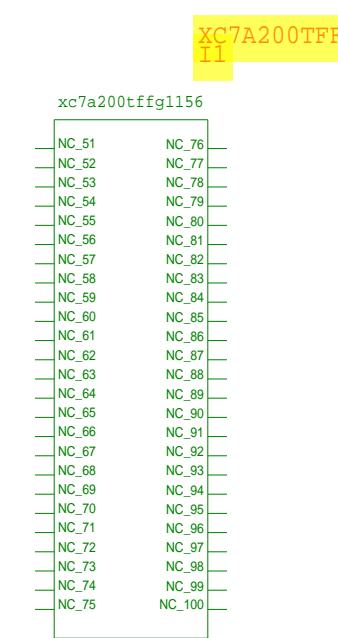
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# ARTIX-7 BANK16

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ZONE	LTR	DESCRIPTION	DATE	APPR.

xc7a200tffg1156  
11

xc7a200tffg1156

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IO_L1P_T0_16	IO_L1N_T2_MRCC_16
IO_L1N_T0_16	IO_L1P_T2_SRCC_16
IO_L2P_T0_16	IO_L1N_T2_SRCC_16
IO_L2P_T0_16	IO_L15P_T2_DQS_16
IO_L2N_T0_16	IO_L15N_T2_DQS_16
IO_L3P_T0_DQS_16	IO_L16P_T2_16
IO_L3N_T0_DQS_16	IO_L16P_T2_16
IO_L4P_T0_16	IO_L17P_T2_16
IO_L4N_T0_16	IO_L17P_T2_16
IO_L5P_T0_16	IO_L17N_T2_16
IO_L5N_T0_16	IO_L18P_T2_16
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IO_L8P_T1_16	IO_L20N_T3_16
IO_L8N_T1_16	IO_L21P_T3_DQS_16
IO_L9P_T1_DQS_16	IO_L21N_T3_DQS_16
IO_L9N_T1_DQS_16	IO_L22P_T3_16
IO_L10P_T1_16	IO_L22N_T3_16
IO_L11P_T1_16	IO_L23P_T3_16
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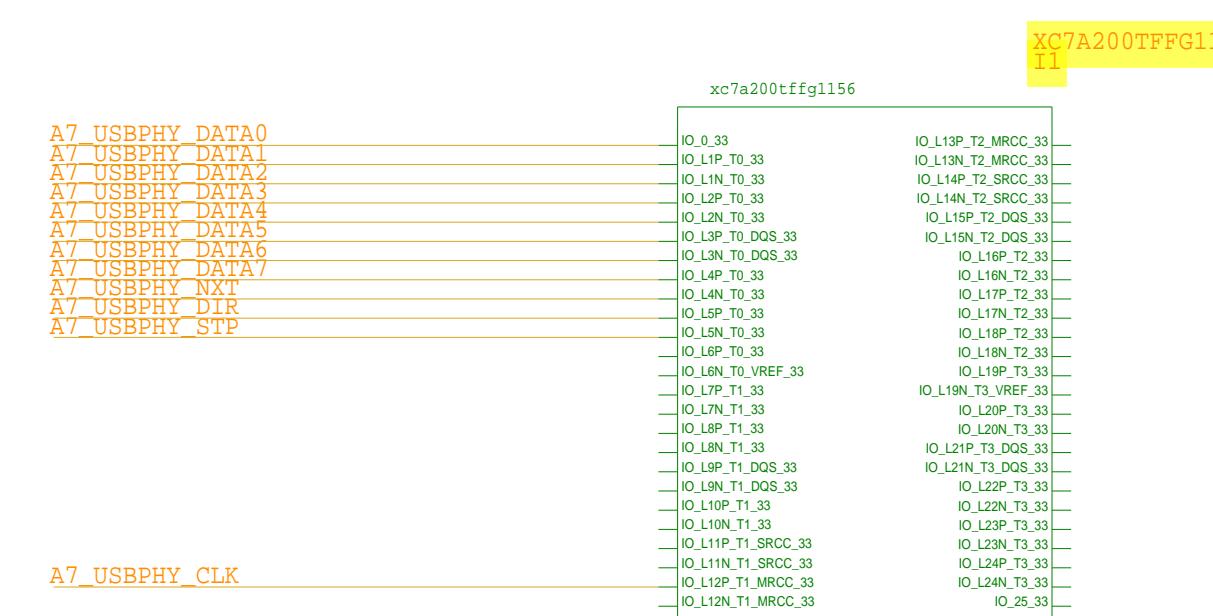
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# ARTIX-7 BANK33

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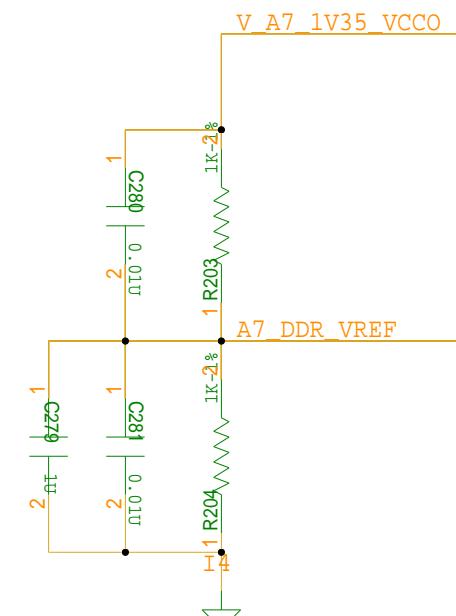
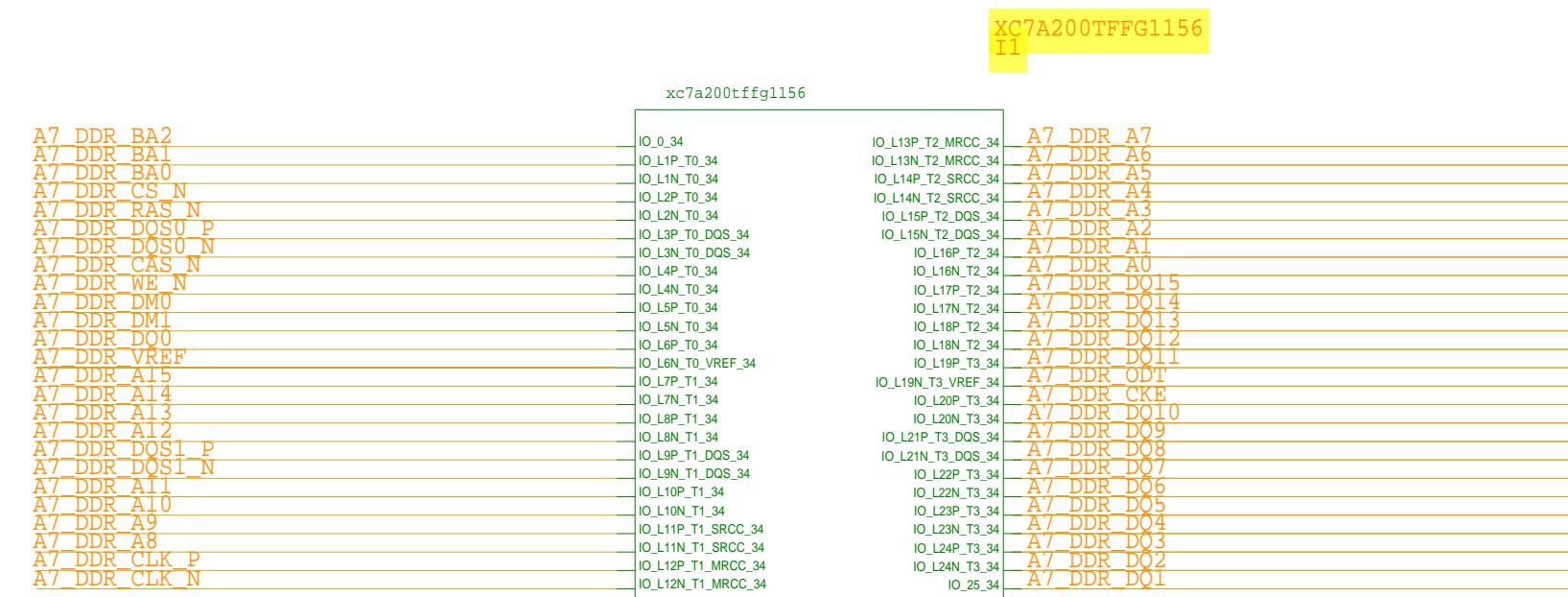


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ARTIX-7 BANK35

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPR.

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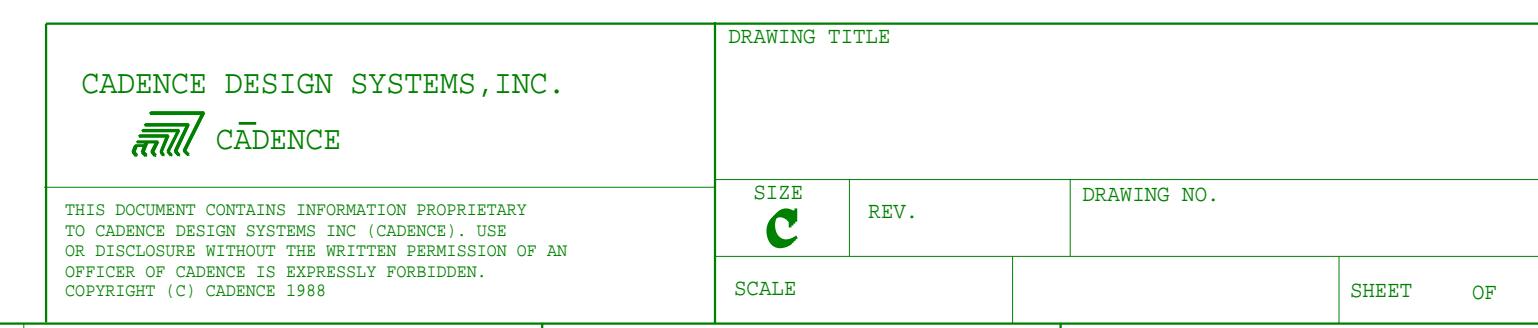
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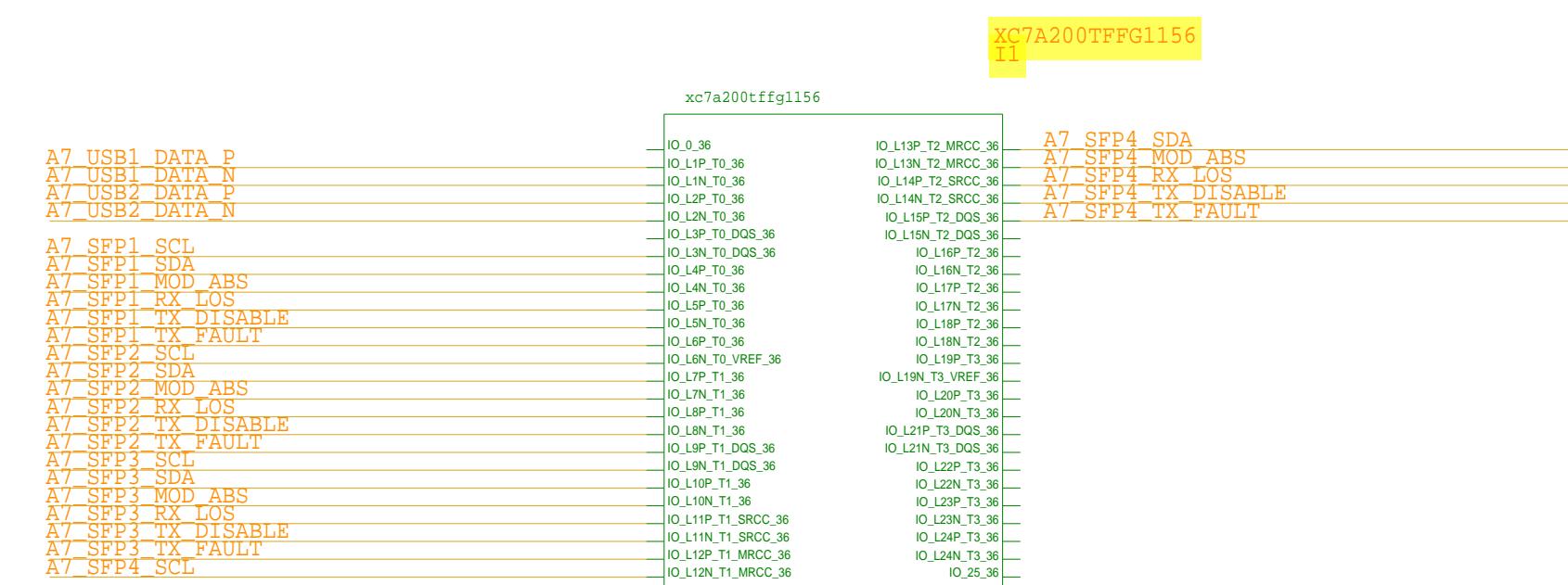
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IO_L1N_T0_AD4N_35	IO_L14P_T2_SRCC_35
IO_L2P_T0_AD12P_35	IO_L14N_T2_SRCC_35
IO_L2N_T0_AD12N_35	IO_L15P_T2_DOS_35
IO_L3P_T0_DQS_AD5P_35	IO_L15N_T2_DOS_35
IO_L3N_T0_DQS_AD5N_35	IO_L16P_T2_35
IO_L4P_T0_35	IO_L16N_T2_35
IO_L4N_T0_35	IO_L17P_T2_35
IO_L5P_T0_AD13P_35	IO_L17N_T2_35
IO_L5N_T0_AD13N_35	IO_L18P_T2_35
IO_L6P_T0_35	IO_L18N_T2_35
IO_L6N_T0_VREF_35	IO_L19P_T3_35
IO_L7P_T1_AD6P_35	IO_L19N_T3_VREF_35
IO_L7N_T1_AD6N_35	IO_L20P_T3_35
IO_L8P_T1_AD14P_35	IO_L20N_T3_35
IO_L8N_T1_AD14N_35	IO_L21P_T3_DQS_35
IO_L9P_T1_DQS_AD7P_35	IO_L21N_T3_DQS_35
IO_L9N_T1_DQS_AD7N_35	IO_L22P_T3_35
IO_L10P_T1_AD15P_35	IO_L22N_T3_35
IO_L10N_T1_AD15N_35	IO_L23P_T3_35
IO_L11P_T1_SRCC_35	IO_L23N_T3_35
IO_L11N_T1_SRCC_35	IO_L24P_T3_35
IO_L12P_T1_MRCC_35	IO_L24N_T3_35
IO_L12N_T1_MRCC_35	IO_25_35



# ARTIX-7 BANK36

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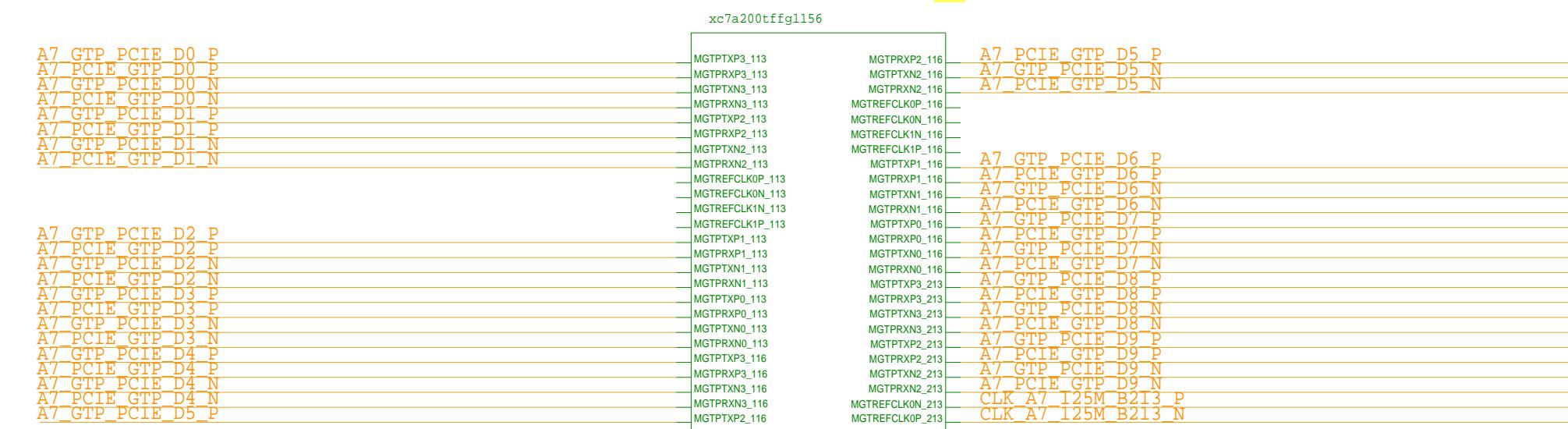


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## ARTIX-7 GTP (2)

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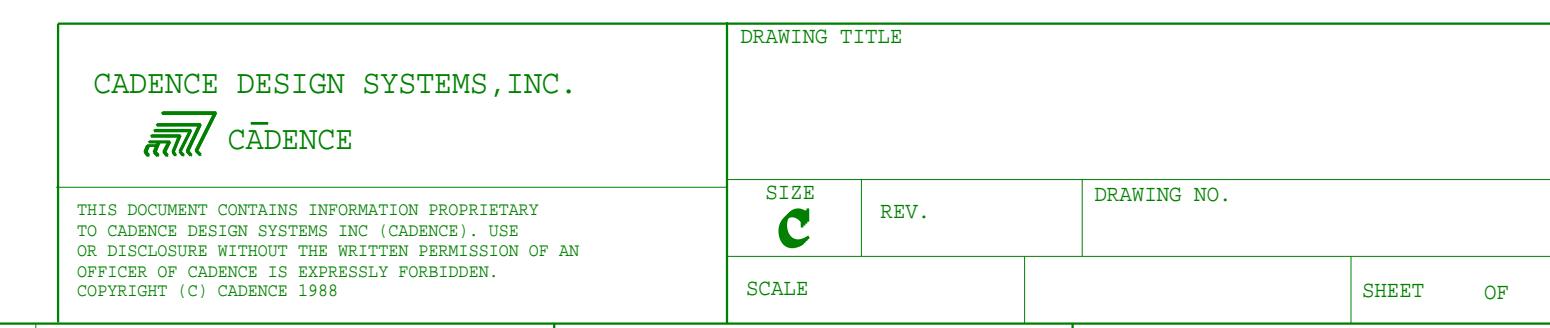
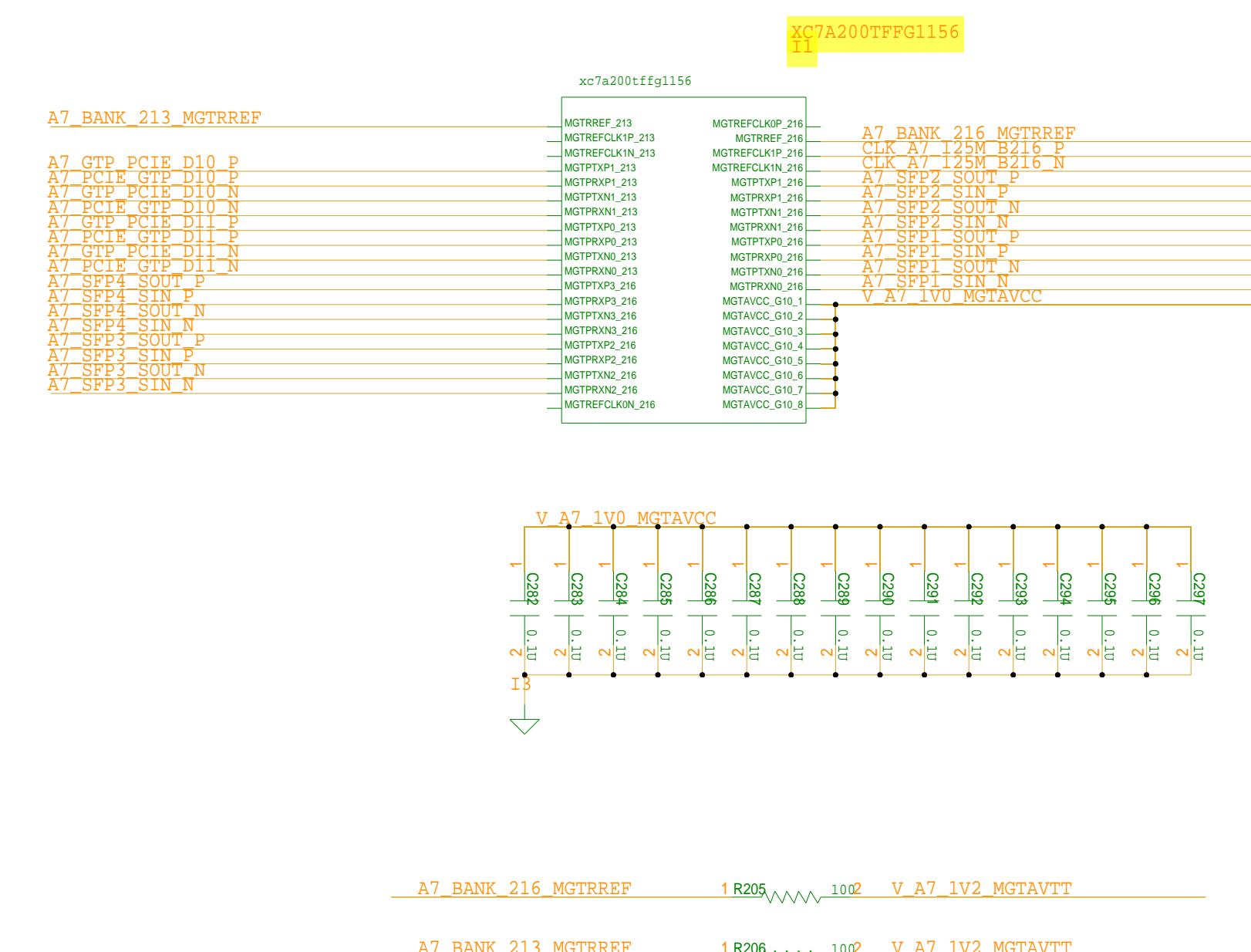
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# ZYNQ-7 INDEX

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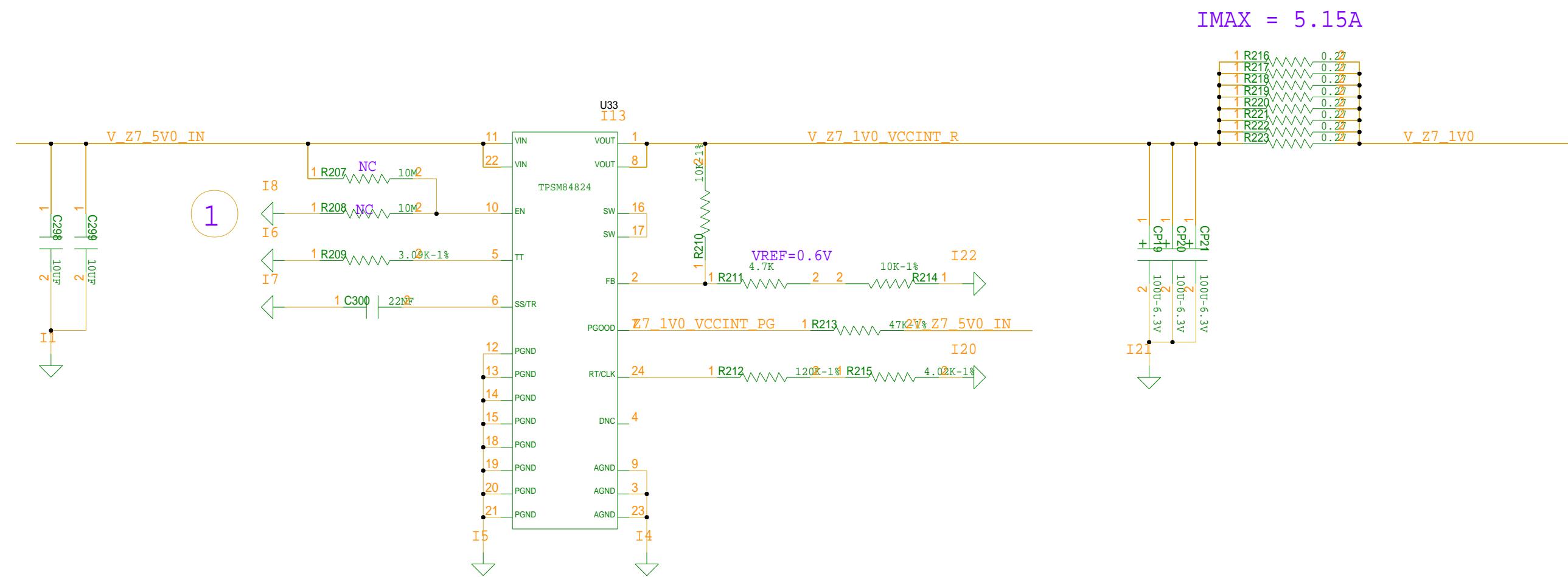
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## REVISIONS

ZONE	LTR	DESCRIPTION	DATE	APPR.

## ZYNQ-7 POWER (1)



SS/TR	6	I	Soft-start and tracking pin. Connecting an external capacitor to this pin adjusts the output voltage soft-start ramp slower than its 1.2 ms default setting. A voltage applied to this pin allows for tracking and sequencing control.
-------	---	---	--

Table 9. Soft-Start Capacitor Values and Soft-Start Time

C <sub>ss</sub> (nF)	open	10	15	22	47
SS Time (ms)	1.2	2.4	3	3.8	6.8

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# ZYNQ-7 POWER (2)

$$V_{OUT} = V_{REF} \times (1 + (R_{TOP}/R_{BOT}))$$

$$R_{RT} (\text{k}\Omega) = [14,822/f_{SW} (\text{kHz})]^{1.081}$$

$$V_{IN\_STARTUP} = (0.8 \text{ nA} + (0.8 \text{ V}/R_{BOT\_EN})) \times \left( R_{TOP\_EN} + \frac{R_{BOT\_EN} \times 1 \text{ M}\Omega}{R_{BOT\_EN} + 1 \text{ M}\Omega} \right)$$

where:

$R_{TOP\_EN}$  is the resistor from  $V_{IN}$  to EN.

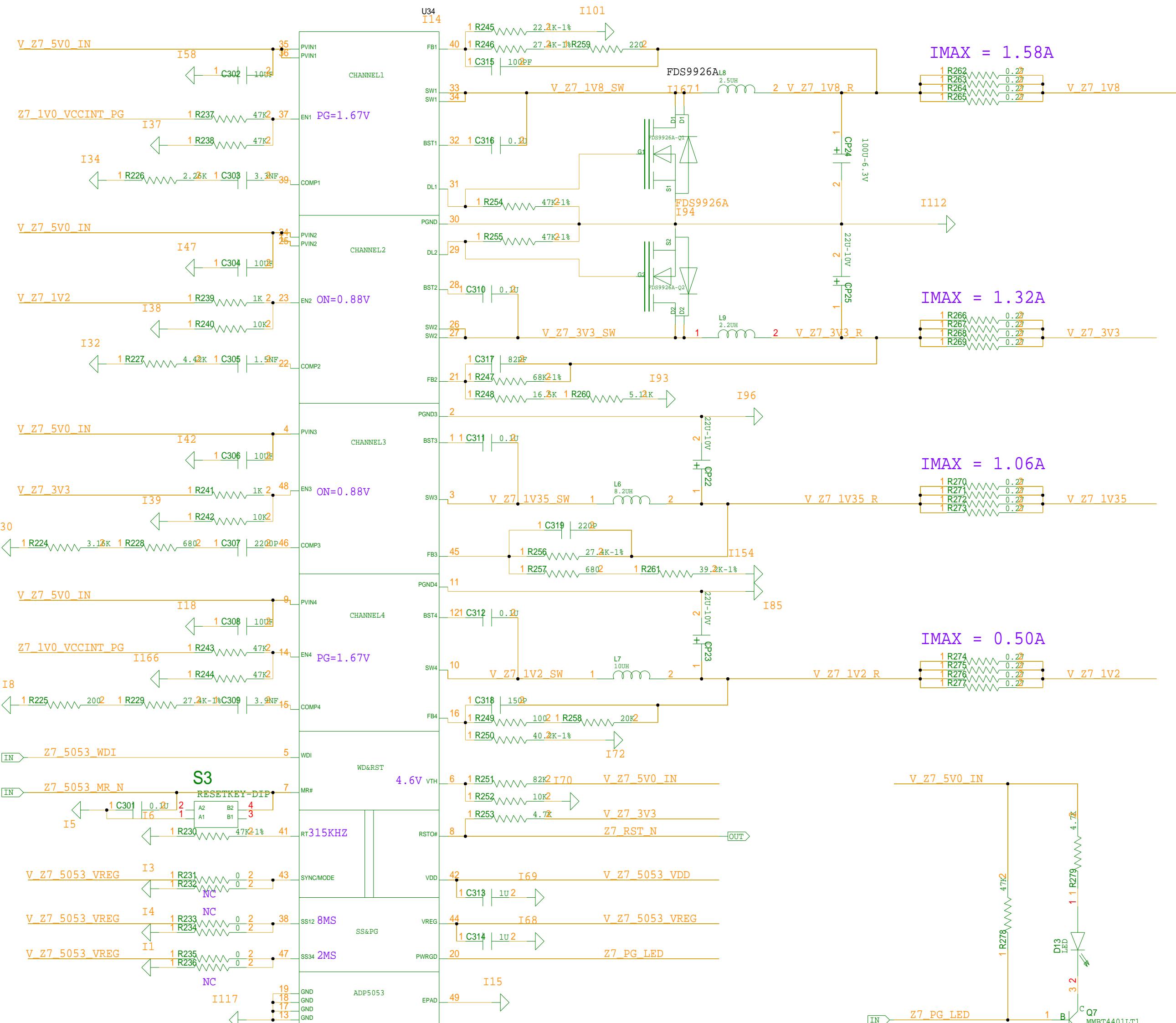
$R_{BOT\_EN}$  is the resistor from EN to ground.

Table 9. Soft Start Time Set by the SS12 and SS34 Pins

$R_{TOP}$ ( $\text{k}\Omega$ )	$R_{BOT}$ ( $\text{k}\Omega$ )	Soft Start Time			
		Channel 1	Channel 2	Channel 3	Channel 4
0	N/A <sup>1</sup>	2 ms	2 ms	2 ms	2 ms
100	600	2 ms	Parallel	2 ms	4 ms
200	500	2 ms	8 ms	2 ms	8 ms
300	400	4 ms	2 ms	4 ms	2 ms
400	300	4 ms	4 ms	4 ms	4 ms
500	200	8 ms	2 ms	4 ms	8 ms
600	100	8 ms	Parallel	8 ms	2 ms
N/A <sup>1</sup>	0	8 ms	8 ms	8 ms	8 ms

Table 16. Factory Default Options

Option	Default Value
Channel 1 Output Voltage	0.8V adjustable output
Channel 2 Output Voltage	0.8V adjustable output
Channel 3 Output Voltage	0.8V adjustable output
Channel 4 Output Voltage	0.8V adjustable output
PWRGD Pin (Pin 20) Output	Monitor Channel 1 output
Output Discharge Function	Enabled for all four buck regulators
Switching Frequency on Channel 1	1x switching frequency set by the RT pin
Switching Frequency on Channel 3	1x switching frequency set by the RT pin
SYNC/MODE Pin (Pin 43) Function	Forced PWM/automatic PWM/PSM mode setting with the ability to synchronize to an external clock
Hiccup Protection	Enabled for overcurrent events
Short-Circuit Latch-Off Function	Disabled for output short-circuit events
Oversupply Latch-Off Function	Disabled for output oversupply events
Reset Timeout Period	200 ms
Watchdog Timeout Period	1.6 sec
Manual Reset Input Mode	Processor manual reset mode



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# ZYNQ-7 POWER (3)

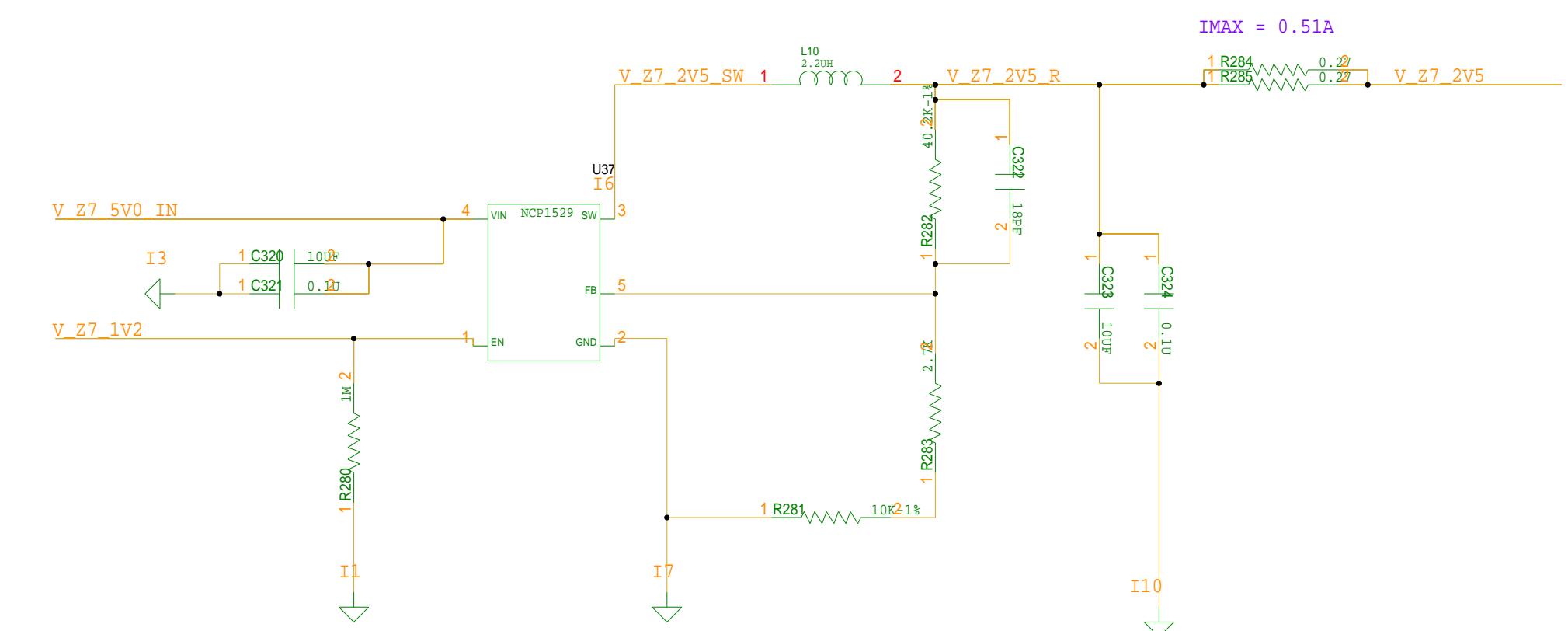
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$$V_{out} = V_{FB} \times (1 + R1/R2)$$

- $V_{OUT}$ : Output Voltage (V)
- $V_{FB}$ : Feedback Voltage = 0.6 V
- $R1$ : Feedback Resistor from  $V_{OUT}$  to FB
- $R2$ : Feedback Resistor from FB to GND

3



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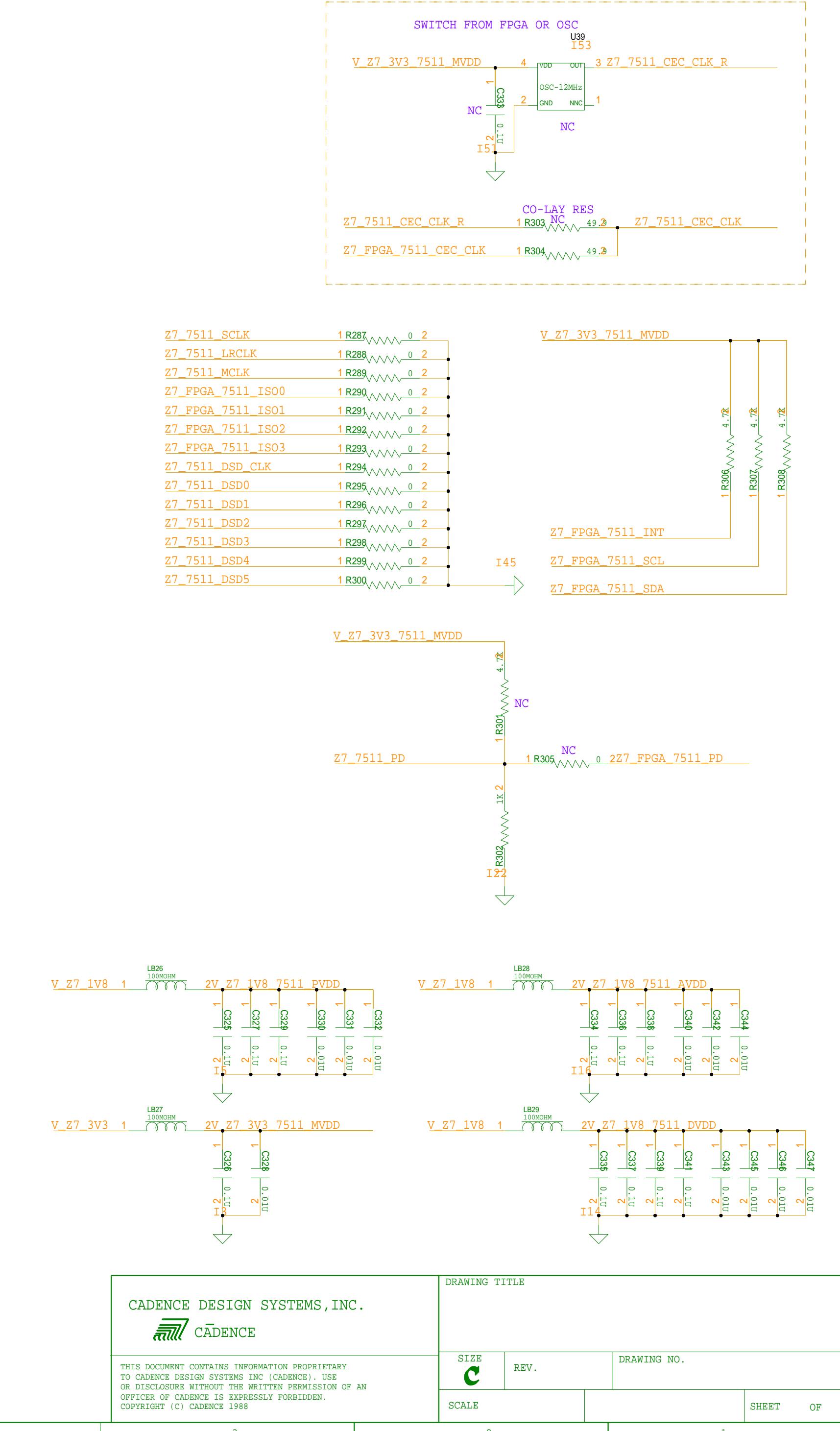
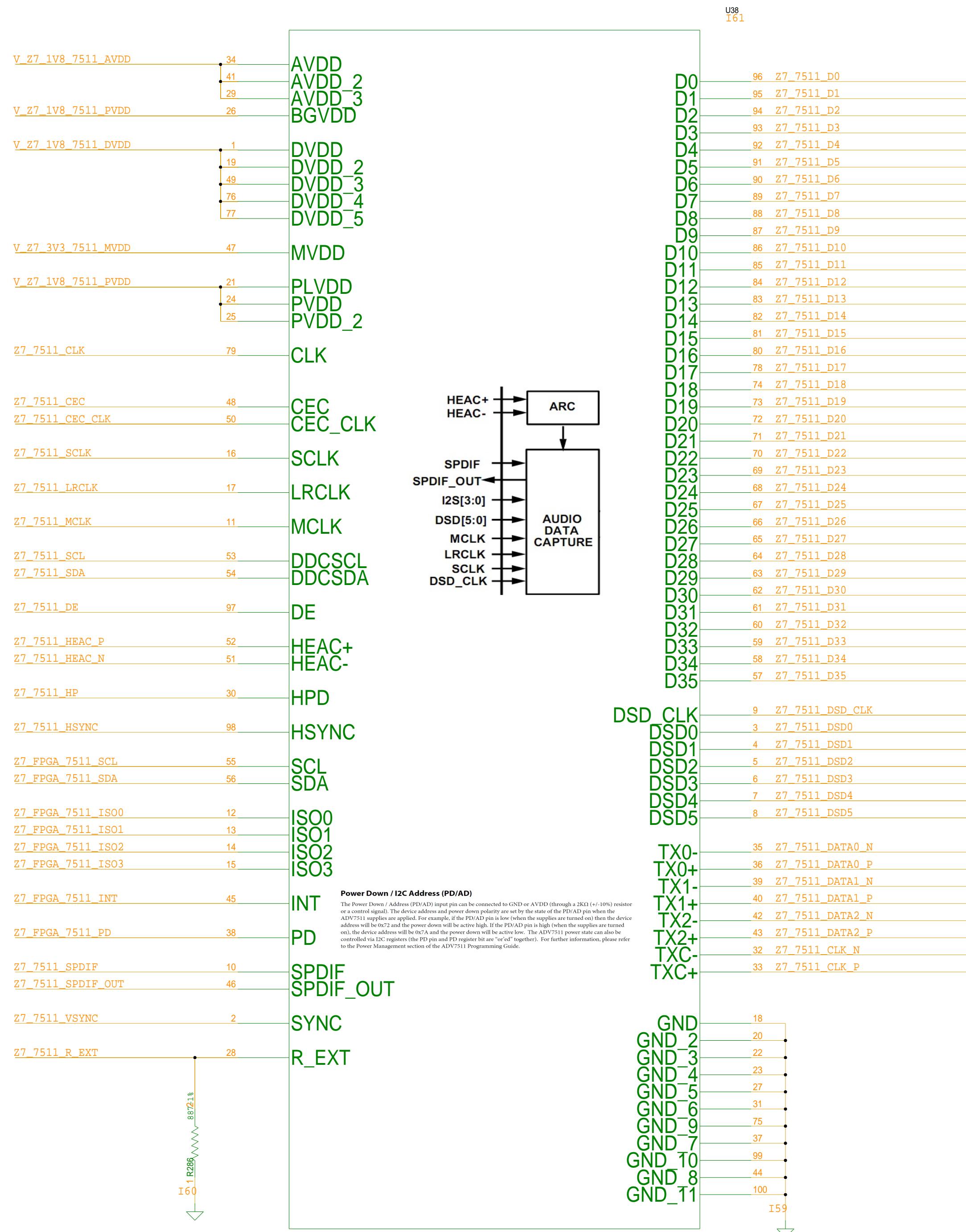


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# ZYNQ-7 PL HDMI TRANSMITTER (1)



# ZYNQ-7 PL HDMI TRANSMITTER (2)

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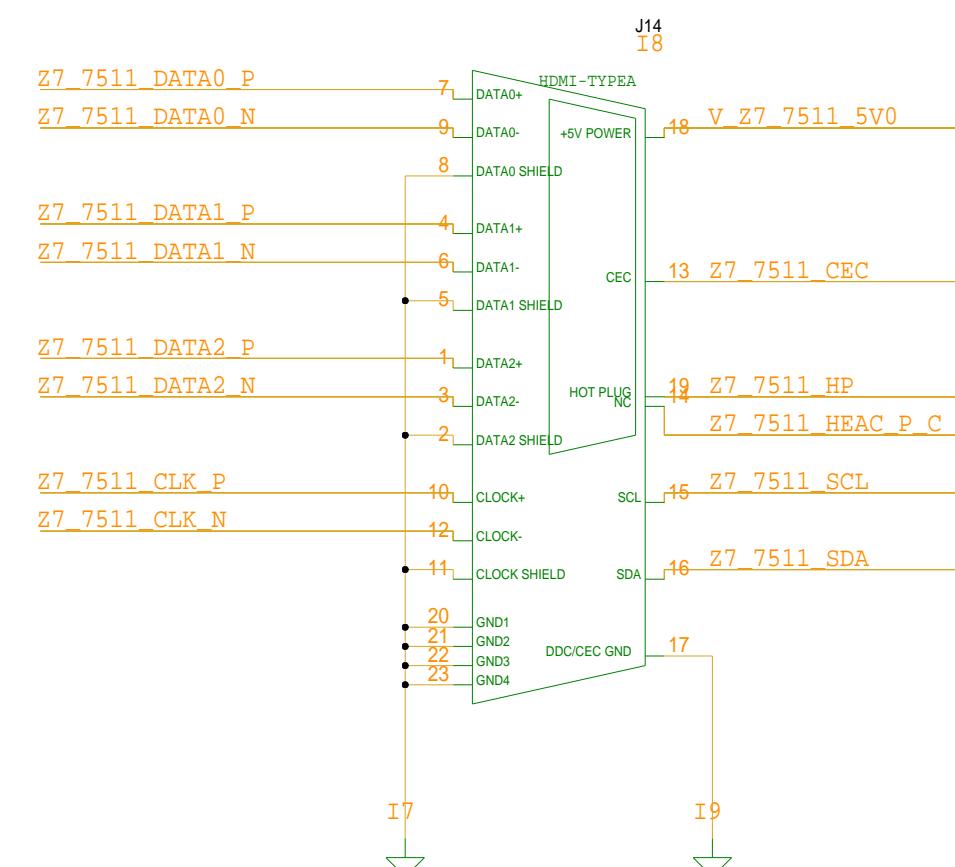
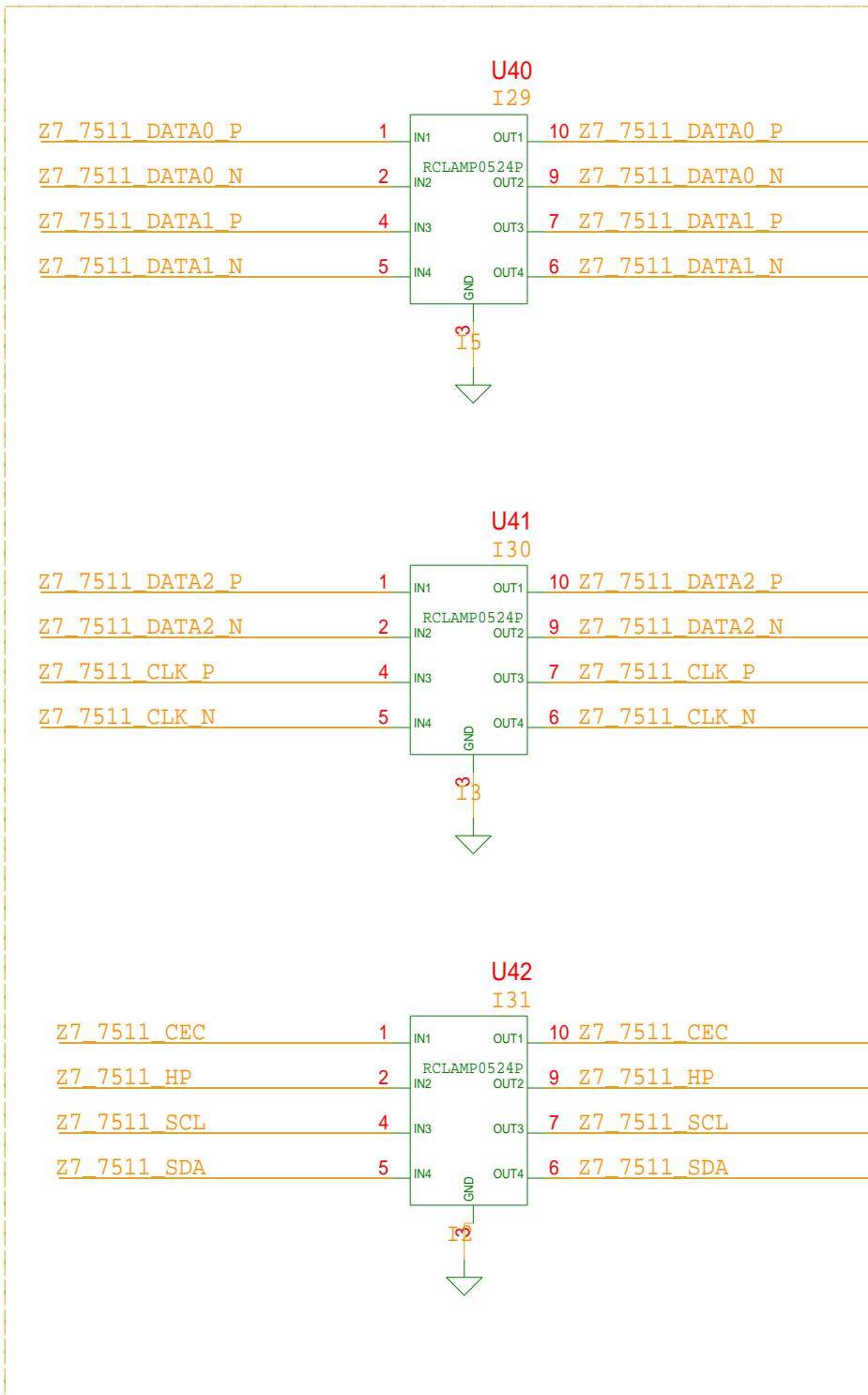
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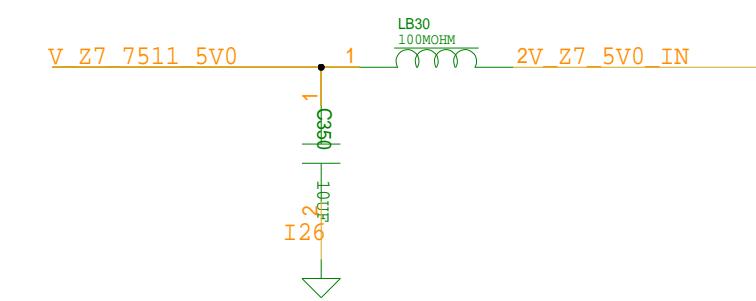
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CHANGE CONNECTION DUE TO LAYOUT

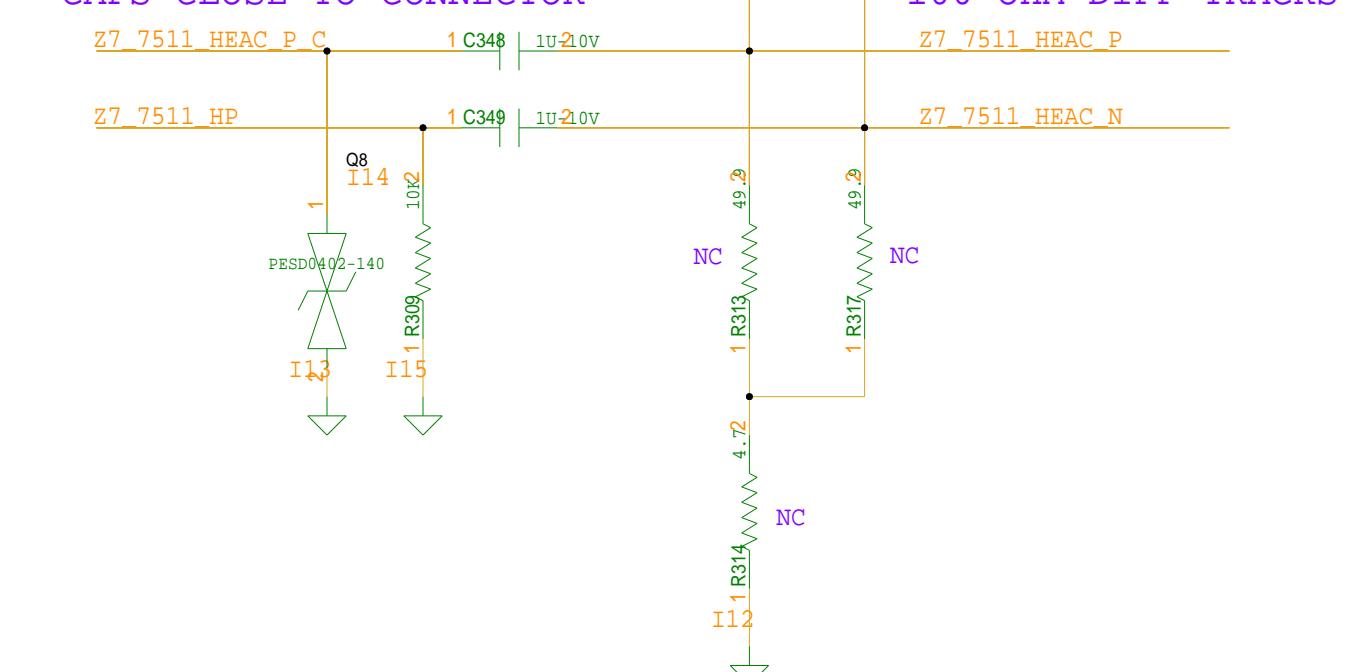


CLOSE TO HDMI CONNECTOR



Z7\_7511\_CEC (2) → D14 (1N4148) → 1 R315 (2.2kΩ) → Z7\_3V3\_7511\_MVDD (1)

CAPS CLOSE TO CONNECTOR



Z7\_7511\_SCL (1) → R310 (1.8kΩ) → Z7\_7511\_5V0 (1)  
Z7\_7511\_SDA (1) → R311 (1.8kΩ) → Z7\_7511\_5V0 (1)

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# ZYNQ-7 PL HDMI INOUT

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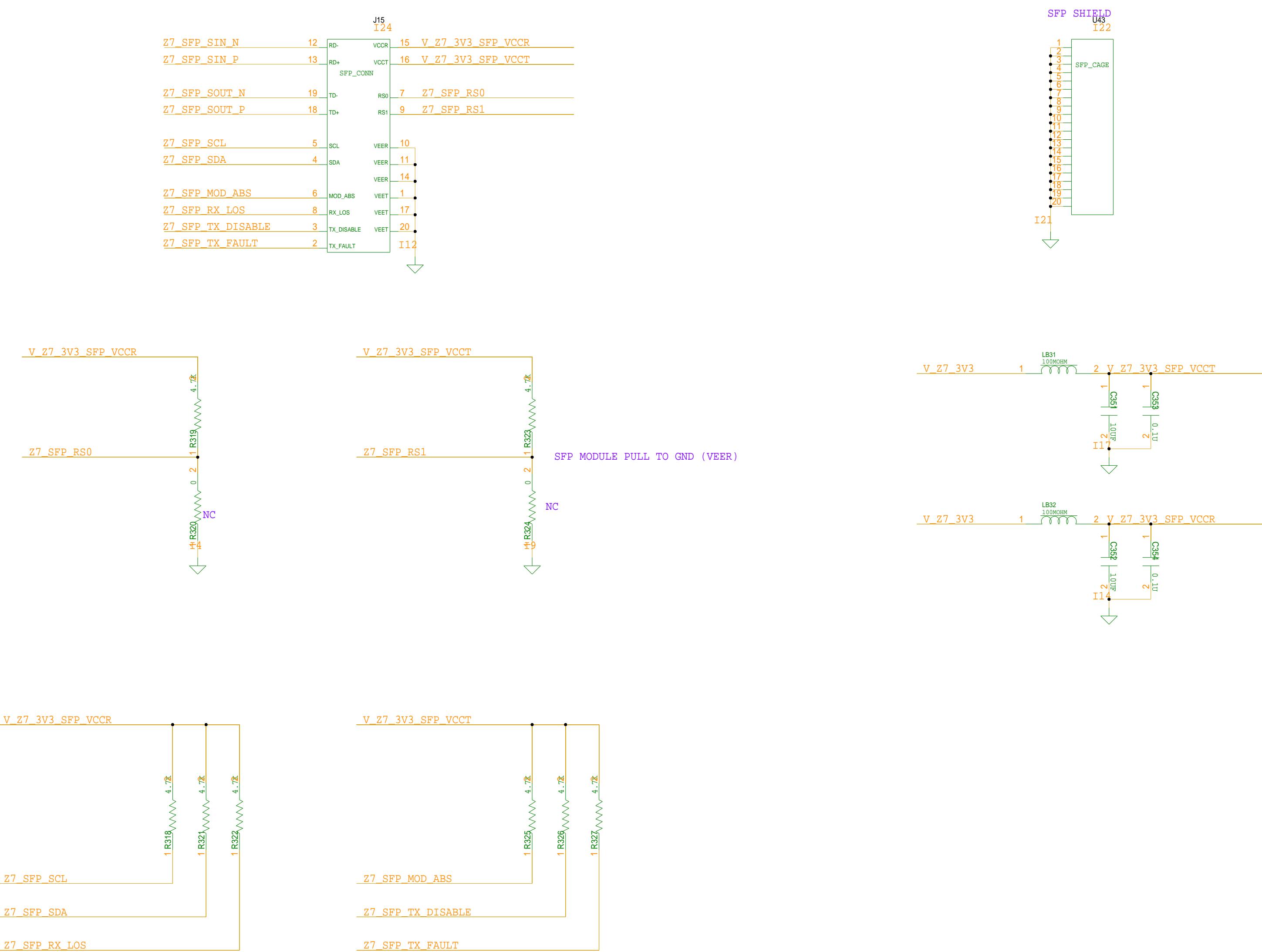
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# ZYNQ-7 PL SFP+/SFP INOUT

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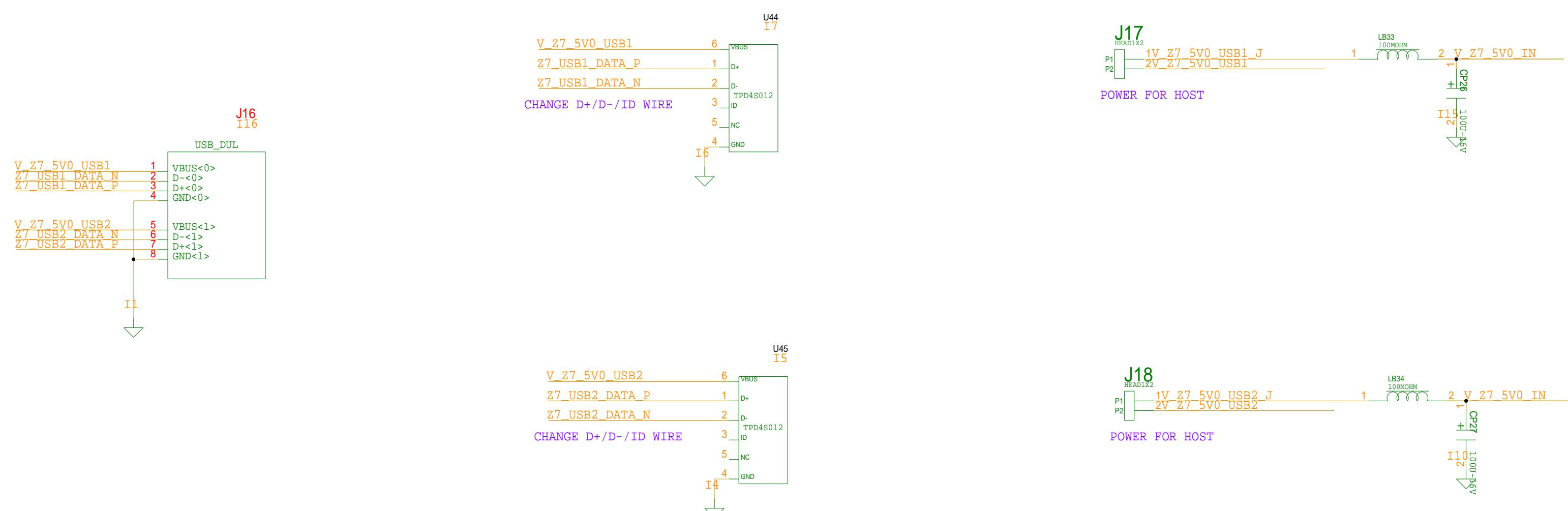
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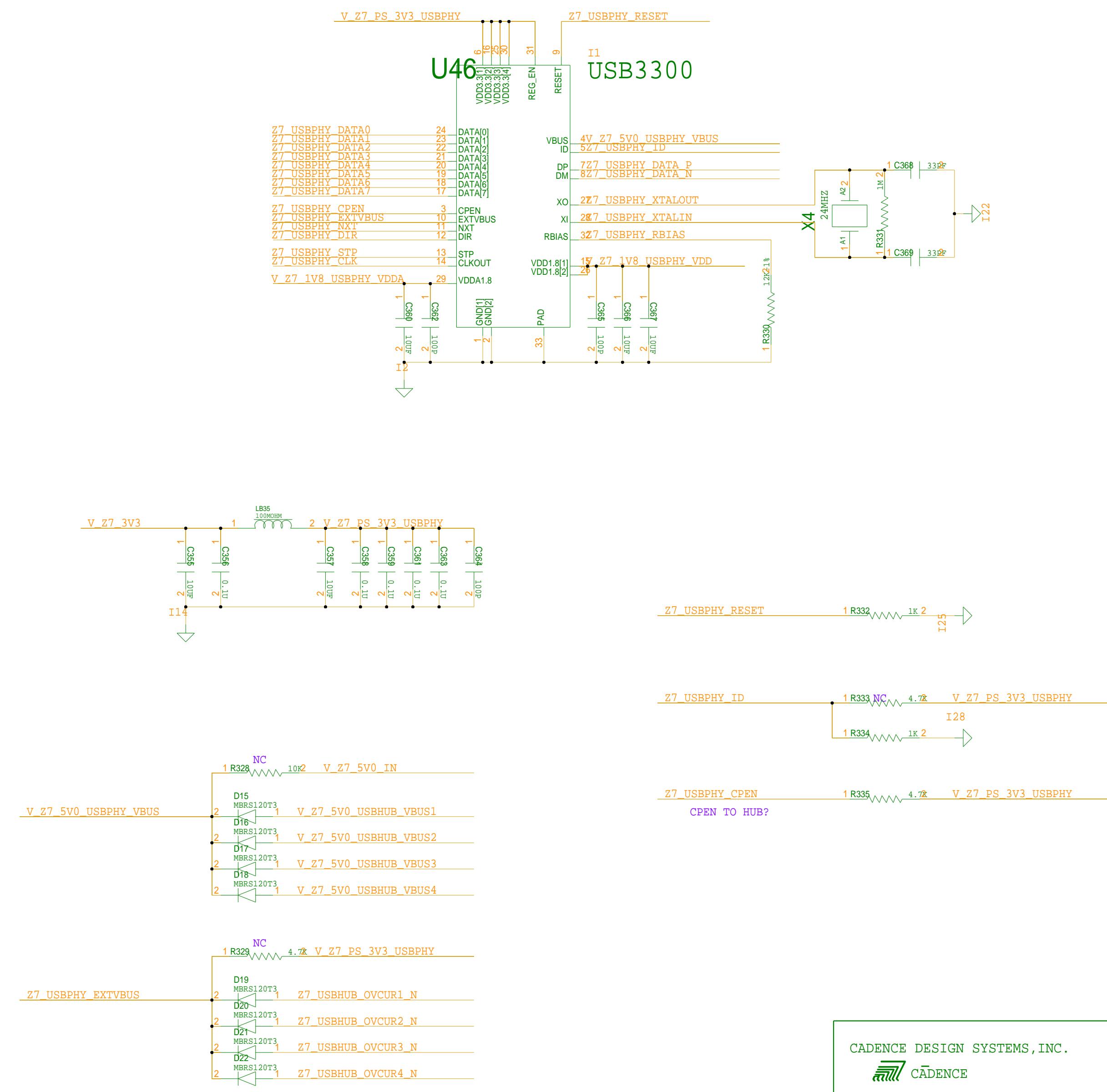


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## ZYNQ-7 PL USB PHY (1)



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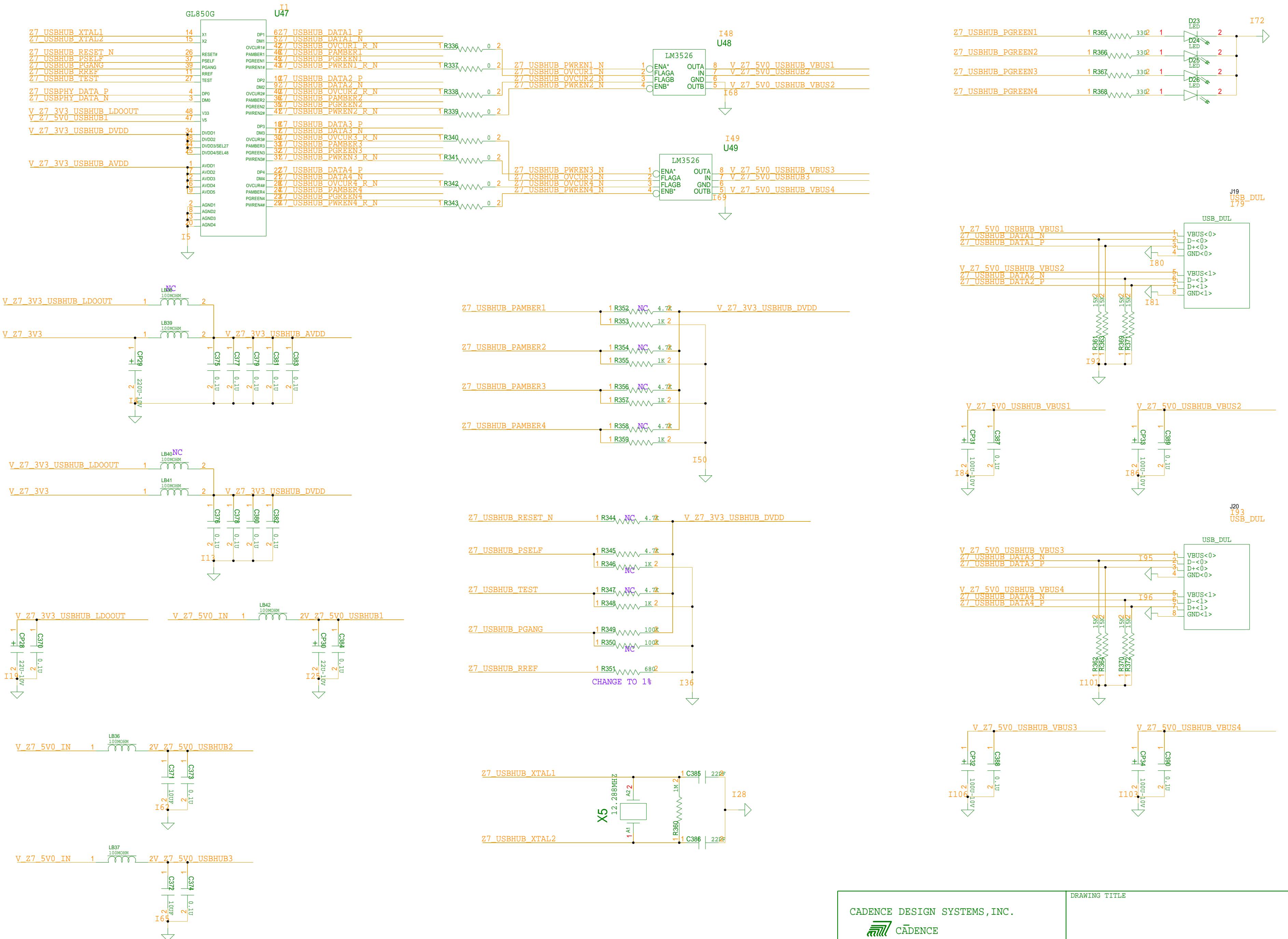
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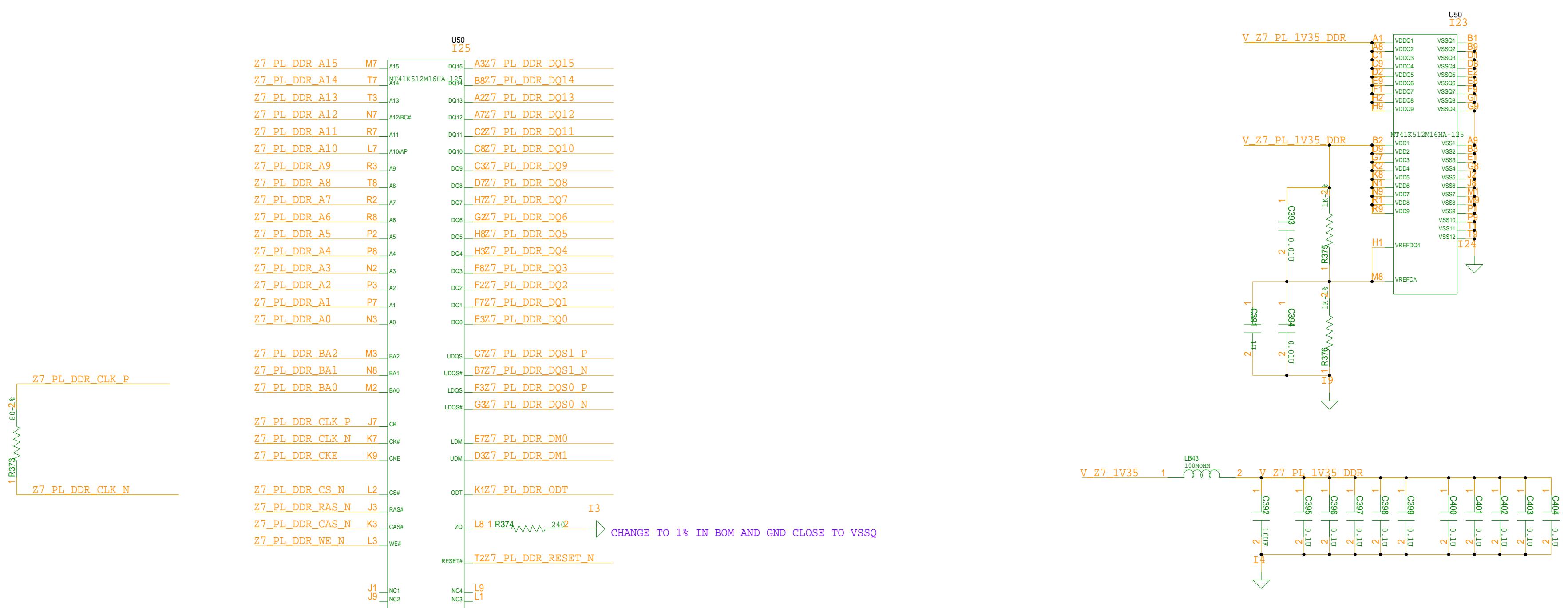
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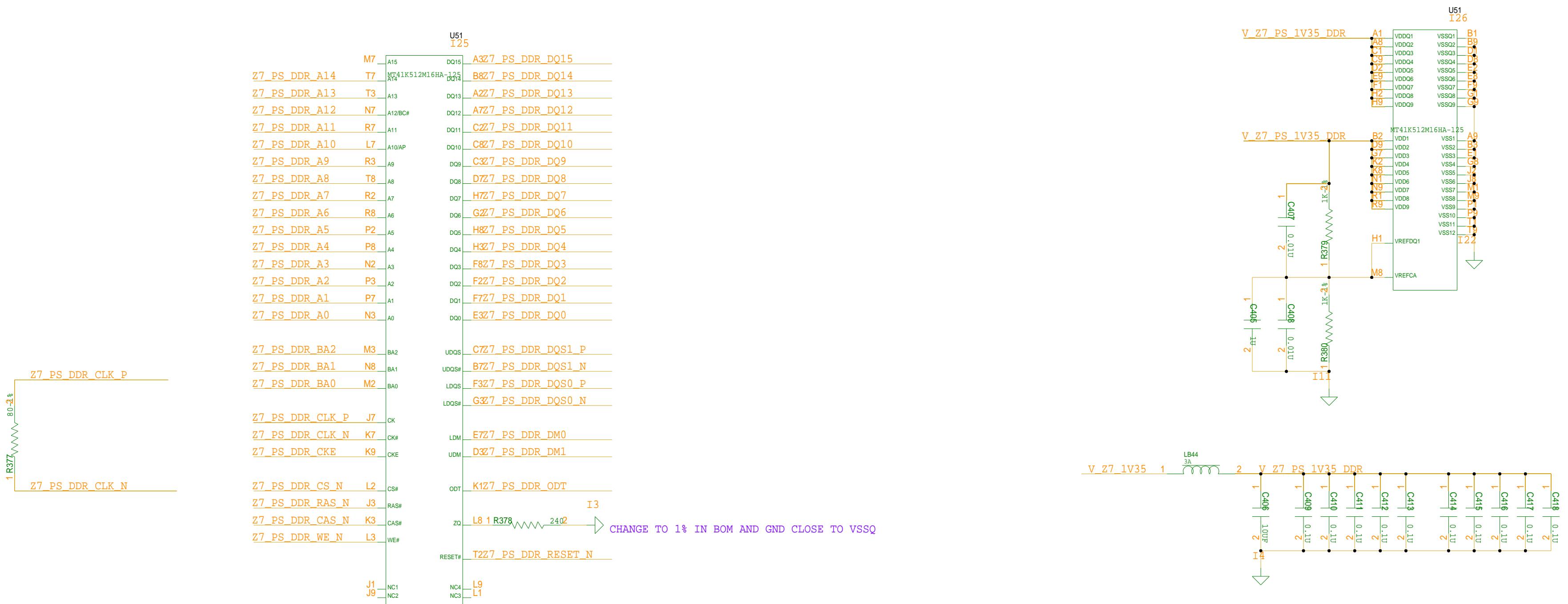
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# ZYNQ-7 PS DDR3 (1)

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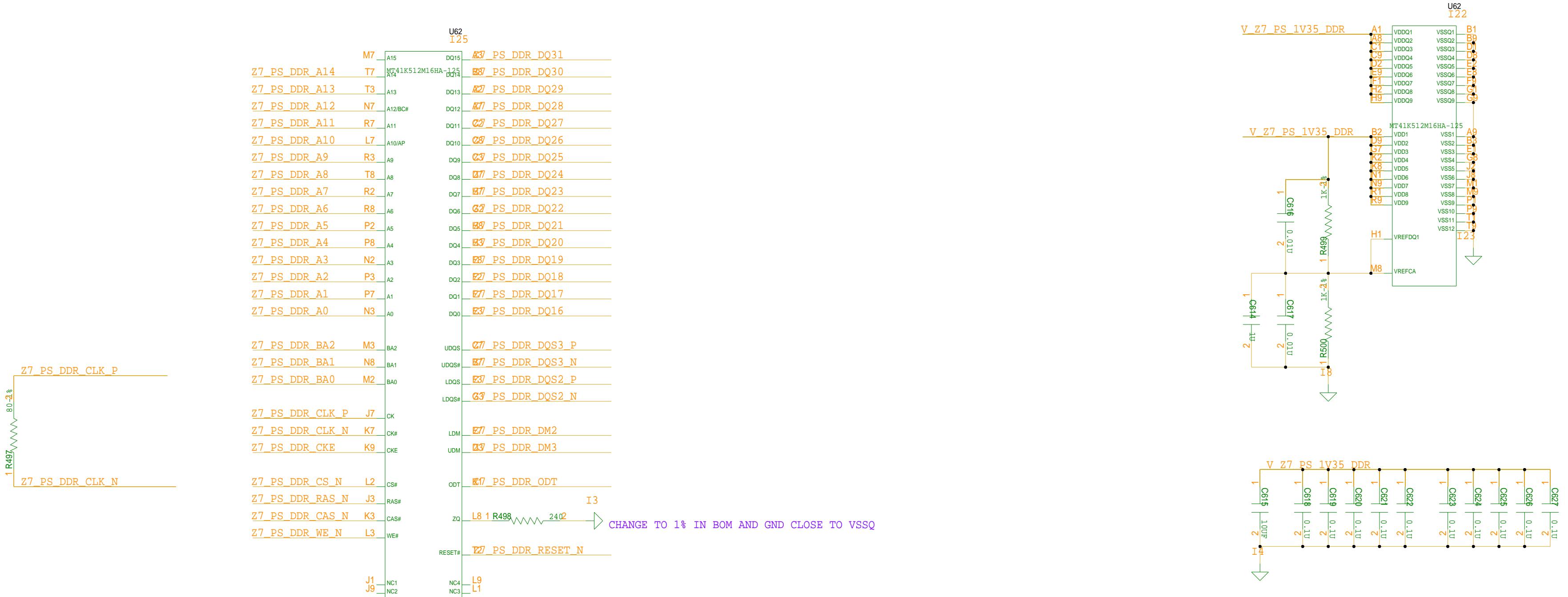
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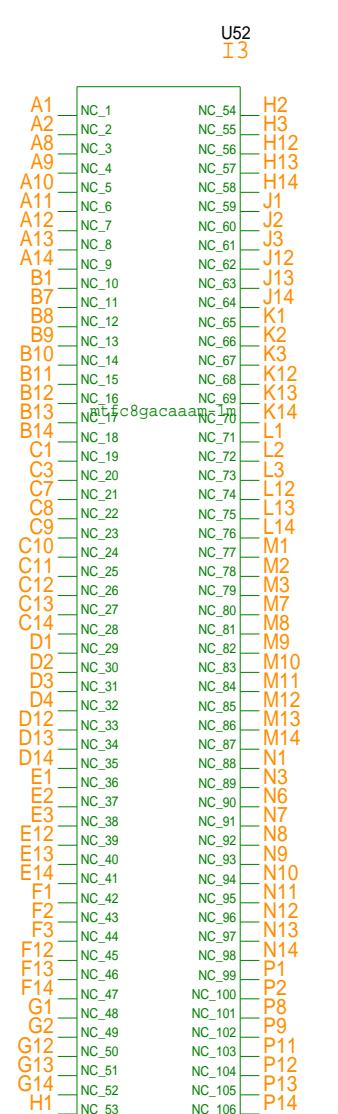
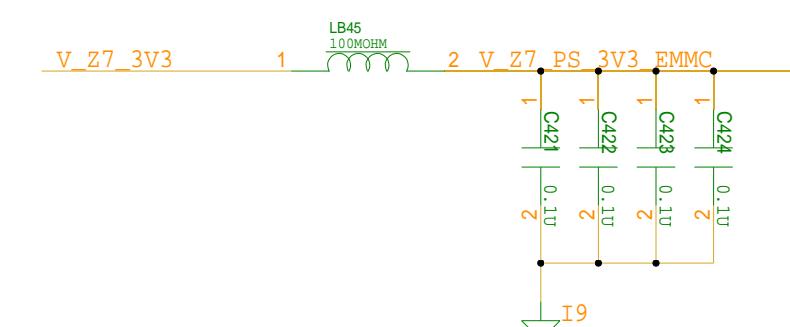
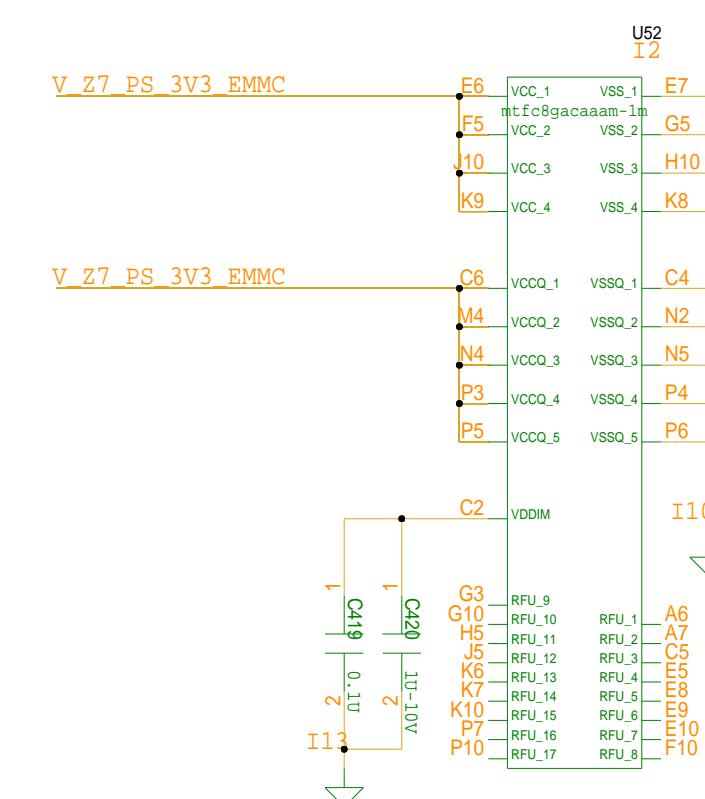
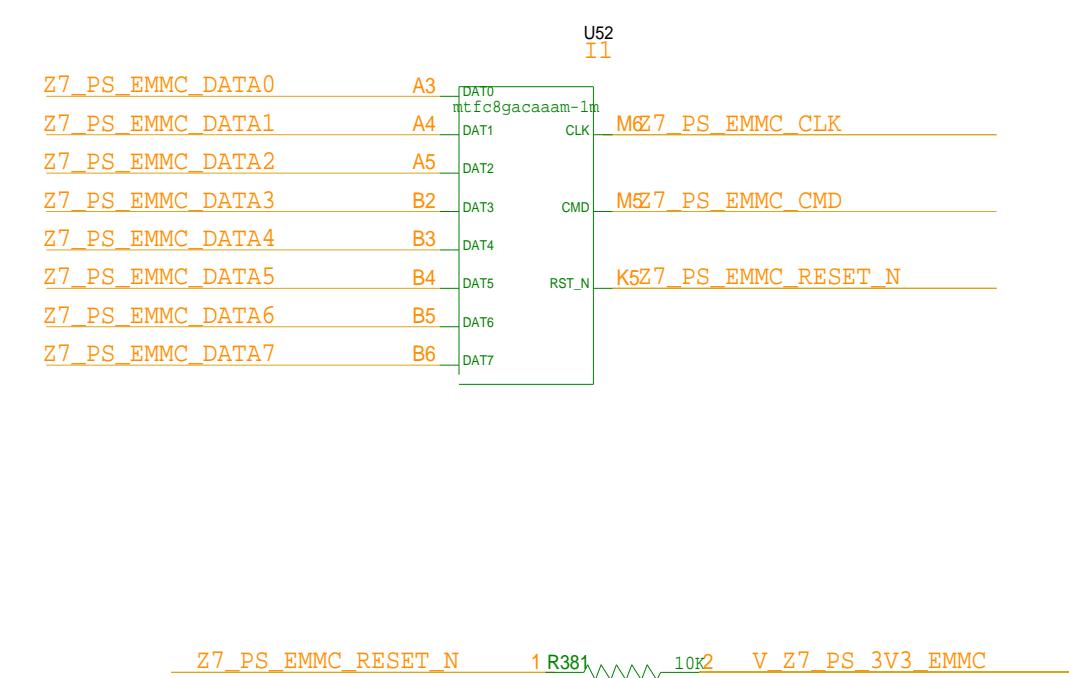
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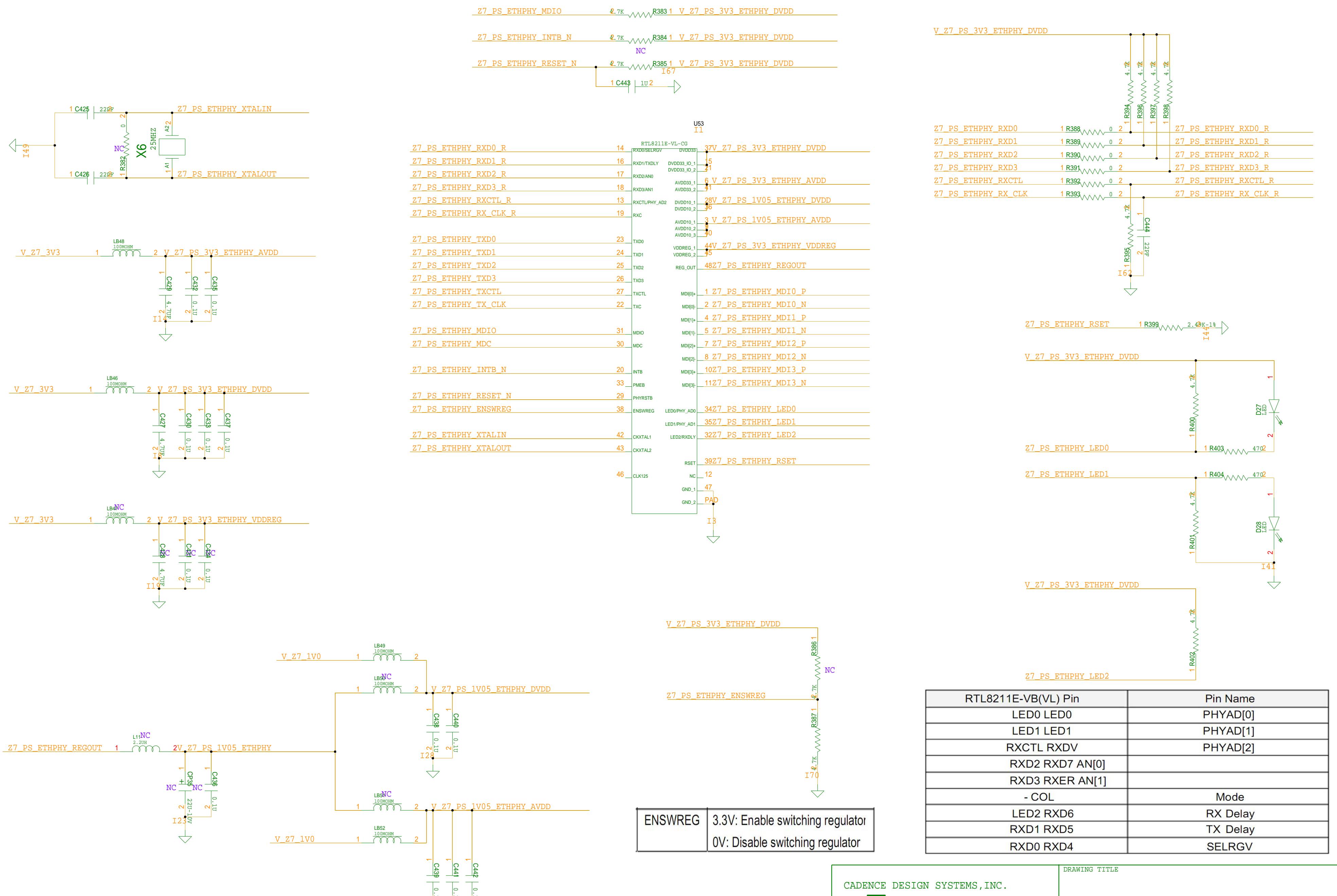
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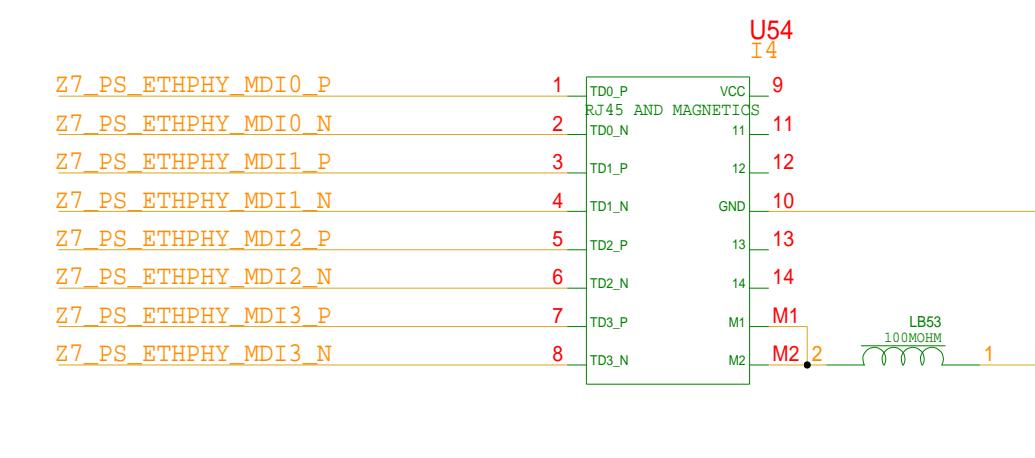
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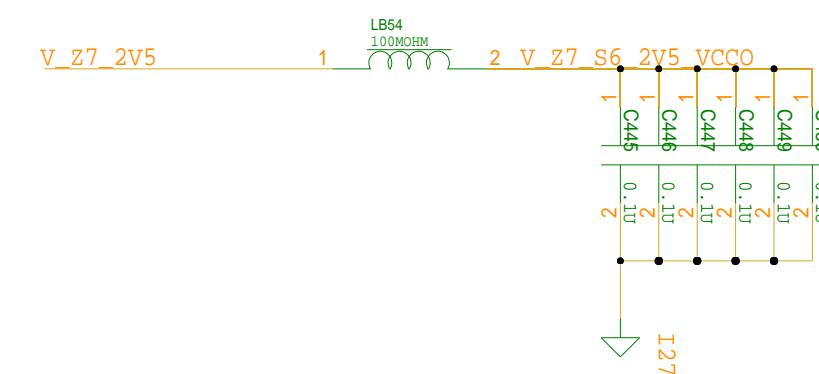
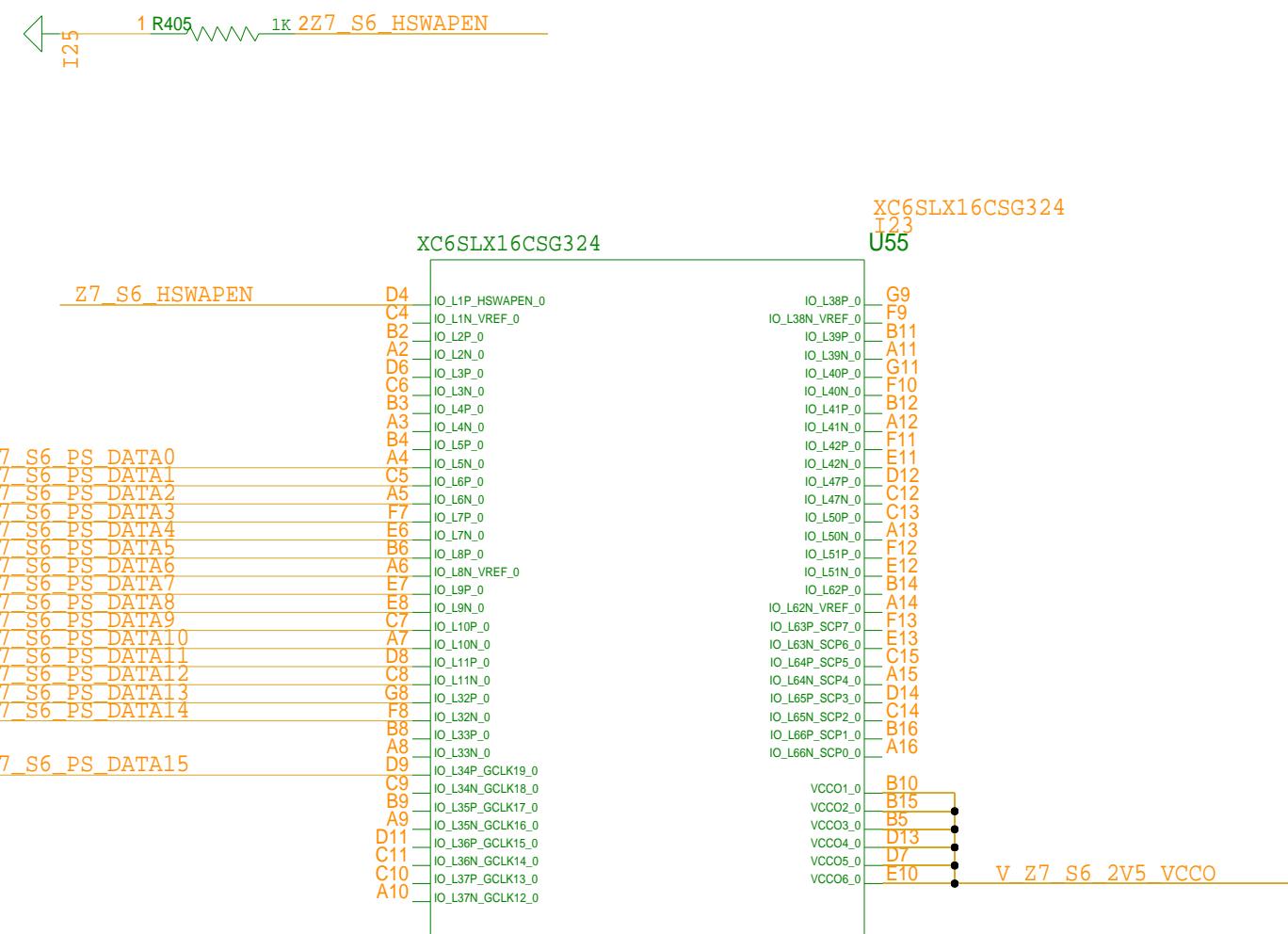


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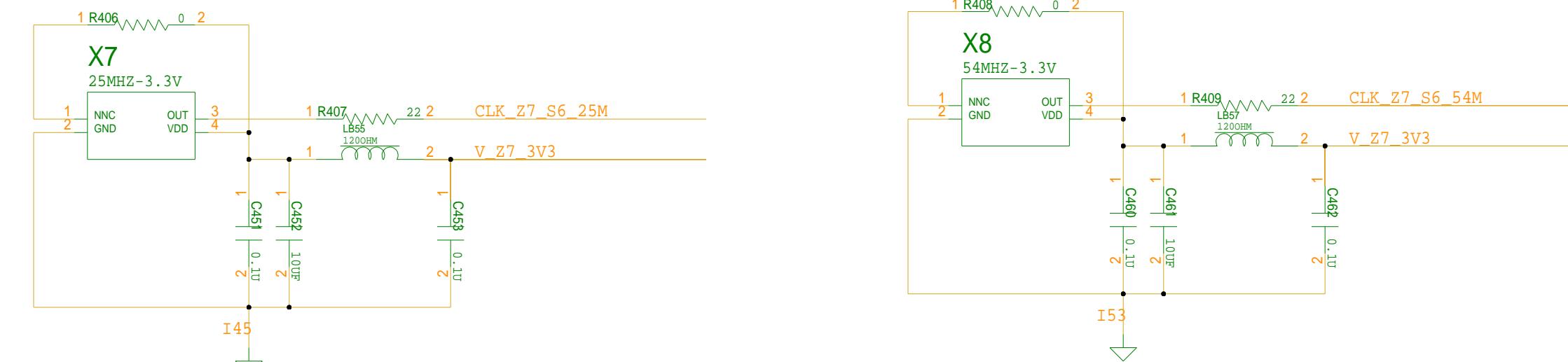
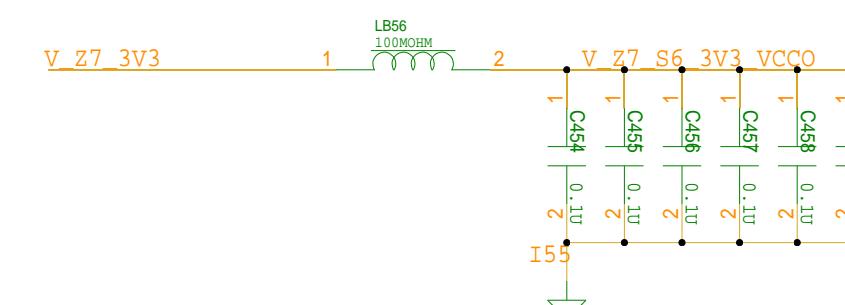
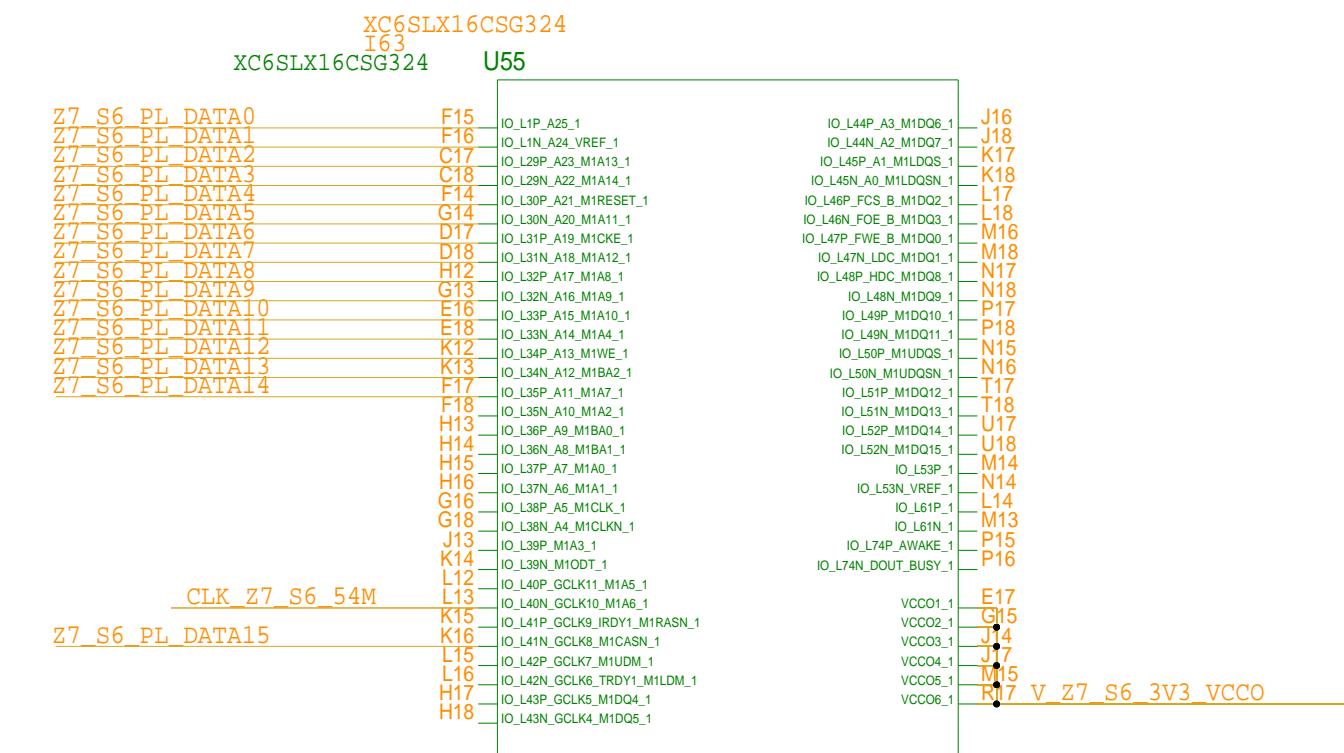
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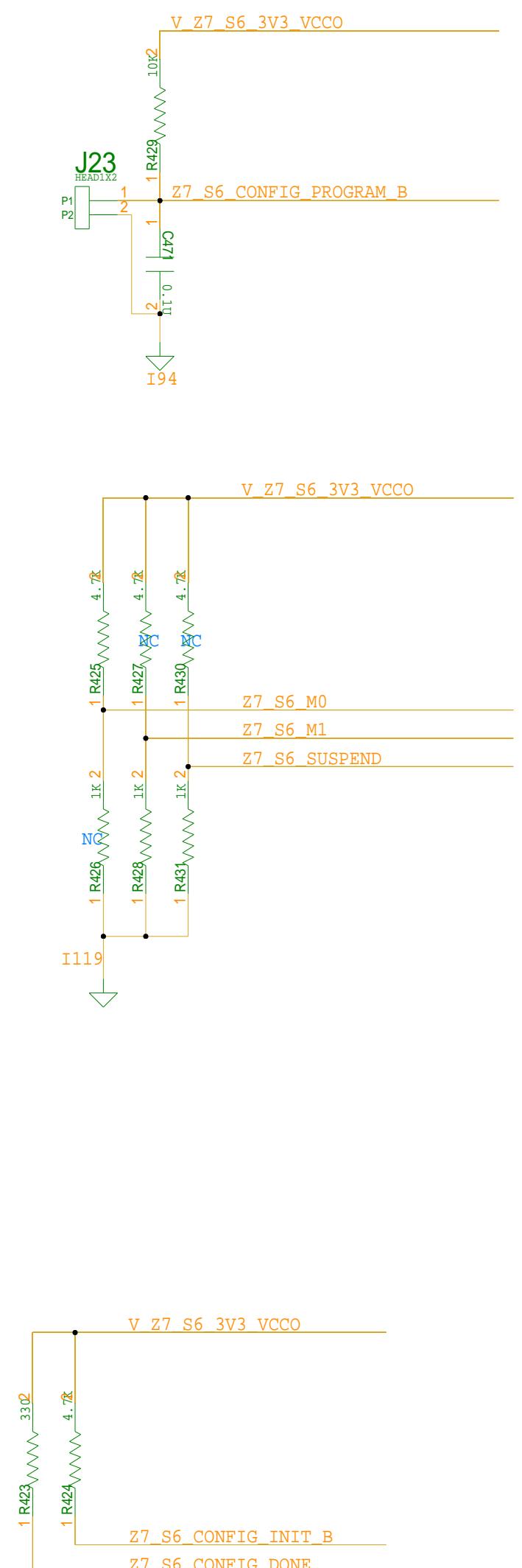
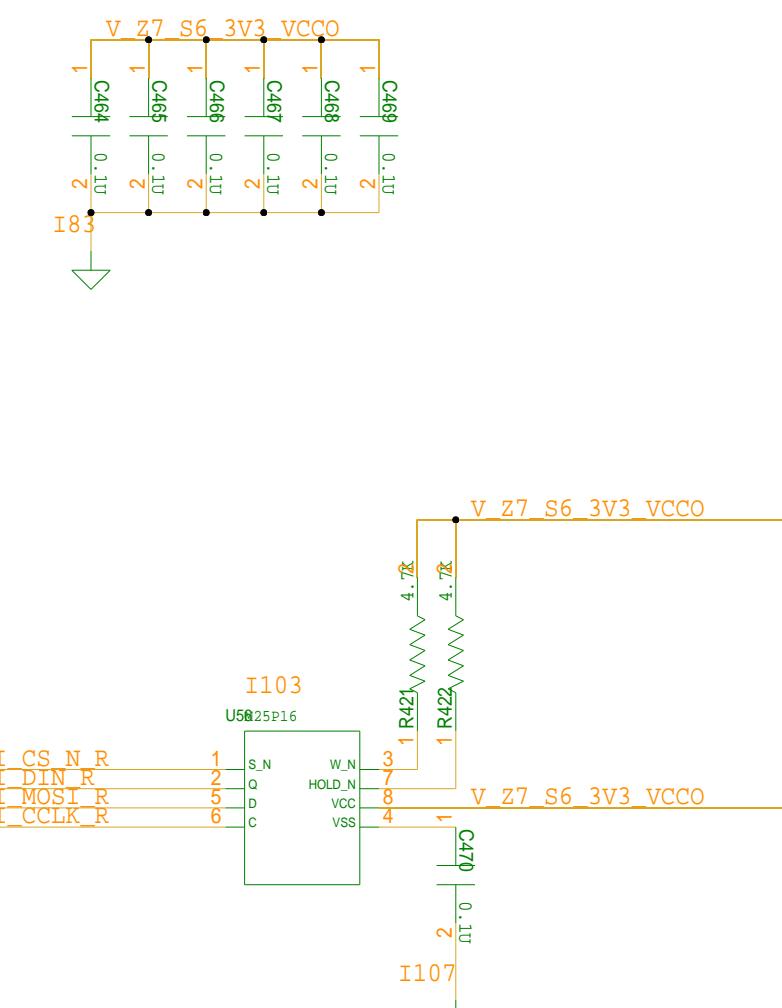
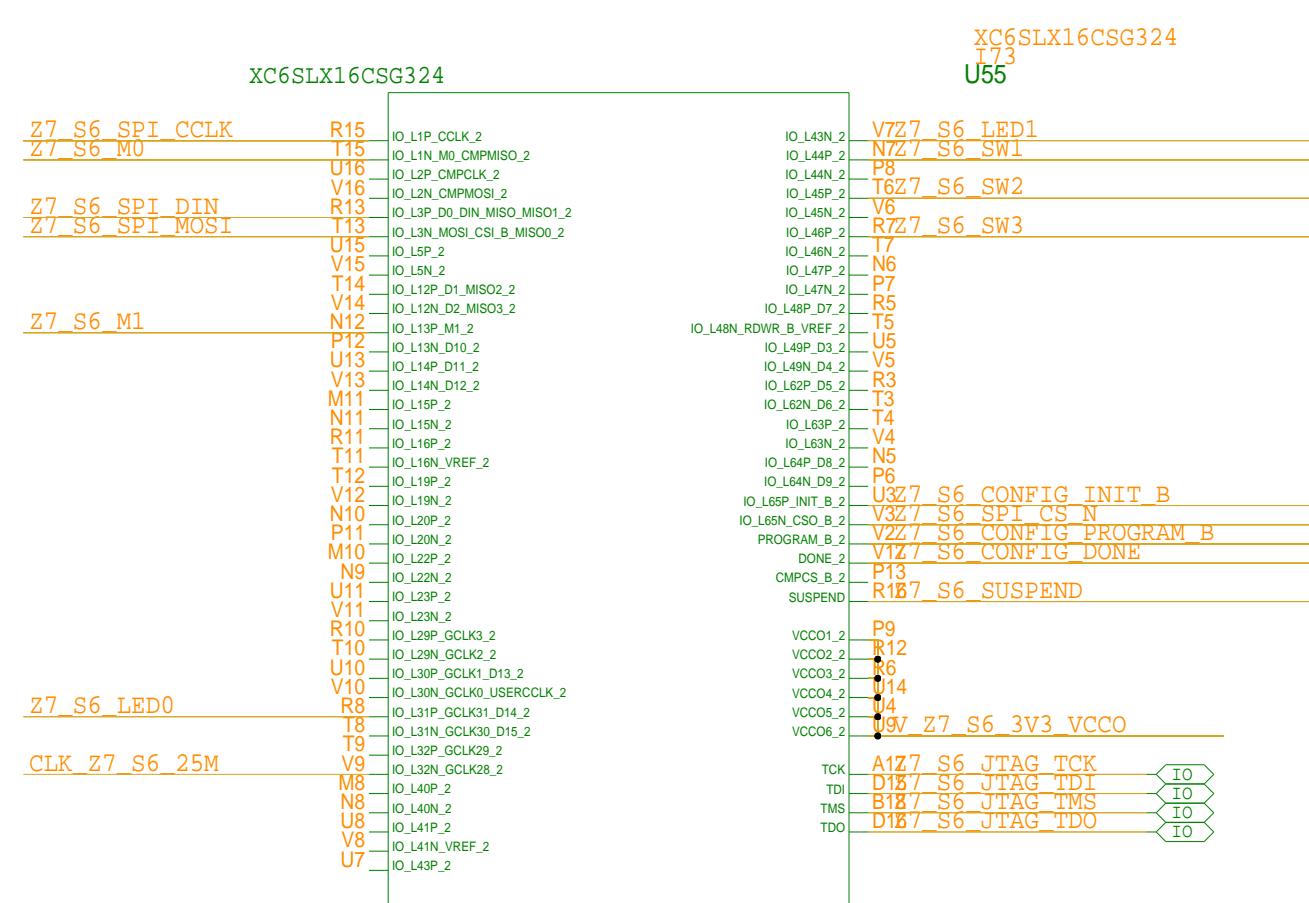
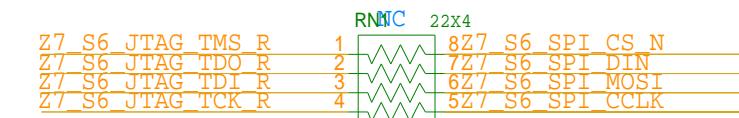
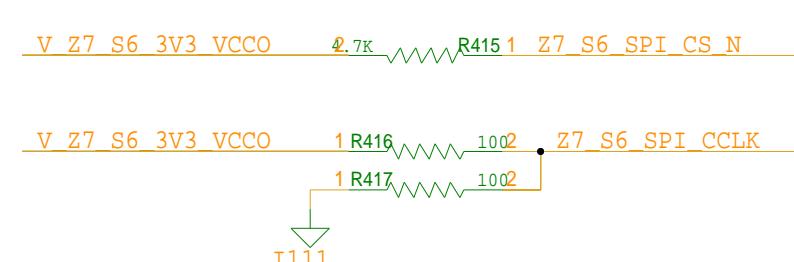
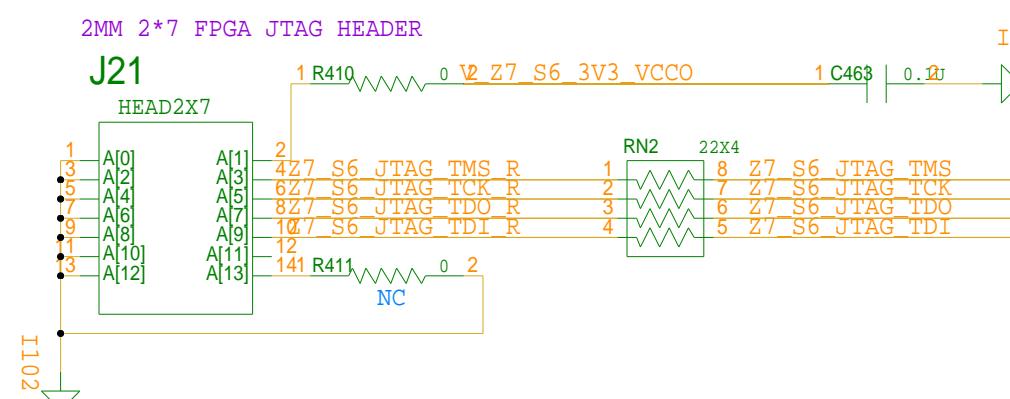
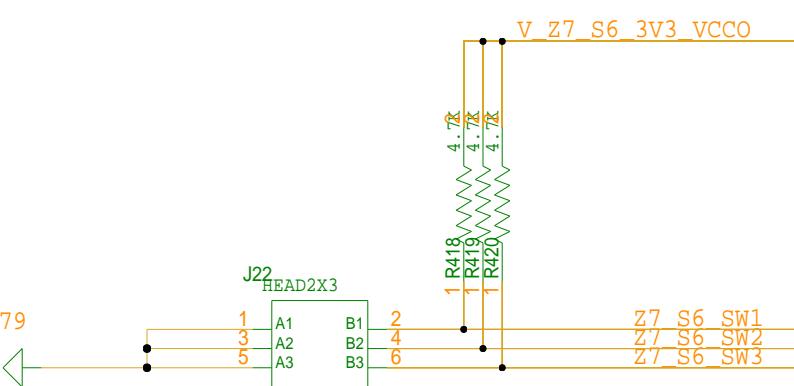
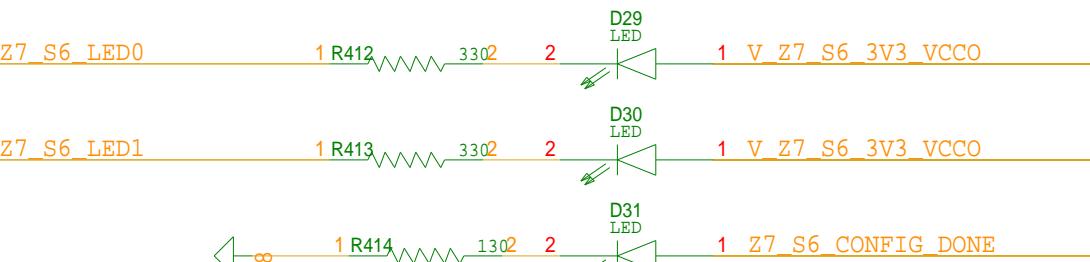
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# ZYNQ-7 SPARTAN6 (3)

## REVISIONS

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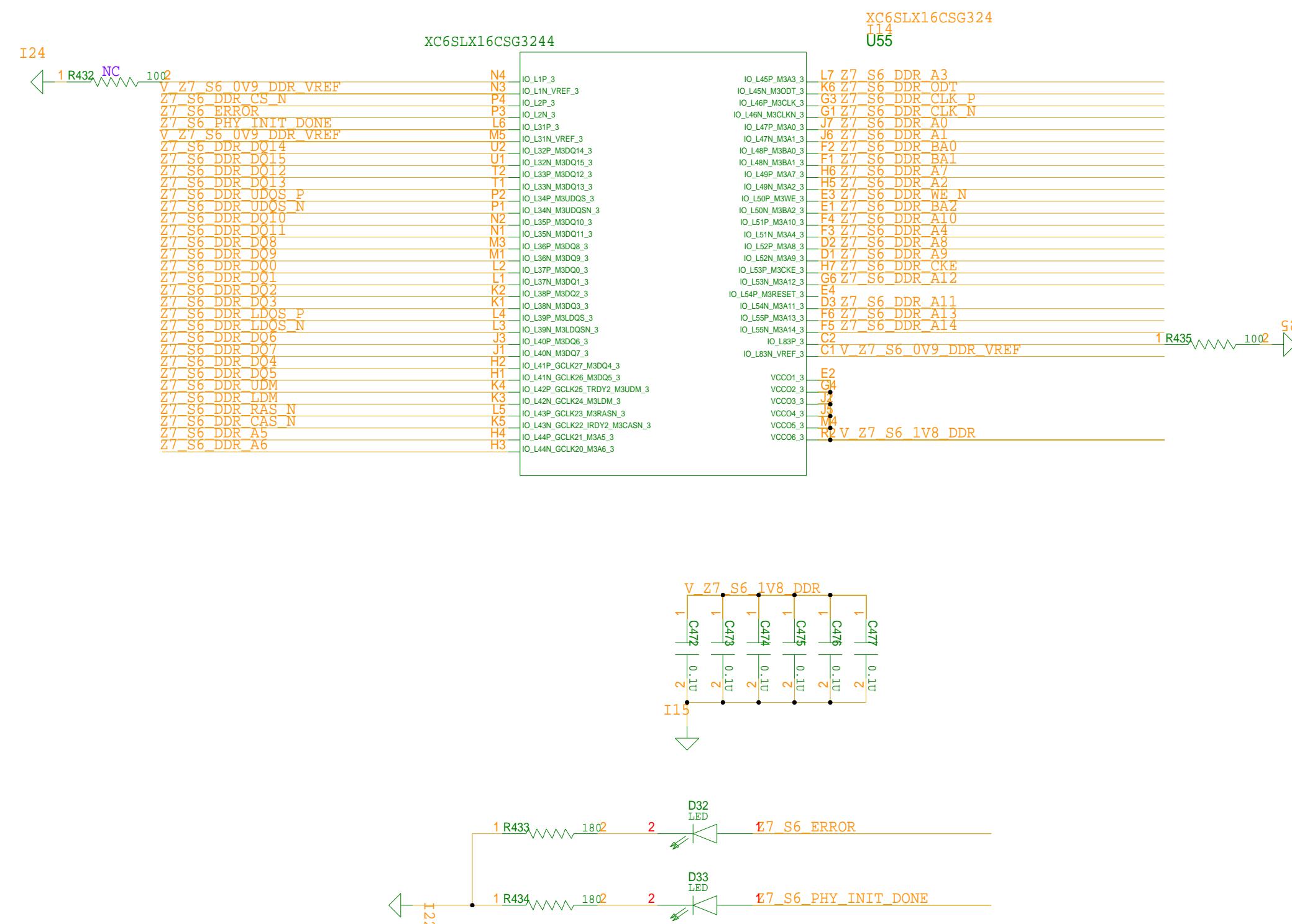
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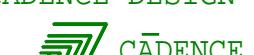
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## ZYNQ-7 SPARTAN6 (4)

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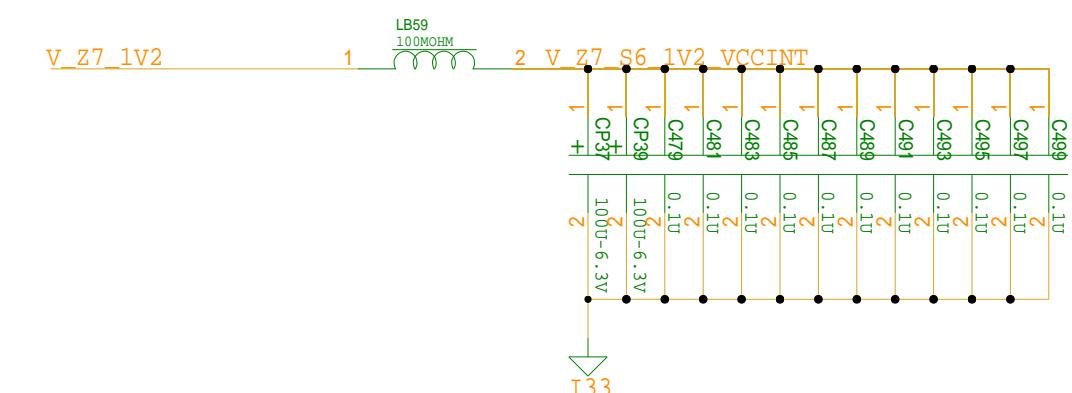
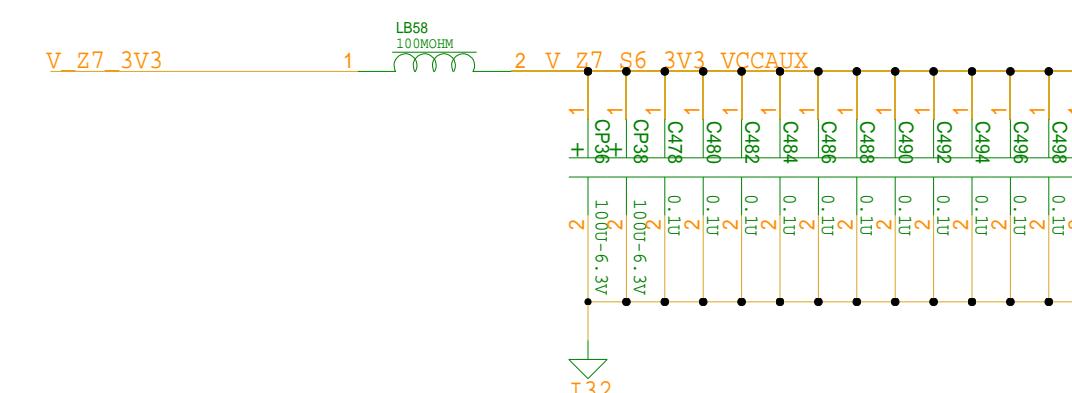
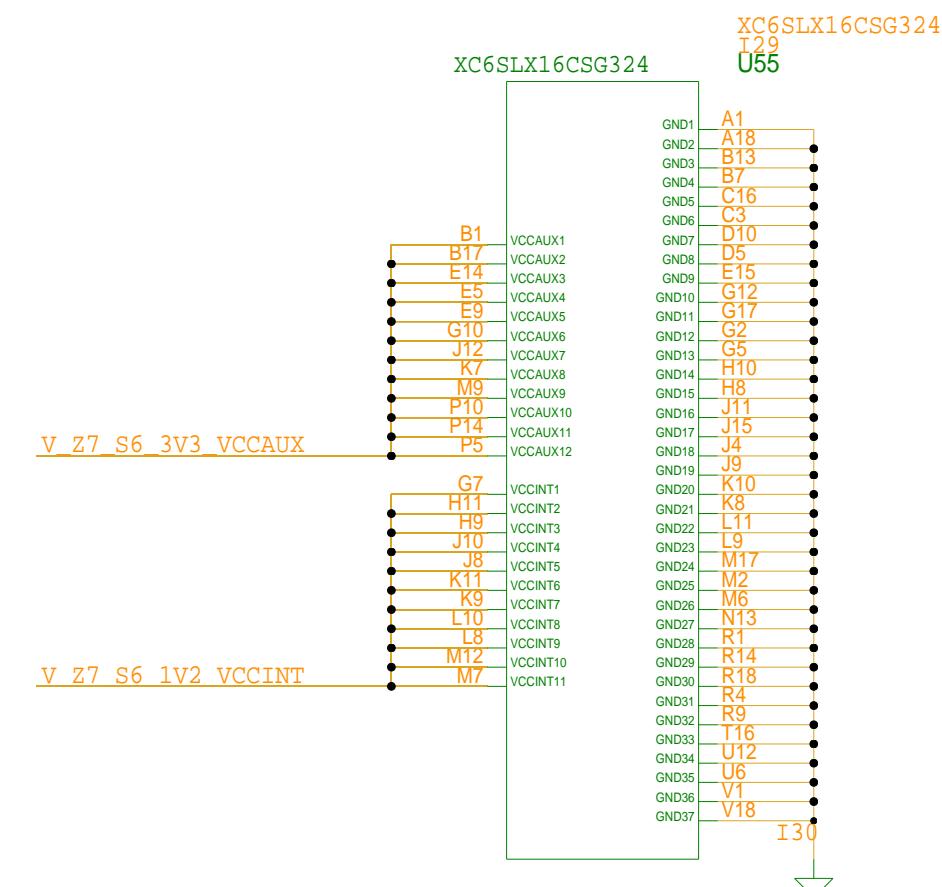
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# ZYNQ-7 SPARTAN6 (5)

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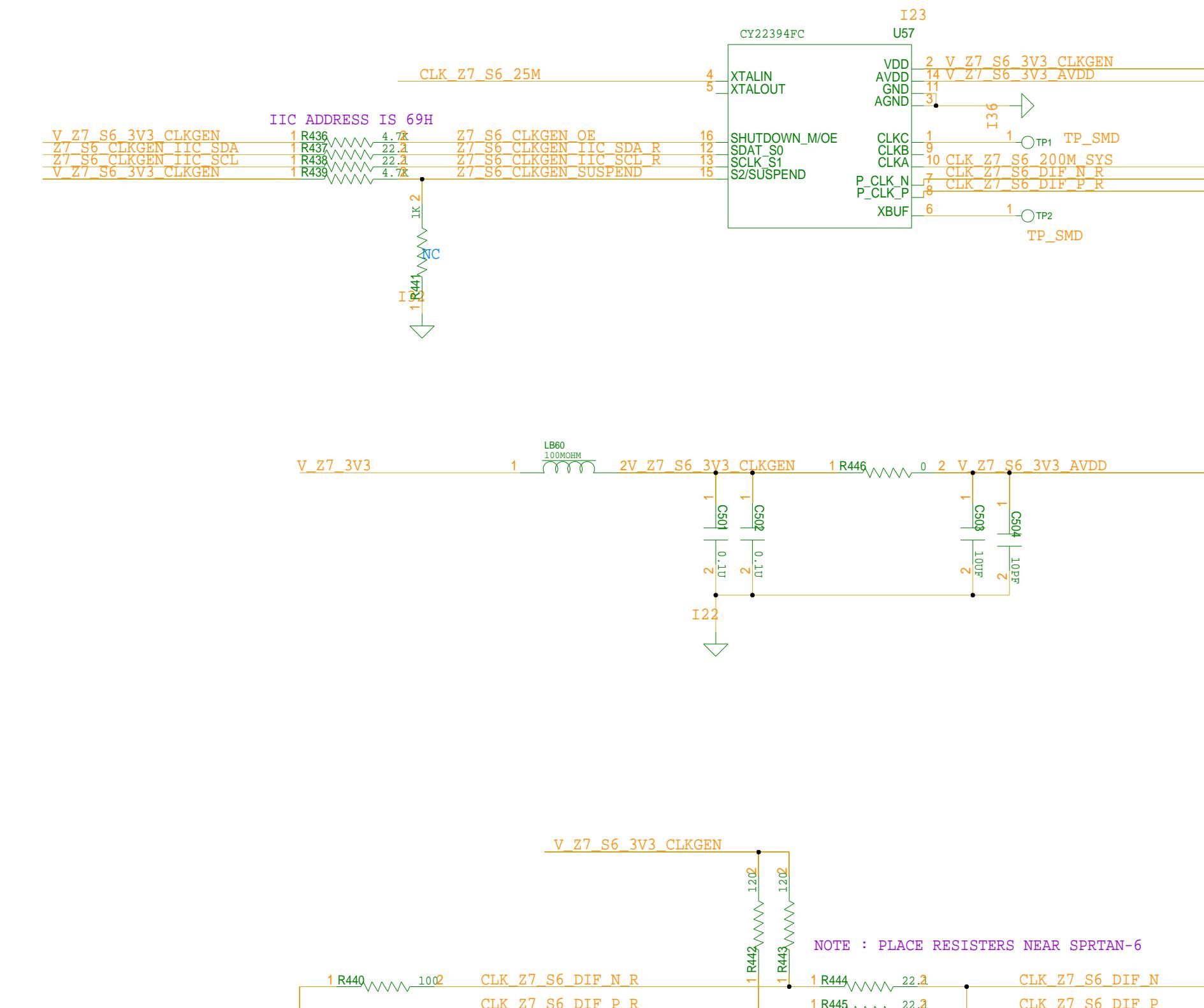
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## REVISIONS

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## FPGA DDR2 200M-CLOCK



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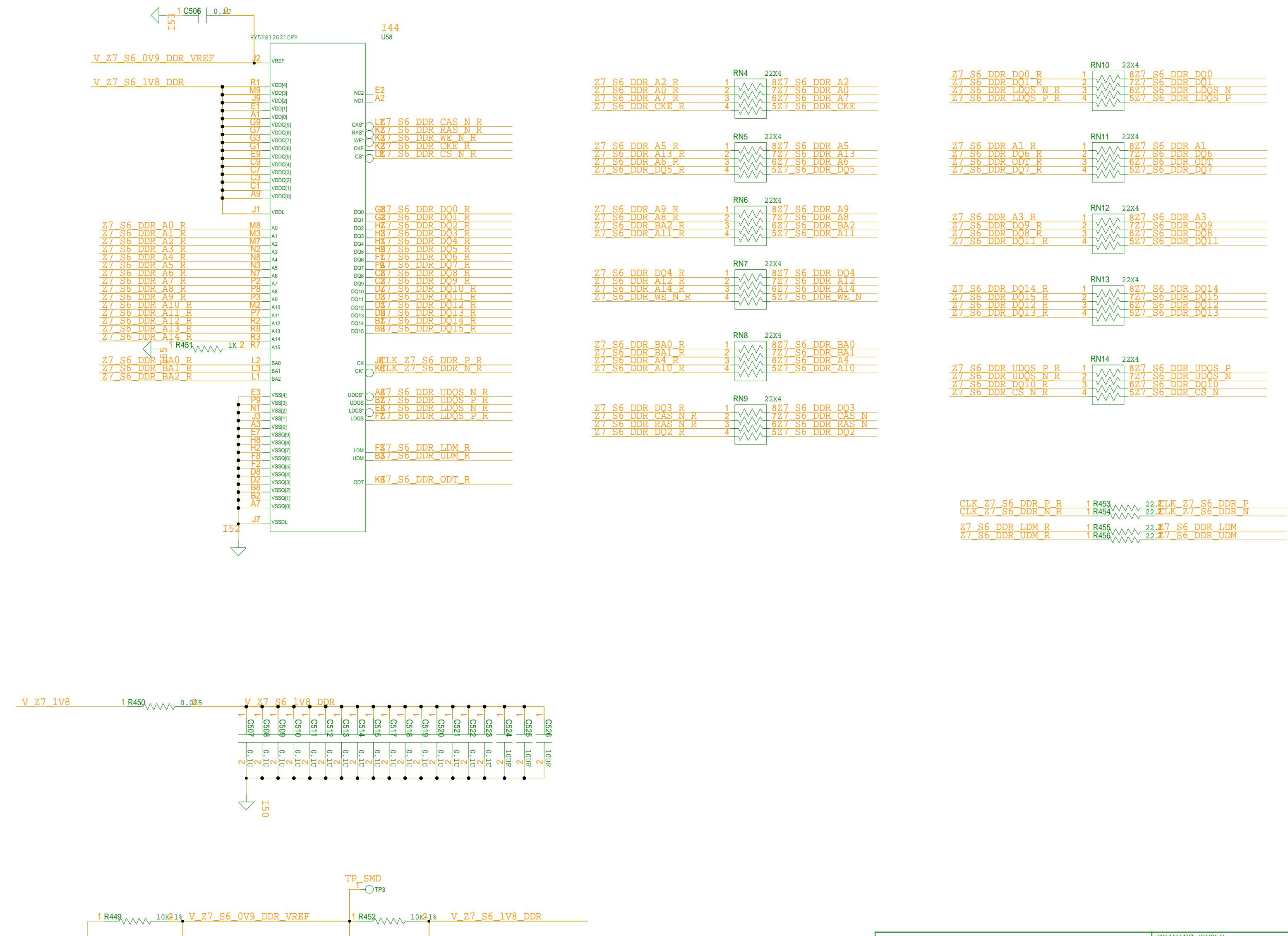
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# ZYNQ-7 SPARTAN6 (7)

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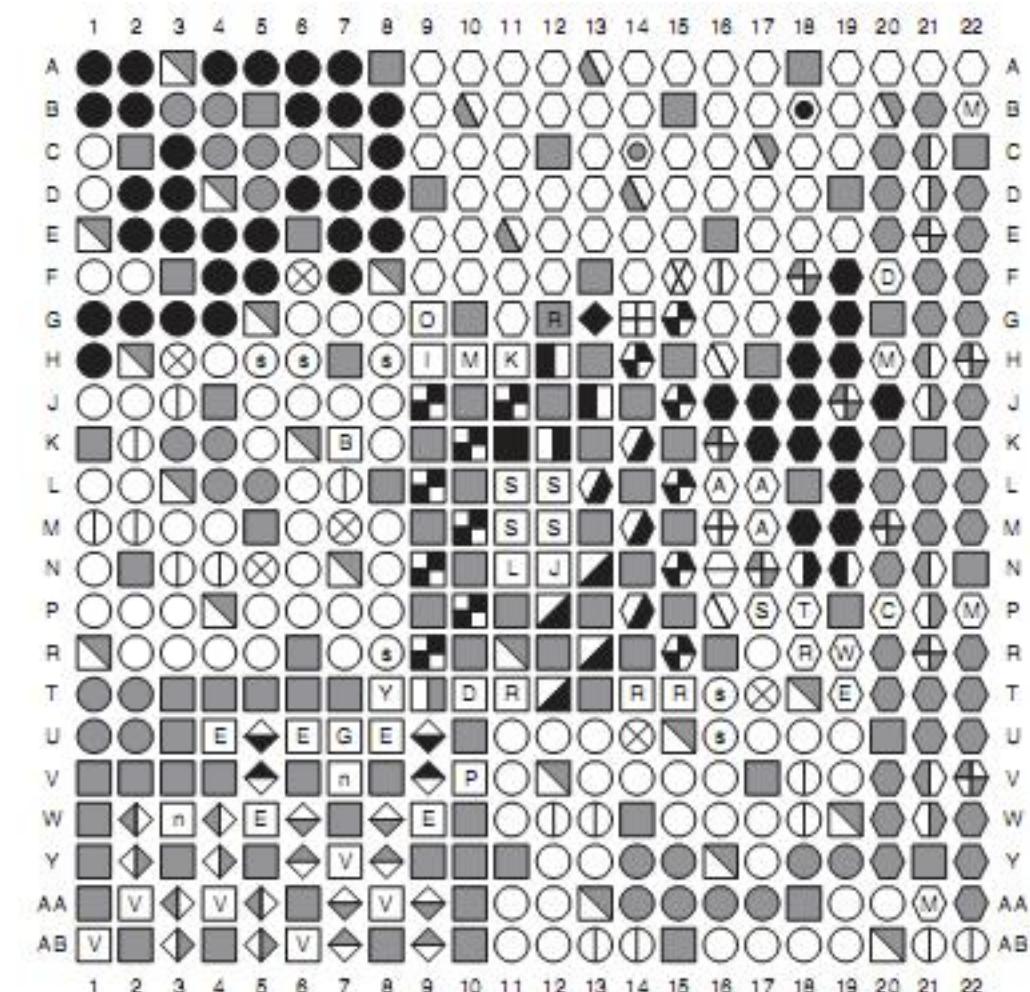
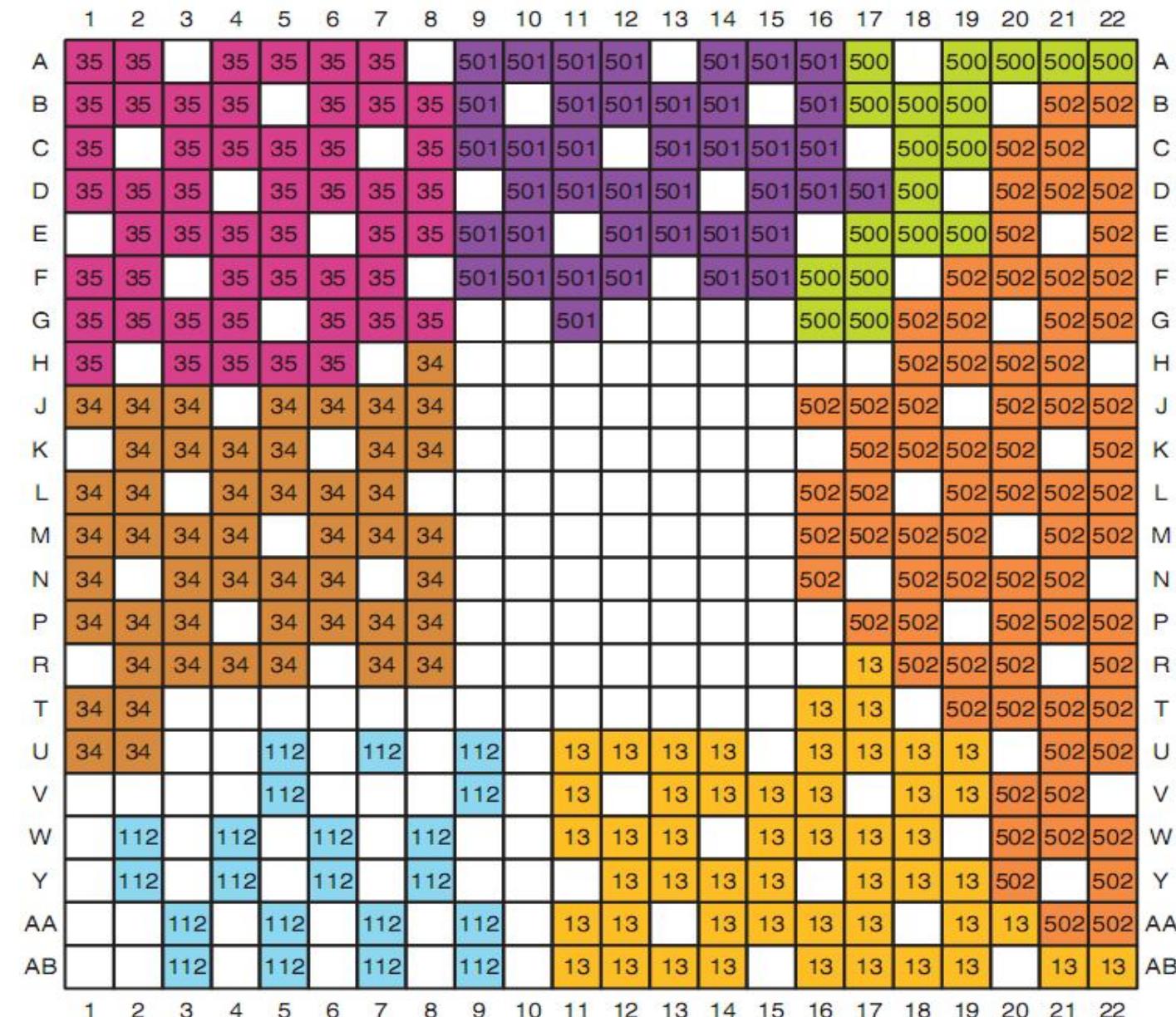
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# ZYNQ-7 PINOUT MAP

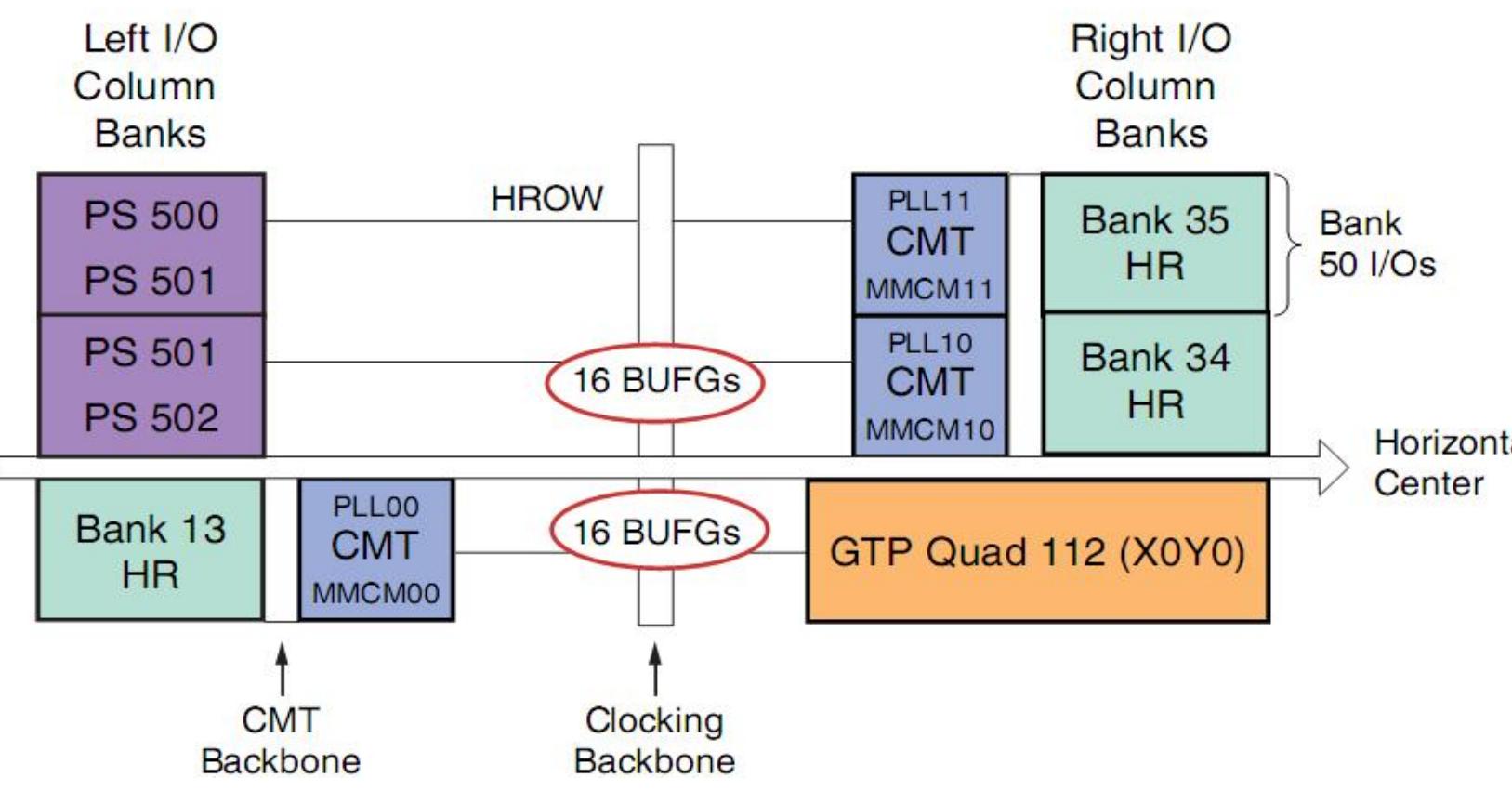
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BANK35 : 3.3V SPARTAN6/ USB/HDMI INOUT  
BANK34 : 1.35V DDR3  
BANK13 : 3.3V HDMI TRANSMITER  
BANK112 : SFP

BANK502 : 1.35V DDR3\*2  
BANK501 : 2.5V SPARTAN6/ 88E1111  
BANK500 : 3.3V SPI FLASH



User I/O Pins	Transceiver Pins	Dedicated Pins	Other Pins	PS MIO Pins	PS DDR Pins
<ul style="list-style-type: none"> <li>○ IO_LXXY_#</li> <li>● IO_XX_#</li> </ul>	<ul style="list-style-type: none"> <li>E MGTAVCC_G#</li> <li>V MGTAVTT_G#</li> <li>A MGTVCVAUX_G#</li> <li>&lt; MGTAVTTRCAL</li> <li>G MGTRREF</li> <li>◆ MGTRFCLK1OP</li> <li>◆ MGTRFCLK1ON</li> <li>◆ MGTPRXP</li> <li>◆ MGTPRXN</li> <li>◆ MGTPTXP</li> <li>◆ MGPTXN</li> <li>B PUDC_B</li> <li>● ADOP/ADON- AD15P/AD15N</li> <li>⊕ VRN</li> <li>⊖ VRP</li> <li>⊗ VREF</li> <li>⊖ DOS</li> <li>● MRCC</li> <li>● SRCC</li> </ul>	<ul style="list-style-type: none"> <li>■ CFGBVS_0</li> <li>□ DONE_0</li> <li>■ DXP_0</li> <li>■ DXN_0</li> <li>■ GNDADC_0</li> <li>■ INIT_B_0</li> <li>■ PROGRAM_B_0</li> <li>■ TCK_0</li> <li>■ TD_L0</li> <li>■ TDO_0</li> <li>■ TMS_0</li> <li>■ VCCADC_0</li> <li>■ VCCBATT_0</li> <li>■ VP_0</li> <li>■ VN_0</li> <li>■ VREFP_0</li> <li>■ VREFN_0</li> </ul>	<ul style="list-style-type: none"> <li>■ GND</li> <li>■ VCCAUX_IO_G#</li> <li>■ VCCAUX</li> <li>■ VCCINT</li> <li>■ VCCO_#</li> <li>■ VCCBRAM</li> <li>■ VCCPINT</li> <li>■ VCCPAUX</li> <li>■ VCCO_MIO0</li> <li>■ VCCO_MIO1</li> <li>■ VCCO_DDR</li> <li>■ VCCPLL</li> <li>■ RSVDVCC[3:1]</li> <li>■ RSVDGND</li> <li>n NC</li> </ul>	<ul style="list-style-type: none"> <li>● PS_POP_B</li> <li>○ PS_CLK</li> <li>○ PS_SRST_B</li> <li>⊗ PS_MIO_VREF</li> <li>○ PS_MIO</li> </ul>	<ul style="list-style-type: none"> <li>○ PS_DDR_CKP</li> <li>○ PS_DDR_CKN</li> <li>● PS_DDR_CKE</li> <li>● PS_DDR_CS_B</li> <li>○ PS_DDR_RAS_B</li> <li>○ PS_DDR_CAS_B</li> <li>● PS_DDR_WE_B</li> <li>● PS_DDR_BA</li> <li>● PS_DDR_A</li> <li>○ PS_DDR_ODT</li> <li>○ PS_DDR_DRST_B</li> <li>● PS_DDR_DO</li> <li>● PS_DDR_DM</li> <li>● PS_DDR_DOS_P</li> <li>● PS_DDR_DOS_N</li> <li>○ PS_DDR_VRP</li> <li>● PS_DDR_VRN</li> <li>○ PS_DDR_VREF</li> </ul>
<ul style="list-style-type: none"> <li>○ IO_LXXY_#</li> <li>● IO_XX_#</li> </ul>	<ul style="list-style-type: none"> <li>E MGTAVCC_G#</li> <li>V MGTAVTT_G#</li> <li>A MGTVCVAUX_G#</li> <li>&lt; MGTAVTTRCAL</li> <li>G MGTRREF</li> <li>◆ MGTRFCLK1OP</li> <li>◆ MGTRFCLK1ON</li> <li>◆ MGTPRXP</li> <li>◆ MGTPRXN</li> <li>◆ MGTPTXP</li> <li>◆ MGPTXN</li> <li>B PUDC_B</li> <li>● ADOP/ADON- AD15P/AD15N</li> <li>⊕ VRN</li> <li>⊖ VRP</li> <li>⊗ VREF</li> <li>⊖ DOS</li> <li>● MRCC</li> <li>● SRCC</li> </ul>	<ul style="list-style-type: none"> <li>■ CFGBVS_0</li> <li>□ DONE_0</li> <li>■ DXP_0</li> <li>■ DXN_0</li> <li>■ GNDADC_0</li> <li>■ INIT_B_0</li> <li>■ PROGRAM_B_0</li> <li>■ TCK_0</li> <li>■ TD_L0</li> <li>■ TDO_0</li> <li>■ TMS_0</li> <li>■ VCCADC_0</li> <li>■ VCCBATT_0</li> <li>■ VP_0</li> <li>■ VN_0</li> <li>■ VREFP_0</li> <li>■ VREFN_0</li> </ul>	<ul style="list-style-type: none"> <li>■ GND</li> <li>■ VCCAUX_IO_G#</li> <li>■ VCCAUX</li> <li>■ VCCINT</li> <li>■ VCCO_#</li> <li>■ VCCBRAM</li> <li>■ VCCPINT</li> <li>■ VCCPAUX</li> <li>■ VCCO_MIO0</li> <li>■ VCCO_MIO1</li> <li>■ VCCO_DDR</li> <li>■ VCCPLL</li> <li>■ RSVDVCC[3:1]</li> <li>■ RSVDGND</li> <li>n NC</li> </ul>	<ul style="list-style-type: none"> <li>● PS_POP_B</li> <li>○ PS_CLK</li> <li>○ PS_SRST_B</li> <li>⊗ PS_MIO_VREF</li> <li>○ PS_MIO</li> </ul>	<ul style="list-style-type: none"> <li>○ PS_DDR_CKP</li> <li>○ PS_DDR_CKN</li> <li>● PS_DDR_CKE</li> <li>● PS_DDR_CS_B</li> <li>○ PS_DDR_RAS_B</li> <li>○ PS_DDR_CAS_B</li> <li>● PS_DDR_WE_B</li> <li>● PS_DDR_BA</li> <li>● PS_DDR_A</li> <li>○ PS_DDR_ODT</li> <li>○ PS_DDR_DRST_B</li> <li>● PS_DDR_DO</li> <li>● PS_DDR_DM</li> <li>● PS_DDR_DOS_P</li> <li>● PS_DDR_DOS_N</li> <li>○ PS_DDR_VRP</li> <li>● PS_DDR_VRN</li> <li>○ PS_DDR_VREF</li> </ul>

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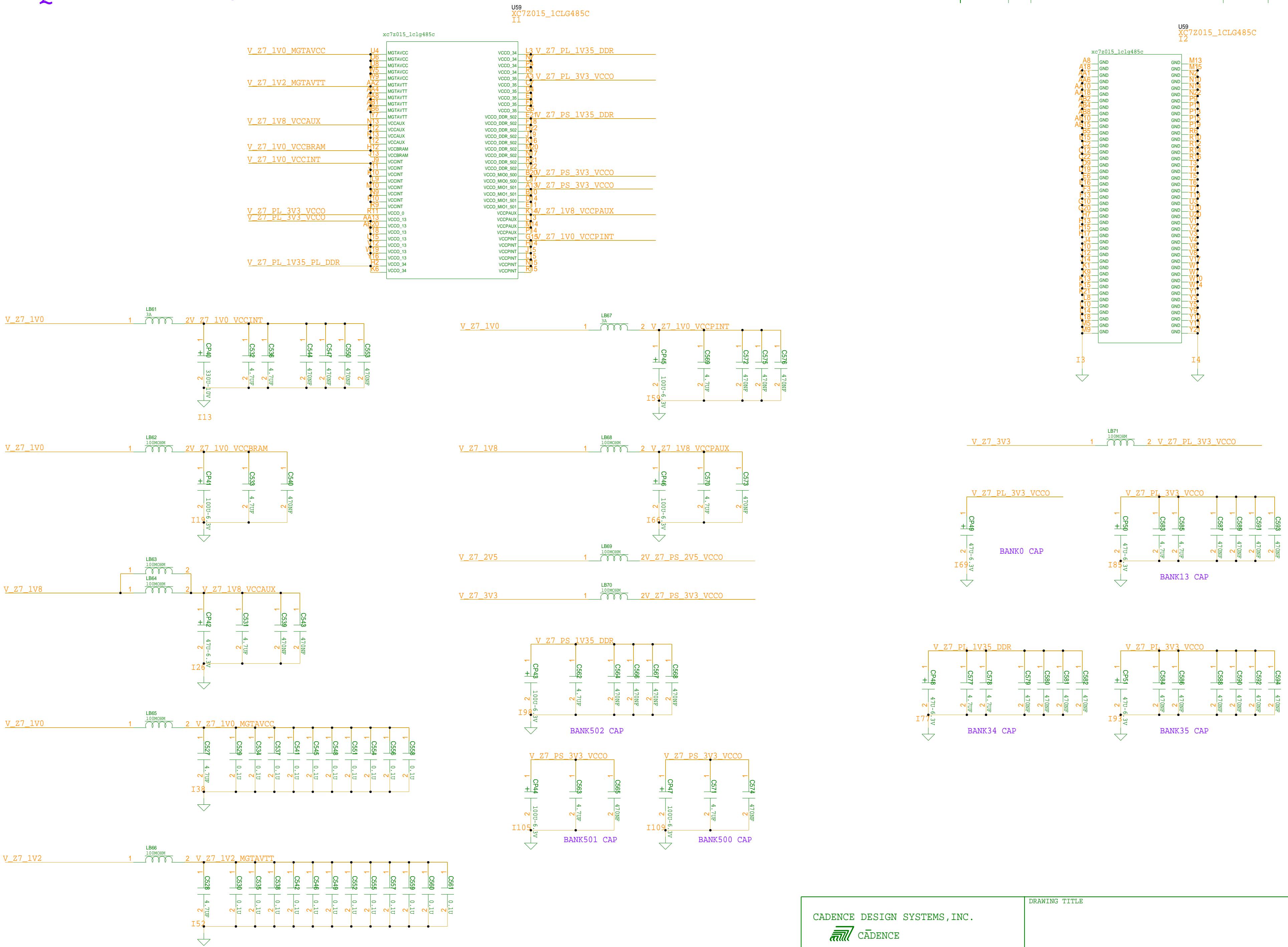
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ZYNQ-7 BANK POWER



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## REVISIONS

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## ZYNQ-7 CLOCK

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D

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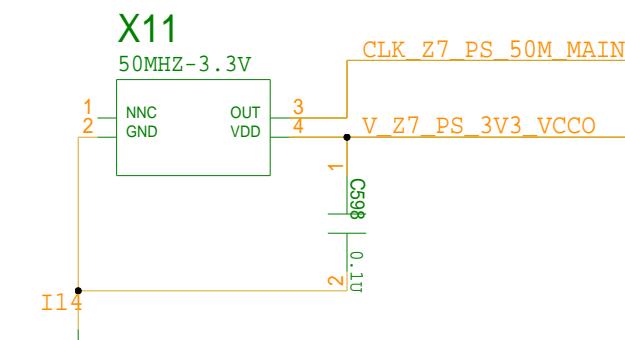
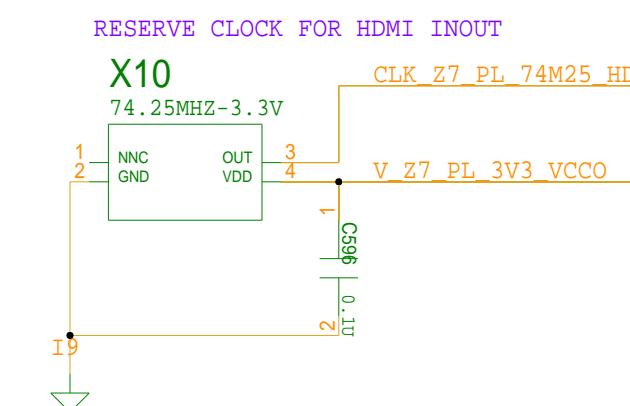
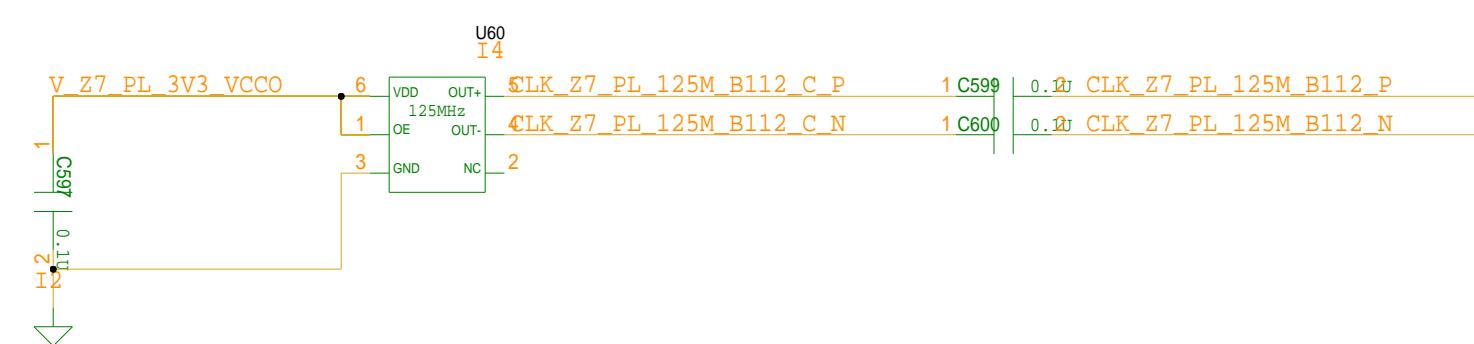
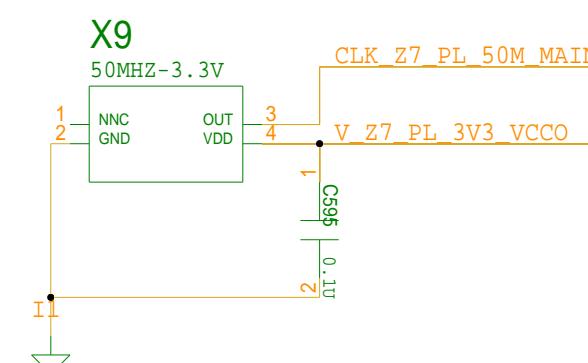
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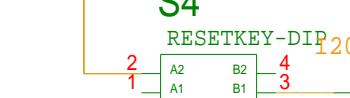
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Z7\_CONFIG\_CFBVS 2.7K R457 1 V\_Z7\_3V3\_VCCO

Z7\_CONFIG\_INIT\_B 2.7K R458 1 V\_Z7\_3V3\_VCCO

Z7\_CONFIG\_PROGRAM\_B 2.7K R461 1 V\_Z7\_3V3\_VCCO

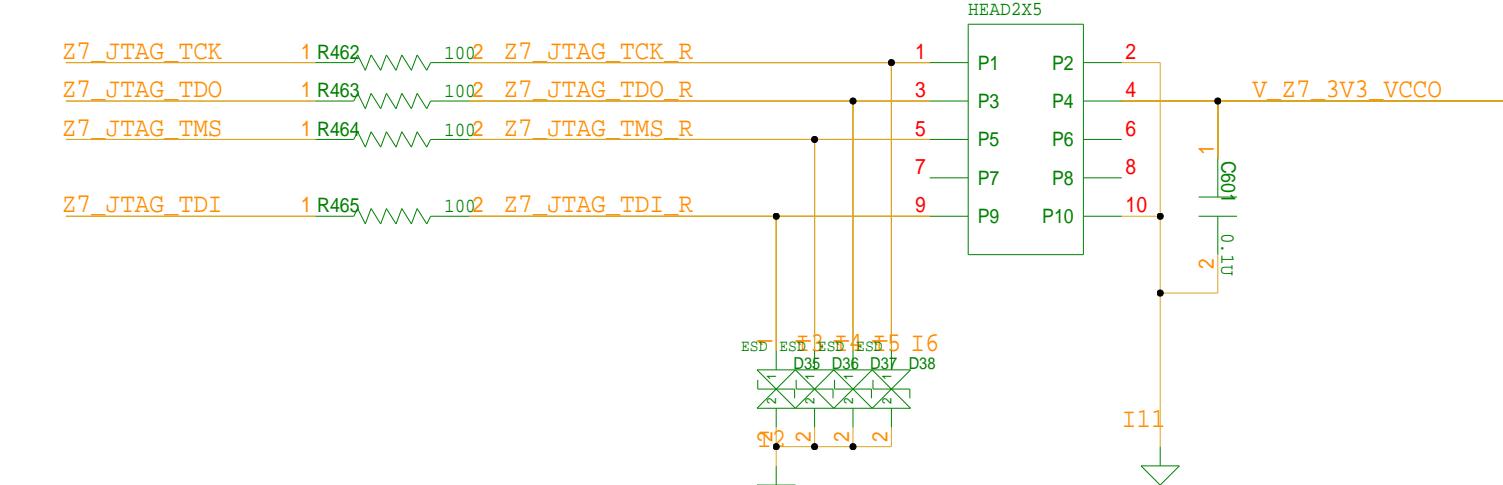
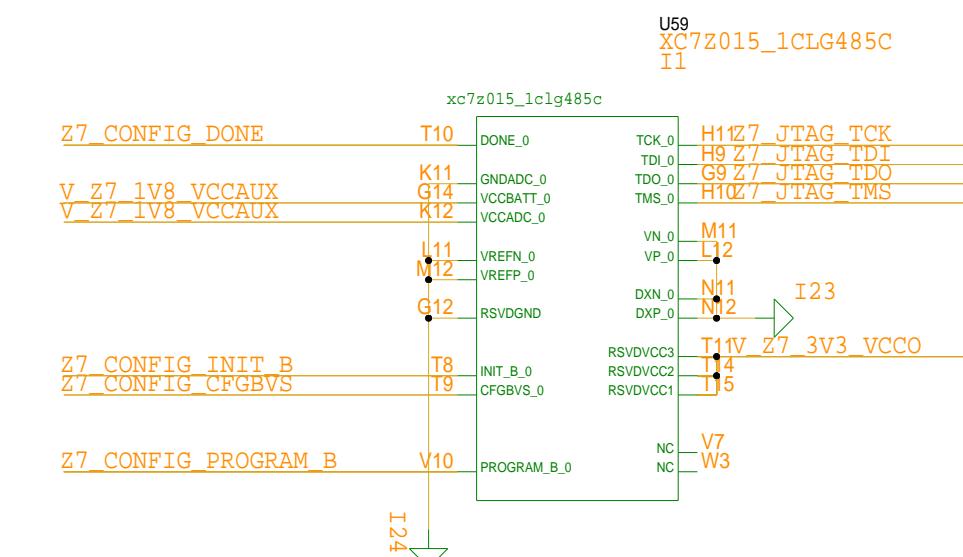


BUTTON FOR RECONFIG

Z7\_CONFIG\_DONE 1 R459 330 2 V\_Z7\_3V3\_VCCO

1 R460 100 2 1 D34 LED 2 I16

LED INDICATE CONFIG DONE



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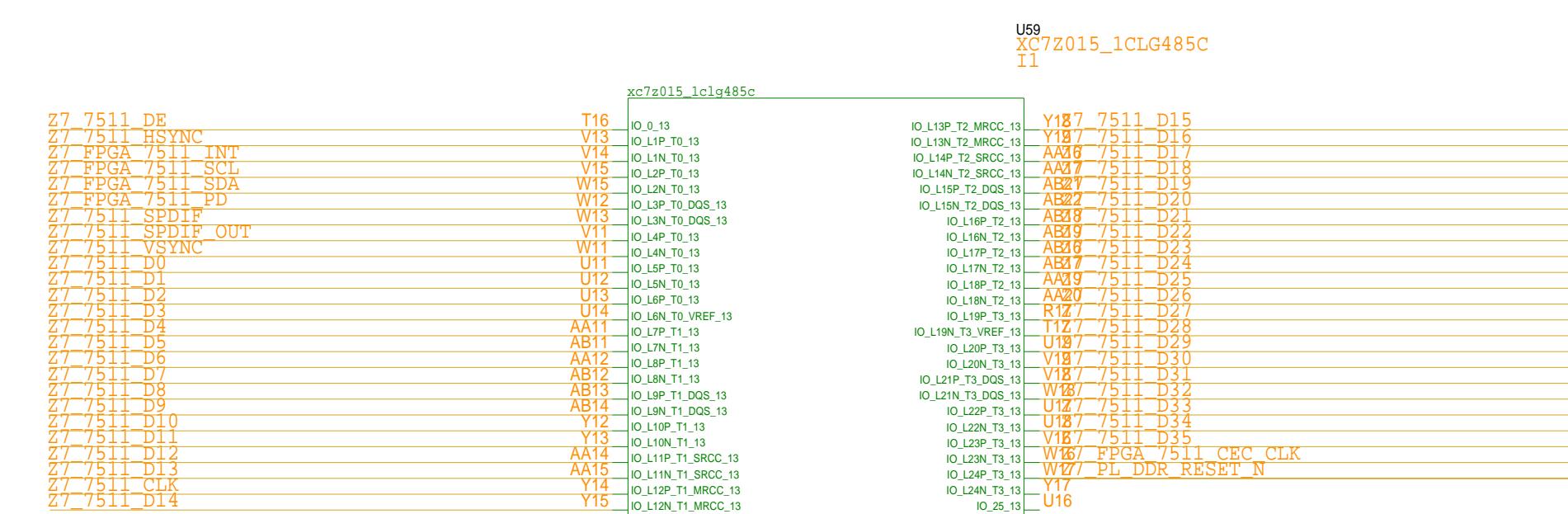
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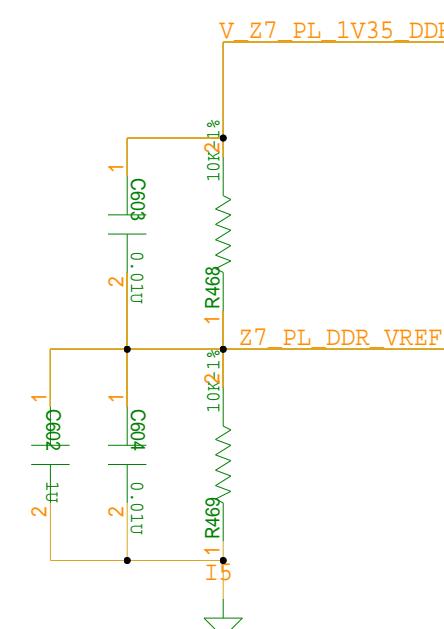
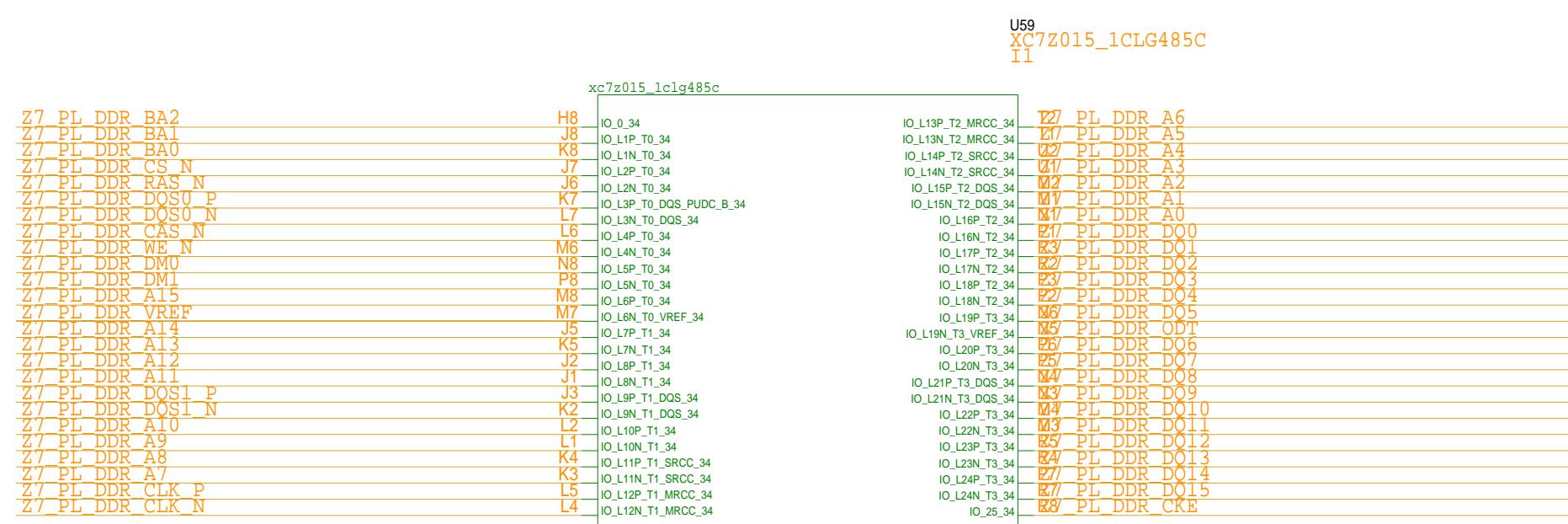
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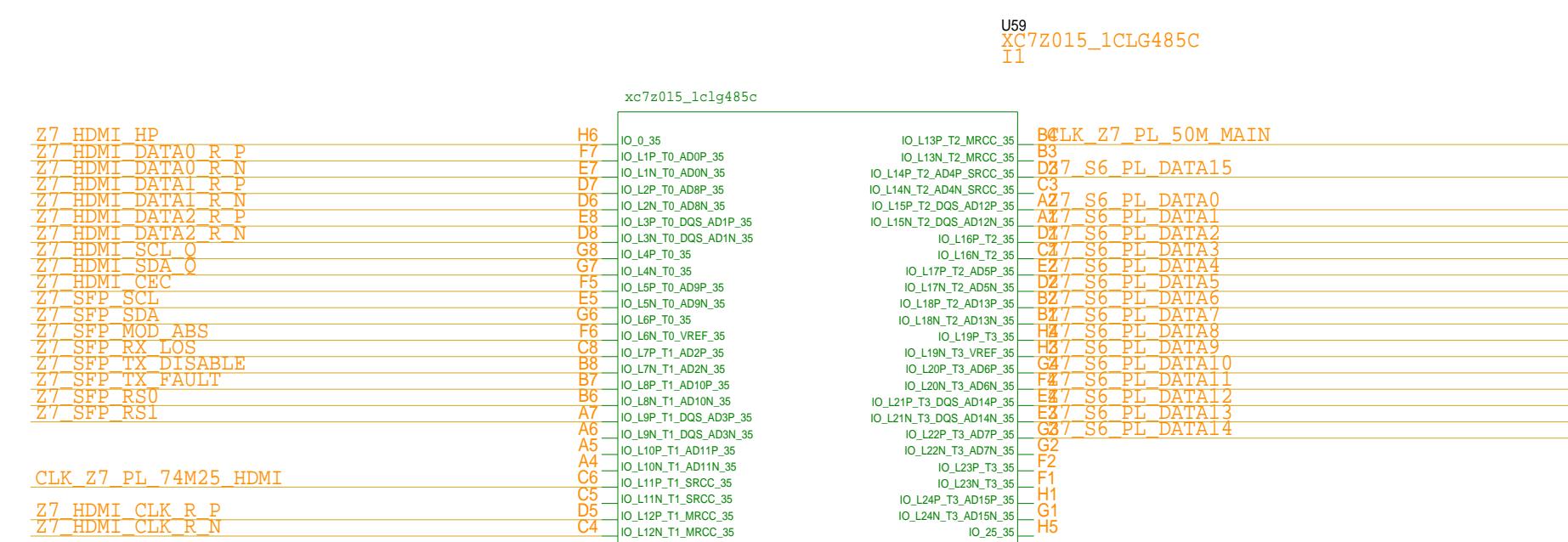
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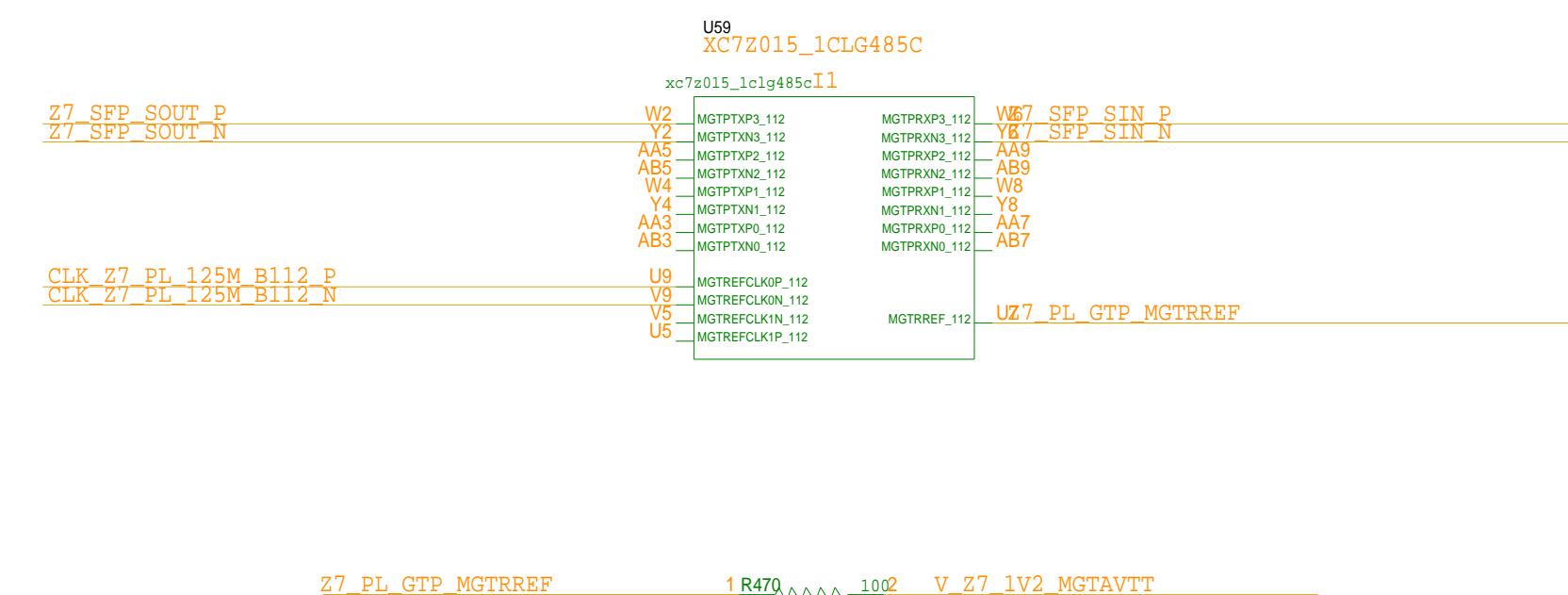
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# ZYNQ-7 PL BANK112

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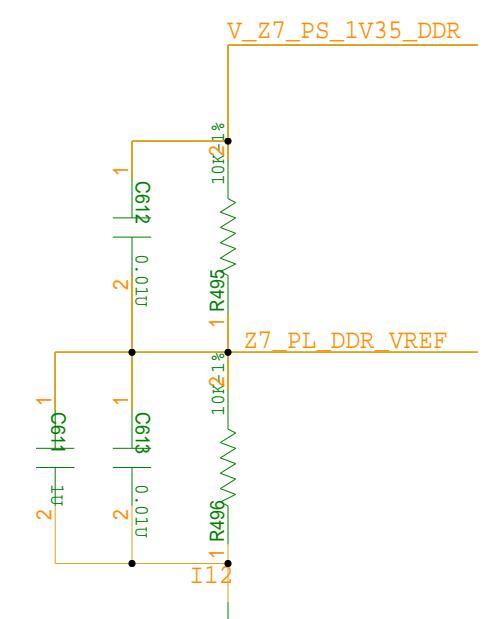
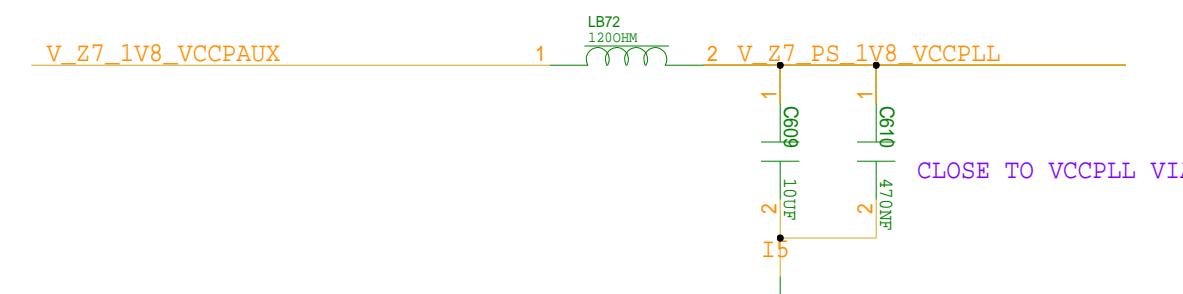
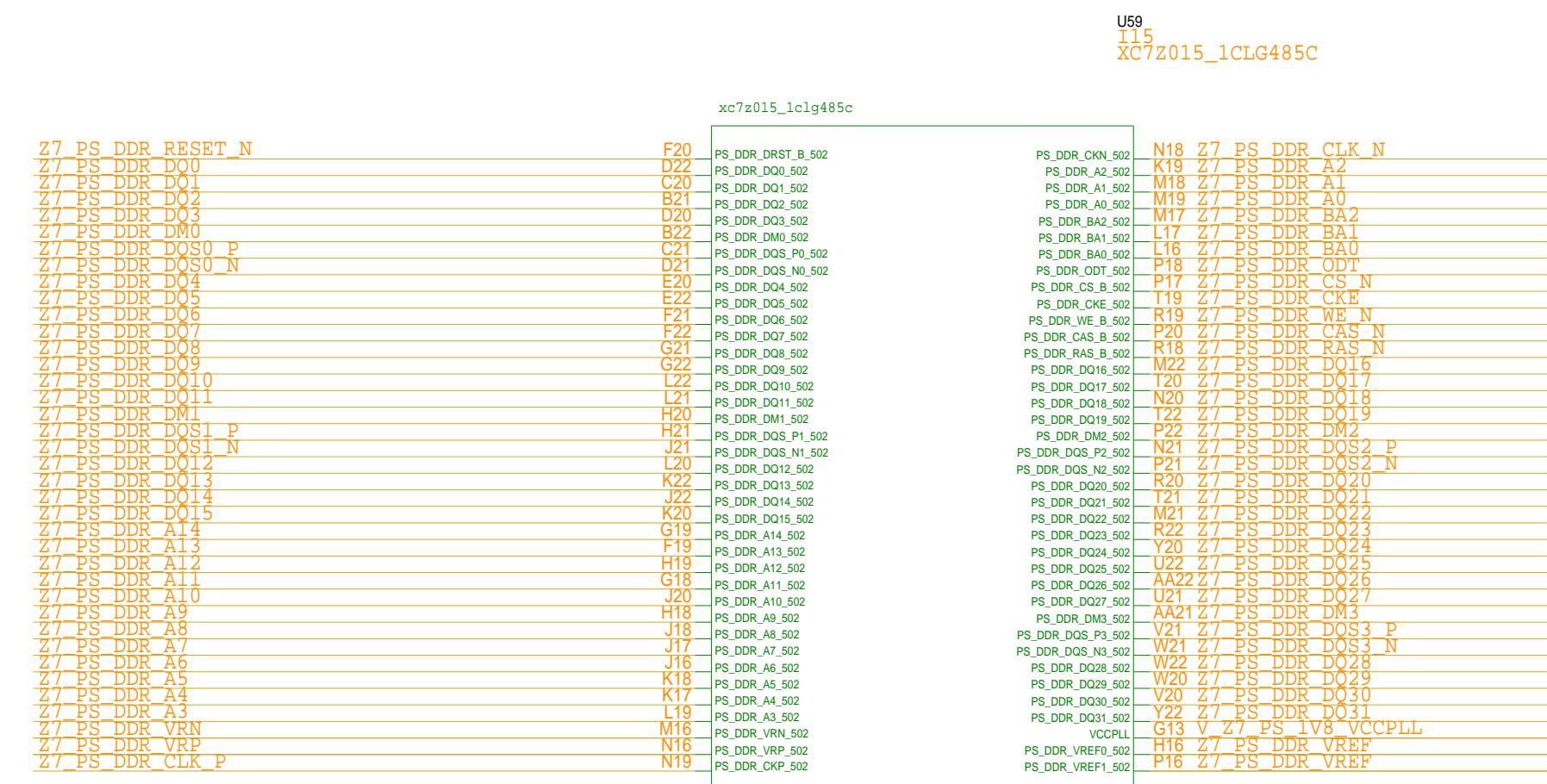
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# ZYNQ-7 PS BANK502

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