

## Introduction

Spartan®-7 FPGAs are available in -2, -1, and -1L speed grades, with -2 having the highest performance. The Spartan-7 FPGAs predominantly operate at a 1.0V core voltage. The -1L devices are screened for lower maximum static power and can operate at lower core voltages for lower dynamic power than the -1 devices. The -1L devices operate only at  $V_{CCINT} = V_{CCBRAM} = 0.95V$  and have the same speed specifications as the -1 speed grade.

Spartan-7 FPGA DC and AC characteristics are specified in commercial and industrial temperature ranges. Except the operating temperature range or unless otherwise noted, all the DC and AC electrical parameters are the same for a particular speed grade (that is, the timing characteristics of a -1I industrial speed grade device are the same as for a -1C commercial speed grade device). However, only selected speed grades and/or devices are available in each temperature range. For example, the -1L speed grade is only available in the industrial (I) temperature range.

All supply voltage and junction temperature specifications are representative of worst-case conditions. The parameters included are common to popular designs and typical applications.

Available device and package combinations can be found in the *7 Series FPGAs Overview* (DS180) [\[Ref 1\]](#).

This Spartan-7 FPGA data sheet, part of an overall set of documentation on the 7 series FPGAs, is available on the Xilinx website at [www.xilinx.com/documentation](http://www.xilinx.com/documentation).

## DC Characteristics

Table 1: Absolute Maximum Ratings<sup>(1)</sup>

Symbol	Description	Min	Max	Units
<b>FPGA Logic</b>				
$V_{CCINT}$	Internal supply voltage.	-0.5	1.1	V
$V_{CCAUX}$	Auxiliary supply voltage.	-0.5	2.0	V
$V_{CCBRAM}$	Supply voltage for the block RAM memories.	-0.5	1.1	V
$V_{CCO}$	Output drivers supply voltage for HR I/O banks.	-0.5	3.6	V
$V_{REF}$	Input reference voltage.	-0.5	2.0	V
$V_{IN}^{(2)(3)(4)}$	I/O input voltage.	-0.4	$V_{CCO} + 0.55$	V
	I/O input voltage (when $V_{CCO} = 3.3V$ ) for $V_{REF}$ and differential I/O standards except TMDS_33. <sup>(5)</sup>	-0.4	2.625	V
$V_{CCBATT}$	Key memory battery backup supply.	-0.5	2.0	V

Table 1: Absolute Maximum Ratings<sup>(1)</sup> (Cont'd)

Symbol	Description	Min	Max	Units
<b>XADC</b>				
V <sub>CCADC</sub>	XADC supply relative to GNDADC.	−0.5	2.0	V
V <sub>REFP</sub>	XADC reference input relative to GNDADC.	−0.5	2.0	V
<b>Temperature</b>				
T <sub>STG</sub>	Storage temperature (ambient).	−65	150	°C
T <sub>SOL</sub>	Maximum soldering temperature for Pb/Sn component bodies. <sup>(6)</sup>	–	+220	°C
	Maximum soldering temperature for Pb-free component bodies. <sup>(6)</sup>	–	+260	°C
T <sub>j</sub>	Maximum junction temperature. <sup>(6)</sup>	–	+125	°C

**Notes:**

- Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.
- The lower absolute voltage specification always applies.
- For I/O operation, refer to the *7 Series FPGAs SelectIO Resources User Guide* (UG471) [Ref 2].
- The maximum limit applies to DC signals. For maximum undershoot and overshoot AC specifications, see Table 4.
- See Table 9 for TMD5\_33 specifications.
- For soldering guidelines and thermal considerations, see the *7 Series FPGA Packaging and Pinout Specification* (UG475) [Ref 3].

Table 2: Recommended Operating Conditions<sup>(1)(2)</sup>

Symbol	Description	Min	Typ	Max	Units
<b>FPGA Logic</b>					
$V_{CCINT}^{(3)}$	For -2 and -1 (1.0V) devices: internal supply voltage.	0.95	1.00	1.05	V
	For -1L (0.95V) devices: internal supply voltage.	0.92	0.95	0.98	V
$V_{CCAUX}$	Auxiliary supply voltage.	1.71	1.80	1.89	V
$V_{CCBRAM}^{(3)}$	For -2 and -1 (1.0V) devices: block RAM supply voltage.	0.95	1.00	1.05	V
	For -1L (0.95V) devices: block RAM supply voltage.	0.92	0.95	0.98	V
$V_{CCO}^{(4)(5)}$	Supply voltage for HR I/O banks.	1.14	–	3.465	V
$V_{IN}^{(6)}$	I/O input voltage.	–0.20	–	$V_{CCO} + 0.20$	V
	I/O input voltage (when $V_{CCO} = 3.3V$ ) for $V_{REF}$ and differential I/O standards except TMDS_33. <sup>(7)</sup>	–0.20	–	2.625	V
$I_{IN}^{(8)}$	Maximum current through any pin in a powered or unpowered bank when forward biasing the clamp diode.	–	–	10	mA
$V_{CCBATT}^{(9)}$	Battery voltage.	1.0	–	1.89	V
<b>XADC</b>					
$V_{CCADC}$	XADC supply relative to GNDADC.	1.71	1.80	1.89	V
$V_{REFP}$	Externally supplied reference voltage.	1.20	1.25	1.30	V
<b>Temperature</b>					
$T_j$	Junction temperature operating range for commercial (C) temperature devices.	0	–	85	°C
	Junction temperature operating range for industrial (I) temperature devices.	–40	–	100	°C

**Notes:**

- All voltages are relative to ground.
- For the design of the power distribution system consult the [7 Series FPGAs PCB Design Guide \(UG483\)](#) [Ref 4].
- If  $V_{CCINT}$  and  $V_{CCBRAM}$  are operating at the same voltage,  $V_{CCINT}$  and  $V_{CCBRAM}$  should be connected to the same supply.
- Configuration data is retained even if  $V_{CCO}$  drops to 0V.
- Includes  $V_{CCO}$  of 1.2V, 1.35V, 1.5V, 1.8V, 2.5V, and 3.3V at  $\pm 5\%$ .
- The lower absolute voltage specification always applies.
- See [Table 9](#) for TMDS\_33 specifications.
- A total of 200 mA per bank should not be exceeded.
- $V_{CCBATT}$  is required only when using bitstream encryption. If battery is not used, connect  $V_{CCBATT}$  to either ground or  $V_{CCAUX}$ .

Table 3: DC Characteristics Over Recommended Operating Conditions

Symbol	Description	Min	Typ <sup>(1)</sup>	Max	Units
$V_{DRINT}$	Data retention $V_{CCINT}$ voltage (below which configuration data might be lost).	0.75	–	–	V
$V_{DRI}$	Data retention $V_{CCAUX}$ voltage (below which configuration data might be lost).	1.5	–	–	V
$I_{REF}$	$V_{REF}$ leakage current per pin.	–	–	15	$\mu A$
$I_L$	Input or output leakage current per pin (sample-tested).	–	–	15	$\mu A$
$C_{IN}^{(2)}$	Die input capacitance at the pad.	–	–	8	pF
$I_{RPU}$	Pad pull-up (when selected) at $V_{IN} = 0V$ , $V_{CCO} = 3.3V$ .	90	–	330	$\mu A$
	Pad pull-up (when selected) at $V_{IN} = 0V$ , $V_{CCO} = 2.5V$ .	68	–	250	$\mu A$
	Pad pull-up (when selected) at $V_{IN} = 0V$ , $V_{CCO} = 1.8V$ .	34	–	220	$\mu A$
	Pad pull-up (when selected) at $V_{IN} = 0V$ , $V_{CCO} = 1.5V$ .	23	–	150	$\mu A$
	Pad pull-up (when selected) at $V_{IN} = 0V$ , $V_{CCO} = 1.2V$ .	12	–	120	$\mu A$
$I_{RPD}$	Pad pull-down (when selected) at $V_{IN} = 3.3V$ .	68	–	330	$\mu A$
$I_{CCADC}$	Analog supply current, analog circuits in powered up state.	–	–	25	mA
$I_{BATT}^{(3)}$	Battery supply current.	–	–	150	nA
$R_{IN\_TERM}^{(4)}$	Thevenin equivalent resistance of programmable input termination to $V_{CCO}/2$ (UNTUNED_SPLIT_40).	28	40	55	$\Omega$
	Thevenin equivalent resistance of programmable input termination to $V_{CCO}/2$ (UNTUNED_SPLIT_50).	35	50	65	$\Omega$
	Thevenin equivalent resistance of programmable input termination to $V_{CCO}/2$ (UNTUNED_SPLIT_60).	44	60	83	$\Omega$
$n$	Temperature diode ideality factor.	–	1.010	–	–
$r$	Temperature diode series resistance.	–	2	–	$\Omega$

**Notes:**

1. Typical values are specified at nominal voltage, 25°C.
2. This measurement represents the die capacitance at the pad, not including the package.
3. Maximum value specified for worst case process at 25°C.
4. Termination resistance to a  $V_{CCO}/2$  level.

Table 4:  $V_{IN}$  Maximum Allowed AC Voltage Overshoot and Undershoot for HR I/O Banks<sup>(1)(2)</sup>

AC Voltage Overshoot	% of UI at –40°C to 100°C	AC Voltage Undershoot	% of UI at –40°C to 100°C
$V_{CCO} + 0.55$	100	–0.40	100
		–0.45	61.7
		–0.50	25.8
		–0.55	11.0
$V_{CCO} + 0.60$	46.6	–0.60	4.77
$V_{CCO} + 0.65$	21.2	–0.65	2.10
$V_{CCO} + 0.70$	9.75	–0.70	0.94
$V_{CCO} + 0.75$	4.55	–0.75	0.43
$V_{CCO} + 0.80$	2.15	–0.80	0.20
$V_{CCO} + 0.85$	1.02	–0.85	0.09
$V_{CCO} + 0.90$	0.49	–0.90	0.04
$V_{CCO} + 0.95$	0.24	–0.95	0.02

**Notes:**

1. A total of 200 mA per bank should not be exceeded.
2. The peak voltage of the overshoot or undershoot, and the duration above  $V_{CCO} + 0.20V$  or below  $GND - 0.20V$ , must not exceed the values in this table.

Table 5: Typical Quiescent Supply Current<sup>(1)(2)(3)</sup>

Symbol	Description	Device	Speed Grade			Units
			1.0V		0.95V	
			–2C/–2I	–1C/–1I	–1LI	
$I_{CCINTQ}$	Quiescent $V_{CCINT}$ supply current.	XC7S6				mA
		XC7S15				mA
		XC7S25	48	48	43	mA
		XC7S50	95	95	58	mA
		XC7S75				mA
		XC7S100				mA
$I_{CCOQ}$	Quiescent $V_{CCO}$ supply current.	XC7S6				mA
		XC7S15				mA
		XC7S25	1	1	1	mA
		XC7S50	1	1	1	mA
		XC7S75				mA
		XC7S100				mA
$I_{CCAUXQ}$	Quiescent $V_{CCAUX}$ supply current.	XC7S6				mA
		XC7S15				mA
		XC7S25	14	14	14	mA
		XC7S50	22	22	19	mA
		XC7S75				mA
		XC7S100				mA

Table 5: Typical Quiescent Supply Current<sup>(1)(2)(3)</sup> (Cont'd)

Symbol	Description	Device	Speed Grade			Units
			1.0V		0.95V	
			-2C/-2I	-1C/-1I	-1LI	
$I_{CCBRAMQ}$	Quiescent $V_{CCBRAM}$ supply current.	XC7S6				mA
		XC7S15				mA
		XC7S25	2	2	1	mA
		XC7S50	2	2	1	mA
		XC7S75				mA
		XC7S100				mA

**Notes:**

1. Typical values are specified at nominal voltage, 85°C junction temperature ( $T_j$ ) with single-ended SelectIO™ resources.
2. Typical values are for blank configured devices with no output current loads, no active input pull-up resistors, all I/O pins are 3-state and floating.
3. Use the *Xilinx Power Estimator* spreadsheet tool [Ref 5] to estimate static power consumption for conditions other than those specified.

## Power-On/Off Power Supply Sequencing

The recommended power-on sequence is  $V_{CCINT}$ ,  $V_{CCBRAM}$ ,  $V_{CCAUX}$ , and  $V_{CCO}$  to achieve minimum current draw and ensure that the I/Os are 3-stated at power-on. The recommended power-off sequence is the reverse of the power-on sequence. If  $V_{CCINT}$  and  $V_{CCBRAM}$  have the same recommended voltage levels then both can be powered by the same supply and ramped simultaneously. If  $V_{CCAUX}$  and  $V_{CCO}$  have the same recommended voltage levels then both can be powered by the same supply and ramped simultaneously.

For  $V_{CCO}$  voltages of 3.3V in HR I/O banks and configuration bank 0 the following conditions apply.

- The voltage difference between  $V_{CCO}$  and  $V_{CCAUX}$  must not exceed 2.625V for longer than  $T_{VCCO2VCCAUX}$  for each power-on/off cycle to maintain device reliability levels.
- The  $T_{VCCO2VCCAUX}$  time can be allocated in any percentage between the power-on and power-off ramps.

There is no recommended sequence for supplies not discussed in this section.

Table 6 shows the minimum current, in addition to  $I_{CCQ}$  maximum, that is required by Spartan-7 devices for proper power-on and configuration. If the current minimums shown in Table 6 are met, the device powers on after all four supplies have passed through their power-on reset threshold voltages. The FPGA must not be configured until after  $V_{CCINT}$  is applied. Once initialized and configured, use the *Xilinx Power Estimator* spreadsheet tool [Ref 5] to estimate current drain on these supplies.

Table 6: Power-On Current for Spartan-7 Devices

Device	$I_{CCINTMIN}$	$I_{CCAUXMIN}$	$I_{CCOMIN}$	$I_{CCBRAMMIN}$	Units
XC7S6	$I_{CCINTQ} + 120$	$I_{CCAUXQ} + 40$	$I_{CCOQ} + 40$ mA per bank	$I_{CCBRAMQ} + 60$	mA
XC7S15	$I_{CCINTQ} + 120$	$I_{CCAUXQ} + 40$	$I_{CCOQ} + 40$ mA per bank	$I_{CCBRAMQ} + 60$	mA
XC7S25	$I_{CCINTQ} + 120$	$I_{CCAUXQ} + 40$	$I_{CCOQ} + 40$ mA per bank	$I_{CCBRAMQ} + 60$	mA
XC7S50	$I_{CCINTQ} + 120$	$I_{CCAUXQ} + 40$	$I_{CCOQ} + 40$ mA per bank	$I_{CCBRAMQ} + 60$	mA
XC7S75	$I_{CCINTQ} + 170$	$I_{CCAUXQ} + 40$	$I_{CCOQ} + 40$ mA per bank	$I_{CCBRAMQ} + 60$	mA
XC7S100	$I_{CCINTQ} + 170$	$I_{CCAUXQ} + 40$	$I_{CCOQ} + 40$ mA per bank	$I_{CCBRAMQ} + 60$	mA

Table 7: Power Supply Ramp Time

Symbol	Description	Conditions	Min	Max	Units
$T_{VCCINT}$	Ramp time from GND to 90% of $V_{CCINT}$ .		0.2	50	ms
$T_{VCCO}$	Ramp time from GND to 90% of $V_{CCO}$ .		0.2	50	ms
$T_{VCCAUX}$	Ramp time from GND to 90% of $V_{CCAUX}$ .		0.2	50	ms
$T_{VCCBRAM}$	Ramp time from GND to 90% of $V_{CCBRAM}$ .		0.2	50	ms
$T_{VCCO2VCCAUX}$	Allowed time per power cycle for $V_{CCO} - V_{CCAUX} > 2.625V$ .	$T_J = 125^{\circ}C^{(1)}$	–	300	ms
		$T_J = 100^{\circ}C^{(1)}$	–	500	ms
		$T_J = 85^{\circ}C^{(1)}$	–	800	ms

**Notes:**

- Based on 240,000 power cycles with a nominal  $V_{CCO}$  of 3.3V or 36,500 power cycles with a worst case  $V_{CCO}$  of 3.465V.

## DC Input and Output Levels

Values for  $V_{IL}$  and  $V_{IH}$  are recommended input voltages. Values for  $I_{OL}$  and  $I_{OH}$  are guaranteed over the recommended operating conditions at the  $V_{OL}$  and  $V_{OH}$  test points. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at a minimum  $V_{CCO}$  with the respective  $V_{OL}$  and  $V_{OH}$  voltage levels shown. Other standards are sample tested.

Table 8: SelectIO DC Input and Output Levels<sup>(1)(2)(3)</sup>

I/O Standard	$V_{IL}$		$V_{IH}$		$V_{OL}$	$V_{OH}$	$I_{OL}$	$I_{OH}$
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA, Max	mA, Min
HSTL_I	-0.300	$V_{REF} - 0.100$	$V_{REF} + 0.100$	$V_{CCO} + 0.300$	0.400	$V_{CCO} - 0.400$	8.00	-8.00
HSTL_I_18	-0.300	$V_{REF} - 0.100$	$V_{REF} + 0.100$	$V_{CCO} + 0.300$	0.400	$V_{CCO} - 0.400$	8.00	-8.00
HSTL_II	-0.300	$V_{REF} - 0.100$	$V_{REF} + 0.100$	$V_{CCO} + 0.300$	0.400	$V_{CCO} - 0.400$	16.00	-16.00
HSTL_II_18	-0.300	$V_{REF} - 0.100$	$V_{REF} + 0.100$	$V_{CCO} + 0.300$	0.400	$V_{CCO} - 0.400$	16.00	-16.00
HSUL_12	-0.300	$V_{REF} - 0.130$	$V_{REF} + 0.130$	$V_{CCO} + 0.300$	20% $V_{CCO}$	80% $V_{CCO}$	0.10	-0.10
LVC MOS12	-0.300	35% $V_{CCO}$	65% $V_{CCO}$	$V_{CCO} + 0.300$	0.400	$V_{CCO} - 0.400$	Note 4	Note 4
LVC MOS15	-0.300	35% $V_{CCO}$	65% $V_{CCO}$	$V_{CCO} + 0.300$	25% $V_{CCO}$	75% $V_{CCO}$	Note 5	Note 5
LVC MOS18	-0.300	35% $V_{CCO}$	65% $V_{CCO}$	$V_{CCO} + 0.300$	0.450	$V_{CCO} - 0.450$	Note 6	Note 6
LVC MOS25	-0.300	0.7	1.700	$V_{CCO} + 0.300$	0.400	$V_{CCO} - 0.400$	Note 5	Note 5
LVC MOS33	-0.300	0.8	2.000	3.450	0.400	$V_{CCO} - 0.400$	Note 5	Note 5
LV TTL	-0.300	0.8	2.000	3.450	0.400	2.400	Note 6	Note 6
MOBILE_DDR	-0.300	20% $V_{CCO}$	80% $V_{CCO}$	$V_{CCO} + 0.300$	10% $V_{CCO}$	90% $V_{CCO}$	0.10	-0.10
PCI33_3	-0.400	30% $V_{CCO}$	50% $V_{CCO}$	$V_{CCO} + 0.500$	10% $V_{CCO}$	90% $V_{CCO}$	1.50	-0.50
SSTL135	-0.300	$V_{REF} - 0.090$	$V_{REF} + 0.090$	$V_{CCO} + 0.300$	$V_{CCO}/2 - 0.150$	$V_{CCO}/2 + 0.150$	13.00	-13.00
SSTL135_R	-0.300	$V_{REF} - 0.090$	$V_{REF} + 0.090$	$V_{CCO} + 0.300$	$V_{CCO}/2 - 0.150$	$V_{CCO}/2 + 0.150$	8.90	-8.90
SSTL15	-0.300	$V_{REF} - 0.100$	$V_{REF} + 0.100$	$V_{CCO} + 0.300$	$V_{CCO}/2 - 0.175$	$V_{CCO}/2 + 0.175$	13.00	-13.00
SSTL15_R	-0.300	$V_{REF} - 0.100$	$V_{REF} + 0.100$	$V_{CCO} + 0.300$	$V_{CCO}/2 - 0.175$	$V_{CCO}/2 + 0.175$	8.90	-8.90
SSTL18_I	-0.300	$V_{REF} - 0.125$	$V_{REF} + 0.125$	$V_{CCO} + 0.300$	$V_{CCO}/2 - 0.470$	$V_{CCO}/2 + 0.470$	8.00	-8.00
SSTL18_II	-0.300	$V_{REF} - 0.125$	$V_{REF} + 0.125$	$V_{CCO} + 0.300$	$V_{CCO}/2 - 0.600$	$V_{CCO}/2 + 0.600$	13.40	-13.40

### Notes:

1. Tested according to relevant specifications.
2. 3.3V and 2.5V standards are only supported in HR I/O banks.
3. For detailed interface specific DC voltage levels, see the *7 Series FPGAs SelectIO Resources User Guide* (UG471) [Ref 2].
4. Supported drive strengths of 4, 8, or 12 mA in HR I/O banks.
5. Supported drive strengths of 4, 8, 12, or 16 mA in HR I/O banks.
6. Supported drive strengths of 4, 8, 12, 16, or 24 mA in HR I/O banks.



Table 9: Differential SelectIO DC Input and Output Levels

I/O Standard	$V_{ICM}^{(1)}$			$V_{ID}^{(2)}$			$V_{OCM}^{(3)}$			$V_{OD}^{(4)}$		
	V, Min	V, Typ	V, Max	V, Min	V, Typ	V, Max	V, Min	V, Typ	V, Max	V, Min	V, Typ	V, Max
BLVDS_25	0.300	1.200	1.425	0.100	–	–	–	1.250	–	Note 5		
MINI_LVDS_25	0.300	1.200	$V_{CCAUX}$	0.200	0.400	0.600	1.000	1.200	1.400	0.300	0.450	0.600
PPDS_25	0.200	0.900	$V_{CCAUX}$	0.100	0.250	0.400	0.500	0.950	1.400	0.100	0.250	0.400
RSDS_25	0.300	0.900	1.500	0.100	0.350	0.600	1.000	1.200	1.400	0.100	0.350	0.600
TMDS_33	2.700	2.965	3.230	0.150	0.675	1.200	$V_{CCO} - 0.405$	$V_{CCO} - 0.300$	$V_{CCO} - 0.190$	0.400	0.600	0.800

**Notes:**

- $V_{ICM}$  is the input common mode voltage.
- $V_{ID}$  is the input differential voltage ( $Q - \overline{Q}$ ).
- $V_{OCM}$  is the output common mode voltage.
- $V_{OD}$  is the output differential voltage ( $Q - \overline{Q}$ ).
- $V_{OD}$  for BLVDS will vary significantly depending on topology and loading.

Table 10: Complementary Differential SelectIO DC Input and Output Levels

I/O Standard	$V_{ICM}^{(1)}$			$V_{ID}^{(2)}$		$V_{OL}^{(3)}$	$V_{OH}^{(4)}$	$I_{OL}$	$I_{OH}$
	V, Min	V, Typ	V, Max	V, Min	V, Max	V, Max	V, Min	mA, Max	mA, Min
DIFF_HSTL_I	0.300	0.750	1.125	0.100	–	0.400	$V_{CCO} - 0.400$	8.00	–8.00
DIFF_HSTL_I_18	0.300	0.900	1.425	0.100	–	0.400	$V_{CCO} - 0.400$	8.00	–8.00
DIFF_HSTL_II	0.300	0.750	1.125	0.100	–	0.400	$V_{CCO} - 0.400$	16.00	–16.00
DIFF_HSTL_II_18	0.300	0.900	1.425	0.100	–	0.400	$V_{CCO} - 0.400$	16.00	–16.00
DIFF_HSUL_12	0.300	0.600	0.850	0.100	–	20% $V_{CCO}$	80% $V_{CCO}$	0.100	–0.100
DIFF_MOBILE_DDR	0.300	0.900	1.425	0.100	–	10% $V_{CCO}$	90% $V_{CCO}$	0.100	–0.100
DIFF_SSTL135	0.300	0.675	1.000	0.100	–	$(V_{CCO}/2) - 0.150$	$(V_{CCO}/2) + 0.150$	13.0	–13.0
DIFF_SSTL135_R	0.300	0.675	1.000	0.100	–	$(V_{CCO}/2) - 0.150$	$(V_{CCO}/2) + 0.150$	8.9	–8.9
DIFF_SSTL15	0.300	0.750	1.125	0.100	–	$(V_{CCO}/2) - 0.175$	$(V_{CCO}/2) + 0.175$	13.0	–13.0
DIFF_SSTL15_R	0.300	0.750	1.125	0.100	–	$(V_{CCO}/2) - 0.175$	$(V_{CCO}/2) + 0.175$	8.9	–8.9
DIFF_SSTL18_I	0.300	0.900	1.425	0.100	–	$(V_{CCO}/2) - 0.470$	$(V_{CCO}/2) + 0.470$	8.00	–8.00
DIFF_SSTL18_II	0.300	0.900	1.425	0.100	–	$(V_{CCO}/2) - 0.600$	$(V_{CCO}/2) + 0.600$	13.4	–13.4

**Notes:**

- $V_{ICM}$  is the input common mode voltage.
- $V_{ID}$  is the input differential voltage ( $Q - \overline{Q}$ ).
- $V_{OL}$  is the single-ended low-output voltage.
- $V_{OH}$  is the single-ended high-output voltage.

## LVDS DC Specifications (LVDS\_25)

Table 11: LVDS\_25 DC Specifications<sup>(1)</sup>

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
$V_{CCO}$	Supply voltage.		2.375	2.500	2.625	V
$V_{OH}$	Output High voltage for Q and $\overline{Q}$ .	$R_T = 100\Omega$ across Q and $\overline{Q}$ signals.	–	–	1.675	V
$V_{OL}$	Output Low voltage for Q and $\overline{Q}$ .	$R_T = 100\Omega$ across Q and $\overline{Q}$ signals.	0.700	–	–	V
$V_{ODIFF}$	Differential output voltage: (Q – $\overline{Q}$ ), Q = High ( $\overline{Q}$ – Q), $\overline{Q}$ = High	$R_T = 100\Omega$ across Q and $\overline{Q}$ signals.	247	350	600	mV
$V_{OCM}$	Output common-mode voltage.	$R_T = 100\Omega$ across Q and $\overline{Q}$ signals.	1.000	1.250	1.425	V
$V_{IDIFF}$	Differential input voltage: (Q – $\overline{Q}$ ), Q = High ( $\overline{Q}$ – Q), $\overline{Q}$ = High		100	350	600	mV
$V_{ICM}$	Input common-mode voltage.		0.300	1.200	1.500	V

### Notes:

1. Differential inputs for LVDS\_25 can be placed in banks with  $V_{CCO}$  levels that are different from the required level for outputs. Consult the *7 Series FPGAs SelectIO Resources User Guide* (UG471) [Ref 2] for more information.

## AC Switching Characteristics

All values represented in this data sheet are based on the speed specifications from the Vivado® Design Suite as outlined in [Table 12](#).

**Table 12: Speed Specification Version By Device**

2017.2	Device
1.17	XC7S6, XC7S15, XC7S25, XC7S50, XC7S75, XC7S100

Switching characteristics are specified on a per-speed-grade basis and can be designated as Advance, Preliminary, or Production. Each designation is defined as follows.

### Advance Product Specification

These specifications are based on simulations only and are typically available soon after device design specifications are frozen. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur.

### Preliminary Product Specification

These specifications are based on complete ES (engineering sample) silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting delays is greatly reduced as compared to Advance data.

### Production Product Specification

These specifications are released once enough production silicon of a particular device family member has been characterized to provide full correlation between specifications and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to Production before faster speed grades.

## Testing of AC Switching Characteristics

Internal timing parameters are derived from measuring internal test patterns. All AC switching characteristics are representative of worst-case supply voltage and junction temperature conditions.

For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer and back-annotate to the simulation net list. Unless otherwise noted, values apply to all Spartan-7 FPGAs.

## Speed Grade Designations

Since individual family members are produced at different times, the migration from one category to another depends completely on the status of the fabrication process for each device. [Table 13](#) correlates the current status of each Spartan-7 device on a per speed grade basis.

**Table 13: Spartan-7 Device Speed Grade Designations**

Device	Speed Grade, Temperature Range, and $V_{CCINT}$ Operating Voltage		
	Advance	Preliminary	Production
XC7S6	-2C (1.0V), -2I (1.0V), -1C (1.0V), -1I (1.0V), and -1LI (0.95V) <sup>(1)</sup>		
XC7S15	-2C (1.0V), -2I (1.0V), -1C (1.0V), -1I (1.0V), and -1LI (0.95V) <sup>(1)</sup>		
XC7S25	-2C (1.0V), -2I (1.0V), -1C (1.0V), -1I (1.0V), and -1LI (0.95V) <sup>(1)</sup>		
XC7S50			-2C (1.0V), -2I (1.0V), -1C (1.0V), -1I (1.0V), and -1LI (0.95V) <sup>(1)</sup>
XC7S75	-2C (1.0V), -2I (1.0V), -1C (1.0V), -1I (1.0V), and -1LI (0.95V) <sup>(1)</sup>		
XC7S100	-2C (1.0V), -2I (1.0V), -1C (1.0V), -1I (1.0V), and -1LI (0.95V) <sup>(1)</sup>		

**Notes:**

1. The lowest power -1LI devices, where  $V_{CCINT} = 0.95V$ , are listed in the Vivado Design Suite as -1LI.

## Production Silicon and Software Status

In some cases, a particular family member (and speed grade) is released to production before a speed specification is released with the correct label (Advance, Preliminary, Production). Any labeling discrepancies are corrected in subsequent speed specification releases.

[Table 14](#) lists the production released Spartan-7 device, speed grade, and the minimum corresponding supported speed specification version and software revisions. The software and speed specifications listed are the minimum releases required for production. All subsequent releases of software and speed specifications are valid.

**Table 14: Spartan-7 Device Production Software and Speed Specification Release**

Device	$V_{CCINT}$ Operating Voltage, Speed Grade, and Temperature Range		
	1.0V		0.95V
	-2C/-2I	-1C/-1I	-1LI
XC7S6			
XC7S15			
XC7S25			
XC7S50	Vivado tools 2017.2 v1.17		
XC7S75			
XC7S100			

# Performance Characteristics

This section provides the performance characteristics of some common functions and designs implemented in Spartan-7 FPGAs. These values are subject to the same guidelines as the [AC Switching Characteristics](#), page 11.

Table 15: Networking Applications Interface Performances

Description	V <sub>CCINT</sub> Operating Voltage, Speed Grade, and Temperature Range			Units
	1.0V		0.95V	
	-2C/-2I	-1C/-1I	-1LI	
SDR LVDS transmitter (using OSERDES; DATA_WIDTH = 4 to 8)	680	600	600	Mb/s
DDR LVDS transmitter (using OSERDES; DATA_WIDTH = 4 to 14)	1250	950	950	Mb/s
SDR LVDS receiver <sup>(1)</sup>	680	600	600	Mb/s
DDR LVDS receiver <sup>(1)</sup>	1250	950	950	Mb/s

**Notes:**

1. LVDS receivers are typically bounded with certain applications where specific dynamic phase-alignment (DPA) algorithms dominate deterministic performance.

Table 16: Maximum Physical Interface (PHY) Rate for Memory Interface IP available with the Memory Interface Generator<sup>(1)</sup>

Memory Standard	V <sub>CCINT</sub> Operating Voltage, Speed Grade, and Temperature Range			Units
	1.0V		0.95V	
	-2C/-2I	-1C/-1I	-1LI	
4:1 Memory Controllers				
DDR3	800	667	667	Mb/s
DDR3L	800	667	667	Mb/s
DDR2	800	667	667	Mb/s
2:1 Memory Controllers				
DDR3	800	667	667	Mb/s
DDR3L	800	667	667	Mb/s
DDR2	800	667	667	Mb/s
LPDDR2	667	533	533	Mb/s

**Notes:**

1. V<sub>REF</sub> tracking is required. For more information, see the *Zynq-7000 AP SoC and 7 Series FPGAs Memory Interface Solutions User Guide* (UG586) [Ref 6].

## IOB Pad Input/Output/3-State

Table 17 summarizes the values of standard-specific data input delay adjustments, output delays terminating at pads (based on standard) and 3-state delays.

- $T_{IOPI}$  is described as the delay from IOB pad through the input buffer to the I-pin of an IOB pad. The delay varies depending on the capability of the SelectIO input buffer.
- $T_{IOOP}$  is described as the delay from the O pin to the IOB pad through the output buffer of an IOB pad. The delay varies depending on the capability of the SelectIO output buffer.
- $T_{IOTP}$  is described as the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is disabled. The delay varies depending on the SelectIO capability of the output buffer. In HR I/O banks, the IN\_TERM termination turn-on time is always faster than  $T_{IOTP}$  when the INTERMDISABLE pin is used.

Table 17: IOB High Range (HR) Switching Characteristics

I/O Standard	T <sub>IOPI</sub>			T <sub>IOOP</sub>			T <sub>IOTP</sub>			Units
	V <sub>CCINT</sub> Operating Voltage and Speed Grade									
	1.0V		0.95V	1.0V		0.95V	1.0V		0.95V	
	-2	-1	-1L	-2	-1	-1L	-2	-1	-1L	
LVTTL_S4	1.34	1.41	1.41	3.93	4.18	4.18	3.96	4.20	4.20	ns
LVTTL_S8	1.34	1.41	1.41	3.66	3.92	3.92	3.69	3.93	3.93	ns
LVTTL_S12	1.34	1.41	1.41	3.65	3.90	3.90	3.68	3.91	3.91	ns
LVTTL_S16	1.34	1.41	1.41	3.19	3.45	3.45	3.22	3.46	3.46	ns
LVTTL_S24	1.34	1.41	1.41	3.41	3.67	3.67	3.44	3.68	3.68	ns
LVTTL_F4	1.34	1.41	1.41	3.38	3.64	3.64	3.41	3.65	3.65	ns
LVTTL_F8	1.34	1.41	1.41	2.87	3.12	3.12	2.90	3.13	3.13	ns
LVTTL_F12	1.34	1.41	1.41	2.85	3.10	3.10	2.88	3.12	3.12	ns
LVTTL_F16	1.34	1.41	1.41	2.68	2.93	2.93	2.71	2.95	2.95	ns
LVTTL_F24	1.34	1.41	1.41	2.65	2.90	2.90	2.68	2.91	2.91	ns
LVDS_25	0.81	0.88	0.88	1.41	1.67	1.67	1.44	1.68	1.68	ns
MINI_LVDS_25	0.81	0.88	0.88	1.40	1.65	1.65	1.43	1.66	1.66	ns
BLVDS_25	0.81	0.88	0.88	1.96	2.21	2.21	1.99	2.23	2.23	ns
RSDS_25 (point to point)	0.81	0.88	0.88	1.40	1.65	1.65	1.43	1.66	1.66	ns
PPDS_25	0.81	0.88	0.88	1.41	1.67	1.67	1.44	1.68	1.68	ns
TMDS_33	0.81	0.88	0.88	1.54	1.79	1.79	1.57	1.80	1.80	ns
PCI33_3	1.32	1.39	1.39	3.22	3.48	3.48	3.25	3.49	3.49	ns
HSUL_12_S	0.75	0.82	0.82	1.93	2.18	2.18	1.96	2.20	2.20	ns
HSUL_12_F	0.75	0.82	0.82	1.41	1.67	1.67	1.44	1.68	1.68	ns
DIFF_HSUL_12_S	0.76	0.83	0.83	1.93	2.18	2.18	1.96	2.20	2.20	ns
DIFF_HSUL_12_F	0.76	0.83	0.83	1.41	1.67	1.67	1.44	1.68	1.68	ns
MOBILE_DDR_S	0.84	0.91	0.91	1.80	2.06	2.06	1.83	2.07	2.07	ns
MOBILE_DDR_F	0.84	0.91	0.91	1.51	1.76	1.76	1.54	1.77	1.77	ns
DIFF_MOBILE_DDR_S	0.78	0.85	0.85	1.82	2.07	2.07	1.85	2.09	2.09	ns

Table 17: IOB High Range (HR) Switching Characteristics (Cont'd)

I/O Standard	T <sub>IOPI</sub>			T <sub>IOOP</sub>			T <sub>IOTP</sub>			Units
	V <sub>CCINT</sub> Operating Voltage and Speed Grade									
	1.0V		0.95V	1.0V		0.95V	1.0V		0.95V	
	-2	-1	-1L	-2	-1	-1L	-2	-1	-1L	
DIFF_MOBILE_DDR_F	0.78	0.85	0.85	1.57	1.82	1.82	1.60	1.84	1.84	ns
HSTL_I_S	0.75	0.82	0.82	1.74	1.99	1.99	1.77	2.01	2.01	ns
HSTL_II_S	0.73	0.80	0.80	1.54	1.79	1.79	1.57	1.80	1.80	ns
HSTL_I_18_S	0.75	0.82	0.82	1.41	1.67	1.67	1.44	1.68	1.68	ns
HSTL_II_18_S	0.75	0.81	0.81	1.54	1.79	1.79	1.57	1.80	1.80	ns
DIFF_HSTL_I_S	0.76	0.83	0.83	1.71	1.96	1.96	1.74	1.98	1.98	ns
DIFF_HSTL_II_S	0.76	0.83	0.83	1.63	1.88	1.88	1.66	1.90	1.90	ns
DIFF_HSTL_I_18_S	0.79	0.86	0.86	1.51	1.76	1.76	1.54	1.77	1.77	ns
DIFF_HSTL_II_18_S	0.78	0.85	0.85	1.58	1.84	1.84	1.61	1.85	1.85	ns
HSTL_I_F	0.75	0.82	0.82	1.22	1.48	1.48	1.25	1.49	1.49	ns
HSTL_II_F	0.73	0.80	0.80	1.24	1.49	1.49	1.27	1.51	1.51	ns
HSTL_I_18_F	0.75	0.82	0.82	1.26	1.51	1.51	1.29	1.52	1.52	ns
HSTL_II_18_F	0.75	0.81	0.81	1.24	1.49	1.49	1.27	1.51	1.51	ns
DIFF_HSTL_I_F	0.76	0.83	0.83	1.30	1.56	1.56	1.33	1.57	1.57	ns
DIFF_HSTL_II_F	0.76	0.83	0.83	1.33	1.59	1.59	1.36	1.60	1.60	ns
DIFF_HSTL_I_18_F	0.79	0.86	0.86	1.33	1.59	1.59	1.36	1.60	1.60	ns
DIFF_HSTL_II_18_F	0.78	0.85	0.85	1.33	1.59	1.59	1.36	1.60	1.60	ns
LVC MOS33_S4	1.34	1.41	1.41	3.93	4.18	4.18	3.96	4.20	4.20	ns
LVC MOS33_S8	1.34	1.41	1.41	3.65	3.90	3.90	3.68	3.91	3.91	ns
LVC MOS33_S12	1.34	1.41	1.41	3.21	3.46	3.46	3.24	3.48	3.48	ns
LVC MOS33_S16	1.34	1.41	1.41	3.52	3.77	3.77	3.55	3.79	3.79	ns
LVC MOS33_F4	1.34	1.41	1.41	3.38	3.64	3.64	3.41	3.65	3.65	ns
LVC MOS33_F8	1.34	1.41	1.41	2.87	3.12	3.12	2.90	3.13	3.13	ns
LVC MOS33_F12	1.34	1.41	1.41	2.68	2.93	2.93	2.71	2.95	2.95	ns
LVC MOS33_F16	1.34	1.41	1.41	2.68	2.93	2.93	2.71	2.95	2.95	ns
LVC MOS25_S4	1.20	1.27	1.27	3.26	3.51	3.51	3.29	3.52	3.52	ns
LVC MOS25_S8	1.20	1.27	1.27	3.01	3.26	3.26	3.04	3.27	3.27	ns
LVC MOS25_S12	1.20	1.27	1.27	2.60	2.85	2.85	2.63	2.87	2.87	ns
LVC MOS25_S16	1.20	1.27	1.27	2.94	3.20	3.20	2.97	3.21	3.21	ns
LVC MOS25_F4	1.20	1.27	1.27	2.87	3.12	3.12	2.90	3.13	3.13	ns
LVC MOS25_F8	1.20	1.27	1.27	2.30	2.56	2.56	2.33	2.57	2.57	ns
LVC MOS25_F12	1.20	1.27	1.27	2.29	2.54	2.54	2.32	2.55	2.55	ns
LVC MOS25_F16	1.20	1.27	1.27	2.13	2.39	2.39	2.16	2.40	2.40	ns
LVC MOS18_S4	0.83	0.89	0.89	1.74	1.99	1.99	1.77	2.01	2.01	ns
LVC MOS18_S8	0.83	0.89	0.89	2.30	2.56	2.56	2.33	2.57	2.57	ns
LVC MOS18_S12	0.83	0.89	0.89	2.30	2.56	2.56	2.33	2.57	2.57	ns

Table 17: IOB High Range (HR) Switching Characteristics (Cont'd)

I/O Standard	T <sub>IOPI</sub>			T <sub>IOOP</sub>			T <sub>IOTP</sub>			Units
	V <sub>CCINT</sub> Operating Voltage and Speed Grade									
	1.0V		0.95V	1.0V		0.95V	1.0V		0.95V	
	-2	-1	-1L	-2	-1	-1L	-2	-1	-1L	
LVC MOS18_S16	0.83	0.89	0.89	1.65	1.90	1.90	1.68	1.91	1.91	ns
LVC MOS18_S24	0.83	0.89	0.89	1.72	1.98	1.98	1.75	1.99	1.99	ns
LVC MOS18_F4	0.83	0.89	0.89	1.57	1.82	1.82	1.60	1.84	1.84	ns
LVC MOS18_F8	0.83	0.89	0.89	1.80	2.06	2.06	1.83	2.07	2.07	ns
LVC MOS18_F12	0.83	0.89	0.89	1.80	2.06	2.06	1.83	2.07	2.07	ns
LVC MOS18_F16	0.83	0.89	0.89	1.52	1.77	1.77	1.55	1.79	1.79	ns
LVC MOS18_F24	0.83	0.89	0.89	1.46	1.71	1.71	1.49	1.73	1.73	ns
LVC MOS15_S4	0.86	0.93	0.93	2.18	2.43	2.43	2.21	2.45	2.45	ns
LVC MOS15_S8	0.86	0.93	0.93	2.21	2.46	2.46	2.24	2.48	2.48	ns
LVC MOS15_S12	0.86	0.93	0.93	1.71	1.96	1.96	1.74	1.98	1.98	ns
LVC MOS15_S16	0.86	0.93	0.93	1.71	1.96	1.96	1.74	1.98	1.98	ns
LVC MOS15_F4	0.86	0.93	0.93	1.97	2.23	2.23	2.00	2.24	2.24	ns
LVC MOS15_F8	0.86	0.93	0.93	1.72	1.98	1.98	1.75	1.99	1.99	ns
LVC MOS15_F12	0.86	0.93	0.93	1.47	1.73	1.73	1.50	1.74	1.74	ns
LVC MOS15_F16	0.86	0.93	0.93	1.46	1.71	1.71	1.49	1.73	1.73	ns
LVC MOS12_S4	0.95	1.02	1.02	2.69	2.95	2.95	2.72	2.96	2.96	ns
LVC MOS12_S8	0.95	1.02	1.02	2.21	2.46	2.46	2.24	2.48	2.48	ns
LVC MOS12_S12	0.95	1.02	1.02	1.91	2.17	2.17	1.94	2.18	2.18	ns
LVC MOS12_F4	0.95	1.02	1.02	2.10	2.35	2.35	2.13	2.37	2.37	ns
LVC MOS12_F8	0.95	1.02	1.02	1.66	1.92	1.92	1.69	1.93	1.93	ns
LVC MOS12_F12	0.95	1.02	1.02	1.51	1.76	1.76	1.54	1.77	1.77	ns
SSTL135_S	0.75	0.82	0.82	1.47	1.73	1.73	1.50	1.74	1.74	ns
SSTL15_S	0.68	0.75	0.75	1.43	1.68	1.68	1.46	1.69	1.69	ns
SSTL18_I_S	0.75	0.82	0.82	1.79	2.04	2.04	1.82	2.06	2.06	ns
SSTL18_II_S	0.75	0.82	0.82	1.43	1.68	1.68	1.46	1.70	1.70	ns
DIFF_SSTL135_S	0.76	0.83	0.83	1.47	1.73	1.73	1.50	1.74	1.74	ns
DIFF_SSTL15_S	0.76	0.83	0.83	1.43	1.68	1.68	1.46	1.69	1.69	ns
DIFF_SSTL18_I_S	0.79	0.86	0.86	1.80	2.06	2.06	1.83	2.07	2.07	ns
DIFF_SSTL18_II_S	0.79	0.86	0.86	1.51	1.76	1.76	1.54	1.77	1.77	ns
SSTL135_F	0.75	0.82	0.82	1.24	1.49	1.49	1.27	1.51	1.51	ns
SSTL15_F	0.68	0.75	0.75	1.19	1.45	1.45	1.22	1.46	1.46	ns
SSTL18_I_F	0.75	0.82	0.82	1.24	1.49	1.49	1.27	1.51	1.51	ns
SSTL18_II_F	0.75	0.82	0.82	1.24	1.49	1.49	1.27	1.51	1.51	ns
DIFF_SSTL135_F	0.76	0.83	0.83	1.24	1.49	1.49	1.27	1.51	1.51	ns
DIFF_SSTL15_F	0.76	0.83	0.83	1.19	1.45	1.45	1.22	1.46	1.46	ns



Table 17: IOB High Range (HR) Switching Characteristics (Cont'd)

I/O Standard	T <sub>IOPI</sub>			T <sub>IOOP</sub>			T <sub>IOTP</sub>			Units
	V <sub>CCINT</sub> Operating Voltage and Speed Grade									
	1.0V		0.95V	1.0V		0.95V	1.0V		0.95V	
	-2	-1	-1L	-2	-1	-1L	-2	-1	-1L	
DIFF_SSTL18_I_F	0.79	0.86	0.86	1.35	1.60	1.60	1.38	1.62	1.62	ns
DIFF_SSTL18_II_F	0.79	0.86	0.86	1.33	1.59	1.59	1.36	1.60	1.60	ns

Table 18 specifies the values of  $T_{IOTPHZ}$  and  $T_{IOIBUFDISABLE}$ .  $T_{IOTPHZ}$  is described as the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is enabled (i.e., a high impedance state).  $T_{IOIBUFDISABLE}$  is described as the IOB delay from IBUFDISABLE to O output. In HR I/O banks, the internal IN\_TERM termination turn-off time is always faster than  $T_{IOTPHZ}$  when the INTERMDISABLE pin is used.

Table 18: IOB 3-state Output Switching Characteristics

Symbol	Description	$V_{CCINT}$ Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
$T_{IOTPHZ}$	T input to pad high-impedance.	2.19	2.37	2.37	ns
$T_{IOIBUFDISABLE}$	IBUF turn-on time from IBUFDISABLE to O output.	2.30	2.60	2.60	ns

## I/O Standard Adjustment Measurement Methodology

### Input Delay Measurements

Table 19 shows the test setup parameters used for measuring input delay.

Table 19: Input Delay Measurement Methodology

Description	I/O Standard Attribute	$V_L^{(1)}$	$V_H^{(1)}$	$V_{MEAS}^{(3)(5)}$	$V_{REF}^{(2)(4)}$
LVC MOS, 1.2V	LVC MOS12	0.1	1.1	0.6	–
LVC MOS, 1.5V	LVC MOS15	0.1	1.4	0.75	–
LVC MOS, 1.8V	LVC MOS18	0.1	1.7	0.9	–
LVC MOS, 2.5V	LVC MOS25	0.1	2.4	1.25	–
LVC MOS, 3.3V	LVC MOS33	0.1	3.2	1.65	–
LV TTL, 3.3V	LV TTL	0.1	3.2	1.65	–
MOBILE_DDR, 1.8V	MOBILE_DDR	0.1	1.7	0.9	–
PCI33, 3.3V	PCI33_3	0.1	3.2	1.65	–
HSTL (high-speed transceiver logic), Class I, 1.2V	HSTL_I_12	$V_{REF} - 0.5$	$V_{REF} + 0.5$	$V_{REF}$	0.60
HSTL, Class I & II, 1.5V	HSTL_I, HSTL_II	$V_{REF} - 0.65$	$V_{REF} + 0.65$	$V_{REF}$	0.75
HSTL, Class I & II, 1.8V	HSTL_I_18, HSTL_II_18	$V_{REF} - 0.8$	$V_{REF} + 0.8$	$V_{REF}$	0.90

Table 19: Input Delay Measurement Methodology (Cont'd)

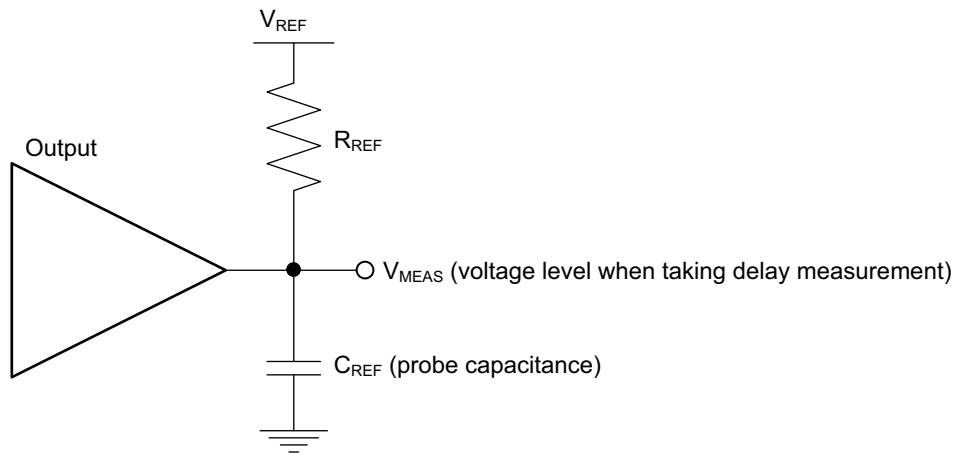
Description	I/O Standard Attribute	$V_L^{(1)}$	$V_H^{(1)}$	$V_{MEAS}^{(3)(5)}$	$V_{REF}^{(2)(4)}$
HSUL (high-speed unterminated logic), 1.2V	HSUL_12	$V_{REF} - 0.5$	$V_{REF} + 0.5$	$V_{REF}$	0.60
SSTL (stub-terminated transceiver logic), 1.2V	SSTL12	$V_{REF} - 0.5$	$V_{REF} + 0.5$	$V_{REF}$	0.60
SSTL, 1.35V	SSTL135, SSTL135_R	$V_{REF} - 0.575$	$V_{REF} + 0.575$	$V_{REF}$	0.675
SSTL, 1.5V	SSTL15, SSTL15_R	$V_{REF} - 0.65$	$V_{REF} + 0.65$	$V_{REF}$	0.75
SSTL, Class I & II, 1.8V	SSTL18_I, SSTL18_II	$V_{REF} - 0.8$	$V_{REF} + 0.8$	$V_{REF}$	0.90
DIFF_MOBILE_DDR, 1.8V	DIFF_MOBILE_DDR	$0.9 - 0.125$	$0.9 + 0.125$	0 <sup>(5)</sup>	–
DIFF_HSTL, Class I, 1.2V	DIFF_HSTL_I_12	$0.6 - 0.125$	$0.6 + 0.125$	0 <sup>(5)</sup>	–
DIFF_HSTL, Class I & II, 1.5V	DIFF_HSTL_I, DIFF_HSTL_II	$0.75 - 0.125$	$0.75 + 0.125$	0 <sup>(5)</sup>	–
DIFF_HSTL, Class I & II, 1.8V	DIFF_HSTL_I_18, DIFF_HSTL_II_18	$0.9 - 0.125$	$0.9 + 0.125$	0 <sup>(5)</sup>	–
DIFF_HSUL, 1.2V	DIFF_HSUL_12	$0.6 - 0.125$	$0.6 + 0.125$	0 <sup>(5)</sup>	–
DIFF_SSTL135/ DIFF_SSTL135_R, 1.35V	DIFF_SSTL135, DIFF_SSTL135_R	$0.675 - 0.125$	$0.675 + 0.125$	0 <sup>(5)</sup>	–
DIFF_SSTL15/ DIFF_SSTL15_R, 1.5V	DIFF_SSTL15, DIFF_SSTL15_R	$0.75 - 0.125$	$0.75 + 0.125$	0 <sup>(5)</sup>	–
DIFF_SSTL18_I/ DIFF_SSTL18_II, 1.8V	DIFF_SSTL18_I, DIFF_SSTL18_II	$0.9 - 0.125$	$0.9 + 0.125$	0 <sup>(5)</sup>	–
LVDS_25, 2.5V	LVDS_25	$1.2 - 0.125$	$1.2 + 0.125$	0 <sup>(5)</sup>	–
BLVDS_25, 2.5V	BLVDS_25	$1.25 - 0.125$	$1.25 + 0.125$	0 <sup>(5)</sup>	–
MINI_LVDS_25, 2.5V	MINI_LVDS_25	$1.25 - 0.125$	$1.25 + 0.125$	0 <sup>(5)</sup>	–
PPDS_25	PPDS_25	$1.25 - 0.125$	$1.25 + 0.125$	0 <sup>(5)</sup>	–
RSDS_25	RSDS_25	$1.25 - 0.125$	$1.25 + 0.125$	0 <sup>(5)</sup>	–
TMDS_33	TMDS_33	$3 - 0.125$	$3 + 0.125$	0 <sup>(5)</sup>	–

**Notes:**

1. Input waveform switches between  $V_L$  and  $V_H$ .
2. Measurements are made at typical, minimum, and maximum  $V_{REF}$  values. Reported delays reflect worst case of these measurements.  $V_{REF}$  values listed are typical.
3. Input voltage level from which measurement starts.
4. This is an input voltage reference that bears no relation to the  $V_{REF}$  /  $V_{MEAS}$  parameters found in IBIS models and/or noted in [Figure 1](#).
5. The value given is the differential input voltage.

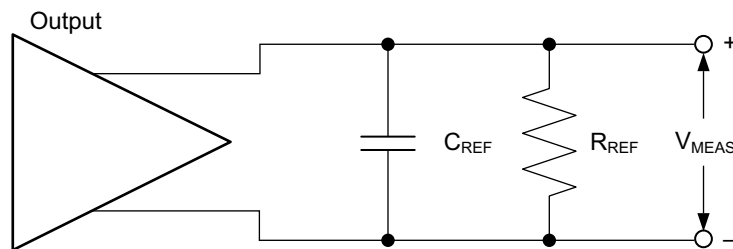
## Output Delay Measurements

Output delays are measured with short output traces. Standard termination was used for all testing. The propagation delay of the trace is characterized separately and subtracted from the final measurement, and is therefore not included in the generalized test setups shown in [Figure 1](#) and [Figure 2](#).



X16654-092616

Figure 1: Single-ended Test Setup



X16640-092616

Figure 2: Differential Test Setup

Parameters  $V_{REF}$ ,  $R_{REF}$ ,  $C_{REF}$ , and  $V_{MEAS}$  fully describe the test conditions for each I/O standard. The most accurate prediction of propagation delay in any given application can be obtained through IBIS simulation, using this method:

1. Simulate the output driver of choice into the generalized test setup using values from [Table 20](#).
2. Record the time to  $V_{MEAS}$ .
3. Simulate the output driver of choice into the actual PCB trace and load using the appropriate IBIS model or capacitance value to represent the load.
4. Record the time to  $V_{MEAS}$ .
5. Compare the results of [step 2](#) and [step 4](#). The increase or decrease in delay yields the actual propagation delay of the PCB trace.

Table 20: Output Delay Measurement Methodology

Description	I/O Standard Attribute	R <sub>REF</sub> ( $\Omega$ )	C <sub>REF</sub> <sup>(1)</sup> (pF)	V <sub>MEAS</sub> (V)	V <sub>REF</sub> (V)
LVC MOS, 1.2V	LVC MOS12	1M	0	0.6	0
LVC MOS, 1.5V	LVC MOS15	1M	0	0.75	0
LVC MOS, 1.8V	LVC MOS18	1M	0	0.9	0
LVC MOS, 2.5V	LVC MOS25	1M	0	1.25	0
LVC MOS, 3.3V	LVC MOS33	1M	0	1.65	0
LVTTL, 3.3V	LVTTL	1M	0	1.65	0
PCI33, 3.3V	PCI33_3	25	10	1.65	0
HSTL (high-speed transceiver logic), Class I, 1.2V	HSTL_I_12	50	0	V <sub>REF</sub>	0.6
HSTL, Class I, 1.5V	HSTL_I	50	0	V <sub>REF</sub>	0.75
HSTL, Class II, 1.5V	HSTL_II	25	0	V <sub>REF</sub>	0.75
HSTL, Class I, 1.8V	HSTL_I_18	50	0	V <sub>REF</sub>	0.9
HSTL, Class II, 1.8V	HSTL_II_18	25	0	V <sub>REF</sub>	0.9
HSUL (high-speed unterminated logic), 1.2V	HSUL_12	50	0	V <sub>REF</sub>	0.6
SSTL12, 1.2V	SSTL12	50	0	V <sub>REF</sub>	0.6
SSTL135/SSTL135_R, 1.35V	SSTL135, SSTL135_R	50	0	V <sub>REF</sub>	0.675
SSTL15/SSTL15_R, 1.5V	SSTL15, SSTL15_R	50	0	V <sub>REF</sub>	0.75
SSTL (stub-series terminated logic), Class I & Class II, 1.8V	SSTL18_I, SSTL18_II	50	0	V <sub>REF</sub>	0.9
DIFF_MOBILE_DDR, 1.8V	DIFF_MOBILE_DDR	50	0	V <sub>REF</sub>	0.9
DIFF_HSTL, Class I, 1.2V	DIFF_HSTL_I_12	50	0	V <sub>REF</sub>	0.6
DIFF_HSTL, Class I & II, 1.5V	DIFF_HSTL_I, DIFF_HSTL_II	50	0	V <sub>REF</sub>	0.75
DIFF_HSTL, Class I & II, 1.8V	DIFF_HSTL_I_18, DIFF_HSTL_II_18	50	0	V <sub>REF</sub>	0.9
DIFF_HSUL_12, 1.2V	DIFF_HSUL_12	50	0	V <sub>REF</sub>	0.6
DIFF_SSTL135/DIFF_SSTL135_R, 1.35V	DIFF_SSTL135, DIFF_SSTL135_R	50	0	V <sub>REF</sub>	0.675
DIFF_SSTL15/DIFF_SSTL15_R, 1.5V	DIFF_SSTL15, DIFF_SSTL15_R	50	0	V <sub>REF</sub>	0.75
DIFF_SSTL18, Class I & II, 1.8V	DIFF_SSTL18_I, DIFF_SSTL18_II	50	0	V <sub>REF</sub>	0.9
LVDS, 2.5V	LVDS_25	100	0	0 <sup>(2)</sup>	0
BLVDS (Bus LVDS), 2.5V	BLVDS_25	100	0	0 <sup>(2)</sup>	0
Mini LVDS, 2.5V	MINI_LVDS_25	100	0	0 <sup>(2)</sup>	0
PPDS_25	PPDS_25	100	0	0 <sup>(2)</sup>	0
RS DS_25	RS DS_25	100	0	0 <sup>(2)</sup>	0
TM DS_33	TM DS_33	50	0	0 <sup>(2)</sup>	3.3

**Notes:**

1. C<sub>REF</sub> is the capacitance of the probe, nominally 0 pF.
2. The value given is the differential output voltage.

# Input/Output Logic Switching Characteristics

Table 21: ILOGIC Switching Characteristics

Symbol	Description	V <sub>CCINT</sub> Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
Setup/Hold					
T <sub>ICE1CK</sub> /T <sub>ICKCE1</sub>	CE1 pin setup/hold with respect to CLK.	0.54/0.02	0.76/0.02	0.76/0.02	ns
T <sub>ISRCK</sub> /T <sub>ICKSR</sub>	SR pin setup/hold with respect to CLK.	0.70/0.01	1.13/0.01	1.13/0.01	ns
T <sub>IDOCK</sub> /T <sub>IOCKD</sub>	D pin setup/hold with respect to CLK without delay.	0.01/0.29	0.01/0.33	0.01/0.33	ns
T <sub>IDOCKD</sub> /T <sub>IOCKDD</sub>	DDL pin setup/hold with respect to CLK (using IDELAY).	0.02/0.29	0.02/0.33	0.02/0.33	ns
Combinatorial					
T <sub>IDI</sub>	D pin to O pin propagation delay, no delay.	0.11	0.13	0.13	ns
T <sub>IDID</sub>	DDL pin to O pin propagation delay (using IDELAY).	0.12	0.14	0.14	ns
Sequential Delays					
T <sub>IDLO</sub>	D pin to Q1 pin using flip-flop as a latch without delay.	0.44	0.51	0.51	ns
T <sub>IDLOD</sub>	DDL pin to Q1 pin using flip-flop as a latch (using IDELAY).	0.44	0.51	0.51	ns
T <sub>ICKQ</sub>	CLK to Q outputs.	0.57	0.66	0.66	ns
T <sub>RQ_ILOGIC</sub>	SR pin to OQ/TQ out.	1.08	1.32	1.32	ns
T <sub>GSRQ_ILOGIC</sub>	Global set/reset to Q outputs.	7.60	10.51	10.51	ns
Set/Reset					
T <sub>RPW_ILOGIC</sub>	Minimum pulse width, SR inputs.	0.72	0.72	0.72	ns, Min

Table 22: OLOGIC Switching Characteristics

Symbol	Description	V <sub>CCINT</sub> Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
Setup/Hold					
T <sub>ODCK</sub> /T <sub>OCKD</sub>	D1/D2 pins setup/hold with respect to CLK.	0.71/−0.11	0.84/−0.11	0.84/−0.11	ns
T <sub>OOCECK</sub> /T <sub>OCKOCE</sub>	OCE pin setup/hold with respect to CLK.	0.34/0.58	0.51/0.58	0.51/0.58	ns
T <sub>OSRCK</sub> /T <sub>OCKSR</sub>	SR pin setup/hold with respect to CLK.	0.44/0.21	0.80/0.21	0.80/0.21	ns
T <sub>OTCK</sub> /T <sub>OCKT</sub>	T1/T2 pins setup/hold with respect to CLK.	0.73/−0.14	0.89/−0.14	0.89/−0.14	ns
T <sub>OTCECK</sub> /T <sub>OCKTCE</sub>	TCE pin setup/hold with respect to CLK.	0.34/0.01	0.51/0.01	0.51/0.01	ns
Combinatorial					
T <sub>ODQ</sub>	D1 to OQ out or T1 to TQ out.	0.96	1.16	1.16	ns
Sequential Delays					
T <sub>OCKQ</sub>	CLK to OQ/TQ out.	0.49	0.56	0.56	ns
T <sub>RQ_OLOGIC</sub>	SR pin to OQ/TQ out.	0.80	0.95	0.95	ns
T <sub>GSRQ_OLOGIC</sub>	Global set/reset to Q outputs.	7.60	10.51	10.51	ns
Set/Reset					
T <sub>RPW_OLOGIC</sub>	Minimum pulse width, SR inputs.	0.74	0.74	0.74	ns, Min

# Input Serializer/Deserializer Switching Characteristics

Table 23: ISERDES Switching Characteristics

Symbol	Description	V <sub>CCINT</sub> Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
Setup/Hold for Control Lines					
T <sub>ISCKK_BITSLIP</sub> / T <sub>ISCKC_BITSLIP</sub>	BITSLIP pin setup/hold with respect to CLKDIV.	0.02/0.15	0.02/0.17	0.02/0.17	ns
T <sub>ISCKK_CE</sub> / T <sub>ISCKC_CE</sub>	CE pin setup/hold with respect to CLK (for CE1).	0.50/−0.01	0.72/−0.01	0.72/−0.01	ns
T <sub>ISCKK_CE2</sub> / T <sub>ISCKC_CE2</sub>	CE pin setup/hold with respect to CLKDIV (for CE2).	−0.10/0.36	−0.10/0.40	−0.10/0.40	ns
Setup/Hold for Data Lines					
T <sub>ISDCK_D</sub> / T <sub>ISCKD_D</sub>	D pin setup/hold with respect to CLK.	−0.02/0.14	−0.02/0.17	−0.02/0.17	ns
T <sub>ISDCK_DDLY</sub> / T <sub>ISCKD_DDLY</sub>	DDLY pin setup/hold with respect to CLK (using IDELAY). <sup>(1)</sup>	−0.02/0.14	−0.02/0.17	−0.02/0.17	ns
T <sub>ISDCK_D_DDR</sub> / T <sub>ISCKD_D_DDR</sub>	D pin setup/hold with respect to CLK at DDR mode.	−0.02/0.14	−0.02/0.17	−0.02/0.17	ns
T <sub>ISDCK_DDLY_DDR</sub> / T <sub>ISCKD_DDLY_DDR</sub>	D pin setup/hold with respect to CLK at DDR mode (using IDELAY). <sup>(1)</sup>	0.14/0.14	0.17/0.17	0.17/0.17	ns
Sequential Delays					
T <sub>ISCKO_Q</sub>	CLKDIV to out at Q pin.	0.54	0.66	0.66	ns
Propagation Delays					
T <sub>ISDO_DO</sub>	D input to DO output pin.	0.11	0.13	0.13	ns

## Notes:

- Recorded at 0 tap value.

# Output Serializer/Deserializer Switching Characteristics

Table 24: OSERDES Switching Characteristics

Symbol	Description	V <sub>CCINT</sub> Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
Setup/Hold					
T <sub>OSDCK_D</sub> / T <sub>OSCKD_D</sub>	D input setup/hold with respect to CLKDIV.	0.45/0.03	0.63/0.03	0.63/0.03	ns
T <sub>OSDCK_T</sub> / T <sub>OSCKD_T</sub>	T input setup/hold with respect to CLK.	0.73/−0.13	0.88/−0.13	0.88/−0.13	ns
T <sub>OSDCK_T2</sub> / T <sub>OSCKD_T2</sub>	T input setup/hold with respect to CLKDIV.	0.34/−0.13	0.39/−0.13	0.39/−0.13	ns
T <sub>OSCKCK_OCE</sub> / T <sub>OSCKC_OCE</sub>	OCE input setup/hold with respect to CLK.	0.34/0.58	0.51/0.58	0.51/0.58	ns
T <sub>OSCKCK_S</sub>	SR (reset) input setup with respect to CLKDIV.	0.52	0.85	0.85	ns
T <sub>OSCKCK_TCE</sub> / T <sub>OSCKC_TCE</sub>	TCE input setup/hold with respect to CLK.	0.34/0.01	0.51/0.01	0.51/0.01	ns
Sequential Delays					
T <sub>OSCKO_OQ</sub>	Clock to out from CLK to OQ.	0.42	0.48	0.48	ns
T <sub>OSCKO_TQ</sub>	Clock to out from CLK to TQ.	0.49	0.56	0.56	ns
Combinatorial					
T <sub>OSDO_TTQ</sub>	T input to TQ out.	0.92	1.11	1.11	ns



# Input/Output Delay Switching Characteristics

Table 25: Input/Output Delay Switching Characteristics

Symbol	Description	V <sub>CCINT</sub> Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
IDELAYCTRL					
T <sub>DLYCCO_RDY</sub>	Reset to ready for IDELAYCTRL.	3.67	3.67	3.67	μs
F <sub>IDELAYCTRL_REF</sub>	Attribute REFCLK frequency = 200.00. <sup>(1)</sup>	200.00	200.00	200.00	MHz
	Attribute REFCLK frequency = 300.00. <sup>(1)</sup>	300.00	300.00	300.00	MHz
	Attribute REFCLK frequency = 400.00. <sup>(1)</sup>	400.00	N/A	N/A	MHz
IDELAYCTRL_REF_PRECISION	REFCLK precision	±10	±10	±10	MHz
T <sub>IDELAYCTRL_RPW</sub>	Minimum reset pulse width.	59.28	59.28	59.28	ns
IDELAY					
T <sub>IDELAYRESOLUTION</sub>	IDELAY chain delay resolution.	1/(32 x 2 x F <sub>REF</sub> )			μs
T <sub>IDELAYPAT_JIT</sub>	Pattern dependent period jitter in delay chain for clock pattern. <sup>(2)</sup>	0	0	0	ps per tap
	Pattern dependent period jitter in delay chain for random data pattern (PRBS 23). <sup>(3)</sup>	±5	±5	±5	ps per tap
	Pattern dependent period jitter in delay chain for random data pattern (PRBS 23). <sup>(4)</sup>	±9	±9	±9	ps per tap
T <sub>IDELAY_CLK_MAX</sub>	Maximum frequency of CLK input to IDELAY.	680.00	600.00	600.00	MHz
T <sub>IDCCK_CE</sub> / T <sub>IDCKC_CE</sub>	CE pin setup/hold with respect to C for IDELAY.	0.16/0.13	0.21/0.16	0.21/0.16	ns
T <sub>IDCCK_INC</sub> /T <sub>IDCKC_INC</sub>	INC pin setup/hold with respect to C for IDELAY.	0.14/0.18	0.16/0.22	0.16/0.22	ns
T <sub>IDCCK_RST</sub> /T <sub>IDCKC_RST</sub>	RST pin setup/hold with respect to C for IDELAY.	0.16/0.11	0.18/0.14	0.18/0.14	ns
T <sub>IDDO_IDATAIN</sub>	Propagation delay through IDELAY.	Note 5	Note 5	Note 5	ps

## Notes:

1. Average tap delay at 200 MHz = 78 ps, at 300 MHz = 52 ps, and at 400 MHz = 39 ps.
2. When HIGH\_PERFORMANCE mode is set to TRUE or FALSE.
3. When HIGH\_PERFORMANCE mode is set to TRUE.
4. When HIGH\_PERFORMANCE mode is set to FALSE.
5. Delay depends on IDELAY tap setting. See the timing report for actual values.

Table 26: IO\_FIFO Switching Characteristics

Symbol	Description	V <sub>CCINT</sub> Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
IO_FIFO Clock to Out Delays					
T <sub>OFFCKO_DO</sub>	RDCLK to Q outputs.	0.60	0.68	0.68	ns
T <sub>CKO_FLAGS</sub>	Clock to IO_FIFO flags.	0.61	0.77	0.77	ns
Setup/Hold					
T <sub>CCK_D</sub> /T <sub>CKC_D</sub>	D inputs to WRCLK.	0.51/0.02	0.58/0.02	0.58/0.02	ns
T <sub>IFFCCK_WREN</sub> / T <sub>IFFCKC_WREN</sub>	WREN to WRCLK.	0.47/−0.01	0.53/−0.01	0.53/−0.01	ns
T <sub>OFFCCK_RDEN</sub> / T <sub>OFFCKC_RDEN</sub>	RDEN to RDCLK.	0.58/0.02	0.66/0.02	0.66/0.02	ns
Minimum Pulse Width					
T <sub>PWH_IO_FIFO</sub>	RESET, RDCLK, WRCLK.	2.15	2.15	2.15	ns
T <sub>PWL_IO_FIFO</sub>	RESET, RDCLK, WRCLK.	2.15	2.15	2.15	ns
Maximum Frequency					
F <sub>MAX</sub>	RDCLK and WRCLK.	200.00	200.00	200.00	MHz

## CLB Switching Characteristics

Table 27: CLB Switching Characteristics

Symbol	Description	V <sub>CCINT</sub> Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
Combinatorial Delays					
T <sub>ILO</sub>	An – Dn LUT address to A.	0.11	0.13	0.13	ns, Max
T <sub>ILO_2</sub>	An – Dn LUT address to AMUX/CMUX.	0.30	0.36	0.36	ns, Max
T <sub>ILO_3</sub>	An – Dn LUT address to BMUX_A.	0.46	0.55	0.55	ns, Max
T <sub>ITO</sub>	An – Dn inputs to A – D Q outputs.	1.05	1.27	1.27	ns, Max
T <sub>AXA</sub>	AX inputs to AMUX output.	0.69	0.84	0.84	ns, Max
T <sub>AXB</sub>	AX inputs to BMUX output.	0.66	0.83	0.83	ns, Max
T <sub>AXC</sub>	AX inputs to CMUX output.	0.68	0.82	0.82	ns, Max
T <sub>AXD</sub>	AX inputs to DMUX output.	0.75	0.90	0.90	ns, Max
T <sub>BXB</sub>	BX inputs to BMUX output.	0.57	0.69	0.69	ns, Max
T <sub>BXD</sub>	BX inputs to DMUX output.	0.69	0.82	0.82	ns, Max
T <sub>CXC</sub>	CX inputs to CMUX output.	0.48	0.58	0.58	ns, Max
T <sub>CXD</sub>	CX inputs to DMUX output.	0.59	0.71	0.71	ns, Max
T <sub>DXD</sub>	DX inputs to DMUX output.	0.58	0.70	0.70	ns, Max
Sequential Delays					
T <sub>CKO</sub>	Clock to AQ – DQ outputs.	0.44	0.53	0.53	ns, Max
T <sub>SHCKO</sub>	Clock to AMUX – DMUX outputs.	0.53	0.66	0.66	ns, Max
Setup and Hold Times of CLB Flip-Flops Before/After Clock CLK					
T <sub>AS</sub> /T <sub>AH</sub>	AN – DN input to CLK on A – D flip-flops.	0.09/0.14	0.11/0.18	0.11/0.18	ns, Min
T <sub>DICK</sub> /T <sub>CKDI</sub>	AX – DX input to CLK on A – D flip-flops.	0.07/0.21	0.09/0.26	0.09/0.26	ns, Min
	AX – DX input through MUXs and/or carry logic to CLK on A – D flip-flops.	0.66/0.09	0.81/0.11	0.81/0.11	ns, Min
T <sub>CECK_CLB</sub> /T <sub>CKCE_CLB</sub>	CE input to CLK on A – D flip-flops.	0.17/0.00	0.21/0.01	0.21/0.01	ns, Min
T <sub>SRCK</sub> /T <sub>CKSR</sub>	SR input to CLK on A – D flip-flops.	0.43/0.04	0.53/0.05	0.53/0.05	ns, Min
Set/Reset					
T <sub>SRMIN</sub>	SR input minimum pulse width.	0.78	1.04	1.04	ns, Min
T <sub>RQ</sub>	Delay from SR input to AQ – DQ flip-flops.	0.59	0.71	0.71	ns, Max
T <sub>CEO</sub>	Delay from CE input to AQ – DQ flip-flops.	0.58	0.70	0.70	ns, Max
F <sub>TOG</sub>	Toggle frequency (for export control).	1286	1098	1098	MHz

## CLB Distributed RAM Switching Characteristics (SLICEM Only)

Table 28: CLB Distributed RAM Switching Characteristics

Symbol	Description	V <sub>CCINT</sub> Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
Sequential Delays					
T <sub>SHCKO</sub>	Clock to A – B outputs.	1.09	1.32	1.32	ns, Max
T <sub>SHCKO_1</sub>	Clock to AMUX – BMUX outputs.	1.53	1.86	1.86	ns, Max
Setup and Hold Times Before/After Clock CLK					
T <sub>DS_LRAM</sub> /T <sub>DH_LRAM</sub>	A – D inputs to CLK.	0.60/0.30	0.72/0.35	0.72/0.35	ns, Min
T <sub>AS_LRAM</sub> /T <sub>AH_LRAM</sub>	Address An inputs to clock.	0.30/0.60	0.37/0.70	0.37/0.70	ns, Min
	Address An inputs through MUXs and/or carry logic to clock.	0.77/0.21	0.94/0.26	0.94/0.26	ns, Min
T <sub>WS_LRAM</sub> /T <sub>WH_LRAM</sub>	WE input to clock.	0.43/0.12	0.53/0.17	0.53/0.17	ns, Min
T <sub>CECK_LRAM</sub> /T <sub>CKCE_LRAM</sub>	CE input to CLK.	0.44/0.11	0.53/0.17	0.53/0.17	ns, Min
Clock CLK					
T <sub>MPW_LRAM</sub>	Minimum pulse width.	1.13	1.25	1.25	ns, Min
T <sub>MCP</sub>	Minimum clock period.	2.26	2.50	2.50	ns, Min

**Notes:**

1. T<sub>SHCKO</sub> also represents the CLK to XMUX output. Refer to the timing report for the CLK to XMUX path.

## CLB Shift Register Switching Characteristics (SLICEM Only)

Table 29: CLB Shift Register Switching Characteristics

Symbol	Description	V <sub>CCINT</sub> Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
Sequential Delays					
T <sub>REG</sub>	Clock to A – D outputs.	1.33	1.61	1.61	ns, Max
T <sub>REG_MUX</sub>	Clock to AMUX – DMUX output.	1.77	2.15	2.15	ns, Max
T <sub>REG_M31</sub>	Clock to DMUX output via M31 output.	1.23	1.46	1.46	ns, Max
Setup and Hold Times Before/After Clock CLK					
T <sub>WS_SHFREG</sub> / T <sub>WH_SHFREG</sub>	WE input.	0.41/0.12	0.51/0.17	0.51/0.17	ns, Min
T <sub>CECK_SHFREG</sub> / T <sub>CKCE_SHFREG</sub>	CE input to CLK.	0.42/0.11	0.52/0.17	0.52/0.17	ns, Min
T <sub>DS_SHFREG</sub> / T <sub>DH_SHFREG</sub>	A – D inputs to CLK.	0.37/0.37	0.44/0.43	0.44/0.43	ns, Min
Clock CLK					
T <sub>MPW_SHFREG</sub>	Minimum pulse width.	0.86	0.98	0.98	ns, Min

## Block RAM and FIFO Switching Characteristics

Table 30: Block RAM and FIFO Switching Characteristics

Symbol	Description	V <sub>CCINT</sub> Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
Block RAM and FIFO Clock-to-Out Delays					
T <sub>RCKO_DO</sub> and T <sub>RCKO_DO_REG</sub>	Clock CLK to DOUT output (without output register). <sup>(1)(2)</sup>	2.13	2.46	2.46	ns, Max
	Clock CLK to DOUT output (with output register). <sup>(3)(4)</sup>	0.74	0.89	0.89	ns, Max
T <sub>RCKO_DO_ECC</sub> and T <sub>RCKO_DO_ECC_REG</sub>	Clock CLK to DOUT output with ECC (without output register). <sup>(1)(2)</sup>	3.04	3.84	3.84	ns, Max
	Clock CLK to DOUT output with ECC (with output register). <sup>(3)(4)</sup>	0.81	0.94	0.94	ns, Max
T <sub>RCKO_DO_CASCOUT</sub> and T <sub>RCKO_DO_CASCOUT_REG</sub>	Clock CLK to DOUT output with cascade (without output register). <sup>(1)</sup>	2.88	3.30	3.30	ns, Max
	Clock CLK to DOUT output with cascade (with output register). <sup>(3)</sup>	1.28	1.46	1.46	ns, Max
T <sub>RCKO_FLAGS</sub>	Clock CLK to FIFO flags outputs. <sup>(5)</sup>	0.87	1.05	1.05	ns, Max
T <sub>RCKO_POINTERS</sub>	Clock CLK to FIFO pointers outputs. <sup>(6)</sup>	1.02	1.15	1.15	ns, Max
T <sub>RCKO_PARITY_ECC</sub>	Clock CLK to ECCPARITY in ECC encode only mode.	0.85	0.94	0.94	ns, Max
T <sub>RCKO_SDBIT_ECC</sub> and T <sub>RCKO_SDBIT_ECC_REG</sub>	Clock CLK to BITERR (without output register).	2.81	3.55	3.55	ns, Max
	Clock CLK to BITERR (with output register).	0.76	0.89	0.89	ns, Max
T <sub>RCKO_RDADDR_ECC</sub> and T <sub>RCKO_RDADDR_ECC_REG</sub>	Clock CLK to RDADDR output with ECC (without output register).	0.88	1.07	1.07	ns, Max
	Clock CLK to RDADDR output with ECC (with output register).	0.93	1.08	1.08	ns, Max
Setup and Hold Times Before/After Clock CLK					
T <sub>RCCK_ADDRA</sub> / T <sub>RCKC_ADDRA</sub>	ADDR inputs. <sup>(7)</sup>	0.49/0.33	0.57/0.36	0.57/0.36	ns, Min
T <sub>RDCK_DI_WF_NC</sub> / T <sub>RCKD_DI_WF_NC</sub>	Data input setup/hold time when block RAM is configured in WRITE_FIRST or NO_CHANGE mode. <sup>(8)</sup>	0.65/0.63	0.74/0.67	0.74/0.67	ns, Min
T <sub>RDCK_DI_RF</sub> / T <sub>RCKD_DI_RF</sub>	Data input setup/hold time when block RAM is configured in READ_FIRST mode. <sup>(8)</sup>	0.22/0.34	0.25/0.41	0.25/0.41	ns, Min
T <sub>RDCK_DI_ECC</sub> / T <sub>RCKD_DI_ECC</sub>	DIN inputs with block RAM ECC in standard mode. <sup>(8)</sup>	0.55/0.46	0.63/0.50	0.63/0.50	ns, Min
T <sub>RDCK_DI_ECCW</sub> / T <sub>RCKD_DI_ECCW</sub>	DIN inputs with block RAM ECC encode only. <sup>(8)</sup>	1.02/0.46	1.17/0.50	1.17/0.50	ns, Min

Table 30: Block RAM and FIFO Switching Characteristics (Cont'd)

Symbol	Description	V <sub>CCINT</sub> Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
T <sub>RDCK_DI_ECC_FIFO</sub> / T <sub>RCKD_DI_ECC_FIFO</sub>	DIN inputs with FIFO ECC in standard mode. <sup>(8)</sup>	1.15/0.59	1.32/0.64	1.32/0.64	ns, Min
T <sub>RCCK_INJECTBITERR</sub> / T <sub>RCKC_INJECTBITERR</sub>	Inject single/double bit error in ECC mode.	0.64/0.37	0.74/0.40	0.74/0.40	ns, Min
T <sub>RCCK_EN</sub> /T <sub>RCKC_EN</sub>	Block RAM enable (EN) input.	0.39/0.21	0.45/0.23	0.45/0.23	ns, Min
T <sub>RCCK_REGCE</sub> / T <sub>RCKC_REGCE</sub>	CE input of output register.	0.29/0.15	0.36/0.16	0.36/0.16	ns, Min
T <sub>RCCK_RSTREG</sub> / T <sub>RCKC_RSTREG</sub>	Synchronous RSTREG input.	0.32/0.07	0.35/0.07	0.35/0.07	ns, Min
T <sub>RCCK_RSTRAM</sub> / T <sub>RCKC_RSTRAM</sub>	Synchronous RSTRAM input.	0.34/0.43	0.36/0.46	0.36/0.46	ns, Min
T <sub>RCCK_WEA</sub> /T <sub>RCKC_WEA</sub>	Write enable (WE) input (block RAM only).	0.48/0.19	0.54/0.20	0.54/0.20	ns, Min
T <sub>RCCK_WREN</sub> / T <sub>RCKC_WREN</sub>	WREN FIFO inputs.	0.46/0.35	0.47/0.43	0.47/0.43	ns, Min
T <sub>RCCK_RDEN</sub> / T <sub>RCKC_RDEN</sub>	RDEN FIFO inputs.	0.43/0.35	0.43/0.43	0.43/0.43	ns, Min
<b>Reset Delays</b>					
T <sub>RCO_FLAGS</sub>	Reset RST to FIFO flags/pointers. <sup>(9)</sup>	0.98	1.10	1.10	ns, Max
T <sub>RREC_RST</sub> /T <sub>RREM_RST</sub>	FIFO reset recovery and removal timing. <sup>(10)</sup>	2.07/-0.81	2.37/-0.81	2.37/-0.81	ns, Max
<b>Maximum Frequency</b>					
F <sub>MAX_BRAM_WF_NC</sub>	Block RAM (write first and no change modes) when not in SDP RF mode.	460.83	388.20	388.20	MHz
F <sub>MAX_BRAM_RF_PERFORMANCE</sub>	Block RAM (read first, performance mode) when in SDP RF mode but no address overlap between port A and port B.	460.83	388.20	388.20	MHz
F <sub>MAX_BRAM_RF_DELAYED_WRITE</sub>	Block RAM (read first, delayed write mode) when in SDP RF mode and there is possibility of overlap between port A and port B addresses.	404.53	339.67	339.67	MHz
F <sub>MAX_CAS_WF_NC</sub>	Block RAM cascade (write first, no change mode) when cascade but not in RF mode.	418.59	345.78	345.78	MHz
F <sub>MAX_CAS_RF_PERFORMANCE</sub>	Block RAM cascade (read first, performance mode) when in cascade with RF mode and no possibility of address overlap/one port is disabled.	418.59	345.78	345.78	MHz

Table 30: Block RAM and FIFO Switching Characteristics (Cont'd)

Symbol	Description	V <sub>CCINT</sub> Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
F <sub>MAX_CAS_RF_DELAYED_WRITE</sub>	When in cascade RF mode and there is a possibility of address overlap between port A and port B.	362.19	297.35	297.35	MHz
F <sub>MAX_FIFO</sub>	FIFO in all modes without ECC.	460.83	388.20	388.20	MHz
F <sub>MAX_ECC</sub>	Block RAM and FIFO in ECC configuration.	365.10	297.53	297.53	MHz

**Notes:**

1. T<sub>RCKO\_DOR</sub> includes T<sub>RCKO\_DOW</sub>, T<sub>RCKO\_DOPR</sub>, and T<sub>RCKO\_DOPW</sub> as well as the B port equivalent timing parameters.
2. These parameters also apply to synchronous FIFO with DO\_REG = 0.
3. T<sub>RCKO\_DO</sub> includes T<sub>RCKO\_DOP</sub> as well as the B port equivalent timing parameters.
4. These parameters also apply to multi-rate (asynchronous) and synchronous FIFO with DO\_REG = 1.
5. T<sub>RCKO\_FLAGS</sub> includes the following parameters: T<sub>RCKO\_AEMPTY</sub>, T<sub>RCKO\_AFULL</sub>, T<sub>RCKO\_EMPTY</sub>, T<sub>RCKO\_FULL</sub>, T<sub>RCKO\_RDERR</sub>, T<sub>RCKO\_WRERR</sub>.
6. T<sub>RCKO\_POINTERS</sub> includes both T<sub>RCKO\_RDCOUNT</sub> and T<sub>RCKO\_WRCOUNT</sub>.
7. The ADDR setup and hold must be met when EN is asserted (even when WE is deasserted). Otherwise, block RAM data corruption is possible.
8. These parameters include both A and B inputs as well as the parity inputs of A and B.
9. T<sub>RCO\_FLAGS</sub> includes the following flags: AEMPTY, AFULL, EMPTY, FULL, RDERR, WRERR, RDCOUNT, and WRCOUNT.
10. RDEN and WREN must be held Low prior to and during reset. The FIFO reset must be asserted for at least five positive clock edges of the slowest clock (WRCLK or RDCLK).

## DSP48E1 Switching Characteristics

Table 31: DSP48E1 Switching Characteristics

Symbol	Description	V <sub>CCINT</sub> Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
Setup and Hold Times of Data/Control Pins to the Input Register Clock					
T <sub>DSPDCK_A_AREG</sub> / T <sub>DSPCKD_A_AREG</sub>	A input to A register CLK.	0.30/ 0.13	0.37/ 0.14	0.37/ 0.14	ns
T <sub>DSPDCK_B_BREG</sub> / T <sub>DSPCKD_B_BREG</sub>	B input to B register CLK.	0.38/ 0.16	0.45/ 0.18	0.45/ 0.18	ns
T <sub>DSPDCK_C_CREG</sub> / T <sub>DSPCKD_C_CREG</sub>	C input to C register CLK.	0.20/ 0.19	0.24/ 0.21	0.24/ 0.21	ns
T <sub>DSPDCK_D_DREG</sub> / T <sub>DSPCKD_D_DREG</sub>	D input to D register CLK.	0.32/ 0.27	0.42/ 0.27	0.42/ 0.27	ns
T <sub>DSPDCK_ACIN_AREG</sub> / T <sub>DSPCKD_ACIN_AREG</sub>	ACIN input to A register CLK.	0.27/ 0.13	0.32/ 0.14	0.32/ 0.14	ns
T <sub>DSPDCK_BCIN_BREG</sub> / T <sub>DSPCKD_BCIN_BREG</sub>	BCIN input to B register CLK.	0.29/ 0.16	0.36/ 0.18	0.36/ 0.18	ns
Setup and Hold Times of Data Pins to the Pipeline Register Clock					
T <sub>DSPDCK_{A, B}_MREG_MULT</sub> / T <sub>DSPCKD_{A, B}_MREG_MULT</sub>	{A, B} input to M register CLK using multiplier.	2.76/ -0.01	3.29/ -0.01	3.29/ -0.01	ns
T <sub>DSPDCK_{A, D}_ADREG</sub> / T <sub>DSPCKD_{A, D}_ADREG</sub>	{A, D} input to AD register CLK.	1.48/ -0.02	1.76/ -0.02	1.76/ -0.02	ns
Setup and Hold Times of Data/Control Pins to the Output Register Clock					
T <sub>DSPDCK_{A, B}_PREG_MULT</sub> / T <sub>DSPCKD_{A, B}_PREG_MULT</sub>	{A, B} input to P register CLK using multiplier.	4.60/ -0.28	5.48/ -0.28	5.48/ -0.28	ns
T <sub>DSPDCK_D_PREG_MULT</sub> / T <sub>DSPCKD_D_PREG_MULT</sub>	D input to P register CLK using multiplier.	4.50/ -0.73	5.35/ -0.73	5.35/ -0.73	ns
T <sub>DSPDCK_{A, B}_PREG</sub> / T <sub>DSPCKD_{A, B}_PREG</sub>	A or B input to P register CLK not using multiplier.	1.98/ -0.28	2.35/ -0.28	2.35/ -0.28	ns
T <sub>DSPDCK_C_PREG</sub> / T <sub>DSPCKD_C_PREG</sub>	C input to P register CLK not using multiplier.	1.76/ -0.26	2.10/ -0.26	2.10/ -0.26	ns
T <sub>DSPDCK_PCIN_PREG</sub> / T <sub>DSPCKD_PCIN_PREG</sub>	PCIN input to P register CLK.	1.51/ -0.15	1.80/ -0.15	1.80/ -0.15	ns
Setup and Hold Times of the CE Pins					
T <sub>DSPDCK_{CEA;CEB}_{AREG;BREG}</sub> / T <sub>DSPCKD_{CEA;CEB}_{AREG;BREG}</sub>	{CEA; CEB} input to {A; B} register CLK.	0.42/ 0.08	0.52/ 0.11	0.52/ 0.11	ns
T <sub>DSPDCK_CEC_CREG</sub> / T <sub>DSPCKD_CEC_CREG</sub>	CEC input to C register CLK.	0.34/ 0.11	0.42/ 0.13	0.42/ 0.13	ns
T <sub>DSPDCK_CED_DREG</sub> / T <sub>DSPCKD_CED_DREG</sub>	CED input to D register CLK.	0.43/ -0.03	0.52/ -0.03	0.52/ -0.03	ns



Table 31: DSP48E1 Switching Characteristics (Cont'd)

Symbol	Description	V <sub>CCINT</sub> Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
T <sub>DSPDCK_CEM_MREG</sub> / T <sub>DSPCKD_CEM_MREG</sub>	CEM input to M register CLK.	0.21/ 0.20	0.27/ 0.23	0.27/ 0.23	ns
T <sub>DSPDCK_CEP_PREG</sub> / T <sub>DSPCKD_CEP_PREG</sub>	CEP input to P register CLK.	0.43/ 0.01	0.53/ 0.01	0.53/ 0.01	ns
<b>Setup and Hold Times of the RST Pins</b>					
T <sub>DSPDCK_{RSTA; RSTB}_{AREG; BREG}</sub> / T <sub>DSPCKD_{RSTA; RSTB}_{AREG; BREG}</sub>	{RSTA, RSTB} input to {A, B} register CLK.	0.46/ 0.13	0.55/ 0.15	0.55/ 0.15	ns
T <sub>DSPDCK_RSTC_CREG</sub> / T <sub>DSPCKD_RSTC_CREG</sub>	RSTC input to C register CLK.	0.08/ 0.11	0.09/ 0.12	0.09/ 0.12	ns
T <sub>DSPDCK_RSTD_DREG</sub> / T <sub>DSPCKD_RSTD_DREG</sub>	RSTD input to D register CLK	0.50/ 0.08	0.59/ 0.09	0.59/ 0.09	ns
T <sub>DSPDCK_RSTM_MREG</sub> / T <sub>DSPCKD_RSTM_MREG</sub>	RSTM input to M register CLK	0.23/ 0.24	0.27/ 0.28	0.27/ 0.28	ns
T <sub>DSPDCK_RSTP_PREG</sub> / T <sub>DSPCKD_RSTP_PREG</sub>	RSTP input to P register CLK	0.30/ 0.01	0.35/ 0.01	0.35/ 0.01	ns
<b>Combinatorial Delays from Input Pins to Output Pins</b>					
T <sub>DSPDO_A_CARRYOUT_MULT</sub>	A input to CARRYOUT output using multiplier.	4.35	5.18	5.18	ns
T <sub>DSPDO_D_P_MULT</sub>	D input to P output using multiplier.	4.26	5.07	5.07	ns
T <sub>DSPDO_B_P</sub>	B input to P output not using multiplier.	1.75	2.08	2.08	ns
T <sub>DSPDO_C_P</sub>	C input to P output.	1.53	1.82	1.82	ns
<b>Combinatorial Delays from Input Pins to Cascading Output Pins</b>					
T <sub>DSPDO_{A; B}_{ACOUT; BCOUT}</sub>	{A, B} input to {ACOUT, BCOUT} output.	0.63	0.74	0.74	ns
T <sub>DSPDO_{A, B}_CARRYCASCOUT_MULT</sub>	{A, B} input to CARRYCASCOUT output using multiplier.	4.65	5.54	5.54	ns
T <sub>DSPDO_D_CARRYCASCOUT_MULT</sub>	D input to CARRYCASCOUT output using multiplier.	4.54	5.40	5.40	ns
T <sub>DSPDO_{A, B}_CARRYCASCOUT</sub>	{A, B} input to CARRYCASCOUT output not using multiplier.	2.03	2.41	2.41	ns
T <sub>DSPDO_C_CARRYCASCOUT</sub>	C input to CARRYCASCOUT output.	1.81	2.15	2.15	ns
<b>Combinatorial Delays from Cascading Input Pins to All Output Pins</b>					
T <sub>DSPDO_ACIN_P_MULT</sub>	ACIN input to P output using multiplier.	4.19	5.00	5.00	ns
T <sub>DSPDO_ACIN_P</sub>	ACIN input to P output not using multiplier.	1.57	1.88	1.88	ns
T <sub>DSPDO_ACIN_ACOUT</sub>	ACIN input to ACOUT output.	0.44	0.53	0.53	ns
T <sub>DSPDO_ACIN_CARRYCASCOUT_MULT</sub>	ACIN input to CARRYCASCOUT output using multiplier.	4.47	5.33	5.33	ns
T <sub>DSPDO_ACIN_CARRYCASCOUT</sub>	ACIN input to CARRYCASCOUT output not using multiplier.	1.85	2.21	2.21	ns
T <sub>DSPDO_PCIN_P</sub>	PCIN input to P output.	1.28	1.52	1.52	ns

Table 31: DSP48E1 Switching Characteristics (Cont'd)

Symbol	Description	V <sub>CCINT</sub> Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
T <sub>DSPDO_PCIN_CARRYCASCOUT</sub>	PCIN input to CARRYCASCOUT output.	1.56	1.85	1.85	ns
<b>Clock to Outs from Output Register Clock to Output Pins</b>					
T <sub>DSPCKO_P_PREG</sub>	CLK PREG to P output.	0.37	0.44	0.44	ns
T <sub>DSPCKO_CARRYCASCOUT_PREG</sub>	CLK PREG to CARRYCASCOUT output.	0.59	0.69	0.69	ns
<b>Clock to Outs from Pipeline Register Clock to Output Pins</b>					
T <sub>DSPCKO_P_MREG</sub>	CLK MREG to P output.	1.93	2.31	2.31	ns
T <sub>DSPCKO_CARRYCASCOUT_MREG</sub>	CLK MREG to CARRYCASCOUT output.	2.21	2.64	2.64	ns
T <sub>DSPCKO_P_ADREG_MULT</sub>	CLK ADREG to P output using multiplier.	3.10	3.69	3.69	ns
T <sub>DSPCKO_CARRYCASCOUT_ADREG_MULT</sub>	CLK ADREG to CARRYCASCOUT output using multiplier.	3.38	4.02	4.02	ns
<b>Clock to Outs from Input Register Clock to Output Pins</b>					
T <sub>DSPCKO_P_AREG_MULT</sub>	CLK AREG to P output using multiplier.	4.51	5.37	5.37	ns
T <sub>DSPCKO_P_BREG</sub>	CLK BREG to P output not using multiplier.	1.87	2.22	2.22	ns
T <sub>DSPCKO_P_CREG</sub>	CLK CREG to P output not using multiplier.	1.93	2.30	2.30	ns
T <sub>DSPCKO_P_DREG_MULT</sub>	CLK DREG to P output using multiplier.	4.48	5.32	5.32	ns
<b>Clock to Outs from Input Register Clock to Cascading Output Pins</b>					
T <sub>DSPCKO_{ACOUT; BCOUT}_{AREG; BREG}</sub>	CLK (ACOUT, BCOUT) to {A,B} register output.	0.73	0.87	0.87	ns
T <sub>DSPCKO_CARRYCASCOUT_{AREG; BREG}_MULT</sub>	CLK (AREG, BREG) to CARRYCASCOUT output using multiplier.	4.79	5.70	5.70	ns
T <sub>DSPCKO_CARRYCASCOUT_BREG</sub>	CLK BREG to CARRYCASCOUT output not using multiplier.	2.15	2.55	2.55	ns
T <sub>DSPCKO_CARRYCASCOUT_DREG_MULT</sub>	CLK DREG to CARRYCASCOUT output using multiplier.	4.76	5.65	5.65	ns
T <sub>DSPCKO_CARRYCASCOUT_CREG</sub>	CLK CREG to CARRYCASCOUT output.	2.21	2.63	2.63	ns
<b>Maximum Frequency</b>					
F <sub>MAX</sub>	With all registers used.	550.66	464.25	464.25	MHz
F <sub>MAX_PATDET</sub>	With pattern detector.	465.77	392.93	392.93	MHz
F <sub>MAX_MULT_NOMREG</sub>	Two register multiply without MREG.	305.62	257.47	257.47	MHz
F <sub>MAX_MULT_NOMREG_PATDET</sub>	Two register multiply without MREG with pattern detect.	277.62	233.92	233.92	MHz
F <sub>MAX_PREADD_MULT_NOADREG</sub>	Without ADREG.	346.26	290.44	290.44	MHz
F <sub>MAX_PREADD_MULT_NOADREG_PATDET</sub>	Without ADREG with pattern detect.	346.26	290.44	290.44	MHz
F <sub>MAX_NOPIPELINEREG</sub>	Without pipeline registers (MREG, ADREG).	227.01	190.69	190.69	MHz
F <sub>MAX_NOPIPELINEREG_PATDET</sub>	Without pipeline registers (MREG, ADREG) with pattern detect.	211.15	177.43	177.43	MHz

## Clock Buffers and Networks

Table 32: Global Clock Switching Characteristics (Including BUFGCTRL)

Symbol	Description	V <sub>CCINT</sub> Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
T <sub>BCCCK_CE</sub> /T <sub>BCCCK_CE</sub> <sup>(1)</sup>	CE pins setup/hold.	0.13/0.40	0.16/0.41	0.16/0.41	ns
T <sub>BCCCK_S</sub> /T <sub>BCCCK_S</sub> <sup>(1)</sup>	S pins setup/hold.	0.13/0.40	0.16/0.41	0.16/0.41	ns
T <sub>BCCCKO_O</sub> <sup>(2)</sup>	BUFGCTRL delay from I0/I1 to O.	0.09	0.10	0.10	ns
<b>Maximum Frequency</b>					
F <sub>MAX_BUFG</sub>	Global clock tree (BUFG).	628.00	464.00	464.00	MHz

**Notes:**

1. T<sub>BCCCK\_CE</sub> and T<sub>BCCCK\_CE</sub> must be satisfied to assure glitch-free operation of the global clock when switching between clocks. These parameters do not apply to the BUFGMUX primitive that assures glitch-free operation. The other global clock setup and hold times are optional; only needing to be satisfied if device operation requires simulation matches on a cycle-for-cycle basis when switching between clocks.
2. T<sub>BGCKO\_O</sub> (BUFG delay from I0 to O) values are the same as T<sub>BCCCKO\_O</sub> values.

Table 33: Input/Output Clock Switching Characteristics (BUFIO)

Symbol	Description	V <sub>CCINT</sub> Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
T <sub>BIOCKO_O</sub>	Clock to out delay from I to O.	1.26	1.54	1.54	ns
<b>Maximum Frequency</b>					
F <sub>MAX_BUFIO</sub>	I/O clock tree (BUFIO).	680.00	600.00	600.00	MHz

Table 34: Regional Clock Buffer Switching Characteristics (BUFR)

Symbol	Description	V <sub>CCINT</sub> Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
T <sub>BRCKO_O</sub>	Clock to out delay from I to O.	0.76	0.99	0.99	ns
T <sub>BRCKO_O_BYP</sub>	Clock to out delay from I to O with Divide Bypass attribute set.	0.39	0.52	0.52	ns
T <sub>BRDO_O</sub>	Propagation delay from CLR to O.	0.85	1.09	1.09	ns
<b>Maximum Frequency</b>					
F <sub>MAX_BUFR</sub> <sup>(1)</sup>	Regional clock tree (BUFR).	375.00	315.00	315.00	MHz

**Notes:**

1. The maximum input frequency to the BUFR is the BUFIO F<sub>MAX</sub> frequency.

Table 35: Horizontal Clock Buffer Switching Characteristics (BUFH)

Symbol	Description	V <sub>CCINT</sub> Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
T <sub>BHCKO_O</sub>	BUFH delay from I to O.	0.11	0.13	0.13	ns
T <sub>BHCKC_CE</sub> / T <sub>BHCKC_CE</sub>	CE pin setup and hold.	0.22/0.15	0.28/0.21	0.28/0.21	ns
<b>Maximum Frequency</b>					
F <sub>MAX_BUFH</sub>	Horizontal clock buffer (BUFH).	628.00	464.00	464.00	MHz

Table 36: Duty Cycle Distortion and Clock-Tree Skew

Symbol	Description	Device	V <sub>CCINT</sub> Operating Voltage and Speed Grade			Units
			1.0V		0.95V	
			-2	-1	-1L	
T <sub>DCD_CLK</sub>	Global clock tree duty-cycle distortion. <sup>(1)</sup>	All	0.20	0.20	0.20	ns
T <sub>CKSKEW</sub>	Global clock tree skew. <sup>(2)</sup>	XC7S6	0.05	0.06	0.06	ns
		XC7S15	0.05	0.06	0.06	ns
		XC7S25	0.26	0.26	0.26	ns
		XC7S50	0.26	0.26	0.26	ns
		XC7S75	0.33	0.36	0.36	ns
		XC7S100	0.33	0.36	0.36	ns
T <sub>DCD_BUFIO</sub>	I/O clock tree duty cycle distortion.	All	0.14	0.14	0.14	ns
T <sub>BUFIOSKEW</sub>	I/O clock tree skew across one clock region.	All	0.03	0.03	0.03	ns
T <sub>DCD_BUFR</sub>	Regional clock tree duty cycle distortion.	All	0.18	0.18	0.18	ns

**Notes:**

- These parameters represent the worst-case duty cycle distortion observable at the I/O flip flops. For all I/O standards, IBIS can be used to calculate any additional duty cycle distortion that might be caused by asymmetrical rise/fall times.
- The T<sub>CKSKEW</sub> value represents the worst-case clock-tree skew observable between sequential I/O elements. Significantly less clock-tree skew exists for I/O registers that are close to each other and fed by the same or adjacent clock-tree branches. Use the Xilinx timing analysis tools to evaluate clock skew specific to your application.

## MMCM Switching Characteristics

Table 37: MMCM Specification

Symbol	Description	V <sub>CCINT</sub> Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
MMCM_F <sub>INMAX</sub>	Maximum input clock frequency.	800.00	800.00	800.00	MHz
MMCM_F <sub>INMIN</sub>	Minimum input clock frequency.	10.00	10.00	10.00	MHz
MMCM_F <sub>INJITTER</sub>	Maximum input clock period jitter.	< 20% of clock input period or 1 ns Max			
MMCM_F <sub>INDUTY</sub>	Allowable input duty cycle: 10—49 MHz.	25	25	25	%
	Allowable input duty cycle: 50—199 MHz.	30	30	30	%
	Allowable input duty cycle: 200—399 MHz.	35	35	35	%
	Allowable input duty cycle: 400—499 MHz.	40	40	40	%
	Allowable input duty cycle: > 500 MHz.	45	45	45	%
MMCM_F <sub>MIN_PSCLK</sub>	Minimum dynamic phase-shift clock frequency.	0.01	0.01	0.01	MHz
MMCM_F <sub>MAX_PSCLK</sub>	Maximum dynamic phase-shift clock frequency.	500.00	450.00	450.00	MHz
MMCM_F <sub>VCOMIN</sub>	Minimum MMCM VCO frequency.	600.00	600.00	600.00	MHz
MMCM_F <sub>VCOMAX</sub>	Maximum MMCM VCO frequency.	1440.00	1200.00	1200.00	MHz
MMCM_F <sub>BANDWIDTH</sub>	Low MMCM bandwidth at typical. <sup>(1)</sup>	1.00	1.00	1.00	MHz
	High MMCM bandwidth at typical. <sup>(1)</sup>	4.00	4.00	4.00	MHz
MMCM_T <sub>STATPHAOFFSET</sub>	Static phase offset of the MMCM outputs. <sup>(2)</sup>	0.12	0.12	0.12	ns
MMCM_T <sub>OUTJITTER</sub>	MMCM output jitter.	Note 3			
MMCM_T <sub>OUTDUTY</sub>	MMCM output clock duty-cycle precision. <sup>(4)</sup>	0.20	0.20	0.20	ns
MMCM_T <sub>LOCKMAX</sub>	MMCM maximum lock time.	100.00	100.00	100.00	μs
MMCM_F <sub>OUTMAX</sub>	MMCM maximum output frequency.	800.00	800.00	800.00	MHz
MMCM_F <sub>OUTMIN</sub>	MMCM minimum output frequency. <sup>(5)(6)</sup>	4.69	4.69	4.69	MHz
MMCM_T <sub>EXTFDVAR</sub>	External clock feedback variation.	< 20% of clock input period or 1 ns Max			
MMCM_RST <sub>MINPULSE</sub>	Minimum reset pulse width.	5.00	5.00	5.00	ns
MMCM_F <sub>PFDMAX</sub>	Maximum frequency at the phase frequency detector.	500.00	450.00	450.00	MHz
MMCM_F <sub>PFDMIN</sub>	Minimum frequency at the phase frequency detector.	10.00	10.00	10.00	MHz
MMCM_T <sub>FBDELAY</sub>	Maximum delay in the feedback path.	3 ns Max or one CLKIN cycle			
MMCM Switching Characteristics Setup and Hold					
T <sub>MMCMDCK_PSEN</sub> / T <sub>MMCMCKD_PSEN</sub>	Setup and hold of phase-shift enable.	1.04/0.00	1.04/0.00	1.04/0.00	ns

Table 37: MMCM Specification (Cont'd)

Symbol	Description	V <sub>CCINT</sub> Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
T <sub>MMCMDCK_PSINCDEC</sub> / T <sub>MMCMCKD_PSINCDEC</sub>	Setup and hold of phase-shift increment/decrement.	1.04/0.00	1.04/0.00	1.04/0.00	ns
T <sub>MMCMCKO_PSDONE</sub>	Phase shift clock-to-out of PSDONE.	0.68	0.81	0.81	ns
<b>Dynamic Reconfiguration Port (DRP) for MMCM Before and After DCLK</b>					
T <sub>MMCMDCK_DADDR</sub> / T <sub>MMCMCKD_DADDR</sub>	DADDR setup/hold.	1.40/0.15	1.63/0.15	1.63/0.15	ns, Min
T <sub>MMCMDCK_DI</sub> / T <sub>MMCMCKD_DI</sub>	DI setup/hold.	1.40/0.15	1.63/0.15	1.63/0.15	ns, Min
T <sub>MMCMDCK_DEN</sub> / T <sub>MMCMCKD_DEN</sub>	DEN setup/hold.	1.97/0.00	2.29/0.00	2.29/0.00	ns, Min
T <sub>MMCMDCK_DWE</sub> / T <sub>MMCMCKD_DWE</sub>	DWE setup/hold.	1.40/0.15	1.63/0.15	1.63/0.15	ns, Min
T <sub>MMCMCKO_DRDY</sub>	CLK to out of DRDY.	0.72	0.99	0.99	ns, Max
F <sub>DCK</sub>	DCLK frequency.	200.00	200.00	200.00	MHz, Max

**Notes:**

1. The MMCM does not filter typical spread-spectrum input clocks because they are usually far below the bandwidth filter frequencies.
2. The static offset is measured between any MMCM outputs with identical phase.
3. Values for this parameter are available in the *Clocking Wizard* [Ref 7].
4. Includes global clock buffer.
5. Calculated as F<sub>VCO</sub>/128 assuming output duty cycle is 50%.
6. When CLKOUT4\_CASCADE = TRUE, MMCM\_F<sub>OUTMIN</sub> is 0.036 MHz.

## PLL Switching Characteristics

Table 38: PLL Specification

Symbol	Description	V <sub>CCINT</sub> Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
PLL_F <sub>INMAX</sub>	Maximum input clock frequency.	800.00	800.00	800.00	MHz
PLL_F <sub>INMIN</sub>	Minimum input clock frequency.	19.00	19.00	19.00	MHz
PLL_F <sub>INJITTER</sub>	Maximum input clock period jitter.	< 20% of clock input period or 1 ns Max			
PLL_F <sub>INDUTY</sub>	Allowable input duty cycle: 19—49 MHz.	25	25	25	%
	Allowable input duty cycle: 50—199 MHz.	30	30	30	%
	Allowable input duty cycle: 200—399 MHz.	35	35	35	%
	Allowable input duty cycle: 400—499 MHz.	40	40	40	%
	Allowable input duty cycle: >500 MHz.	45	45	45	%
PLL_F <sub>VCOMIN</sub>	Minimum PLL VCO frequency.	800.00	800.00	800.00	MHz
PLL_F <sub>VCOMAX</sub>	Maximum PLL VCO frequency.	1866.00	1600.00	1600.00	MHz

Table 38: PLL Specification

Symbol	Description	V <sub>CCINT</sub> Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
PLL_F <sub>BANDWIDTH</sub>	Low PLL bandwidth at typical.	1.00	1.00	1.00	MHz
	High PLL bandwidth at typical. <sup>(1)</sup>	4.00	4.00	4.00	MHz
PLL_T <sub>STATPHAOFFSET</sub>	Static phase offset of the PLL outputs. <sup>(2)</sup>	0.12	0.12	0.12	ns
PLL_T <sub>OUTJITTER</sub>	PLL output jitter.	Note 3			
PLL_T <sub>OUTDUTY</sub>	PLL output clock duty-cycle precision. <sup>(4)</sup>	0.20	0.20	0.20	ns
PLL_T <sub>LOCKMAX</sub>	PLL maximum lock time.	100.00	100.00	100.00	μs
PLL_F <sub>OUTMAX</sub>	PLL maximum output frequency.	800.00	800.00	800.00	MHz
PLL_F <sub>OUTMIN</sub>	PLL minimum output frequency. <sup>(5)</sup>	6.25	6.25	6.25	MHz
PLL_T <sub>EXTFDVAR</sub>	External clock feedback variation.	< 20% of clock input period or 1 ns Max			
PLL_RST <sub>MINPULSE</sub>	Minimum reset pulse width.	5.00	5.00	5.00	ns
PLL_F <sub>PFDMAX</sub>	Maximum frequency at the phase frequency detector.	500.00	450.00	450.00	MHz
PLL_F <sub>PFDMIN</sub>	Minimum frequency at the phase frequency detector.	19.00	19.00	19.00	MHz
PLL_T <sub>FBDELAY</sub>	Maximum delay in the feedback path.	3 ns Max or one CLKIN cycle			
Dynamic Reconfiguration Port (DRP) for PLL Before and After DCLK					
T <sub>PLLDCK_DADDR</sub> / T <sub>PLLCKD_DADDR</sub>	Setup and hold of D address.	1.40/0.15	1.63/0.15	1.63/0.15	ns, Min
T <sub>PLLDCK_DI</sub> / T <sub>PLLCKD_DI</sub>	Setup and hold of D input.	1.40/0.15	1.63/0.15	1.63/0.15	ns, Min
T <sub>PLLDCK_DEN</sub> / T <sub>PLLCKD_DEN</sub>	Setup and hold of D enable.	1.97/0.00	2.29/0.00	2.29/0.00	ns, Min
T <sub>PLLDCK_DWE</sub> / T <sub>PLLCKD_DWE</sub>	Setup and hold of D write enable.	1.40/0.15	1.63/0.15	1.63/0.15	ns, Min
T <sub>PLLCKO_DRDY</sub>	CLK to out of DRDY.	0.72	0.99	0.99	ns, Max
F <sub>DCK</sub>	DCLK frequency.	200.00	200.00	200.00	MHz, Max

**Notes:**

1. The PLL does not filter typical spread-spectrum input clocks because they are usually far below the bandwidth filter frequencies.
2. The static offset is measured between any PLL outputs with identical phase.
3. Values for this parameter are available in the *Clocking Wizard* [Ref 7].
4. Includes global clock buffer.
5. Calculated as FVCO/128 assuming output duty cycle is 50%.

## Device Pin-to-Pin Output Parameter Guidelines

**Table 39: Clock-Capable Clock Input to Output Delay Without MMCM/PLL (Near Clock Region)<sup>(1)</sup>**

Symbol	Description	Device	V <sub>CCINT</sub> Operating Voltage and Speed Grade			Units
			1.0V		0.95V	
			-2	-1	-1L	
SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, <i>without</i> MMCM/PLL.						
T <sub>ICKOF</sub>	Clock-capable clock input and OUTFF at pins/banks closest to the BUFGs <i>without</i> MMCM/PLL (near clock region). <sup>(2)</sup>	XC7S6	5.55	6.50	6.50	ns
		XC7S15	5.55	6.50	6.50	ns
		XC7S25	5.55	6.44	6.44	ns
		XC7S50	5.71	6.62	6.62	ns
		XC7S75	5.73	6.71	6.71	ns
		XC7S100	5.73	6.71	6.71	ns

**Notes:**

1. This table lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. Refer to the *Die Level Bank Numbering Overview* section of the *7 Series FPGA Packaging and Pinout Specification* (UG475) [Ref 3].

**Table 40: Clock-Capable Clock Input to Output Delay Without MMCM/PLL (Far Clock Region)<sup>(1)</sup>**

Symbol	Description	Device	V <sub>CCINT</sub> Operating Voltage and Speed Grade			Units
			1.0V		0.95V	
			-2	-1	-1L	
SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, <i>without</i> MMCM/PLL.						
T <sub>ICKOFFAR</sub>	Clock-capable clock input and OUTFF at pins/banks farthest from the BUFGs <i>without</i> MMCM/PLL (far clock region). <sup>(2)</sup>	XC7S6	5.55	6.50	6.50	ns
		XC7S15	5.55	6.50	6.50	ns
		XC7S25	5.55	6.44	6.44	ns
		XC7S50	5.71	6.62	6.62	ns
		XC7S75	6.01	7.02	7.02	ns
		XC7S100	6.01	7.02	7.02	ns

**Notes:**

1. This table lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. Refer to the *Die Level Bank Numbering Overview* section of the *7 Series FPGA Packaging and Pinout Specification* (UG475) [Ref 3].



Table 41: Clock-Capable Clock Input to Output Delay With MMCM<sup>(1)</sup>

Symbol	Description	Device	V <sub>CCINT</sub> Operating Voltage and Speed Grade			Units
			1.0V		0.95V	
			-2	-1	-1L	
SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, <i>with</i> MMCM.						
T <sub>ICKOFMMCMCC</sub>	Clock-capable clock input and OUTFF <i>with</i> MMCM. <sup>(2)</sup>	XC7S6	1.03	1.03	1.03	ns
		XC7S15	1.03	1.03	1.03	ns
		XC7S25	1.00	1.00	1.00	ns
		XC7S50	1.00	1.00	1.00	ns
		XC7S75	1.00	1.00	1.00	ns
		XC7S100	1.00	1.00	1.00	ns

**Notes:**

1. This table lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. MMCM output jitter is already included in the timing calculation.

Table 42: Clock-Capable Clock Input to Output Delay With PLL<sup>(1)</sup>

Symbol	Description	Device	V <sub>CCINT</sub> Operating Voltage and Speed Grade			Units
			1.0V		0.95V	
			-2	-1	-1L	
SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, <i>with</i> PLL.						
T <sub>ICKOFPLLCC</sub>	Clock-capable clock input and OUTFF <i>with</i> PLL. <sup>(2)</sup>	XC7S6	0.85	0.85	0.85	ns
		XC7S15	0.85	0.85	0.85	ns
		XC7S25	0.83	0.83	0.83	ns
		XC7S50	0.83	0.83	0.83	ns
		XC7S75	0.83	0.83	0.83	ns
		XC7S100	0.83	0.83	0.83	ns

**Notes:**

1. This table lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. PLL output jitter is already included in the timing calculation.

Table 43: Pin-to-Pin, Clock-to-Out using BUFIO

Symbol	Description	V <sub>CCINT</sub> Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, with BUFIO.					
T <sub>ICKOFCS</sub>	Clock to out of I/O clock.	5.61	6.64	6.64	ns

## Device Pin-to-Pin Input Parameter Guidelines

All devices are 100% functionally tested. Values are expressed in nanoseconds unless otherwise noted.

Table 44: Global Clock Input Setup and Hold Without MMCM/PLL with ZHOLD\_DELAY on HR I/O Banks

Symbol	Description	Device	V <sub>CCINT</sub> Operating Voltage and Speed Grade			Units
			1.0V		0.95V	
			-2	-1	-1L	
Input Setup and Hold Time Relative to Global Clock Input Signal for SSTL15 Standard. <sup>(1)</sup>						
T <sub>PSFD</sub> / T <sub>PHFD</sub>	Full delay (legacy delay or default delay) global clock input and IFF <sup>(2)</sup> without MMCM/PLL with ZHOLD_DELAY on HR I/O banks.	XC7S6	2.76/−0.43	3.17/−0.43	3.17/−0.43	ns
		XC7S15	2.76/−0.43	3.17/−0.43	3.17/−0.43	ns
		XC7S25	2.66/−0.41	3.11/−0.41	3.11/−0.41	ns
		XC7S50	2.66/−0.41	3.11/−0.41	3.11/−0.41	ns
		XC7S75	2.91/−0.37	3.36/−0.37	3.36/−0.37	ns
		XC7S100	2.91/−0.37	3.36/−0.37	3.36/−0.37	ns

### Notes:

- Setup and hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the global clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the global clock input signal using the fastest process, lowest temperature, and highest voltage.
- IFF = Input flip-flop or latch.

Table 45: Clock-Capable Clock Input Setup and Hold With MMCM

Symbol	Description	Device	V <sub>CCINT</sub> Operating Voltage and Speed Grade			Units
			1.0V		0.95V	
			-2	-1	-1L	
Input Setup and Hold Time Relative to Global Clock Input Signal for SSTL15 Standard. <sup>(1)(2)</sup>						
T <sub>PSMMCMCC</sub> / T <sub>PHMMCMCC</sub>	No delay clock-capable clock input and IFF <sup>(3)</sup> with MMCM.	XC7S6	2.73/−0.59	3.27/−0.59	3.27/−0.59	ns
		XC7S15	2.73/−0.59	3.27/−0.59	3.27/−0.59	ns
		XC7S25	2.69/−0.61	3.21/−0.61	3.21/−0.61	ns
		XC7S50	2.80/−0.62	3.35/−0.62	3.35/−0.62	ns
		XC7S75	2.81/−0.62	3.36/−0.62	3.36/−0.62	ns
		XC7S100	2.81/−0.62	3.36/−0.62	3.36/−0.62	ns

### Notes:

- Setup and hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the global clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the global clock input signal using the fastest process, lowest temperature, and highest voltage.
- Use IBIS to determine any duty-cycle distortion incurred using various standards.
- IFF = Input flip-flop or latch.

Table 46: Clock-Capable Clock Input Setup and Hold With PLL

Symbol	Description	Device	V <sub>CCINT</sub> Operating Voltage and Speed Grade			Units
			1.0V		0.95V	
			-2	-1	-1L	
Input Setup and Hold Time Relative to Clock-Capable Clock Input Signal for SSTL15 Standard. <sup>(1)(2)</sup>						
T <sub>PSPLLCC</sub> / T <sub>PHPLLCC</sub>	No delay clock-capable clock input and IFF <sup>(3)</sup> with PLL.	XC7S6	3.07/−0.17	3.69/−0.17	3.69/−0.17	ns
		XC7S15	3.07/−0.17	3.69/−0.17	3.69/−0.17	ns
		XC7S25	3.04/−0.19	3.63/−0.19	3.63/−0.19	ns
		XC7S50	3.15/−0.19	3.77/−0.19	3.77/−0.19	ns
		XC7S75	3.15/−0.19	3.78/−0.19	3.78/−0.19	ns
		XC7S100	3.15/−0.19	3.78/−0.19	3.78/−0.19	ns

**Notes:**

- Setup and hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the global clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the global clock input signal using the fastest process, lowest temperature, and highest voltage.
- Use IBIS to determine any duty-cycle distortion incurred using various standards.
- IFF = Input flip-flop or latch.

Table 47: Data Input Setup and Hold Times Relative to a Forwarded Clock Input Pin Using BUFIO

Symbol	Description	V <sub>CCINT</sub> Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
Input Setup and Hold Time Relative to a Forwarded Clock Input Pin Using BUFIO for SSTL15 Standard.					
T <sub>PSCS</sub> /T <sub>PHCS</sub>	Setup and hold of I/O clock.	-0.38/1.46	-0.38/1.73	-0.38/1.76	ns

Table 48: Sample Window

Symbol	Description	V <sub>CCINT</sub> Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
T <sub>SAMP</sub>	Sampling error at receiver pins. <sup>(1)</sup>	0.64	0.70	0.70	ns
T <sub>SAMP_BUFIO</sub>	Sampling error at receiver pins using BUFIO. <sup>(2)</sup>	0.40	0.46	0.46	ns

**Notes:**

- This parameter indicates the total sampling error of the Spartan-7 FPGAs DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the MMCM to capture the DDR input registers' edges of operation. These measurements include:
  - CLK0 MMCM jitter
  - MMCM accuracy (phase offset)
  - MMCM phase shift resolution
These measurements do not include package or clock tree skew.
- This parameter indicates the total sampling error of the Spartan-7 FPGAs DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the BUFIO clock network and IDELAY to capture the DDR input registers' edges of operation. These measurements do not include package or clock tree skew.

## Additional Package Parameter Guidelines

The parameters in this section provide the necessary values for calculating timing budgets for Spartan-7 FPGA clock transmitter and receiver data-valid windows.

Table 49: Package Skew<sup>(1)</sup>

Symbol	Description	Device	Package	Value	Units
T <sub>PKGSKEW</sub>	Package skew. <sup>(2)</sup>	XC7S6	CPGA196		ps
			CSGA225		ps
			FTGB196		ps
		XC7S15	CPGA196		ps
			CSGA225		ps
			FTGB196		ps
		XC7S25	CSGA225		ps
			CSGA324		ps
			FTGB196		ps
		XC7S50	CSGA324	80	ps
			FGGA484	110	ps
			FTGB196		ps
		XC7S75	FGGA484		ps
			FGGA676		ps
		XC7S100	FGGA484		ps
			FGGA676		ps

### Notes:

- Package delay information is available for these device/package combinations. This information can be used to deskew the package.
- These values represent the worst-case skew between any two SelectIO resources in the package: shortest delay to longest delay from die pad to ball.

# XADC Specifications

The *7 Series FPGAs Overview* (DS180) [Ref 1] lists the devices that contain a 7 series XADC dual 12-Bit 1 MSPS analog-to-digital converter.

Table 50: XADC Specifications

Parameter	Symbol	Comments/Conditions	Min	Typ	Max	Units
$V_{CCADC} = 1.8V \pm 5\%$ , $V_{REFP} = 1.25V$ , $V_{REFN} = 0V$ , $ADCCLK = 26\text{ MHz}$ , $-55^{\circ}\text{C} \leq T_j \leq 125^{\circ}\text{C}$ . Typical values at $T_j = +40^{\circ}\text{C}$ .						
<b>ADC Accuracy<sup>(1)</sup></b>						
Resolution			12	–	–	Bits
Integral nonlinearity <sup>(2)</sup>	INL	$-40^{\circ}\text{C} \leq T_j \leq 100^{\circ}\text{C}$	–	–	$\pm 2$	LSBs
		$-55^{\circ}\text{C} \leq T_j < -40^{\circ}\text{C}$ ; $100^{\circ}\text{C} < T_j \leq 125^{\circ}\text{C}$	–	–	$\pm 3$	LSBs
Differential nonlinearity	DNL	No missing codes, guaranteed monotonic.	–	–	$\pm 1$	LSBs
Offset error	Unipolar	$-40^{\circ}\text{C} \leq T_j \leq 100^{\circ}\text{C}$	–	–	$\pm 8$	LSBs
		$-55^{\circ}\text{C} \leq T_j < -40^{\circ}\text{C}$ ; $100^{\circ}\text{C} < T_j \leq 125^{\circ}\text{C}$	–	–	$\pm 12$	LSBs
	Bipolar	$-55^{\circ}\text{C} \leq T_j \leq 125^{\circ}\text{C}$	–	–	$\pm 4$	LSBs
Gain error			–	–	$\pm 0.5$	%
Offset matching			–	–	4	LSBs
Gain matching			–	–	0.3	%
Sample rate			–	–	1	MS/s
Signal to noise ratio <sup>(2)</sup>	SNR	$F_{SAMPLE} = 500\text{ KS/s}$ , $F_{IN} = 20\text{ kHz}$	60	–	–	dB
RMS code noise		External 1.25V reference.	–	–	2	LSBs
		On-chip reference.	–	3	–	LSBs
Total harmonic distortion <sup>(2)</sup>	THD	$F_{SAMPLE} = 500\text{ KS/s}$ , $F_{IN} = 20\text{ kHz}$	70	–	–	dB
<b>Analog Inputs<sup>(3)</sup></b>						
ADC input ranges		Unipolar operation.	0	–	1	V
		Bipolar operation.	–0.5	–	+0.5	V
		Unipolar common mode range (FS input).	0	–	+0.5	V
		Bipolar common mode range (FS input).	+0.5	–	+0.6	V
Maximum external channel input ranges		Adjacent analog channels set within these ranges should not corrupt measurements on adjacent channels.	–0.1	–	$V_{CCADC}$	V
Full-resolution bandwidth	FRBW	Auxiliary channel full resolution bandwidth.	250	–	–	kHz
<b>On-chip Sensors</b>						
Temperature sensor error		$-40^{\circ}\text{C} \leq T_j \leq 100^{\circ}\text{C}$	–	–	$\pm 4$	$^{\circ}\text{C}$
		$-55^{\circ}\text{C} \leq T_j < -40^{\circ}\text{C}$ ; $100^{\circ}\text{C} < T_j \leq 125^{\circ}\text{C}$	–	–	$\pm 6$	$^{\circ}\text{C}$
Supply sensor error		$-40^{\circ}\text{C} \leq T_j \leq 100^{\circ}\text{C}$	–	–	$\pm 1$	%
		$-55^{\circ}\text{C} \leq T_j < -40^{\circ}\text{C}$ ; $100^{\circ}\text{C} < T_j \leq 125^{\circ}\text{C}$	–	–	$\pm 2$	%

Table 50: XADC Specifications (Cont'd)

Parameter	Symbol	Comments/Conditions	Min	Typ	Max	Units
<b>Conversion Rate<sup>(4)</sup></b>						
Conversion time: continuous	$t_{\text{CONV}}$	Number of ADCCLK cycles.	26	–	32	Cycles
Conversion time: event	$t_{\text{CONV}}$	Number of CLK cycles.	–	–	21	Cycles
DRP clock frequency	DCLK	DRP clock frequency.	8	–	250	MHz
ADC clock frequency	ADCCLK	Derived from DCLK.	1	–	26	MHz
DCLK duty cycle			40	–	60	%
<b>XADC Reference<sup>(5)</sup></b>						
External reference	$V_{\text{REFP}}$	Externally supplied reference voltage.	1.20	1.25	1.30	V
On-chip reference		Ground $V_{\text{REFP}}$ pin to AGND, $-40^{\circ}\text{C} \leq T_j \leq 100^{\circ}\text{C}$	1.2375	1.25	1.2625	V
		Ground $V_{\text{REFP}}$ pin to AGND, $-55^{\circ}\text{C} \leq T_j < -40^{\circ}\text{C}; 100^{\circ}\text{C} < T_j \leq 125^{\circ}\text{C}$	1.225	1.25	1.275	V

**Notes:**

- Offset and gain errors are removed by enabling the XADC automatic gain calibration feature. The values are specified for when this feature is enabled.
- Only specified for bitstream option XADCEnhancedLinearity = ON.
- For a detailed description, see the ADC chapter in the *7 Series FPGAs and Zynq-7000 AP SoC XADC Dual 12-Bit 1 MSPS Analog-to-Digital Converter User Guide* (UG480) [Ref 8].
- For a detailed description, see the *Timing* chapter in the *7 Series FPGAs and Zynq-7000 AP SoC XADC Dual 12-Bit 1 MSPS Analog-to-Digital Converter User Guide* (UG480) [Ref 8].
- Any variation in the reference voltage from the nominal  $V_{\text{REFP}} = 1.25\text{V}$  and  $V_{\text{REFN}} = 0\text{V}$  will result in a deviation from the ideal transfer function. This also impacts the accuracy of the internal sensor measurements (i.e., temperature and power supply). However, for external ratiometric type applications allowing reference to vary by  $\pm 4\%$  is permitted.

# Configuration Switching Characteristics

Table 51: Configuration Switching Characteristics

Symbol	Description	V <sub>CCINT</sub> Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
Power-up Timing Characteristics					
T <sub>PL</sub> <sup>(1)</sup>	Program latency.	5.00	5.00	5.00	ms, Max
T <sub>POR</sub> <sup>(2)</sup>	Power-on reset (50 ms ramp rate time).	10/50	10/50	10/50	ms, Min/Max
	Power-on reset (1 ms ramp rate time).	10/35	10/35	10/35	ms, Min/Max
T <sub>PROGRAM</sub>	Program pulse width.	250.00	250.00	250.00	ns, Min
CCLK Output (Master Mode)					
T <sub>ICCK</sub>	Master CCLK output delay.	150.00	150.00	150.00	ns, Min
T <sub>MCCKL</sub>	Master CCLK clock Low time duty cycle.	40/60	40/60	40/60	%, Min/Max
T <sub>MCCKH</sub>	Master CCLK clock High time duty cycle.	40/60	40/60	40/60	%, Min/Max
F <sub>MCCK</sub>	Master CCLK frequency.	100.00	100.00	100.00	MHz, Max
	Master CCLK frequency for AES encrypted x16. <sup>(2)</sup>	50.00	50.00	50.00	MHz, Max
F <sub>MCCK_START</sub>	Master CCLK frequency at start of configuration.	3.00	3.00	3.00	MHz, Typ
F <sub>MCCKTOL</sub>	Frequency tolerance, master mode with respect to nominal CCLK.	±50	±50	±50	%, Max
CCLK Input (Slave Modes)					
T <sub>SCCKL</sub>	Slave CCLK clock minimum Low time.	2.50	2.50	2.50	ns, Min
T <sub>SCCKH</sub>	Slave CCLK clock minimum High time.	2.50	2.50	2.50	ns, Min
F <sub>SCCK</sub>	Slave CCLK frequency.	100.00	100.00	100.00	MHz, Max
EMCCLK Input (Master Mode)					
T <sub>EMCCKL</sub>	External master CCLK Low time.	2.50	2.50	2.50	ns, Min
T <sub>EMCCKH</sub>	External master CCLK High time.	2.50	2.50	2.50	ns, Min
F <sub>EMCCK</sub>	External master CCLK frequency.	100.00	100.00	100.00	MHz, Max
Internal Configuration Access Port					
F <sub>ICAPCK</sub>	Internal configuration access port (ICAPE2) clock frequency.	100.00	100.00	100.00	MHz, Max
Master/Slave Serial Mode Programming Switching					
T <sub>DCCK</sub> / T <sub>CCKD</sub>	D <sub>IN</sub> setup/hold.	4.00/0.00	4.00/0.00	4.00/0.00	ns, Min
T <sub>CCO</sub>	D <sub>OUT</sub> clock to out.	8.00	8.00	8.00	ns, Max
SelectMAP Mode Programming Switching					
T <sub>SMDCK</sub> / T <sub>SMCKD</sub>	D[31:00] setup/hold.	4.00/0.00	4.00/0.00	4.00/0.00	ns, Min

Table 51: Configuration Switching Characteristics (Cont'd)

Symbol	Description	V <sub>CCINT</sub> Operating Voltage and Speed Grade			Units
		1.0V		0.95V	
		-2	-1	-1L	
T <sub>SMCSCCK</sub> / T <sub>SMCCKCS</sub>	CSI_B setup/hold.	4.00/0.00	4.00/0.00	4.00/0.00	ns, Min
T <sub>SMWCCK</sub> / T <sub>SMCCKW</sub>	RDWR_B setup/hold.	10.00/0.00	10.00/0.00	10.00/0.00	ns, Min
T <sub>SMCKCSO</sub>	CSO_B clock to out (330 $\Omega$ pull-up resistor required).	7.00	7.00	7.00	ns, Max
T <sub>SMCO</sub>	D[31:00] clock to out in readback.	8.00	8.00	8.00	ns, Max
F <sub>RBCK</sub>	Readback frequency.	100.00	100.00	100.00	MHz, Max
<b>Boundary-Scan Port Timing Specifications</b>					
T <sub>TAPTCK</sub> / T <sub>TCKTAP</sub>	TMS and TDI setup/hold.	3.00/2.00	3.00/2.00	3.00/2.00	ns, Min
T <sub>TCKTDO</sub>	TCK falling edge to TDO output.	7.00	7.00	7.00	ns, Max
F <sub>TCK</sub>	TCK frequency.	66.00	66.00	66.00	MHz, Max
<b>SPI Flash Master Mode Programming Switching</b>					
T <sub>SPIDCC</sub> / T <sub>SPICCD</sub>	D[03:00] setup/hold.	3.00/0.00	3.00/0.00	3.00/0.00	ns, Min
T <sub>SPICCM</sub>	MOSI clock to out.	8.00	8.00	8.00	ns, Max
T <sub>SPICFC</sub>	FCS_B clock to out.	8.00	8.00	8.00	ns, Max
<b>STARTUPE2 Ports</b>					
T <sub>USRCCLKO</sub>	STARTUPE2 USRCCLKO input to CCLK output.	0.50/6.70	0.50/7.50	0.50/7.50	ns, Min/Max
F <sub>CFGMCLK</sub>	STARTUPE2 CFGMCLK output frequency.	65.00	65.00	65.00	MHz, Typ
F <sub>CFGMCLKTOL</sub>	STARTUPE2 CFGMCLK output frequency tolerance.	$\pm 50$	$\pm 50$	$\pm 50$	%, Max
<b>Device DNA Access Port</b>					
F <sub>DNACK</sub>	DNA access port (DNA_PORT).	100.00	100.00	100.00	MHz, Max

**Notes:**

- To support longer delays in configuration, use the design solutions described in the *7 Series FPGA Configuration User Guide* (UG470) [Ref 9].
- See the *7 Series FPGAs Overview* (DS180) [Ref 1] for a list of devices that support bitstream encryption.



## eFUSE Programming Conditions

Table 52 lists the programming conditions specifically for eFUSE. For more information, see the *7 Series FPGA Configuration User Guide* (UG470) [Ref 9].

Table 52: eFUSE Programming Conditions<sup>(1)</sup>

Symbol	Description	Min	Typ	Max	Units
$I_{FS}$	$V_{CCAUX}$ supply current	–	–	115	mA
$T_j$	Temperature range	15	–	125	°C

### Notes:

1. The FPGA must not be configured during eFUSE programming.

## References

1. *7 Series FPGAs Overview* (DS180)
2. *7 Series FPGAs SelectIO Resources User Guide* (UG471)
3. *7 Series FPGA Packaging and Pinout Specification* (UG475)
4. *7 Series FPGAs PCB Design Guide* (UG483)
5. Xilinx Power Estimator spreadsheet tool (XPE)
6. *Zynq-7000 AP SoC and 7 Series FPGAs Memory Interface Solutions User Guide* (UG586)
7. See the [Clocking Wizard](#) in Vivado software.
8. *7 Series FPGAs and Zynq-7000 AP SoC XADC Dual 12-Bit 1 MSPS Analog-to-Digital Converter User Guide* (UG480)
9. *7 Series FPGA Configuration User Guide* (UG470)

## Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
06/20/2017	1.2	Updated paragraph before <a href="#">Table 6</a> . In <a href="#">Table 12</a> , updated Vivado tools version to 2017.2. In <a href="#">Table 13</a> , moved all speed grades for XC7S50 from Preliminary to Production and updated <a href="#">Note 1</a> . In <a href="#">Table 14</a> , added Vivado tools version for XC7S50. In <a href="#">Table 49</a> , added package skew value for XC7S50 device in FGGA484 package.
04/07/2017	1.1	Added 1.35V to <a href="#">Note 5</a> in <a href="#">Table 2</a> . In <a href="#">Table 12</a> , updated Vivado tools version to 2016.4. In <a href="#">Table 13</a> , moved all speed grades for XC7S50 from Advance to Preliminary. Removed SFI-4.1 and SPI-4.2 from descriptions of SDR LVDS receiver and DDR LVDS receiver, respectively, in <a href="#">Table 15</a> . In <a href="#">Table 25</a> , changed $T_{IDELAYRESOLUTION}$ units from ps to $\mu$ s. Removed BUFMR from <a href="#">Note 1</a> in <a href="#">Table 34</a> . In <a href="#">Table 49</a> , replaced TQGA144 with FTGB196 for XC7S6, XC7S15, and XC7S25 devices, added FTGB196 package for XC7S50 device, and added package skew value for XC7S50 device in CSGA324 package.
09/27/2016	1.0	Initial Xilinx release.

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