ZYNQ_NvDIMM SCHEMAITC

CETHIK

中电海康集团有限公司

绘制：	审核：	批准：
Title		
Size: A3	SCHEMATIC CODE: TOP	Rev: 1.00
	PROJECT NAME: ZYNQ_NvDIMM	
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TITLE TABLE

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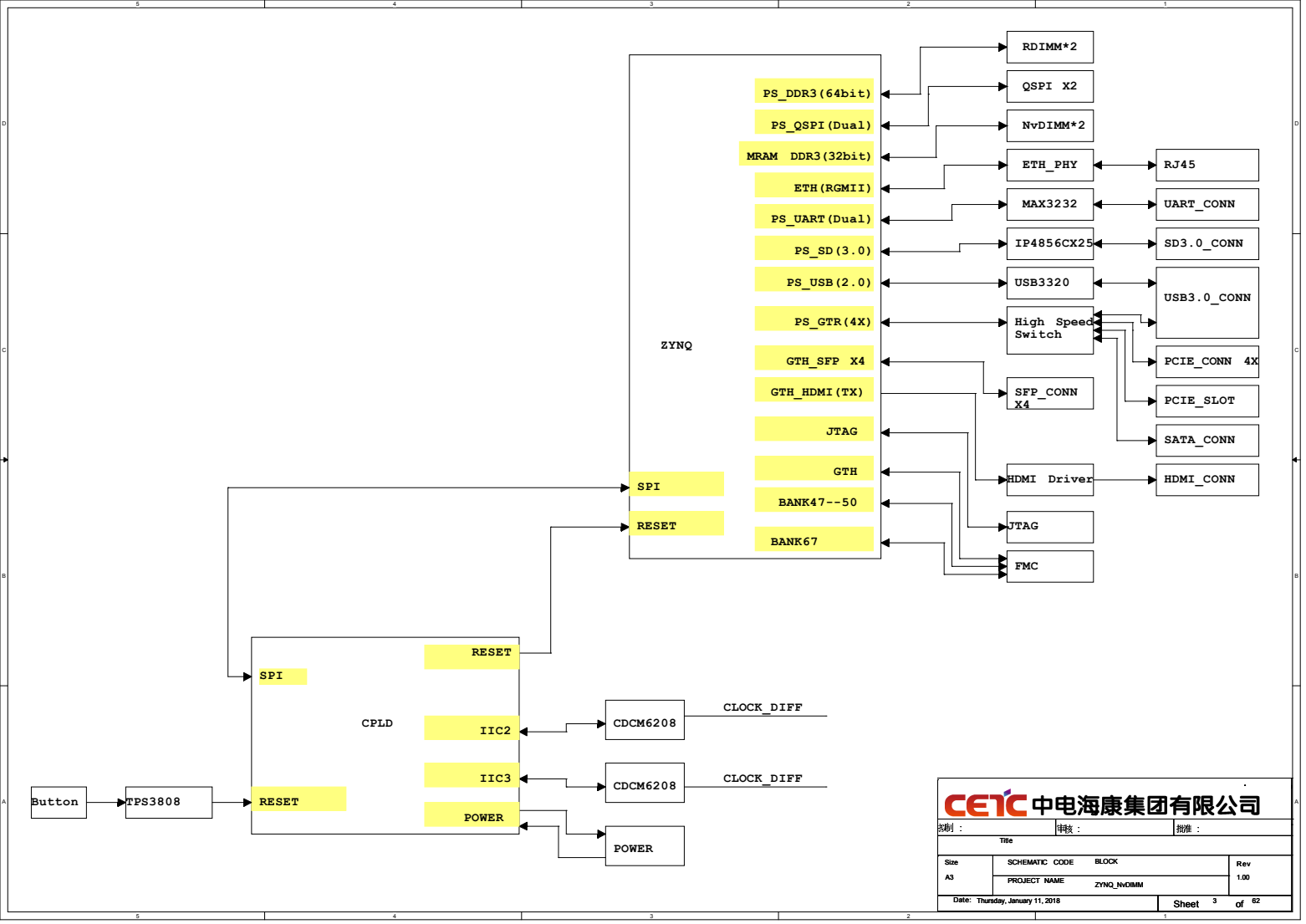

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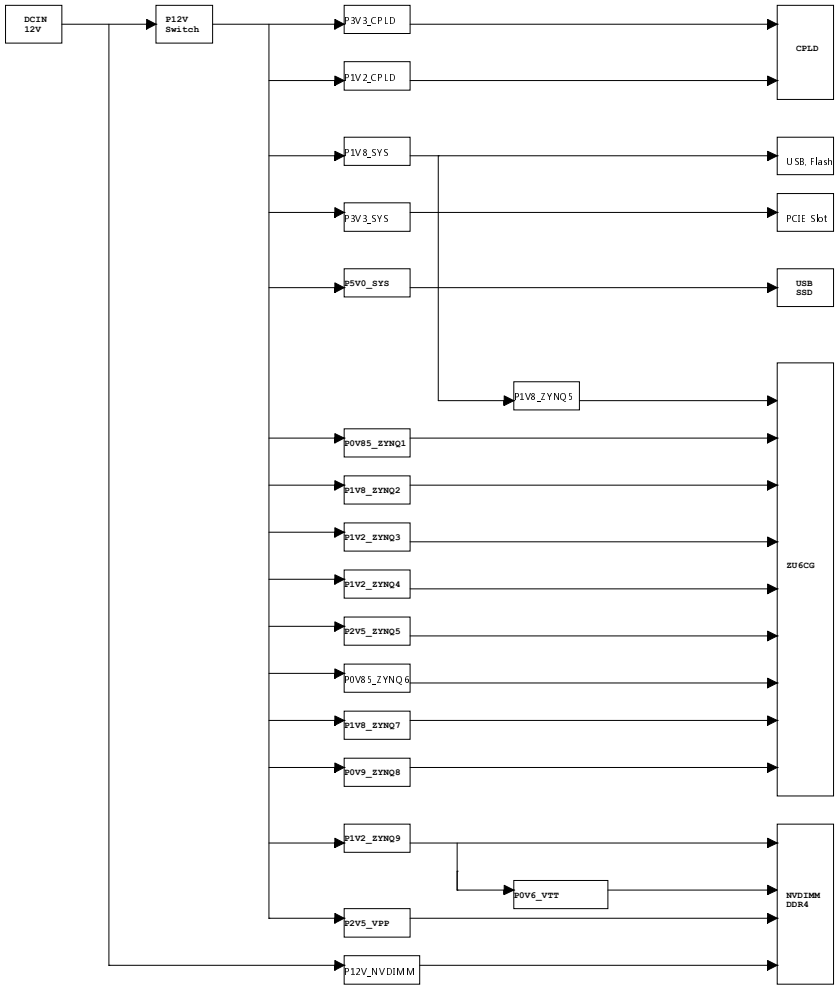

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拟制：	审核：	批准：

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A3	PROJECT NAME	ZYNQ_NvDIMM	1.00

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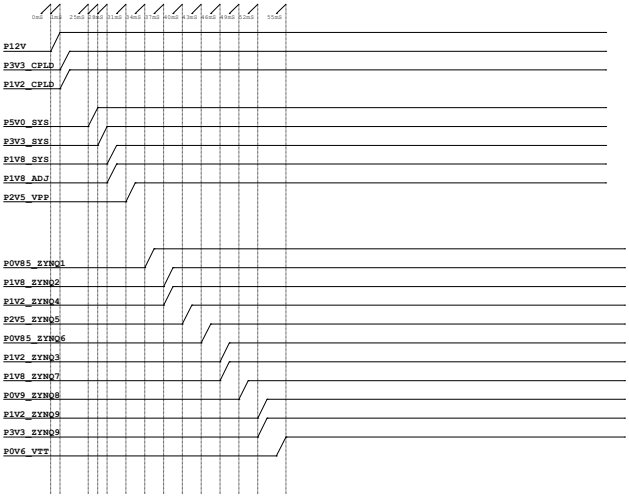

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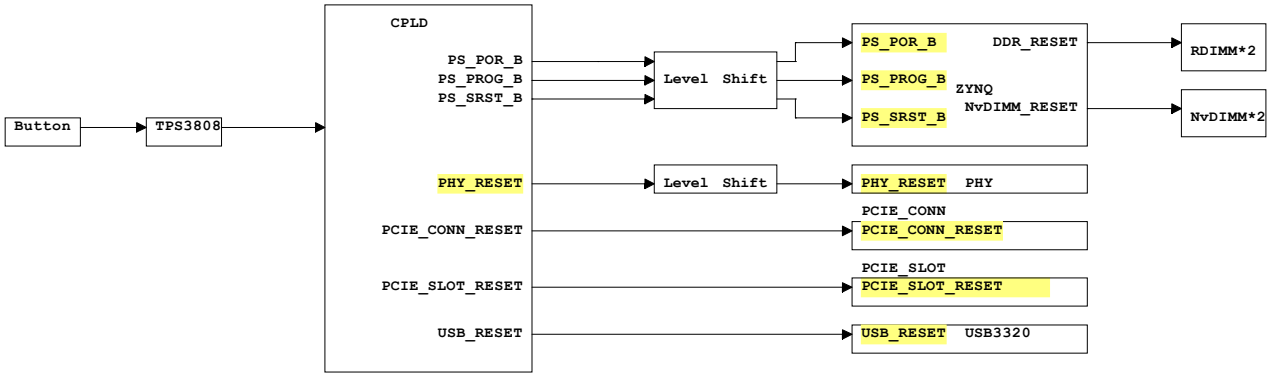

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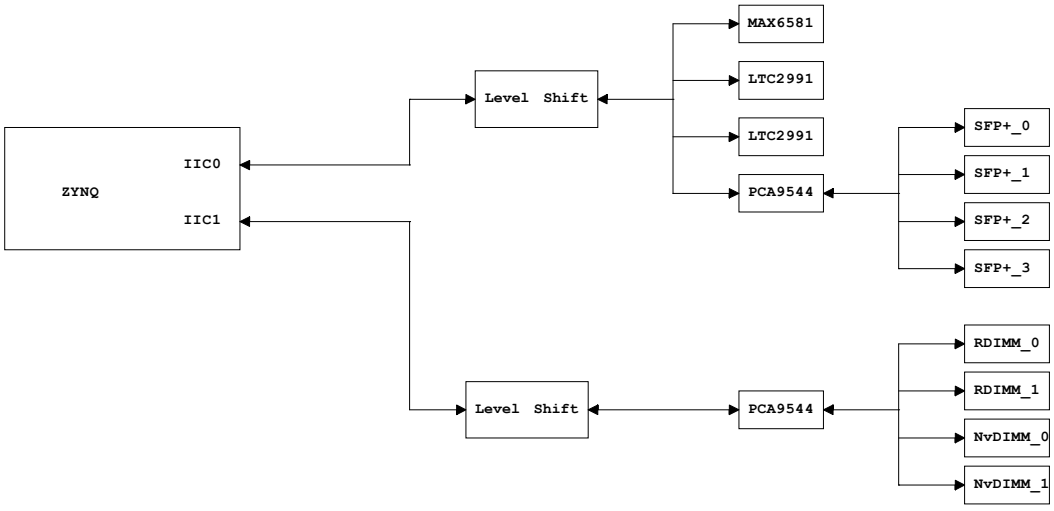

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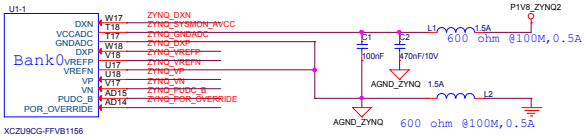

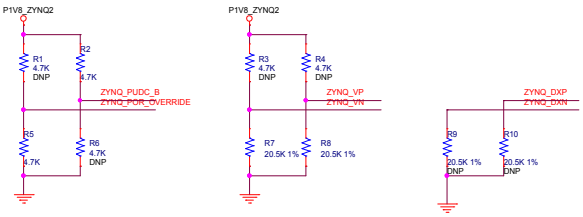

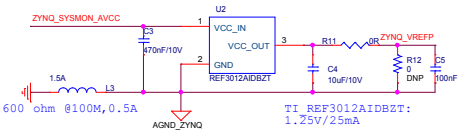

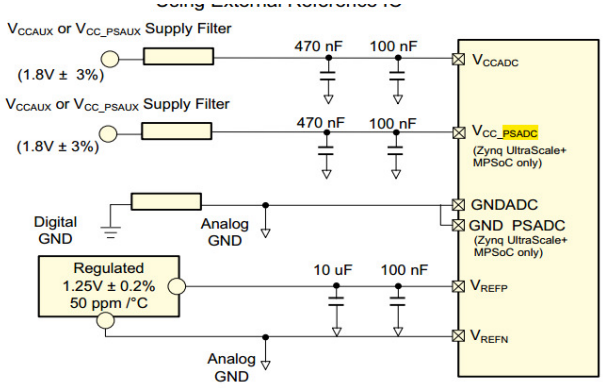

see ug580.p13

PUDC_B:1 = Weak preconfiguration I/O pull-up resistors disabled.PUDC_B is powered by VCCAUX.

POR_OVERRIDE:0 = Standard PL power-on delay time.

VP_VN:This pin should be connected to GNDADC if not used.

DXP_DXN: When not used, tie to GND.

VREFP:Voltage reference input(1.25V).

VREFN:Voltage reference GND.

VCCADC:PL System Monitor supply relative to GNDADC(1.8V).

CETC 中电海康集团有限公司

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Size	SCHEMATIC CODE	ZYNQ_CONFIG	Rev
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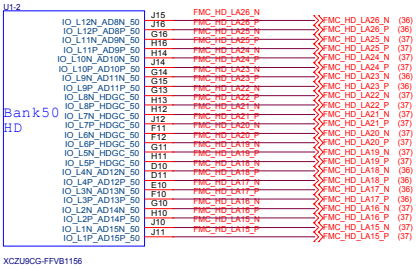

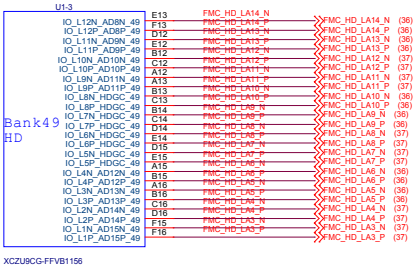

CETC 中电海康集团有限公司

拟制：	审核：	批准：

Title

Size	SCHEMATIC CODE	ZYNQ_HD_BANK49/50	Rev
A3	PROJECT NAME	ZYNQ_NvDIMM	1.00

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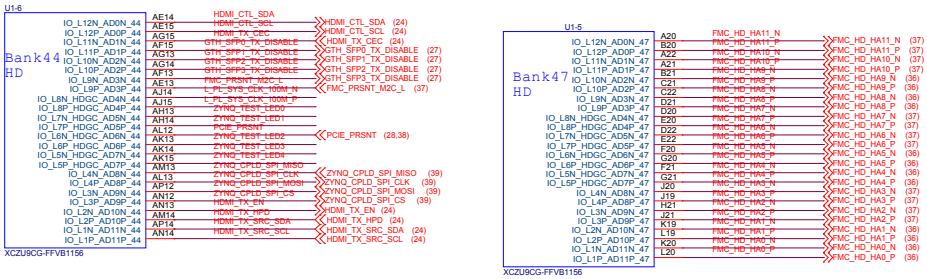

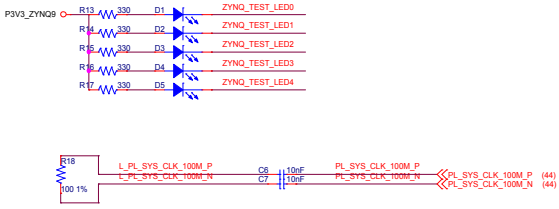

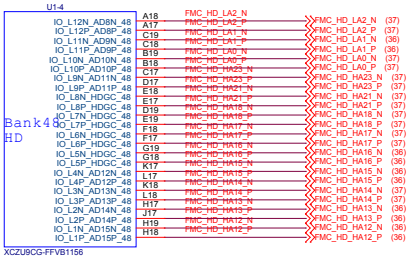

NOTE:
HDGC pins have direct access to the global clock buffers.

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Size: A3	SCHEMATIC CODE: ZYNQ_HD_BANK44/47/48	Rev: 1.00
	PROJECT NAME: ZYNQ_NvDIMM	
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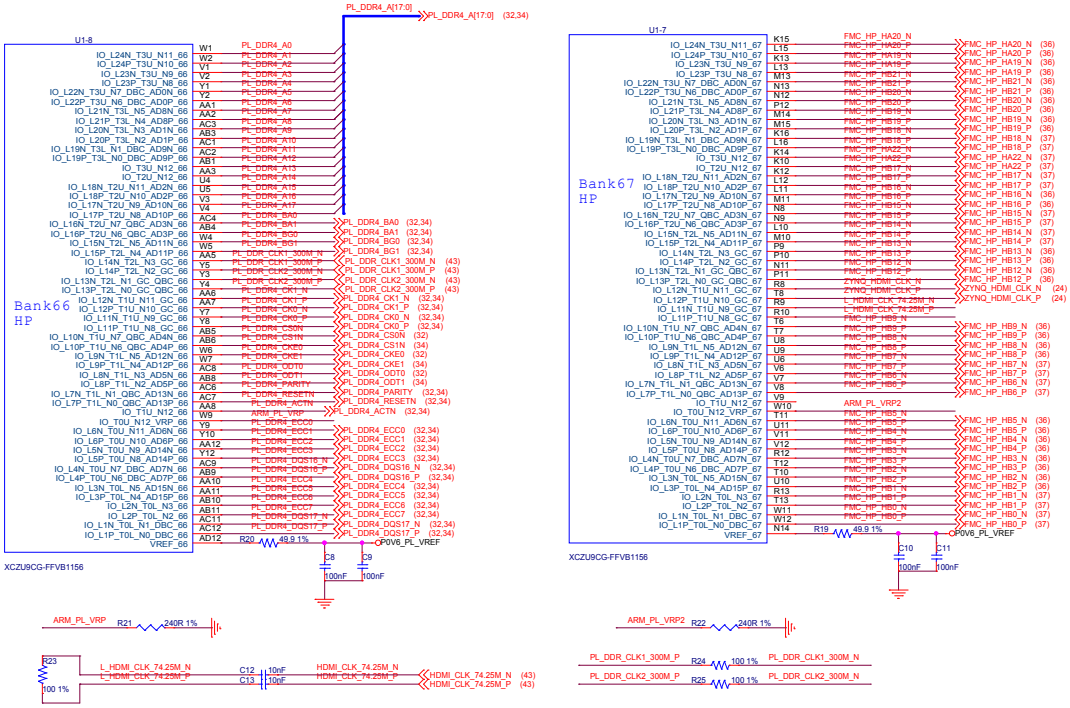

NOTE:
VRP:This pin is for the DCI voltage reference resistor of P
transistor.Digitally controlled impedance (DCI) is only available in HP I/O banks.
DCI uses only one reference resistor per bank, 240Ω to GND on the VRP pin

NOTE:
GC pins have direct access to the global clock buffers and the MMCMs and PLLs
that are in the clock management tile (CMT) adjacent to the same I/O bank.

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拟制：	审核：	批准：
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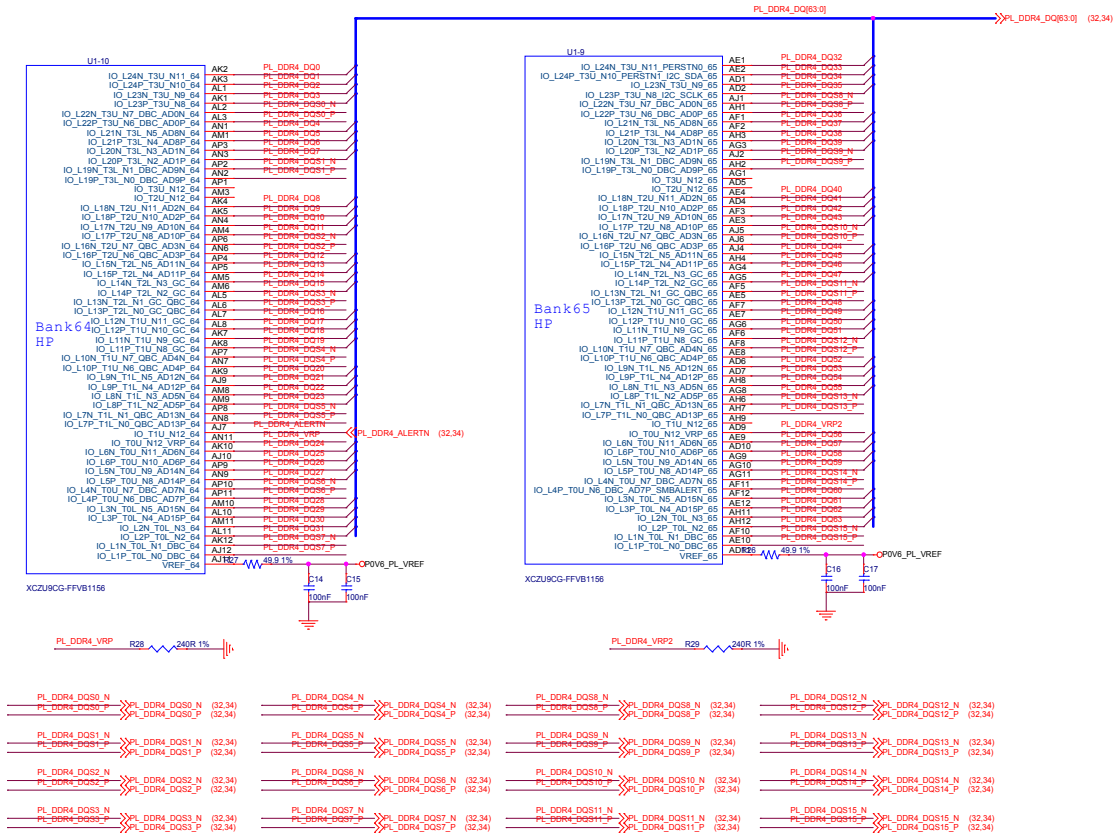

NOTE:
VRP:This pin is for the DCI voltage reference resistor of P
transistor.Digitally controlled impedance (DCI) is only available in HP I/O banks.
DCI uses only one reference resistor per bank, 240Ω to GND on the VRP pin

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Size	SCHEMATIC CODE	ZYNQ_HP_BANK64/65	Rev
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NOTE:
MGTREFCLK*_P/N:The dedicated differential reference clock input pair MGTREFCLKP/MGTREFCLKN is internally terminated with 100Ω differential impedance. The common mode voltage for UltraScale+ FPGAs is MGTAVCC, or nominal of 0.9V. If the reference clock input is not used, leave the reference clock input pins unconnected (both MGTREFCLKP and MGTREFCLKN).(see ug576.p324)

NOTE:
MGTHRXP[3:0]/MGTHRXN[3:0]
If a receiver will never be used under any conditions, connect the associated pin pair to GND. If a transmitter is not used, leave the associated pin pair unconnected.

NOTE:
Connect the MGTAVTTRCAL pin to the MGTAVTT supply and to a pin on the 100Ω precision external resistor.the trace from the MGTAVTTRCAL pin to the resistor should have the same length and geometry as the trace that connects the other pin of the resistor to the MGTRREF pin.

NOTE:
Connect the MGTAVTTRCAL pin to the MGTAVTT supply and to a pin on the 100Ω precision external resistor.the trace from the MGTAVTTRCAL pin to the resistor should have the same length and geometry as the trace that connects the other pin of the resistor to the MGTRREF pin.

U1-11 Bank128 GTH — XCZU9CG-FFVB1156
U1-12 Bank130 GTH — XCZU9CG-FFVB1156
U1-13 Bank229 GTH — XCZU9CG-FFVB1156
Bank228 GTH — XCZU9CG-FFVB1156
Bank230 GTH — XCZU9CG-FFVB1156

制图：	审核： 批准：
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Size A3	SCHEMATIC CODE ZYNQ_GTH_BANK
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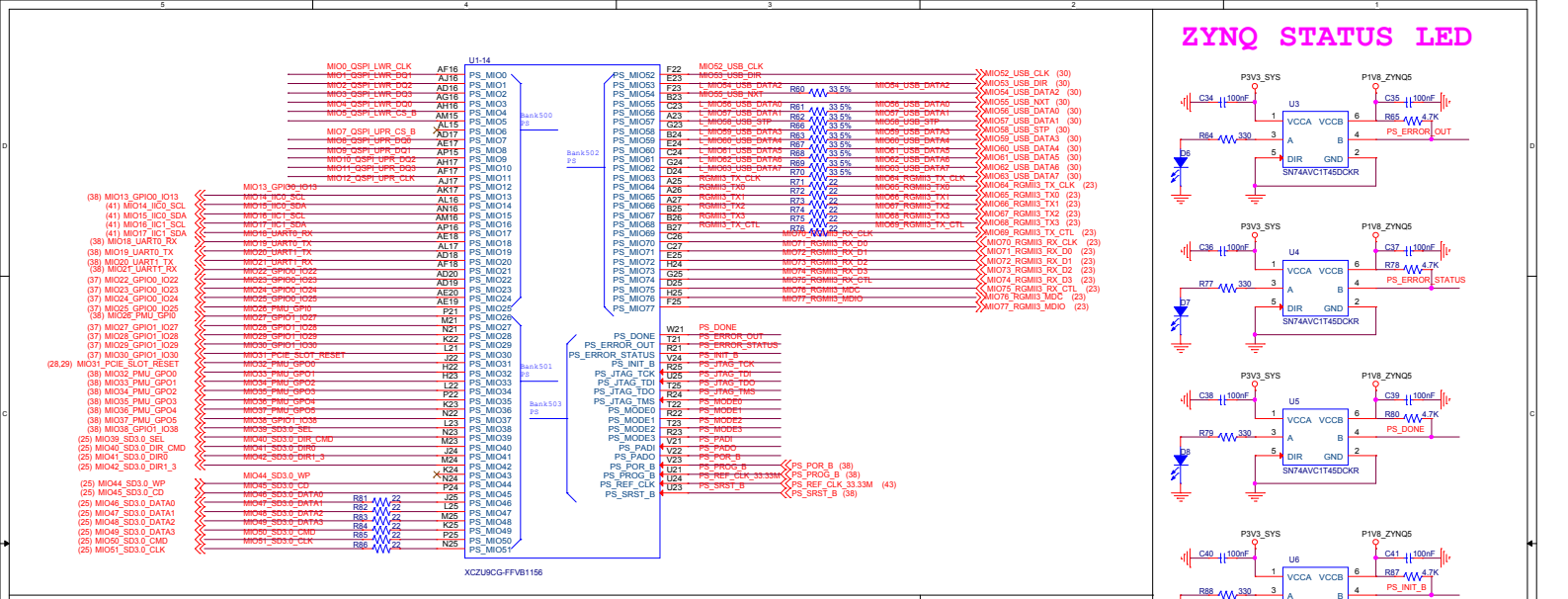


ZYNQ STATUS LED

NOTE:SN74AVC1T45
DIR:DIR Input Circuit Referenced to VCCA.
L:B Data --> A Bus;
H:A Data --> B Bus.

PS_INIT_B:
Initialization completion indicator after POR.Requires an external pull-up resistor.

PS_DONE:
Requires an external pull-up resistor.

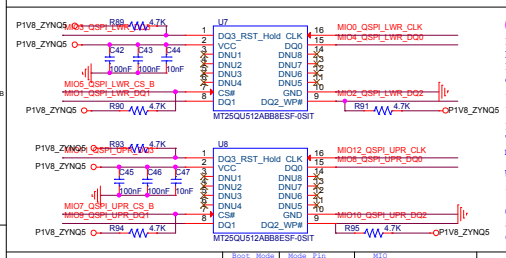
QSPI

DQ3_RST_HOLD_B:
RESET# or HOLD# signals can share Pin 1 with DQ3
DQ3 must be driven high by the host, or an external pull-up resistor must be placed on the PCB, in order to avoid allowing the HOLD# or RESET# input to float.

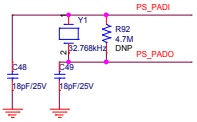
Pin 3 = RESET# or DNU, depending on the part number. This signal has an internal pullup resistor and may be left unconnected if not used.

WP#:This signal does not have internal pull-ups, it cannot be left floating and must be driven

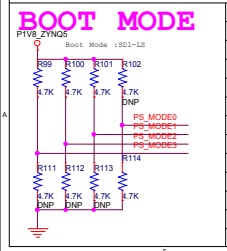
CS#: When S# is driven HIGH, the device will enter standby mode, unless an internal PROGRAM, ERASE, or WRITE STATUS REGISTER cycle is in progress



RTC CLK

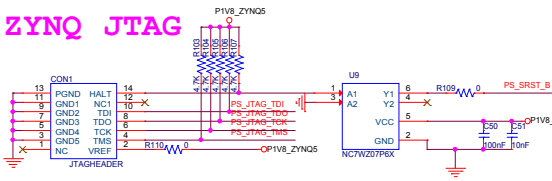


BOOT MODE



Boot Mode	Mode Pin [3:0]	MIO Location
JTAG	0x0	JTAG
QSPI24	0x1	MIO[12:0]
QSPI32	0x2	MIO[12:0]
SD0	0x3	MIO[25:13]
NAND	0x4	MIO[25:9]
SD1	0x5	MIO[51:38]
eMMC_1B	0x6	MIO[22:13]
USB0	0x7	MIO[63:52]
PJTAG0	0x8	MIO[29:26]
PJTAG1	0x9	MIO[15:12]
SD1_LS	0xE	MIO[51:39]

ZYNQ JTAG



NC7WZ07P6X Function Table

Input A	output Y
L	L
H	High Impedance Output State,Open Drain

NOTE: VCC1.65V to 5.5V

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制：	审核：	批准：
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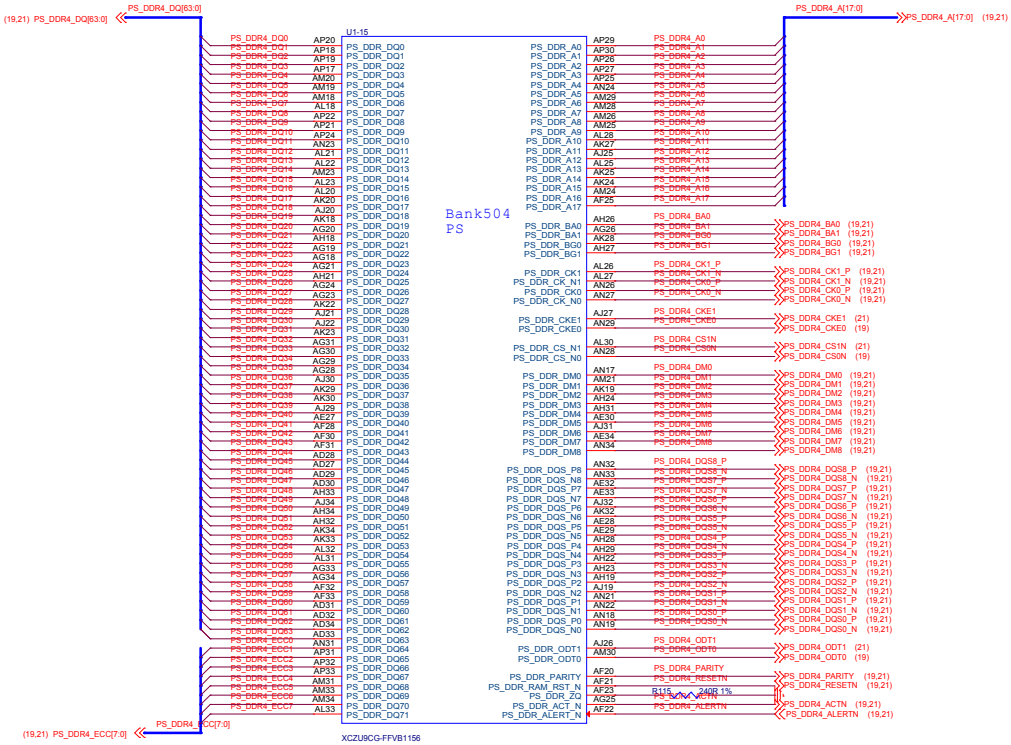

NOTE:
1、All unused DDR pins can be left unconnected.
2、Connect the PS_DDR_ZQ pin to GND using a 240Ω resistor.
There should be separate 240Ω resistors at the FPGA and at the DRAM.

NOTE:
DDR3/3L Pin Swapping Restrictions
1、Address/command/control bits cannot be swapped.
2、DQ byte lane swapping is allowed.
3、DQ bits swapping within a byte lane is allowed.(see ug1075.p52)

NOTE:
PS_DDR_PARITY:Can be left unconnected for components and UDIMMs.
(see ug1075)

PS_DDR_ALERT_N:Can be left unconnected.

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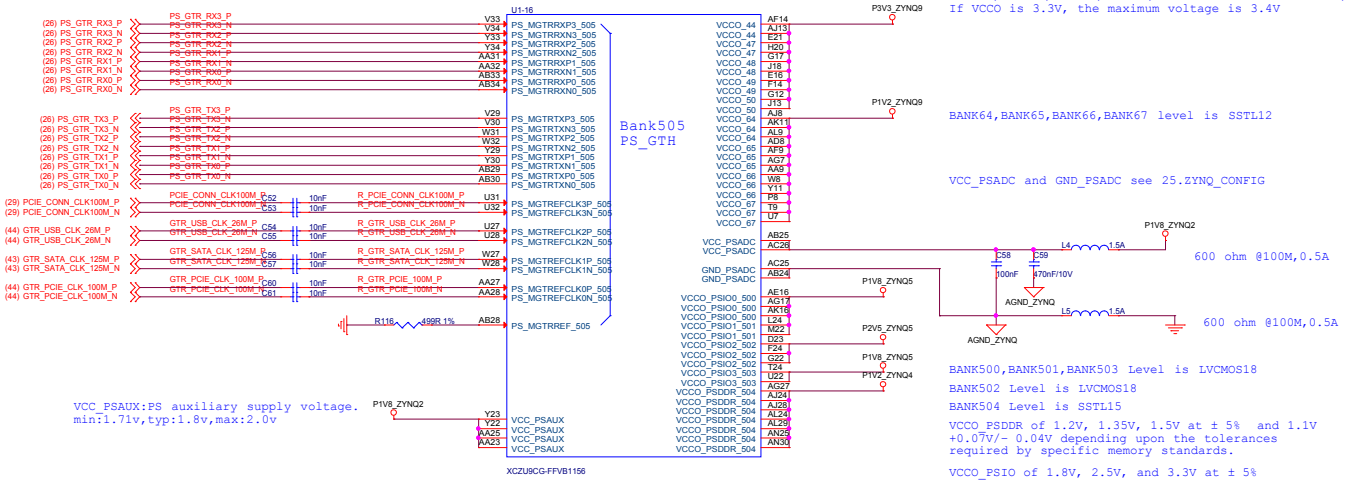

NOTE:
BANK44,BANK47,BANK48,BANK49,BANK50 level is LVCMOS33,
If VCCO is 3.3V, the maximum voltage is 3.4V

BANK64,BANK65,BANK66,BANK67 level is SSTL12

VCC_PSADC and GND_PSADC see 25.ZYNQ_CONFIG

BANK500,BANK501,BANK503 Level is LVCMOS18

BANK502 Level is LVCMOS18

BANK504 Level is SSTL15

VCCO_PSDDR of 1.2V, 1.35V, 1.5V at ± 5% and 1.1V +0.07V/- 0.04V depending upon the tolerances required by specific memory standards.

VCCO_PSIO of 1.8V, 2.5V, and 3.3V at ± 5%

NOTE:
PS_MGTRREF:Connect to a 500Ω 0.5% resistor to this pin with the other terminal of the resistor connected to ground.(see ug583.p176)

PS_MGTRTX[3:0]_P/_N:
If a transmitter is not used, leave the associated pin pair unconnected.(see ug583.p176)

PS_MGTRRX[3:0]_P/_N:
If a transmitter is not used, leave the associated pin pair unconnected.
The recommended value for AC coupling capacitors is 100 nF.(see ug583.p176)

PS_MGTREFCLK[3:0]_P/_N:
Use AC coupling capacitors for connection to oscillator;
For AC coupling capacitors,The recommended value for LVDS is 10 nF.
If the reference clock input is not used, leave the associated pin pair unconnected.(see ug583.p176)

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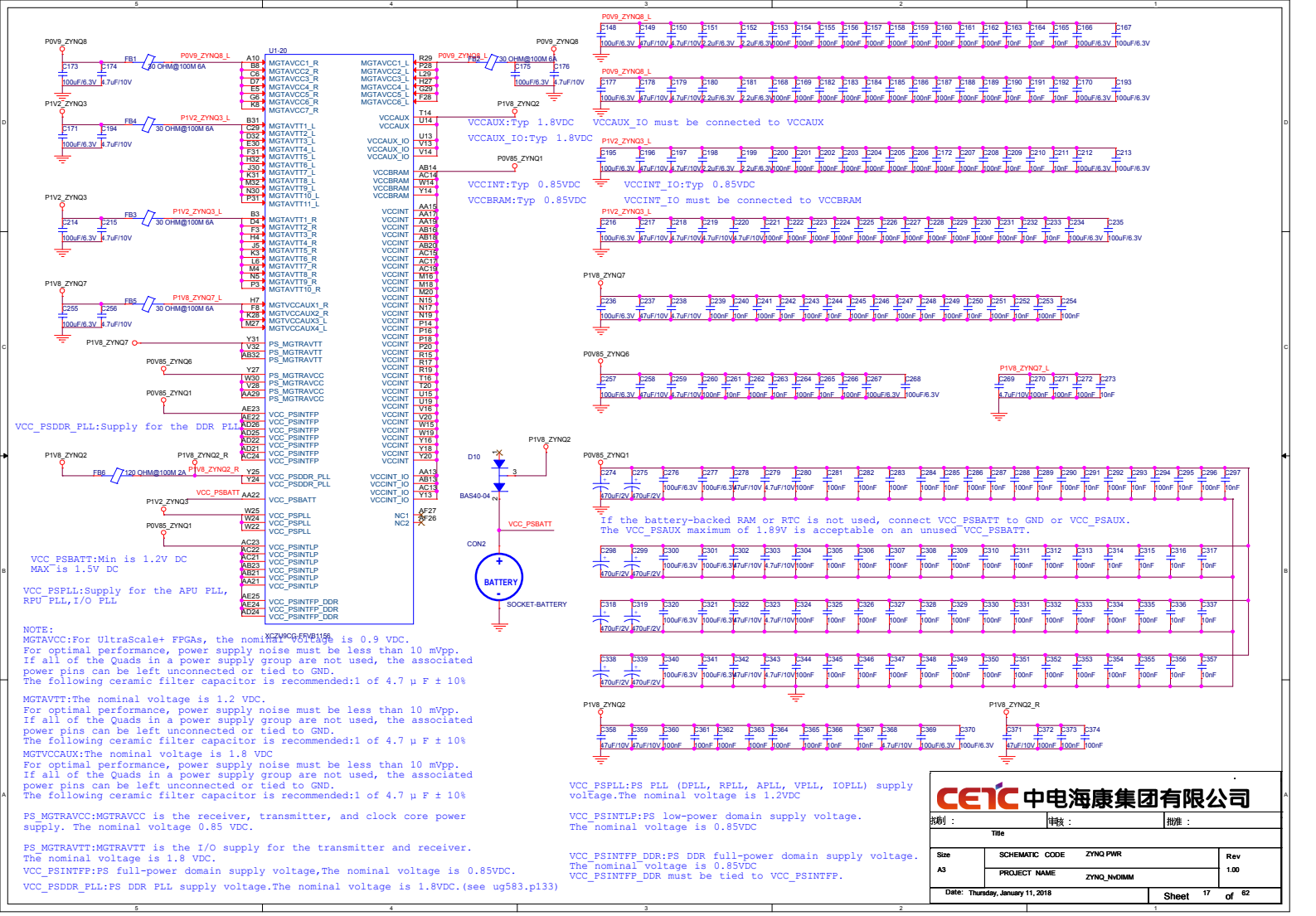

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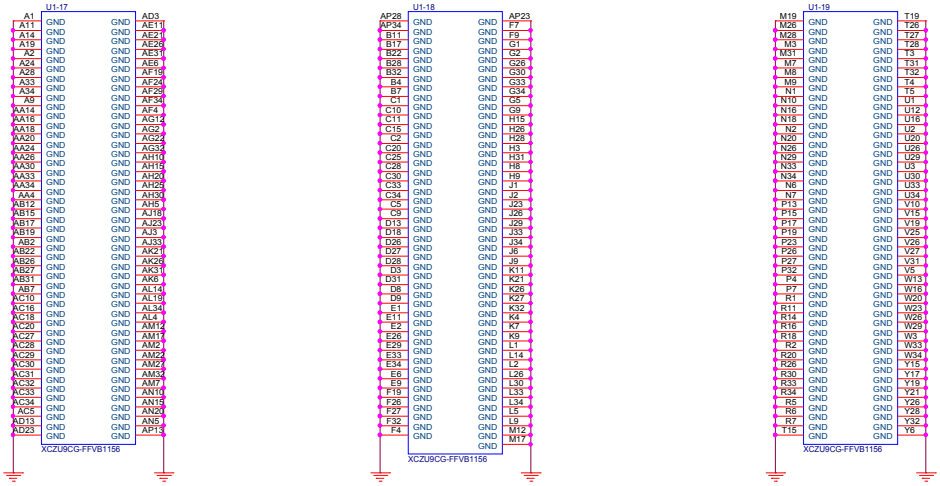

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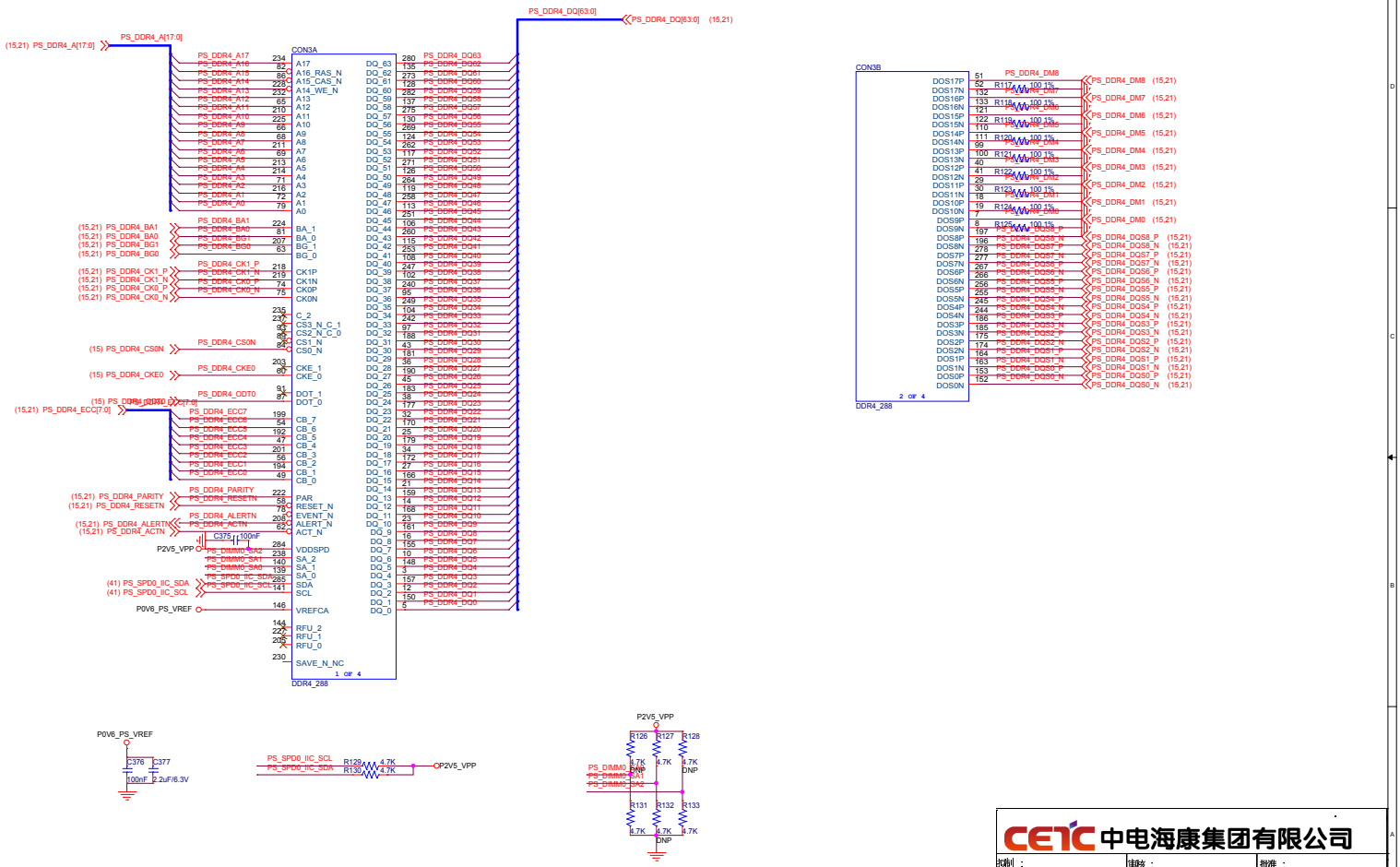

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制：	审核：	批准：
Title		
Size: A3	SCHEMATIC CODE: ZYNQ PS DDR4_DIMM0	Rev: 1.00
	PROJECT NAME: ZYNQ_NvDIMM	
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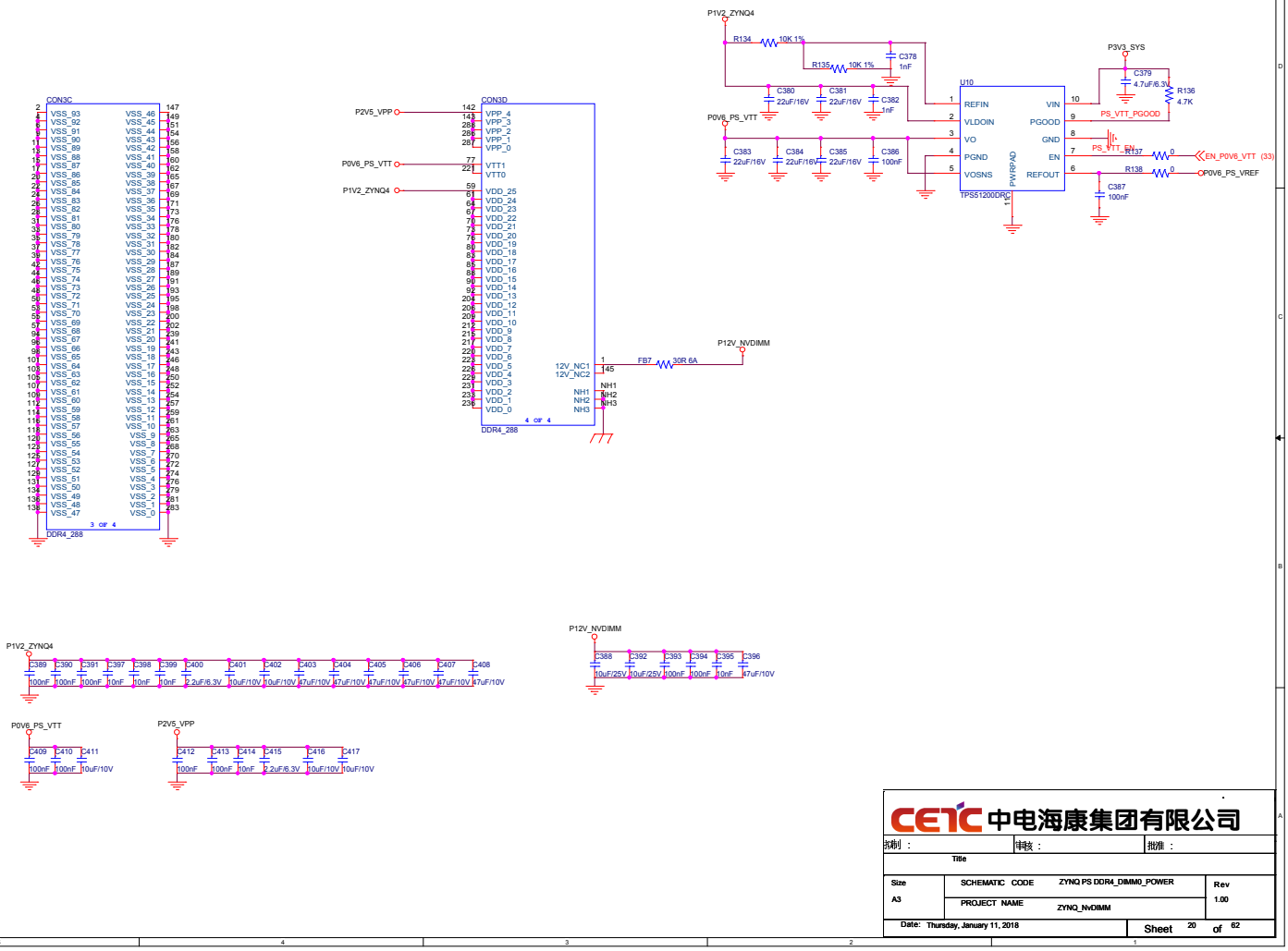

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绘制：	审核：	批准：
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	PROJECT NAME: ZYNQ_NvDIMM	
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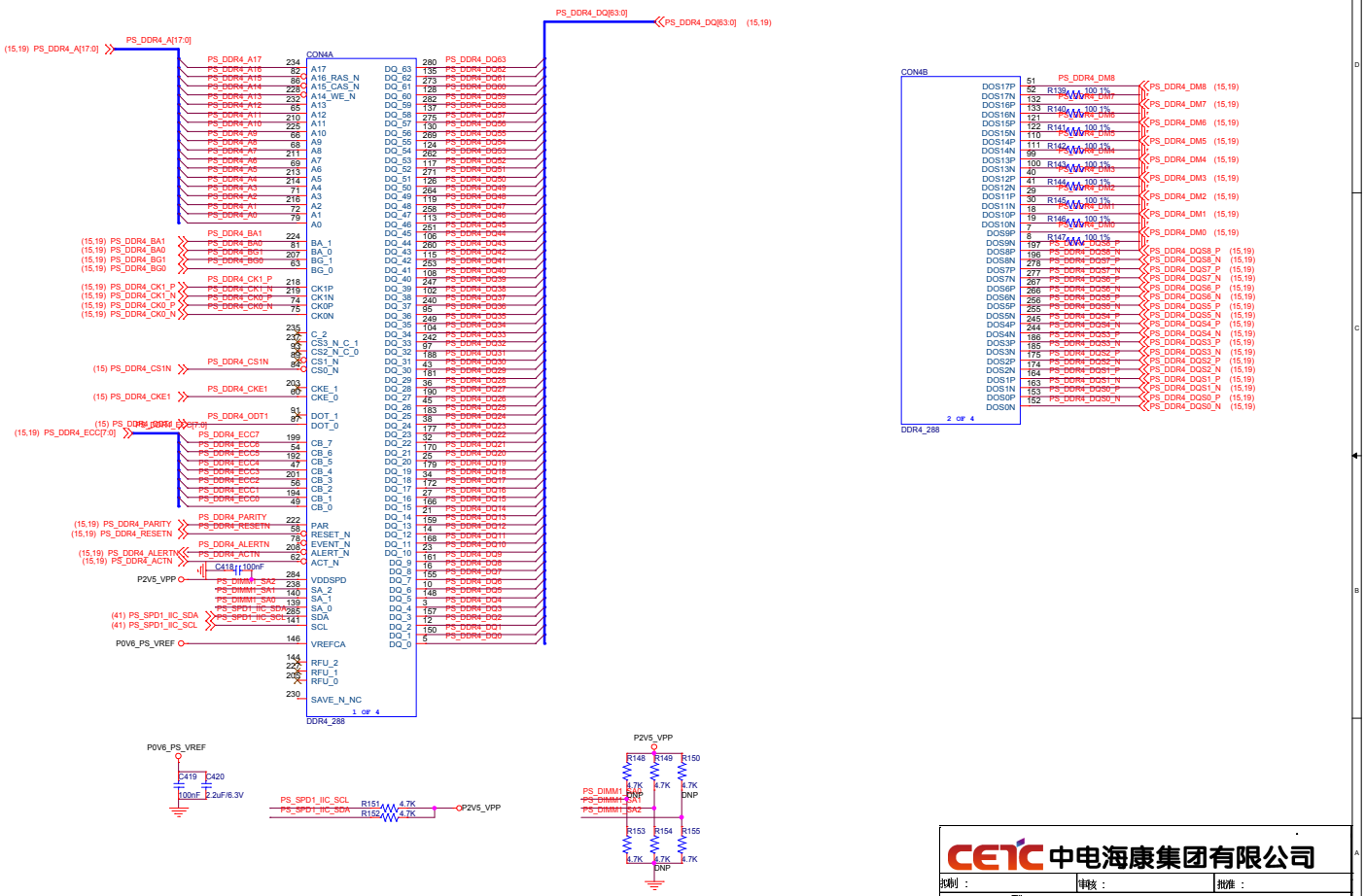

中电海康集团有限公司			
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	PROJECT NAME: ZYNQ_NvDIMM		
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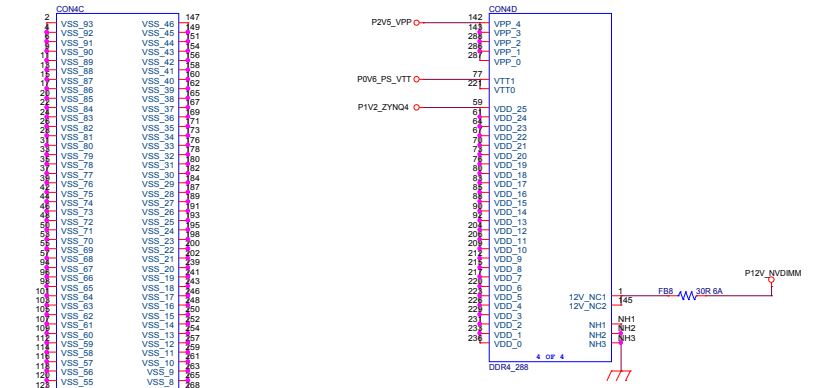

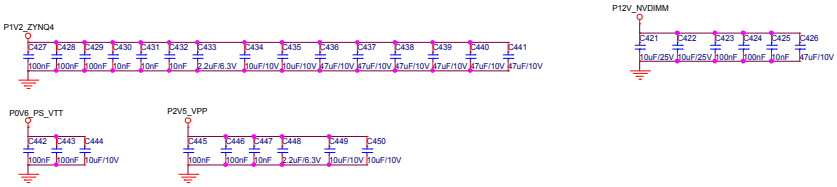

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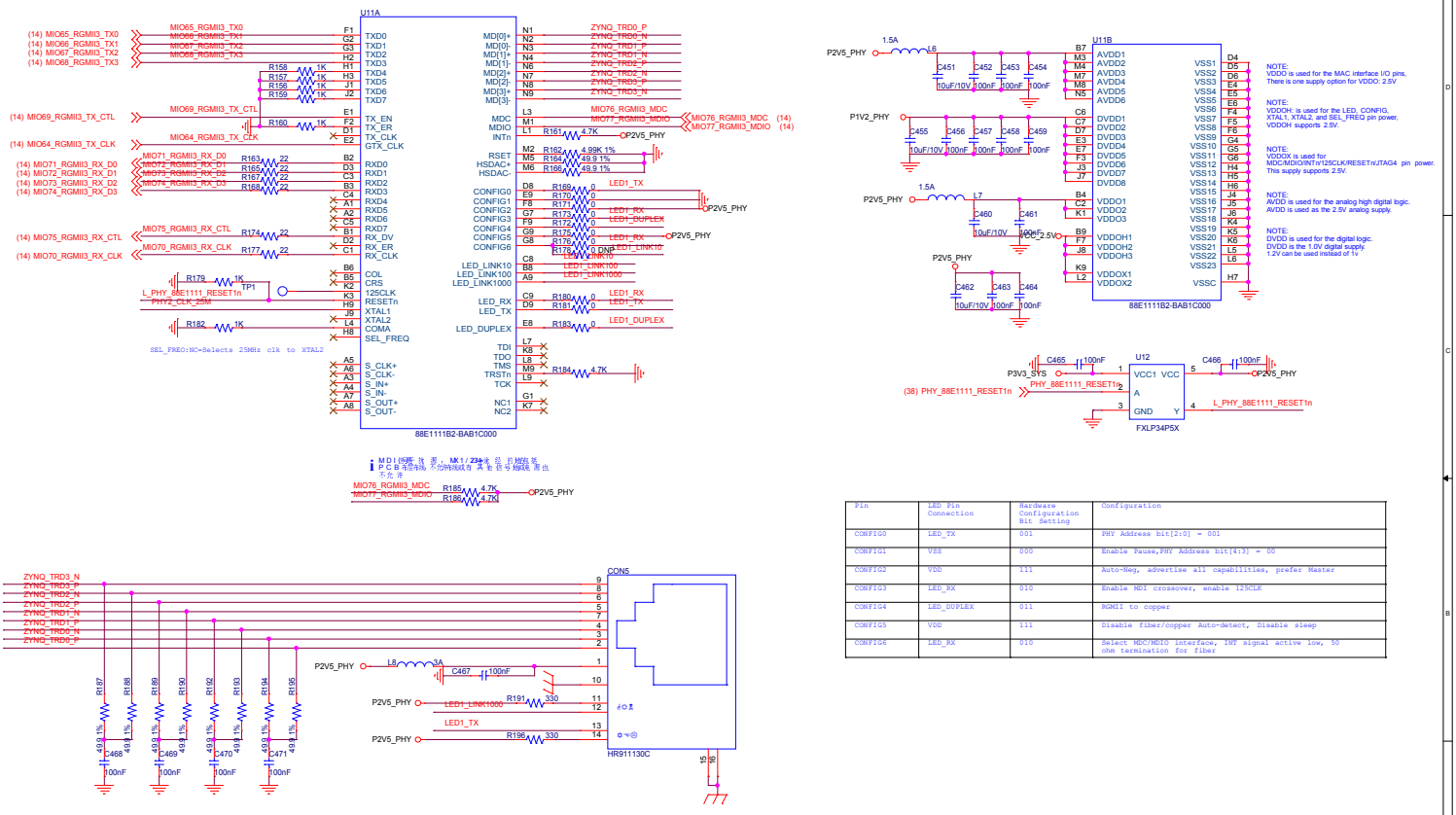
拟制：	审核：	批准：

Title

Size	SCHEMATIC CODE	ZYNQ_PS_DDR4_DIMM1_POWER	Rev
A3	PROJECT NAME	ZYNQ_NvDIMM	1.00

Date: Thursday, January 11, 2018 Sheet 22 of 62



Pin	LED Pin Connection	Hardware Configuration Bit Setting	Configuration
CONFIG0	LED_TX	001	PHY Address bit[2:0] = 001
CONFIG1	VSS	000	Enable Pause,PHY Address bit[4:3] = 00
CONFIG2	VDD	111	Auto-Neg, advertise all capabilities, prefer Master
CONFIG3	LED_RX	010	Enable MDI crossover, enable 125CLK
CONFIG4	LED_DUPLEX	011	RGMII to copper
CONFIG5	VDD	111	Disable fiber/copper Auto-detect, Disable sleep
CONFIG6	LED_RX	010	Select MDC/MDIO interface, INT signal active low, 50 ohm termination for fiber

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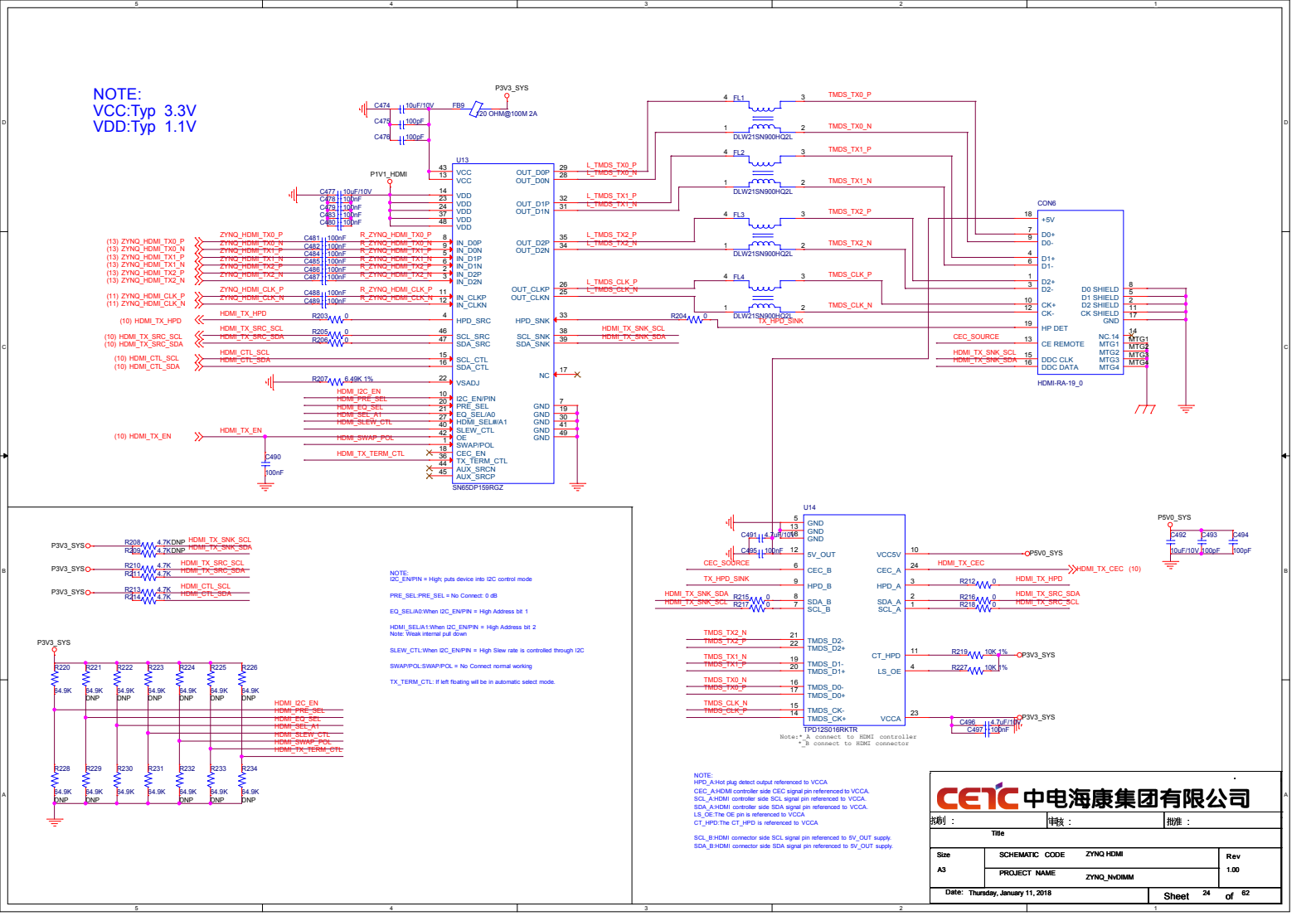
绘制：	审核：	批准：
Title		
Size: A3	SCHEMATIC CODE: ZYNQ ETH PHY	Rev: 1.00
	PROJECT NAME: ZYNQ_NvDIMM	
Date: Thursday, January 11, 2018	Sheet 23 of 62	


NOTE:
VCC:Typ 3.3V
VDD:Typ 1.1V
P3V3_SYS
P1V1_HDMI
U13
SN65DP159RGZ
CON6
HDMI-RA-19_0
U14
TPD12S016RKTR
TMDS_TX0_P
TMDS_TX0_N
TMDS_TX1_P
TMDS_TX1_N
TMDS_TX2_P
TMDS_TX2_N
TMDS_CLK_P
TMDS_CLK_N
HDMI_TX_SNK_SCL
HDMI_TX_SNK_SDA
HDMI_TX_HPD
HDMI_TX_SRC_SCL
HDMI_TX_SRC_SDA
HDMI_CTL_SCL
HDMI_CTL_SDA
HDMI_TX_EN
HDMI_I2C_EN
HDMI_PRE_SEL
HDMI_EQ_SEL
HDMI_SEL_A1
HDMI_SLEW_CTL
HDMI_SWAP_POL
HDMI_TX_TERM_CTL
CEC_SOURCE
TX_HPD_SINK
HDMI_TX_CEC
P5V0_SYS
NOTE:
I2C_EN/PIN = High: puts device into I2C control mode
PRE_SEL:PRE_SEL = No Connect: 0 dB
EQ_SEL/A0:When I2C_EN/PIN = High Address bit 1
HDMI_SELA1:When I2C_EN/PIN = High Address bit 2
Note: Weak internal pull down
SLEW_CTL:When I2C_EN/PIN = High Slew rate is controlled through I2C
SWAP/POL:SWAP/POL = No Connect normal working
TX_TERM_CTL: If left floating will be in automatic select mode.
NOTE:
HPD_A:Hot plug detect output referenced to VCCA
CEC_A:HDMI controller side CEC signal pin referenced to VCCA.
SCL_A:HDMI controller side SCL signal pin referenced to VCCA.
SDA_A:HDMI controller side SDA signal pin referenced to VCCA.
LS_OE:The OE pin is referenced to VCCA
CT_HPD:The CT_HPD is referenced to VCCA
SCL_B:HDMI connector side SCL signal pin referenced to 5V_OUT supply.
SDA_B:HDMI connector side SDA signal pin referenced to 5V_OUT supply.
Note:*_A connect to HDMI controller
*_B connect to HDMI connector
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Title
Size
A3
SCHEMATIC CODE
ZYNQ HDMI
PROJECT NAME
ZYNQ_NvDIMM
Rev
1.00
Date: Thursday, January 11, 2018
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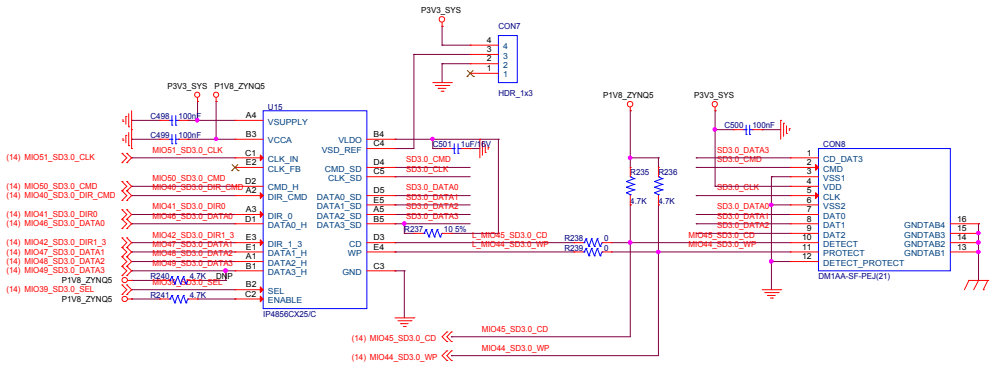

NOTE:
It is designed to interface between a memory card operating at 1.8 V or 2.9 V signal levels and a host with a fixed nominal supply voltage of 1.7 V to 3.6 V.The device supports SD 3.0, SDR104, SDR50, DDR50, SDHQS, SDR12 and SD 2.0 high-speed (50 MHz) and default-speed (25 MHz) modes.

ZYNQ:Support Transfers the data in SDR104, SDR50, and DDR50 modes.

The bidirectional level translator shifts the data between the I/O supply levels of the host and the memory card. Dedicated direction control signals determine if a command and data signals are transferred from the memory card to the host (card read mode) or from the host to the memory card (card write mode).

I/O function control signal truth table

Control		Host side		Memory card side	
Pin	Level	Pin	Function	Pin	Function
Pin ENABLE = HIGH and VCCA >=1.62 V					
DIR_CMD	H	CMD_H	input	CMD_SD	output
	L	CMD_H	output	CMD_SD	input
DIR_0	H	DATA0_H	input	DATA0_SD	output
	L	DATA0_H	output	DATA0_SD	input
DIR_1_3	H	DATA1_H	input	DATA1_SD	output
		DATA2_H	input	DATA2_SD	output
		DATA3_H	input	DATA3_SD	output
	L	DATA1_H	output	DATA1_SD	input
		DATA2_H	output	DATA2_SD	input
		DATA3_H	output	DATA3_SD	input
-	-	CLK_IN	input	CLK_SD	output
-	-	CLK_FB	output	-	-
Pin ENABLE = LOW or VCCA <= 0.8 V					
DIR_CMD	X	CMD_H	Hi-Z	CMD_SD	Hi-Z
DIR_0	X	DATA0_H	Hi-Z	DATA0_SD	Hi-Z
DIR_1_3	X	DATA1_H	Hi-Z	DATA1_SD	Hi-Z
		DATA2_H	Hi-Z	DATA2_SD	Hi-Z
		DATA3_H	Hi-Z	DATA3_SD	Hi-Z
-	-	CLK_IN	input	CLK_SD	Hi-Z
-	-	CLK_IN	Hi-Z	-	-

SD card side voltage level control signal truth table

Input		Output		
SEL	VSD_REF	VLDO	Pin	Function
H	X	1.8 V	DATA0_SD to DATA3_SD, CLK_SD	low supply voltage level (1.8 V typical)
L	< 1 V	2.9 V	DATA0_SD to DATA3_SD, CLK_SD	high supply voltage level (2.9 V typical)
	> 1.5 V	VSD_REF	DATA0_SD to DATA3_SD, CLK_SD	supply voltage level based on VSD_REF

Pins Write Protect (WP) and Card Detection (CD) might be pulled down by the memory card which has to be detected by the host. Both signals must be HIGH if no card is inserted.So pull-up resistors connected to the host supply VCCA.

VCCA:supply voltage from host side
CMD_H, DATA0_H to DATA3_H and CLK_IN SEL, ENABLE, DIR_0, DIR_1_3 and DIR_CMD Referenced to VCCA(1.8V)

VSUPPLY:supply voltage(3.3V)

VLDO:internal supply decoupling

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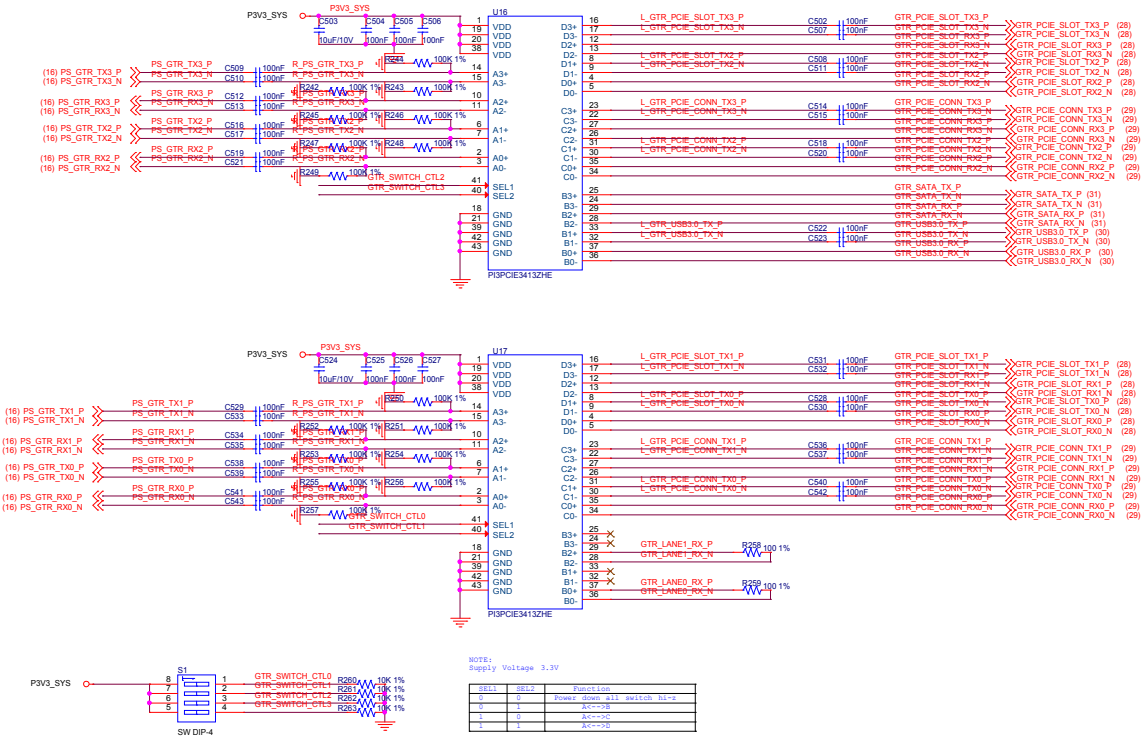
拟制：	审核：	批准：

Title

Size	SCHEMATIC CODE	ZYNQ SD3.0	Rev
A3	PROJECT NAME	ZYNQ_NvDIMM	1.00

Date: Thursday, January 11, 2018 Sheet 25 of 82



NOTE:
Supply Voltage 3.3V

SEL1	SEL2	Function
0	0	Power down all switch hi-z
0	1	A<-->B
1	0	A<-->C
1	1	A<-->D

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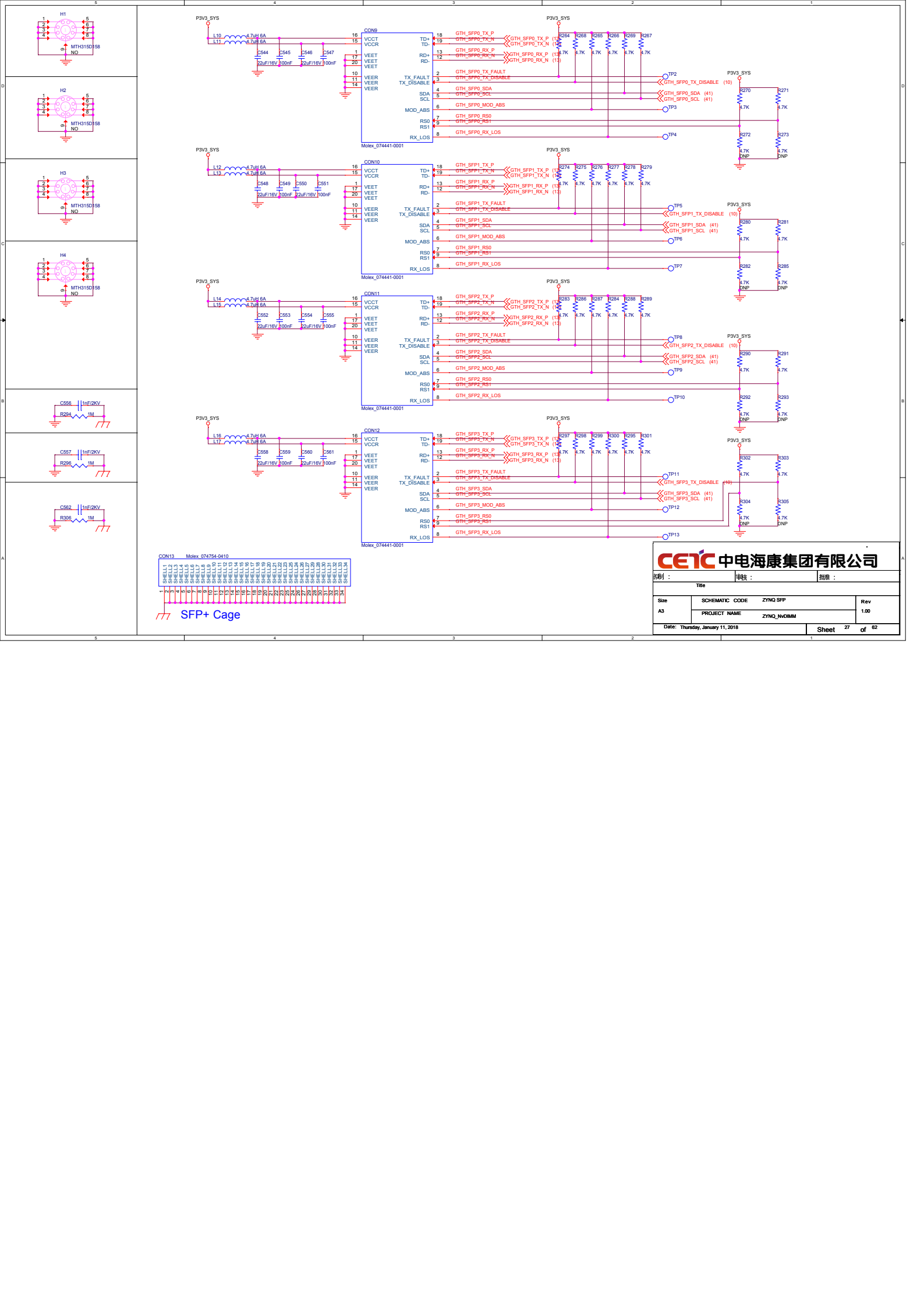
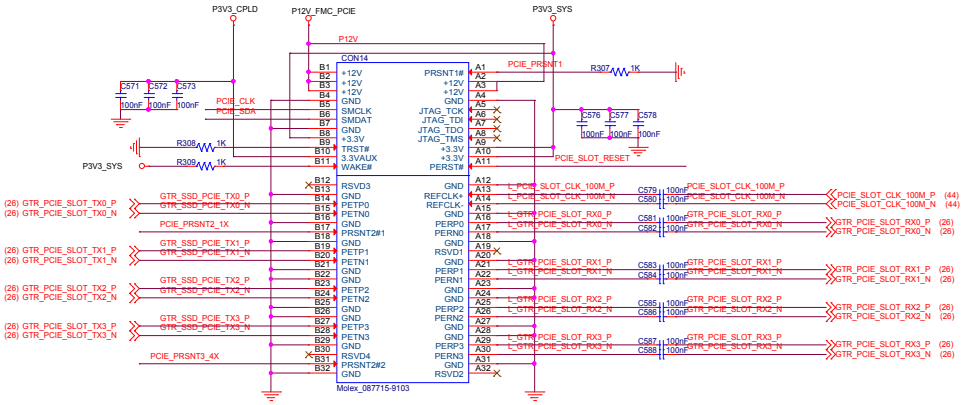
拟制：	审核：	批准：

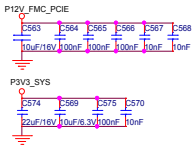
Title

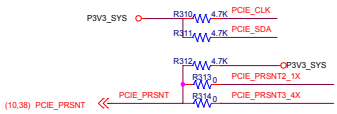
Size	SCHEMATIC CODE	ZYNQ GTR SWITCH	Rev
A3	PROJECT NAME	ZYNQ_NvDIMM	1.00

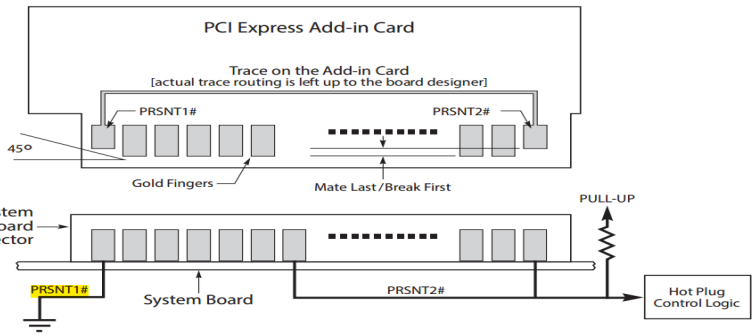
Date: Thursday, January 11, 2018 Sheet 26 of 62


H1
MTH315D158
NO
H2
MTH315D158
NO
H3
MTH315D158
NO
H4
MTH315D158
NO
C556 1nF/2KV
R294 1M
C557 1nF/2KV
R296 1M
C562 1nF/2KV
R306 1M
P3V3_SYS
L10 4.7uH 6A
L11 4.7uH 6A
C544 22uF/16V
C545 100nF
C546 22uF/16V
C547 100nF
CON9
Molex_074441-0001
VCCT
VCCR
VEET
VEER
TD+
TD-
RD+
RD-
TX_FAULT
TX_DISABLE
SDA
SCL
MOD_ABS
RS0
RS1
RX_LOS
GTH_SFP0_TX_P
GTH_SFP0_TX_N
GTH_SFP0_RX_P
GTH_SFP0_RX_N
GTH_SFP0_TX_FAULT
GTH_SFP0_TX_DISABLE
GTH_SFP0_SDA
GTH_SFP0_SCL
GTH_SFP0_MOD_ABS
GTH_SFP0_RS0
GTH_SFP0_RS1
GTH_SFP0_RX_LOS
R264 R268 R265 R266 R269 R267 4.7K
TP2
TP3
TP4
R270 R271 4.7K
R272 R273 4.7K DNP
L12 4.7uH 6A
L13 4.7uH 6A
C548 22uF/16V
C549 100nF
C550 22uF/16V
C551 100nF
CON10
GTH_SFP1_TX_P
GTH_SFP1_TX_N
GTH_SFP1_RX_P
GTH_SFP1_RX_N
GTH_SFP1_TX_FAULT
GTH_SFP1_TX_DISABLE
GTH_SFP1_SDA
GTH_SFP1_SCL
GTH_SFP1_MOD_ABS
GTH_SFP1_RS0
GTH_SFP1_RS1
GTH_SFP1_RX_LOS
R274 R275 R276 R277 R278 R279 4.7K
TP5
TP6
TP7
R280 R281 4.7K
R282 R285 4.7K DNP
L14 4.7uH 6A
L15 4.7uH 6A
C552 22uF/16V
C553 100nF
C554 22uF/16V
C555 100nF
CON11
GTH_SFP2_TX_P
GTH_SFP2_TX_N
GTH_SFP2_RX_P
GTH_SFP2_RX_N
GTH_SFP2_TX_FAULT
GTH_SFP2_TX_DISABLE
GTH_SFP2_SDA
GTH_SFP2_SCL
GTH_SFP2_MOD_ABS
GTH_SFP2_RS0
GTH_SFP2_RS1
GTH_SFP2_RX_LOS
R283 R286 R287 R284 R288 R289 4.7K
TP8
TP9
TP10
R290 R291 4.7K
R292 R293 4.7K DNP
L16 4.7uH 6A
L17 4.7uH 6A
C558 22uF/16V
C559 100nF
C560 22uF/16V
C561 100nF
CON12
GTH_SFP3_TX_P
GTH_SFP3_TX_N
GTH_SFP3_RX_P
GTH_SFP3_RX_N
GTH_SFP3_TX_FAULT
GTH_SFP3_TX_DISABLE
GTH_SFP3_SDA
GTH_SFP3_SCL
GTH_SFP3_MOD_ABS
GTH_SFP3_RS0
GTH_SFP3_RS1
GTH_SFP3_RX_LOS
R297 R298 R299 R300 R295 R301 4.7K
TP11
TP12
TP13
R302 R303 4.7K
R304 R305 4.7K DNP
CON13 Molex_074754-0410
SHELL1 SHELL2 SHELL3 SHELL4 SHELL5 SHELL6 SHELL7 SHELL8 SHELL9 SHELL10 SHELL11 SHELL12 SHELL13 SHELL14 SHELL15 SHELL16 SHELL17 SHELL18 SHELL19 SHELL20 SHELL21 SHELL22 SHELL23 SHELL24 SHELL25 SHELL26 SHELL27 SHELL28 SHELL29 SHELL30 SHELL31 SHELL32 SHELL33 SHELL34
SFP+ Cage
中电海康集团有限公司
制：
审核：
批准：
Title
Size A3
SCHEMATIC CODE ZYNQ SFP
PROJECT NAME ZYNQ_NvDIMM
Rev 1.00
Date: Thursday, January 11, 2018
Sheet 27 of 62

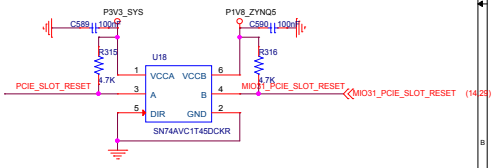








PCIe RST



NOTE:
DIR:DIR Input Circuit Referenced to VCCA.
L:B Data --> A Bus;
H:A Data --> B Bus.

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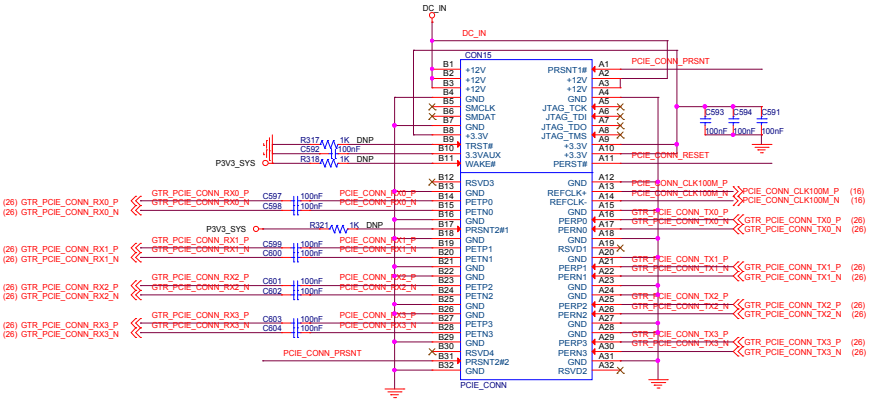
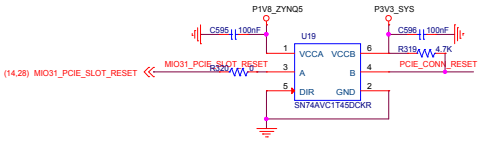
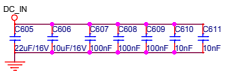
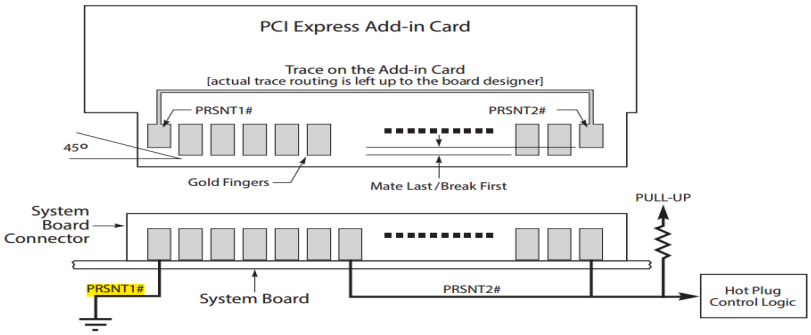
拟制：	审核：	批准：
Title		
Size: A3	SCHEMATIC CODE: ZYNQ PCIE SLOT	Rev: 1.00
	PROJECT NAME: ZYNQ_NVDIMM	
Date: Thursday, January 11, 2018	Sheet 28 of 62	

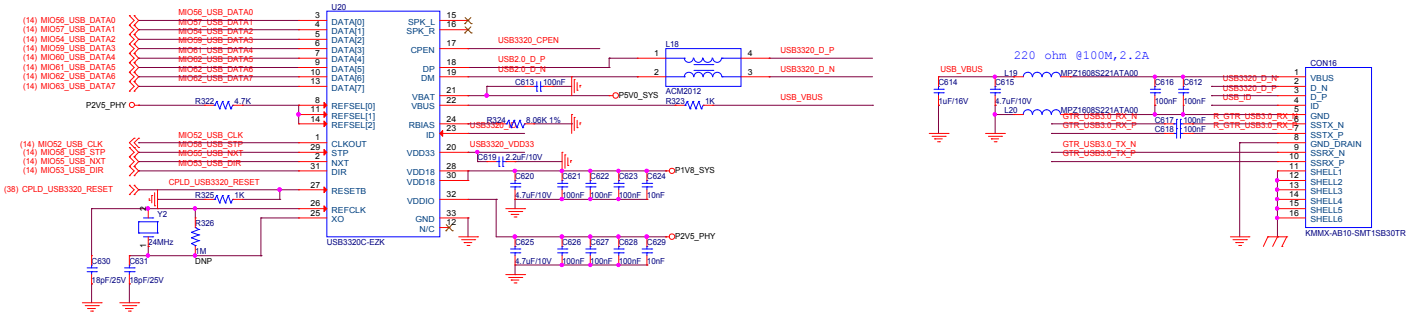


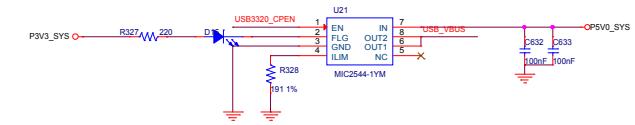


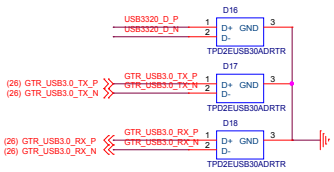




中电海康集团有限公司		
制：	审核：	批准：
Title		
Size: A3	SCHEMATIC CODE: ZYNQ PCIE CONN	Rev: 1.00
	PROJECT NAME: ZYNQ_NvDIMM	
Date: Thursday, January 11, 2018	Sheet 29 of 62	







REQUIRED RVBUS RESISTOR VALUE

Configuration Pins			Description
REFSEL[2]	REFSEL[1]	REFSEL[0]	Reference Frequency
0	0	0	52 MHz
0	0	1	38.4MHz
0	1	0	32MHz
0	1	1	27MHz
1	0	0	26MHz
1	0	1	19.2MHz
1	1	0	20MHz
1	1	1	24MHz

REQUIRED RVBUS RESISTOR VALUE

Operating Mode	Rvbus
Device only	10k ± 5%
OTG	1k ± 5%
Host	10k ± 5%

CAPACITANCE VALUES AT VBUS OF USB CONNECTOR

Mode	MIN Value	MAX Value
Host	120uF	--
Device	1uF	10uF
OTG	1uF	6.5uF

VDDIO:
External 1.8V to 3.3V ULPI supply input pin. This voltage sets the value of VOH for the ULPI signals. This pad needs to be bypassed with a 0.1uF capacitor to ground,placed as close as possible to the USB3320.

VDD18:
External 1.8V Supply input pin. This pad needs to be bypassed with a 0.1uF capacitor to ground, placed as close as possible to the USB3320.

CPEN:
External 5V supply enable. Controls the external VBUS power switch. CPEN is low on POR.

RBIAS:
This pin requires an 8.06k(± 1%) resistor to ground, placed as close as possible to the USB3320. Nominal voltage during ULPI operation is 0.8V.

RESETB,CLKOUT,STP,DIR,NXT,DATA[7:0],REFCLK are referenced to VDDIO

VDD33:
3.3V Regulator Output. A 2.2uF (<1 ohm ESR) bypass capacitor to ground is required for regulator stability. The bypass capacitor should be placed as close as possible to the USB3320.

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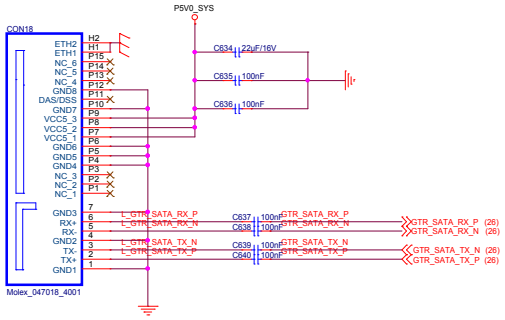
设计：	审核：	批准：
Title		
Size: A3	SCHEMATIC CODE: ZYNQ USB2.0/3.0	Rev: 1.00
	PROJECT NAME: ZYNQ_NvDIMM	
Date: Thursday, January 11, 2018	Sheet 30 of 62	



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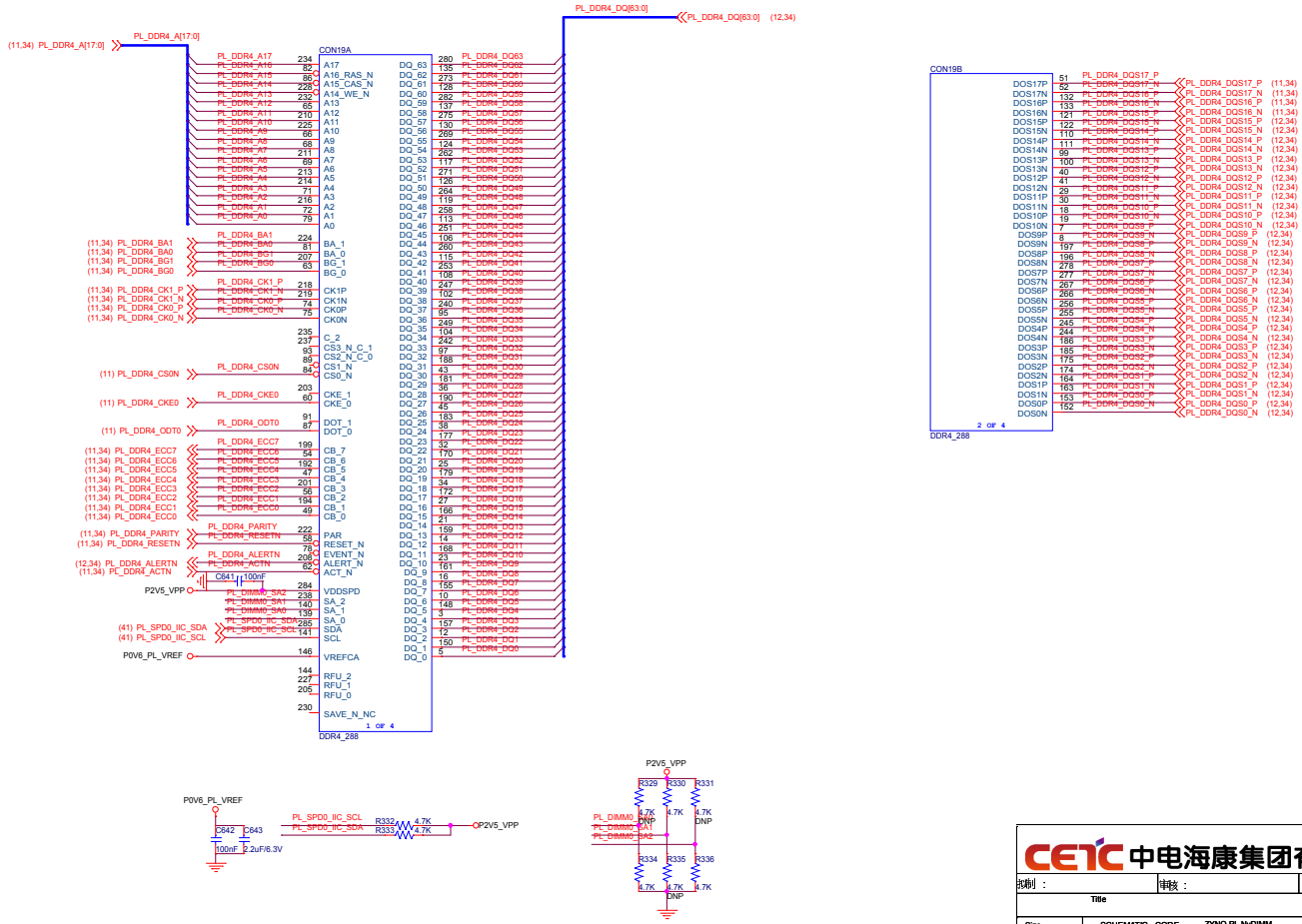
拟制：	审核：	批准：

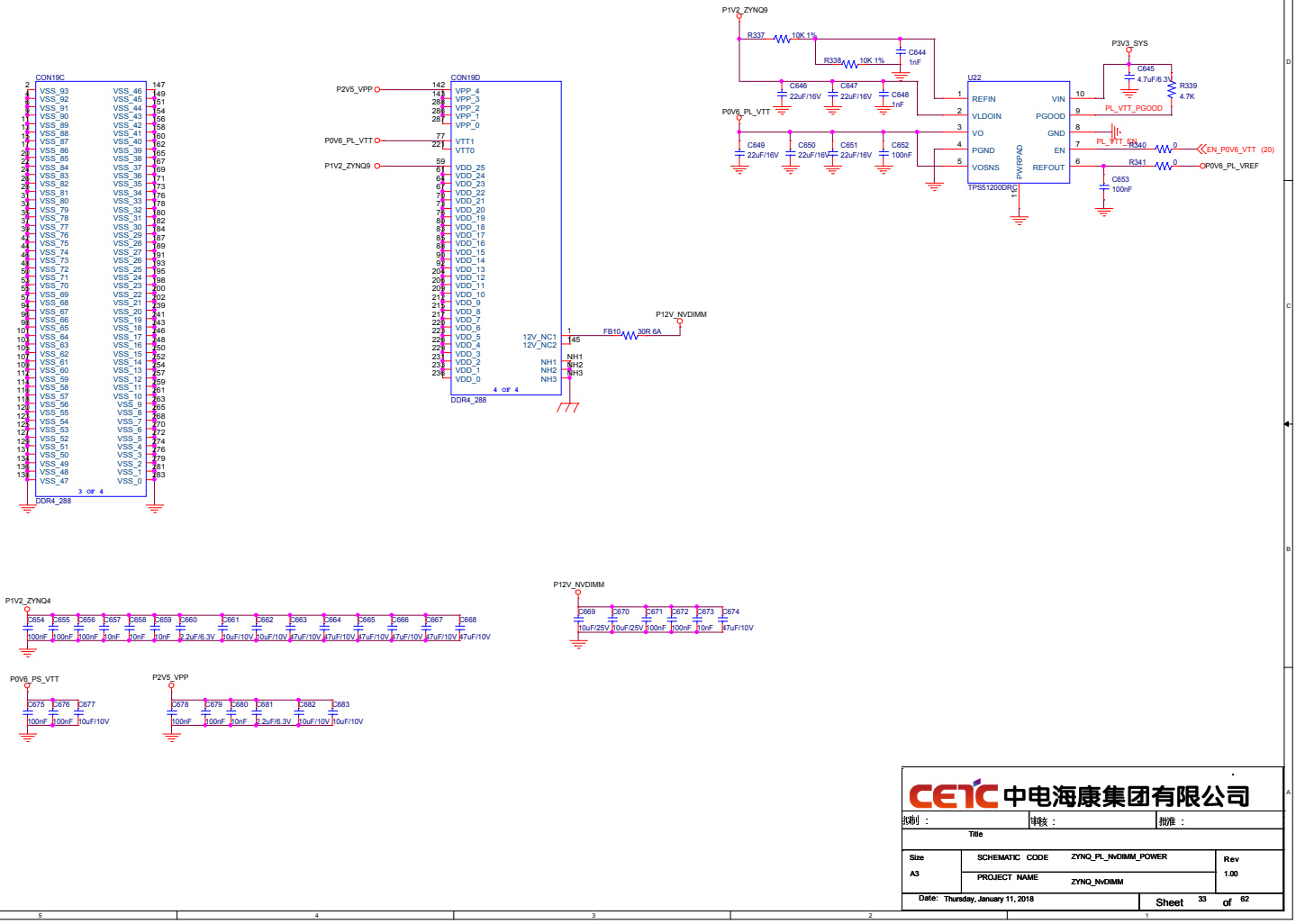
Title

Size	SCHEMATIC CODE	ZYNQ SATA	Rev
A3	PROJECT NAME	ZYNQ_NvDIMM	1.00
Date: Thursday, January 11, 2018	Sheet 31 of 62		



中电海康集团有限公司

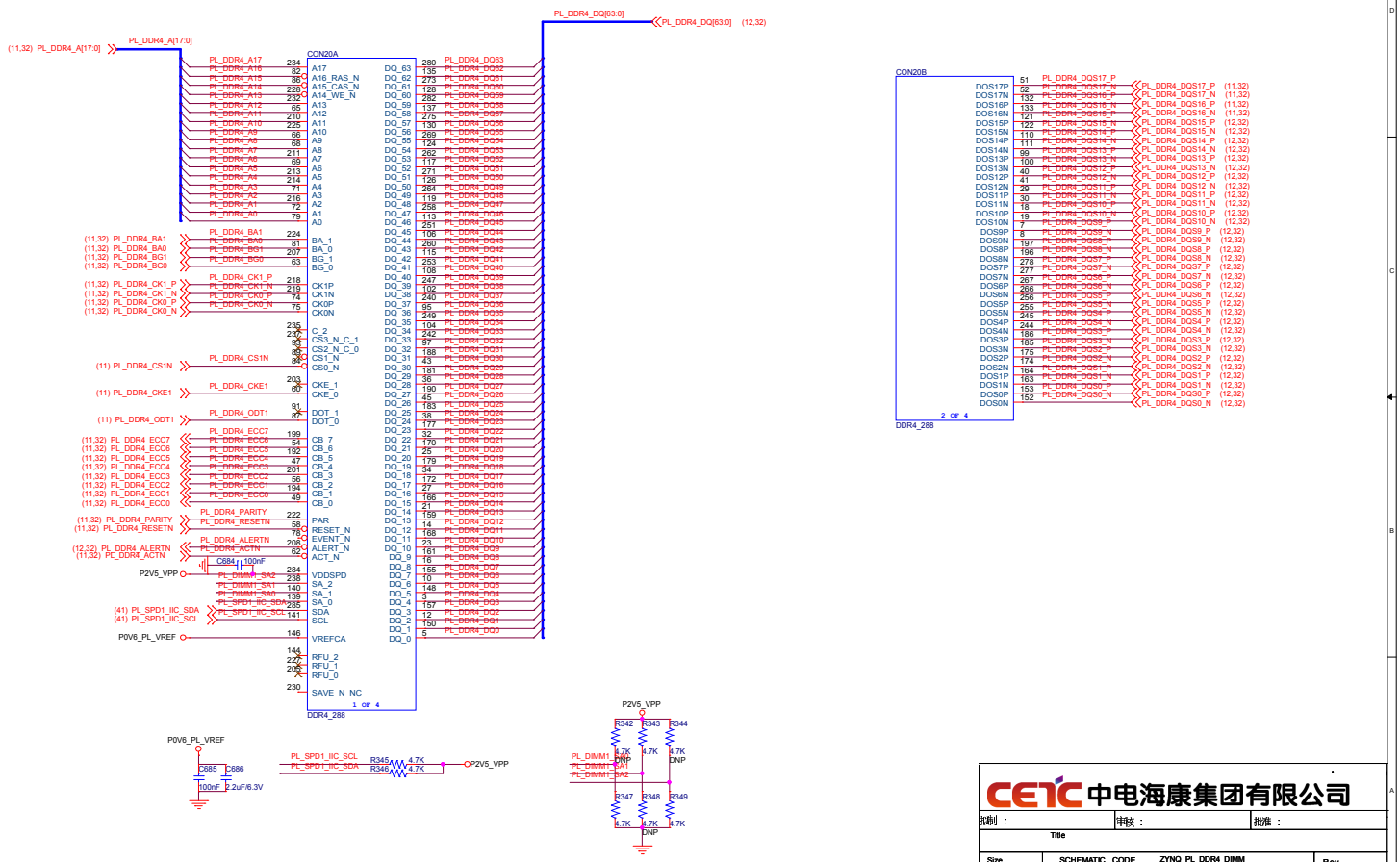
拟制：	审核：	批准：
Title		
Size: A3	SCHEMATIC CODE: ZYNQ PL NvDIMM PROJECT NAME: ZYNQ_NvDIMM	Rev: 1.00
Date: Thursday, January 11, 2018	Sheet 32 of 62	



CETC 中电海康集团有限公司

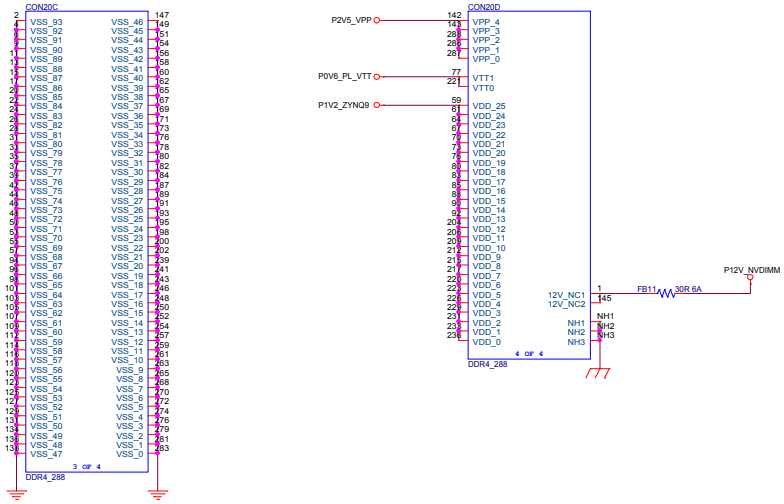
制：	审核：	批准：
Title		

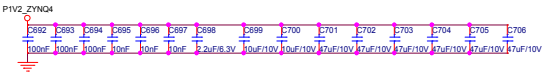
Size	SCHEMATIC CODE	ZYNQ_PL_NvDIMM_POWER	Rev
A3	PROJECT NAME	ZYNQ_NvDIMM	1.00
Date: Thursday, January 11, 2018	Sheet 33 of 62		

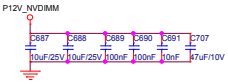


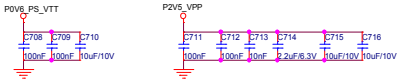
中电海康集团有限公司

拟制：	审核：	批准：
Title		
Size: A3	SCHEMATIC CODE: ZYNQ_PL_DDR4_DIMM PROJECT NAME: ZYNQ_NvDIMM	Rev: 1.00
Date: Thursday, January 11, 2018	Sheet 34 of 62	









中电海康集团有限公司

拟制：	审核：	批准：
Title		
Size: A3	SCHEMATIC CODE: ZYNQ_PL_DDR4_DIMM_POWER PROJECT NAME: ZYNQ_NvDIMM	Rev: 1.00
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CON21A
ASP_134486_01
CON21B
ASP_134486_01
CON21C
ASP_134486_01
CON21D
TP15
ASP_134486_01
CON21E
ASP_134486_01
CON21F
TP14
ASP_134486_01
P3V3_SYS
P12V_FMC_PCIE
P1V8_ADJ
CENC 中电海康集团有限公司
Title
Size A3
SCHEMATIC CODE ZYNQ_PL_FMC1
PROJECT NAME ZYNQ_NvDIMM
Rev 1.00
Date: Thursday, January 11, 2018
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制：	审核：	批准：
Title		
Size: A3	SCHEMATIC CODE: ZYNQ_PL_FMC2	Rev: 1.00
	PROJECT NAME: ZYNQ_NvDIMM	
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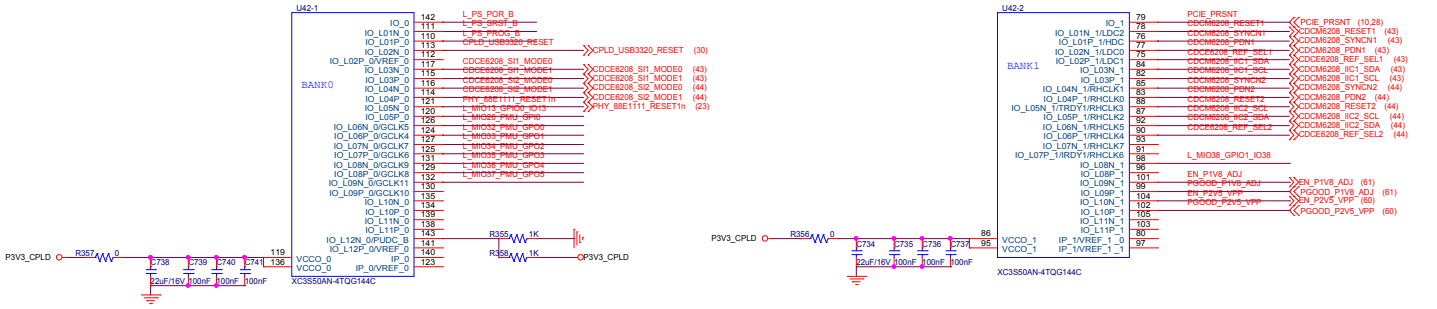
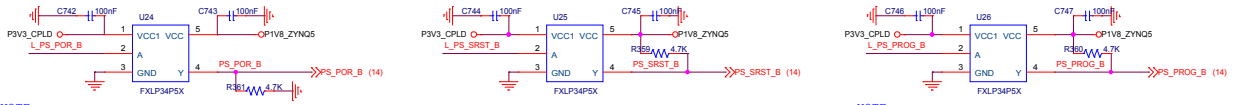




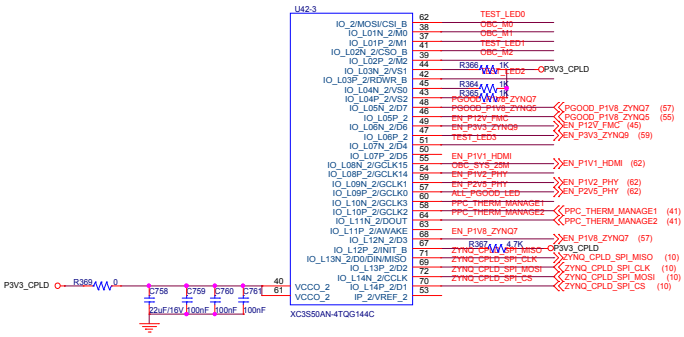
NOTE:
PS_POR_B must be held at 0 until all
PS power supplies meet voltage requirements and
the PS_CLK reference is within specification.

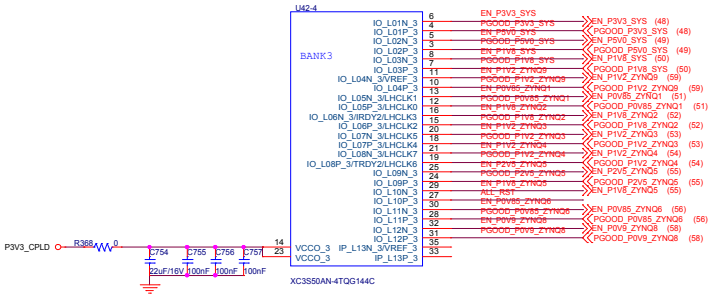
NOTE:
PS_SRST_B:System reset. For use when debugging. When 0,
forces the PS to enter the system reset sequence.

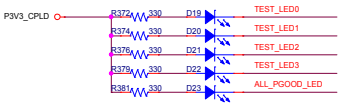
NOTE:
PROG_B signal to reset configuration block. Requires
an external pull-up resistor.

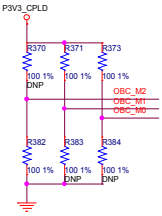
TXS0108
1.2 V to 3.6 V on A Port and 1.65 V to 5.5 V on B Port (VCCA ≤ VCCB)
OE:Referenced to VCCA

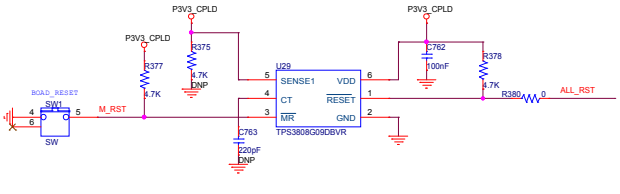
中电海康集团有限公司		
制：	审核：	批准：
Title		
Size: A3	SCHEMATIC CODE: CPLD BANK0/1	Rev: 1.00
	PROJECT NAME: ZYNQ_NvDIMM	
Date: Thursday, January 11, 2018	Sheet 38 of 62	

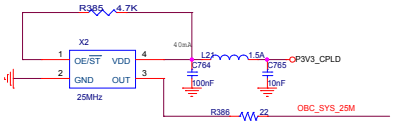












中电海康集团有限公司		
制：	审核：	批准：
Title		
Size: A3	SCHEMATIC CODE: CPLD BNAK2/3	Rev: 1.00
	PROJECT NAME: ZYNQ_NvDIMM	
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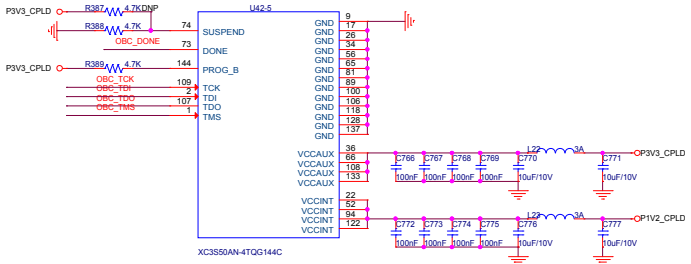

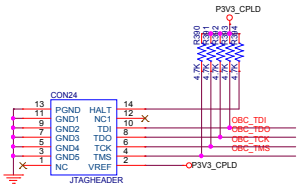

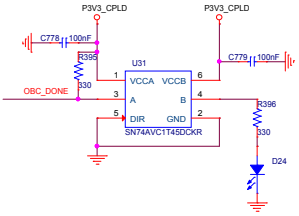

中电海康集团有限公司		
制：	审核：	批准：
Title		
Size: A3	SCHEMATIC CODE: CPLD POWER	Rev: 1.00
	PROJECT NAME: ZYNQ_NvDIMM	
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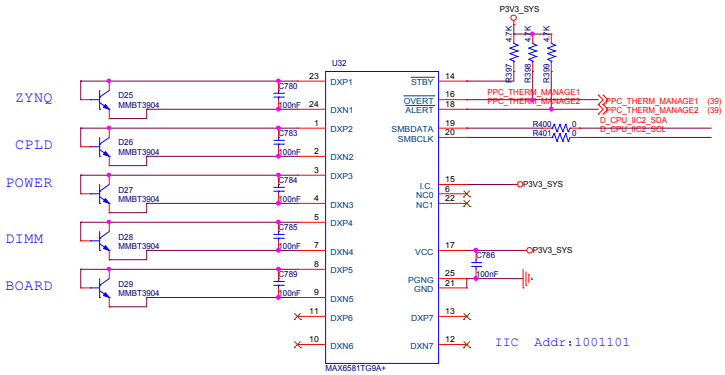

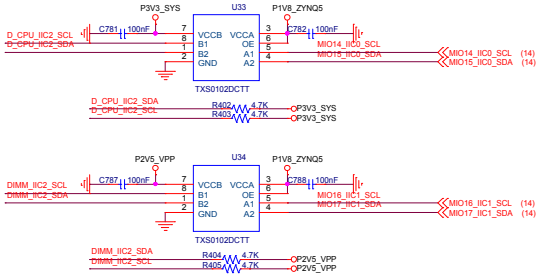

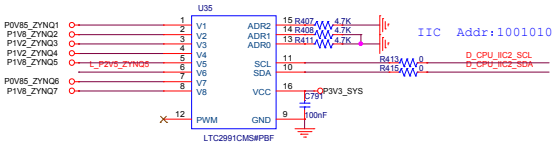

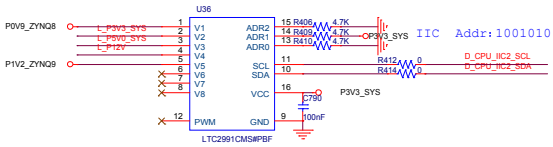

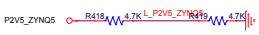

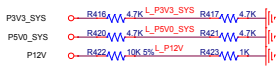

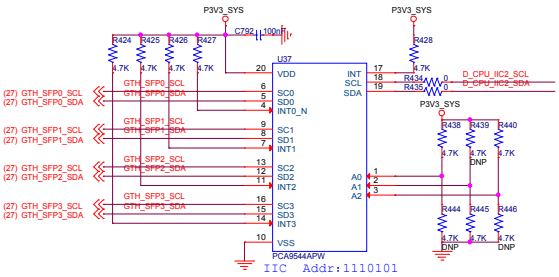

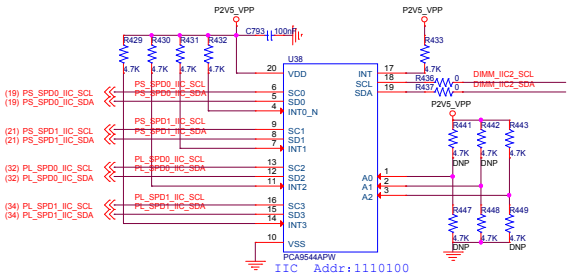

中电海康集团有限公司

拟制：	审核：	批准：

Title

Size	SCHEMATIC CODE	Temp&&Voltage Monitor	Rev
A3	PROJECT NAME	ZYNQ_NvDIMM	1.00

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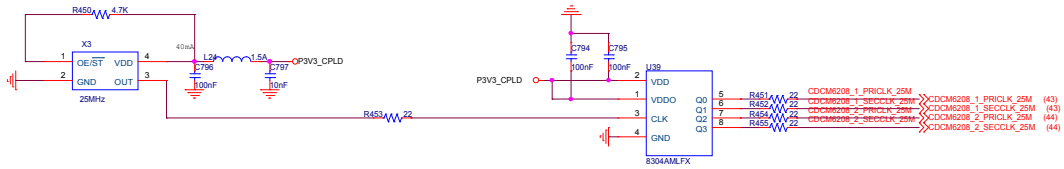

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拟制：	审核：	批准：

Title

Size	SCHEMATIC CODE	CLOCK1	Rev
A3	PROJECT NAME	ZYNQ_NvDIMM	1.00

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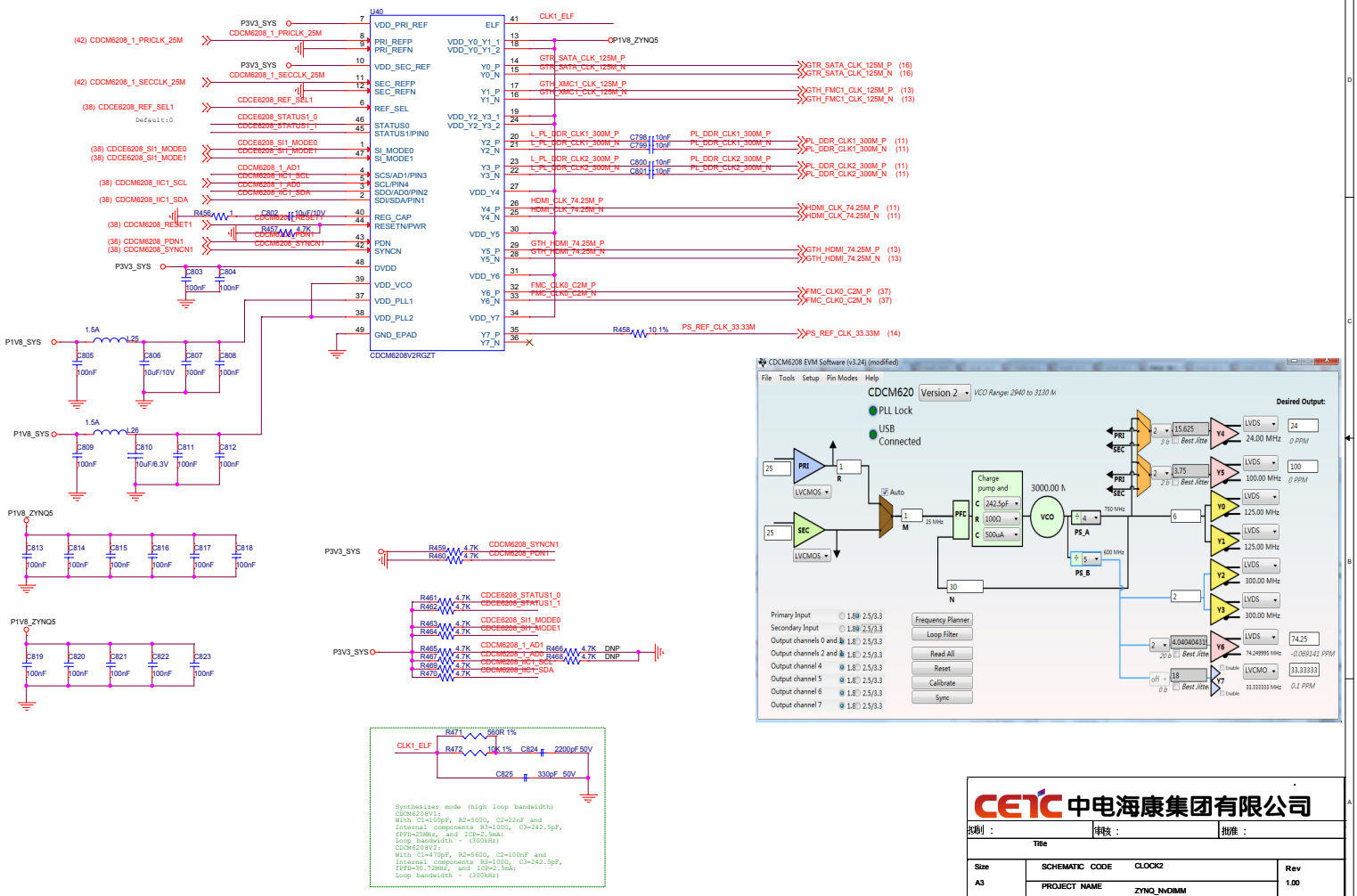

制图：	审核：	批准：
Title		
Size: A3	SCHEMATIC CODE: CLOCK2	Rev: 1.00
	PROJECT NAME: ZYNQ_NvDIMM	
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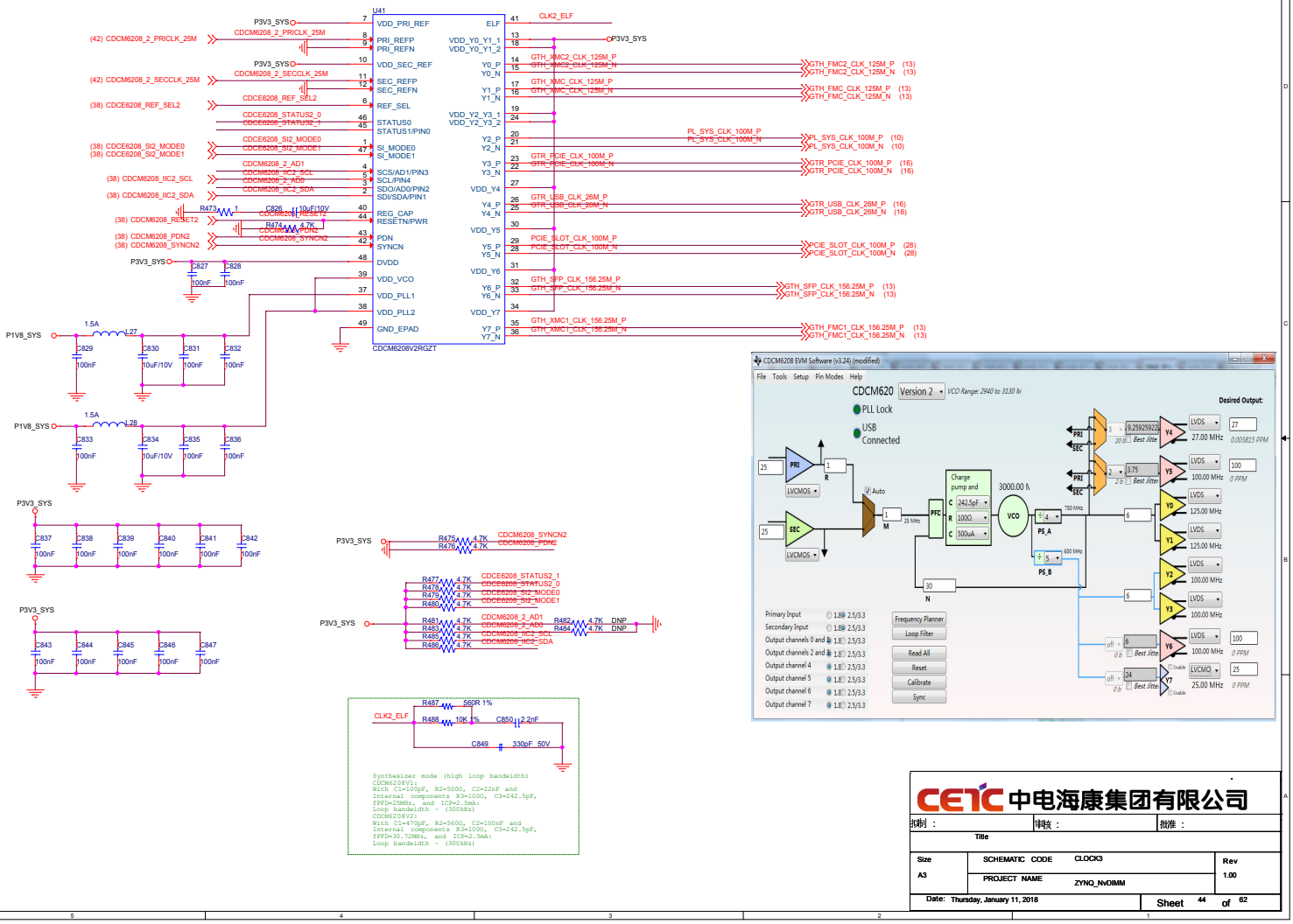

拟制：	审核：	批准：
Title		
Size: A3	SCHEMATIC CODE: CLOCK3	Rev: 1.00
	PROJECT NAME: ZYNQ_NvDIMM	
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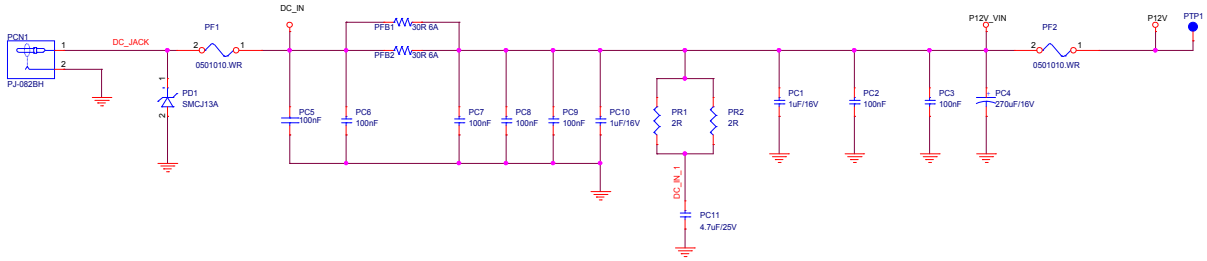

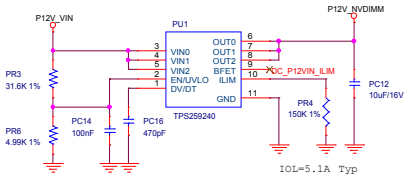

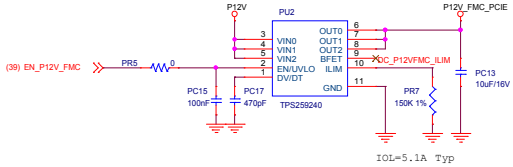

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拟制：	审核：	批准：
Title		
Size: A3	SCHEMATIC CODE: DCIN	Rev: 1.00
	PROJECT NAME: ZYNQ_NvDIMM	
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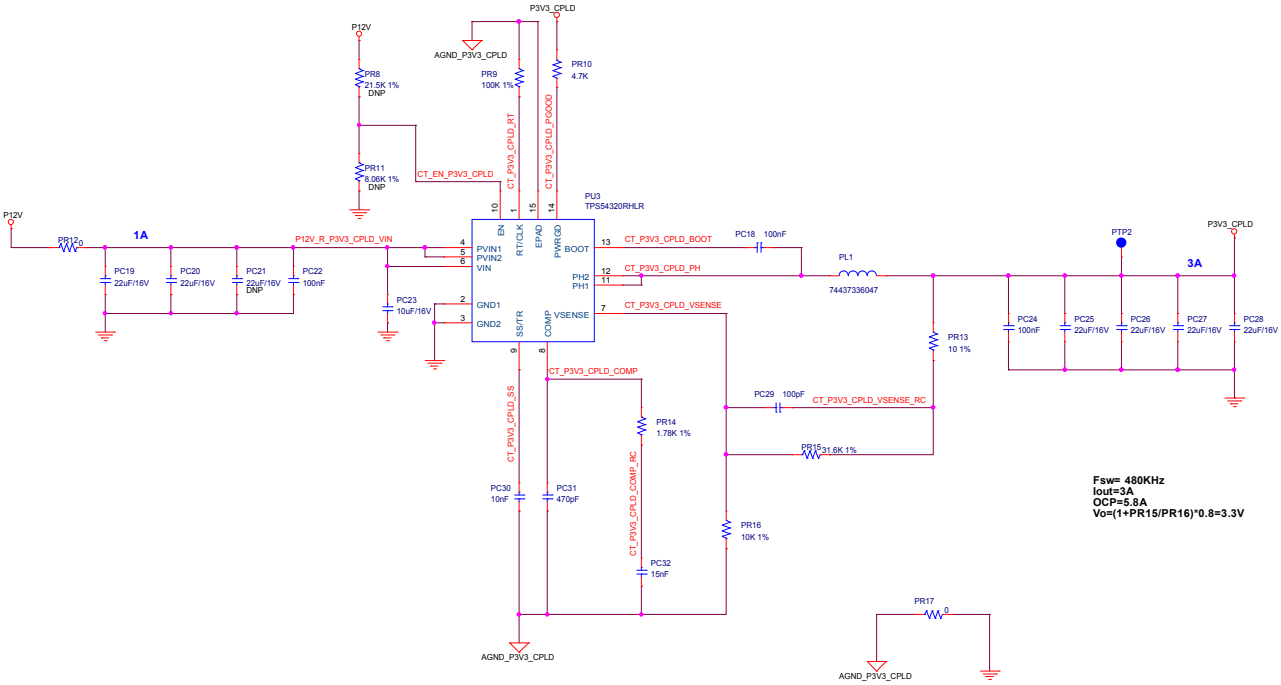

中电海康集团有限公司

绘制：	审核：	批准：

Title

Size	SCHEMATIC CODE	P3V3_CPLD	Rev
A3	PROJECT NAME	ZYNQ_NvDIMM	1.00

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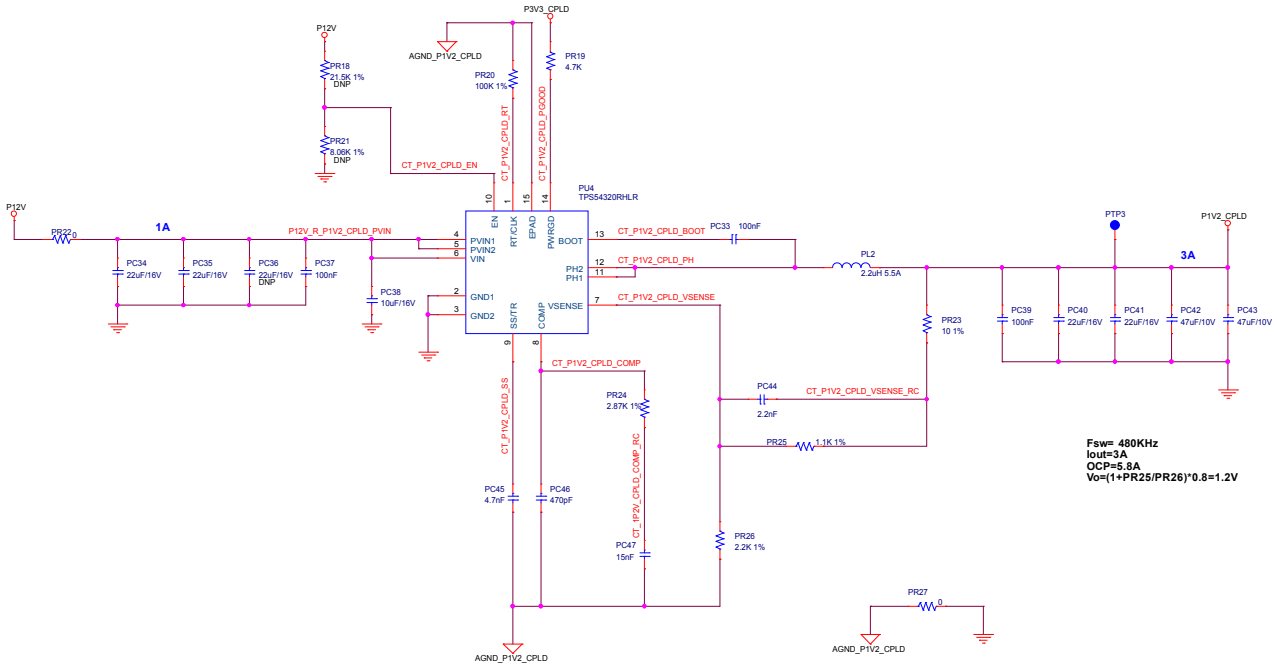

中电海康集团有限公司

拟制：	审核：	批准：

Title

Size	SCHEMATIC CODE	P1V2_CPLD	Rev
A3	PROJECT NAME	ZYNQ_NvDIMM	1.00

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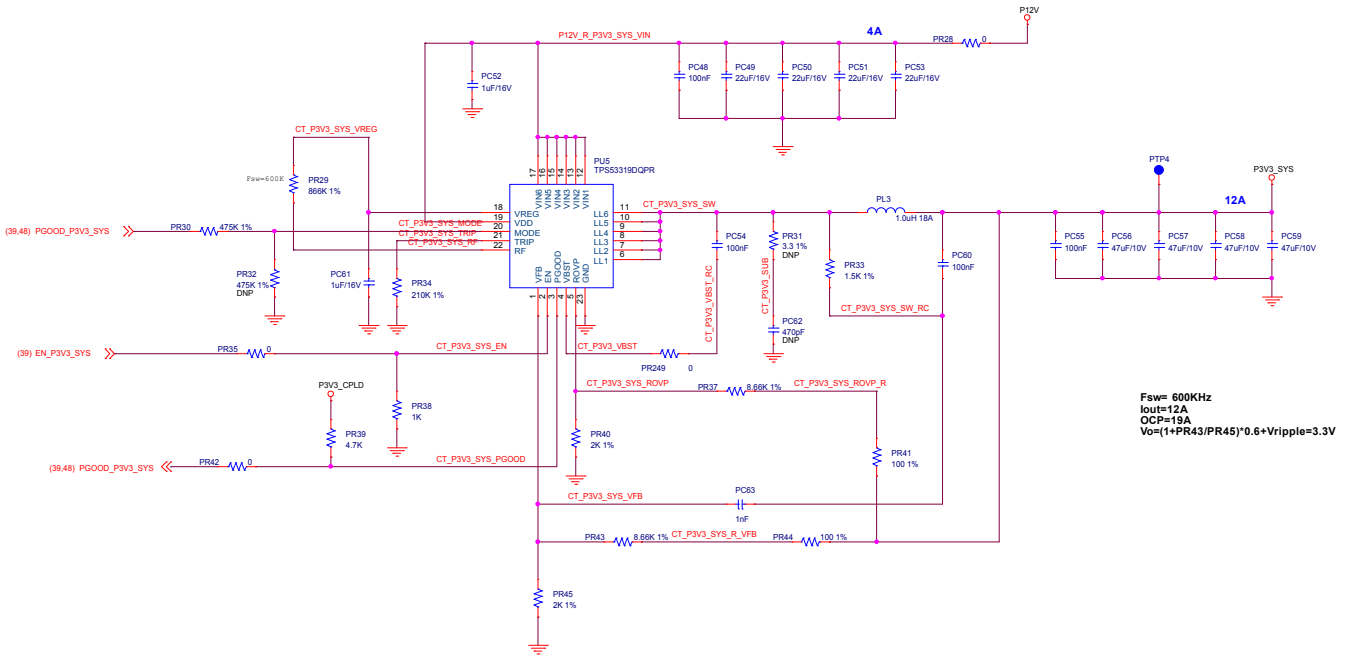

中电海康集团有限公司

拟制：	审核：	批准：

Title

Size	SCHEMATIC CODE	P3V3_SYS	Rev
A3	PROJECT NAME	ZYNQ_NvDIMM	1.00

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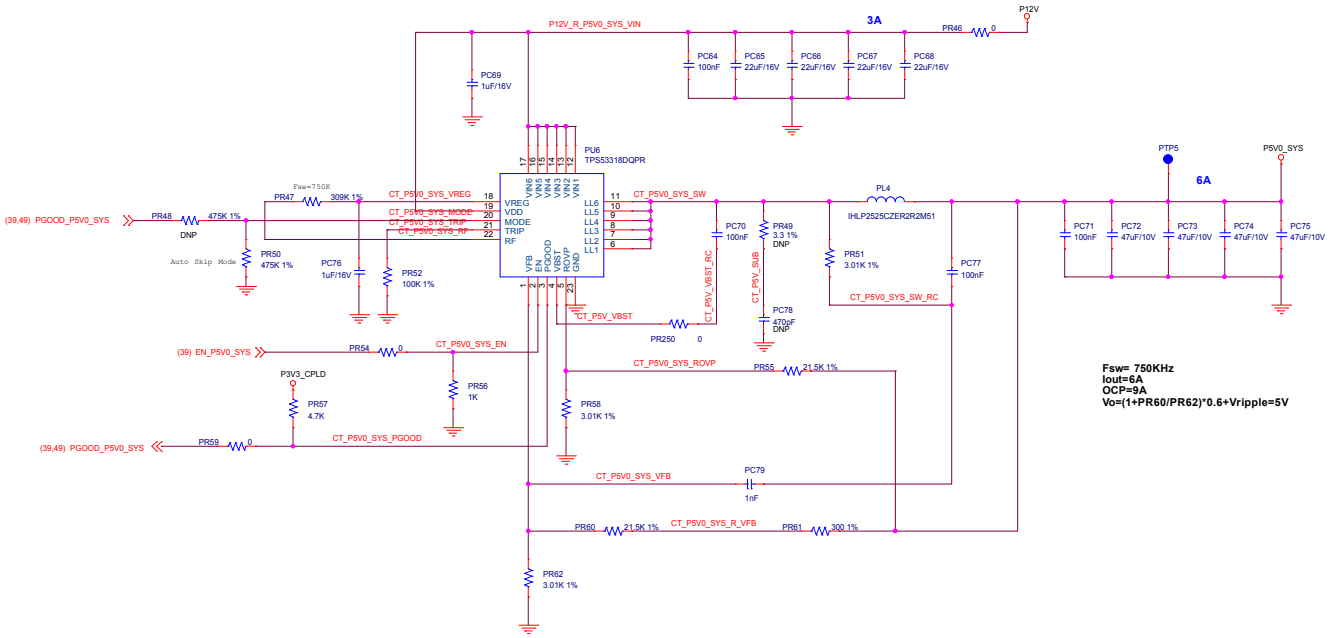
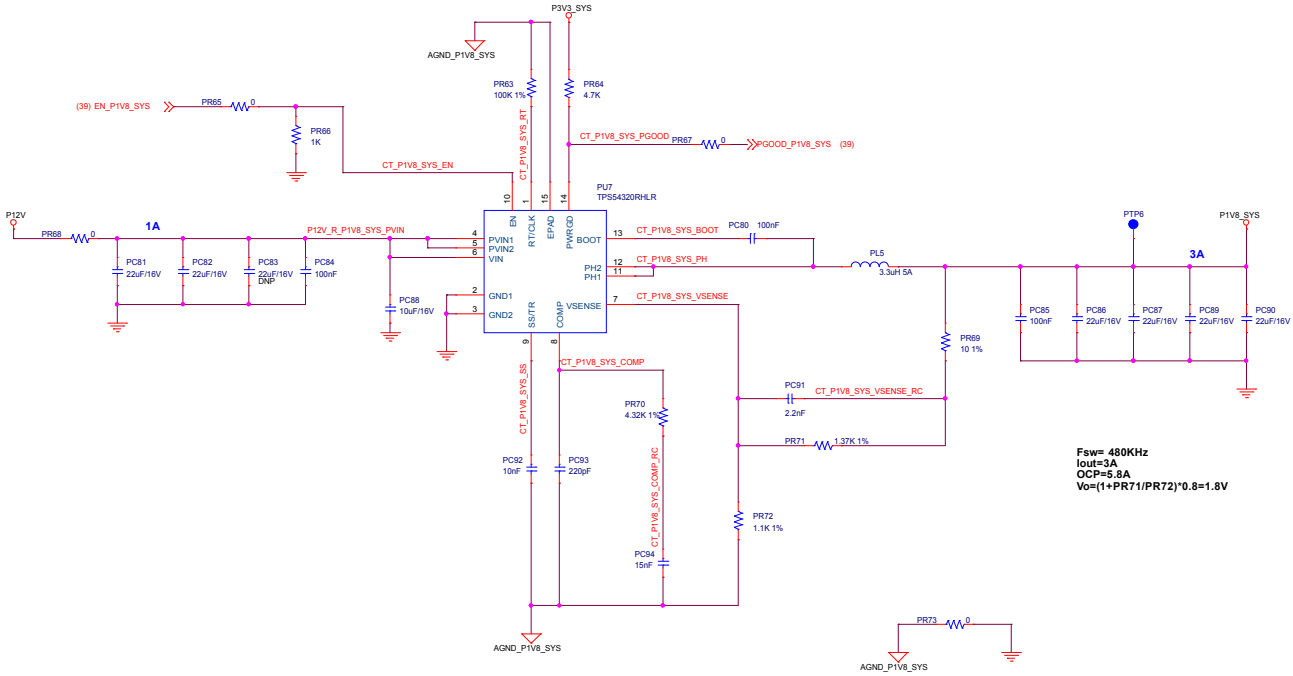


中电海康集团有限公司

拟制：	审核：	批准：

Title

Size	SCHEMATIC CODE	P5V0_SYS	Rev
A3	PROJECT NAME	ZYNQ_NvDIMM	1.00
Date: Thursday, January 11, 2018	Sheet 49 of 62		



中电海康集团有限公司		
制：	审核：	批准：
Title		
Size: A3	SCHEMATIC CODE: P1V8_SYS	Rev: 1.00
	PROJECT NAME: ZYNQ_NvDIMM	
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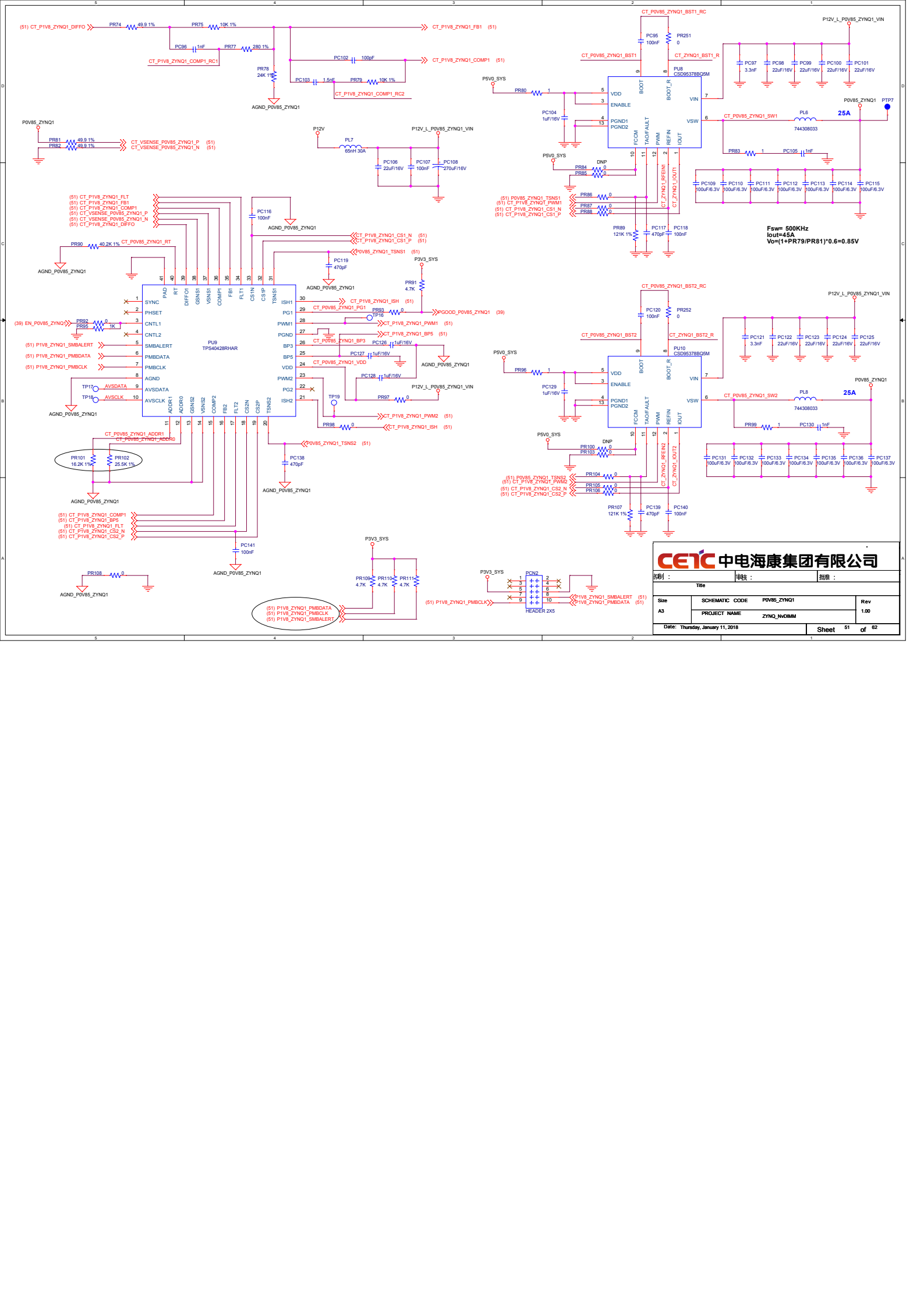
(51) CT_P1V8_ZYNQ1_DIFFO
PR74 49.9 1%
PR75 10K 1%
PC96 1nF
PR77 280 1%
CT_P1V8_ZYNQ1_COMP1_RC1
PR78 24K 1%
AGND_P0V85_ZYNQ1
CT_P1V8_ZYNQ1_FB1 (51)
PC102 100pF
CT_P1V8_ZYNQ1_COMP1 (51)
PC103 1.5nF
PR79 10K 1%
CT_P1V8_ZYNQ1_COMP1_RC2
P0V85_ZYNQ1
PR81 49.9 1%
PR82 49.9 1%
CT_VSENSE_P0V85_ZYNQ1_P (51)
CT_VSENSE_P0V85_ZYNQ1_N (51)
P12V
PL7 65nH 30A
P12V_L_P0V85_ZYNQ1_VIN
PC106 22uF/16V
PC107 100nF
PC108 270uF/16V
(51) CT_P1V8_ZYNQ1_FLT
(51) CT_P1V8_ZYNQ1_FB1
(51) CT_P1V8_ZYNQ1_COMP1
(51) CT_VSENSE_P0V85_ZYNQ1_P
(51) CT_VSENSE_P0V85_ZYNQ1_N
(51) CT_P1V8_ZYNQ1_DIFFO
PC116 100nF
AGND_P0V85_ZYNQ1
CT_P1V8_ZYNQ1_CS1_N (51)
CT_P1V8_ZYNQ1_CS1_P (51)
P0V85_ZYNQ1_TSNS1 (51)
PR90 40.2K 1%
CT_P0V85_ZYNQ1_RT
PC119 470pF
P3V3_SYS
PR91 4.7K
PU9
TPS40428RHAR
SYNC
PHSET
CNTL1
CNTL2
SMBALERT
PMBDATA
PMBCLK
AGND
AVSDATA
AVSCLK
PAD
RT
DIFFO1
GSNS1
VSNS1
COMP1
FB1
FLT1
CS1N
CS1P
TSNS1
ISH1
PG1
PWM1
PGND
BP3
BP5
VDD
PWM2
PG2
ISH2
(39) EN_P0V85_ZYNQ1
PR92 0
PR95 1K
(51) P1V8_ZYNQ1_SMBALERT
(51) P1V8_ZYNQ1_PMBDATA
(51) P1V8_ZYNQ1_PMBCLK
TP17 AVSDATA
TP18 AVSCLK
AGND_P0V85_ZYNQ1
CT_P1V8_ZYNQ1_ISH (51)
CT_P0V85_ZYNQ1_PG1
PR93 0
TP16
PGOOD_P0V85_ZYNQ1 (39)
CT_P1V8_ZYNQ1_PWM1 (51)
CT_P1V8_ZYNQ1_BP5 (51)
CT_P0V85_ZYNQ1_BP3
PC126 1uF/16V
PC127 1uF/16V
CT_P0V85_ZYNQ1_VDD
AGND_P0V85_ZYNQ1
PC128 1uF/16V
P12V_L_P0V85_ZYNQ1_VIN
TP19
PR97 0
CT_P1V8_ZYNQ1_PWM2 (51)
PR98 0
CT_P1V8_ZYNQ1_ISH (51)
P0V85_ZYNQ1_TSNS2 (51)
CT_P0V85_ZYNQ1_ADDR1
CT_P0V85_ZYNQ1_ADDR0
PR101 16.2K 1%
PR102 25.5K 1%
AGND_P0V85_ZYNQ1
PC138 470pF
AGND_P0V85_ZYNQ1
(51) CT_P1V8_ZYNQ1_COMP1
(51) CT_P1V8_ZYNQ1_BP5
(51) CT_P1V8_ZYNQ1_FLT
(51) CT_P1V8_ZYNQ1_CS2_N
(51) CT_P1V8_ZYNQ1_CS2_P
PC141 100nF
AGND_P0V85_ZYNQ1
PR108 0
AGND_P0V85_ZYNQ1
P3V3_SYS
PR109 4.7K
PR110 4.7K
PR111 4.7K
(51) P1V8_ZYNQ1_PMBDATA
(51) P1V8_ZYNQ1_PMBCLK
(51) P1V8_ZYNQ1_SMBALERT
P3V3_SYS
PCN2
HEADER 2X5
(51) P1V8_ZYNQ1_PMBCLK
P1V8_ZYNQ1_SMBALERT (51)
P1V8_ZYNQ1_PMBDATA (51)
CT_P0V85_ZYNQ1_BST1_RC
PC95 100nF
PR251 0
CT_P0V85_ZYNQ1_BST1
CT_ZYNQ1_BST1_R
PU8
CSD95378BQ5M
P5V0_SYS
PR80 1
VDD
ENABLE
PGND1
PGND2
BOOT
BOOT_R
VIN
VSW
FCCM
TAO/FAULT
PWM
REFIN
IOUT
PC104 1uF/16V
P5V0_SYS
DNP
PR84 0
PR85 0
CT_ZYNQ1_RFEIN
CT_ZYNQ1_IOUT1
(51) P0V85_ZYNQ1_TSNS1
(51) CT_P1V8_ZYNQ1_PWM1
(51) CT_P1V8_ZYNQ1_CS1_N
(51) CT_P1V8_ZYNQ1_CS1_P
PR86 0
PR87 0
PR88 0
PR89 121K 1%
PC117 470pF
PC118 100nF
P12V_L_P0V85_ZYNQ1_VIN
PC97 3.3nF
PC98 22uF/16V
PC99 22uF/16V
PC100 22uF/16V
PC101 22uF/16V
P0V85_ZYNQ1
PTP7
CT_P0V85_ZYNQ1_SW1
PL6
25A
744308033
PR83 1
PC105 1nF
PC109 100uF/6.3V
PC110 100uF/6.3V
PC111 100uF/6.3V
PC112 100uF/6.3V
PC113 100uF/6.3V
PC114 100uF/6.3V
PC115 100uF/6.3V
Fsw= 500KHz
Iout=45A
Vo=(1+PR79/PR81)*0.6=0.85V
CT_P0V85_ZYNQ1_BST2_RC
PC120 100nF
PR252 0
CT_P0V85_ZYNQ1_BST2
CT_ZYNQ1_BST2_R
PU10
CSD95378BQ5M
P5V0_SYS
PR96 1
PC129 1uF/16V
P12V_L_P0V85_ZYNQ1_VIN
PC121 3.3nF
PC122 22uF/16V
PC123 22uF/16V
PC124 22uF/16V
PC125 22uF/16V
P0V85_ZYNQ1
CT_P0V85_ZYNQ1_SW2
PL8
25A
744308033
P5V0_SYS
DNP
PR100 0
PR103 0
PR99 1
PC130 1nF
PC131 100uF/6.3V
PC132 100uF/6.3V
PC133 100uF/6.3V
PC134 100uF/6.3V
PC135 100uF/6.3V
PC136 100uF/6.3V
PC137 100uF/6.3V
PR104 0
(51) P0V85_ZYNQ1_TSNS2
(51) CT_P1V8_ZYNQ1_PWM2
(51) CT_P1V8_ZYNQ1_CS2_N
(51) CT_P1V8_ZYNQ1_CS2_P
PR105 0
PR106 0
CT_ZYNQ1_RFEIN2
CT_ZYNQ1_IOUT2
PR107 121K 1%
PC139 470pF
PC140 100nF
中电海康集团有限公司
制：
审核：
批准：
Title
Size
A3
SCHEMATIC CODE P0V85_ZYNQ1
PROJECT NAME ZYNQ_NvDIMM
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1.00
Date: Thursday, January 11, 2018
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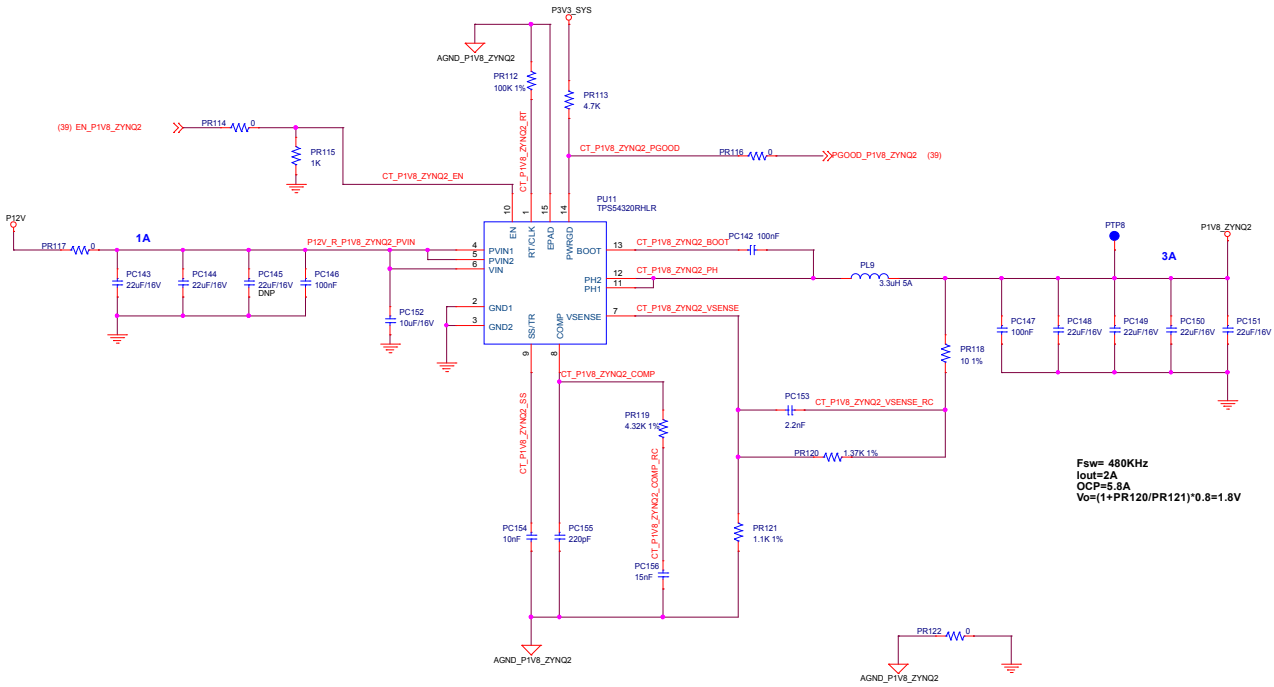

中电海康集团有限公司

制：	审核：	批准：
Title		
Size: A3	SCHEMATIC CODE: P1V8_ZYNQ2 PROJECT NAME: ZYNQ_NvDIMM	Rev: 1.00
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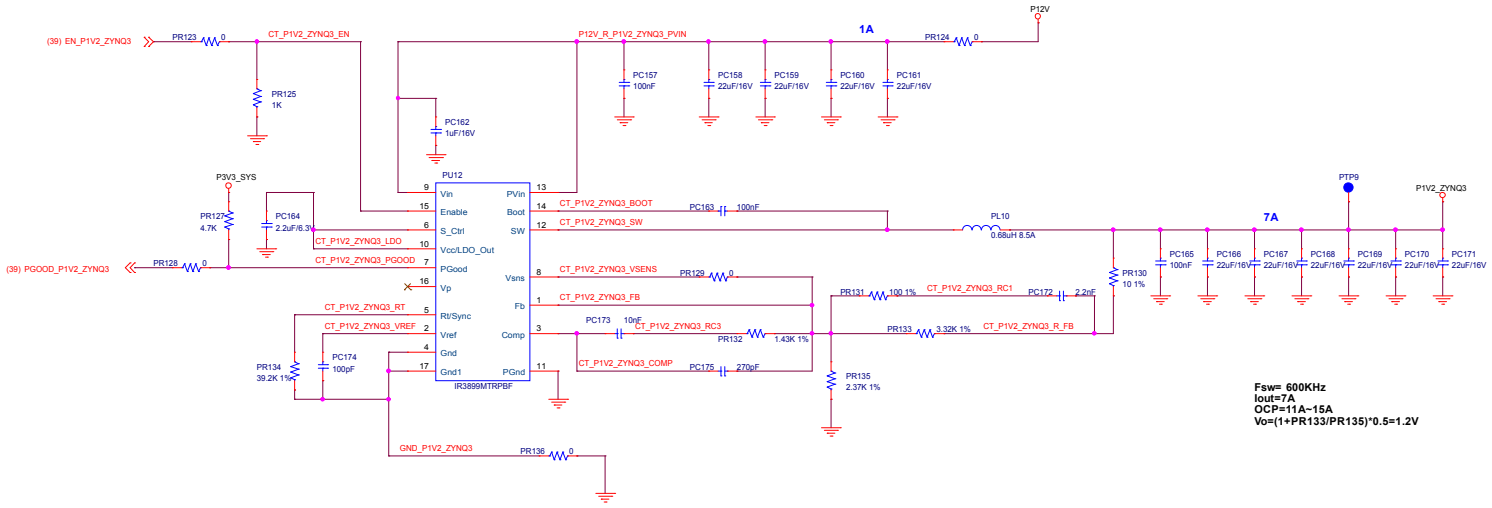

中电海康集团有限公司		
制：	审核：	批准：
Title		
Size: A3	SCHEMATIC CODE: P1V2_ZYNQ3	Rev: 1.00
	PROJECT NAME: ZYNQ_NvDIMM	
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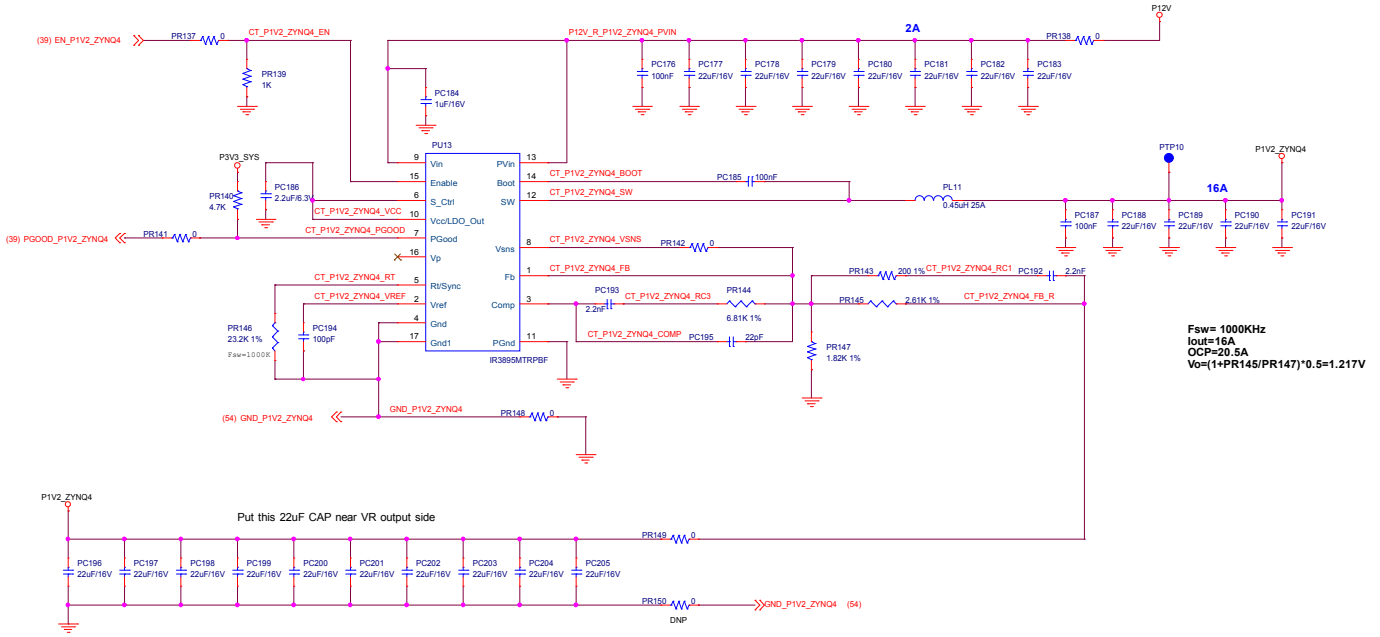

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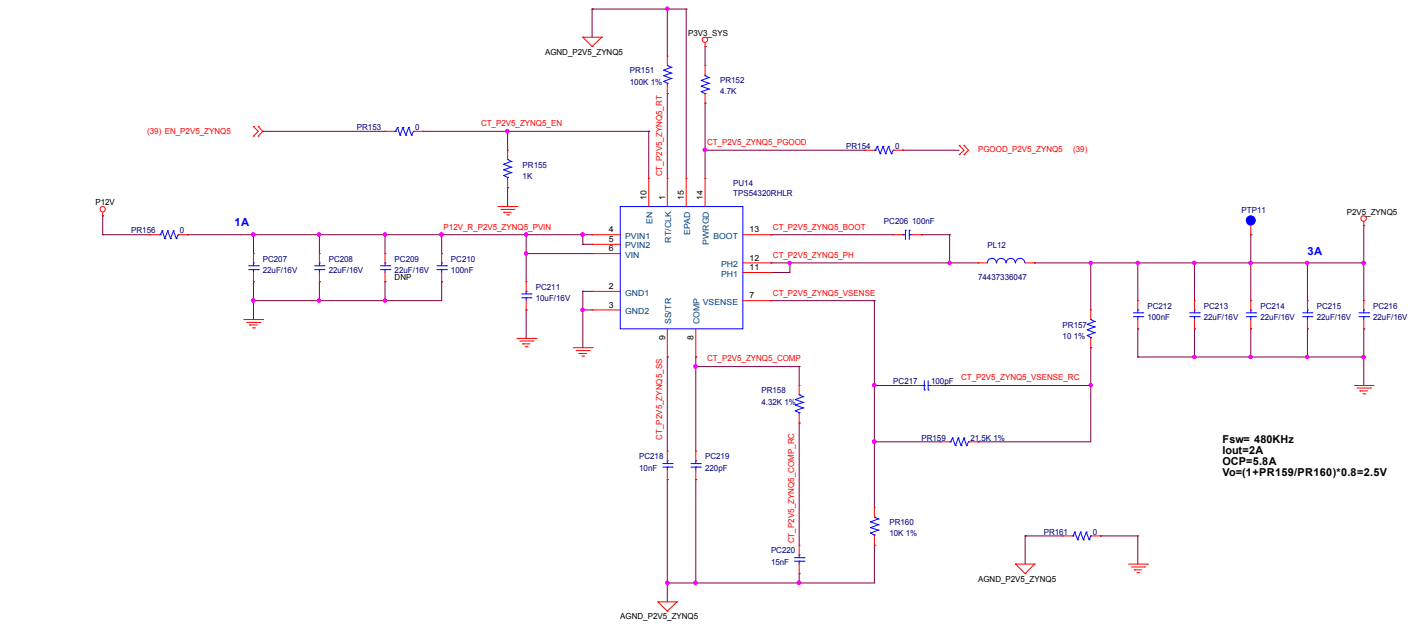
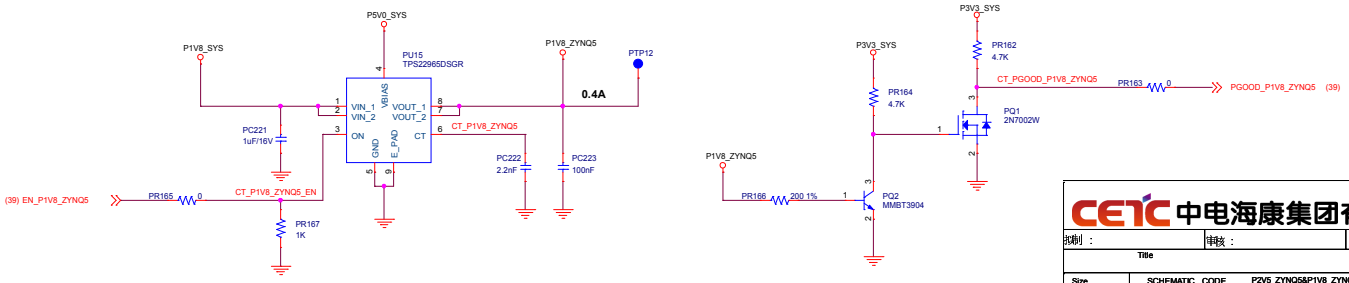
制：	审核：	批准：

Title

Size	SCHEMATIC CODE	P1V2_ZYNQ4	Rev
A3	PROJECT NAME	ZYNQ_NvDIMM	1.00
Date: Thursday, January 11, 2018	Sheet 54 of 62		





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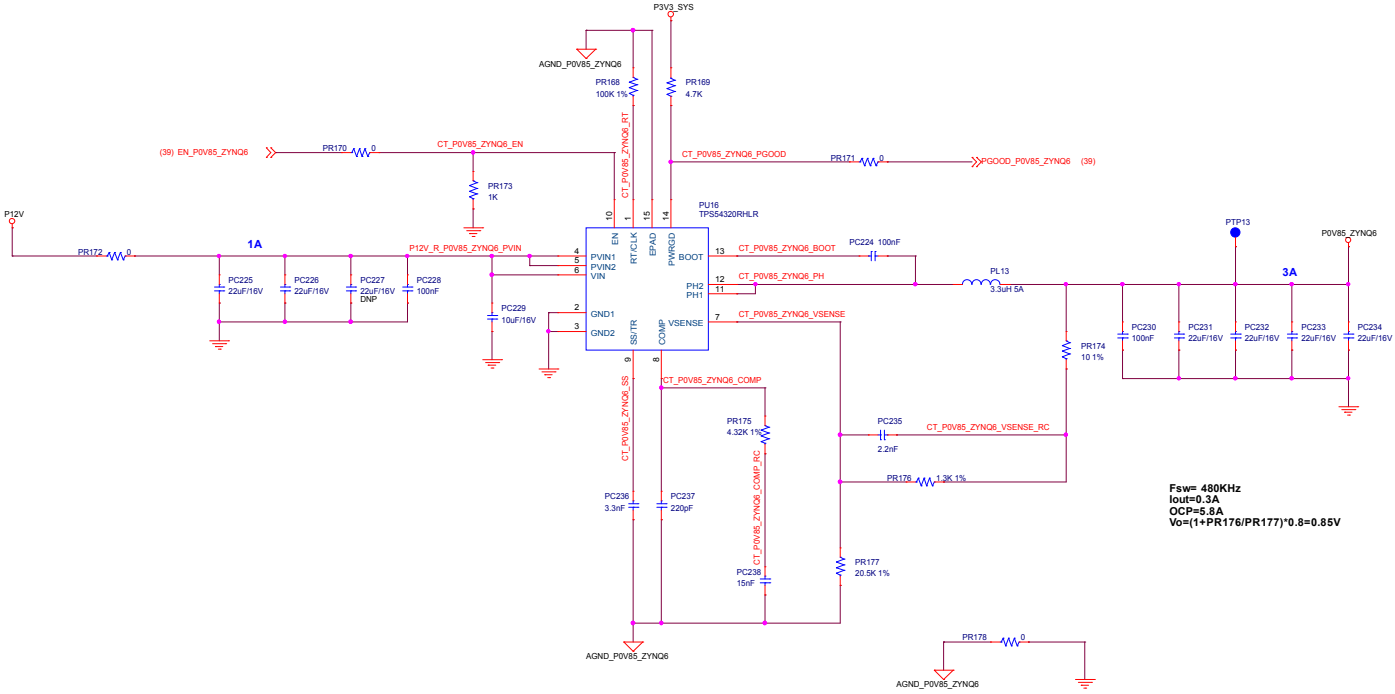
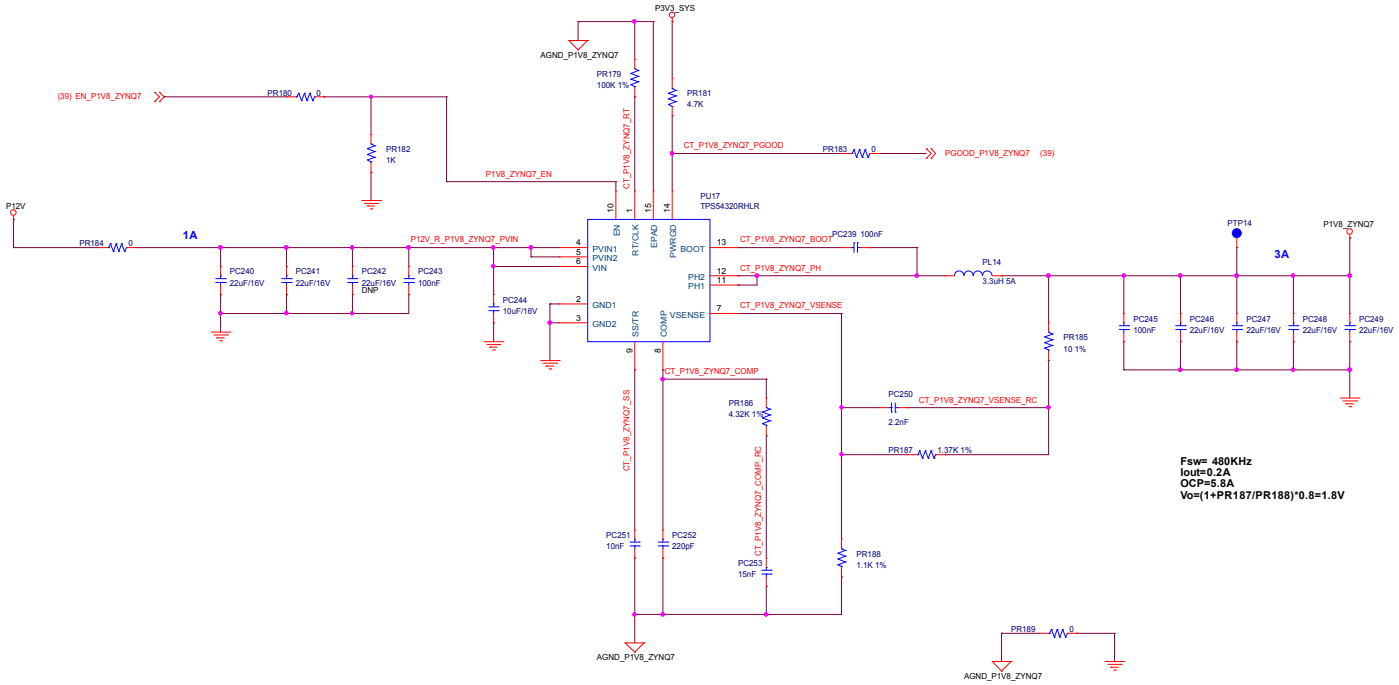
制：	审核：	批准：
Title		
Size: A3	SCHEMATIC CODE: P2V5_ZYNQ5&P1V8_ZYNQ5	Rev: 1.00
	PROJECT NAME: ZYNQ_NvDIMM	
Date: Thursday, January 11, 2018	Sheet 55 of 62	



中电海康集团有限公司		
制：	审核：	批准：
Title		
Size: A3	SCHEMATIC CODE: P0V85_ZYNQ6	Rev: 1.00
	PROJECT NAME: ZYNQ_NvDIMM	
Date: Thursday, January 11, 2018	Sheet 56 of 62	



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制：	审核：	批准：

Title

Size	SCHEMATIC CODE	P1V8_ZYNQ7	Rev
A3	PROJECT NAME	ZYNQ_NvDIMM	1.00
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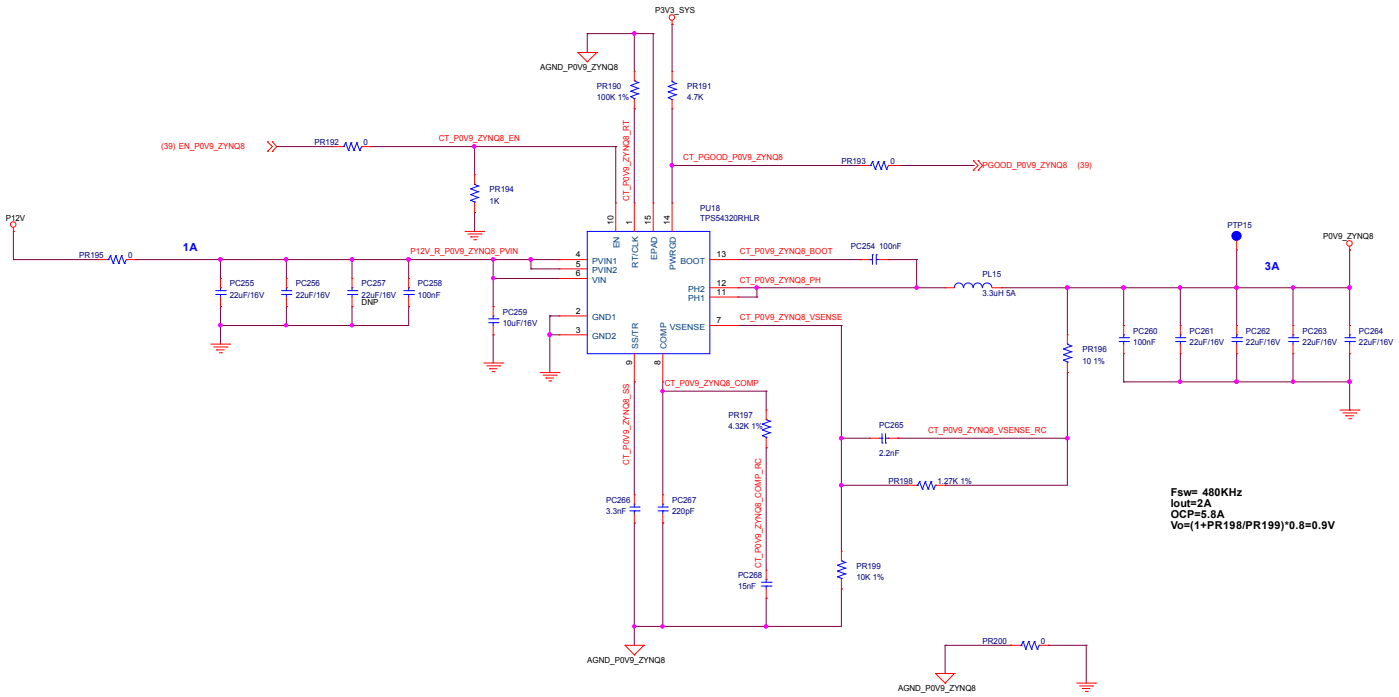

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Size	SCHEMATIC CODE	P0V9_ZYNQ8	Rev
A3	PROJECT NAME	ZYNQ_NvDIMM	1.00

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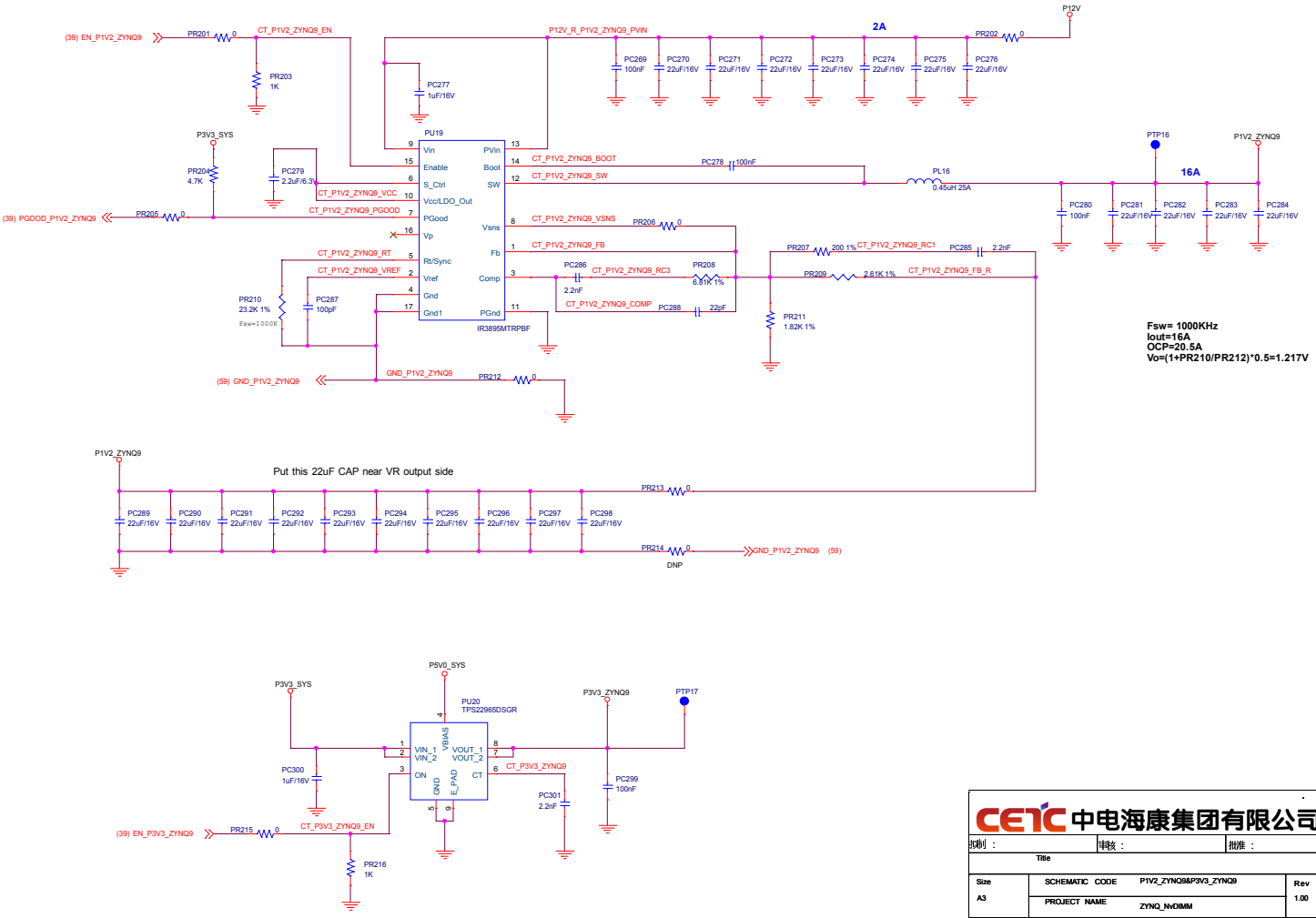

中电海康集团有限公司		
制：	审核：	批准：
Title		
Size: A3	SCHEMATIC CODE: P1V2_ZYNQ9&P3V3_ZYNQ9	Rev: 1.00
	PROJECT NAME: ZYNQ_NvDIMM	
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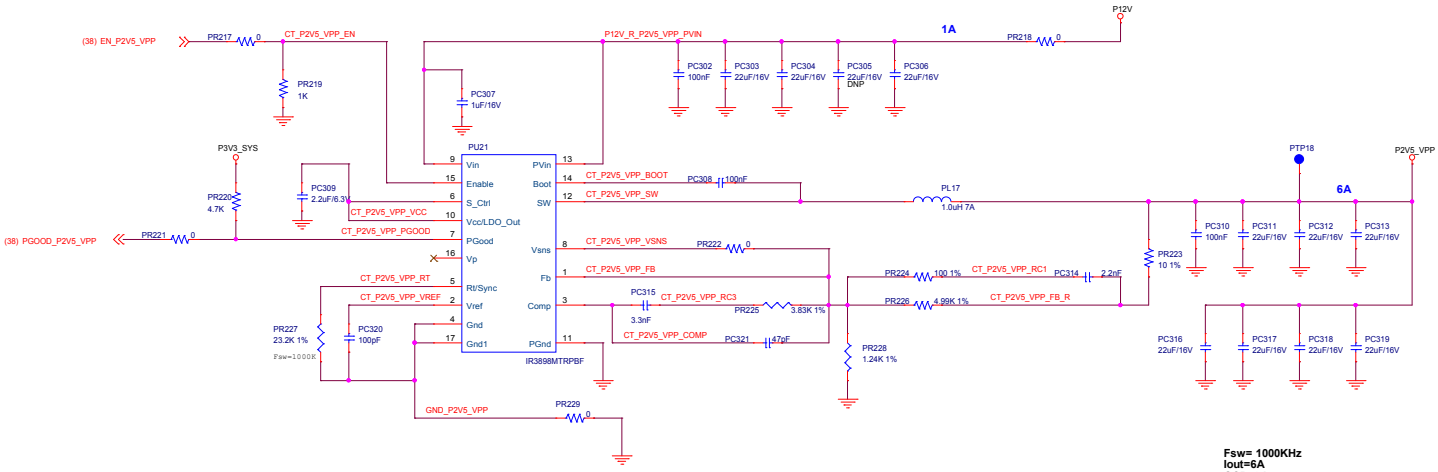

Fsw= 1000KHz
Iout=6A
OCP=9A
Vo=(1+PR227/PR229)*0.5=2.51V

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Title

Size	SCHEMATIC CODE	P2V5_VPP	Rev
A3	PROJECT NAME	ZYNQ_NvDIMM	1.00

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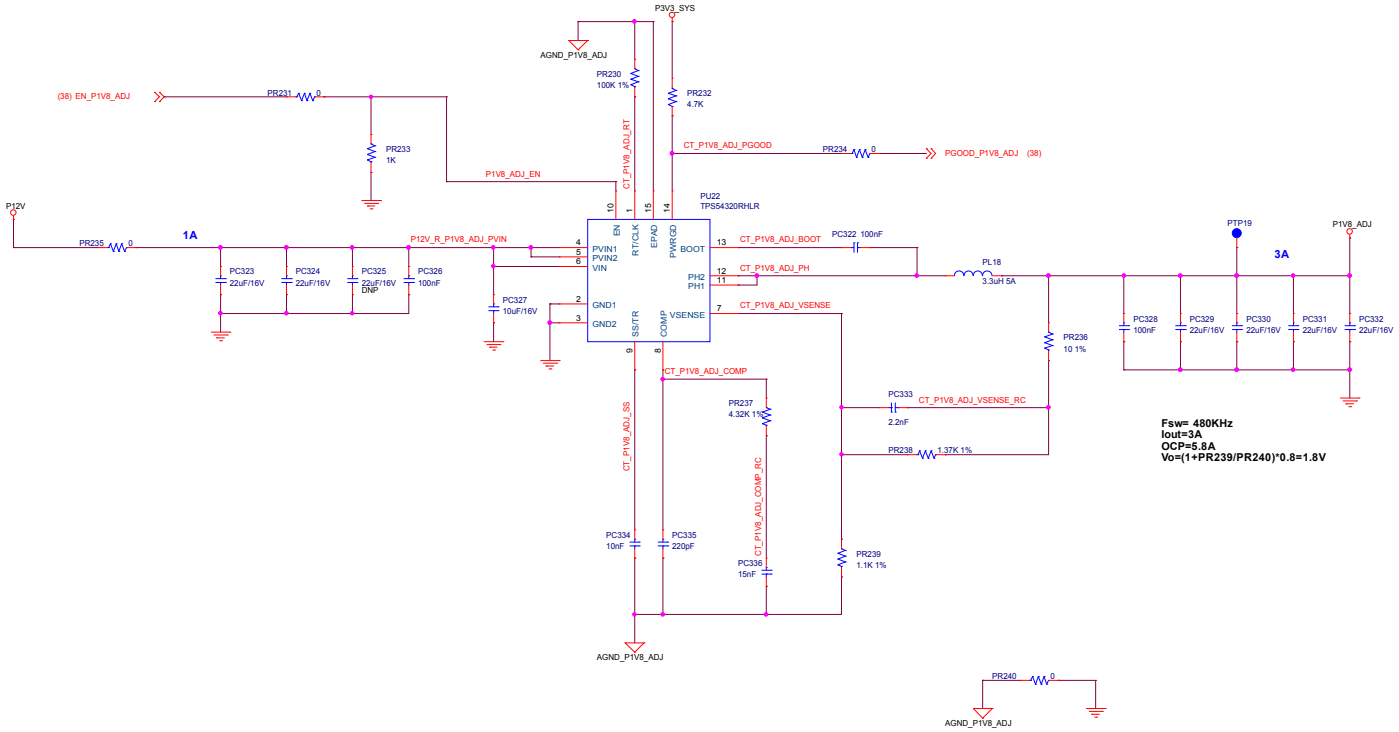

中电海康集团有限公司		
制：	审核：	批准：
Title		
Size: A3	SCHEMATIC CODE: P1V8_ADJ PROJECT NAME: ZYNQ_NvDIMM	Rev: 1.00
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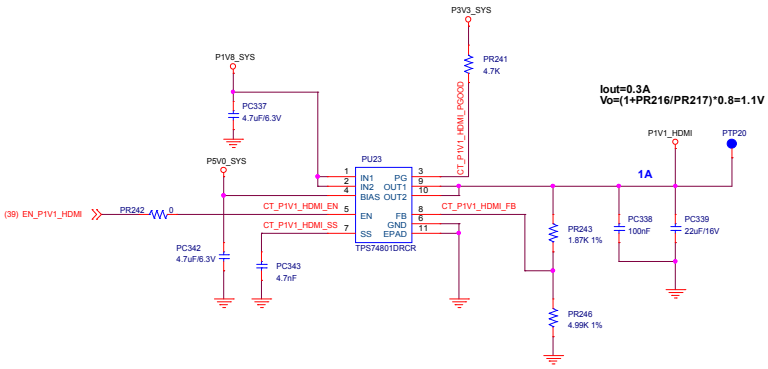

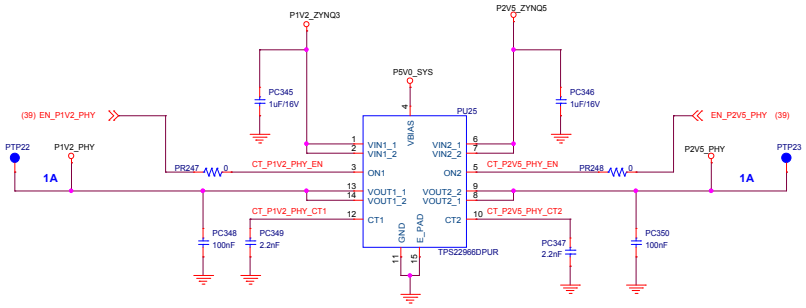

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制：	审核：	批准：

Title

Size	SCHEMATIC CODE	Other Power	Rev
A3	PROJECT NAME	ZYNQ_NvDIMM	1.00

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