SFQ Wafer T053017A
Processing Report

Contents

1 Layer M1

Bottom electrode of JJ stack and DC/SFQ shunt inductor.

2 Layer V2

JJ pocket definition in dielectric.

2.1 PECVD Deposition (Aug 01, 2017)

Ezpz

2.1.1 Parameters

DC Response (V)	-18
Deposition Material	SiOx
Platen Temperature (C)	250
Recipe Name (ch1)	SiOxide2
Thickness Target (nm)	180
Tool	PT 70

2.1.2 Steps

1) Pre-clean Time (x2, s): 150
2) Pre-seed Time (s): 500
3) Deposition Time (s): 350

2.2 Etching (Aug 01, 2017)

Etch the Ezpz

2.2.1 Parameters

DC Response (V)	272
Etched Material	PECVD SiOx
Platen	Carbon
Recipe Name	50CHF3
Tool	Unaxis 790

2.2.2 Steps

4) Pre-clean Time (s): 300
5) Pre-seed Time (s): 0
6) Etch Time (s): 480

3 Layer M2

JJ oxidation and wiring layer.