Buck Converter Nonidealities and their Influence on Design

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Contents

Abstract:

The intent of this report is to investigate the most common nonidealities plaguing the buck converter and determine those most harmful to a design. The ideal buck design analysis is sufficient for simulation, but how does it compare to practical implementations. The insight gained by investigating the various nonidealities will ultimately assist the designer in shifting losses across components and in choosing the most appropriate component. A reference buck converter design will be provided using sample component values of readily available components. After addressing the barriers to practical implementation the Synchronous buck converter will be analyzed and simulated. The synchronous topology is discussed to address issues regarding losses and design tradeoffs. The paper will conclude a discussion of the synchronous buck's disadvantages, both practically and in simulating the converter.

Motivation:

The figure below, provided by Wurth Electroniks®, highlights the performance characteristics of the most common isolated and non-isolated DC-DC converters. The figure is a reduced form of the chart containing only the buck, boost, and buck-boost converters.

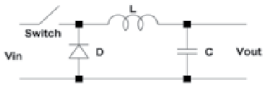
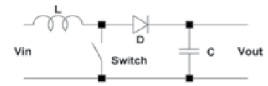
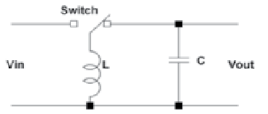
	Topology	Schematic	Power (Watts)	Typical Efficiency	Relative Cost	Magnetics Required	DC Transfer Function (V_{OUT}/V_{IN})	Maximum Practical Duty Cycle	Universal Input (90-264) V_{AC}	Multiple Outputs	$V_{OUT}<V_{IN}$ Range	$V_{OUT}>V_{IN}$ Range
Isolated Topologies	Buck		500	85	1	Single Inductor	D	0.9	No	No	Yes	No
	Boost		150	70	1	Single Inductor	$\frac{1}{1-D}$	0.9	No	No	No	Yes
	Buck-Boost		150	70	1	Single Inductor	$\frac{-D}{1-D}$	0.9	No	No	Yes	Yes

Figure 1: Wurth Electronics SMPS characteristics chart [5].

In the figure above, note the second left-most column. Wurth claims that the typical efficiency for a Buck converter is 85%. One of the founding principles of this course is the assumption of ideal components, implying the input power and output power of any converter topology are equal. An efficiency drop of 15% seemed significant and worthy of further analysis into which of the components could cause such a drop in efficiency.

Types of Nonidealities:

The buck converter requires a quite small number of components: a transistor, diode, inductor, output capacitor, and the intended load. For simplicity, the load is assumed to be a fixed resistance, R, and the input DC voltage is assumed to have zero ripple. Input capacitance could be introduced to minimize input ripple, but it is beyond the scope to shift the efficiency drop to nonidealities involved with the input signal. By assuming a perfect DC input, any drop in efficiency will be contributed to the converter.

It is known that transistors operating in saturation exhibit an on-voltage and a series resistance from collector to emitter or drain to source, depending on the transistor used. The transistor's cutoff behavior will be assumed as an ideal open circuit since any leakage currents are orders of magnitude less than the on-current of the device. Similarly, diodes exhibit a forward voltage and

a series resistance when in the on-state. The leakage current, while the diode is off, will also be ignored for identical reasons as the transistor. The inductor exhibits a series resistance at DC, denoted r_{DC}. Lastly, the capacitor exhibits an equivalent series resistance (ESR) in series with the capacitor. Note that other nonideal parasitics such as inductor interwinding capacitance anddiode reverse-bias capacitance exist, but will not be the focus of this paper albeit interesting to ponder their effects.

To summarize, the following six nonidealities which will be investigated are listed and visualized below:

- Inductor Series Resistance
- Output Capacitor ESR
- Diode Forward Voltage
- Diode On-resistance
- Switch On-voltage
- Switch On-resistance

The figure below presents the final circuit the analysis will build toward.

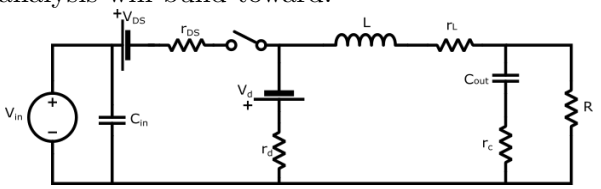


Figure 2: Buck nonidealitites schematic.

The output capacitor ESR can be made negligible if the converter is designed with a low output voltage ripple. The ESR will only contribute to sufficient power loss when the ripple or ESR are large. The major parts distributors have a wealth of several μF capacitors with ESRs on the order of several mΩ.

Reference Buck Design:

Prior to analyzing each of the above nonidealities, a reference design is needed for comparison. Hence, a 10 to 5 V buck converter was designed to supply 5 W with a current ripple of 5%, and a voltage ripple of 1%. A current ripple of 5% is quite aggressive, however, pushing the converter design to an extreme will help determine weak points within the design. The following set of equations were derived in the course and are provided for reference. A switching frequency of 25 kHz was chosen arbitrarily.

$$f_s = 25\text{kHz} \Rightarrow T = 40\mu s$$

$$R = \frac{P_o}{I_o} = 5\ \Omega \tag{1}$$

$$D = \frac{V_o}{V_{in}} = \frac{5}{10} = 0.5 \tag{2}$$

$$L_{crit} = \frac{(1-D)\,RT}{2} = 50\ \mu\text{H} \tag{3}$$

$$\text{Let L } = 100L_{crit} = \ 5\text{mH}$$

$$C_{out} = \frac{(1-D)}{8Lf^2\frac{\Delta V_c}{V_o}} = 2\ \mu\text{F} \tag{4}$$

$$\frac{\Delta V_c}{V_o} = 0.01 \Rightarrow \Delta V_c = 50\ \text{mV} \tag{5}$$

$$\frac{\Delta I_L}{I_o} = 0.05 \Rightarrow \Delta I_L = 50\ \text{mA} \tag{6}$$

The final component values for the ideal buck converter are a 5 mH inductor, 2 μF capacitor, and a 5 Ω load. The switch and diode are assumed ideal, and the theoretical current and voltage ripple should be within 50 mA and mV respectively. The next section will simulate this initial design and verify these specifications.

Ideal Buck Simulation:

LTSpice® was chosen to simulate each of the circuits and designs throughout this report. Many other spice-based simulators exist, but the modeling process is quite intuitive and allowed for

rapid testing of component values. The initial for the buck converter is provided in the figure below.

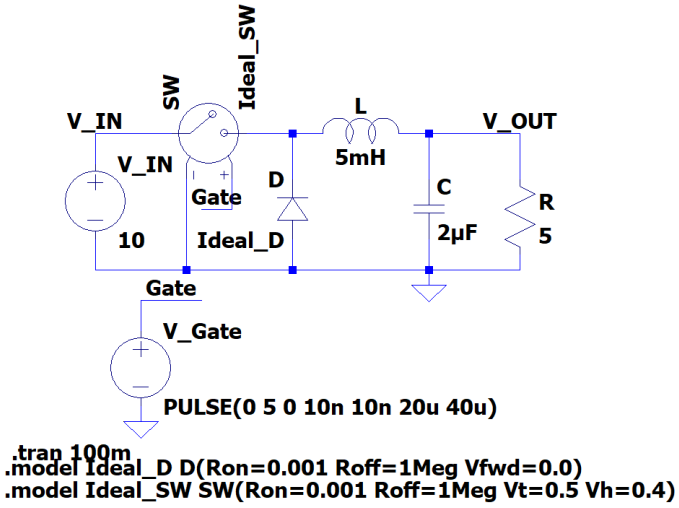


Figure 3: Ideal Buck Converter Schematic in LTSpice.

The two model statements at the bottom of the figure allow the setting of various device parameters. For an ideal diode and switch, an on-resistance of 1 mΩ was set. A smaller resistance could be used, but a 1 mV drop across each device is sufficiently small. The off resistance for both devices was set to 1 MΩ to guarantee open circuit behavior. The diode forward voltage was explicitly set to zero volts. The switch requires additional parameters to define the switching hysteresis. Setting the upper and lower level thresholds to 0.5 and 0.4 V, respectively was sufficient. The square wave toggling the switch was chosen to have a 10 ns rise and fall time with a logic high of 5 V. The incredibly short rise time provides quick switching times.

It is necessary to mention that LTSpice includes a 1 mΩ resistance in series with an inductor unless set otherwise. It is unknown whether or not the ideal capacitor model exhibits a built-in ESR but none of the resultant simulations would indicate so. The load resistor is represented as the theoretical 5 Ω load. The circuit was simulated and the waveforms for the input current, inductor current, and output voltage were captured.

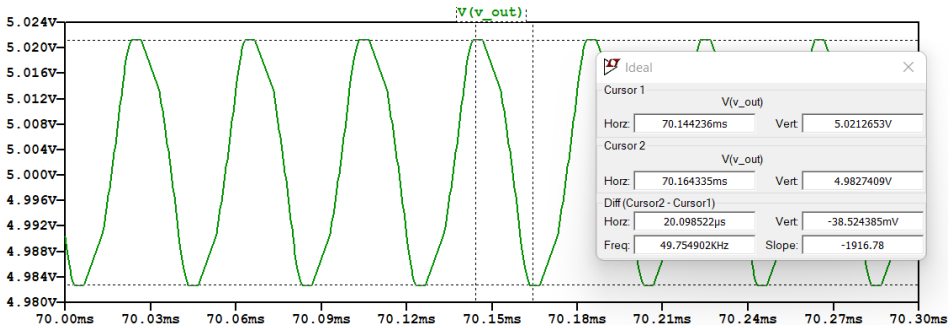


Figure 4: Ideal buck output voltage waveform.

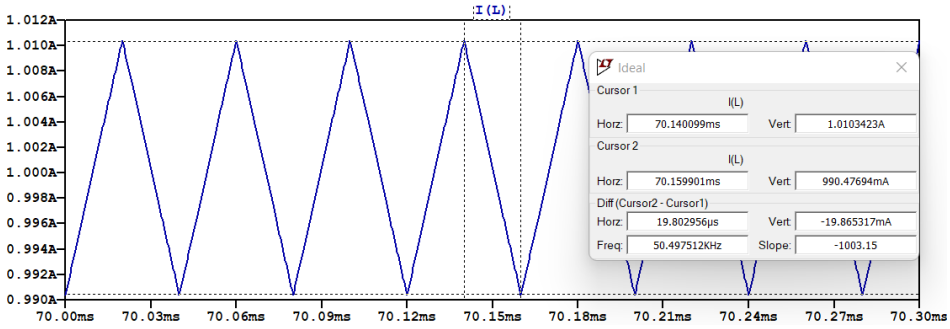


Figure 5: Ideal buck inductor current waveform.

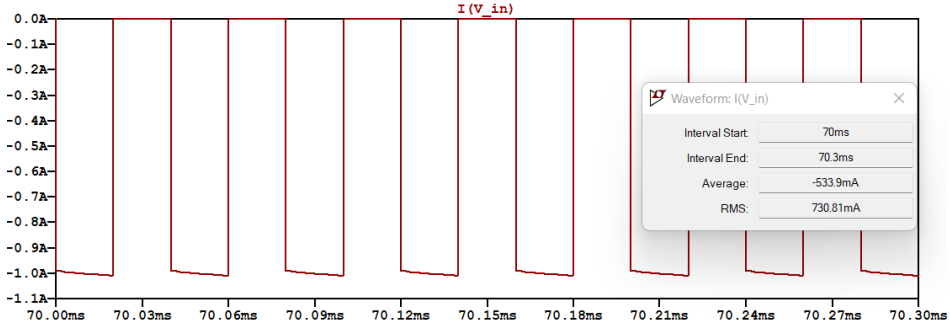


Figure 6: Ideal buck input current waveform

To save space the above figures have been kept relatively small. Two cursors were used to measure the ripple of the waveform, while the measurement values are recorded in the box to the right. The average value of the input current was recorded using the averaging function. By inspection, the output voltage and load current is 5 V and 1 A, respectively. The converter was designed to operate in CCM, which the inductor current waveform confirms. The voltage and current ripple were measured to be approximately 38.5 mV and 19.9 mA, which is well within the 50 mV and 50 mA limit. Choosing an inductor 100 times the critical value results in an inductor ripple well below 5%. It is unsure what component, or setting caused the 11.5 mV drop in the voltage ripple. However, the ripple is within the 1% specification, and the error will be neglected.

Efficiency Calculation

This section will highlight the efficiency derivation from LTSpice measurements. For simplicity, the average input current was not explicitly derived for each of the nonidealities. The average input current, needed to compute the average input power, is easily measured in LTSpice's waveform monitor. From Fig. 6 the average input current is 533.9 mA. The current is negative because LTSpice assumes the current direction is into the voltage source. With the average input current the efficiency may be calculated,

$$P_{o,avg} = \frac{V_o^2}{R} = 5 \text{ W}$$

$$P_{in,avg} = \frac{V_{in}}{I_{in,avg}} = 5.339 \text{ W}$$

$$\eta = \frac{5}{5.339} \cdot 100\% = 92.6\%$$

Under nearly-ideal component parameters, the converter efficiency is not 100%. The sum of average losses across each component contributes to less than 5 mW. The only other source of power loss is due to switching losses. Inspection of the LTSpice waveforms calculated an average

power loss of 1.45 W during only the rise time. Dividing the 1.45 W over the 20 μs period implies 72.5 mW per state switch. Within a period a rise and falling edge occur, implying 145 mW is lost purely in the switch. The same occurs for the diode, contributing another 145 mW each cycle. Therefore, an additional 300 mW is provided by the input to account for the switching losses. The LTSpice averaging was used, implying slight errors may be possible. Regardless, a base efficiency of 92.6% will be used in further comparisons.

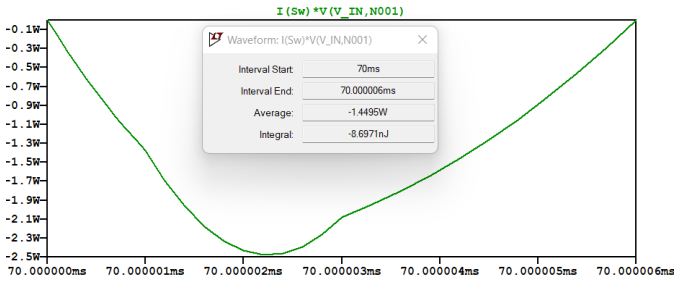


Figure 7: Ideal buck switch loss waveform.

Sample Components:

To adequately compare the ideal converter with practical configurations practical components much be chosen. Two diodes, MOSFETs, and three inductors were chosen to insert into the simulations. The table of components and their various parameters are provided below.

Diode Selection:

Manufacturer	Part Number	V_{block}(V)	Max. Current (A)	$V_{forward}$(V)	r_{on} (mΩ)
Vishay®	1N5400 [1]	50	3	0.75	125
Vishay	1N5822 [2]	40	3	0.4	11.6

Table 1: Silicon and Schottky diode component choice.

The 1N5400 and 1N5822 are standard silicon and Schottky diodes manufactured by Vishay. The two diodes were chosen because they have nearly identical blocking voltage and current capabilities. The primary difference between the two is the forward voltage and resultant on-resistance. The forward voltage of each diode was gathered from the respective datasheet by observing the IV characteristic. The on-resistance was calculated by taking the reciprocal of the IV characteristic's slope near the 1 A operating point. A steep IV curve results in a lower on-resistance. Yes, the diode on-resistance model is typically reserved for small signal analysis. Regardless of the 1 A passing through the diode, the ripple current of $\pm$ 10 mA does constitute a small signal.

The following figure demonstrates the on-resistance calculation. The slope was drawn near the 1 A operating point and calculated based on well-defined points along the IV characteristic. The change in current is approximately 1.06 A and the change in voltage is 0.2 V; dividing the two results in a conductance of 5.3 $\frac{A}{V}$. Taking the reciprocal gives the on-resistance as approximately 125 mΩ.

MOSFET Selection:

The two chosen MOSFETs were chosen based on their on-resistance. Graciously, most MOSFET datasheets provide the on-resistance as a parameter. A large resistance MOSFET from STM was chosen to illustrate a high-loss switch and a low resistance as low-loss, more-ideal component. The drain-source on-voltage was gathered from the respective datasheet.

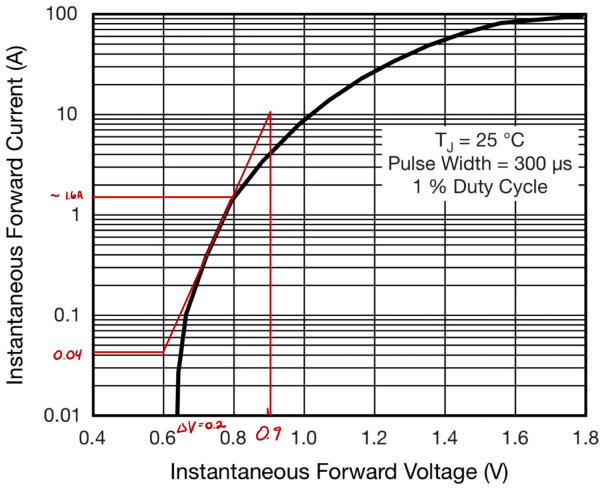


Figure 8: 1N5400 on-resistance calculation [1].

Manufacturer	Part Number	Max. Current (A)	$V_{DS,\ on}$ (V)	$r_{ds,on}$ (Ω)
STM®	STF4N80K5 [9]	3	2.0	2.5
Vishay	IRFD024PBF2 [7]	2.5	0.1	0.1

Table 2: N-channel MOSFET component list.

Inductor Selection:

The last component is the inductor, which proposed a significant challenge. According to the major parts distributors, a 5 mH fixed inductor is not only expensive but uncommon. The three following inductors are on the order of $10 and have varying DC resistances and maximum currents. The second entry of table 3 is unable to be used in the design due to the 39 mA maximum current. However, it is included to show the vast differences between market products.

Manufacturer	Part Number	Inductance (mH)	Max. Current (A)	r_{DC} (Ω)
Bourns®	1130-472k-RC [6]	4.7	1	1.86
Bourns	SDR0503-502JL [10]	5	0.039	60
ITG®	L301308 [8]	4.5	2.5	0.636

Table 3: Inductor component list.

Inductor Nonidealities:

The inductor nonideality analysis is provided in [3]. A brief overview of the analysis will be provided to illustrate the methodology used for the remaining configurations.

Mode 1 - Energizing:

While the switch is on, the inductor is being energized according to the schematic below.

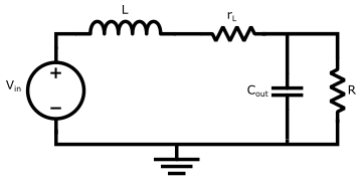


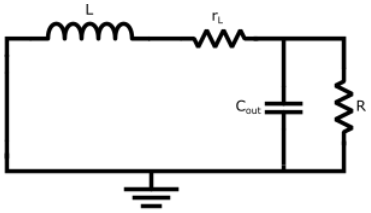
Figure 9: Inductor resistance energizing schematic.

$$
\begin{aligned}
V_{in} &= V_L + I_L r_L + V_o \\
V_L &= V_{in} - I_L r_L - V_o \\
V_L &\approx V_{in} - \frac{V_o}{R} r_L - V_o \\
\Rightarrow V_L &\approx V_{in} - V_o \left(\frac{r_L}{R} + 1 \right) \qquad (7)
\end{aligned}
$$

Eq. 7 has been derived by taking the KVL of Fig. 8 and applying several assumptions. An output voltage ripple of 1% is sufficient in assuming an approximately DC output voltage. Similarly, the low ripply current through the inductor implies the inductor current is approximately equal to the average inductor current. The load current is equivalent to the average inductor current, hence, $I_L = V_o/R$. The inductor voltage while the inductor is de-energized is needed to utilize the volt-second balance.

Mode 2 - Deenergizing:

The de-energizing cycle of the converter is relatively unchanged from the ideal buck. The series resistance results in another drop within the KVL. The same assumptions of minimal current and voltage ripple. The schematic and analysis are provided below.



$$
\begin{aligned}
V_L + I_L r_L + V_o &= 0 \\
V_L &= -V_o - I_L r_L \\
V_L &= -V_o - \frac{Vo}{R} r_L \\
\Rightarrow V_L &\approx -V_o(1 + \frac{r_L}{R}) \qquad (8)
\end{aligned}
$$

Figure 10: Inductor resistance deenergizing schematic.

With the inductor voltage across both modes, they can be equated to derive the voltage gain for the converter.

$$
\begin{aligned}
\left[V_{in} - V_o(\frac{r_L}{R} + 1)\right] DT - \left[V_o(1 + \frac{r_L}{R})\right](1 - D)T &= 0 \\
DV_{in} - \left[V_o(1 + \frac{r_L}{R}\right] &= 0 \\
\Rightarrow V_o &= \frac{DV_{in}}{1 + \frac{r_L}{R}} \qquad (9)
\end{aligned}
$$

Eq. 9 can be verified by substituting an ideal inductor; $r_L = 0$. The denominator becomes unity, implying the gain of the converter equals D. Note that the denominator of Eq. 9 is limited by the load resistance. The $\frac{r_L}{R}$ term may be ignored if the inductor resistance is significantly smaller than load resistance. However, for large current draws at low voltages, such as 5 V at 1 A, an inductor resistance of below 50 mΩ is necessary to minimize the error to below 1%; $\frac{r_L}{5\Omega} = 0.01 \Rightarrow r_L = 0.05\ \Omega$.

Simulation Results:

The waveforms for the inductor case will not be included for space, opting instead to include the waveforms for more complicated configurations. The following table records the various voltages and currents from LTSpice and utilizes them to compute the efficiency. The results of this table will be discussed in the simulation conclusion section.

r_L (Ω)	I_{in} (mA)	V_{out} (V)	P_{in} (W)	P_{out} (W)	η (%)
1.86	379.5	3.656	3.795	2.673	70.4
0.636	461.9	4.437	4.691	3.937	83.9

Table 4: Inductor nonidealities simulation results

Inductor and Diode Nonidealitities:

With the inductor nonidealities analyzed, the diode is the next component to introduce. During the energizing of the inductor, the circuit is identical to mode 1 of the inductor-only section.

Mode 2 - Deenergizing:

The circuit diagram including diode nonidealities and the resulting analysis is provided below.

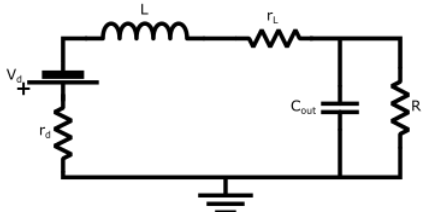


Figure 11: Inductor and diode nonidealities schematic.

$$
\begin{aligned}
V_o + V_L + V_d + I_L(r_L + r_d) &= 0 \\
V_L &= -V_o - V_d - I_L(R_L + r_d) \\
V_L &= -V_o - V_d - \frac{V_o}{R}(R_L + r_d) \\
\Rightarrow V_L &\approx -V_o\left(1 + \frac{r_L + r_d}{R}\right) - V_d \qquad (10)
\end{aligned}
$$

Eq. 10 indicates that the diode on-resistance behaves similar to the inductor resistance. As for the on-voltage, the value directly shifts the inductor voltage by a fixed value. Equating Eq. 7 and 10 via the volt-second balance the gain is derived; the intermediate algebra has been omitted for space.

$$
\begin{aligned}
\left[V_{in} - V_o\left(\frac{r_L}{R} + 1\right)\right] DT + \left[-V_o\left(1 + \frac{r_L + r_d}{R}\right) - V_d\right](1 - D)\,T &= 0 \\
V_o = \frac{V_{in}D - V_d\,(1 - D)}{1 + \frac{1}{R}\,(r_L + r_d(1 - D))} \qquad (11)
\end{aligned}
$$

Simulation Results:

Again, Eq. 11 may be verified equal DV_{in} when zero value for r_L, r_d, and V_d are substituted. Eq. 11 is also confirmed by the simulation results provided in the following table. The low and high resistance inductors were used and both the silicon and Schottky diode was swapped into the circuit.

r_L (Ω)	r_d (Ω)	V_d (V)	V_{out} (V)	I_{in} (mA)	η (%)
0.636	0.1250	0.75	4.058	406.4	81.0
0.636	0.0116	0.4	4.254	426.0	85.0
1.860	0.1250	0.75	3.341	334.6	66.7
1.860	0.0116	0.4	3.496	350.1	69.8

Table 5: Simulation results including diode and inductor nonidealities.

Inductor, Diode, and Switch Nonidealities:

Integrating the last of the nonidealities, the switch will affect the energizing cycle of the converter. Hence, analysis is only necessary for mode 1. The switch is replaced with a voltage source, denoted V_{DS} and a series resistance r_{DS}. As with prior sections, KVL paired with the volt-second balance will be used.

Mode 1 - Energizing:

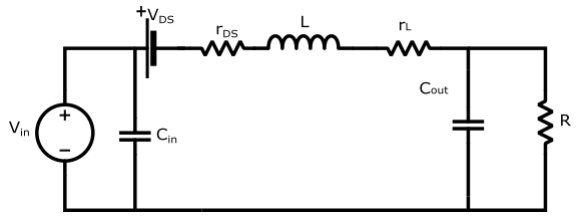


Figure 12: Inductor and diode nonidealities schematic.

$$
\begin{aligned}
V_{in} &= V_{DS} + V_o + V_L + I_L(r_L + r_{DS}) \\
V_L &= V_{in} - V_{DS} - V_o - I_L(r_L + r_{DS}) \\
V_L &= V_{in} - V_{DS} - V_o - \frac{V_o}{R}(r_L + r_{DS}) \\
\Rightarrow V_L &\approx V_{in} - V_{DS} - V_o(1 + \frac{r_L + r_{DS}}{R}) \quad (12)
\end{aligned}
$$

Using the volt-second balance with Eq. 10 and 12,

$$
\left[V_{in} - V_{DS} - V_o(1 + \frac{r_L + r_{DS}}{R})\right] DT + \left[-V_{DS} - V_o(1 + \frac{r_L + r_{DS}}{R})\right] (1 - D)T = 0
$$

$$
\Rightarrow V_o = \frac{V_{in}D - V_{DS}D - V_d(1 - D)}{\left[1 + \frac{1}{R}(r_L + r_d(1 - D) + r_{DS}D)\right]} \quad (13)
$$

Eq. 13 reinforces how extensive the analysis of nonidealities can become. Luckily, there is a structure that can intuitively describe the output voltage. The switch is on while for a duration DT, implying the V_{DS} term should be scaled by D. Similarly, the diode is on for the $(1 - D)T$ duration, implying a scaling of $(1 - D)T$. As for the denominator, each of the resistances is scaled by their relevant duty. r_{DS} is included over DT and r_d is included over $(1 - D)T$. Interestingly, the denominator is dependent on each component's resistance. Any attempt to optimize one component over another may prove helpful, but maximizing the output voltage requires a joint effort in minimizing the parasitics of each component.

Simulation Results:

To reduce the number of configurations simulated, the best and worst-case of the converter will be simulated. Best-case implies the Schottky diode, low on-resistance MOSFET, and the low-resistance inductor. Inversely, the worst-case converter will use the silicon power diode, high on-resistance MOSFET, and the high-resistance inductor. The waveforms for the worst-case are provided below.

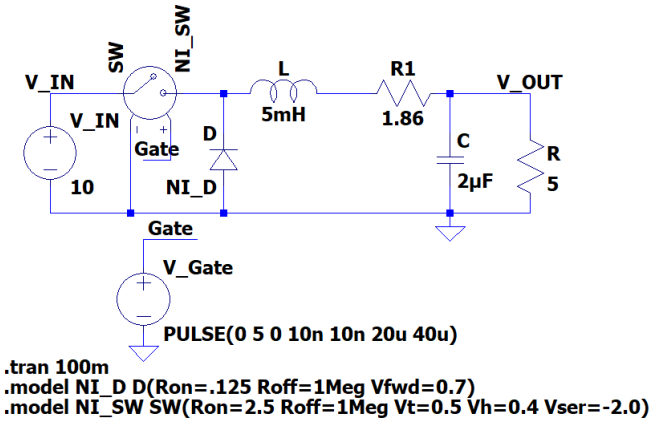


Figure 13: L, D, and SW nonideal converter Spice schematic.

Note that the sign of the series resistance in the switch model is negative. By default, the series resistance is in the direction of the positive to the negative terminal of the switch, opposite of the intended direction for the converter.

Compiling the data from the two simulations, the results are provided in the table below.

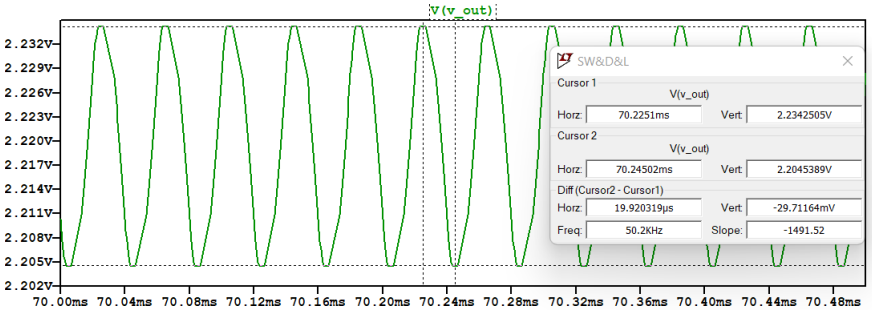


Figure 14: Nonideal buck output voltage waveform.

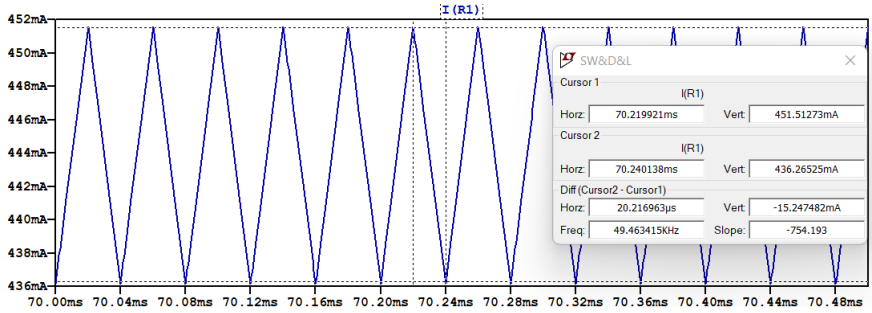


Figure 15: Nonideal buck inductor current waveform.

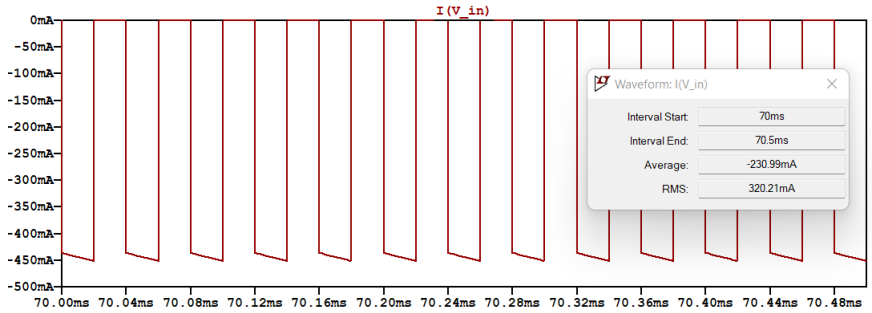


Figure 16: Nonideal buck input current waveform.

r_L Ω	V_{DS} (V)	r_{DS} (Ω)	V_d (V)	r_d (mΩ)	V_{out} (V)	I_{in} (mA)	P_{in} (W)	P_{out} (W)	η %
0.636	0.1	0.1	0.4	11.6	4.176	434.6	4.346	3.488	80.3
1.86	2.0	2.5	0.75	125	2.219	231.0	2.310	0.9849	42.6

Table 6: Nonideal buck converter range of efficiencies simulation results.

Simulation Conclusion:

Throughout circuit design, it can be easy to think of a design as a purely simulated and mathematical process. That each component is ideal, or that any nonidealities are negligible and can be negligible toward the design, yet this is drastically incorrect. The values from table 6 reiterate why Wurth claimed the typical efficiency of a buck converter to be 85%. None of the parts chosen have any property that would make them undesirable to a designer, just that their properties are not sufficient for the required specifications.

Ranking the affect of each nonideality on performance would be inductor, diode, then switch. The second set of simulations showed that for long-duty converters, the diode forward will significantly drop the output voltage. The effect is not negligible but being forced to use a significant series resistance inductor will always contribute to a drop in output voltage. Within each of the output voltage equations, Eq. 9, 11, and 13, the inductor resistance is present.

Assuming purely ideal switches and diodes does not address that the load current will form a drop across the series resistance. The switch is surprisingly the least lossy component; from an averaging perspective. Another report could be drafted based on the switching losses alone.

The substantial losses have been caused by the inductor and the arbitrary design rule to scale the critical inductance by 100. This converter does not have a specified application. However, choosing the current ripple specification to be 5% is a significant factor. Say a 10x inductor, 500 mH, was chosen. Some of the specifications from the major parts distributors included DC resistances on the order of 100-300 mΩ with current maximums well over 1 A. Switching the inductor to a 500 μF inductor will increase the simulated ripple by 10x, implying the inductor will experience 100 mA peaks. Ultimately the tradeoff is the ripple through the inductor.

An alternate redesign is to increase the duty, however, each of the on-voltages become more prevalent. For the best-case converter the duty would need to be increased to 0.592 to increase the output voltage to 5 V. However, the efficiency would either remain unchanged or increase slightly. A large issue with this approach is that it does not work for the worst-case converter. The duty would theoretically need to be increased to 1.317 to output 5 V. Increase the duty beyond 1 is not only impractical, it still does not address the efficiency. Hence, the only viable solution which keeps the device in CCM is to pick as low parasitic components as possible and adjust the duty to account for the dropped voltage. The focus of which should be on the inductor's DC resistance.

Synchronous Buck Topology:

Ironically, the report so far has provided motivation toward an alternate topology which was thought to improve efficiency. It was initially thought that the most significant nonideality would be the diode's on-voltage. The above simulation and analysis indicate otherwise, but the diode becomes prevalent in a design where the inductor has been appropriately chosen. The synchronous buck converter simply replaces the diode with a switch.

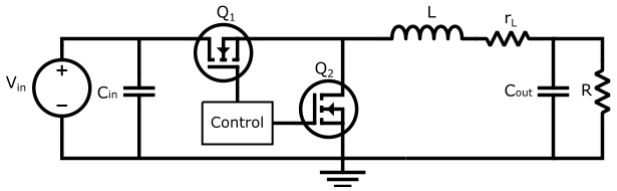


Figure 17: Synchronous buck converter topology.

The benefit of simulating the synchronous converter in LTSpice is that the sources driving each switch can be easily synchronized. Implementing the circuit practically presents its own challenges, but they are beyond the scope of this report.

Reference Simulation:

To highlight the behavior of the synchronous converter the best-case scenario from above was simulated. The best-case converter was chosen to examine how the efficiency varied. A 50% duty cycle, 0.636 Ω inductor, on-voltage of 0.1 V, and on-resistance of 100 mΩ was used for the simulation. The schematic is provided below.

For the sake of space, only the waveform for the input current will be included. The table below lists the performance characteristics of the converter. The input current is the only waveform that was significantly affected.

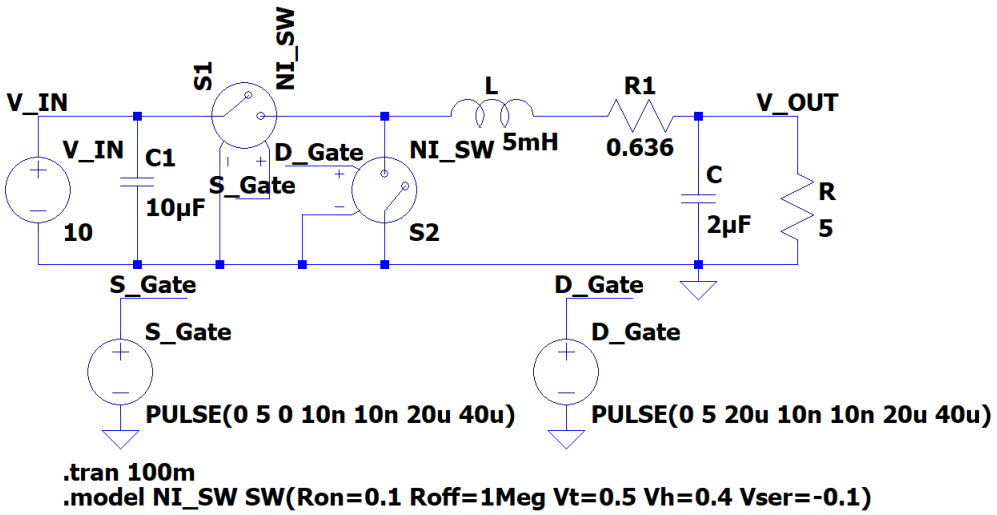


Figure 18: Synchronous buck converter schematic in LTSpice.

V_{out} (V)	ΔV_o (mV)	I_L (mA)	ΔI_L (mA)	$I_{in,avg}$ (mA)	$I_{in,max}$ (A)	η (%)
4.271	38.6	854.1	19.4	480.9	50	75.8

Table 7: Synchronous buck converter best-case performance characteristics.

Note the performance of the converter in Table 7. At first, the converter seems to behave almost identical to the asynchronous topology. The output voltage varies by approximately 0.1 V, the efficiency has dropped by 5%, but somehow a 50 A current spike is present. The two following waveforms investigate the input current and some properties of the spike.

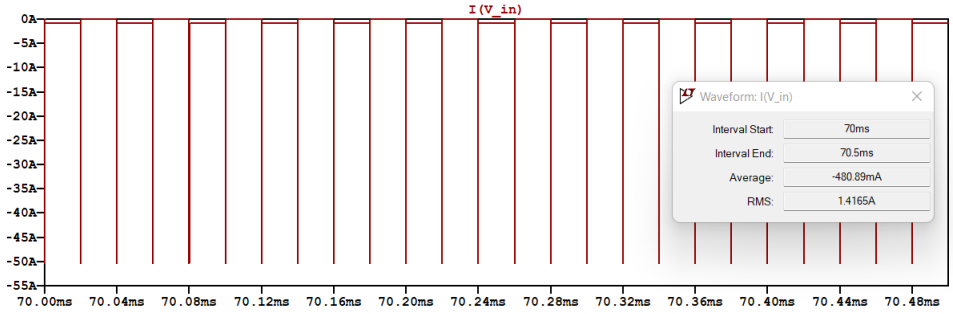
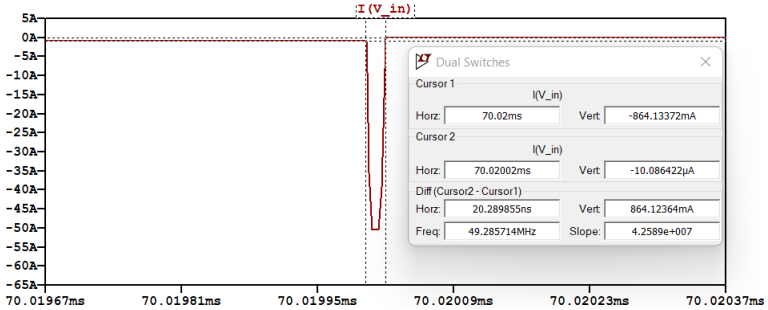


Figure 19: Synchronous buck input current waveform.



The width of the spike hints at the origin, the switching transient. The simulation above utilizes ideal switches, whereas a practical converter would likely use power MOSFETs. An unintentional advantage of the power MOSFET is the internal body diode connecting the substrate to the drain. Implying that the switch, S2, has a parasitic diode in the same orientation as the asynchronous buck converter. Not only does the body diode suppress the switching transient

it also keeps the ground-referenced voltage at the switch node clamped. The switch node is defined as the node where switching is present, or the node connecting to the positive terminals of S1 and S2. Keeping the switch node voltage is preferable and sometimes required for many common SMPS power supply controllers on the market, but the benefits exceed the scope of the report.

Disadvantages of Synchronous Buck:

The synchronous buck converter is a good first step at minimizing the losses of the humble buck converter. However, increased efficiency must come with a tradeoff. Replacing the diode with a switch immediately opens several control-related issues. Questions such as when is the optimal time to toggle each switch? What stresses will be placed on each switch? Which switch will fail first? Other observations that the second switch does not ultimately resolve the shortcomings of the inductor. While true, it is hoped someone designing a converter would not be a constraint to an inductor introducing such losses. The emphasis on the 5 mH inductor was to push a design to the extremes. Lastly, the ability to briefly short the input source is possible. It would be interesting to devise device a simulation to include the body diodes, but sadly the time has not allowed for it.

Conclusion:

The once simple buck converter has proved to be much more complex than initially thought. This paper has looked at practical considerations when designing and constructing a buck converter. Nonidealities such as on-voltages and parasitic resistance composed the bulk of the report. However, the addition of seemingly simple nonidealities proves how difficult design can be. Luckily, the volt-second balance provided a method to derive closed form expressions for the output voltage in terms of each nonideality. From these closed forms, a mass of simulations and comparisons of various components, their values, and their effect on efficiency were made. The last section of the report introduced one potential solution, the synchronous converter. Surprisingly, the synchronous converter did not boost the efficiency as expected. Instead, the converter showed a new wealth of issues to design against. However, a well-designed synchronous converter addresses some of the losses within the asynchronous buck. The key takeaway from this report is that no component is truly ideal and a tradeoff is always being made when a component is chosen.

List of Figures

List of Tables

References

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