Topic 2: The Silicon Lattice, Properties, and Doping.

Preface:

This section of notes will involve us studying the crystalline structure of silicon. This analysis will reveal why silicon behaves as a semiconductor and provide techniques in how we can influence the conductivity of the material. Due to the chemistry review, this section is quite lengthy. If you feel comfortable with solid-state materials, I recommend skipping to the Doping section. I have also included additional information and simulations to hopefully provide a new perspective, or interest to the topic.

Periodic Table Review:

Before we delve into why silicon has become a standard material for semiconductors, we need to review the periodic table. Encoded in the columns of the table is the **group number**. Some periodic tables will include a number above the column or a Roman numeral. There are currently 18 columns in the table and silicon falls into column 14. We also use the terminology that silicon is a group 4 element. This terminology excludes the transition metals. Therefore, Boron, Silicon, and Phosphorous correspond to groups 3, 4, and 5, respectively. This group number tells us the number of electrons in an element's valence shell. Recall that the valence shell is the outermost shell of the atom and that these electrons allow elements to bond with other elements or compounds.

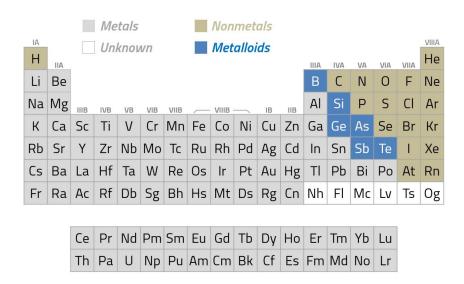


Figure 1: Periodic Table separated by conductivity. (Draeger, N., PhD., 2019)

The figure below should be familiar, it is the Lewis dot structure for a silicon atom and each dot corresponds to a valence electron. The valence electrons are in separate positions because orbitals are filled sequentially, this goes more formally as the Pauli Exclusion principle for orbitals. To reiterate, silicon's valence shell is of the form $3s^2 3p^2$. If you are feeling worried, please do not be. This review is to provide a thorough background into why silicon has several

favorable properties. This information is not critical to the examinations, beyond how many valence electrons are in a certain group.



Figure 2: The Lewis dot structure of silicon.(Ball, D. PhD., 2012)

We tend to use this Figure 2 instead of Figure 3 because we do not need to concern ourselves with the inner orbitals of the atom. The positively charged nucleus exerts a Coulombic force on the surrounding electrons. Since the inner shells are not just attracted to the nucleus, but also repelled by surrounding electrons they have less must energy than the valence shell. Hence, our focus will be on the high-energy valence electrons and how they interact with surrounding atoms.

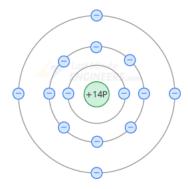


Figure 3: The Bohr-Rutherford Model of the Silicon Atom. (Unknown, 2021)

The Silicon Lattice:

A question we may ask ourselves is, "How do these silicon atoms bond with one another?" Assuming we have a compound of pure silicon, with no impurities, the silicon atoms would form a grid-like structure. A valence electron from one orbital would pair with an electron from another atom.

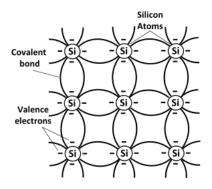


Figure 4: Lewis structure of pure silicon. (Wikipedia Contributors, 2021)

I particularly like and dislike the figure above. It is great in that it shows the covalent bond as more than an abstract line. The electrons are present in the valence shell and have a negative charge. It also shows that electrons are free to leave the influence of the host atom if there is enough energy to break the bond. I dislike the image because it does not present any information beyond 2-dimensions.

Transitioning from two to 3-Dimensions is no trivial task. We must first address how a silicon atom with a full valence shell occupies 3D Space. I am not aware of if this topic is discussed in Introductory Chemistry courses, however, it is necessary to understand the lattice. Note that these covalent bonds are just pairs of electrons, implying there is a non-zero charge associated with the bond. Therefore, these bonds will repel each other into a stable, more optimal shape, the tetrahedron. We will not delve into the specific of why the tetrahedron is the optimal shape.

The link below is to a Sketchfab model of a tetrahedron. If you were to measure the angle between bonds, it would be 120°. We will not delve into why it is 120° but it has to do partially with the fact that silicon can bond with four other atoms. I encourage you to play with the simulation and convince yourself that the bonds must repel themselves into this shape.

Tetrahedron (Rodriguez, E., 2019): https://sketchfab.com/3d-models/tetrahedral-27d804e87b6d431ea15e240ce9874e36

Now we know what silicon should do, we need to define a way to combine this shape into more complex shapes. The term **Unit Cell** is commonly used to define the smallest unit, or configuration, of atoms composing the crystal. If we were to combine these unit cells into the shape of a cube, it would imitate the lattice of the element under discussion. The simplest unit cell is called the **simple cube**, which consists of 8 atoms placed in the vertices of a cube. The edges of the cube represent the covalent bonds between atoms. An example of how we use unit cells to create a lattice and the simple cube structure is provided in the figure below.

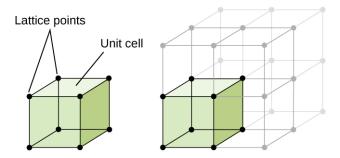


Figure 5: Unit Cell stacking into a crystal lattice.(Flowers P., 2020)

Some standard unit cells are the simple, body-centered, and face-centered configurations. The body-centered cubic takes the simple cell and inserts an atom at the center of the cell, or body, of the cube. Similarly, face-centered takes the simple cell and inserts an atom at the center of each face. Note that nature is not randomly choosing where the atoms lie within the unit cell. It is due to the intermolecular forces within the lattice that the atoms are stable in these configurations. The following link directs you to a Sketchfab collection of common unit cell visualizations (YorkPhysics3D, 2018).https://sketchfab.com/YorkPhysics3D/collections/solid-state

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Below are some of the common unit cells displayed in 2-Dimensions.

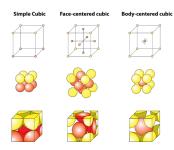


Figure 6: The simple, body-centered, and face-centered cubic unit cells.(Auyeung, kown)

Provided below is the link to another Sketchfab model. This model represents the bonding of several tetrahedra into a hybrid face-centered unit cell. The unit cell for silicon is a combination of two face-centered cells. Within the model also includes several planes that are formed within the lattice. For our purposes, these planes do not matter but are interesting to see.

Silicon Lattice (Lee, L., 2015):

https://sketchfab.com/3d-models/silicon-crystal-lattice-73e292f32ffe4ca490e166 faeba317e7

Hopefully, the idea that silicon is a semiconductor is more apparent. With all the atoms being perfectly bonded together, there is ideally zero free charge to form a current. If there was some way to temporarily break a bond, it would result in an electron traveling throughout the lattice. The last thing we need to discuss is how an electron travels throughout the lattice. Imagine inserting an electron at some random point in the Silicon Lattice interactive model, what would happen? The bonds themselves are electrons, so the free electron would be repelled. This process would happen indefinitely until an atom with an empty valence shell is found. However, the large density of atoms in a region of space would cause the electron to stay effectively in the same region.

Why? I know this is a qualitative description, but I hope you will see some analogies to gas mechanics from modern Physics. We know that a piece of silicon has no net current through it. If there were to be a current, there there is a net motion of electrons throughout the material. However, one way to explain a lack of current is that the distribution of all electrons within the material are moving in a way that their net-motion is canceled out. We can argue this behavior because of the scale of atoms in as little as a gram of silicon. Recall Avogadro's number, 6.022×10^{22} , is the number of atoms in one mole of an element; 1 mole of Si corresponds to 28 grams. Therefore, if we somehow guarantee 1 in every 1 billion atoms contributing a free electron there is on the order of 10^{13} electrons moving within the lattice. We will justify this quantitatively later, but from a theoretical perspective it is possible. We call this phenomenon Brownian motion; named after the botanist Robert Brown. Provided below is an interactive simulator from Boston University demonstrating Brownian motion. The key parameter is, as we discussed earlier, temperature.

Brownian Motion Simulation:

https://physics.bu.edu/~duffy/HTML5/brownian_motion.html

We now might shift our focus into mechanisms to free these valence electrons. However, what would happen if we could somehow cut a covalent bond in two? Well in the same way that electrons pair into bonds, breaking them causes a hole where one electron used to be, and the other electron flies off into the lattice. This is where we get the terminology of electrons

and holes as charge carriers. **Note that a Hole is not a true particle.** in the sense that an electron is. The hole is viewed as the anti-particle of the electron, or the absence of an electron. Hence, the hole has a positive charge q, equal to coulombs constant; the only difference is holes are positively charged and electrons are negatively charged.

The figure below is from the Streetman and Banerjee text, showing an interpretation of holes and free electron within the lattice.

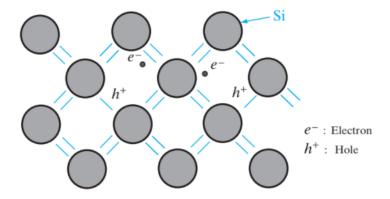


Figure 7: Covalent bonds represented as a hole and free electron. (Streetman, B. G., & Banerjee, S. K., 2015)

If we could imagine a situation where a large number of free electrons, or holes, are within the lattice, then an electric field across the device would induce a non-zero current. Placing an electric field across the device is equivalent to placing a voltage across the ends of the device. Before we can address the manipulation of these charge carriers, we need to discover some way to free them from the lattice. It turns out that at room temperature, there are very few carriers in this free state. The silicon lattice, similar to diamond, is very stable. The thermal energy provided at room temperature is not enough to break a substantial number of covalent bonds.

We will discuss how charge carriers form various currents throughout the device in later sections. As for now, the only concern is that electrons and holes may combine to "recreate the covalent bond." If a hole is the absence of an electron, it is seems reasonable to imply that an electron and hole combine to form a covalent bond. However, if an electron now occupies the position where the hole was, it must mean that the hole has transfered to a nearby atom. Therefore, we can have current due to both holes and electrons within semiconductors.

Increasing Charge Carriers:

I mentioned earlier that if one in every 10 billion atoms produces an electron, we would have on the order of 10^{13} free electrons. This number is not that many orders of magnitude from the actual value. We call the number of free electrons at room temperature the **intrinsic carrier concentration**, which is equal to approximately $10^{10} e^- \text{ cm}^{-3}$. This may seem like a lot but the charge of an electron is on the order of 10^{-19} C, therefore, the current produced at room temperature is on the order of nanoamps.

We have established that temperature is one of the key factors affecting conductivity. However, it would take temperatures much greater than what we could survive in. I do not know the exact temperature, but we are on the order of several hundreds of degrees Celsius. The solution, and a quite clever one, is to dope the semiconductor.

Doping:

Doping aims at introducing controlled quantities of impurities into a semiconductor. These impurities should be elements that either donate an electron or accept a hole into the lattice. Depending on the dopant used, we can form N-type semiconductors by inserting free electrons into the lattice. Likewise, we can form P-type semiconductors by introducing an element that effectively "removes an electron." We commonly use the terms **Donor Concentration** and **Acceptor Concentration** when referring to the amount of dopant introducing electrons, and holes, respectively.

Recall that Silicon is a group 4 element. Some elements nearby Silicon are Boron and Phosphorous, belonging to groups 3 and 5, respectively. These two compounds form the basis for P and N-type dopants. With Boron having 3 valence electrons, if we were to inject Boron atoms into the lattice it would force a hole into the lattice. The hole is forced because Boron can only form three covalent bonds with its three valence electrons. Similarly, if we dope with phosphorous then four covalent bonds could be made with a Silicon atom. The fifth valence electron is left trapped within the lattice. There are many images on the internet showing this phenomenon, so I have created a simulation to provide a different perspective.

The link below leads to a Geogebra interactive animation. Geogebra is a graphing calculator suite, similar to Desmos. There are two sliders that control the amount of N and P-type dopants. Electrons are represented as blue dots and holes are hollow red dots. There is a third slider dedicated to the voltage across the device. Making the voltage negative will swap the polarity across the device. Note that each Si-Si, Si-P, and Si-B bond are a double bond.

Doping Simulation:

https://www.geogebra.org/m/fyjfe37d

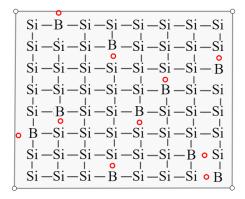


Figure 8: P-Type Silicon Lattice.

Some of you might notice that the holes and electrons in the simulation do not move under the influence of the electric field. The number of components in the simulation has made the animation quite slow. I will provide a more thorough simulation when we start our discussion on semiconductor currents. As of now, we note that the electric field will exert a force on the free charges. Holes will move in the direction of the field and electrons opposite the field. Since we define conventional current as the flow of positive charge, the motion of electrons in the opposite direction results in an electron current opposite of the electron monition. To emphasize, electron motion and current due to electrons are in the opposite direction. Therefore, both electron and hole currents are aligned in the same direction.

Below is a figure from the simulation showing both the current direction and velocity for

0	——с
Si -Si -P -Si -Si -Si -Si	−Si
$\operatorname{Si} - \operatorname{P} - \operatorname{Si} - \operatorname{Si} - \operatorname{P} - \operatorname{P}$	−Si
Si-Si-Si-Si-Si-Si	-Si
P-Si-Si-Si-Si-Si	-Si
Si-Si-Si-Si-Si-P	-Si
Si-Si-Si-Si-Si-Si	−s¦i
Si-P-Si-Si-Si-P-Si	−s¦i
Si - Si - Si - Si - Si - Si - Si	−Si

Figure 9: N-Type Silicon Lattice.

both holes and electrons.

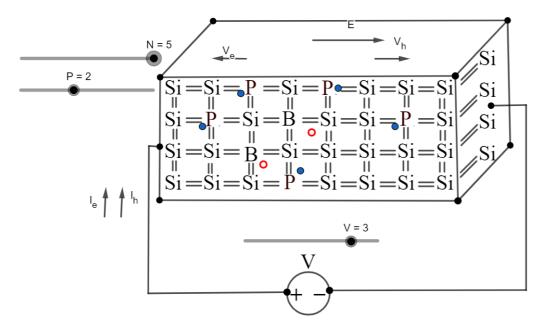


Figure 10: Semiconductor charge excitation by an external voltage.

Doping Mechanisms:

We have two primary mechanisms of doping semiconductors: 1. Diffusion, and 2. Ion Implantation.

1. Diffusion:

By definition **Diffusion is the act of a substance spreading out from a higher concentration to a lower concentration.** Imagine a bowl of water. A singular drop of ink is dropped into the center of the bowl. As the ink contacts the water, it spreads radially across the surface of the water. At the point where the ink contacted the water, the concentration of ink is the highest and points toward the edge of the bowl have a low concentration. Therefore, the act of ink spreading out is the ink diffusing across the water. Here is a link from (3M, 2020) demonstrating diffusion by dropping food coloring into water. https://www.3m.com/3M/en_U S/gives-us/education/science-at-home/diffusion-science-experiment-for-kids/

It is necessary to mention that ink, or food coloring, in water diffuses similar to dopant in a semiconductor. In this experiment, the effect of gravity on the food coloring causes the coloring to move not just to an area of lower concentration, but also downward. For our purposes, this level of depth into the mechanics is not necessary.

As for semiconductor devices, dopants are usually referred to as spin-on. A layer of the dopant is placed on top of a semiconductor. The material is then rotated to a high speed, creating an even layer of the top surface of the material. Ideally, the dopant will penetrate the silicon lattice over time. However, we know that silicon is extremely stable at room temperature. Therefore, we need to heat the silicon to a high temperature, approximately 1200 to 1300 °C; the melting point of silicon is approximately 1400 °C.

2. Ion Implantation:

Cathode-Ray-Tube (CRT) monitors used to take advantage of charge by aiming and shooting a beam of electrons at the screen. The electron beam could be controlled by applying a voltage across sets of plates which the beam traveled across. The voltage across these plates would create an electric field within the region which deflected the electron, causing it to curve effectively aiming the beam at a certain position of the screen.

I do not bring up this old technology to bore you, but to remind us that it is still prevalent today. Instead of electrons imagine if we applied this process to ions. Recall that an **ion is an atom or molecule with a non-zero net charge.** In theory, the principle works because of the non-zero net charge on the particle. The primary difference would be the mass of an electron is different from that of the dopant ion. If we could convert a dopant element into a steady stream of ion, then we could accelerate and shoot the ion into the semiconductor. This process forms the basis of ion implantation. The practical implementation is beyond the scope of this course, but it is a clever harmony of optics, magnetic, and electric fields accelerating and deflection ions. Hence, we have both a broad and accurate technique for doping silicon.

Gauging the pros and cons of each technique, doping allows us to dope a large surface area quite easily. Whereas ion implantation allows us to dope with incredible accuracy at the cost of heating the device several hundreds of kelvin. However, the practical cost of ion implementation is incredibly expensive compared to buying a bottle of dopant and a furnace.

Brief History:

This section is a short summary of semiconductor advances in the last decade. Many honorable mentions are excluded from this list, focusing on both major advancements and moments in your lifetime.

- 1947 Bipolar Junction Transistor invented at Bell Labs by John Bardeen, Walter Brattain, and William Schockley.
- 1949 The P-N Junction is invented at Bell Labs by Russel Ohl.
- 1954 The Solar Cell is invented at Bell Labs by Daryl Chapin, Calvin Fuller, and Gerald Pearson .
- 1960 The MOSFET is invented at Bell Labs by Mohamed Atalla and Dawon Kahng.
- 1963 Complimentary-MOSFET (CMOS) is invented at Fairchild Semiconductor by Chih-Tang Sah and Frank Wanlass.

- 1967 Non-volatile Solid-State Memory at Bell Labs by invented by Simon Sze.
- 1991 Intel's 4004 processor was released.
- 1998 The FinFET is invented Chenming Hu at the University of California, Berkeley.
- 2004 5 nanometer process achieved at Nippon Electric Company.

If this list hasn't made it clear, Bell Labs was at the forefront of Semiconductor innovations. I also hope at least one of these names is familiar, Simon Sze is the author of one of this course's texts. As for some more recent innovations below is a list of Intel's recent generation of processors and how they have advanced over time.

- 2nd Gen. Sandy Bridge 32 nm.
- 3rd Gen. Ivy Bridge 22 nm
- 4th Gen. Haswell 22 nm
- 5th Gen. Broadwell 14 nm
- 6th Gen. Sky Lake 14 nm
- 7th Gen. Kaby Lake 14 nm
- 8th Gen. Coffee Lake 14 nm

From this list, it seems that processor manufacturers had a tough time passing the 14 nm gap. During this period, we saw an increase in the number of cores as a means to bypass decreasing the transistor process. While reaching a sub-nanometer process would be an incredible advancement, it may not be possible. The smaller the transistor becomes, quantum mechanical effects become more apparent and the devices tend to become unreliable; see quantum tunneling for more information. There is also the issue called the power wall. Cramming so many transistors into a tiny space increases the power density of the device. Modern heat sinks are unable to extract heat from the chip efficiently enough.

Perhaps new advancements will come out which will allow us to deal with the power wall and quantum tunneling. However, as of now, it seems that 5 nm is going to stick around for a while.

Semiconductor Properties:

Now that we have discussed the physical structure of silicon, and how to generate a substantial current, we need to address some terminology. We have talked about the ability of a semiconductor to conduct. This quantity is called **Conductivity**, is denoted by a lower case sigma and has units of Siemens per centimeter; $[\sigma] = \frac{S}{cm}$. Recall that a Siemen is the inverse of resistance; $[S] = \frac{1}{\Omega}$. We use centimeters as our unit length because the size of semiconductor devices are very small. Hence, using meters would require unnecessary precision to our calculations. We know from physics and circuit theory that resistivity and conductivity are inverse quantities. If a resistor exhibits a high resistance, you can phrase it equivalently that the resistor's conductivity is low. Alternative, we are interested in the material's **resistivity**, denoted by rho $([\rho] = \Omega * cm)$, which describes how resistant a material is to a current. The inverse relationship of these two quantities is expressed mathematically by $\sigma = \frac{1}{\rho}$.

Please note that resistivity and conductivity are different from Resistance and Admittance. Resistivity and conductivity are parameters of the material, whereas the total resistance and admittance are ultimately dependent on the shape of the material. A common formula in Electromagnetism is that the resistance of a material is, $R = \frac{\rho L}{A}$, where L and A represent the length and cross-sectional area of the material, respectively. Unit Analysis confirms that this quantity has identical units of resistance; Ω cm² $\frac{1}{cm^2} = \Omega$.

These definitions are nice and all, but we have no scale for a high, or low, resistivity or conductivity. Provided below is a figure displaying the spectrum of conductivity and resistivity for common materials. I particularly like this figure because it gives values for both conductors and insulators. The horizontal is on a log axis, so each tick corresponds to increasing the value by powers of $10^{\pm 2}$.

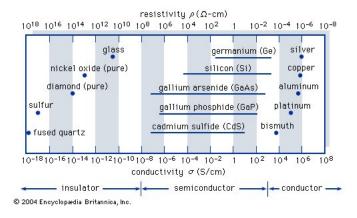


Figure 11: Conduivity and resistivity spectrum (Brittanica, kown)

From this figure we can quantify a material as being a semiconductor if it's resistivity lies in the range of 10^{-3} to 10^{9} . Note that many of the semiconductor materials have a range of resistivity due to doping. If we increase the carrier density of a device by doping it, the resistivity must drop because we are introducing more carriers into the lattice. The inverse argument regarding conductivity is equivalent, if you prefer to think about conductivity instead of resistivity.

Conclusion

This marks the end of this set of notes. We have looked at the lattice of silicon, examined several of its properties, and have set the stage for carrier transport throughout the material. The next set of notes will introduce Energy Band diagrams and quantifying how a doped semiconductor behaves under thermal equilibrium.

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