Topic 12: PN Junction Analysis 2

Preface:

This set of notes continues the PN junction analysis from the last set of notes. We will begin by deriving equations for the linearly graded PN junction and introduce the concept of junction capacitance.

Linearly Graded Junction:

The linearly graded junction setup is similar to the abrupt junction. The doping profile varies linearly across the junction as opposed to an immediate jump from p to n-type. The junction still lies at $x = 0$, and we will denote the boundaries of the space charge region as $x = -x_p$ and $x = x_n$ as well. The doping profile is linear, implying $\rho = qax$, where a is referred to as the gradient of charge density and represents the slope of the doping curve. The q term is needed to convert the doping density to the charge density.

Unlike the abrupt junction, we do not need to rely on $p - n + N_D - N_A$ for the charge density. This equation was needed because we do not have a convenient way to express the discontinuity at the junction. However, the linearly graded junction is easily described by the function $\rho = qax$. The depletion assumption removes n and p from the charge density, leaving a function of only N_A and N_D. Therefore, we can directly apply the doping profile to Poisson's equation or Gauss' law. However, we can make some initial assumptions from our abrupt junction analysis to simplify our lives. Charge conversation implies the area under the n and p-type depletions must be equal. If the doping profile is linear then $x_p = x_n = \frac{w}{2}$. Therefore, it will be easier to frame the integration from $\pm\frac{w}{2}$ to take advantage of symmetry by placing the junction at the origin.

$$\begin{aligned}
\frac{d\mathscr{E}}{dx} &= \frac{\rho}{\epsilon} \\
d\mathscr{E} &= \frac{qa}{\epsilon} x dx \\
\int_{\mathscr{E}\left(-\frac{w}{2}\right)}^{\mathscr{E}(x)} d\mathscr{E} &= \int_{-\frac{w}{2}}^{x} \frac{qa}{\epsilon} x dx \\
\mathscr{E}(x) - \mathscr{E}\left(\frac{w}{2}\right) &= \frac{qa}{2\epsilon} x^2 \Big|_{-\frac{w}{2}}^{x} \\
\mathscr{E}(x) &= \frac{qa}{2\epsilon}\left(x^2 - \frac{w^2}{4}\right), \text{ for } |x| \leq \frac{w}{2}
\end{aligned} \tag{1}$$

Again, we took advantage of the neutral p-type region to set the boundary condition $\mathscr{E}\left(-\frac{w}{2}\right) = 0$. The maximum electric field will occur at $x = 0$. If we plug in $x = \frac{w}{2}$ the electric field on the n-type boundary is also zero.

$$\mathscr{E}_{max} = \mathscr{E}(0) = -\frac{qaw^2}{8\epsilon} \tag{2}$$

Integrating again allows us to derive the potential of the junction.

$$\begin{aligned}
\frac{d\phi}{dx} &= -\mathscr{E} \\
d\phi &= -\frac{qa}{2\epsilon}\left(x^2 - \frac{w^2}{4}\right) dx \\
\int_{\phi\left(-\frac{w}{2}\right)}^{\phi(x)} d\phi &= -\int_{-\frac{w}{2}}^{x} \frac{qa}{2\epsilon}\left(x^2 - \frac{w^2}{4}\right) dx
\end{aligned}$$

$$\Rightarrow \phi(x) - \phi\left(-\frac{w}{2}\right) = -\frac{qa}{2\epsilon}\left(\frac{x^3}{3} - \frac{w^2}{4}x\right)\Big|_{-\frac{w}{2}}^{x}$$

$$\phi(x) = -\frac{qa}{2\epsilon}\left(\frac{x^3}{3} - \frac{w^2}{4}x\right) \tag{3}$$

$$\Rightarrow V_{bi} = \frac{qaw^3}{12\epsilon}, \text{ for } |x| \leq \frac{w}{2} \tag{4}$$

$$w = \sqrt[3]{\frac{12\epsilon V_{bi}}{qa}} \tag{5}$$

$$\Rightarrow w = \sqrt[3]{\frac{12\epsilon(V_{bi} - V_{bias})}{qa}} \tag{6}$$

The steps above should be surprisingly simple compared to the abrupt junction. There is no need to split the device into two sets of equations and find ways to equate one another. The built-in voltage is again taken with respect to the neutral p-type region, implying $\phi\left(-\frac{w}{2}\right) = 0$. After integrating the electric field, evaluating the expression at $x = -\frac{w}{2}$ results in zero, and presents a more complex equation than the abrupt junction. We can verify that this equation is reasonable since a linear doping profile integrates into a quadratic electric, which then integrates again into a cubic potential. To compute the built-in voltage the integral is evaluated at $x = \frac{w}{2}$. After finding V_{bi} only algebra is necessary to find the depletion width both under a bias and without a bias.

Note that a common trap is to rely on the $V_{bi} = \frac{kT}{q}\ln\left(\frac{N_A N_D}{n_i^2}\right)$. Recall that when we derived this formula for the built-in potential it used uniform doping in each region. With a dependence on position, we need to determine the doping concentration at the boundary of the depletion width, these values are the correct quantities to plug into the V_{bi} equation. The linear doping profile makes this process easy since $x_n = x_p = \frac{w}{2}$. The doping concentration at both boundaries are equal in size, implying $N_A \rightarrow \frac{aw}{2}$ and $N_D \rightarrow \frac{aw}{2}$, where the arrow indicates how the abrupt junction variables for V_{bi} transform to the new quantities.

$$V_{bi} = \frac{kT}{q}\ln\left(\frac{a^2w^2}{4n_i^2}\right) \tag{7}$$

$$= \frac{2kT}{q}\ln\left(\frac{aw}{2n_i}\right) \tag{8}$$

Note that the 4 in the denominator of the natural log equals 2^2. To extract the square from each term in the logarithm 4 was expanded as a square. With expressions for the electric field and potential across the device, we can plot them over the length of the junction.

Example: We have a Silicon Linearly graded junction with an impurity gradient of 10 cm^{-4}, find the width of the depletion region, w, and the built-in voltage, V_{bi}.

Solution: A naive attempt would be to plug in values into the above V_{bi} equation. Every quantity is known, except the built-in voltage and the depletion width; 2 unknowns with 1 equation. Luckily we have the cubic root equation for the depletion region width in terms of the built-in voltage. **Note** substitution will not work because we are solving a system of nonlinear equations. There are several techniques to solve nonlinear equations: Iterative, graphical, and load-line. Granted, the load-line technique requires one of the equations to be linear which does not apply to this problem. The iterative technique involves assuming an initial w, or V_{bi} and solving for the other value. We would prefer to choose V_{bi} because we have an intuitive range of values. We know typical silicon abrupt junctions have built-in voltages around 0.7 V, but we cannot confidently say the depletion width is 1 μ m, or 10 nm, and so on.

For the sake of length, the full iterative process will not be included. The first iteration with a built-in voltage guessed at 0.3 V results in a depletion width of 0.619 μmeee;. The 0.619 microns results in $V_{bi} = 0.657V$ and the process repeats. The answer using either iterative or graphical results in $V_{bi} \approx 0.671$ V and $w \approx 0.809\mu$m.

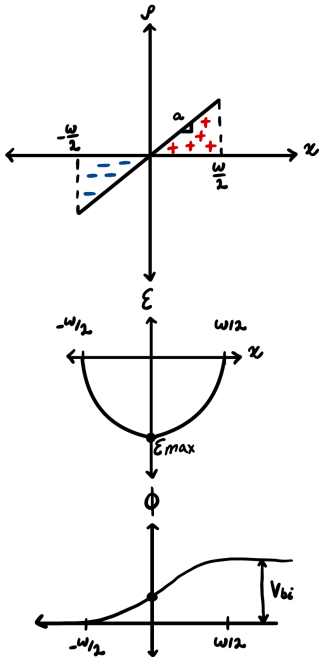

Figure 1: Doping profile, electric field, and potential across a linearly graded junction.

Junction Capacitance:

Throughout the several plots of the doping density, detail has been given toward the depletion region charge. Note that the positive and negative space charges are explicitly drawn. We know that each depletion region has an associated width that these charges "congregate". This should be reminiscent of a capacitor. Hence, a PN junction **under reverse bias** has an associated junction capacitance.

The general equation for a capacitor is $C = \epsilon \frac{A}{D}$. The size of the plates is the cross-sectional area of the device, and the distance is the depletion width. Typically we omit the area units to better compare the capacitance of various devices without knowing the area. Implying the junction capacitance is more accurately $C = \frac{\epsilon}{w}$ and the units are $[C] = \frac{F}{\text{cm}^2}$.

Before we dive into the short derivation, we might want to ask if this junction capacitance is useful? Reverse biases applied to the junction will vary the depletion region width. Increasing the reverse bias increases w, which decreases the capacitance. Inversely, decreasing the reverse bias decreases the depletion width, increasing the capacitance. Thinking of the physical distance between capacitor plates is a good way of remembering this property. As for the utility of the device, a variable capacitance, or varactor, is used in analog filters, radio receivers, and voltage-controlled oscillators. There are many other applications, but these are the three most common applications. The name varactor is a combination of the variable nature of a reactive component. Capacitors and inductors are reactive components since they have reactance as opposed to resistance.

To derive the junction capacitance, we can use our already derived equations, and plug them into the depletion region width. For an abrupt and linearly graded junction the junction capacitance C_j is,

$$C_j = \frac{\epsilon}{\sqrt{\frac{2\epsilon(N_A+N_D)}{qN_AN_D}(V_{bi} - V_{bias})}} \tag{9}$$

$$C_j = \frac{\epsilon}{\sqrt[3]{\frac{12\epsilon}{qa}(V_{bi} - V_{bias})}} \tag{10}$$

Where the first equation is for the abrupt junction and the second for the linearly graded. Another way of deriving these equations involves the fundamental, $Q = CV$ equation for a capacitor. The junction capacitance is the differential charge over the differential voltage,

$$C_j = \frac{dQ}{dV} \tag{11}$$

The electric field is a voltage over some distance, implying $dV = wd\mathscr{E}$.

$$C_j = \frac{dQ}{wd\mathscr{E}}$$

Charge and electric field are related by the dielectric permittivity. For example, a high permittivity material holds onto the stored charge which reduces the amount of field passing through the material. Inversely, a very leaky dielectric will have a large electric field since the material cannot easily hold onto charge.

$$\begin{aligned} d\mathscr{E} &= \frac{dQ}{\epsilon} \\ \Rightarrow C_j &= \frac{\epsilon}{w} \end{aligned} \tag{12}$$

Note that the above equation is identical to the ideal capacitor normalized with respect to the area. With these equations, we can see the inverse relationship between junction capacitance and bias voltage. The denominator of each junction capacitance depends on $(V_{bi} - V_{bias})$. As V_{bias} approaches V_{bi} the denominator will become smaller since $(V_{bi} - V_{bias}) \to 0$. As the denominator decreases the capacitance must increase. However, the capacitance cannot increase indefinitely. **Forward bias eliminates the junction capacitance**. Hence, our equations only apply for applied voltages below the built-in voltage.

Example: To provide some practical values of this junction capacitance lets examine a Silicon abrupt junction with $N_A = 2 \cdot 10^{19}$ cm^{-3} and $N_D = 8 \cdot 10^{15}$ cm^{-3}. The device is under room temperature and we apply zero bias and a -4 V bias.

Solution: The built-in voltage for the device is calculated from the doping concentrations,

$$\begin{aligned} V_{bi} &= \frac{kT}{q} \ln\left(\frac{N_A N_D}{{n_i}^2}\right) \\ &= 0.026 * \ln\left(\frac{2 \cdot 10^{19} 8 \cdot 10^{15}}{2.25 \cdot 10^{20}}\right) \\ &= 0.886V \end{aligned}$$

With the built-in voltage we can plug into the junction capacitance equation above, and the depletion region width equation from the last notes. The respective capacitance and depletion width are,

$$\begin{aligned} C_j &= 2.76 \cdot 10^{-8} \frac{\text{F}}{\text{cm}^2} \text{ , for } V_{bias} = 0 \text{ V} \\ C_j &= 1.175 \cdot 10^{-8} \frac{\text{F}}{\text{cm}^2} \text{ , for } V_{bias} = \text{-4 V} \\ w &= 3.82 \cdot 10^{-5} \text{ cm} = 0.382\mu\text{m} \text{ , for } V_{bias} = 0 \text{ V} \\ w &= 8.96 \cdot 10^{-5} \text{ cm} = 0.896\mu\text{m} \text{ , for } V_{bias} = \text{-4 V} \end{aligned}$$

The standard units for length are in centimeters, cm. It is an incredibly common mistake to either drop the units of the depletion width if it is given, or to not convert given lengths to centimeters. Over time you will memorize that 10,000 μm = 1 cm, and the conversion will be easy. Regardless, if you get seemingly nonsense numbers from an equation double check you are using the correct units. Also, note the capacitance is on the order of several to tens of nanofarads. Using a varactor to achieve large capacitances is not a viable technique.

Conclusion:

This concludes our discussion on the PN junction. This set of notes has been kept relatively short. In our discussion of devices, the abrupt junction will be assumed. Hence, the linearly graded junction and junction capacitance are somewhat secondary to the core PN junction discussion. Hence, they have kept separated into a different set of notes. Calling these topics secondary does not imply they are unimportant and not worthy of study. Linearly graded junctions have their own uses in BJTs optimization, and

junction capacitance is an incredibly interesting phenomenon that makes for many interesting circuits and exam questions. The overall process used to derive the linearly graded junction is identical to the abrupt junction. However, we were lucky in not needing to utilize a piece-wise approach to stitch together both depletion regions. Paired with charge conservation eliminating the need to track x_n and $-x_p$, the derivation is relatively straightforward. Our next set of notes will look at the current-voltage characteristic of the PN junction.