Topic 16: MOS System Introduction

Preface:

Our discussion of MOS devices will be more qualitative than prior sections. To rigorously derive expressions describing MOS systems would take several more weeks than the semester gives us. If you choose to continue your study of semiconductor physics, other courses offered by the university will delve into MOS physics at a less introductory level. The key takeaway from this set of notes is the fundamentals of how a MOS system operates.

MOS Definition:

You may be familiar with the MOSFET, an alternate transistor to the BJT. Before we discuss the MOSFETS we must describe what a MOS system is and some of the underlying properties. MOS is short for Metal-Oxide-Semiconductor. I will use the term substrate, or body, to denote the semiconductor layer, and any MOS system involves a metaphorical sandwich of these three materials. The metal allows a voltage to be applied to the device. A thin layer of oxide, typically silicon dioxide (SiO_2), separates the metal from physically contacting the substrate. The substrate is typically p-type silicon, but n-type may be used as well. The substrate is then doped in various ways to create MOSFETS and MOS Capacitors, the two devices we will discuss. Unless stated otherwise, we will assume a p-type substrate.

The standard physical structure for a MOS system is provided below.

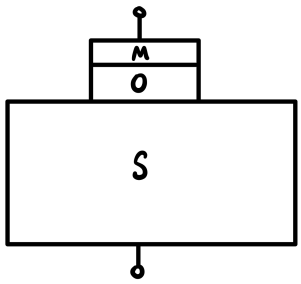

Figure 1: MOS system physical structure.

MOS Capacitor:

The MOS system provided in Fig. 1 is identical to the physical structure of a MOS capacitor. We will see shortly why the system is called a capacitor. Imagine we tie the substrate to ground and apply a voltage to the metal. What would happen? The oxide physically blocks current from entering the substrate, implying the oxide creates an open circuit. When we attach the voltage source the metal it will become the same potential as the voltage source, accumulating positive charge. Let's call the voltage source V_G and sketch the physical structure.

As positive charges gather on the metal, an electric field is emitted into the oxide. One could imagine the metal layer as a sheet of charge, and sheet charges emit an electric field perpendicular to the surface. Hence, the electric field will pass through the oxide into the semiconductor. If the bias voltage is sufficiently large, the electric field will be large; $\mathscr{E} = -\frac{dV}{dx}$. A sufficiently strong electric field will repel holes within the substrate. The majority holes within the substrate will be repelled near the oxide-substrate interface. The repelled holes will leave a pocket of net negative charge.

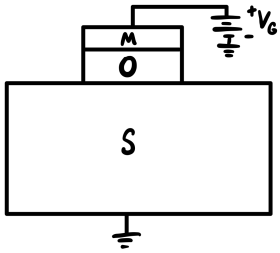

Figure 2: MOS capacitor biased by a voltage source.

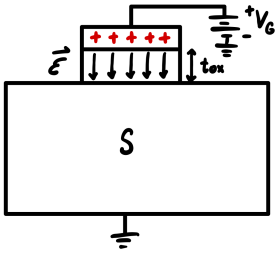

Figure 3: MOS capacitor internal electric field.

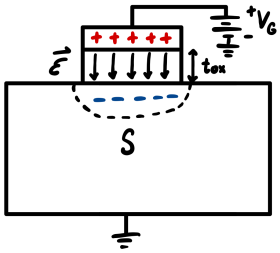

Figure 4: MOS capacitor internal capacitance.

The dashed black line represents the pocket of negative charge induced by the electric field. This pocket is a small depletion region sustained by the applied voltage. Hopefully, now the name MOS capacitor makes sense. A strong V_G forms a capacitor with the plates being the metal and the pocket of charge within the substrate. The oxide composes the dielectric since it is sandwiched between the metal and substrate.

We can calculate this capacitance quite easily. As with the junction capacitance of a PN junction, the capacitance is normalized with respect to the metal contact area. The normalization provides a fair comparison across devices. The typical oxide thickness is on the order of tens to hundreds of nanometers. Let's assume the oxide is 50 nm thick and the relative permitivity of silicon dioxide is approximately 3.9. To calculate the normalized capacitance, we rely on the parallel plate definition of capacitance,

$$\begin{aligned} C &= \frac{\epsilon_r \epsilon_0}{t_{ox}} \\ &= \frac{3.9 * 8.85 \cdot 10^{-14} \frac{\text{F}}{\text{cm}}}{5 \cdot 10^{-6} \text{cm}} \\ &= 0.6903 \frac{\text{nF}}{\text{cm}^2} \end{aligned}$$

Anytime we calculate a quantity double check you have correct units. I cannot reiterate enough that centimeters is our standard length and you will get incorrect values if you do not adhere to it. It is typical for most MOS capacitors to exhibit a capacitance on the order of several nanofarads. If we has a MOS device with a 10 nm, square, contact the contact area would be approximately $1 \cdot 10^{-12}$ cm^2, producing an extremely small capacitance; $\approx 10^{-20}$ F. This small example is aimed at iterating

how small oxide capacitance can be, especially with the 5 to 10 nanometer processes at the major chip foundries.

MOSFET Structure:

MOSFET is short for Metal-Oxide-Semiconductor Field-Effect Transistor. The Field-effect term in MOSFET heavily implies the electric field will be important throughout our investigation. The physical structure for the MOSFET is provided below. Note, the substrate is p-type.

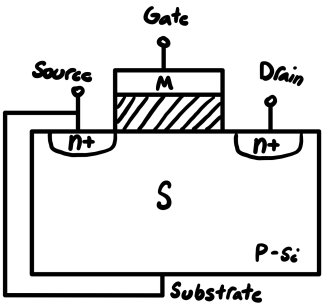

Figure 5: MOSFET physical structure.

At first, the MOSFET does not seem drastically different from a MOS capacitor. The metal, oxide, and semiconductor are still present. Note that some people, including myself, prefer to color the oxide with lines. Taking the extra time to "color" the oxide reminds me that a physical barrier is in place between the metal and substrate. The primary difference between the MOS capacitor and the MOSFET is the n-type diffusions within the substrate. These diffusions are called **wells** since they form metaphorical wells in the substrate. In a MOSFET it is necessary that the well type differs from the substrate type. If both of the n-type wells were p-type then we would have essentially a MOS capacitor with slightly different behavior.

Unlike the MOS capacitor, the MOSFET is a four-terminal device. We have the gate and substrate, also called the body, like before, but the addition of the two wells. The MOSFET is a symmetrical device, so it does not matter which terminal you call source and drain. However, whichever terminal you defined as the source must be shorted to the body. The terminology describes which terminal is sourcing carriers and which terminal is draining carriers from the device. We will use the left n-well as the source. The source is typically connected to the body to mitigate the body effect. The body effect is beyond the scope of this course, but tieing the source and body together prevents the substrate from floating at a random voltage.

If we ignore the two n-wells for a moment, the MOSFET is identical to the MOS capacitor. If we apply some large gate-to-source voltage, V_{GS}, the positive charge on the gate will repel the majority carriers within the bulk. If sufficient majority carriers have been repelled we say the device is in **inversion**. We call this process inversion since it inverts the majority charge of the body. The figure below visualizes the inverted MOSFET.

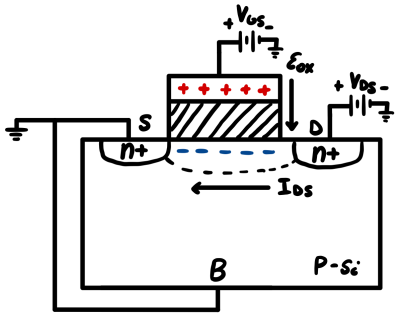

Figure 6: Inverted n-channel MOSFET.

Note that the term **channel** has been used in the caption above. The channel refers to the region of inversion within the body. If the channel is composed of electrons, the MOSFET is an n-channel device. Similarly, a p-channel device exhibits a channel formed by holes. When a MOSFET is under strong inversion, large V_{GS}, a channel of charges connects the two n-wells. Under this state, we say the MOSFET is on, but without some voltage across the drain-to-source, V_{DS}, the carriers will be stationary. The drain-to-source current, I_{DS} , has been drawn to show that carriers pass through the channel from the source to the drain. Remember that I_{DS} is a conventional current, implying the electrons flow from the source to the drain; hence the terminology.

V_{GS} Influence:

Like the BJT, we have two voltage sources controlling the behavior of the MOSFET. V_{GS} is responsible for the formation of the channel and will ultimately determine when the device is on or off. We can imagine that small V_{GS} cannot form a complete channel. The electric field is not strong enough to repel the majority carriers in the body. As V_{GS} increases, the channel will form, and further increases to the voltage will increase the thickness of the channel into the body. A thicker channel can sustain a larger current, similar to water flowing through a large diameter pipe.

While it is convenient knowing that V_{GS} controls the on/off state of the device, we do not know the first point at which the device turns on. We know that applying 10 V to the gate will likely turn the device on, but what is the minimum such voltage to form the channel. We call this voltage the **threshold voltage** and denote it by V_T. Any voltage below V_T the device is considered off, and any voltage above V_T the device is on. The body effect mentioned earlier offsets this threshold since V_{GS} is not purely across the oxide.

V_{DS} Influence:

To better understand the effects of V_{DS} we need to observe a practical MOSFET datasheet. Within the datasheet, you will likely see a parameter called the on-resistance. When we have a MOSFET that is on, implying the channel is fully formed, then we can model the channel as a resistor. The channel has some resistivity, ρ. We know from physics that the resistance of a material is $R = \frac{\rho L}{A}$. The channel has a fixed length, the distance between the two n-wells, and a cross-sectional area. Hence, it is perfectly reasonable to model the channel as a resistance when the device is under strong inversion. If the gate-to-source voltage is held relatively constant then the physical size of the channel remains the same.

The resistance model is mentioned because V_{DS} will influence the magnitude of the drain current. As long as V_{GS} is sufficiently large, then I_{DS} is due to a voltage across a resistor. Hence, somewhere in our current-voltage characteristic, a linear-like relation is expected. However, we must ask ourselves what happens for large V_{DS}? In the MOS capacitor, the metal-substrate voltage was responsible for inversion. Whereas the MOSFET includes a voltage across the gate-to-source, gate-to-drain, and drain-to-source.

Imagine for a moment that V_{DS} is large. Let's say that $V_{GS} = 5\text{V}$ and $V_{DS} = 5\text{V}$. We know the gate-to-source voltage is 5V and the drain-to-source voltage is 5V, but what about the gate-to-drain voltage? A KVL across the device gives $V_{GD} = V_{GS} - V_{DS} = 0\text{V}$; V_{GS} and V_{DS} are referenced with respect to the source, implying the gate-to-drain is the difference of the two voltages. These values imply $V_{GS} = 5\text{V}$ and $V_{GD} = 0\text{V}$. Would we still expect that the channel has a uniform thickness? No. The channel would not be uniform since the electric field near the source well is larger than the electric field near the drain terminal. The channel thickness reduction is shown in the figure below.

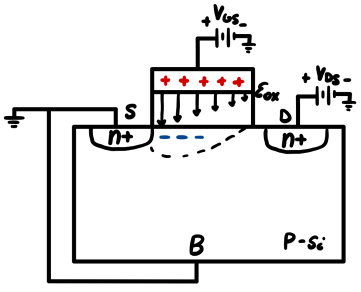

Figure 7: N-channel MOSFET under Saturation.

The oxide color has been removed to visualize electric field strengths. As mentioned, the field near the source will be strong, and it decays toward the drain. The decay will leave inverted charges near the source but not the drain, forcing the channel to be pinched off. The pinch-off point is defined as the point where the inverted region ends. If V_{DS} were to increase, the pinch-off would become more substantial, forcing the point to move toward the source. Since V_{DS} controls pinch-off we can define the voltage where pinch-off first starts as $V_{DS,sat}$. This mode is called saturation, which will be discussed shortly.

The figure below visualizes the channel pinch-off for several V_{DS} values.

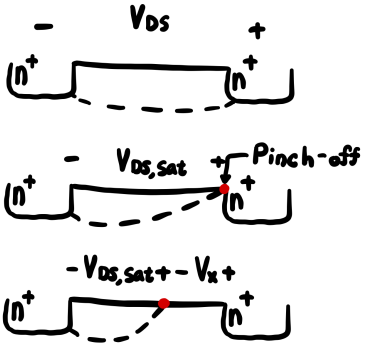

Figure 8: MOSFET pinchoff visualization.

The figure above represents the channel due to three different V_{DS} values. An n-channel device is assumed, and the solid line connecting the two channels is the oxide-semiconductor interface. The source terminal is to the left, and the drain is to the right. In the top-most sketch, the channel is uniform in thickness and without pinch-off. This implies that $V_{GS} \approx V_{GD}$ or that V_{DS} is relatively small. As V_{DS} is increased V_{GD} decreases, forming a pinch-off. The pinch-off point is shown as a red dot. Under this V_{DS} value, the drain-to-source voltage equals the saturation voltage. As V_{DS} is further increased the pinchoff point moves toward the source, but the voltage across the region must still be $V_{DS,sat}$.

Hopefully, now the definition of the saturation voltage is clear. Since we defined $V_{DS,sat}$ as the voltage across the channel under pinch-off, under saturation, the voltage across the channel will be $V_{DS,sat}$ regardless of V_{DS}. Any increases in V_{DS} beyond the saturation voltage will be dropped across the non-channel region, denoted by V_x. As V_{DS} increases, V_x will increase as well. To reiterate, moving downwards across each sketch implies a larger V_{DS}.

So why does this non-intuitive definition of saturation voltage matter? Imagine the electrons within the channel. The saturation voltage will still induce a current. When an electron reaches the end of the channel several things could happen. The momentum of the carrier is large enough to continue by diffusing through the p-type into the drain terminal, or the carrier will recombine before reaching the drain. Either way, a non-negligible current is present throughout the device. Since $V_{DS,sat}$ is always present across the channel the current will be constant for V_{DS} above the saturation voltage. This is why the mode is called saturation since additional V_{DS} does not produce a larger current.

Terminology:

For the remainder of our discussion, it will be helpful to define some terms beforehand.

- Channel Depth, Z: The depth, into the page, of the MOSFET channel; typically in μm or nm.
- Channel Length, L: The length between the two n or p-type wells; typically in μm or nm.
- Electron Mobility, μ_n: The mobility of electrons within an n-channel; given in $\frac{\text{cm}^2}{\text{V-s}}$
- Hole Mobility, μ_p: The mobility of holes within a p-channel; given in $\frac{\text{cm}^2}{\text{V-s}}$
- Oxide Capacitance C_{ox}: The oxide capacitance, normalized with respect to the contact area; $C_{ox} = \frac{\epsilon_{ox}\epsilon_0}{t_{ox}}$. Units are typically in the $\frac{\text{nF}}{\text{cm}^2}$ range.

- Transconductance, g_m: The ratio of output current to an input voltage when all other voltages are held constant. For the MOSFET, it is the ratio of drain current to gate voltage when V_{DS} is held constant.
- Channel Conductance, g_D: The ratio of output current to output voltage when all other voltages are held constant. For the MOSFET, it is the ratio of drain current to drain-to-source voltage, when V_{GS} is held constant.

Current Voltage Characteristic:

As with the BJT, the current-voltage characteristic will help visualize the modes of operation for the device. The IV characteristic for the MOSFET is provided below.

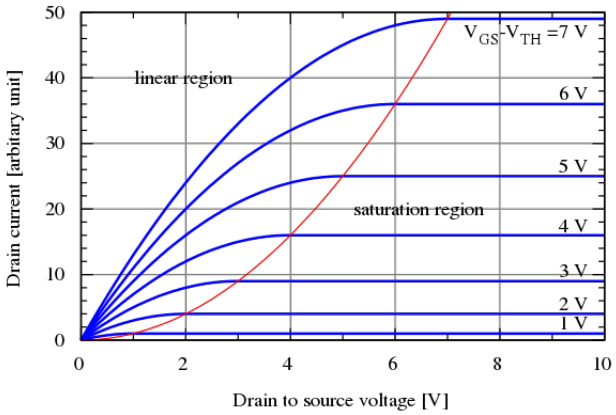

Figure 9: MOSFET IV characteristic curves. ([2])

The horizontal axis represents the drain-to-source voltage, V_{DS}, and the vertical axis represents the drain current I_D. Since we have two input voltages and one output current, we must fix one voltage and plot against the other. For the reasons mentioned above, we fix V_{GS} and allow V_{DS} to vary, forcing the device into various modes of operation. As V_{GS} increases, we know the current must increase, providing a family of current curves for various V_{GS}.

The Sze text provides the following equation for the drain current. This expression is valid for any mode of operation. However, the derivation is quite lengthy and out of scope for our purposes. The more convenient choice is to break down each mode of operation and describe their current expressions respectively.

$$I_D \approx \frac{Z\mu_n C_{ox}}{L}\left[V_D\left(V_G - 2\Psi_B - \frac{V_D}{2}\right) - \frac{2\sqrt{2\epsilon_s q N_A}}{3C_{ox}}\left((V_D + 2\Psi_B)^{3/2} - (2\Psi_B)^{3/2}\right)\right] \tag{1}$$

We will not derive the current equations from scratch, and we will not expect you to learn the derivation on your own. For our purposes we will provide the general drain current expressions and focus on investigating them.

Cutoff:

The horizontal axis represents $I_D = 0$. When the channel is not present, the region exhibits a high resistance restricting the current. For $V_{GS} < V_T$, the device is operating in cutoff. For our purposes, we do not care about the sub-threshold behavior of the device. Hence, we will assume for $V_{GS} < V_T$ that $I_D = 0$. The value of V_{DS} is irrelevant because if V_{GS} is below the threshold the channel cannot be formed on the source-side. If the channel cannot be formed on the source side then any value of V_{DS} will reduce V_{GD} and hence the channel width on the drain-side. Either way, the channel cannot be formed if $V_{GS} < V_T$.

Saturation:

In Fig. 9 the red curve represents the saturation voltage over continuous V_{GS} values. For example, observe the $V_{GS} = 4\text{V}$ curve. The red curve intersects the blue curve at $V_{DS} = 4\text{V}$. It is not a coincidence that the saturation voltage is approximately the gate-to-source voltage. If we were given the figure without the red curve, we can visually inspect the plot and approximate the saturation voltage as 4V. The general current equation for the saturation mode is provided below. **Note** the independence of V_{DS}.

$$I_D = \frac{Z\mu_n C_{ox}}{2L}\left(V_{GS} - V_T\right)^2 \tag{2}$$

Beginning with the constants on the left, the term $\frac{Z\mu_n C_{ox}}{L}$ will appear in every current equation for the MOSFET; excluding cutoff. This term must have units of $\frac{\text{A}}{\text{V}^2}$. The $(V_{GS} - V_T)^2$ term must cancel with the units of this large constant. This constant is based on physical parameters of the device. The ratio of Z and L represents the ratio of width to length of the MOSFET. Remember the MOSFET is a three-dimensional device and the size of the length and width are important. Imagine a long channel with a fixed width, would the resistance be large or small compared to a short channel? If a carrier must travel longer within the channel it is equivalent to a larger value resistance, so the current must decrease as the channel length increases. As for the width of the channel, if the width increases it simply means more current can pass through the channel. The mobility term is necessary since higher mobility materials will produce a higher drain current. As for the subscript, the channel type determines which mobility to use. Lastly, the oxide capacitance is the only confusing term. The oxide capacitance is dependent on the threshold voltage since large thickness oxides produce small oxide capacitance. A small capacitance requires a large gate voltage to drive the device into inversion, hence increasing the threshold voltage. Therefore, the oxide capacitance will be proportional to the drain current due to the dependence on the threshold voltage.

Triode (Linear):

Depending on who created the IV characteristics figure, people use the terms **ohmic**, **triode**, and **linear** to represent the linear-region of the MOSFET. For context, an ohmic device is a device that satisfies Ohm's law. Since the region is linear, it indeed satisfies Ohm's law. The more interesting name, triode, originates from the triode vacuum tube since they behave similarly. The general current equation for the triode mode is provided below.

$$I_D = \frac{Z\mu_n C_{ox}}{L}\left(V_{GS} - V_T - \frac{V_{DS}}{2}\right)V_{DS} \text{ , for } V_{DS} << (V_{GS} - V_T) \tag{3}$$

The condition $V_{DS} << (V_{GS} - V_T)$ may seem arbitrary so let's investigate further. When pinch-off first appears, we know $V_{DS} = V_{DS,sat}$. We also know that $V_{GS} \geq V_T$ since the channel is complete on the source-side. Again, when $V_{DS} = V_{DS,sat}$, it is the first such moment when the channel is complete, implying $V_{GS} \geq V_T$. When the channel is complete, both V_{GS} and V_{GD} must be greater than the threshold. If V_{GD} is below the threshold then the device is saturated. If V_{GD} is above the threshold then the channel is complete and zero pinch-off is present. From a KVL across the device,

$$\begin{aligned} V_{GD} &= V_{GS} - V_{DS,sat} \\ V_T &= V_{GS} - V_{DS,sat} \\ \Rightarrow V_{DS,sat} &= V_{GS} - V_T \end{aligned} \tag{4}$$

This saturation equation is rife throughout circuit analysis of MOSFETS. If we substitute the final expression into the constraint $V_{DS} << (V_{GS} - V_T)$ we see $V_{DS} << V_{DS,sat}$. In short, as long as V_{DS} is well below the saturation voltage, we know the device is behaving linearly. Under the small V_{DS} assumption we can simplify the current expression into a linear equation.

$$I_D = \frac{Z\mu_n C_{ox}}{L}\left(V_{GS} - V_T\right)V_{DS} \text{ , for } V_{DS} << (V_{GS} - V_T) \tag{5}$$

Before we address the simplified current expression, it is important to reiterate that Eq. 3 is quadratic. If we look at the IV characteristic for $V_{DS} \leq V_{DS,sat}$ there is a linear region and a quadratic region. For

low V_{DS}, we have shown in the equation above that a linear relationship exists since every quantity aside V_{DS} is constant for a given curve. As V_{DS} increases to values near $V_{DS,sat}$, we can no longer assume small V_{DS}, and the current becomes quadratic. We know that the current cannot be linear since the physical shape of the channel varies as V_{DS} approaches the saturation voltage.

Device Properties:

Transconductance:

The transconductance is defined as,

$$g_m = \left.\frac{\partial I_D}{\partial V_{GS}}\right|_{V_{DS}=constant} \tag{6}$$

If we have a resistor, we know that Ohm's law states $R = \frac{V}{I}$. If we wanted to find the conductance of the resistor, we invert the fraction since $G = \frac{1}{R}$. Taking the derivative of $\frac{I}{V}$ gives the conductance of a device with respect to some voltage. The added constraint of holding either V_{DS} or V_{GS} constant ensures the conductance is due to whichever voltage is being differentiated with respect to. The partial derivative is necessary since the provided current expressions are functions of both V_{GS} and V_{GD}.

The term transconductance should remind us of two-port networks. If we imagine the MOSFET as a two-port network with the gate as the input, the drain is the output, and the source as common, then the transconductance term becomes incredibly powerful. Varying the voltage on the gate induces a current through the device for a fixed V_{DS}. Hence, modulating the gate voltage transfers this change into the drain current.

Channel Conductance:

The channel conductance is defined as,

$$g_D = \left.\frac{\partial I_D}{\partial V_{DS}}\right|_{V_{GS}=constant} \tag{7}$$

Intuitively we know that the channel conductance must provide information on how conductive a channel is. If we hold V_{GS} constant and take the derivative with respect to V_{DS}, the channel conductance will tell us how small changes in V_{DS} will affect the current. If we operate the MOSFET in the linear region, this property will help determine how small-signal voltages are converted into current.

Modes of Operation:

If we apply the transconductance and channel conductance equations to the three modes of operations we can see some interesting results. For cutoff,

$$g_m = g_D = 0 \tag{8}$$

Cutoff mode is relatively straightforward since we assume the current is zero. The partial derivative of zero with respect to V_{GS} or V_{DS} must equal zero. For saturation we have,

$$g_m = \frac{Z\mu_n C_{ox}}{L}(V_{GS} - V_T) \tag{9}$$

$$g_D = 0 \tag{10}$$

From the IV curve, the saturation current is constant with respect to V_{DS}. Implying, it should not be surprising that $g_D = 0$. **Note** that the saturation current is not truly constant. As with the BJT, nonidealities exist that prevent the drain current from remaining truly constant. For those curious, this effect is called channel-length modulation. The nonzero transconductance is due to V_{GS} driving the current capability of the channel. Lastly, for triode mode we have,

$$g_m = \frac{Z\mu_n C_{ox}}{L} V_{DS} \tag{11}$$

$$g_D = \frac{Z\mu_n C_{ox}}{L} (V_{GS} - V_T) \tag{12}$$

Under triode, we would expect both the transconductance and channel conductance to be nonzero. The transconductance should always be nonzero outside of cutoff for reasons mentioned above. The channel conductance must be nonzero since we have a nonzero slope of the current curve. It is quite interesting that the channel conductance under triode is equal to the transconductance of saturation. Regardless, the point is that variations in either V_{DS} or V_{GS} will influence the characteristics of the MOSFET in a predictable manner.

MOSFET Types:

The bulk of this set of notes assumed an n-channel MOSFET, but there are several other types. There are four types of MOSFETS: enhancement mode and depletion mode NMOS and PMOS devices. We differentiate between N and PMOS devices based on the channel type; NMOS exhibit an n-channel, and PMOS exhibit a p-channel. To form the p-channel, we need an n-type substrate with p-type source and drain wells. To form the channel the gate-source voltage must become negative; typically we swap the subscript to V_{SG}. The negative charges on the metal will repel electrons within the body, leaving holes. The holes will then form the channel between the two p-type wells.

The enhancement versus depletion mode is where interesting device behavior emerges. **Enhancement mode** devices are off by default. The channel is not present, and hence a voltage is necessary to enhance, or create, the channel. Inversely, depletion mode devices are on by default. The channel is always present, requiring a voltage to turn the device off. For example, a depletion NMOS device requires a negative gate-to-source voltage to accumulate holes back into the region where the channel exists. An alternate perspective is a negative voltage repels electrons. However, one mode of operation within a MOS device is called **accumulation**. Whenever a voltage is applied to the device such that the majority carrier within the substrate is attracted toward the oxide, the device is under accumulation. Accumulation is the inverse of inversion.

The following table is presented in the Sze text and concisely describes the four modes of operations, their IV characteristics, and transfer characteristics.

The chart is split into the four MOSFET types, beginning with n-channel devices. The top-most row is the familiar n-type device studied throughout this set of notes. Note that the transfer characteristics states under what V_{GS} the device is on or off. For example, we know that $V_{GS} \geq V_T$ for the drain current to be non-zero.

When we shift our focus to the n-channel depletion device we see some interesting behavior in the IV characteristic. When $V_{GS} = 0$V the drain current is non-zero for a positive V_{DS}. By definition, a depletion mode device is on when no gate voltage is applied. The threshold voltage for the device is negative, as shown by the transfer characteristic. As a negative voltage is applied, the device gradually turns off. However, if a positive voltage is applied, the device is, for lack of a better word, turned on "harder." Depletion mode devices can be driven by voltages that increase the size of the channel increasing the current capabilities.

The PMOS devices are also included in the figure. The key difference between the various curves is the voltage and current polarities. We defined the drain current as the current from the drain to the source. Similarly, we have used the gate-to-source, and drain-to-source conventions. To properly bias a PMOS device we need to swap this convention to source-to-gate, V_{SG}, and source-to-drain, V_{SD}. It seems the Sze text wanted to minimize confusion and stick to the V_{GS} and I_D convention, opting to multiply by -1 to convert the polarities of each voltage and current.

To reiterate, a PMOS device needs a negative gate-source voltage to turn the device on. If V_{DS} is kept positive, holes would traverse from the drain-to-source composing a current from the drain-to-source. If V_{SD} is used, the current through the channel is from the source-to-drain. It is unsure why Sze opted to swap the drain current polarity for the PMOS, but as long as you keep track of the polarities it does not matter if you choose a positive V_{SD} or a negative V_{DS}.

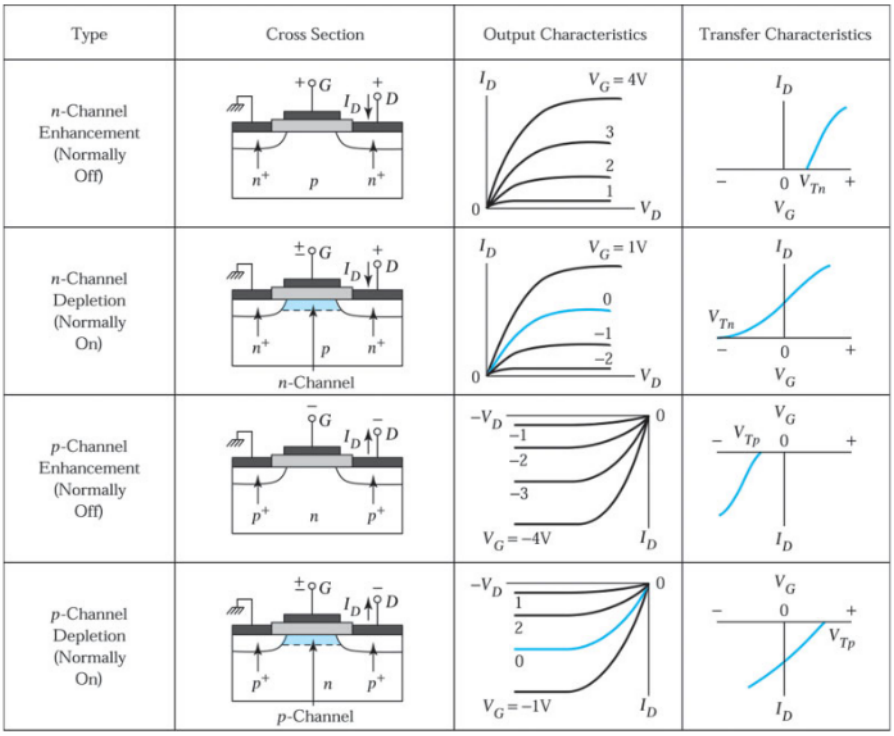

Figure 10: MOSFET types, IV characteristics, and transfer characteristics. ([1])

Conclusion:

This set of notes marks the end of the course. As mentioned we sadly do not get to delve into the derivations of MOSFET physics, however, I hope that this introduction has been sufficient. The MOSFET is an incredibly interesting device when you dive into the more complex physics, so I encourage you to do some investigation if you are interested. Within these notes we discusses MOS systems, the MOS capacitor and the MOSFET. The bulk of the notes were focused on the MOSFET with the MOS capacitor serving as a simple case of charge inversion within the semiconductor layer. The MOSFET operates under three modes: cutoff, triode, and saturation. The IV characteristic is incredibly similar to the BJT, although some regions have been swapped. Despite the similarity in IV curves the fundamental process of charge inversion, channel formation, pinch-off, and such differentiate the two devices. The MOSFET can also be manufactured in either enhancement or depletion mode introducing many variations of the device.

I would like to thank Dr. Chan for giving me the opportunity to write these notes. I know I can be quite verbose at times, however, I do it to emulate me sitting with you talking through the concepts. For those who have read through these notes and have any feedback please direct them to Dr. Chan.

References

[1] Lee M. K. Sze S. M. *Semiconductor Devices: Physics and Technology 3rd edition*. Wiley. (2012).

[2] Wikipedia contributors. *Current–voltage characteristic*. Aug. 2021. URL: https://en.wikipedia.org/wiki/Current%E2%80%93voltage_characteristic.