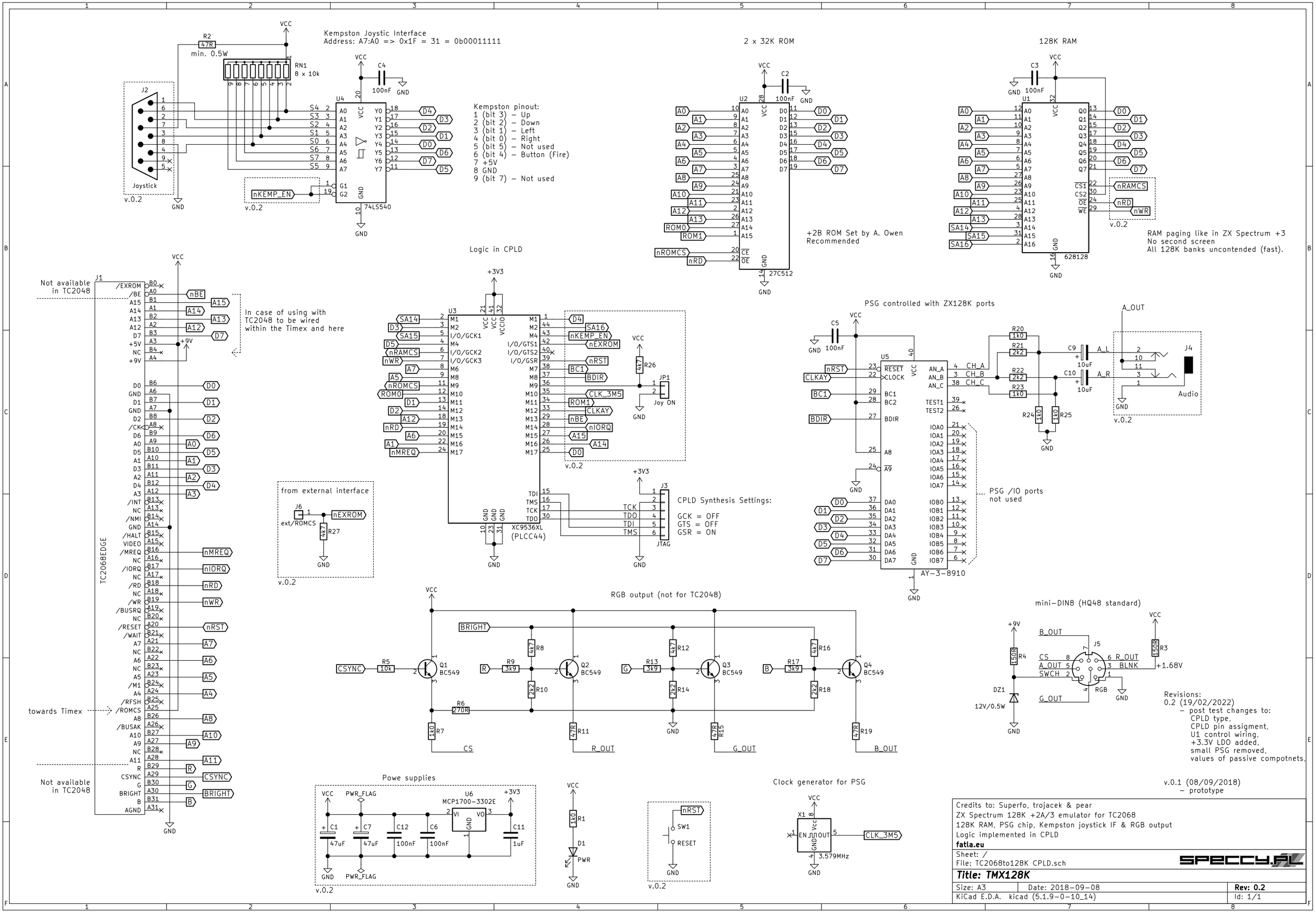
Kempston Joystic Interface
Address: A7:A0 => 0x1F = 31 = 0b00011111
Kempston pinout:
1 (bit 3) – Up
2 (bit 2) – Down
3 (bit 1) – Left
4 (bit 0) – Right
5 (bit 5) – Not used
6 (bit 4) – Button (Fire)
7 +5V
8 GND
9 (bit 7) – Not used
2 x 32K ROM
+2B ROM Set by A. Owen
Recommended
128K RAM
RAM paging like in ZX Spectrum +3
No second screen
All 128K banks uncontended (fast).
Not available in TC2048
In case of using with TC2048 to be wired within the Timex and here
Logic in CPLD
from external interface
CPLD Synthesis Settings:
GCK = OFF
GTS = OFF
GSR = ON
PSG controlled with ZX128K ports
PSG /IO ports not used
towards Timex
Not available in TC2068
RGB output (not for TC2048)
mini-DIN8 (HQ48 standard)
Revisions:
0.2 (19/02/2022)
– post test changes to:
CPLD type,
CPLD pin assigment,
U1 control wiring,
+3.3V LDO added,
small PSG removed,
values of passive compotnets.
v.0.1 (08/09/2018)
– prototype
Powe supplies
Clock generator for PSG
Credits to: Superfo, trojacek & pear
ZX Spectrum 128K +2A/3 emulator for TC2068
128K RAM, PSG chip, Kempston joystick IF & RGB output
Logic implemented in CPLD
fatla.eu
Sheet: /
File: TC2068to128K CPLD.sch
Title: TMX128K
Size: A3
Date: 2018-09-08
Rev: 0.2
KiCad E.D.A. kicad (5.1.9-0-10_14)
Id: 1/1