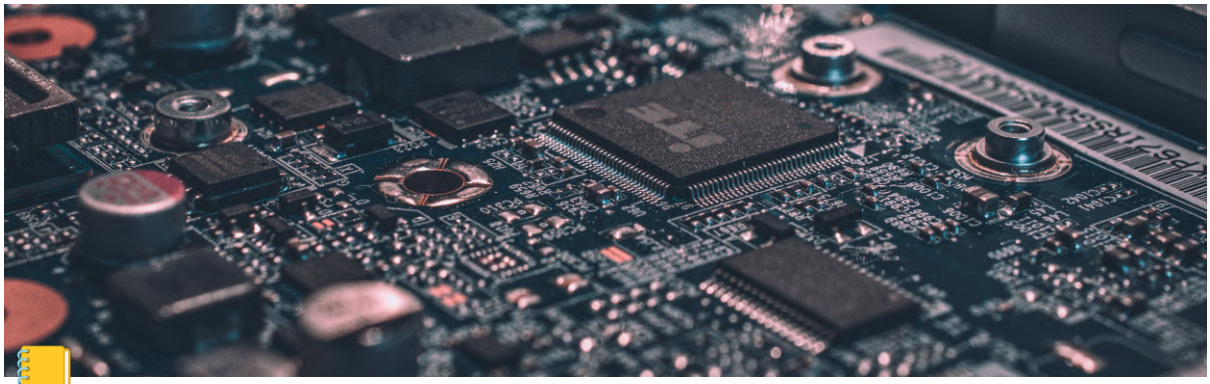
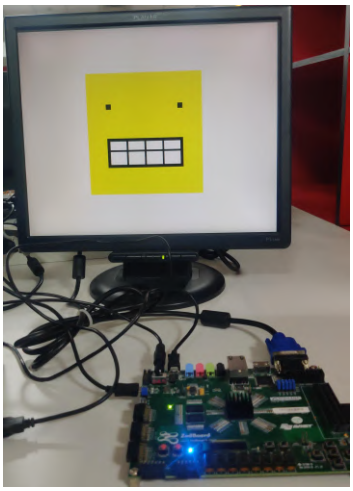


FPGA Report

Created	@November 29, 2022 12:13 AM
Class	FPGA
Description	Maurya Patel - IMT2020517 Anshul Madurwar - IMT2020554 In this project we have built a programmable device that will be co VGA screen, using this you need to display an animation video on the VGA monitor.
Resources	http://www.cse.cuhk.edu.hk/~mcyang/ceng3430/2020S/Lec07%20Driving%20VGA%20Display%20with%20ZedBoard.pdf https meads/Emoji_Animation http://tinyvga.com/vga-timing/640x480@60Hz https://github.com/delhatch/Zedboard_Mandel/blob/ma

Proposed design:



Simulation of the final project using Zed-board

In this proposed design we are displaying a 3 framed animated video on the screen using a VGA Cable. For this, we are using 640p x 480p resolution running at a 60Hz frame rate. To satisfy these VGA Timing requirements we look at certain factors that determine the pitch frequency of the output screen.

VGA stands for Video Graphics Array and it has a simple pinout structure based on 15 pins. The pinout is different for different boards but the amazing documentation makes it a fun activity. Thus we configure it separately each time we work with a different board.

Now talking about the Pitch Frequency, we are working with a 640p x 480p image for which the pitch frequency is defined to be 25MHz

The calculation is done as follows:

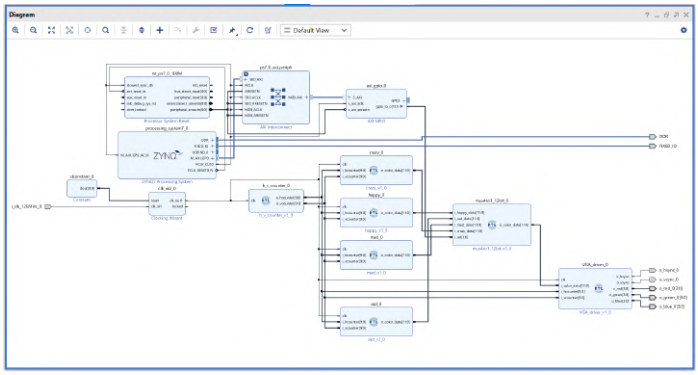
Horizontal Timing
Horizontal Pixels: 640
Front Porch : 16
Sync Width : 96
Back Porch : 48
Total Pixels : 800

Vertical Timing
Horizontal Pixels: 480
Front Porch : 10
Sync Width : 2
Back Porch : 33
Total Pixels : 525

For a single frame = 800 * 525 pixel duration
For a frame rate of 60Hz = 800 * 525 * 60 = 25.2 MHz.

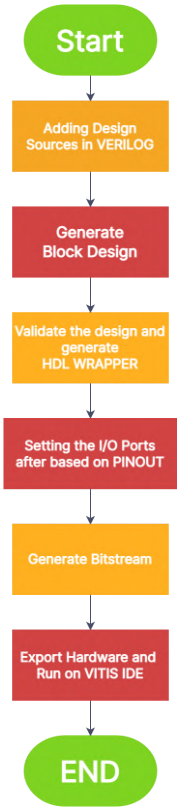
Thus approximating it to the nearest frequency we use 25 Mhz as our pitch frequency.

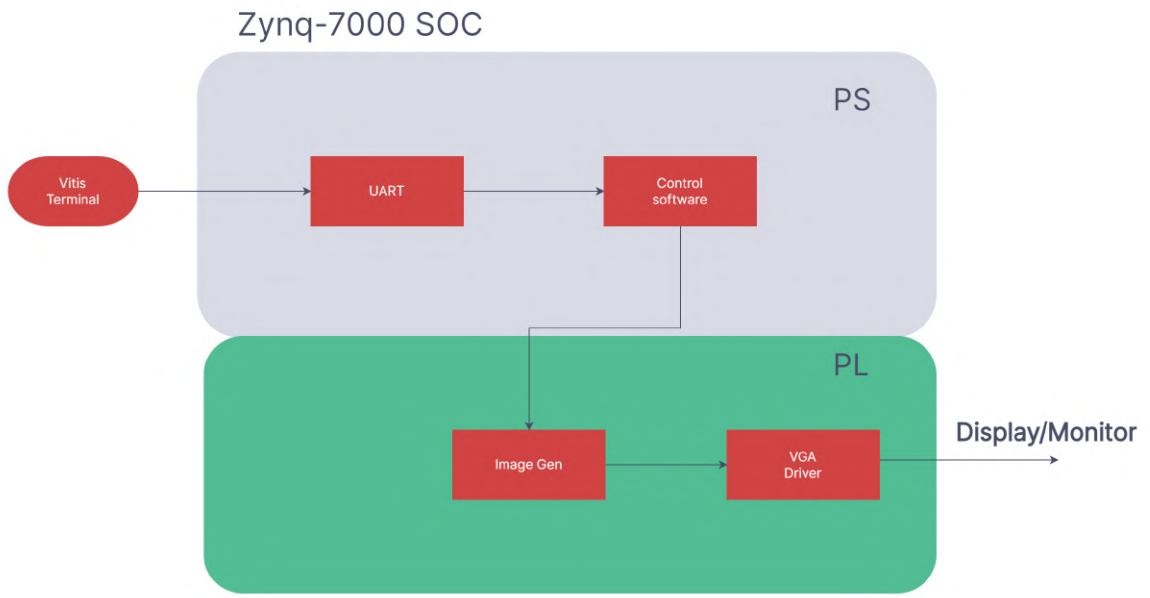
Block design:



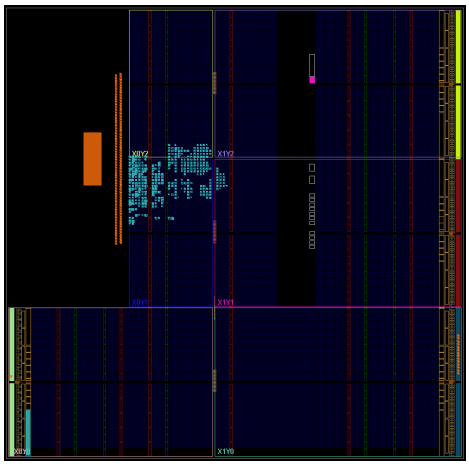
Block Design based on VGA driver and other Verilog files.

Flowchart:





Implementation:

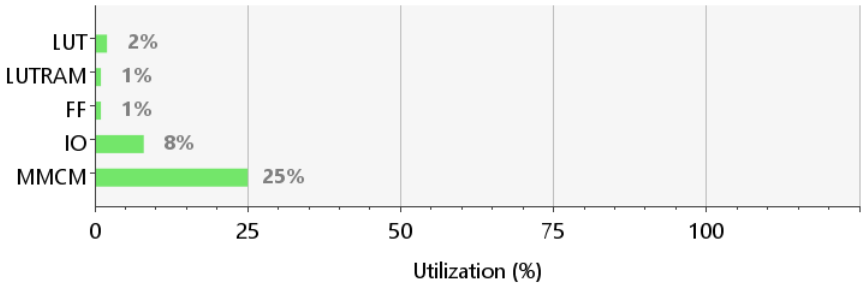


Resource utilization:

Name	Slice LUTs (53200)	Slice Registers (106400)	F7 Muxes (26600)	Slice (13300)	LUT as Logic (53200)	LUT as Memory (17400)	Bonded IOB (200)	Bonded IOPADs (130)	BUFGCTRL (32)	MMCME2_ADV (4)
N design_1_wrapper	956	690	3	346	896	60	15	130	3	1
design_1_i (design_1)	956	690	3	346	896	60	0	0	3	1
xlconstant_0 (design_1_xlconstant_0	0	0	0	0	0	0	0	0	0	0
VGA_driver_0 (design_1_VGA_driver	21	0	0	9	21	0	0	0	0	0
sad_0 (design_1_sad_0_0)	149	33	0	49	149	0	0	0	0	0
rst_ps7_0_100M (design_1_rst_ps7_	17	33	0	9	16	1	0	0	0	0
ps7_0_axi_periph (design_1_ps7_0_a	350	464	0	148	291	59	0	0	0	0
processing_system7_0 (design_1_pr	0	0	0	0	0	0	0	0	1	0
mux4to1_12bit_0 (design_1_mux4to	12	0	0	6	12	0	0	0	0	0
mad_0 (design_1_mad_0_0)	97	35	2	35	97	0	0	0	0	0
happy_0 (design_1_happy_0_0)	84	31	1	36	84	0	0	0	0	0
h_v_counter_0 (design_1_h_v_counte	21	20	0	9	21	0	0	0	0	0
crazy_0 (design_1_crazy_0_0)	174	34	0	57	174	0	0	0	0	0
clk_wiz_0 (design_1_clk_wiz_0_0)	0	0	0	0	0	0	0	0	2	1
axi_gpio_0 (design_1_axi_gpio_0_0)	38	40	0	12	38	0	0	0	0	0

Detailed Resource Utilization

Resource	Utilization	Available	Utilization %
LUT	956	53200	1.80
LUTRAM	60	17400	0.34
FF	690	106400	0.65
IO	15	200	7.50
MMCM	1	4	25.00



Resource Summary

Timing Summary

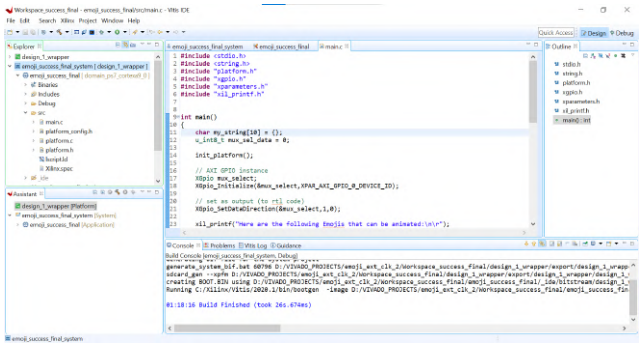
Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	3.944 ns	Worst Hold Slack (WHS):	0.030 ns	Worst Pulse Width Slack (WPWS):	3.000 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	1480	Total Number of Endpoints:	1480	Total Number of Endpoints:	761

All user specified timing constraints are met.

Setup and Hold Slack

VITIS IDE



main.c implementation in VITIS IDE

Pinout Structure of VGA for ZedBoard

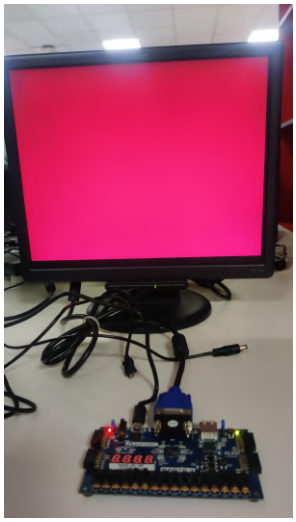
Here is the link to our animation video demonstration and files related to our project:

https://iiitbac-my.sharepoint.com/personal/maurya_patel_iiitb_ac_in/_layouts/15/onedrive.aspx?ga=1&id=%2Fpersonal%2Fmaurya_patel_iiitb_ac_in%2FDocuments%2FFPGA_project

These were our final results but there was a lot behind this…

#Trial 1:

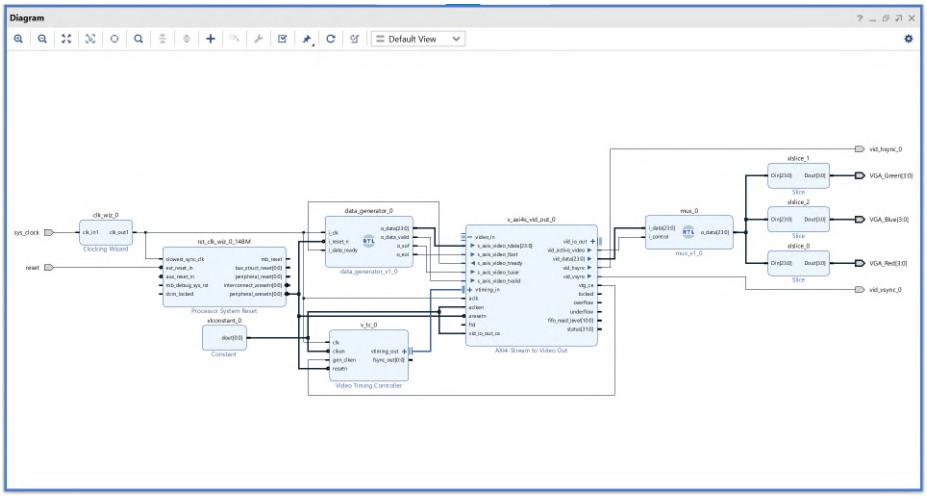
We initially used the Basys-3 board for our first demonstration. In this part, we figured out how to assign 12 VGA pins to the package pins. We were able to display one image and change the intensity of RGB using switches.



Display colouring module using Basys3 board

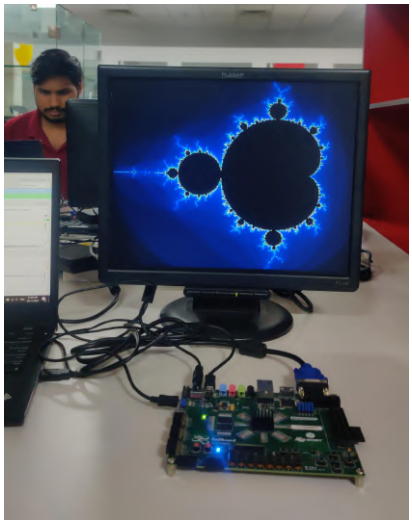
#Trial 2:

We tried to follow a tutorial to display images using the Zedboard but the Bit-Stream file was not displaying any kind of output.



#Trial 3:

We managed to display an image using ZedBoard. Here we have obtained the image based on a mathematical equation.



Displaying the image using Zed Board

Errors we encountered:

- When running the design for emoji-animated-video, we did not include the HDL wrapper, which gave us a faulty .xsa file. So we weren't able to open Vitis.
- We did not get the platform.h file in Vitis at first but after making some changes in our main.c file, we were able to locate it.
- Initially, after generating the block design, interconnect pins for the VGA were randomly assigned, so we had to change them according to the pinout structure.

Future works:

- We are planning to implement AXI4Stream for videos with a higher number of frames or longer videos.
- We plan to implement multiple select lines to display different videos based on user input.
- Currently, our design is targeted towards a 640p*480p display. We plan to generalize this for more displays.

References:

- http://www.cse.cuhk.edu.hk/~mcyang/ceng3430/2020S/Lec07 Driving VGA Display with ZedBoard.pdf
- https://github.com/dominic-meads/Emoji_Animation
- http://tinyvga.com/vga-timing/640x480@60Hz
- https://github.com/delhatch/Zedboard_Mandel/blob/master/VGA_Controller.v