Digital systems and basics of electronics

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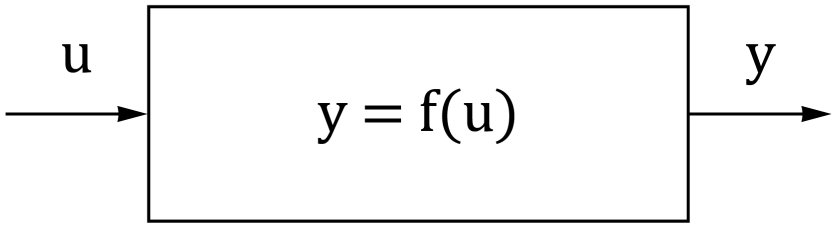
Sequential Circuits - introduction - lecture 9

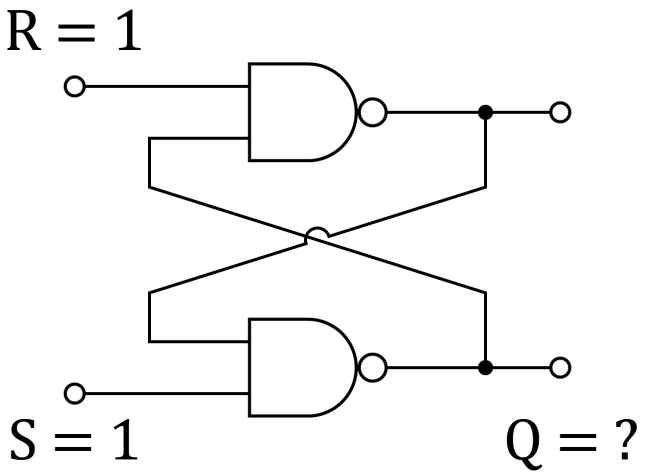
Combinational circuits



układ kombinacyjny

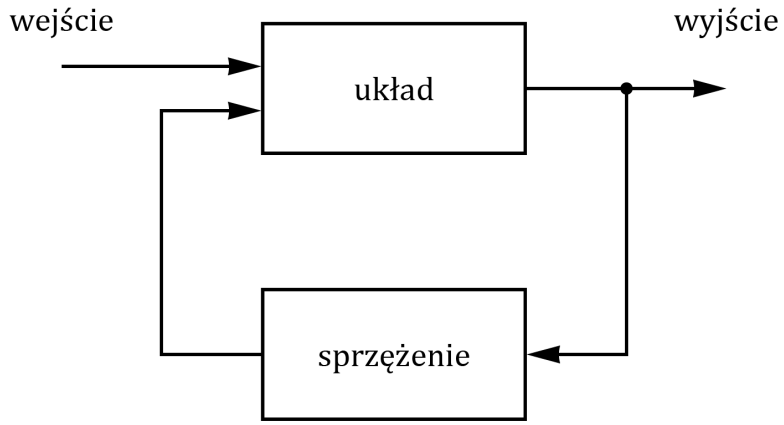
- *Combinational circuits* outputs depend only on inputs.

Flip-flops and "memory effect"



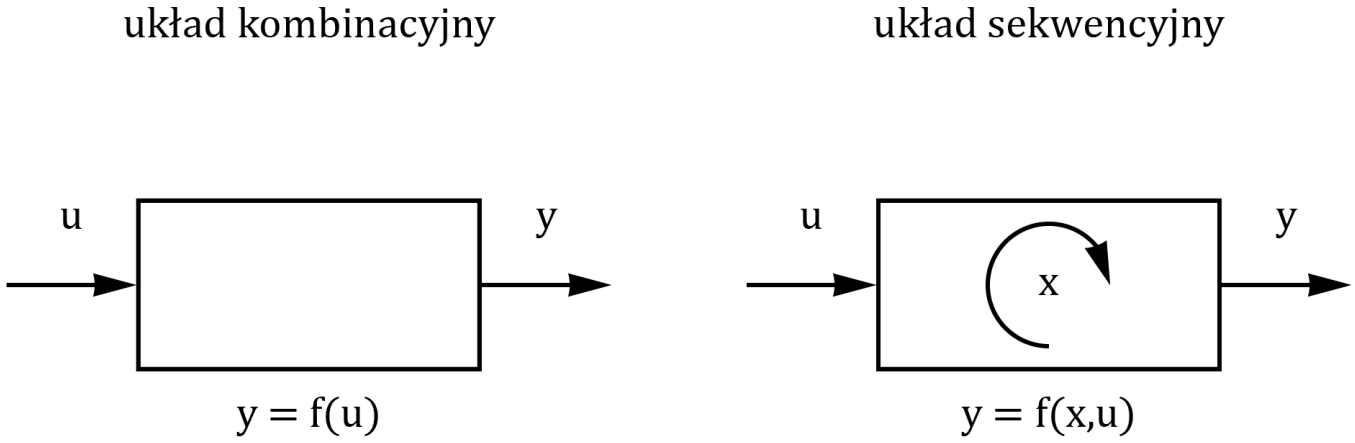
What is the current value of output Q ?

Feedback and "memory effect"



- In closed feedback loop system *output* influences *input*,
- That influence is an reason, why output depends not only on inputs, but also on history of outputs.

Combinational and sequential circuits



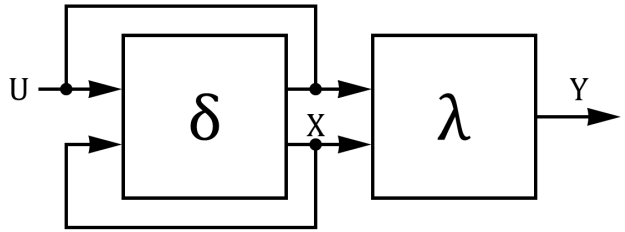
Sequential circuit as dynamical system

$$\begin{cases} x(k+1) = a \cdot x(k) + b \cdot u(k) & \text{state equation} \\ y(k) = c \cdot x(k) + d \cdot u(k) & \text{output equation} \end{cases}$$

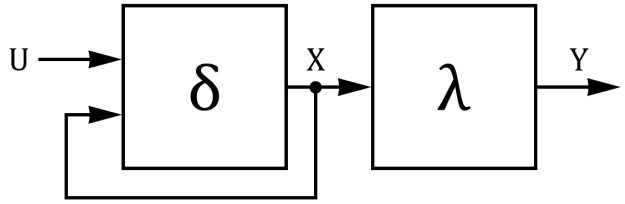
- *sequential* (dynamical) system there is *internal state*,
- *Internal state* can not be changed ąs one wishes". The value of current state depends on previously,
- *Internal state* can be not visible on system output (because is "internal").

Meayl'ego and Moore'a automata

automat Mealy'ego



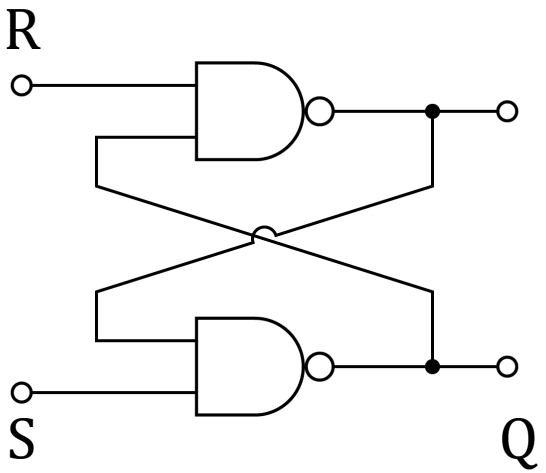
automat Moore'a



Output function is realized by combinational block (λ) and block (δ) realizes memory (sequential circuit).

RS flip-flop

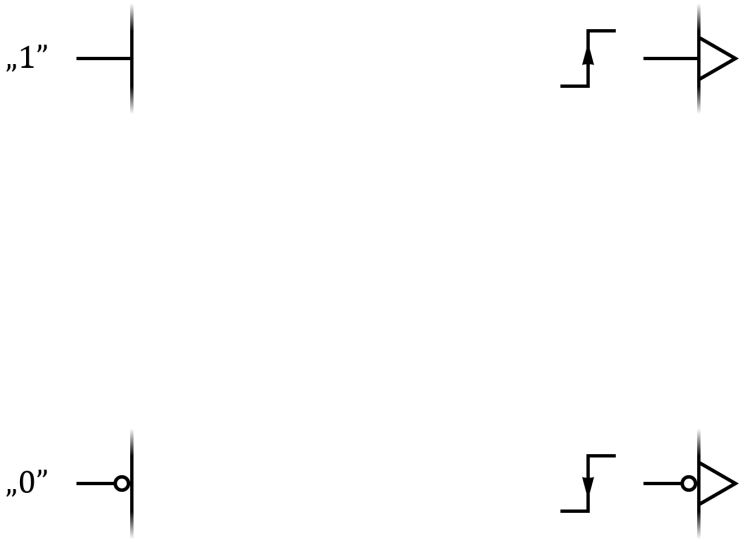
S_t	R_t	Q_{t+1}
0	0	*forbidden*
0	1	1
1	0	0
1	1	Q_t *(previously)*



$$Q_{t+1} = Q_t \cdot R_t + \overline{S_t}$$

- *Flip-flps* are the main components to build *sequential circuits*.

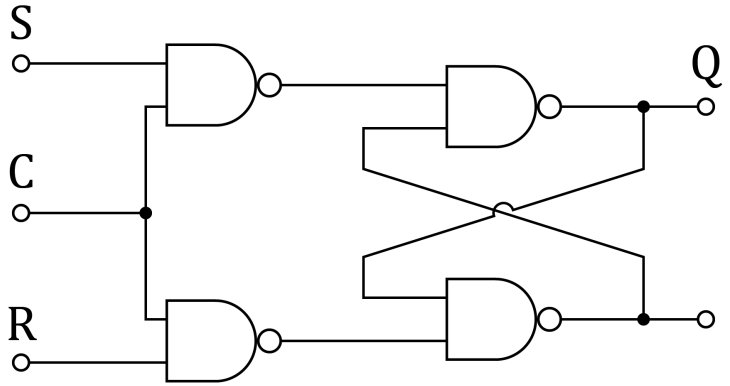
Clock - the way to synchronize changes



- The sequence of states is important in sequential circuits,
- Additional signal called *clock* is used to synchronize changes,
- Clock input can be activated by *state* (level) or *slope* (level change).

Clock activated with level

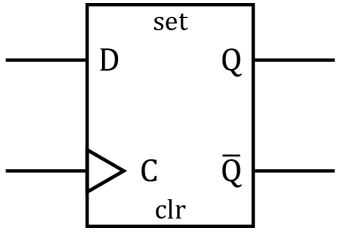
S	R	Q_{t+1}
0	0	Q_t
0	1	0
1	0	1
1	1	$forbidden$

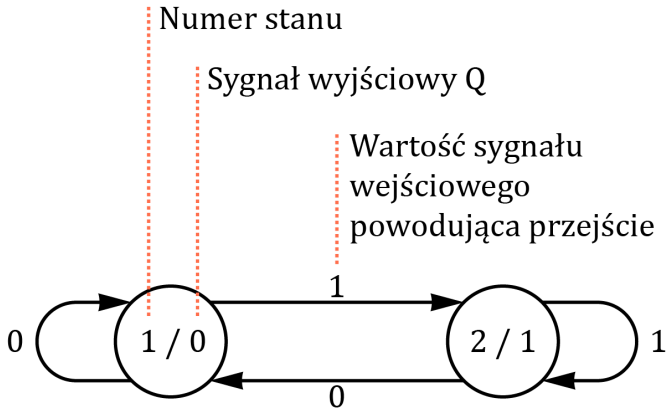


- If clock signal is equal zero $C = 0$ signals R and S have no any influence on output Q.
- If clock signal is equal one $C = 1$ output Q changes due to the table,
- the change of clock signal C from 1 to 0 causes the łatchóf output state - for that reason that circuit is sometimes called *latch*.

Type D flip-flop

D_t	Q_{t+1}
0	0
1	1



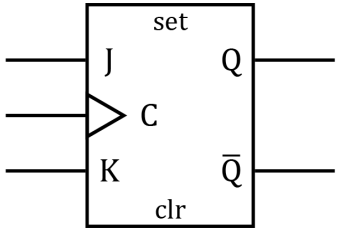


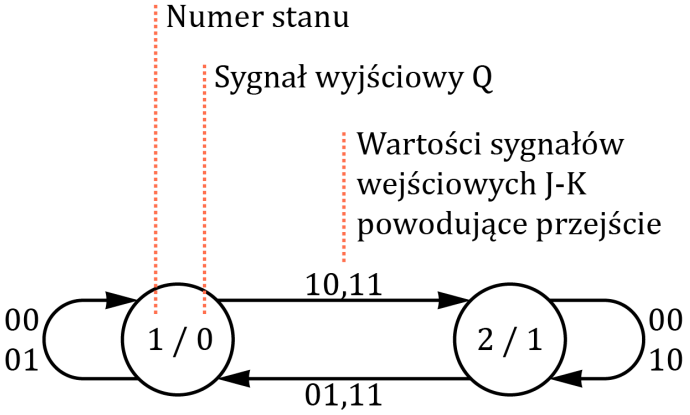
$$Q_{t+1} = D_t$$

- Output Q changes follow input D,
- Flip-flop has two states.
- Changes are synchronized with clock slope C,
- Flip-flop has asynchronic clearing input (CLR) and setting input (SET). Both inputs work independently on clock (immediately clears or sets output Q).

Type J-K flip-flop

J_t	K_t	Q_{t+1}
0	0	Q_t
0	1	0
1	0	1
1	1	$\overline{Q_t}$



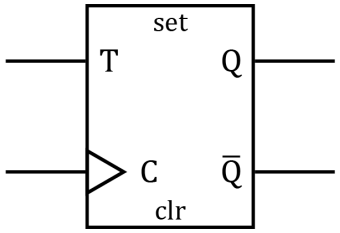


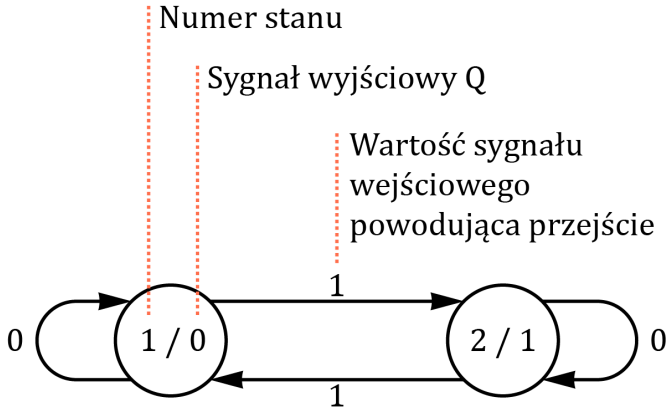
$$Q_{t+1} = J_t \cdot \overline{Q_t} + \overline{K_t} \cdot Q_t$$

- Flip-flop has two states.
- Changes are synchronized with clock slope C,
- Flip-flop has asynchronic inputs - clearing (CLR) and setting (SET).

Type T flip-flop

T_t	Q_t	Q_{t+1}
0	0	0
0	1	1
1	0	1
1	1	0

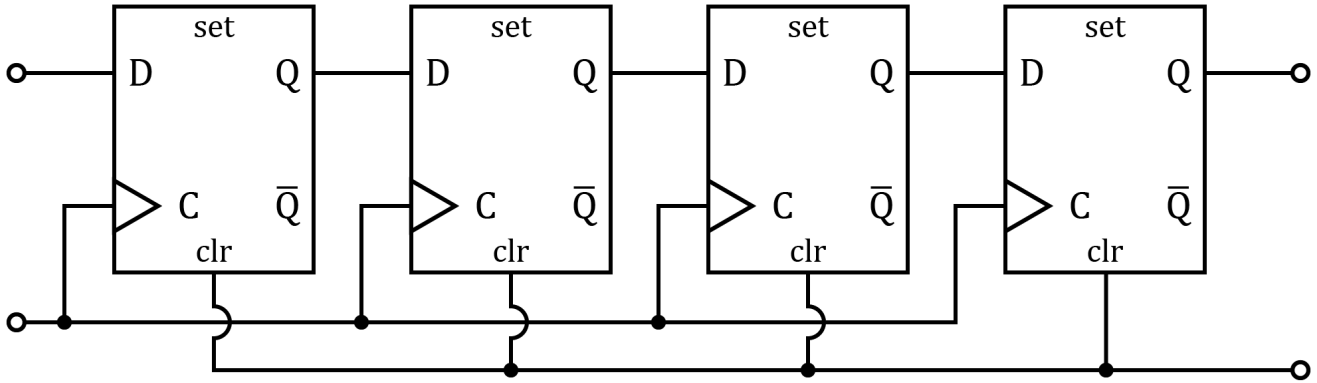




$$Q_{t+1} = T_t \oplus Q_t$$

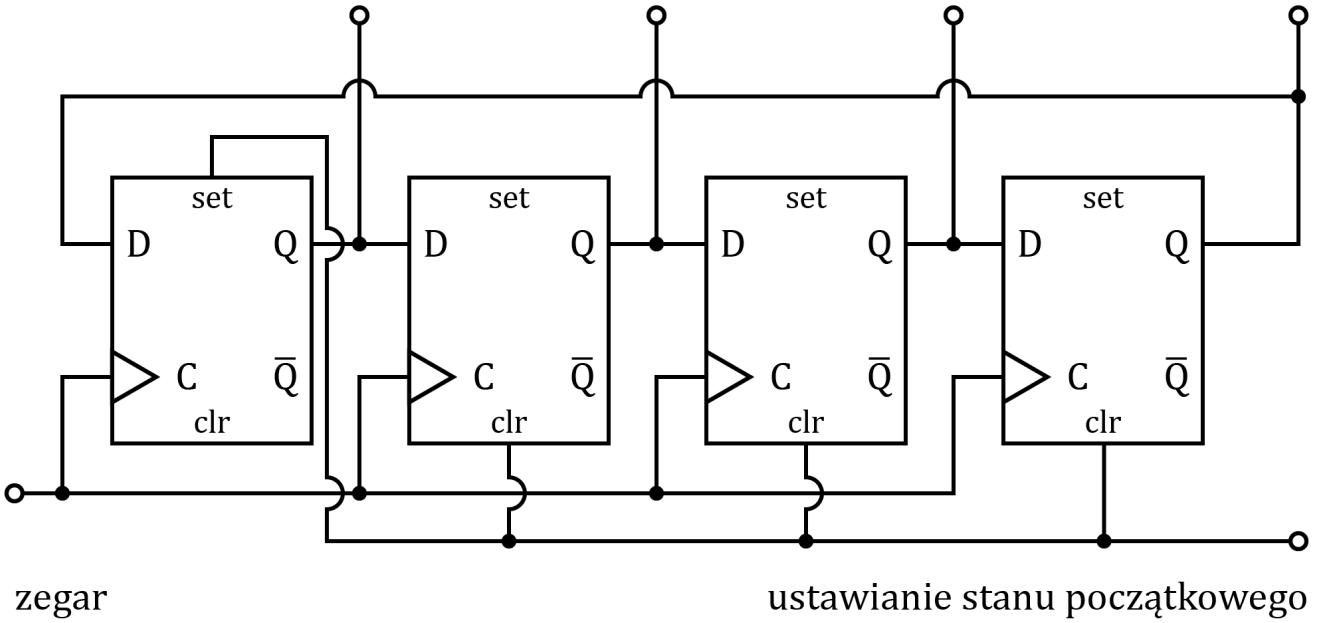
- In T-type flip-flop logical one on input causes that flip flop will change the state of output,
- Logical 0 on input T cause keeping the state of output.

Register



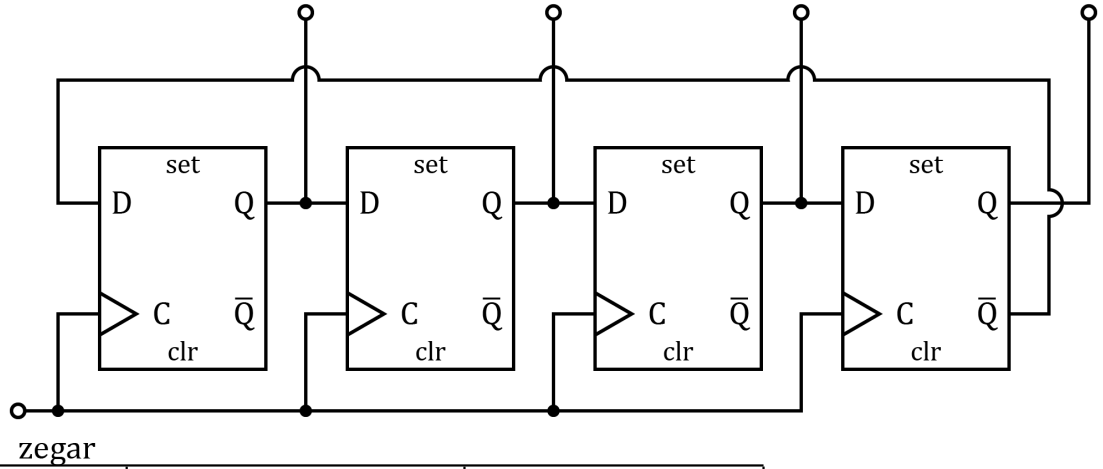
4-bits shifting register.

Ring counter



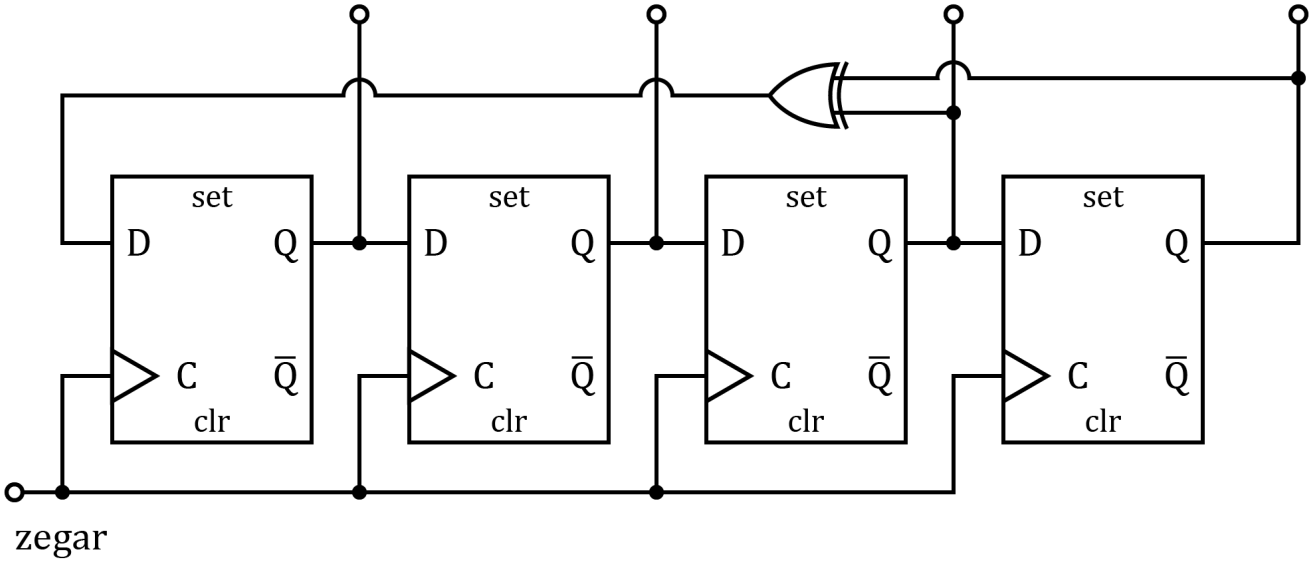
A ring counter is a type of counter composed of a circular shift register.

Twisted ring - Johnson counter



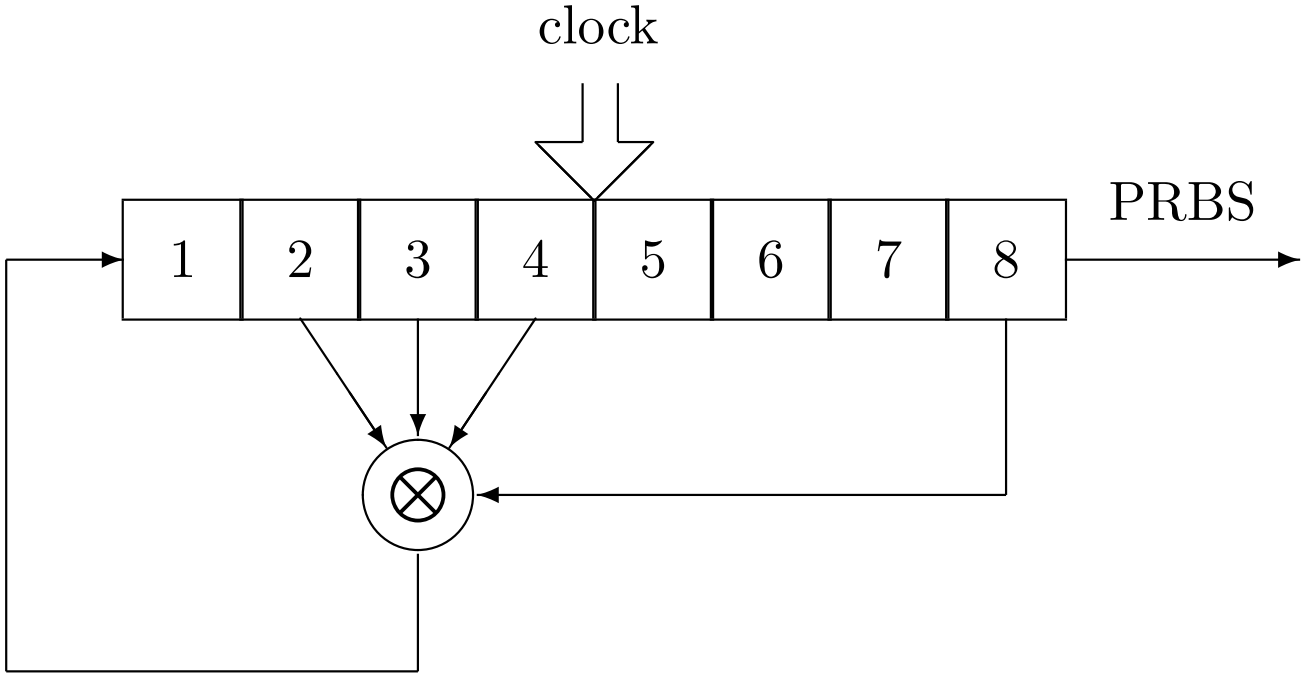
Wartość dziesiętna	Wartość binarna	Kod Johnsona
0	0000	0000
1	0001	0001
2	0010	0011
3	0011	0111
4	0100	1111
5	0101	1110
6	0110	1100
7	0111	1000

Pseudo-random signal generator using shift register



Generated signal seems to be randomly.

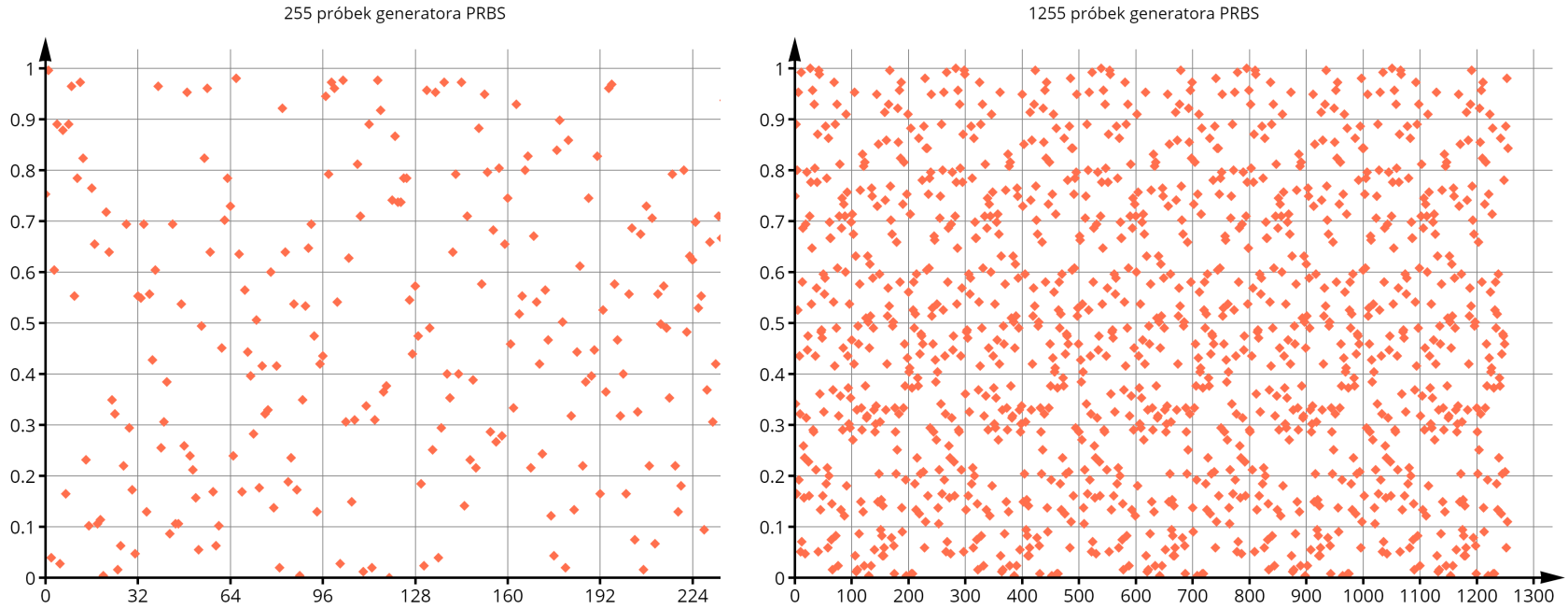
PRBS generator using shift register



Pseudo Random Binary Signal generator using 8-bits shift register.

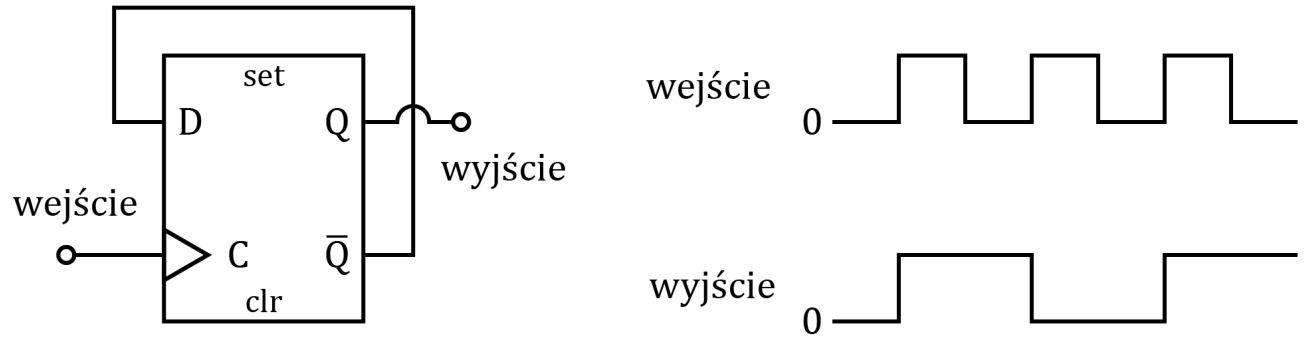
- **PRBS must be initialized with ones**
- For $T/T_o = 255$ bits: $2, 3, 4, 8,$
- for $T/T_o = 1023$ bts: $7, 10.$

Results of PRBS for 255 and 1255 samples



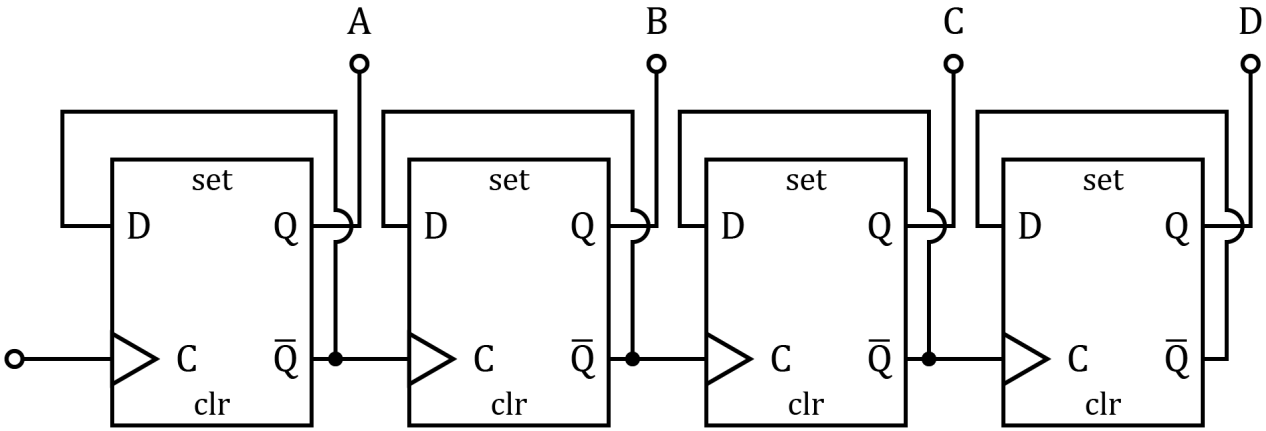
- PRBS is periodical

Frequencv divider 2



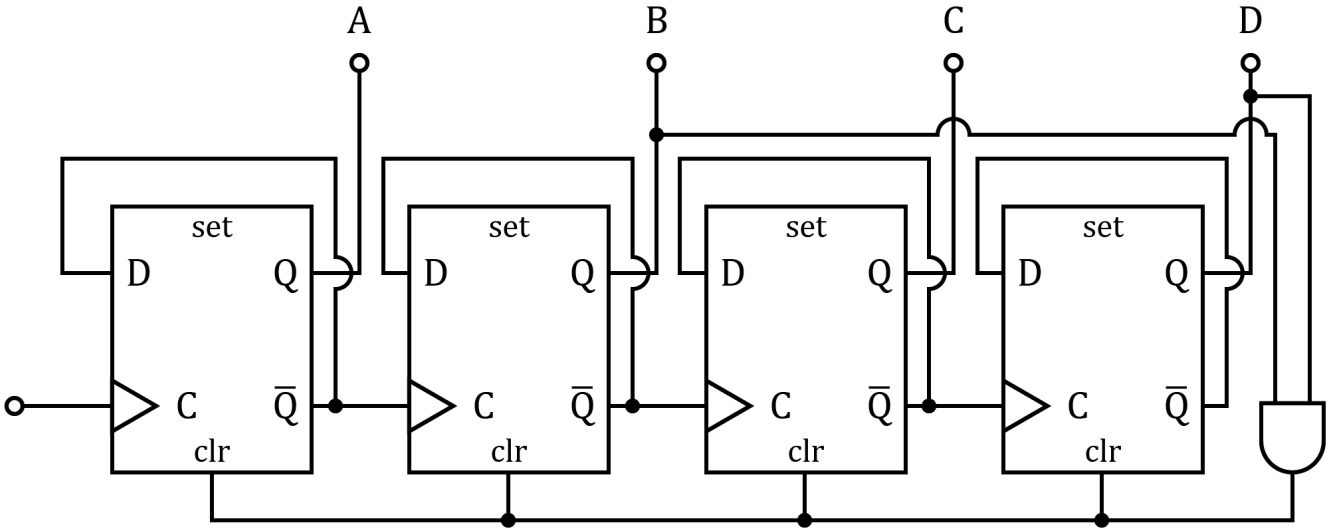
- J-K flip-flop can be used as frequency divider when both input are logically "1",
- Similar way works D-type flip-flop when to the input D is connected signal from negated output $\overline{Q}$.

Forward counter



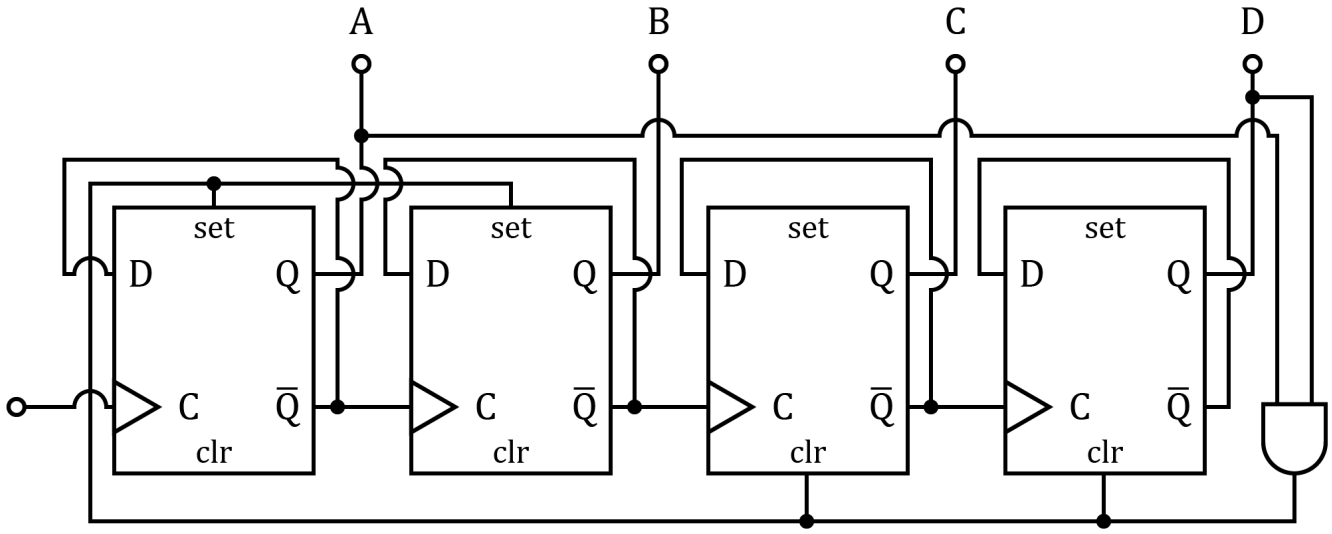
4-bits forward counter.

Modulo counter



Asynchronic counter $mod10$

Counter - setting input



Asynchronic counter realizes sequence $3-4-5-6-7-8$.

Tasks for laboratory

1. Using D-type flip-flops build 4-bit *shift register*,
2. Using *shift register* from point 1. build ring counter,
3. Using *shift register* from point 1. build Johnson counter,
4. Using D-type flip-flops build *mod*9 *counter*,
5. Using D-type flip-flops build counter from 3 to 9,
6. Using *shift register* from point 1. and XOR logic gate make PRBS *Pseudo Random Binary Signal* generator.
7. Build, in a separate circuit, the 1-bit latch using the RS flip-flops built from the NAND gates.
8. Implement the 4-bit serial shift register, in the possibility of parallel writing out and latching the state of the registry. The latch can be used from the previous point