1.4.2 The MCS6502

1.4.2.1 Product Characteristics

The MCS6502 is very similar to the MCS6501 described in detail in the previous section. It provides a full 16-pin address bus and therefore addresses a full 65,536 words in memory. It also has the same data bus, R/W and RDY available on the MCS 6501.

Figure 1.15 illustrates the pin configuration of the MCS6502.

The differences between the two devices are as follows:

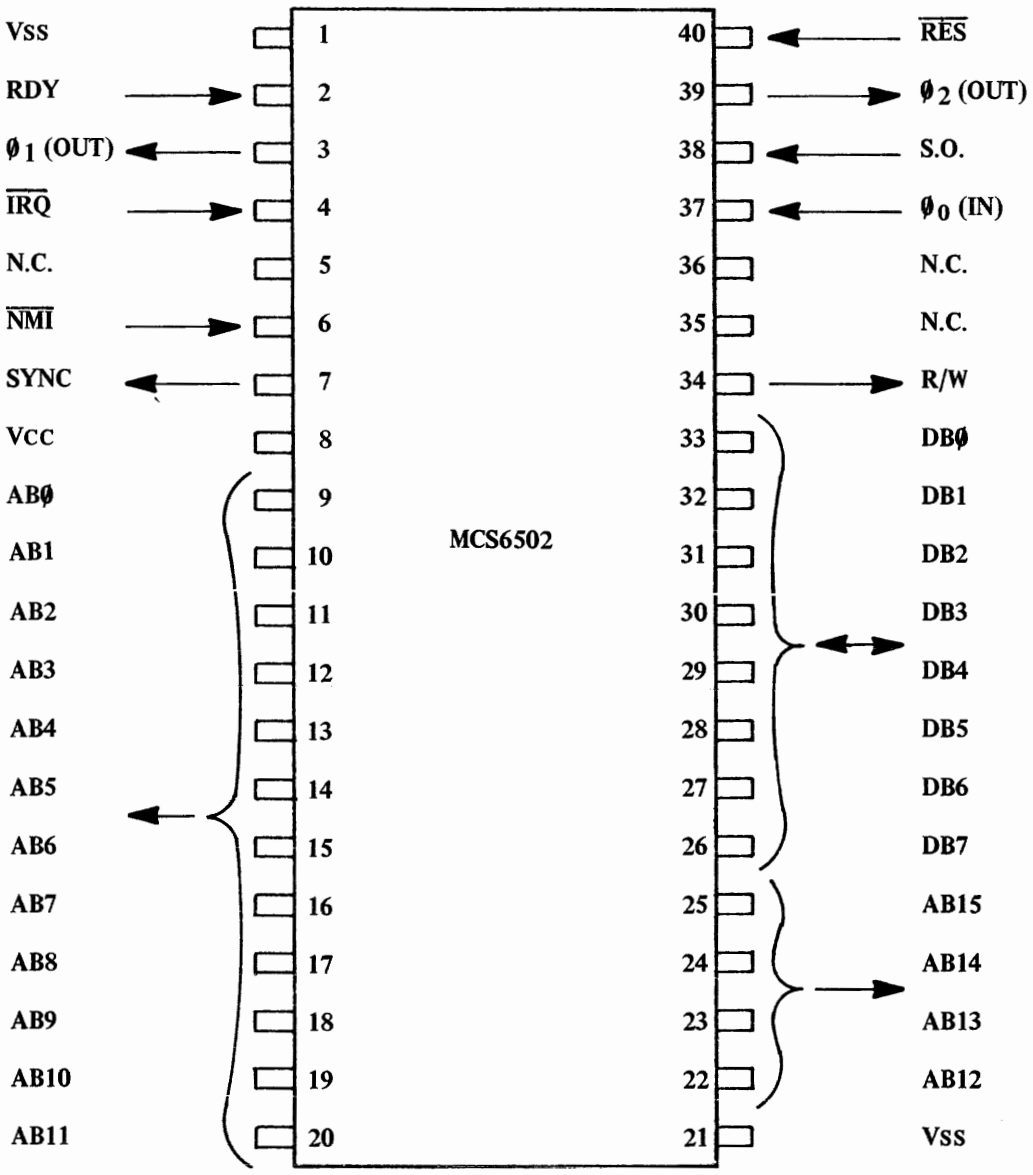
1. The MCS6502 has the oscillator and clock driver on-chip, thus eliminating the need for an external high-level two-phase clock generator.
2. The MCS6502 generates a SYNC signal instead of the bus available (BA) signal. The SYNC signal is described in detail below.
3. Pin 5, corresponding to the MC6800 VMA signal, is not connected.
4. The internal data bus enable function is connected directly to the phase two clock on the chip. Therefore pin 36 on the MCS6502 is not connected.

1.4.2.2 Device Timing--Requirements and Generation

The MCS6501, in maintaining total bus compatibility with the MC6800 product family, requires a 5-volt two-phase clock. The MCS6502, however, can be used with an externally generated time base consisting of either a TTL level single-phase clock, crystal oscillator or RC network.

Figures 1.16 and 1.17 show the configuration for setting the frequency of oscillations with a crystal or with an RC network.

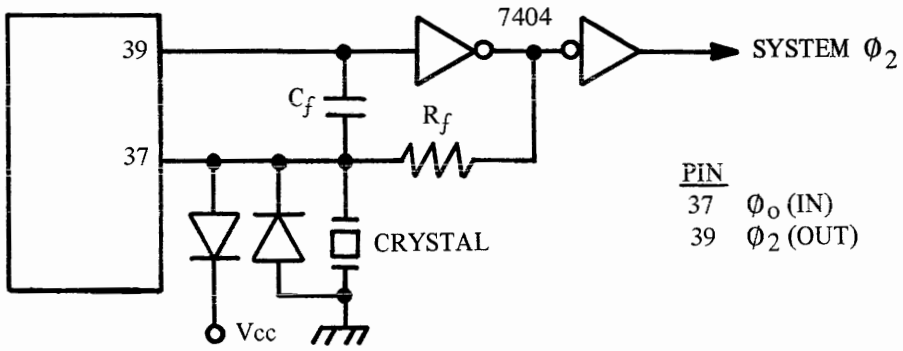
Figure 1.16 displays the crystal mode of operation in which the frequency of oscillation is set by the crystal operating in conjunction with the RC network. Figure 1.17 displays the same interconnects as in the crystal mode of time base generation, with the crystal removed from the



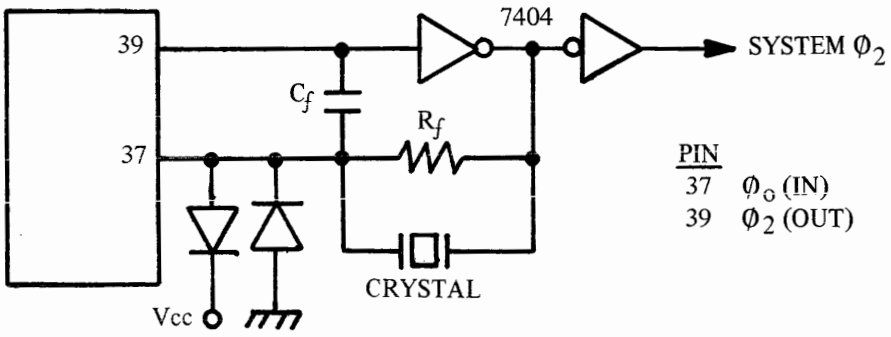
N.C. = NO CONNECTION

MCS6502 Pinout Designation

FIGURE 1.15

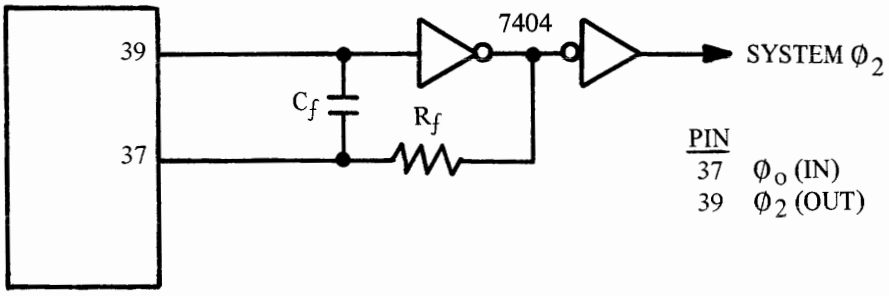


MCS6502 Parallel Mode Crystal Controlled Oscillator
FIGURE 1.16a



MCS6502 Series Mode Crystal Controlled Oscillator
FIGURE 1.16b

MCS6502 Time Base Generation - Crystal Controlled
FIGURE 1.16



MCS6502 Time Base Generator – RC Network
FIGURE 1.17

circuit. Values of the feedback resistor, R_F, and feedback capacitor, C_F, will be different for the crystal mode versus the RC mode. While the detail specifications for values of R_F and C_F are found in the data sheet for the MCS6502, clock timing can be generated by use of combinations of R_F in the range of 0 to 500K ohms and C_F in the range of 2 to 12 pf. The reader is referred to the MCS6502 data sheet for a detailed description of the application of RC networks and crystal oscillators for generation of the time base in these modes of operation.

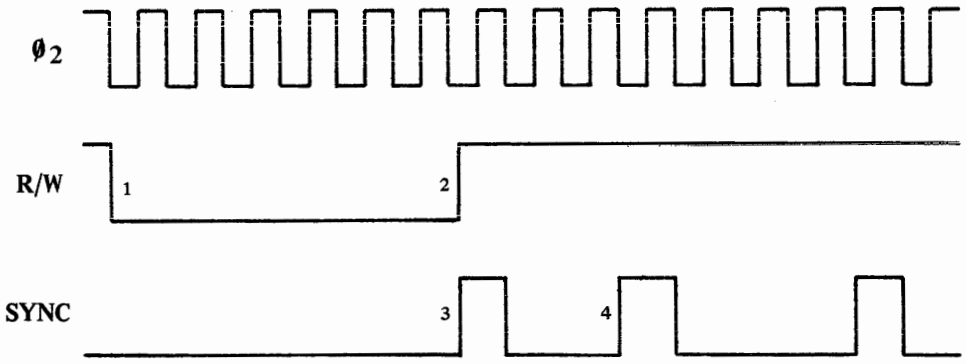
The MCS6500 bus discipline described in Section 1.3.1 is applicable wherever the oscillator is located. For data transfers to be properly carried out between the processor and the various support chips in the systems, the timing of the clocks controlling the internal processor operations must be very close to that of the phase two clock out of pin 39 of the processor with no more than two TTL delays for clock buffering. It is important in systems which drive the clock generators with a TTL square wave that this input waveform not be used to control the peripheral chips unless care is taken to assure proper timing of the phase two clock being used in these support chips.

1.4.2.3 SYNC Signal

In the MCS6502, a SYNC signal is provided to identify those cycles in which the processor is doing an OP CODE fetch. The SYNC line goes high during phase one of an OP CODE fetch and stays high for the remainder of that cycle. If the RDY line is pulled low during the phase one clock pulse in which the SYNC line went high, the processor will stop in its current state. It remains in that state until the RDY line goes high. In this manner, the SYNC signal can be used to control RDY to cause single-instruction execution. This application is discussed in detail in Chapter 2. Figure 1.18 contains a timing diagram for this signal.

1.4.2.4 S.O.--Set Overflow

This pin sets the overflow flag on a negative transition from TTL one to TTL zero. This is designed to work with a future I/O part and should not be used in normal applications unless the user has programmed for the fact the arithmetic operations also affect the overflow flag.



1. During a microprocessor write cycle, R/W signal low, the SYNC pulse does not occur.

2. The R/W signal goes high to signal the beginning of a microprocessor read cycle.

3. At the beginning of the read cycle a SYNC pulse will be be generated. This pulse will last for one cycle time. The SYNC pulse indicates that the microprocessor is reading an OP CODE from the memory field. In this case the SYNC pulse is high for one cycle as the processor reads the OP CODE.

4. The processor outputs another SYNC pulse indicating it has completed the previous instruction and is fetching another OP CODE. In this case three more cycles are needed to complete this instruction before the next SYNC pulse is generated. The SYNC pulse is aperiodic in that its generation is a function of the program and the resultant lengths of the instructions and addressing modes.

MCS6502 SYNC Signal

FIGURE 1.18