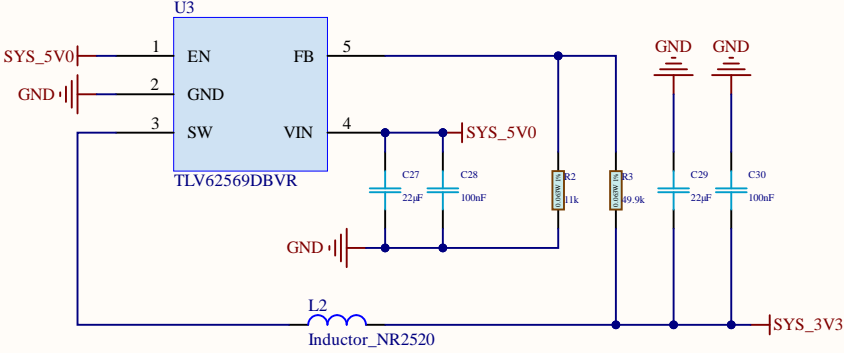
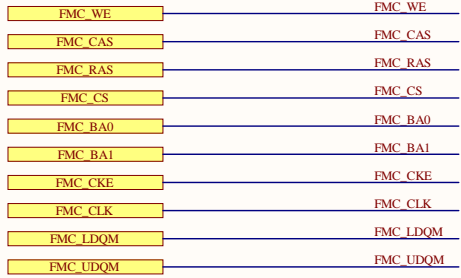
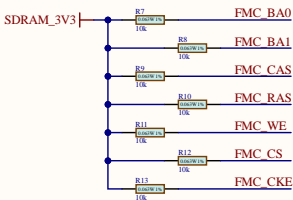
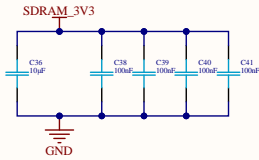
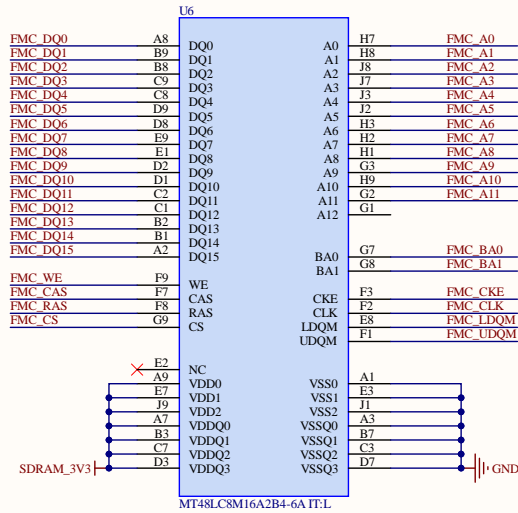


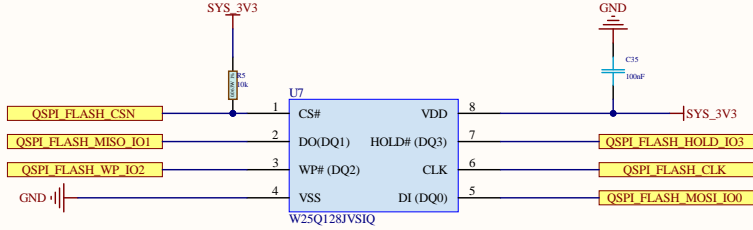
Power 3.3V



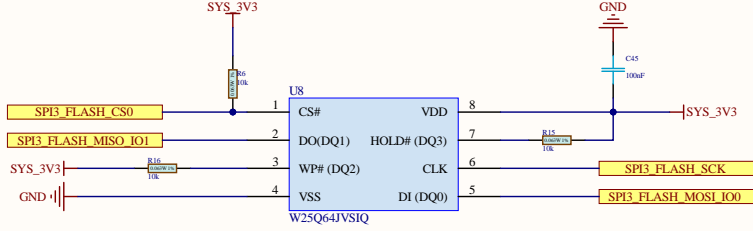
SDRAM



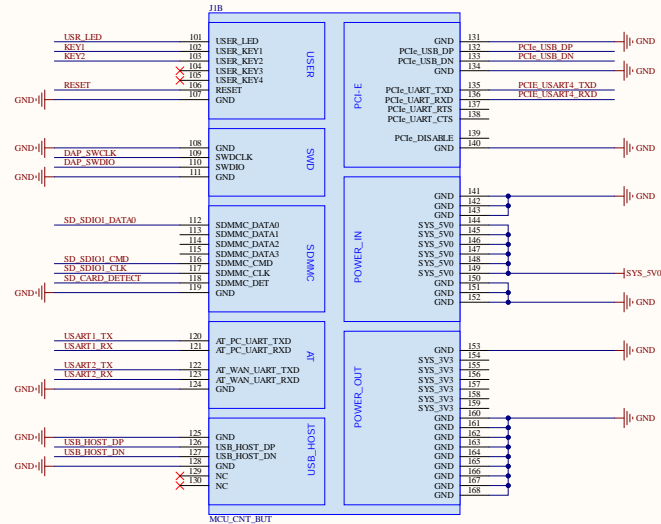
QSPI Flash



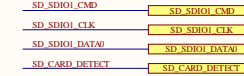
SPI Flash



Pin	STM32F405 Pin Name	STM32F405 Description	Pin	STM32F407 Pin Name	STM32F407 Description
1	VDD	VDD	51	IC1_SCL	IC1_SCL
2	VDD	VDD	52	IC1_SDA	IC1_SDA
3	VDD	VDD	53	IC1_SCL	IC1_SCL
4	VDD	VDD	54	IC1_SDA	IC1_SDA
5	VDD	VDD	55	IC1_SCL	IC1_SCL
6	VDD	VDD	56	IC1_SDA	IC1_SDA
7	VDD	VDD	57	IC1_SCL	IC1_SCL
8	VDD	VDD	58	IC1_SDA	IC1_SDA
9	VDD	VDD	59	IC1_SCL	IC1_SCL
10	VDD	VDD	60	IC1_SDA	IC1_SDA
11	VDD	VDD	61	IC1_SCL	IC1_SCL
12	VDD	VDD	62	IC1_SDA	IC1_SDA
13	VDD	VDD	63	IC1_SCL	IC1_SCL
14	VDD	VDD	64	IC1_SDA	IC1_SDA
15	VDD	VDD	65	IC1_SCL	IC1_SCL
16	VDD	VDD	66	IC1_SDA	IC1_SDA
17	VDD	VDD	67	IC1_SCL	IC1_SCL
18	VDD	VDD	68	IC1_SDA	IC1_SDA
19	VDD	VDD	69	IC1_SCL	IC1_SCL
20	VDD	VDD	70	IC1_SDA	IC1_SDA
21	VDD	VDD	71	IC1_SCL	IC1_SCL
22	VDD	VDD	72	IC1_SDA	IC1_SDA
23	VDD	VDD	73	IC1_SCL	IC1_SCL
24	VDD	VDD	74	IC1_SDA	IC1_SDA
25	VDD	VDD	75	IC1_SCL	IC1_SCL
26	VDD	VDD	76	IC1_SDA	IC1_SDA
27	VDD	VDD	77	IC1_SCL	IC1_SCL
28	VDD	VDD	78	IC1_SDA	IC1_SDA
29	VDD	VDD	79	IC1_SCL	IC1_SCL
30	VDD	VDD	80	IC1_SDA	IC1_SDA
31	VDD	VDD	81	IC1_SCL	IC1_SCL
32	VDD	VDD	82	IC1_SDA	IC1_SDA
33	VDD	VDD	83	IC1_SCL	IC1_SCL
34	VDD	VDD	84	IC1_SDA	IC1_SDA
35	VDD	VDD	85	IC1_SCL	IC1_SCL
36	VDD	VDD	86	IC1_SDA	IC1_SDA
37	VDD	VDD	87	IC1_SCL	IC1_SCL
38	VDD	VDD	88	IC1_SDA	IC1_SDA
39	VDD	VDD	89	IC1_SCL	IC1_SCL
40	VDD	VDD	90	IC1_SDA	IC1_SDA
41	VDD	VDD	91	IC1_SCL	IC1_SCL
42	VDD	VDD	92	IC1_SDA	IC1_SDA
43	VDD	VDD	93	IC1_SCL	IC1_SCL
44	VDD	VDD	94	IC1_SDA	IC1_SDA
45	VDD	VDD	95	IC1_SCL	IC1_SCL
46	VDD	VDD	96	IC1_SDA	IC1_SDA
47	VDD	VDD	97	IC1_SCL	IC1_SCL
48	VDD	VDD	98	IC1_SDA	IC1_SDA
49	VDD	VDD	99	IC1_SCL	IC1_SCL
50	VDD	VDD	100	IC1_SDA	IC1_SDA
51	VDD	VDD	101	IC1_SCL	IC1_SCL
52	VDD	VDD	102	IC1_SDA	IC1_SDA
53	VDD	VDD	103	IC1_SCL	IC1_SCL
54	VDD	VDD	104	IC1_SDA	IC1_SDA
55	VDD	VDD	105	IC1_SCL	IC1_SCL
56	VDD	VDD	106	IC1_SDA	IC1_SDA
57	VDD	VDD	107	IC1_SCL	IC1_SCL
58	VDD	VDD	108	IC1_SDA	IC1_SDA
59	VDD	VDD	109	IC1_SCL	IC1_SCL
60	VDD	VDD	110	IC1_SDA	IC1_SDA
61	VDD	VDD	111	IC1_SCL	IC1_SCL
62	VDD	VDD	112	IC1_SDA	IC1_SDA
63	VDD	VDD	113	IC1_SCL	IC1_SCL
64	VDD	VDD	114	IC1_SDA	IC1_SDA
65	VDD	VDD	115	IC1_SCL	IC1_SCL
66	VDD	VDD	116	IC1_SDA	IC1_SDA
67	VDD	VDD	117	IC1_SCL	IC1_SCL
68	VDD	VDD	118	IC1_SDA	IC1_SDA
69	VDD	VDD	119	IC1_SCL	IC1_SCL
70	VDD	VDD	120	IC1_SDA	IC1_SDA
71	VDD	VDD	121	IC1_SCL	IC1_SCL
72	VDD	VDD	122	IC1_SDA	IC1_SDA
73	VDD	VDD	123	IC1_SCL	IC1_SCL
74	VDD	VDD	124	IC1_SDA	IC1_SDA
75	VDD	VDD	125	IC1_SCL	IC1_SCL
76	VDD	VDD	126	IC1_SDA	IC1_SDA
77	VDD	VDD			

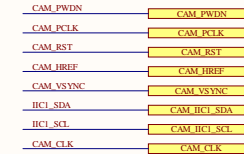
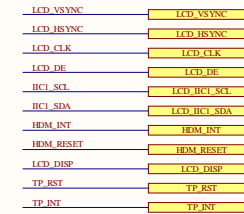


RESET	DAP_RESET
DAP_SWCLK	DAP_SWCLK
DAP_SWDIO	DAP_SWDIO



RESET	USER RESET
KEY1	KEY1
KEY2	KEY2
USR_LFD	USR_LFD

LCD DB[0..23] → LCD_DB[0..23] → LCD



SAI2_MCLKH	SAI2_MCLKB
SAI2_SCKB	SAI2_SCKB
SAI2_FSB	SAI2_FSB
SAI2_SDB	SAI2_SDB
SAI_SDA	SAI_SDA
IIC1_SDA	AUDIO_IIC1_SDA
IIC1_SCL	AUDIO_IIC1_SCL

SP1_CS	WLAN_SP1_CS3
SP3_MISO	WLAN_SP1_MISO
SP3_SCK	WLAN_SP1_SCK
SP3_MOSI	WLAN_SP1_MOSI
WLAN_GPIO	WLAN_GPIO
USART2_RX	USART2_RX
USART2_TX	USART2_TX
USART1_RX	USART1_RX
USART1_TX	USART1_TX
RESET	WLAN_RESET

RESET	PCIE_RESET
PCIE_USART4_TXD	PCIE_USART4_TXD
PCIE_USART4_RXD	PCIE_USART4_RXD

The diagram shows two signal lines, USB_HOST_DP and USB_HOST_DN, each connected to a corresponding pin on a component. The connections are as follows:

Signal Name	Pin Name
USB_HOST_DP	USB_HOST_DP
USB_HOST_DN	USB_HOST_DN

SP11_CS2	ES3_SP11_CS2
SP13_SCK	ES3_SP11_SCK
SP13_MOSI	ES3_SP11_MOSI
SP13_MISO	ES3_SP11_MISO
ES3_GP0D1	ES3_GP0D1
ES3_GP0D2	ES3_GP0D2
ES3_GP0D3	ES3_GP0D3
ES3_GP0D4	ES3_GP0D4
ES3_GP0D5	ES3_GP0D5
ES3_UARTS_RX	ES3_UARTS_RX
ES3_UARTS_TX	ES3_UARTS_TX
HC1_SCL	ES3_HC1_SCL
HC1_SDA	ES3_HC1_SDA
ES3_ADC1_INP4	ES3_ADC1_INP4
PWM2_A3	ES3_DACL_OUT3