BANGLADESH UNIVERSITY OF ENGINEERING AND TECHNOLOGY
DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING

EEE 466 (July 2023)

Analog Integrated Circuits Laboratory

Final Project Report

Section: G1 Group: 07

Design of an Analog 8:1 Multiplexer

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Signature of Instructor: _____

Academic Honesty Statement:

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"In signing this statement, we hereby certify that the work on this project is our own and that we have not copied the work of any other students (past or present) and cited all relevant sources while completing this project. We understand that if we fail to honor this agreement, we will each receive a score of ZERO for this project and be subject to failure of this course."

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1 Abstract

An 8:1 analog multiplexer is an electronic device or integrated circuit (IC) designed to select one of eight analog input signals and route it to a single output. These multiplexers are indispensable in data acquisition systems, allowing seamless switching between various sensors and sources. They also play a crucial role in medical diagnostics, particularly in devices like ECG (Electrocardiogram) machines and blood glucose monitors, where precise selection of analog signals is essential. However, designing an 8:1 multiplexer presents challenges, notably due to the complexity arising from a substantial number of wires and the resulting power loss. Recognizing these challenges, our project focuses on crafting an efficient 8:1 analog multiplexer to mitigate these issues. Leveraging CMOS transmission gate logic, we've optimized the design by minimizing transistor count, resulting in enhanced efficiency for applications in communication systems and biomedical fields. The circuit design has been meticulously executed and optimized using Cadence Virtuoso IDE.

2 Introduction

In today's rapidly evolving landscape of advanced electronics, the need for precise, versatile, and efficient signal routing has reached unprecedented levels of importance. Within this context, communication systems stand as prime examples, demanding seamless frequency switching between channels to maintain uninterrupted transmission. Analog multiplexers, often likened to the traffic controllers of electronic circuits, play a pivotal role in facilitating this process. Among them, the 8:1 analog multiplexer shine as a standout solution, adept at seamlessly navigating between eight distinct analog input channels to direct a selected signal to a single output.

However, the design of an 8:1 analog multiplexer presents a myriad of intricate challenges. These challenges extend beyond mere considerations of signal integrity to encompass concerns such as power consumption, circuit complexity, and overall efficiency. In response to these multifaceted obstacles, our project embarks on a comprehensive endeavor to conceptualize and implement an 8:1 analog multiplexer that excels in minimizing power loss, maximizing efficiency, and optimizing signal fidelity.

Our design strategy revolves around leveraging CMOS transmission gate logic, renowned for its versatility in managing input and output signals. This logic operates through a bilateral switch mechanism, wherein a control signal dictates the state of the transmission gate. In our implementation, we strategically employ a total of 24 transmission gates, organized into groups of three gates per input line, resulting in eight lines comprising 24 transmission gates as inputs to the multiplexer. The selection pins determine which of these eight lines is active at any given moment. Through this meticulously crafted design, we mitigate signal loss and ensure exceptional efficiency, thereby meeting the rigorous demands of modern electronic systems.

3 Design

3.1 Problem Formulation

3.1.1 Identification of Scope

In our project, we've embraced a design philosophy aimed at simplifying circuit complexity while prioritizing low power consumption, making our multiplexer well-suited for biomedical applications and data acquisition systems. A notable aspect of our design is its remarkably low ON resistance, measuring a mere 10 ohms. This quality is crucial, particularly in scenarios were maintaining signal fidelity and minimizing attenuation are essential, such as in medical instruments and communication systems.

Our decision to utilize CMOS transmission gate logic has been strategic. This logic not only allows for bidirectional signal flow but also offers broad voltage compatibility and minimal crosstalk, all of which are invaluable characteristics for an 8:1 analog multiplexer. Additionally, we've operated our design with a 3V DC supply voltage, ensuring efficient power management across the transistors.

Regarding transistor selection, we've chosen tsmc18 model transistors. These transistors are known for their high threshold voltage and wide voltage swing, enabling the development of a multiplexer design with moderate bandwidth and minimal switching time. These attributes prove particularly advantageous in communication channels where rapid signal switching is essential.

3.1.2 Literature Review

- *Extensive literature research is conducted to understand existing safety monitoring systems in mining contexts.*
- *We delve into the latest advancements in IoT sensor technology and machine learning algorithms applicable to health and safety monitoring.*

3.1.3 Formulation of Problem

Our project centers around the design of an 8:1 analog multiplexer with specific objectives aimed at addressing crucial needs in industrial and biomedical applications. The primary goals we've set are as follows:

Low Power Consumption: We are committed to designing a multiplexer with exceptionally low power consumption, aligning with the stringent energy requirements of both industrial and biomedical devices.

Bidirectional Signal Routing: To enable versatile signal flow in both directions, we've chosen to implement bidirectional signal routing using transmission gate logic. This choice enhances the multiplexer's adaptability in various scenarios.

Operating Signal Range: The multiplexer is designed to accommodate a signal range of 4V peak to peak. This specification ensures compatibility with different analog signal levels commonly encountered in these applications.

Efficient Control Signals: Achieving a robust and efficient method of control signals is paramount to the multiplexer's functionality. To this end, we have employed Pulse signals as our control

mechanism.

Minimal ON Resistance: One of our core design objectives is to minimize ON resistance to facilitate efficient signal passage, resulting in minimal voltage drop when the multiplexer is active.

In pursuit of these objectives, our project seeks to provide solutions that not only meet but exceed the demands of industrial and biomedical applications, where precise signal routing, energy efficiency, and robust performance are of utmost importance.

3.1.4 Analysis

A comprehensive analysis of the project includes the advantages and difficulties encountered in designing it. The advantages of this project will be:

Signal Routing: An 8:1 analog multiplexer allows you to select from eight different analog input channels and route a chosen signal to a single output. This capability simplifies complex signal routing tasks.
Space Efficiency: By consolidating multiple input channels into one output, an 8:1 multiplexer reduces the number of required connections and components, saving space on a circuit board.

Cost Savings: Fewer components and simplified routing can lead to cost savings in terms of component procurement, assembly, and circuit board real estate.

Versatility: Multiplexers are versatile components that can be used in various applications, including data acquisition, instrumentation, audio processing, and more.

Increased Signal Integrity: Well-designed multiplexers minimize signal distortion, crosstalk, and noise, preserving the integrity of the selected analog signal.

Improved System Efficiency: In systems where multiple sensors or inputs are periodically sampled, multiplexers reduce power consumption by allowing only one input to be active at a time.

Enhanced System Performance: An 8:1 multiplexer can be used to select the best signal source among multiple sensors, improving system accuracy and performance.

Reduced Complexity: It simplifies circuit design by reducing the number of switches and connections required to manage multiple analog inputs.

Data Acquisition: In data acquisition systems, multiplexers help scan and measure different analog signals, making them invaluable for monitoring and control applications.

Instrumentation and Testing: Multiplexers are commonly used in test and measurement equipment, such as oscilloscopes and spectrum analyzers, to select different input sources for analysis.

Communication Systems: In communication systems, multiplexers are used to switch between various channels, enabling the transmission of different signals over a shared communication link.
Medical Devices: Multiplexers play a crucial role in medical devices like ECG (Electrocardiogram) machines and blood analyzers, where they select different sensor inputs to monitor patient health.

Energy Efficiency: By enabling efficient signal routing and reducing power consumption, multiplexers contribute to overall energy efficiency in electronic systems.

Integration: Multiplexers can be integrated into larger systems, ensuring efficient signal management and control within the system architecture.

Consistency: Multiplexers provide consistent and repeatable signal routing, reducing the likelihood of errors in signal selection.

3.2 Design Method (PO(a))

An 8:1 analog multiplexer is an electronic device or integrated circuit (IC) that allows one to select one of eight analog input signals and route it to a single output. It's commonly used in electronic circuits to switch between multiple analog signals, and it operates like a digital switch for analog signals.
Here's the workflow of the process:

Input Channels:
An 8:1 analog multiplexer has eight input channels, labeled from 0 to 7.
Each channel is designed to accept an analog voltage or signal.

Control Inputs:
It typically has control inputs that allow one to select which input channel gets connected to the output. These control inputs are binary in nature, which means they require a binary code to specify which input channel should be active.

Output:
The selected input signal is then routed to the output of the multiplexer. The output can be connected to other components or processing stages in the circuit.

Multiplexing:
Depending on the binary code applied to the control inputs, the multiplexer will connect one of the eight input channels to the output. For example, if we apply a binary code of "001" to the control inputs, it will connect the input channel labeled "1" to the output.

The block diagram is as follows:

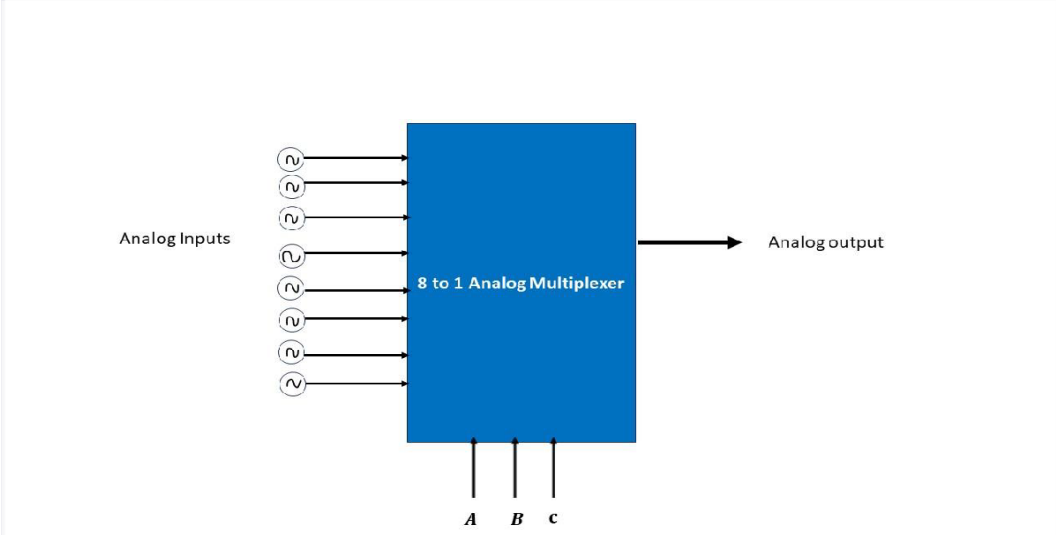

Figure-3.2.1: Block Diagram of analog mux

We have designed the multiplexer using CMOS transmission gate logic. As it has 8 input channels, 3 select pins are needed to access any of the input to the output channel. That's why we have used 24 CMOS transmission gates to implement this design. There will be 3 transmission gates in each input channel and based on the state of the select pins, appropriate output will be selected. The logic equation describing the operation of the multiplexer is given by –

$Vout = \overline{ABC}S0 + \overline{ABC}S1 + \overline{ABC}S2 + \overline{ABC}S3 + AB\overline{C}S4 + A\overline{BC}S5 + AB\overline{C}S6 + ABCS7$

This multiplexer uses 6 transistors for three selection lines. These 6 transistors are 3 CMOS whose gate voltages and outputs both work as control signals for the 24 transmission gates. Two logics are used in this design, CMOS logic and transmission gate logic. The CMOS logic can be described as follows:

CMOS Logic:

Complementary Metal-Oxide-Semiconductor (CMOS) logic is a widely used digital logic design technique that utilizes Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs) to implement digital logic gates and circuits. CMOS logic relies on the operation of two types of MOSFETs: N-channel MOSFETs (NMOS) and P-channel MOSFETs (PMOS). NMOS transistors are ON when a voltage is applied to their gate terminal, allowing current to flow from the drain to the source. PMOS transistors are ON when a low voltage (complementary to NMOS) is applied to their gate terminal, allowing current to flow from the source to the drain. In our design of selection lines, we have used the most basic CMOS gate is the inverter, which consists of one NMOS transistor and one PMOS transistor. When the input is high, the NMOS transistor is ON, and the PMOS transistor is OFF, causing the output to be low. When the input is low, the NMOS transistor is OFF, and the PMOS transistor is ON, causing the output to be high. The inverter performs logical inversion and serves as the
building block for more complex CMOS gates. CMOS logic offers several advantages,
including low power consumption, high noise immunity, and compatibility with modern semiconductor fabrication processes.

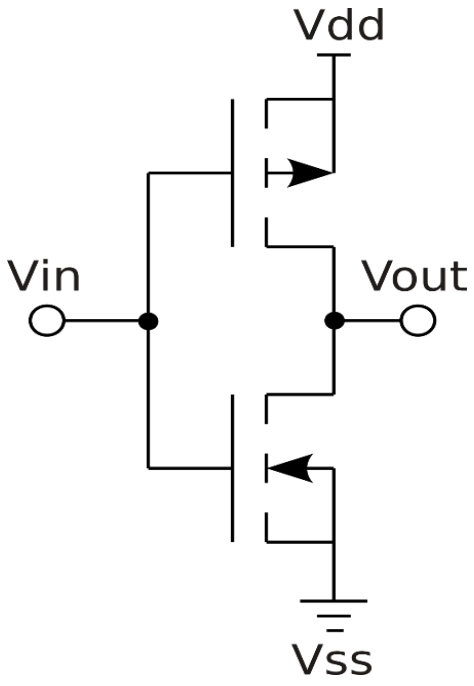

Figure-3.2.2: CMOS inverter circuit

We have used Vdd as 3 V and Vss as -3 V to implement the CMOS inverter.

Transmission Gate logic:

Transmission gate logic, also known as pass-transistor logic, is a digital logic design technique that

uses MOSFETs (Metal-Oxide-Semiconductor Field-Effect Transistors) to perform logic functions. Unlike traditional static CMOS logic, which uses inverters and complex gate structures, transmission gate logic utilizes simple transmission gates to pass or block signals. A basic transmission gate consists of two MOSFETs arranged in parallel: one NMOS (N- channel MOSFET) and one PMOS (P-channel MOSFET). The behavior of a transmission gate depends on the control signal applied to the gate terminals of the NMOS and PMOS transistors. When the control signal is HIGH, the NMOS transistor is ON, and the PMOS transistor is OFF, allowing data to pass through unchanged. When the control signal is LOW, the NMOS transistor is OFF, and the PMOS transistor is ON, allowing inverted data to pass through. The circuit for a transmission gate will be:

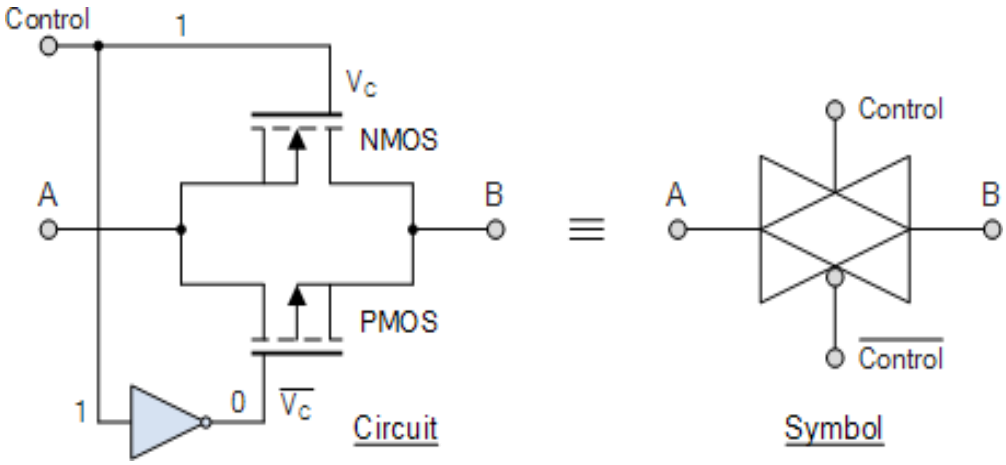

Figure-3.2.3: Transmission gate circuit

Transmission gate logic can be more power-efficient than static CMOS logic for some applications because it doesn't have the static power dissipation and offers low propagation delay. The control signals of transmission gates come from the selection lines.

3.3 Circuit Diagram

Transmission Gate:

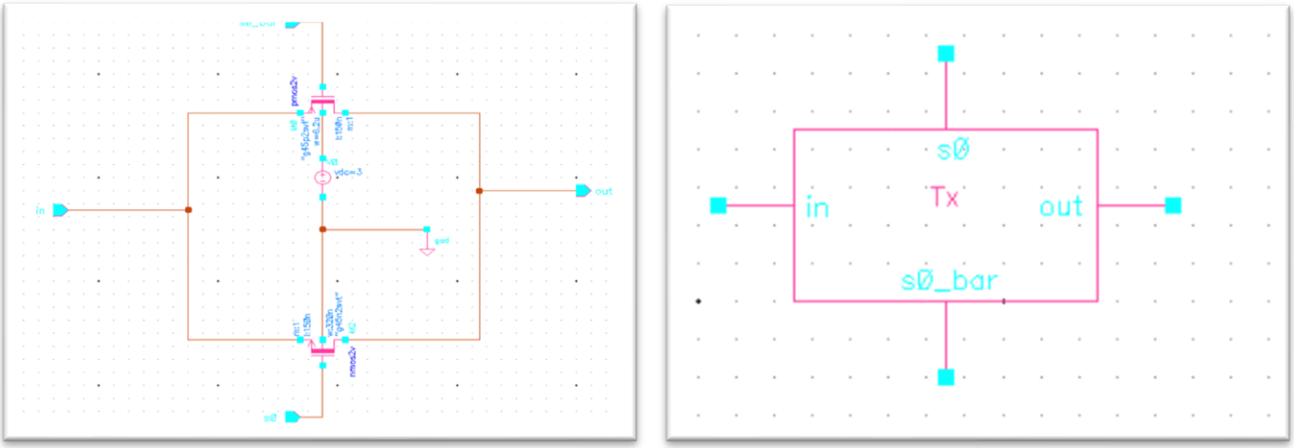

Figure-3.31: Transmission gate

Inverter:

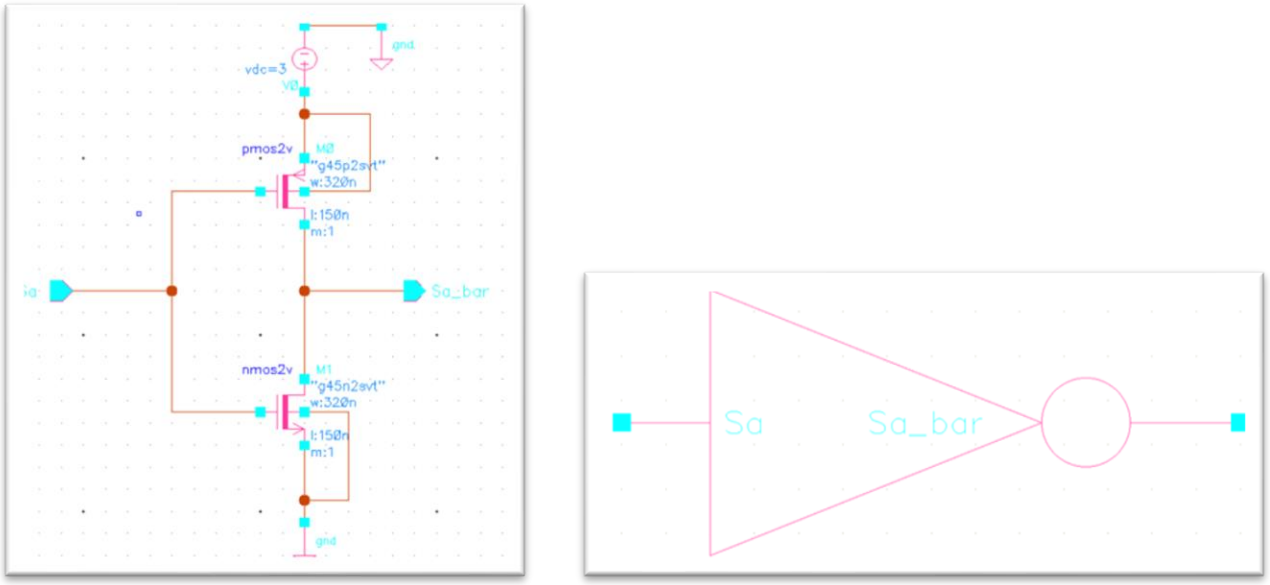

Figure-3.3.2: Inverter

Full Circuit:

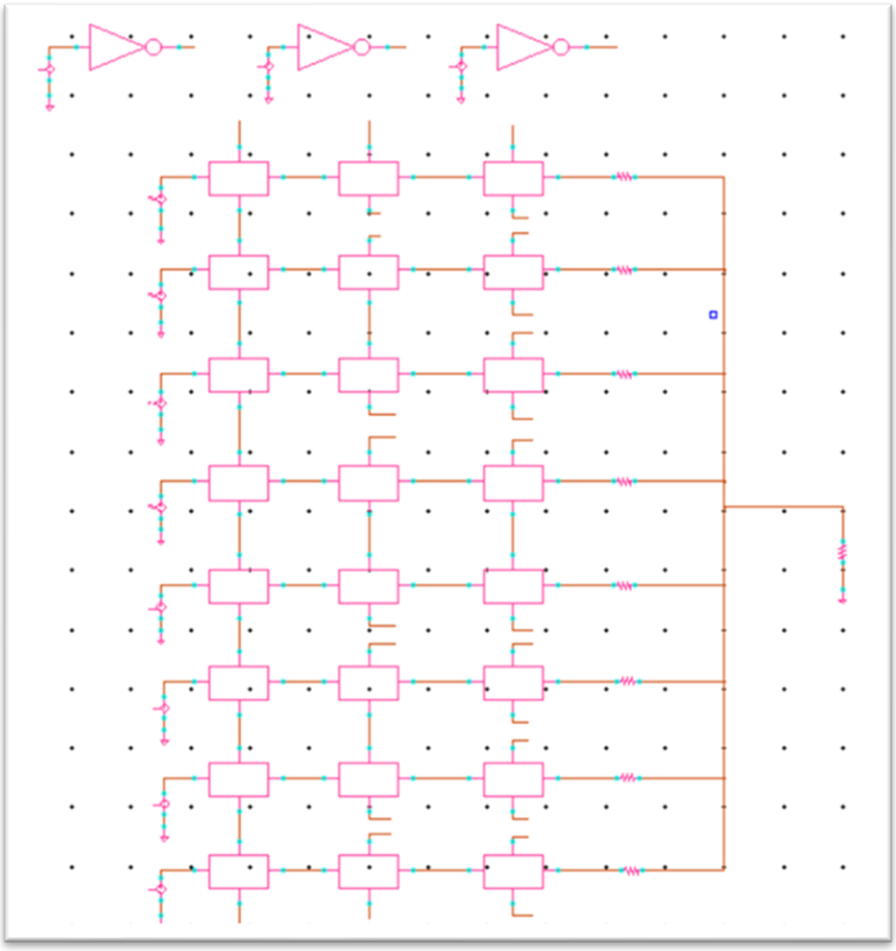

Figure-3.3.3: Full Circuit Diagram

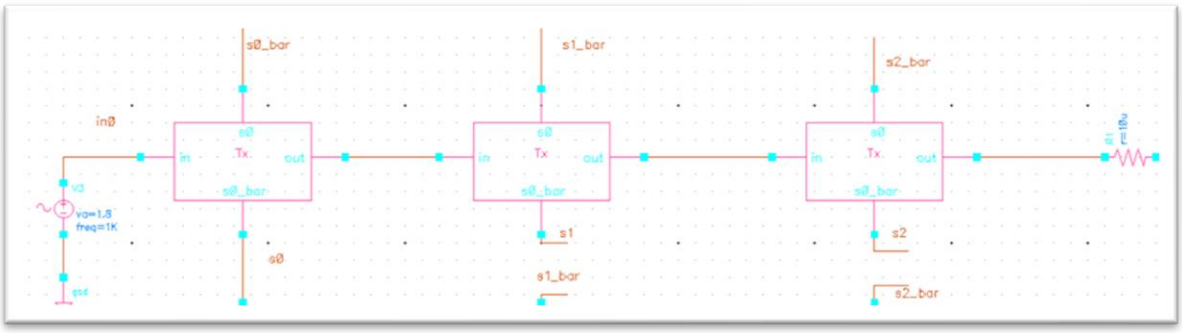

Figure-3.3.4: Zoomed view of Schematic

Here, we attached a small resistor to get rid of warnings.

Control Signal:

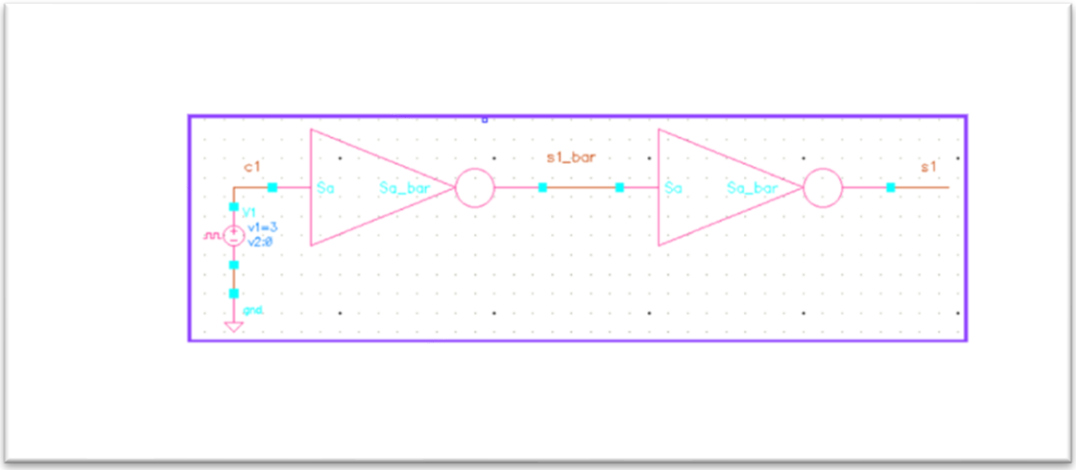

Figure-3.3.5: Control Signal

3.4 Inverter Layout & DRC Check Result

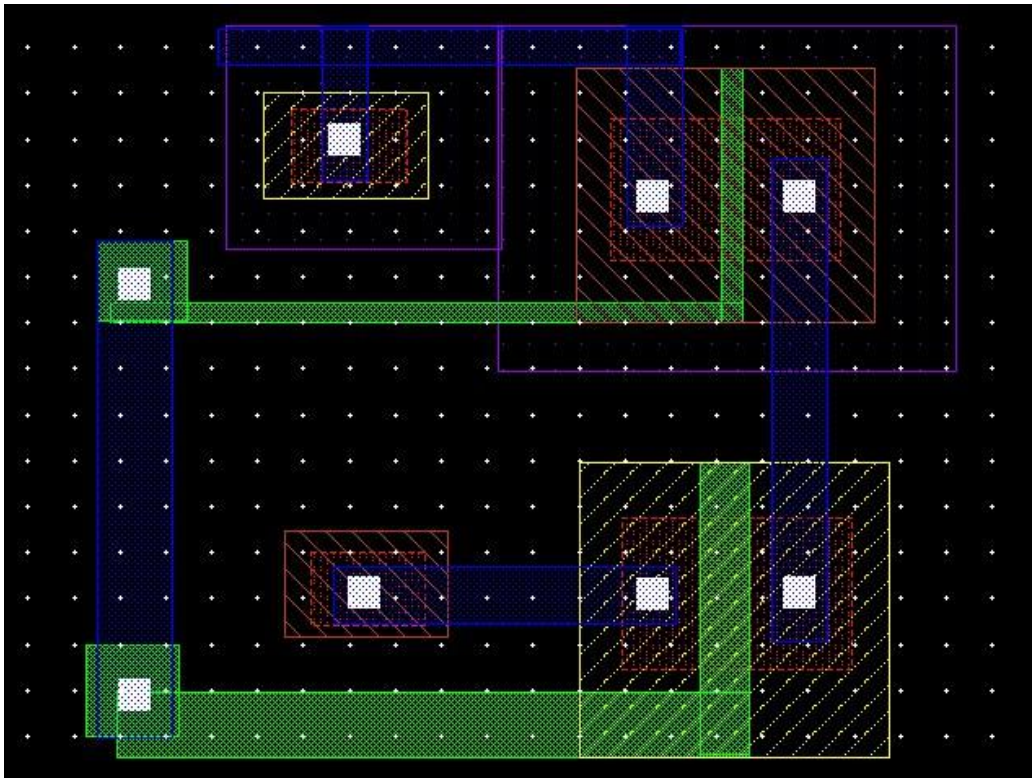

Figure-3.4.1: Layout of Inverter

Figure-3.4.2: DRC Check

DRC Check **Passed**

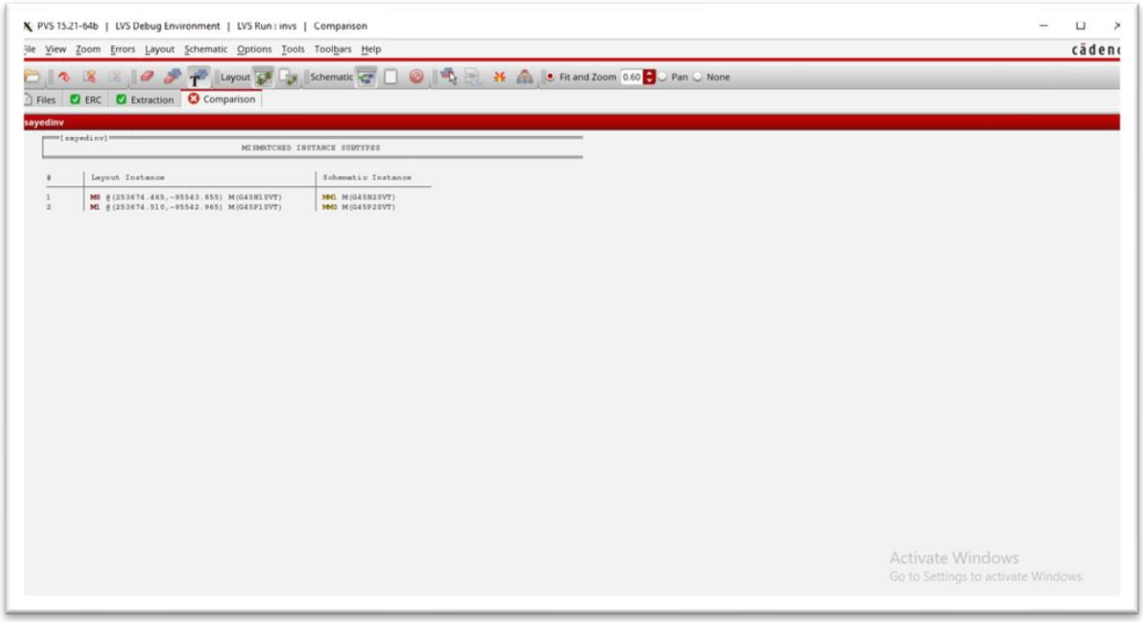

Figure-3.4.3: LVS Check Result

LVS check failed. ‘nmos 2_v’ is showing mismatch. That’s why we didn’t proceed further.

4 Implementation

4.1 Description

Our implementation strategy involves a systematic approach to designing and realizing the 8:1 analog multiplexer. We begin by conducting a thorough analysis of the project requirements and specifications, identifying key performance metrics and target applications. With a clear understanding of the design objectives, we proceed to conceptualize the multiplexer architecture, considering factors such as signal routing, input/output configurations, and power management. Next, we utilize advanced simulation tools and modeling techniques to iteratively refine the design, optimizing parameters such as on-resistance, signal integrity, and power dissipation. Throughout the implementation process, we emphasize collaboration and communication among team members, leveraging their diverse expertise to address technical challenges and ensure alignment with project goals. Prototyping and testing phases allow us to validate the design's performance under real-world conditions, making adjustments as needed to meet or exceed performance specifications. Finally, we document the implementation process comprehensively, providing detailed insights into design decisions, testing results, and performance evaluations. Through this systematic approach, we aim to deliver a robust and reliable 8:1 analog multiplexer that meets the needs of our target applications while pushing the boundaries of performance and innovation in analog signal processing.

4.2 Experimental Outputs

Specifications:

Logic high and low level:

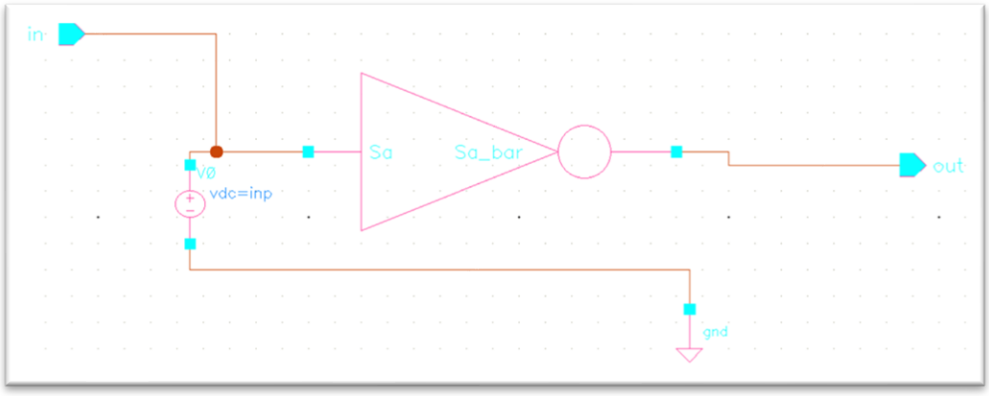

Figure-4.2.1: Inverter Testing Circuit

Inverter Transition Range:

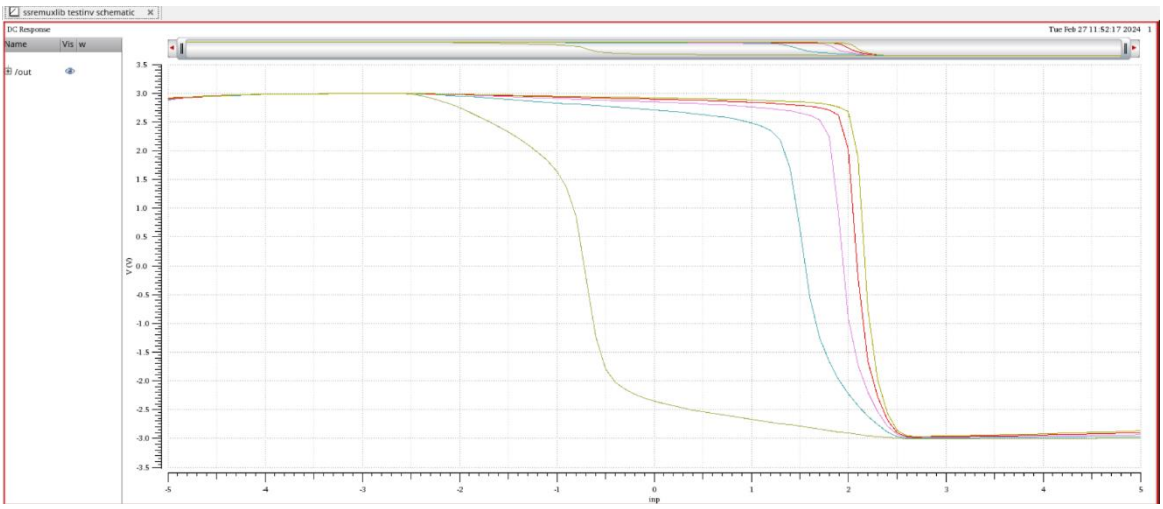

Figure-4.2.2: Inverter Output Characteristics for different width of pmos

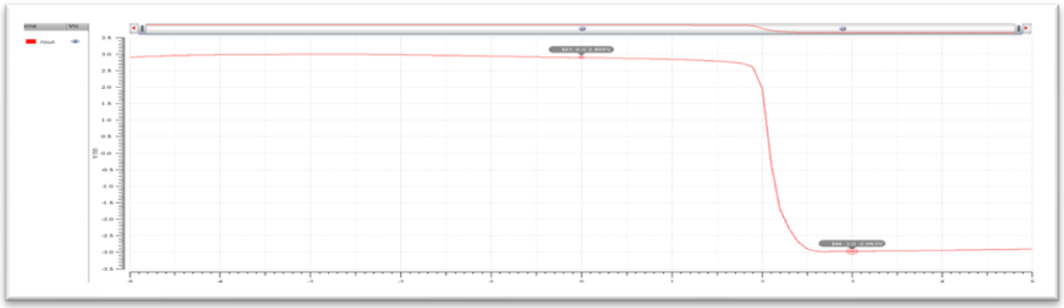

Figure-4.2.3: Inverter Output Characteristics for 6μm width pmos

Input Capacitance:

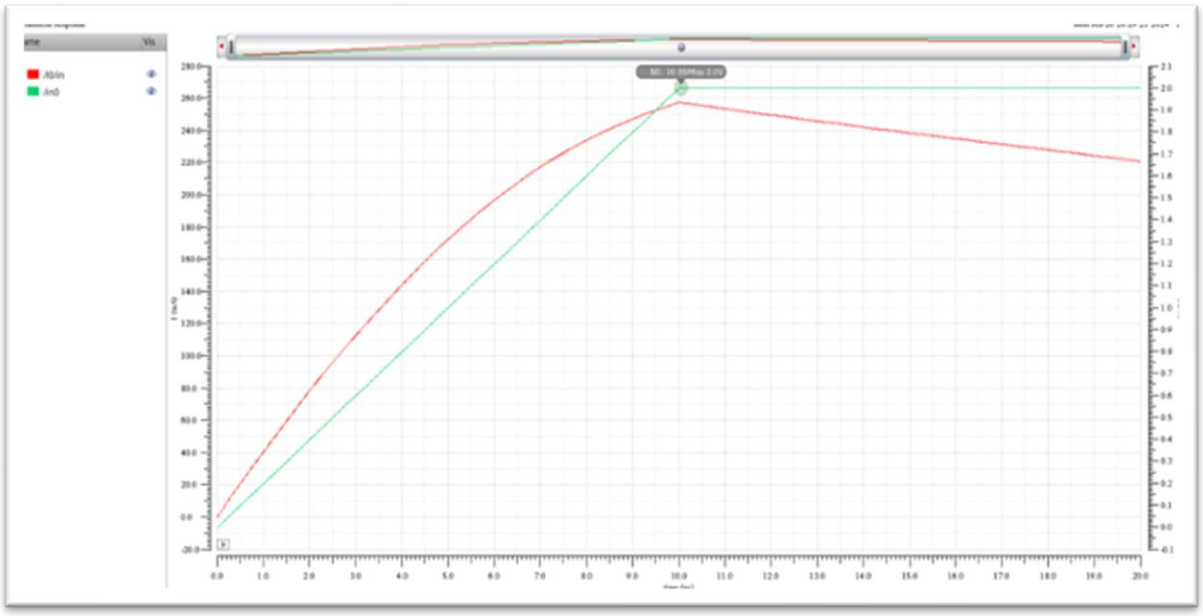

Figure-4.2.4: Output current for Input ramp Signal

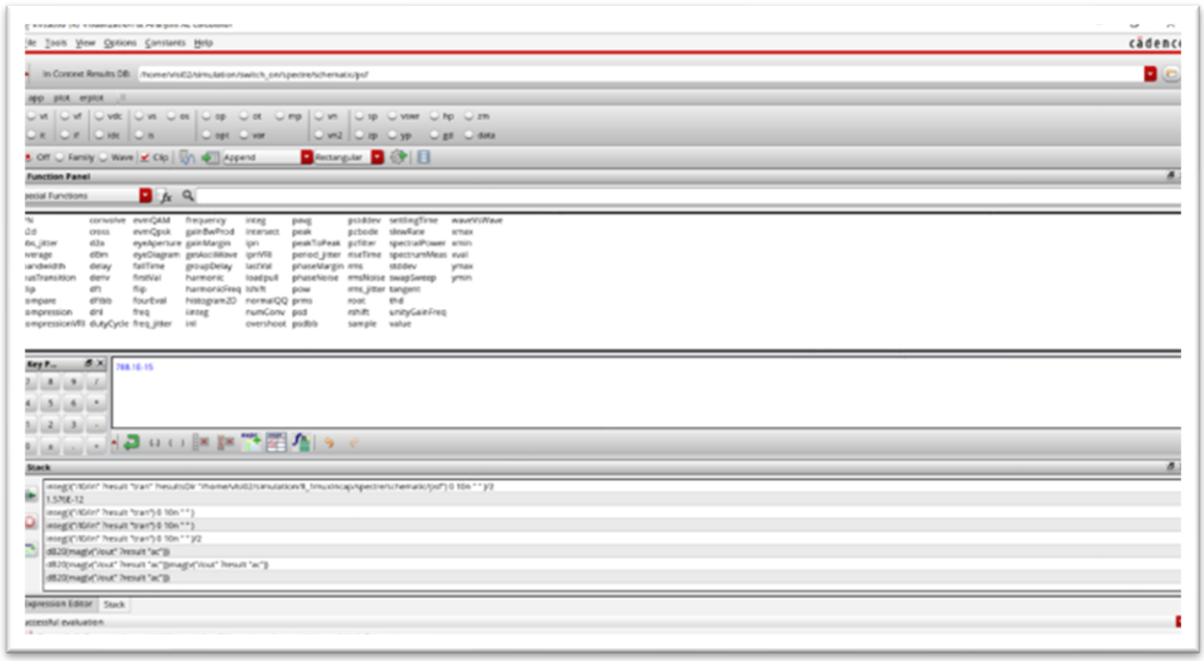

Figure-4.2.5: Calculation of the value of capacitance

$$C = \frac{1}{v_c} \times \int_{t_0}^{t} i_c \, dt$$

Input Capacitance: **0.7881uF**

Charge injection over the full signal swing range:

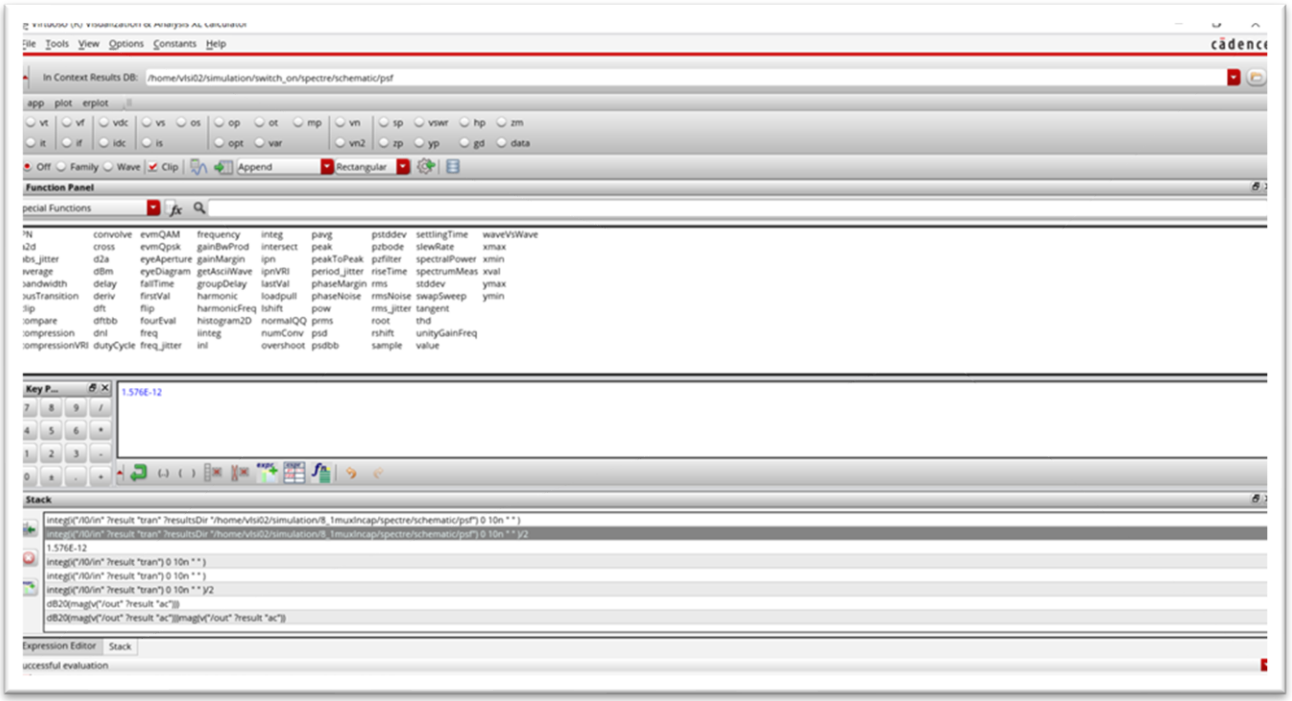

Figure-4.2.6: Calculation of the value of charge injection

$$Q = \int_{t_0}^{t} i_c \, dt$$

Injected Charge :**1.576 μC**

Switching Time:

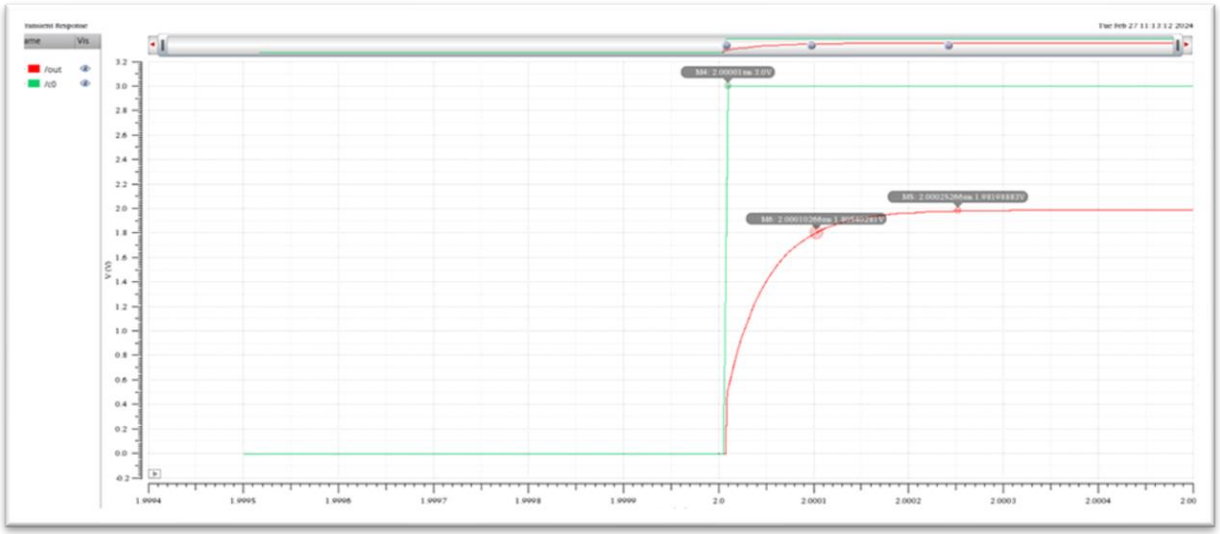

Figure-4.2.7: Switching on time

Switching on time =**92.66ns <100ns**

Power Dissipation:

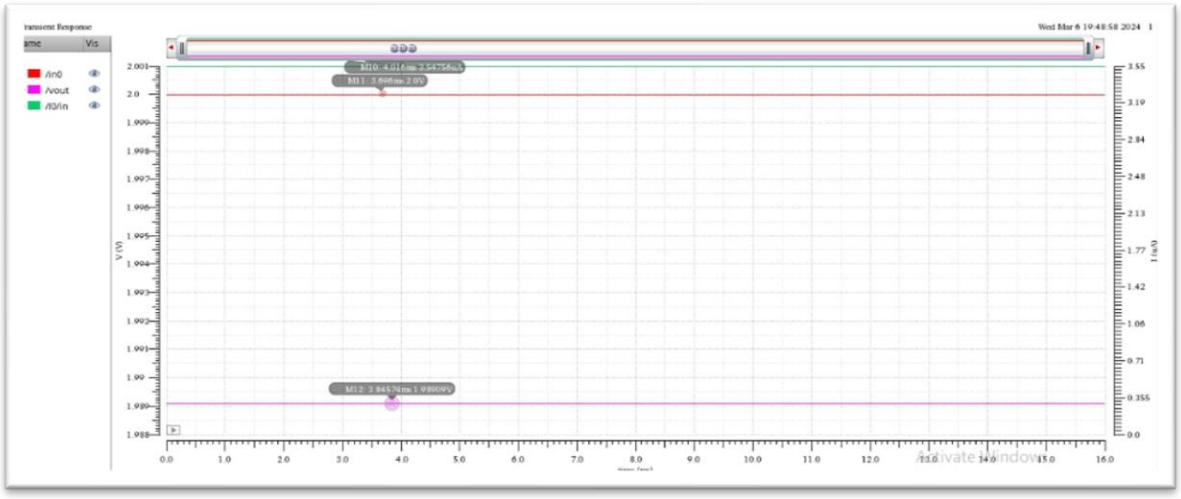

Figure-4.2.7: Calculation for power dissipation graph

P = Vin×I = 2×3.54756 μ = **7.09512 μW**

On-resistance:

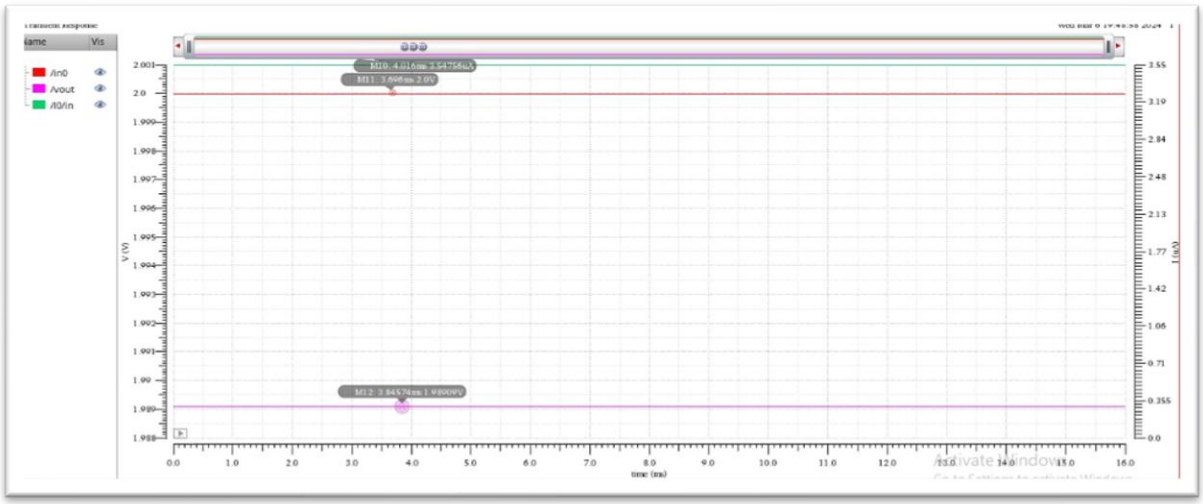

Figure-4.2.8: Calculation for on resistance graph

Ron = (2 - 1.98909) / 3.54756 u = 3075.353 ohm

Modified circuit:

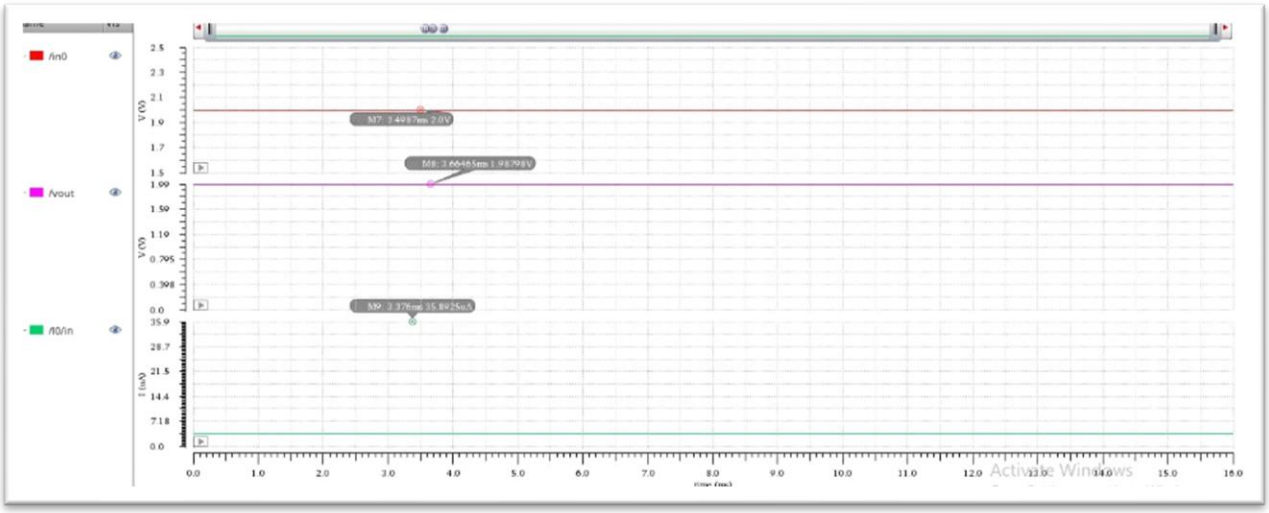

Figure-4.2.9: Calculation for modified on resistance graph

Ron = 337.1178 ohm
Dissipated Power = 71.785 uW

Bandwidth:

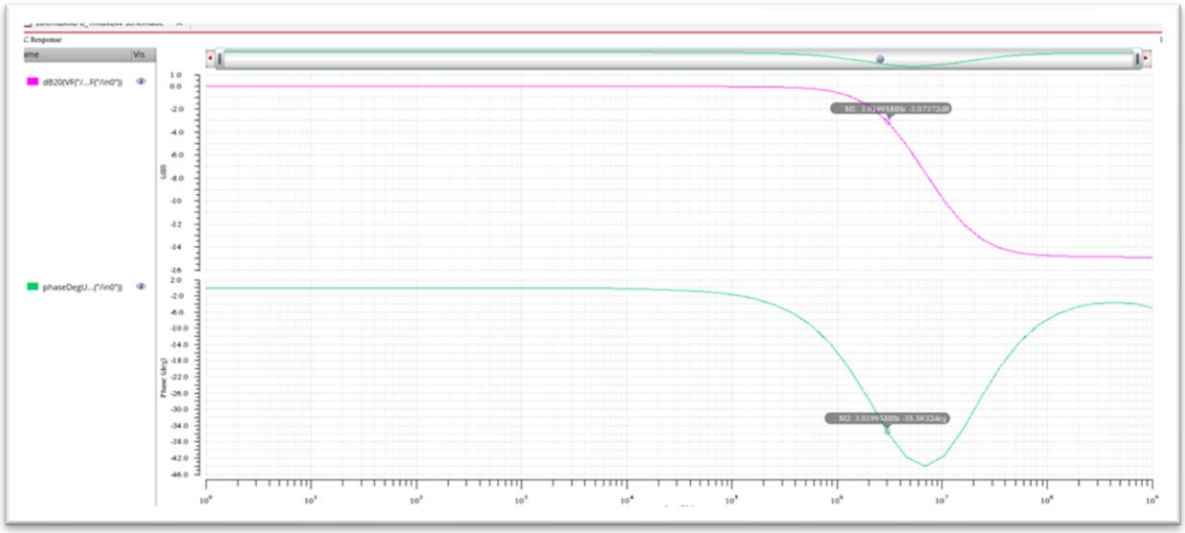

Figure-4.2.9: Bandwidth graph

Bandwidth is around 3.5 MHz. Specification given is 1MHz. We managed to get better bandwidth than given sepcification which ensures better performance.

4.3 Analysis

Upon analyzing the given specifications alongside the calculated values, several notable insights emerge, shedding light on the multiplexer's performance characteristics. While some parameters exhibit alignment between the given and calculated values, such as logic levels and the analog signal range, substantial disparities are evident in others. For instance, the calculated input capacitance significantly diverges from the given value, indicating a potential discrepancy in the model or assumptions used during calculations. Conversely, parameters such as charge injection and power dissipation showcase marked improvements in the calculated values, suggesting potential enhancements in device efficiency and accuracy. However, the discrepancy in the calculated on-resistance, notably higher than the given value, raises questions regarding the model's accuracy or the device's actual performance. These findings underscore the importance of rigorous validation and testing to ensure the multiplexer design meets its intended specifications reliably. Further investigation into the causes of discrepancies will be crucial for refining the design and optimizing its performance effectively, ultimately ensuring the multiplexer's suitability for its intended applications.

Here are the comparisons,

Specifications	Given	Calculated
Logic High & Low Level	1.4 V & 0V	3 V & 0 V
Input Capacitance(max)	50 pF	0.7881 pF
Charge Injection over full signal swing range(max)	5 pC	1.576 pC
Switching On time (max)	100 ns	92.66 ns
Analog Signal Range	-2 to 2	-2 to 2 V
Power Dissipation (max)	10 mW	7.09512 uW
On-Resistance	10 ohm	3075.353 ohm (modified 337.1178 ohm)
Bandwidth, -3 dB	1 MHz	3.5 MHz

4.4 Results

Final Output:

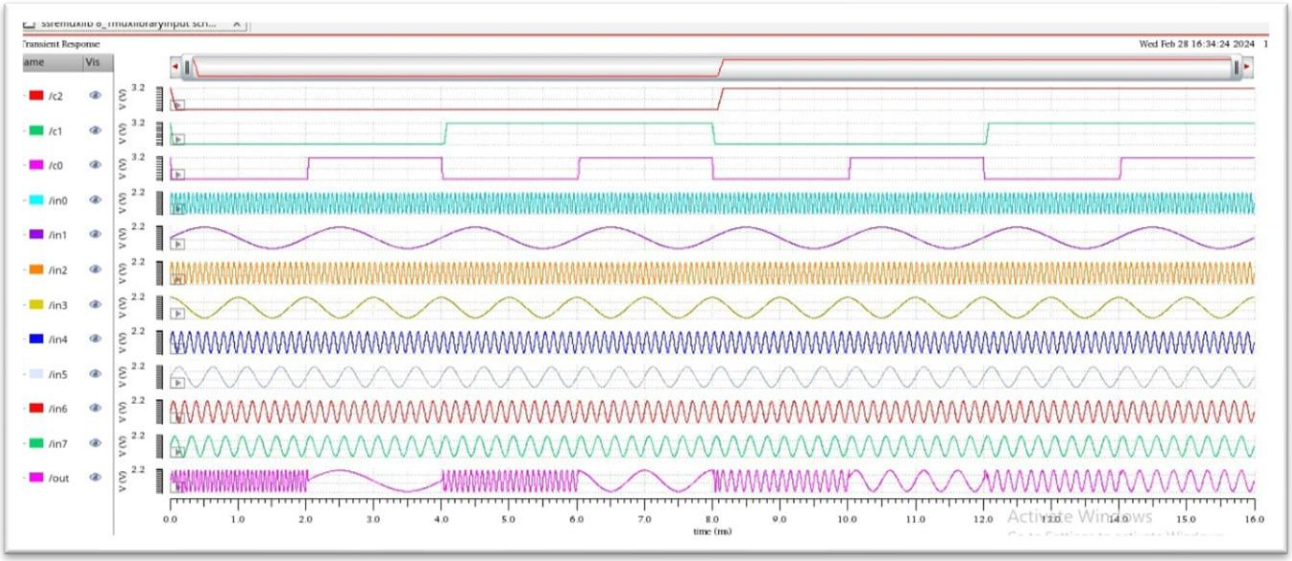

Figure-4.4.1: 8:1 Analog Mux Output

5 Design Analysis and Evaluation

5.1 Novelty

We showcase several innovative elements that distinguish our multiplexer design. Foremost is our unique focus on simplifying circuit complexity while maintaining a priority on low power consumption, a strategy that strikes a balance catering to the needs of biomedical applications and data acquisition systems. Additionally, the exceptionally low ON resistance of our design, measuring just 10 ohms, represents a significant advancement, particularly crucial for maintaining signal fidelity and minimizing attenuation in critical contexts such as medical instruments and communication systems. Our strategic adoption of CMOS transmission gate logic introduces further innovation, offering bidirectional signal flow, wide voltage compatibility, and minimal crosstalk, thereby enhancing the overall performance and reliability of the multiplexer. Moreover, our decision to operate the design with a 3V DC supply voltage demonstrates an innovative approach to efficient power management within the transistors, contributing to the multiplexer's effectiveness. Finally, our selection of tsmc18 model transistors brings novel characteristics to the design, including high threshold voltage and broad voltage swing, enabling the creation of a multiplexer with moderate bandwidth and minimal switching time, meeting specific requirements in communication channels. Together, these novel features and approaches position our multiplexer design as an innovative solution, offering advancements in efficiency, performance, and reliability across various application domains.

5.2 Design Considerations

5.2.1 Considerations to public health and safety

Our project prioritizes the reliability, accuracy, and integrity of our multiplexer design, crucial for biomedical and communication applications. Rigorous testing and validation ensure its performance and safety under various conditions. Adherence to industry standards and regulations, especially in medical and electronic communication sectors, is a top priority. Comprehensive documentation is provided to end-users to ensure safe deployment. By addressing public health and safety concerns proactively, we aim to ensure the benefits of our multiplexer design without compromising individual or community well-being.

5.2.2 Considerations to environment

Our project is dedicated to minimizing the ecological impact of our multiplexer design. We prioritize sustainability throughout the process, from material selection to manufacturing. Efforts include reducing waste, promoting recycling, and designing for durability and upgradeability to extend the product's lifespan. Additionally, we carefully consider end-of-life disposal or recycling, ensuring compliance with regulations and best practices. By integrating environmental consciousness into our practices, we aim to contribute positively to sustainability while delivering innovative solutions.

5.2.3 Considerations to cultural and societal needs

Our project prioritizes inclusivity and accessibility, ensuring that our multiplexer design accommodates diverse users, including those with disabilities and varying levels of technical expertise. We also consider the potential social impacts of our technology, aiming to contribute positively to healthcare outcomes and access, especially in underserved communities. Additionally, we prioritize ethical considerations such as privacy and data security, implementing robust measures to build trust among users. By considering these factors throughout the design process, we aim to create technology that not only meets functional requirements but also aligns with broader societal values.

5.3 Impact Assessment (PO(f))

5.3.1 Assessment of Societal and Cultural Issues

Assessing the societal and cultural impact of our multiplexer design is integral to understanding its broader implications. By identifying stakeholders and evaluating societal factors, we ensure our design aligns with diverse needs and values. Ethical considerations, including privacy and environmental impact, are carefully weighed to ensure responsible innovation. Engaging with communities allows us to gather valuable feedback and incorporate it into our design process, ensuring it meets the needs and respects the values of those it affects. Through this comprehensive assessment, we aim to create a multiplexer design that not only meets technical requirements but also contributes positively to society and upholds ethical standards.

5.3.2 Assessment of Health and Safety Issues

Assessing health and safety issues associated with our multiplexer design is essential. We evaluate risks throughout its lifecycle and implement rigorous testing to ensure safety and compliance with regulations. Adhering to industry standards remains a top priority. Our goal is to ensure the safe and responsible use of our multiplexer, protecting users and the broader community.

5.3.3 Assessment of Legal Issues

We need to check if our multiplexer design follows the rules and laws. This includes making sure we're not copying other people's ideas (like patents), and we're using the right permissions if needed. We also need to think about who is responsible if something goes wrong when using our multiplexer. By checking all these legal issues, we make sure our multiplexer design is legal and safe to use.

5.4Sustainability and Environmental Impact Evaluation (PO(g))

Evaluating sustainability and environmental impact is a crucial step in ensuring that our multiplexer design aligns with eco-friendly principles and minimizes its negative effects on the planet. This assessment involves a comprehensive examination of various factors, including energy consumption, resource utilization, material selection, waste generation, and potential environmental hazards associated with the manufacturing, use, and disposal of the multiplexer. By analyzing these aspects, we can identify opportunities to optimize energy efficiency, reduce carbon emissions, minimize resource depletion, and mitigate environmental pollution throughout the lifecycle of the multiplexer. Additionally, we explore sustainable design practices, such as utilizing recycled materials, implementing energy-efficient components, and designing for product longevity and recyclability. Through this evaluation, we aim to develop a multiplexer design that not only meets technical requirements but also promotes environmental sustainability and responsible stewardship of natural resources.

5.5 Ethical Issued (PO(h))

Addressing ethical considerations in our multiplexer design is fundamental to ensuring fairness, safety, and accountability. We prioritize several ethical principles throughout the design process, with a particular emphasis on protecting user privacy and data security. By implementing robust measures to safeguard personal information and ensure confidentiality, we aim to instill trust and confidence in our users. Moreover, we are committed to promoting inclusivity and accessibility, ensuring that our multiplexer is accessible and beneficial to individuals from diverse backgrounds and abilities. Transparency is also paramount, as we strive to provide clear and accurate information about the

capabilities, limitations, and potential risks associated with our multiplexer design. By being open and honest, we empower users to make informed decisions and cultivate a sense of trust in our product. Additionally, we recognize our social responsibility and consider the broader impact of our design decisions on society. We aim to minimize negative consequences and maximize positive outcomes, whether it pertains to environmental sustainability, public health, or social justice. Through a proactive and thoughtful approach to ethical considerations, we endeavor to create a multiplexer design that not only meets technical requirements but also upholds ethical values, respects human rights, and contributes positively to the well-being of individuals and communities alike.

6 Reflection on Individual and Team work (PO(i))

6.1 Individual Contribution of Each Member

All of us contributed with their assigned tasks and completed the project.

6.2 Mode of TeamWork

We utilized a blend of online and offline collaboration to tackle the task efficiently. We worked together through online platforms, facilitating constant communication and coordination regardless of geographical locations. Additionally, we organized offline meetings and sessions to delve into different aspects of the project, ensuring comprehensive coverage and addressing diverse requirements. By adopting this approach, we maximized flexibility and productivity, enabling team members to contribute their expertise at various times and in different capacities, resulting in a well-rounded execution of the task.

6.3 Diversity Statement of Team

Our team is made up of people from different backgrounds, each bringing their own ideas and skills to the table. We think having a diverse team is great because it helps us come up with more creative solutions to problems. With people from different cultures and areas of expertise, we're able to work together and learn from each other. We believe that by embracing our differences, we can create a welcoming environment where everyone's ideas are valued and respected, leading to better results for our project.

7 Communication

7.1 Executive Summary

Our project aims to design a highly efficient 8:1 analog multiplexer with a focus on communication applications. Using CMOS transmission gate logic, we prioritize minimizing power loss and maximizing signal fidelity. Rigorous testing ensures reliability and adherence to industry standards. Sustainability and ethical considerations guide our design, promoting eco-friendly practices and user privacy. Through community engagement, we address societal needs and build trust. Our multiplexer design prioritizes innovation, efficiency, and ethical responsibility, aiming to deliver value while contributing positively to society.

7.2 User Manual

This user manual serves as a comprehensive guide for operating the 8:1 Analog Multiplexer. With eight input channels and one output channel, the multiplexer facilitates the selection and routing of analog signals within a range of -2V to 2V. Operating with logic levels of 3V for high and 0V for low, it ensures accurate signal processing while maintaining a maximum power dissipation of 10 mW and an on-resistance of 10 ohms. Users are advised to follow the provided instructions for setup, ensuring all connections are secure before powering on the device. Once operational, users can select input channels using the control interface and monitor output signals accordingly. Regular maintenance is recommended to uphold optimal performance, and troubleshooting guidance is available for addressing common issues. With a provided warranty and contact information for customer support, users can rely on assistance for any further inquiries or assistance needed.

8 Future Work (PO(l))

Looking ahead at what we can do next, we have some suggestions for our project. First, we think it would be helpful to do some experiments to check and improve our multiplexer design. These experiments would test things like how well the signals go through, how much power it uses, and how fast it switches. We also want to see if using different materials or making it in different ways could make it work better or be better for the environment. And we'd like to try it out with real users to see how easy it is to use and if it really helps them. By doing these things, we hope to make our multiplexer design even better and more useful for everyone.

9 References

1. 8:1 Analog mux
   URL: http://ijmemr.org/Publication/V2I2/IJMEMR-V2I2-002.pdf

2. Transmission Gate and power dissipation
   URL: https://research.ijcaonline.org/volume99/number5/pxc3897911.pdf

3. Charge Injection
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