National Institute of Technology, Silchar
End-Semester (UG) Examinations, April- 2022

Subject Code: Ec 101 | Subject: Basic Electronics
Semester: 1st | Department: ECE, CSE, EE
Duration: 1.15 hours | Total Marks: 30

Attempt any five Questions

Q1. (a) Consider a CE circuit using a BJT having $I_s=10^{-15}$A, a collector resistance R_c=8.8KΩ, and a power supply of V_{cc}=12V.

I. Determine the value of the bias voltage V_{BE} required to operate the transistor at V_{CE}=5.2V. What is the corresponding value of I_c?

II. Find the voltage gain A_v at this bias point. If an input sine-wave of 5mV peak amplitude is superimposed on V_{BE}, find the amplitude of output sine-wave signal (assume linear operation). **[3]**

(b) Simplify the following function F using K map: F(A,B,C,D)=(0,2,3,5,7,9,11,13,14) **[3]**

Q2. (a) A CE amplifier utilizes a BJT with β=100 and V_A=100 V, is biased at I_c=1mA and has a collector resistance R_c=5KΩ. Find R_{in}, R_o and A_{vo}. If the amplifier is fed with a signal source having a resistance of 5KΩ, and a load resistance R_L=5 KΩ is connected to the output terminal, find the resulting A_v. **[3]**

(b) Draw the output characteristics of N-channel Enhancement type MOSFET and explain different regions of operation. **[3]**

Q3. (a) Simplify the following Boolean expression into one literal
W'X(Z'+YZ)+X(W+Y'Z) **[3]**

(b) In the circuit shown in Figure 1, the voltage at the emitter was measured and found to be -0.7V. If β=50, find I_E, I_B, I_C and V_C. **[3]**

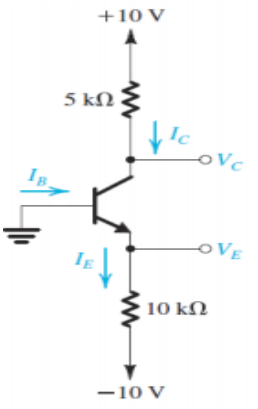


Figure 1

Q4. (a) Find V_{out} of the circuit given in figure 2: **[3]**

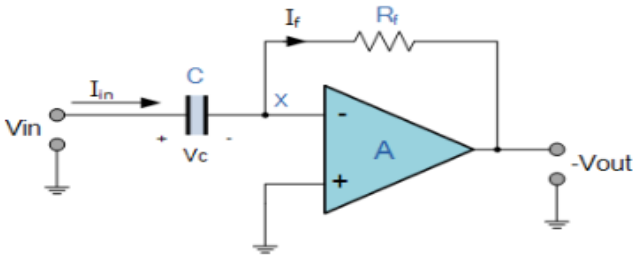


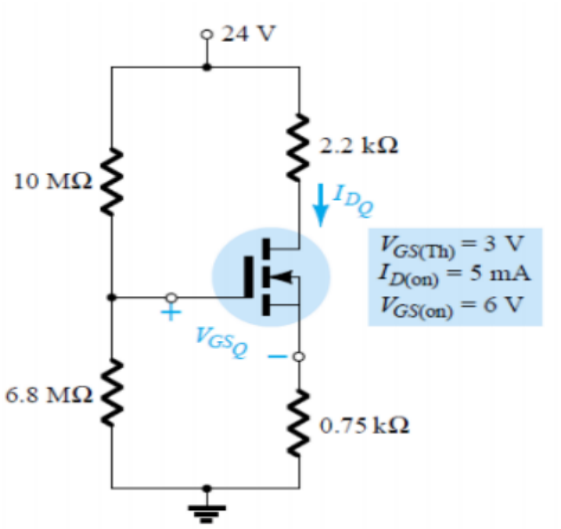
Figure 2

(b) Design a combinational logic circuit with three input variables that will produce a logic 0 as output when more than one input variable are logic 0. **[3]**

Q5. (a) If the differential amplifier has a differential gain of 20000. CMRR-80dB, then Find the common mode gain. **[1]**

(b) An OP-AMP has a slew rate of 5 V/usec. Find the largest sine wave output voltage possible at a frequency of 1 MHZ. **[1]**

c) For the circuit as shown in the figure 3, determine the following:
i) Drain current I_{DQ} ii) Gate to source voltage V_{GSQ} ii) Drain voltage V_D iv) Source voltage V_s

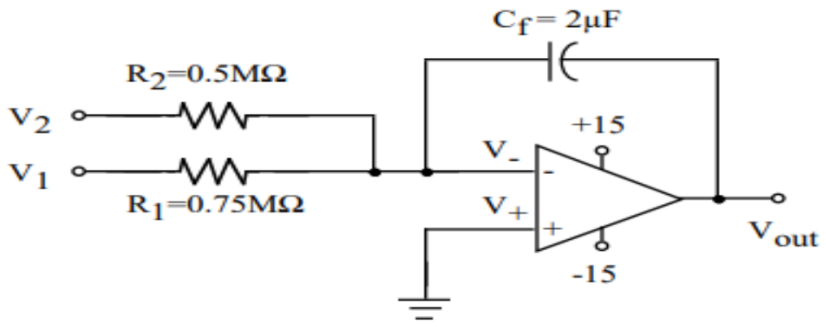


[4]

Figure 3

Q6. (a) What is the drain current for D-MOSFET having the characteristics of $I_{DSS} = 10$ mA, $V_{GS\,(off)} = -4$ V, and $V_{GS} = 2$ V. **[2]**

(b) If $V_1 = 10\sin(200t)$ and $V_2 = 15\sin(200t)$. What is V_{out}? **[4]**


$C_f = 2\mu F$
$R_2 = 0.5M\Omega$
V_2
V_1
$R_1 = 0.75M\Omega$
V_-
V_+
+15
-15
V_{out}