Project Report: VLSI 1 Lab (EEE 456)

Project Title: IC Layout Design of 4-bit Universal Shift Register using Electric VLSI Design System

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ABSTARCT

This project describes the design of an Integrated Circuit (IC) layout for a 4-bit USR. The layout was designed by use of a well-known IC design software named "Cadence" which is an Electronic Design Automation (EDA) tool. USR means Universal Shift Register which is capable to operate in 4 state and this register can shift data from left to right as well as right to left. Control inputs decides the direction of shift of data. 4 units of 4*1 Multiplexers and 4 units of D flip-flops are used to implement the whole circuit. CMOS technology has been used to build the circuit diagrams and we have also tried to use GDI technology. We have found a trade-off relationship between speed, power, no. of MOSFETs vs output wave form accuracy. 360 MOSFETs are used here to complete the whole circuit.

KEYWORDS:

1. NAND gate
2. Schematic diagram
3. DRC error
4. LVS error
5. Layout
6. Substrate Tapping
7. Bidirectional shift register
8. GDI technology
9. CMOS technology
10. 5T technology
11. Multiplexer
12. D-latch
13. Edge Triggered
14. Level triggered
15. Schematic driven layout

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INTRODUCTION

Universal shift register is a digital logic device which is capable of shifting input data from left to right as well as right to left. Two input data control the shifting direction. 4 unique combinations are possible using 2 control inputs. Multiplexer is used to select the desired direction data shift and D flip-flop shifts the bits.

OBJECTIVES

- Sketching the transistor-level schematic circuit diagram of Universal Shift Register
- Providing proper input to the USR and evaluate the output waveform.
- Drawing the layout of whole circuit and checking DRC as well as LVS.
- Simulate Universal Shift Register layout and compare the result with the result from schematic simulation.

THEORY

Shift registers could either perform right or left data shift, or both depending on the kind of shift register and their configuration. In right shift operations, the binary data is divided by two. If this operation is reversed, the binary data gets multiplied by two. With suitable application of combinational logic, a serial shift register can be configured to perform both operations.

Here is the 4-bits register in the image below. A couple of NAND gates are configured as OR gates and are used to control the direction of shift, either right or left [1].

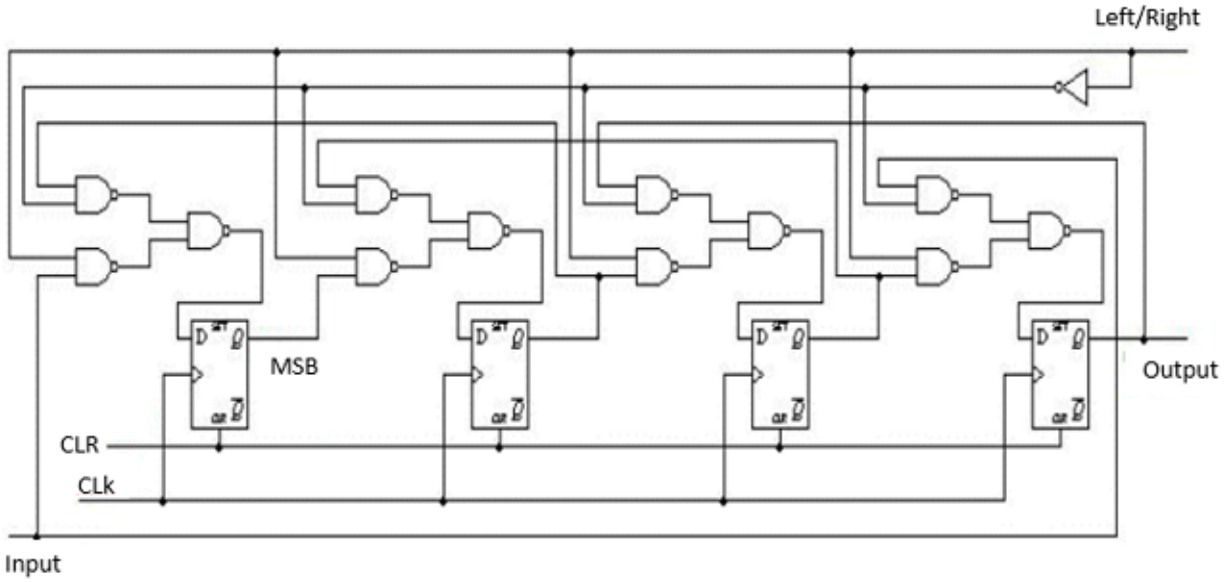


Fig: Schematic and layout design of 2 inputs NAND gate [2]

The control line left/write is used to determine the direction to which data is shifted, either right or left.

TOOLS USED

- VMware Workstation
- Cadence
- Computer

PROCEDURE

Inverter: the starter

It is obvious that the project has started with inverter. Very easy to implement but much essential in most of the devices.

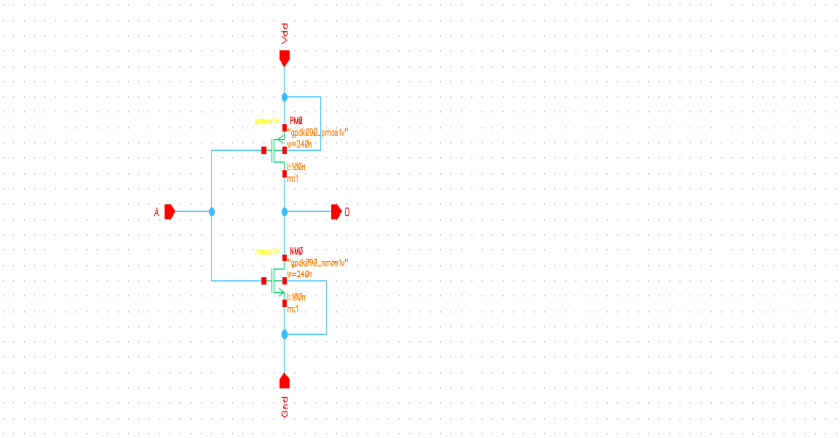


Fig: Schematic- CMOS Inverter

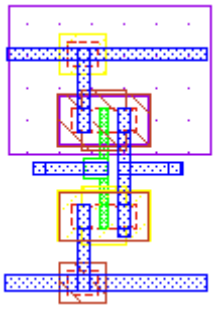


Fig: Layout- CMOS Inverter

2,3-input NAND: universal gate for universal shift register

When D flip-flop is needed, then NAND is the best choice because its high speed. Its pull-up network is connected through parallel MOS connection where NOR has series one.

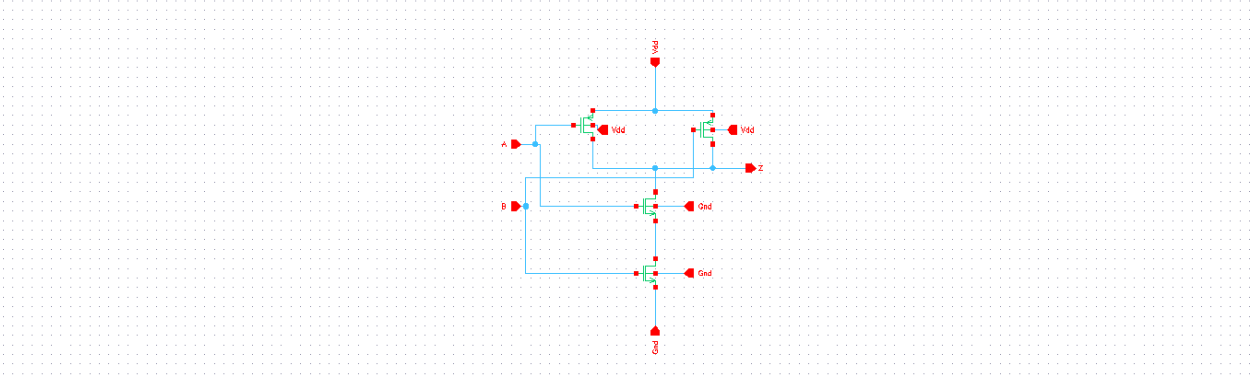


Fig: Schematic- CMOS 2-input NAND gate

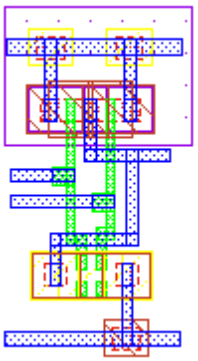


Fig: Layout- CMOS 2-input NAND gate

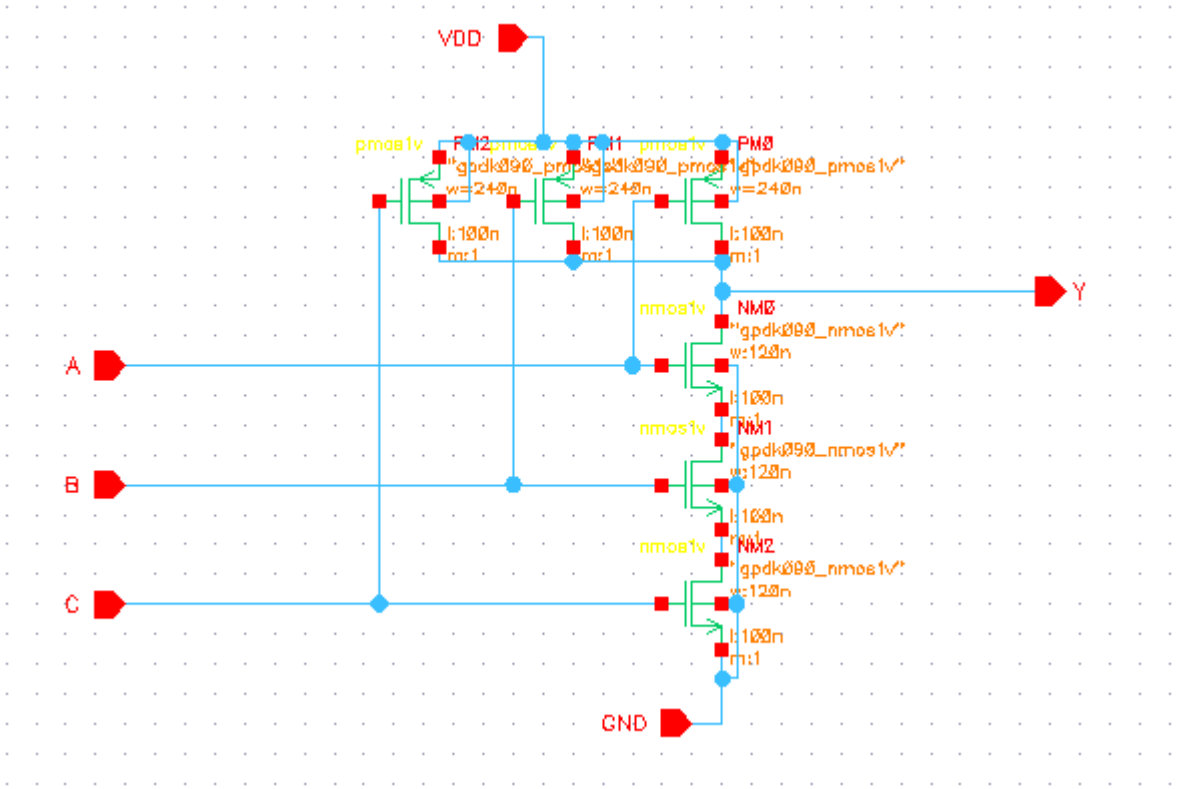


Fig: Schematic- CMOS 3-input NAND gate

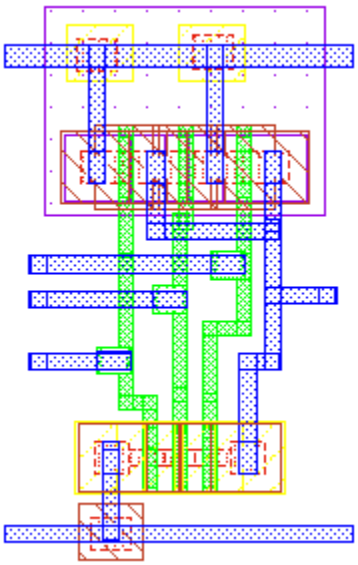


Fig: Layout- CMOS 3input NAND gate

3-input AND: Basic for myriad

We need MUX and the basic need of a MUX is AND gate. 4*1 MUX needs 4 units of 3-input AND gate.

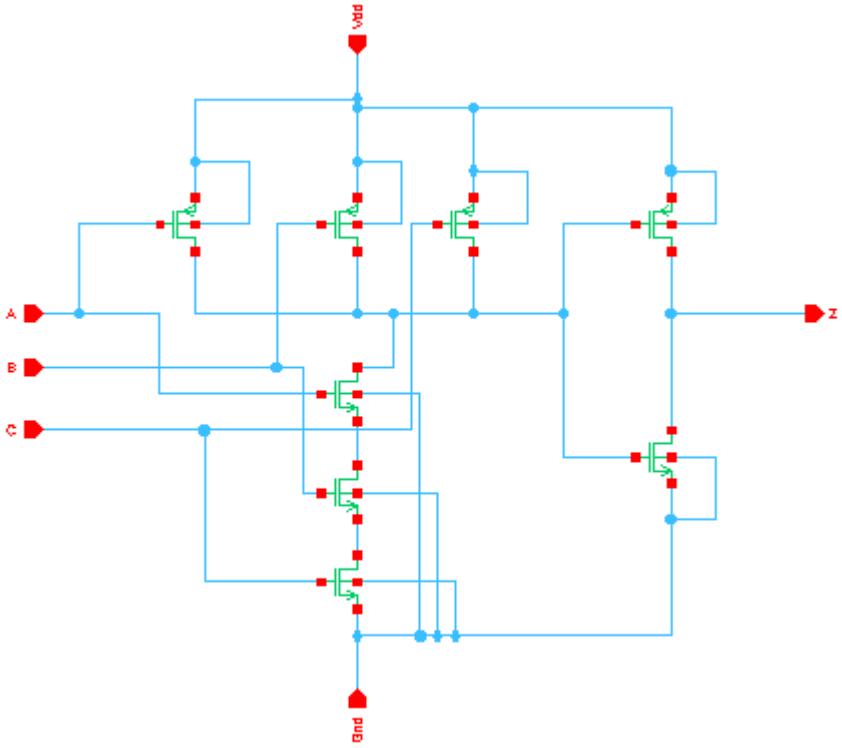


Fig: Schematic- CMOS 3-input AND gate

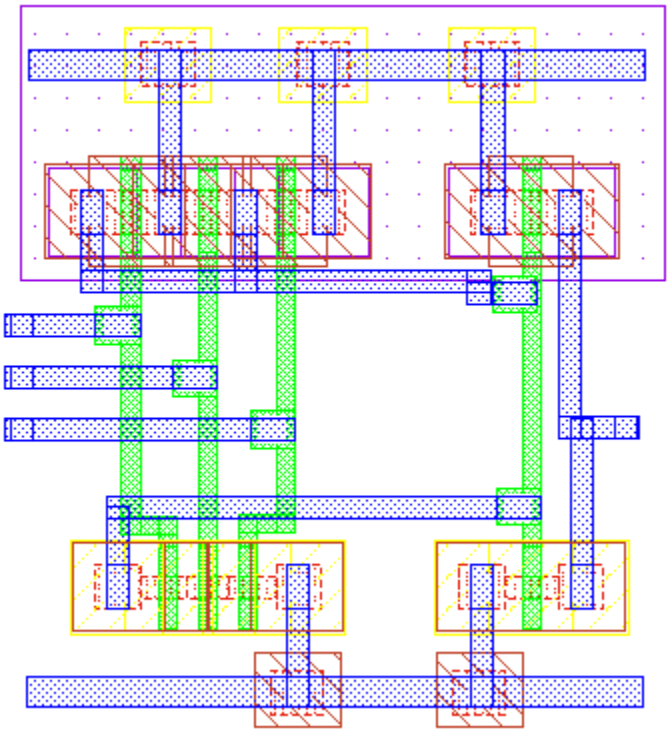


Fig: Layout- CMOS 3input AND gate

4-input OR: 4 Bit USB-4 modes-4bit mux-4bit OR

Although we can operate a bidirectional shift register with NAND gates, but it's good to use a MUX to fully control the modes, and obviously, MUX needs OR gate. Here, 4-bit OR gate is needed as 4*1 MUX will be implemented.

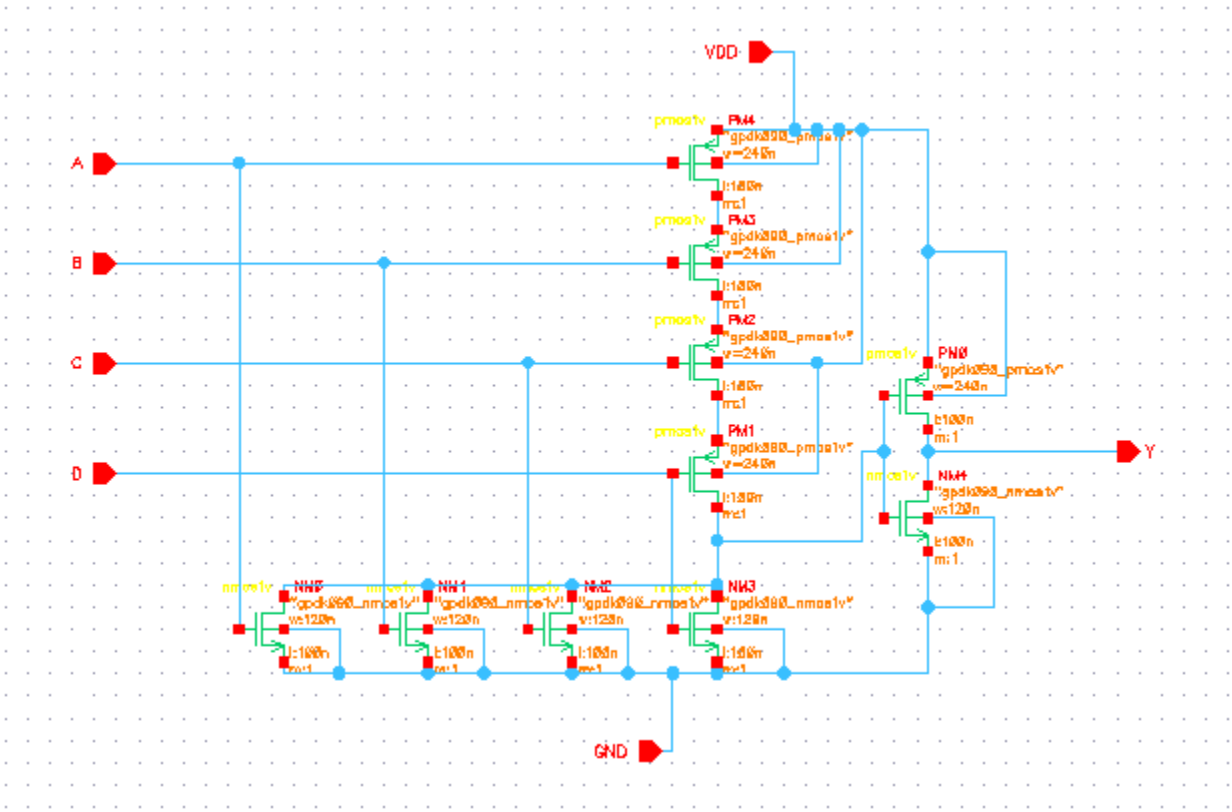


Fig: Schematic- CMOS 4 input OR gate

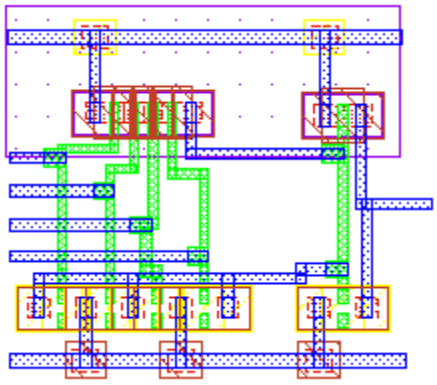


Fig: Layout- CMOS 4 input OR gate

D flip-flop:

Register means a lump of Flip-flop. We have to handle 4 bits here and for simplicity, we have used 4 units of D flip-flop. The main data shifter of our USR is D flip-flop, we have used D

flip-flop as it is much simpler and it can be constructed with less MOSFETs. Our flip-flops are negative edge triggered and these have also Preset and Clear pin and both of these are 0 activated type.

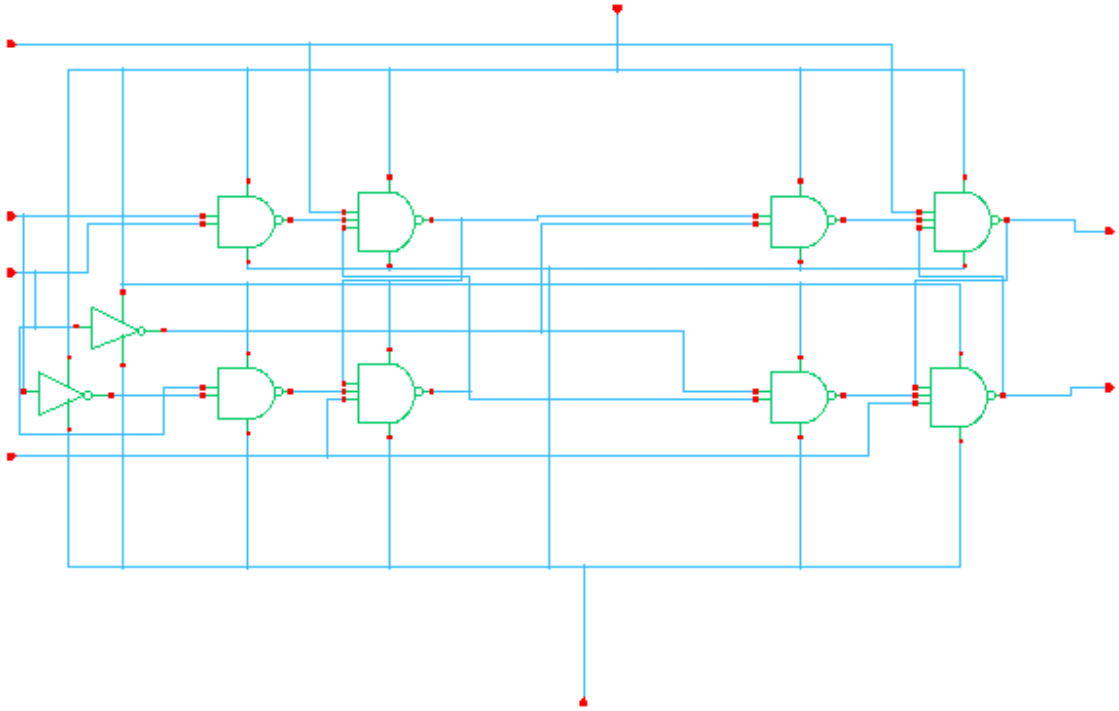


Fig: Schematic- CMOS D flip-flop

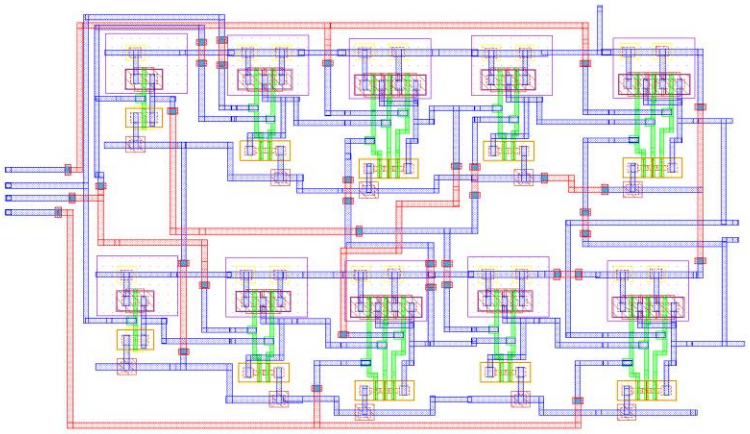


Fig: Layout- CMOS D flip-flop

MUX: for Maximum controllability

We have 4 different mode and MUXs are the controller of these modes and operates the flip-flop to shift the data in the desired direction. Here it's a 4:1 MUX.

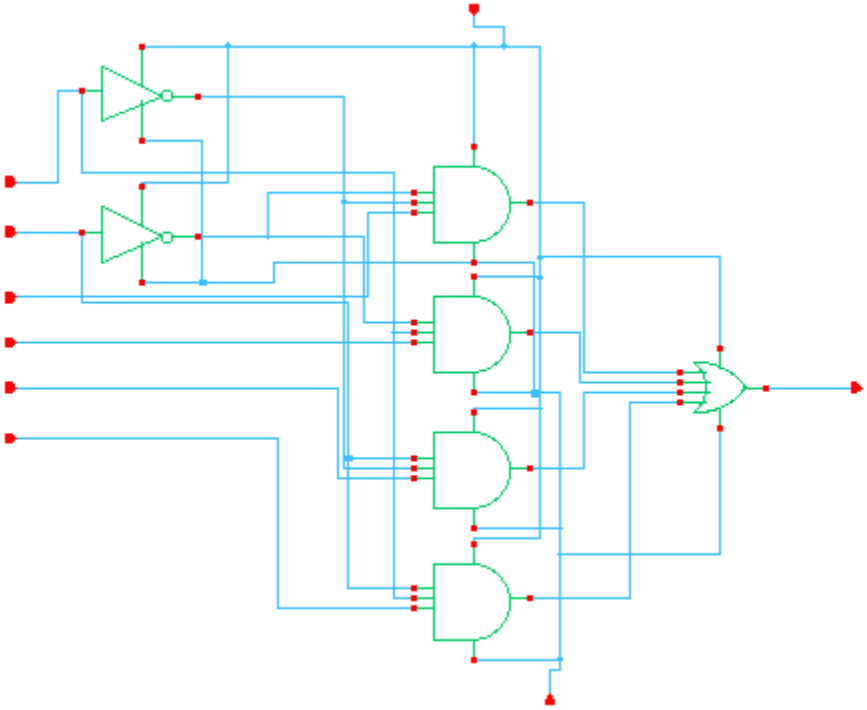


Fig: Schematic- CMOS 4:1 MUX

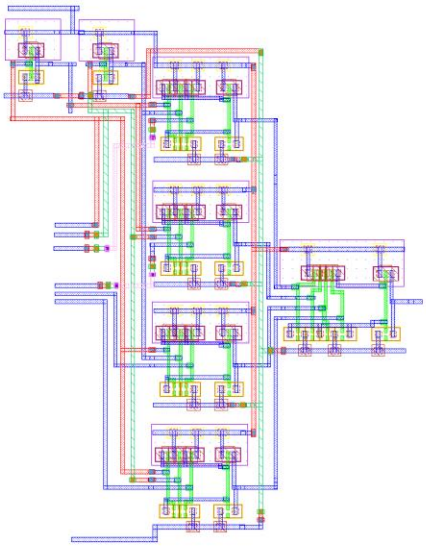


Fig: Layout- CMOS 4:1 MUX

USR: The terminator

Cascading 4 MUXs and 4 D flip-flop makes our cherished Universal shift register and it's operating in 4 modes!

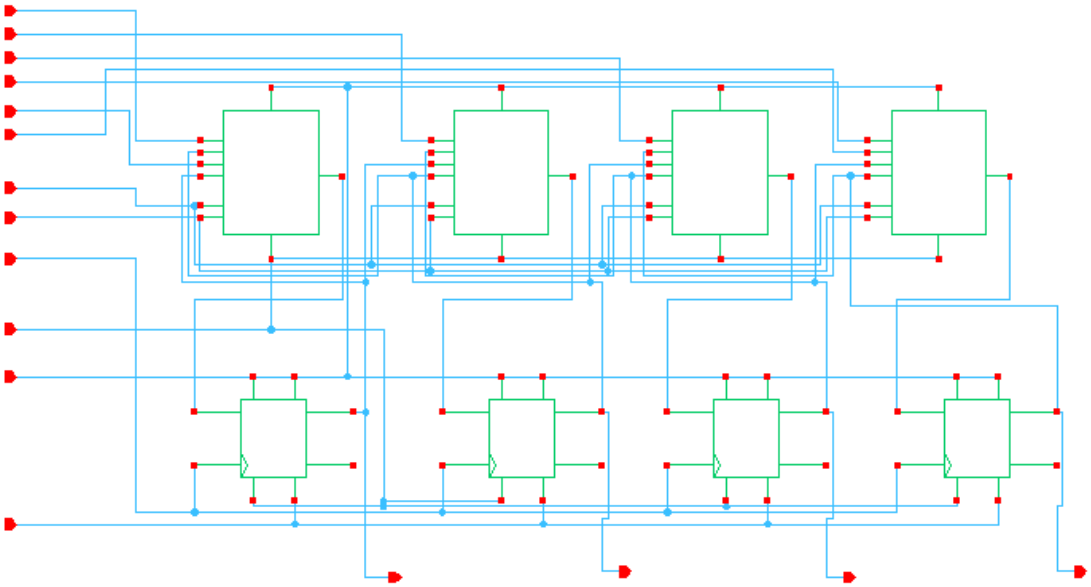


Fig: Schematic- CMOS Universal Shift Register (USR)

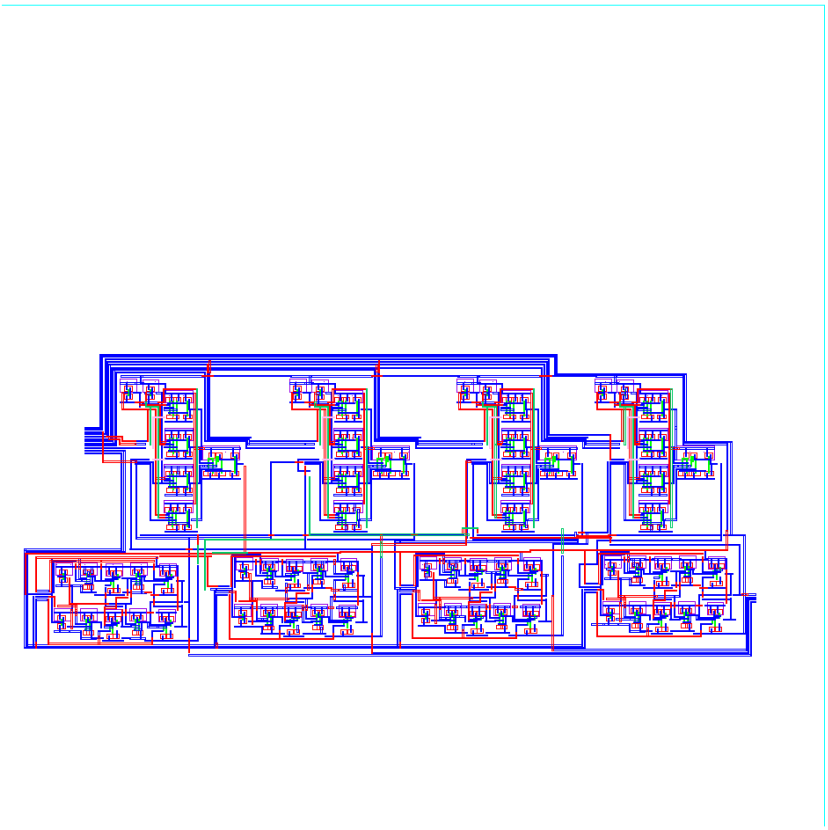


Fig: Layout- CMOS Universal Shift Register (USR)

Run from Layout

To make sure that our layout is totally compatible with our schematic, we have run the schematic and layout separately, then compare two results(plot). To do this, parasitic extraction is needed.

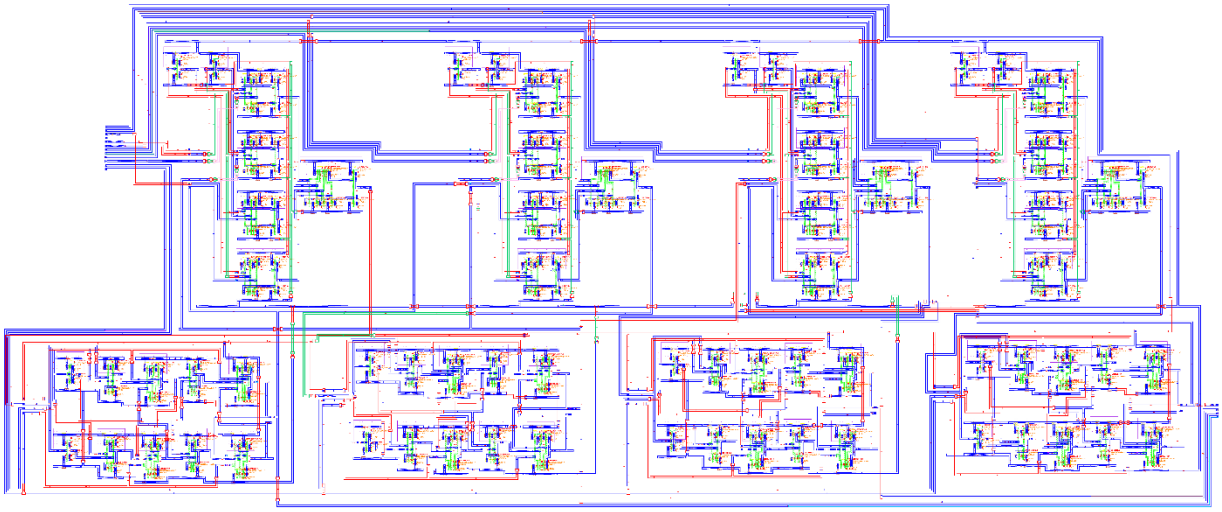


Fig: Parasitic Extracted Layout- CMOS Universal Shift Register (USR)

Testing and Result

Testing Circuits:

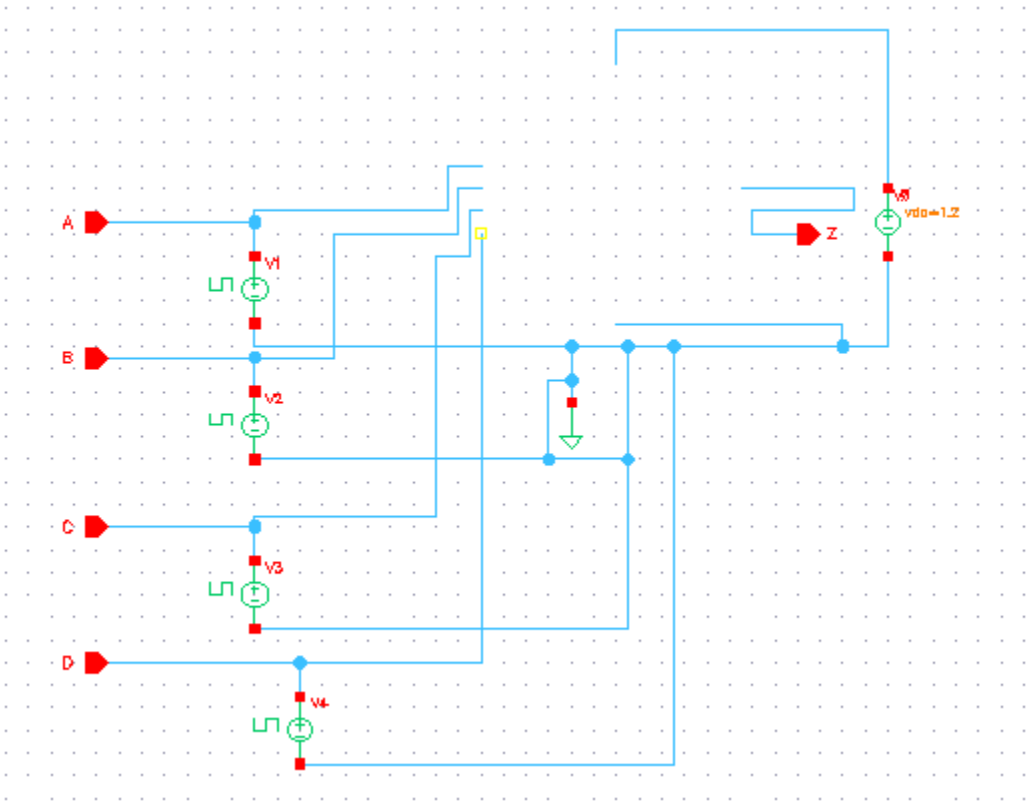


Fig: Schematic- Testing Circuit for Basic and Universal gates

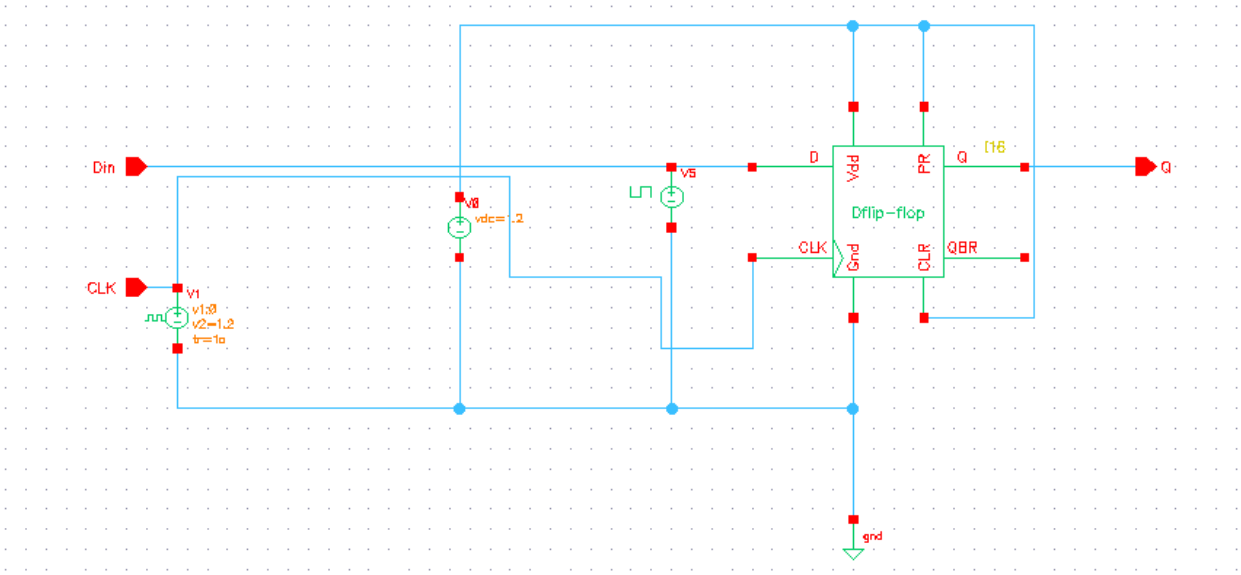


Fig: Schematic- Testing Circuit for D flip-flop

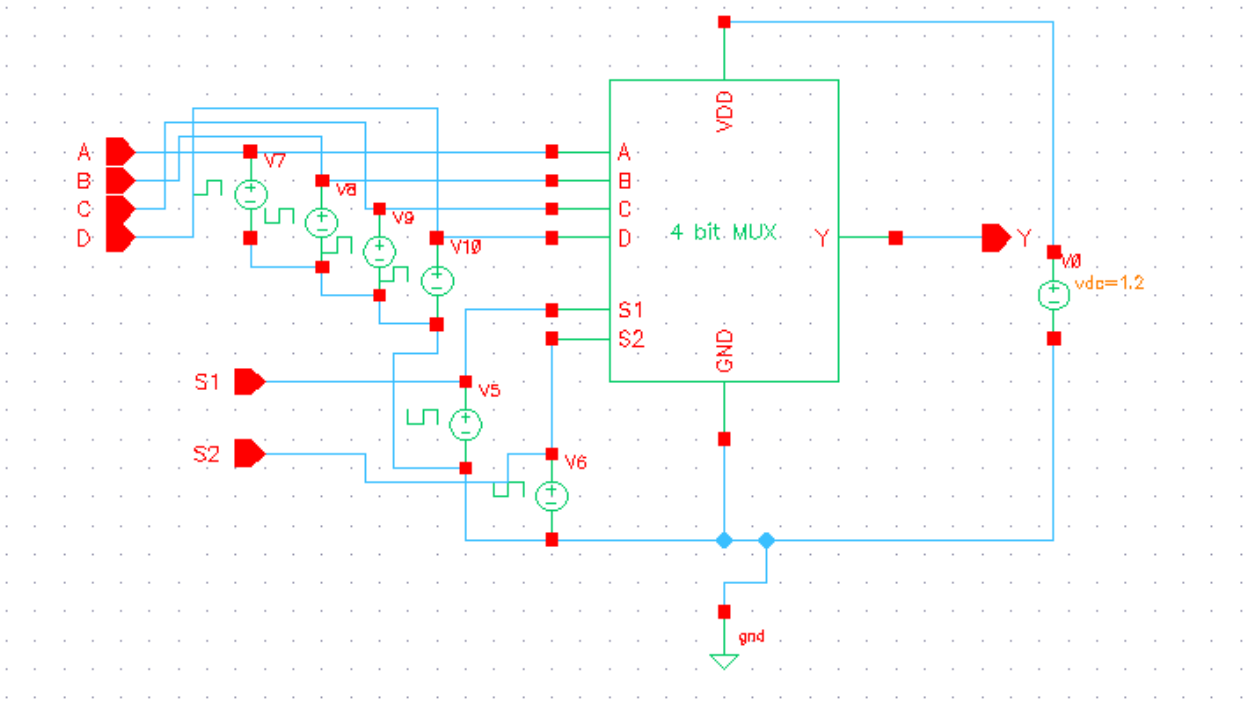


Fig: Schematic- Testing Circuit for 4*1 MUX

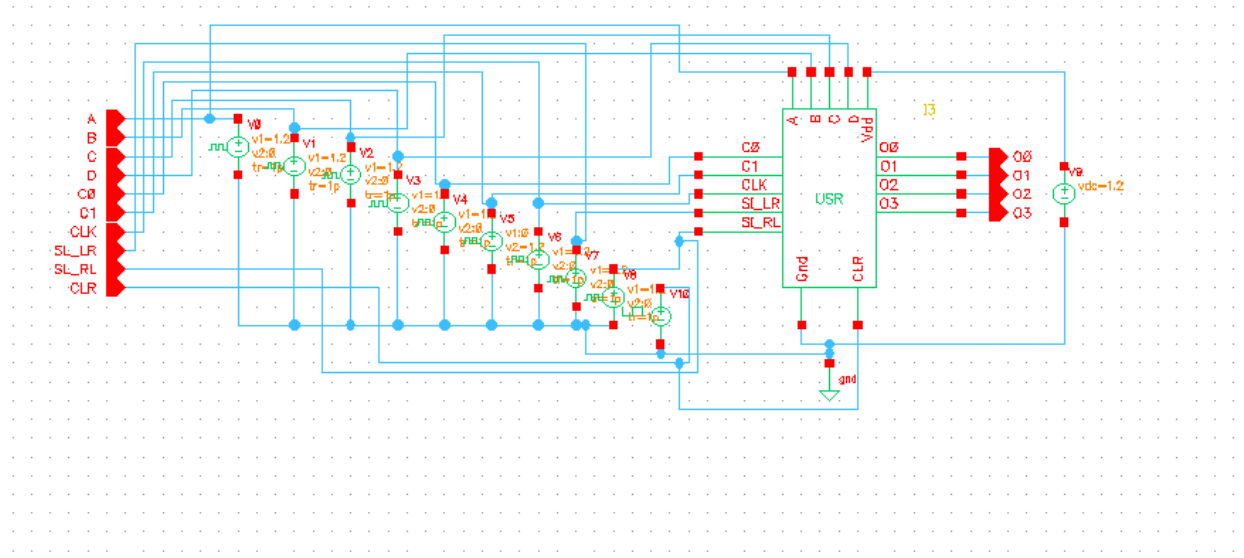
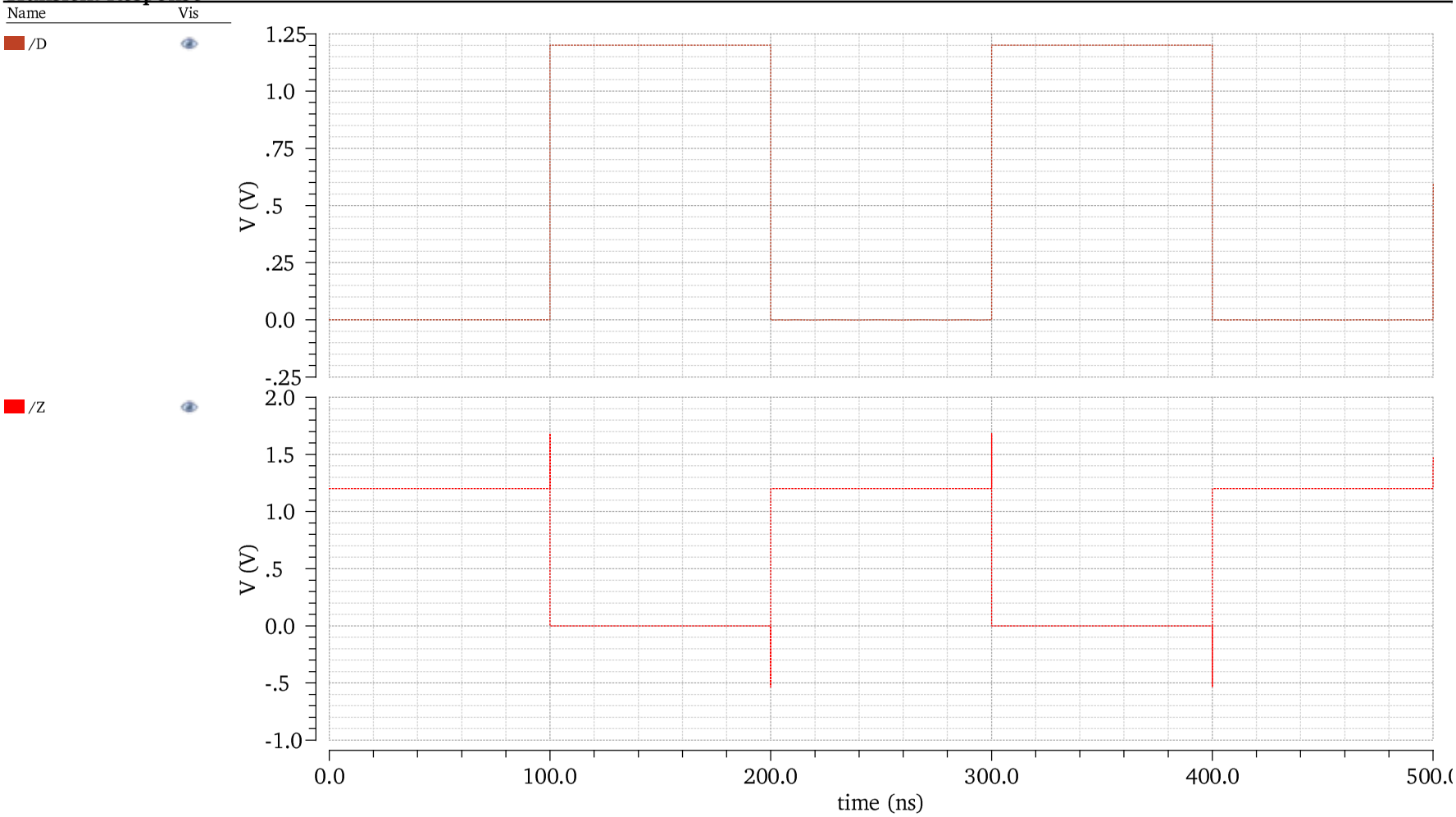


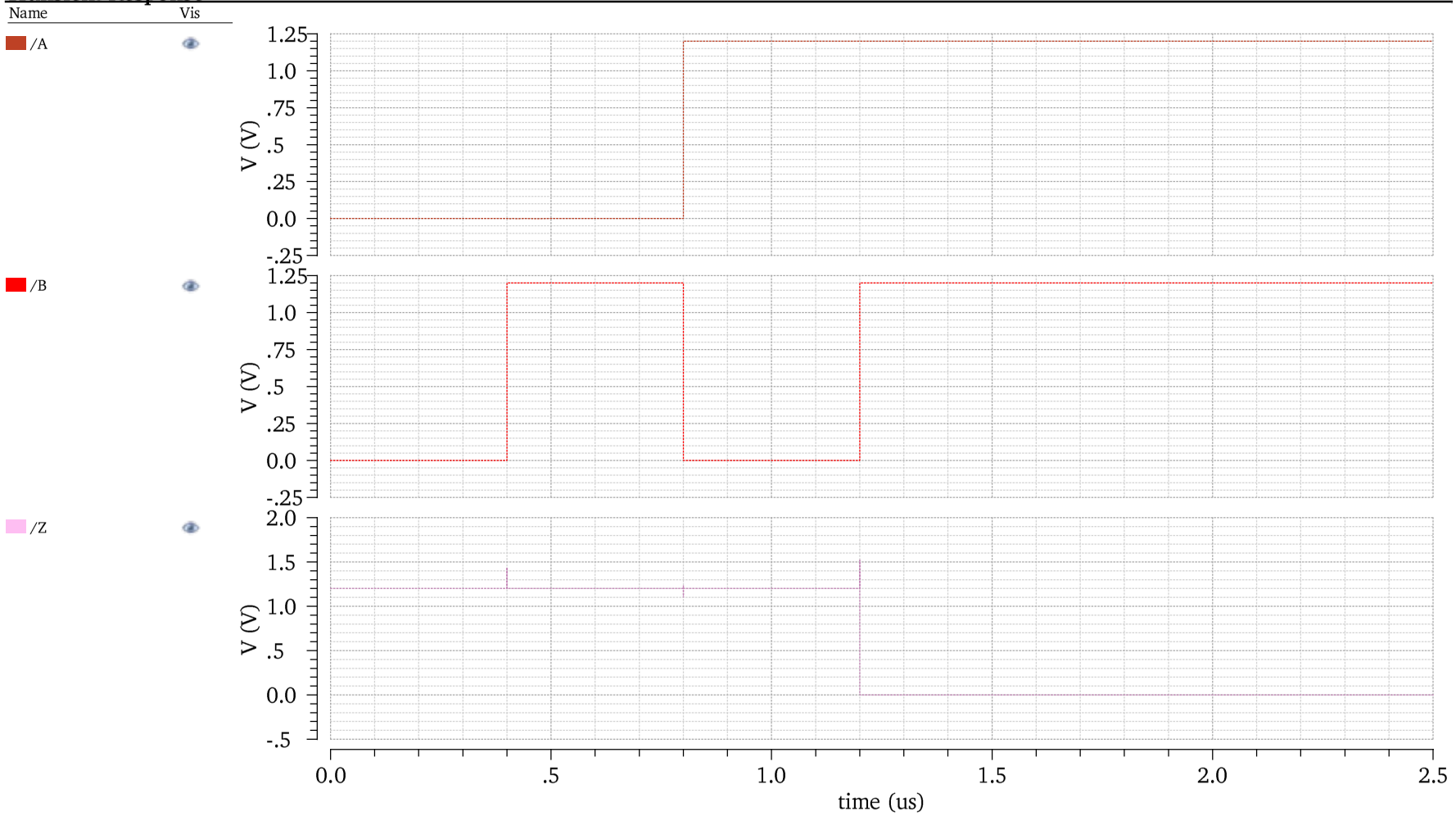
Fig: Schematic- Testing Circuit for Universal Shift Register (USR)

Output Plots:

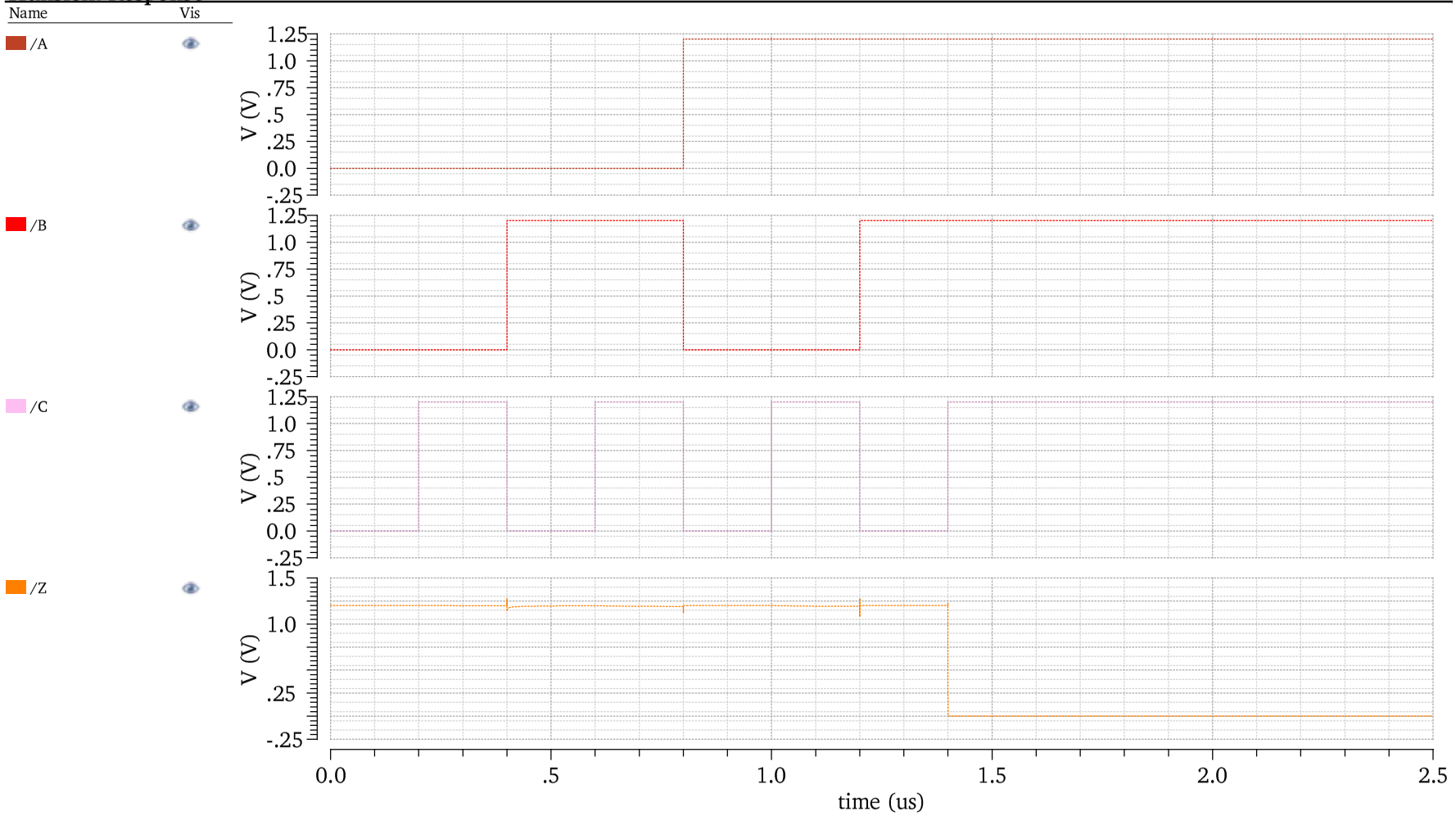
Transient Response



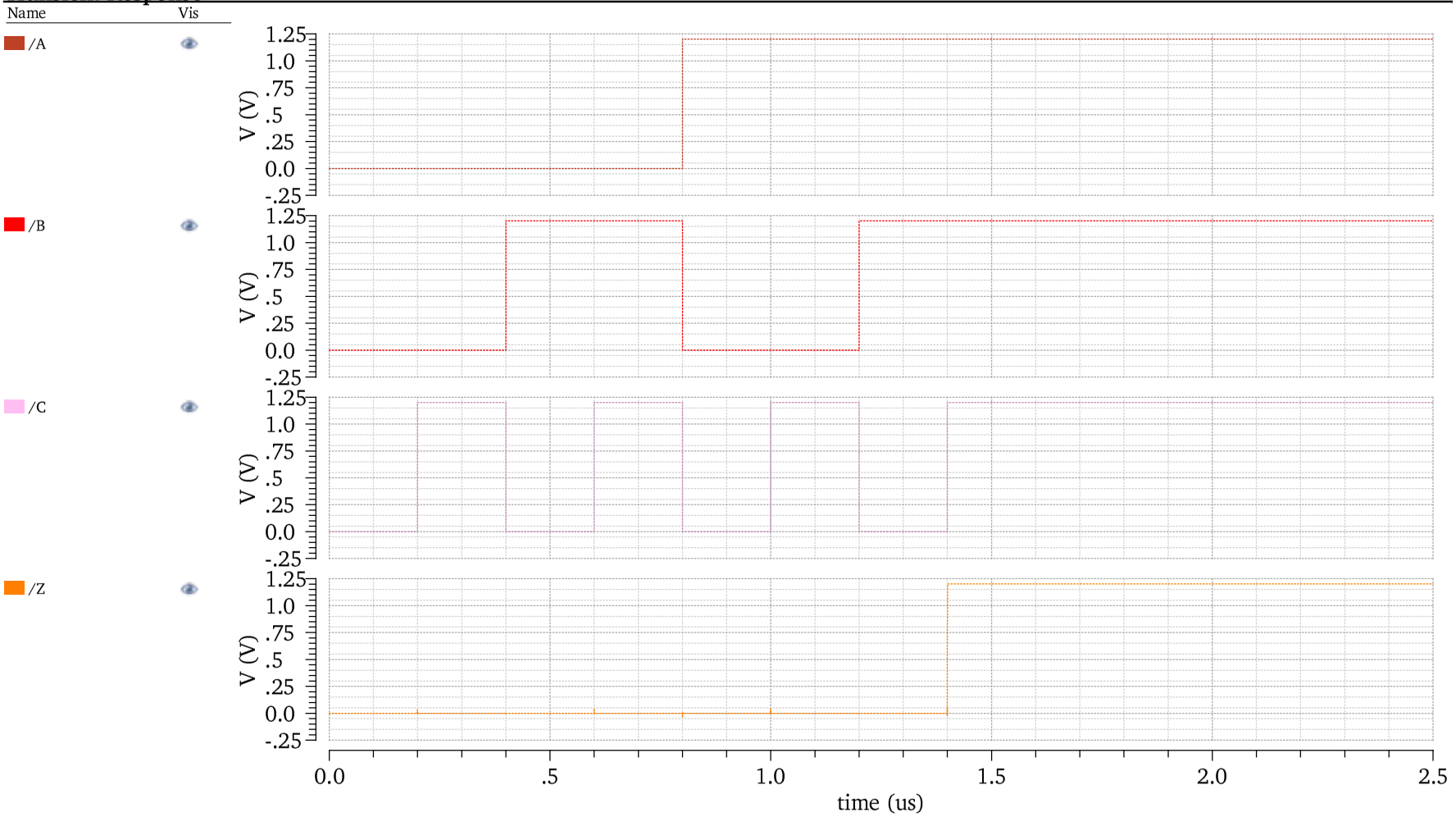
Transient Response



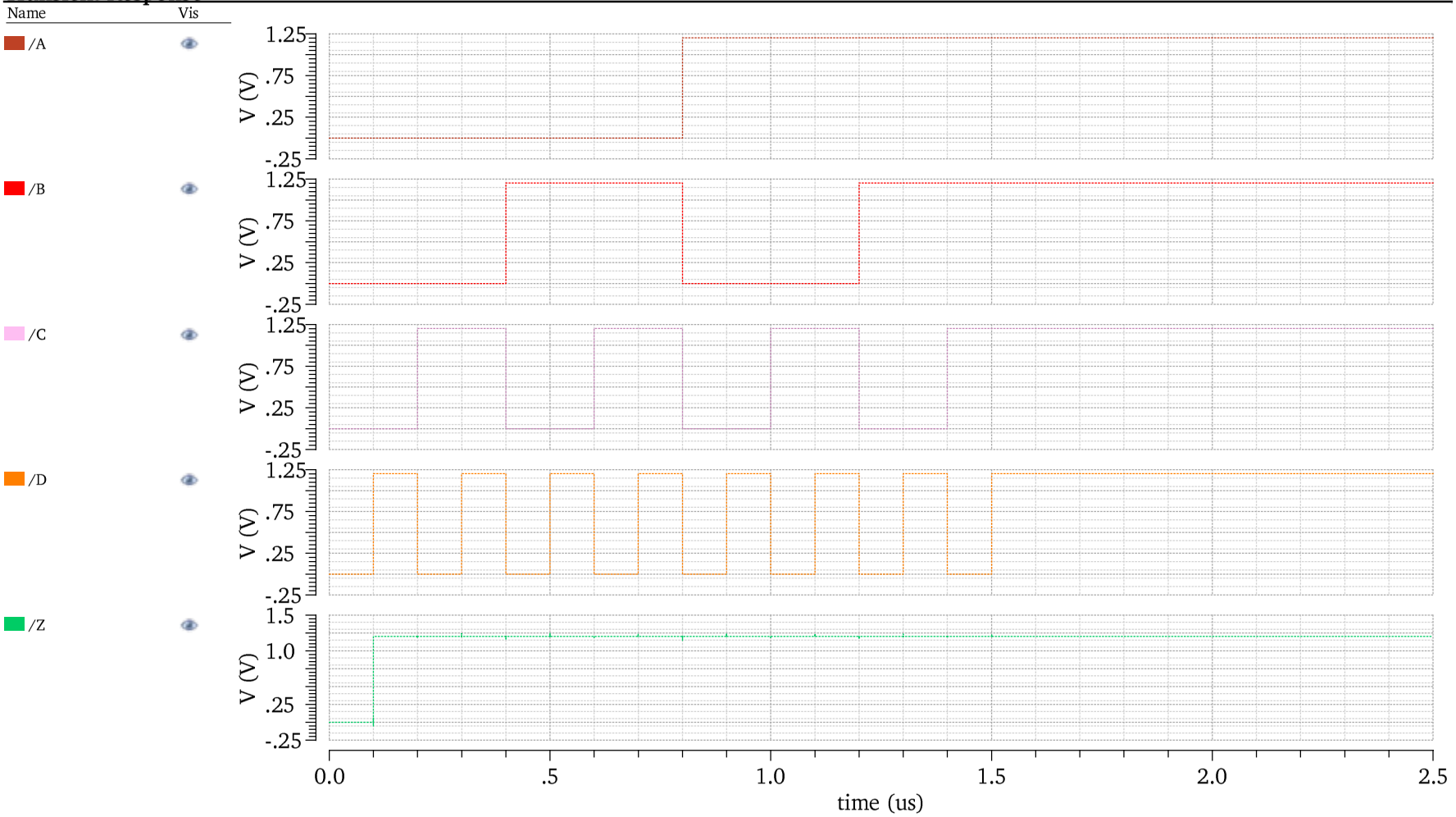
Transient Response



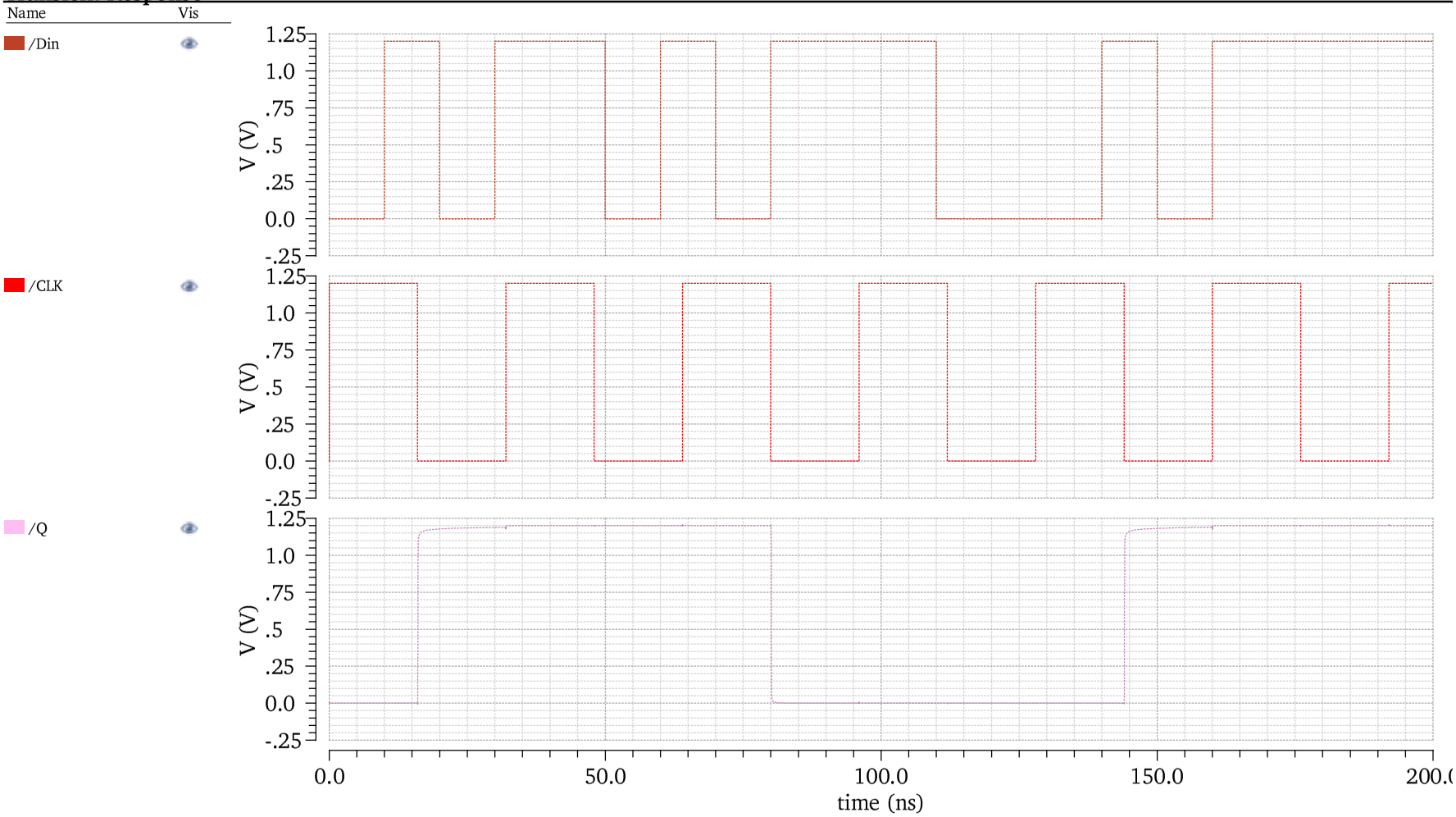
Transient Response



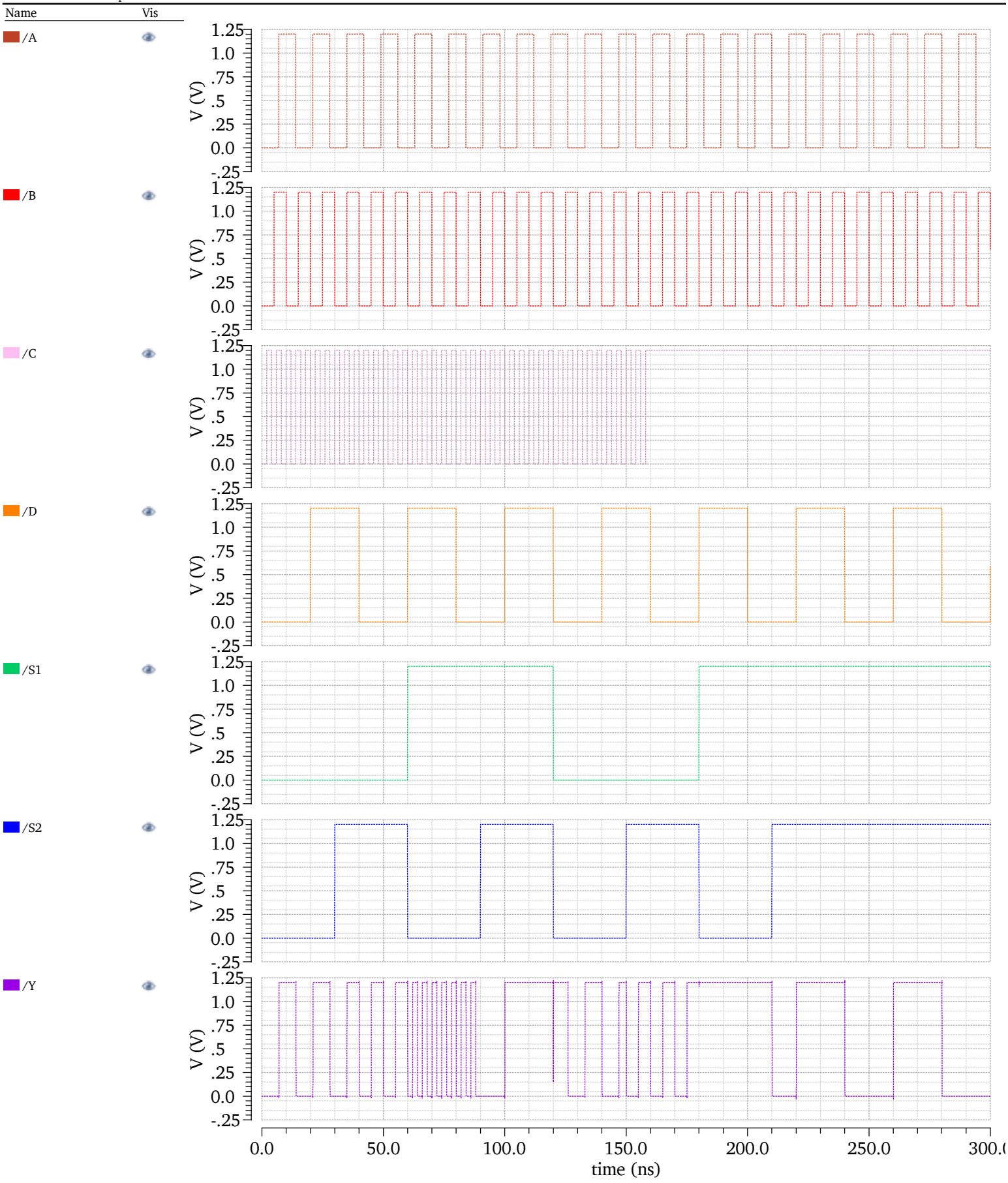
Transient Response



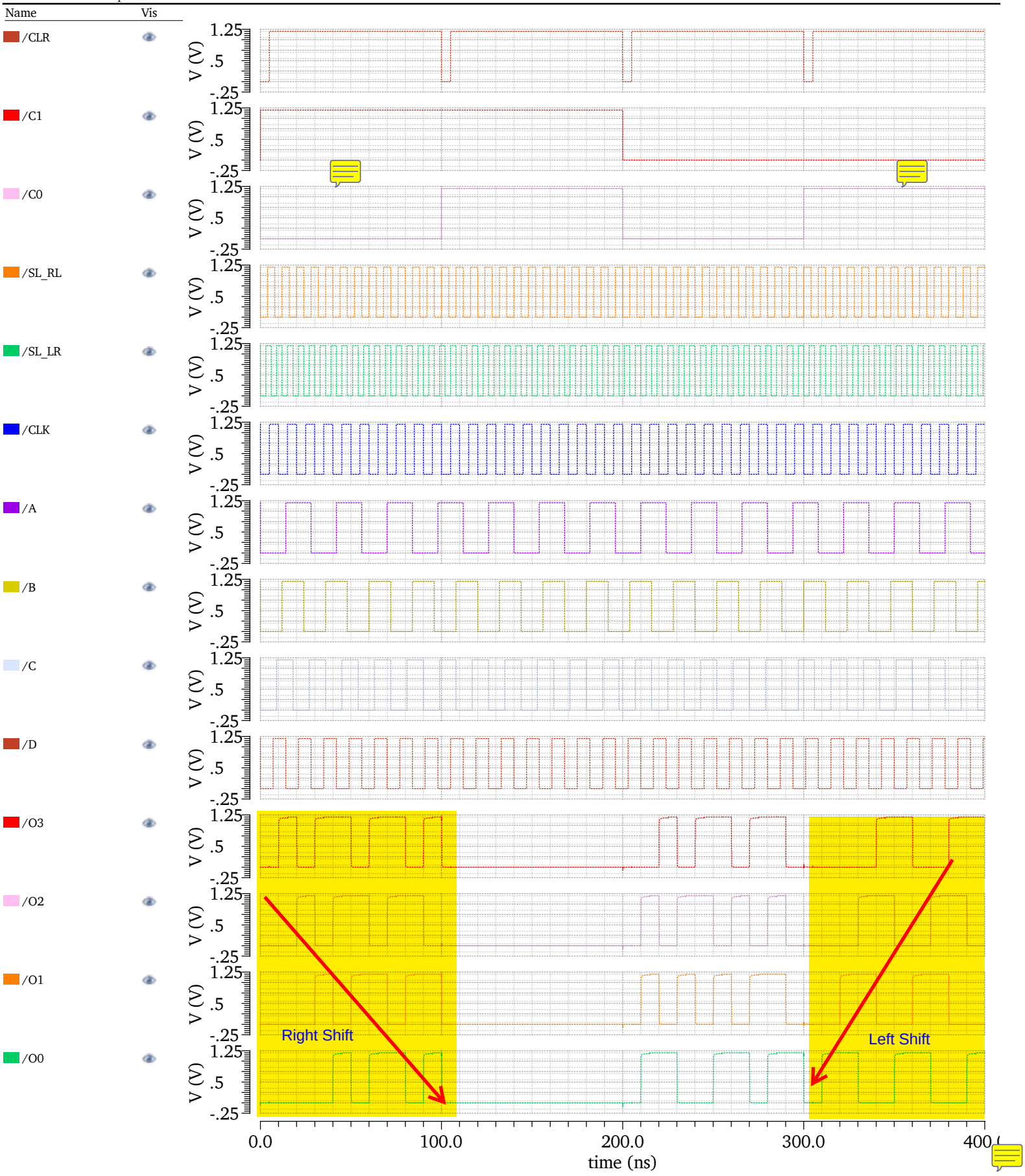
Transient Response



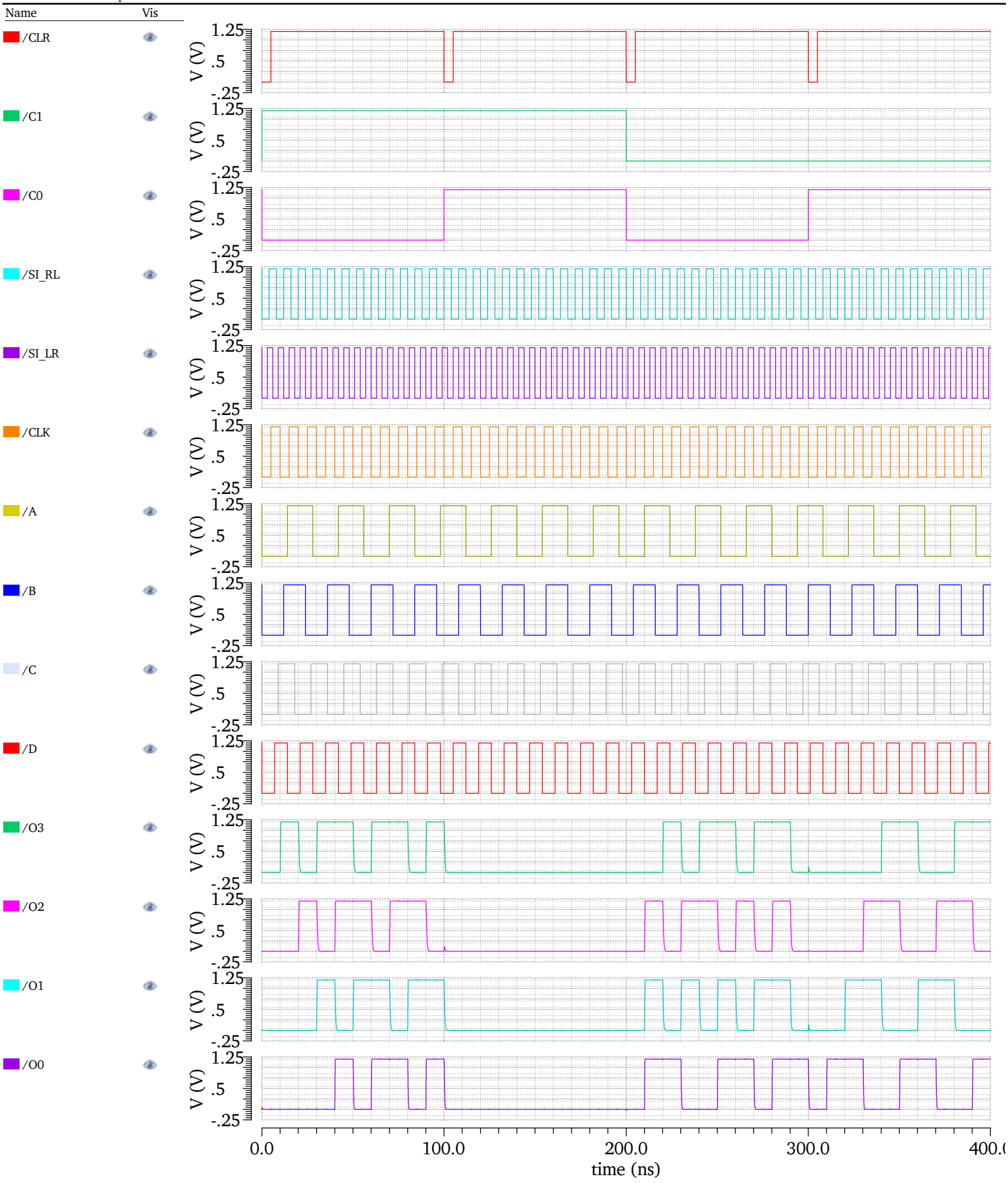
Transient Response



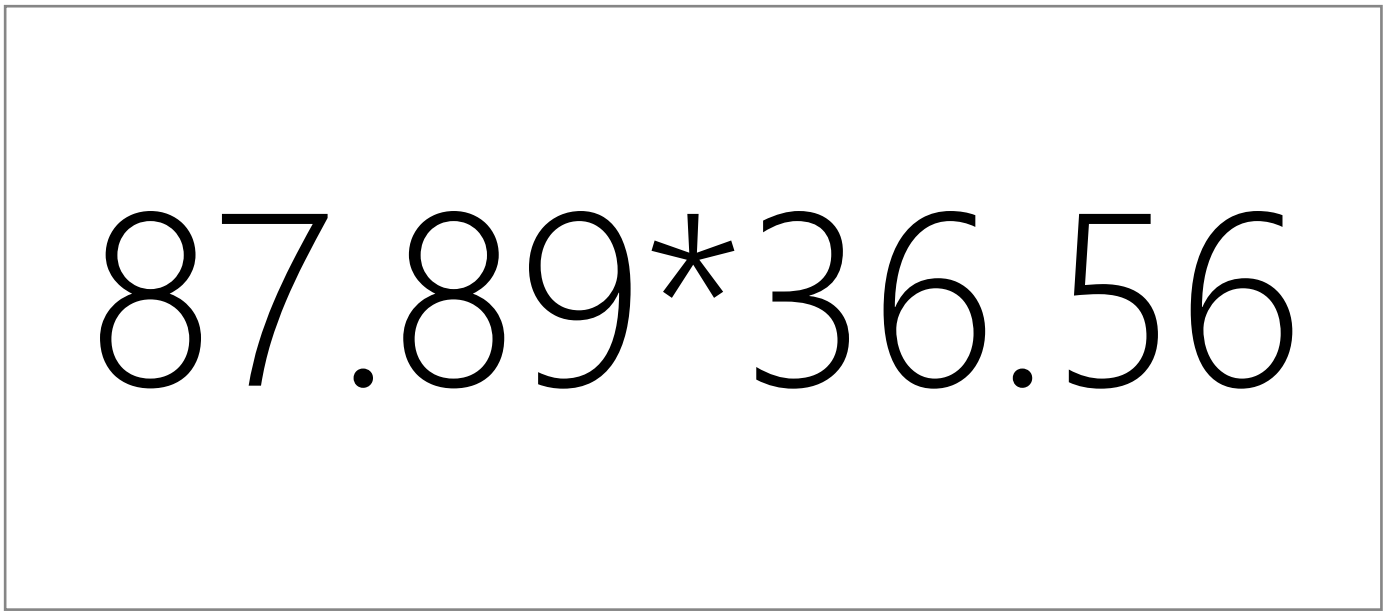
Transient Response



Transient Response



Our Designed Chip Area



CONCLUSION

It is obvious that layout design using Virtuoso XL is much better than manually designing layout. Especially it is much cumbersome in larger circuit layout design. Minimum size design can be achieved by practicing.

In modern IC design industry, it is pretty important to achieve minimum delay with low power consumption and obviously, it can be achieved by using least number of transistors. In Universal Shift Register, D flip-flop contains most of the transistors and is mostly responsible for delay. So, we have tried to minimize the number of transistors in D flip-flop and had found some non-conventional technologies [4]:

- GDI Technology
- 5T Technology [7] (only 5 transistors are needed to implement a D flip-flop)
- TSPC Technology [3]
- Pass transistor Technology
- MTCMOS Technology [5]

We have tried to implement D flip-flop by using these techniques, but the reality is, these short-cut technologies are power and time efficient [6], but the output characteristics of these circuits are too poor to use these in more complex circuits like USR. So finally, we have used CMOS technology to ensure correctness of our output.

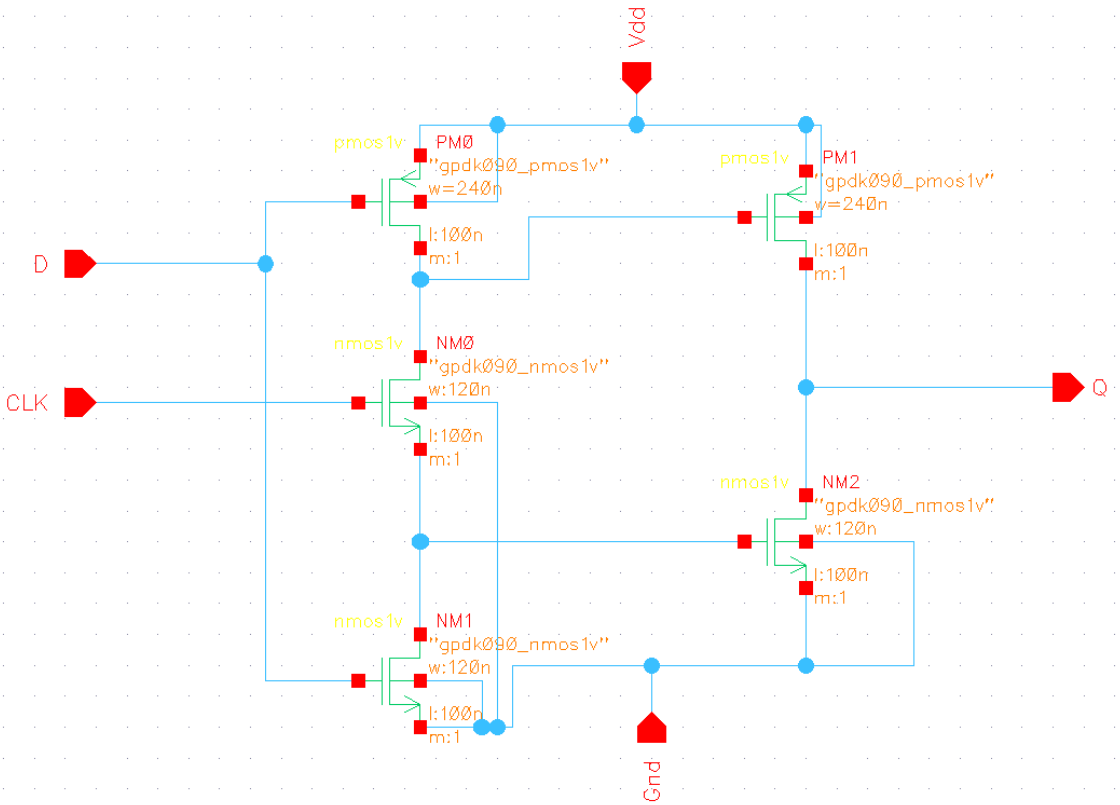


Figure: D flip-flop in 5 T technology

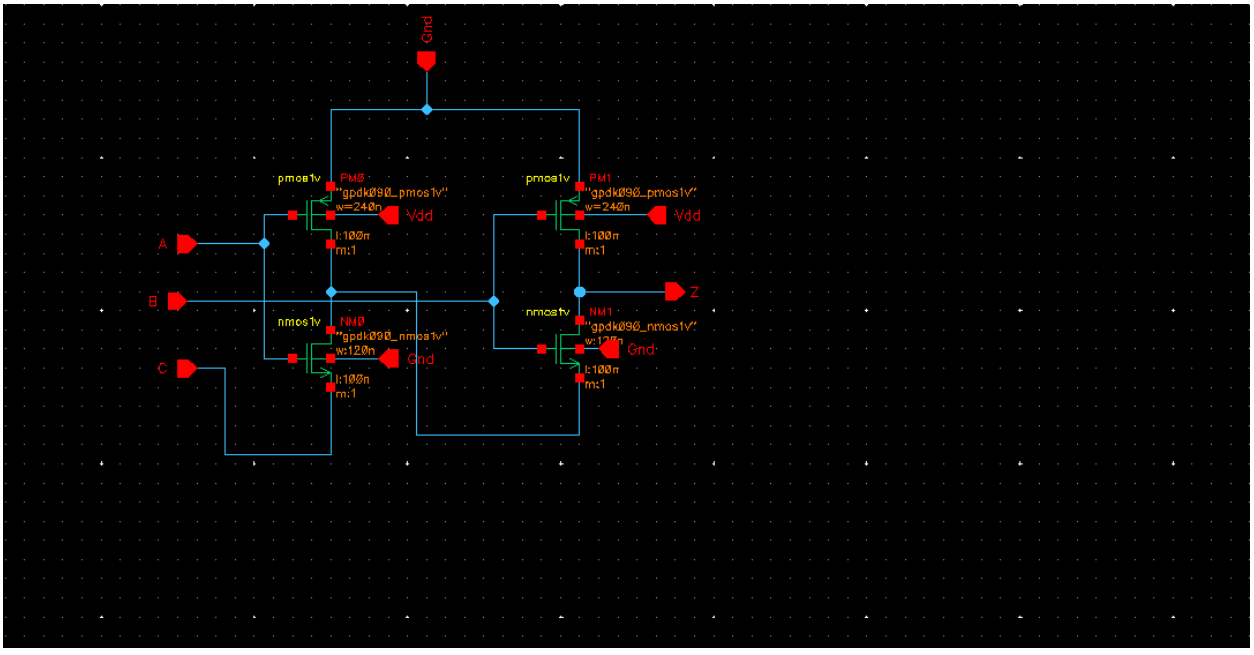


Figure: A schematic in GDI technology [8]

Another important observation is, we can use normal D flip-flop in this device but we've used master-slave D flip-flop. The reason behind this is, if we use conventional D flip-flop, we need an edge detection circuit which needs several (odd numbers) of inverter. In this way we need a significant number of inverters in our circuit which needs MOSs and the output if of the edge detection circuit isn't satisfactory when we have tested it. On the other hand, the master slave flip-flop doesn't need any edge triggering external device, its internal structure is compatible to detect edge (positive or negative) by its master slave dependency technique.

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