Error Control Codes

Course Code: CSC 3116 Course Title: Computer Networks

Dept. of Computer Science
Faculty of Science and Technology

Lecturer No:	11	**Week No:**	12	**Semester:**	Summer 19-20
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Lecture Outline

Datalink layer

EDC → Error detection code

ERC → Error correction

EDC

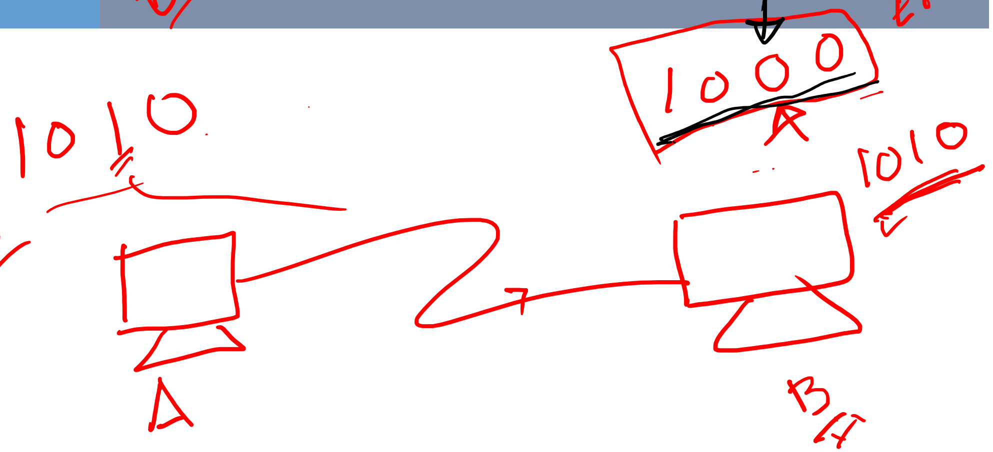
1. Cyclic redundancy check
2. Linear block code

ECC

H | Packet | T

Error

data rate



Cyclic Redundancy Check

Introduction

- What if the transmitted bits get altered on the way?
  - Is there any technique to detect the error?

Yes, using Cyclic Redundancy Check (CRC)

- CRC
  - In CRC, some redundant bits are sent in addition to the message bits.
  - The purpose of the redundant bits is to facilitate detecting error.
  - *The redundant bits are called frame check sequence (FCS)*

How is FCS generated?

Cyclic Redundancy Check….

Introduction….

- Strength of the CRC depends on the number of redundant bits (that is, FCS length)
- Longer FCS length results in better accuracy in detecting error

❑ Required two sequence

- *Message sequence, M*
  - The desired data to be sent
  - Can be of any length
- *Pattern sequence, P*
  - Known to both sender and receiver
  - If we want to use *K* bits FCS, we need a pattern bit sequence, *P*, of length *K+1* bits.

Hello

1011010

say additional

Cyclic Redundancy Check….

Generation of FCS

1. Decide how many FCS bits, K, you are going to use.
2. Append K zeros at the end of the message bits to generate $M+K$ bits long sequence S.
3. Select a $K+1$ bits long pattern sequence, P.
4. Divide the sequence S by the pattern sequence P to find the K bits of the remainder, R.
5. Remove the appended zeros from S and append the calculated remainder R Thus, the N bits message bits and K bits remainder constitutes the transmitting sequence, T.

Cyclic Redundancy Check….

Error detection at the receiver

1. At the destination, the received sequence, T', is divided by the same patter sequence, P.
2. If at this step there is no remainder, the data unit is assumed to be correct and is therefore accepted.
3. A remainder indicates that the data unit has been damaged on the way and therefore must be rejected.

Cyclic Redundancy Check….

Error detection at the receiver

$\overset{4}{1}\ \overset{3}{0}\ \overset{2}{1}\ \overset{1}{0}\ \overset{0}{0}$

represent it in polynomial

$x^4 + x^3 + x^2 + x^1 + x^0$

remove remove

$\boxed{x^4 + x^2}$

$\overset{5}{1}\ \overset{4}{1}\ \overset{3}{1}\ \overset{2}{0}\ \overset{1}{0}\ \overset{0}{1}$

$x^5 + x^4 + x^3 + x^0$

$= x^5 + x^4 + x^3 + 1$

$x^0 = 1$

$x^5 + x^4 + x^3 + 1 =$

$1\ 1\ 1\ 0\ 0\ 1$

$x^1 = x$

$x^0 = 1$

Cyclic Redundancy Check….

Example 1

sender

Pattern polynomial

- Generate FCS if the message polynomial and generator polynomial are $X^3 + X^2 + 1$ And $X^3 + X + 1$, respectively.

is known to the sender & receiver

Let M(x) be the **message polynomial**

Let P(x) be the **generator polynomial/Pattern sequence**

Let $P(x) = X^3 + X + 1 \longrightarrow$ **1 0 1 1**

Let $M(x) = X^3 + X^2 + 1 \longrightarrow$ **1 1 0 1**

is P's length or (n-1) additional bits will be sent.

1. Consider the case where M=*1101 and P=1011.*
2. *Since P consists of 4 bits, append K=3 bits zeros (000) at the end of M, S=1101000*
3. *Divide S by P to get 3 bits remainder.*

M n-1 zero

P = 4 bits or length = 4 - 1 = 3 bits

Cyclic Redundancy Check….

Example 1

At sender

```
                 1111
            ___________
P → 1011   |  1101000   ← S
              1011
              ------
               1100
               1011
               ------
                1110
                1011
                ------
                 1010
                 1011
                 ------
                  001   ← R
```

Transmit sequence or codeword

T = 1 1 0 1 0 0 1

Same bit = 0

Different bit = 1

1101

FCS

1101001

codeword

Transmit sequence

```
        1111
1011 | 1101000
       1011
       ----
        1100
        1011
        ----
         1110
         1011
         ----
          1010
          1011
          ----
           001
```

1101001

Cyclic Redundancy Check….

Example 1

At Receiver

```
1011 | 1 1 0 1 0 0 1
       1 0 1 1
         1 1 0 0
         1 0 1 1
           1 1 1 0
           1 0 1 1
             1 0 1 1
             1 0 1 1
             0 0 0 0
```

1101001 → channel → 1101001

P

correct received sequence

zero remainder indicates error free reception

Since the remainder is zero, there is no error in the received sequence

Cyclic Redundancy Check….

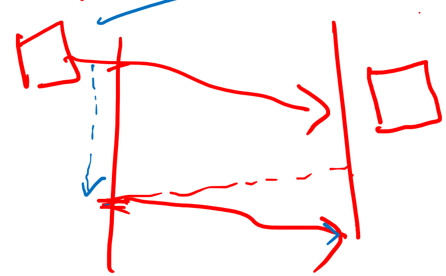
Example 1

1101001

1001001

Sender

Receiver



What if any bit gets altered in the channel?

Suppose that the second bit (red) has altered from 1 to 0.

```
           1 0 1
1011 | 1 0 0 1 0 0 1
       1 0 1 1
       -------------
         1 0 0 0
         1 0 1 1
       -------------
       0 0 1 1 1
```

≠ 000

The nonzero remainder indicates an erroneous reception.

The frame will not be acknowledged.

The sender will resend the frame.

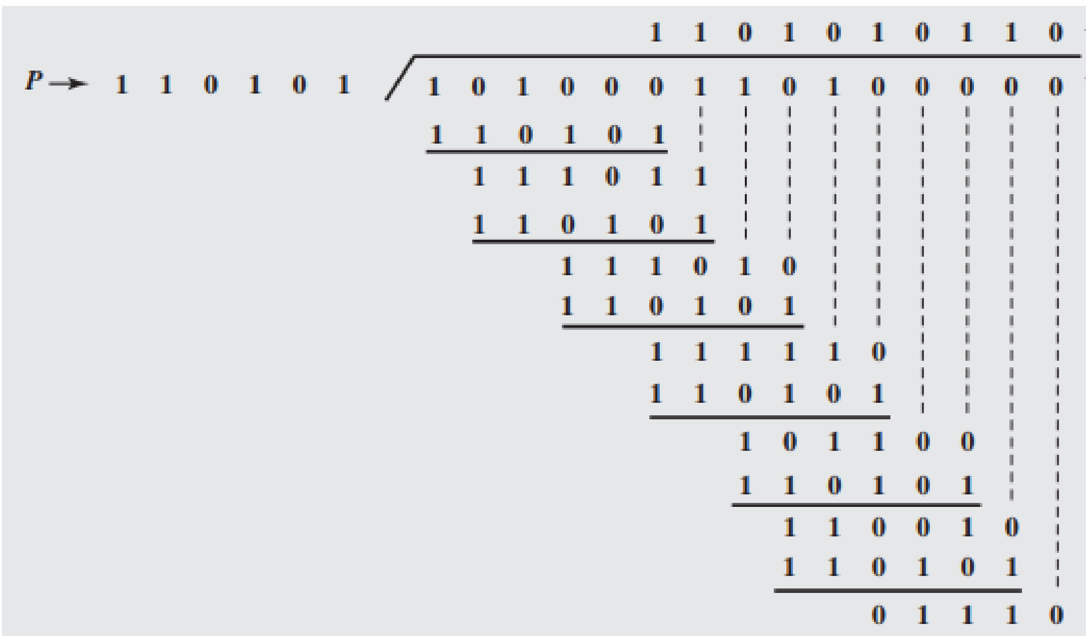
Cyclic Redundancy Check….

Example 2

- Message M = 1010001101
- Pattern P = 110101
  1 2 3 4 5 6
- Length of P=6
- Append K=6-1=5 zeros at the end of M
- S=101000110100000
- Now divide S by P to find 5 bits remainder [1].

Cyclic Redundancy Check….

Example 2



- Transmitted sequence, T=101000110101110
- At the receiving end, T is divided by P to see if the remainder is zero. The zero remainder indicates error free reception.

Cyclic Redundancy Check….

Example 1

```
                                1 1 0 1 0 1 0 1 1 0
                      ________________________________
P → 1 1 0 1 0 1    /  1 0 1 0 0 0 1 1 0 1 0 1 1 1 0
                      1 1 0 1 0 1
                      -----------
                        1 1 1 0 1 1
                        1 1 0 1 0 1
                        -----------
                            1 1 1 0 1 0
                            1 1 0 1 0 1
                            -----------
                                1 1 1 1 1 0
                                1 1 0 1 0 1
                                -----------
                                    1 0 1 1 1 1
                                    1 1 0 1 0 1
                                    -----------
                                      1 1 0 1 0 1
                                      1 1 0 1 0 1
                                      -----------
                                                0
```

Because there is no remainder, it is assumed that there have been no errors.

Homework

1. Detect whether the received sequence 101110101 is error free if the pattern sequence is 1010.

Linear Block Code

Generator Matrix

$M = 1011$; $k = 4$

$Q = 11$; $q = 2$

$\therefore n = 4+2 = 6$

Linear Block Code: A code in which addition of any two codewords gives another codeword [2].

Message, M: ✓ k bits long

Redundant bits, Q: q bits long

Codeword length, N: $k+q$ bits long

$P_{k\times q} = P_{4\times 2}$

$I_k = I_2$ Identity matrix $\begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}$

Example

Generator matrix, $G = [P_{k\times q} I_k]$

no. of rows

No. column

For $k = 3$ and $q = 3$,

$k = 3$

$q = 3$

$$P_{3\times 3} = \begin{bmatrix} 1 & 1 & 0 \\ 0 & 1 & 1 \\ 1 & 0 & 1 \end{bmatrix}$$

$$G = \begin{bmatrix} 1 & 1 & 0 & 1 & 0 & 0 \\ 0 & 1 & 1 & 0 & 1 & 0 \\ 1 & 0 & 1 & 0 & 0 & 1 \end{bmatrix}$$

$$I_3 = \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix}$$

Then, it is a (n, k) =(6, 3) block code

Linear Block Code….

Codeword calculation

The codeword for the message [0 1 1] is

$$C = M \times G$$

$$C = [0 \quad 1 \quad 1] \times \begin{bmatrix} 1 & 1 & 0 & 1 & 0 & 0 \\ 0 & 1 & 1 & 0 & 1 & 0 \\ 1 & 0 & 1 & 0 & 0 & 1 \end{bmatrix}$$

$$C = [\underbrace{1 \quad 1 \quad 0}_{Q} \quad \underbrace{0 \quad 1 \quad 1}_{M}]$$

codeword

Modulo-2 summation

$$0 \times 1 \oplus 0 \times 1 \oplus 1 \times 1 = 1$$

$$0 \times 1 \oplus 1 \times 1 \oplus 1 \times 0 = 1$$

$$0 \times 0 \oplus 1 \times 1 \oplus 1 \times 1 = 0$$

$$0 \times 1 \oplus 1 \times 0 \oplus 1 \times 0 = 0$$

$$0 \times 0 \oplus 1 \times 1 \oplus 1 \times 0 = 1$$

$$0 \times 0 \oplus 1 \times 0 \oplus 1 \times 1 = 1$$

$0 \times 1 \oplus 1 \times 1 \oplus 1 \times 0$

$0 \oplus 1 \oplus 0$

$1 \oplus 0$

1

$0 \times 1 \oplus 0 \times 1 \oplus 1 \times 1$

$0 \oplus 0 \oplus 1$

$0 \oplus 1$

1

xor

Linear Block Code….

Error-detection

Receiving end

$n = ?$

Parity check matrix,

$$H = [I_q \;\; P^T_{k\times q}]$$

$$H = [I_3 \;\; P^T_{3\times 3}]$$

$$H = \begin{bmatrix} 1 & 0 & 0 & 1 & 0 & 1 \\ 0 & 1 & 0 & 1 & 1 & 0 \\ 0 & 0 & 1 & 0 & 1 & 1 \end{bmatrix}$$

I_3

Square matrix

diagonal elements 1

I_3

$$P_{3\times 3} = \begin{bmatrix} 1 & 1 & 0 \\ 0 & 1 & 1 \\ 1 & 0 & 1 \end{bmatrix}$$

$$P^T_{3\times 3} = \begin{bmatrix} 1 & 0 & 1 \\ 1 & 1 & 0 \\ 0 & 1 & 1 \end{bmatrix}$$

$P^T_{3\times 3}$ is the transpose of $P_{3\times 3}$

$$H^T = \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \\ 1 & 1 & 0 \\ 0 & 1 & 1 \\ 1 & 0 & 1 \end{bmatrix}$$

Linear Block Code….

Error-detection….

110011 sent

channel

110011

Suppose that there is no error in the received sequence.

Hence the received sequence, r, is the same as the transmit sequence, C.

$$r = C$$

$$r = [1 \quad 1 \quad 0 \quad 0 \quad 1 \quad 1]$$

Syndrome, $s = rH^T$

$$s = [1 \quad 1 \quad 0 \quad 0 \quad 1 \quad 1] \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \\ 1 & 1 & 0 \\ 0 & 1 & 1 \\ 1 & 0 & 1 \end{bmatrix}$$

$$s = [0 \quad 0 \quad 0]$$

The all-zero syndrome indicates a correct reception !

$$H = \begin{bmatrix} 1 & 0 & 0 & 1 & 0 & 1 \\ 0 & 1 & 0 & 1 & 1 & 0 \\ 0 & 0 & 1 & 0 & 1 & 1 \end{bmatrix}$$

$$H^T = \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \\ 1 & 1 & 0 \\ 0 & 1 & 1 \\ 1 & 0 & 1 \end{bmatrix}$$

Linear Block Code….

Error-detection….

1 1 0 0 1 1

[1 0 0 0 1 1

error

Suppose that there is an error in the received sequence.

The second bit (from left side) has altered from 1 to 0

$r = [1 \quad 0 \quad 0 \quad 0 \quad 1 \quad 1]$

1

$1\times 1 \oplus 0\times 0 \oplus 0\times 0 \oplus 0\times 1 \oplus 1\times 0 \oplus 1\times 1$

$1 \oplus 0 \oplus 0 \oplus 0 \oplus 0 \oplus 1$

Syndrome, $s = rH^T$

$1 \oplus 1 = 0$

modulo 2 - addition

$2)2(1$

$\underline{2}$

0

$$s = [1 \quad 0 \quad 0 \quad 0 \quad 1 \quad 1]\begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \\ 1 & 1 & 0 \\ 0 & 1 & 1 \\ 1 & 0 & 1 \end{bmatrix}$$

$s = [0 \quad 1 \quad 0]$

The non-zero syndrome indicates an erroneous reception !

$0 \oplus 0 + 0 + 0 + 1 + 0 = 1$

Linear Block Code….

Error-correction

How to correct the error?

$$H^T = \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \\ 1 & 1 & 0 \\ 0 & 1 & 1 \\ 1 & 0 & 1 \end{bmatrix}$$

1. Syndrome , $s = [0 \quad 1 \quad 0]$
2. Locate the syndrome in H^T
3. It is in second row
4. So, the second element in the received sequence, $r = [1 \quad 0 \quad 0 \quad 0 \quad 1 \quad 1]$ is erroneous.
4. Alter the second bit from 0 to 1.
5. So the correct received sequence is [1 1 0 0 1 1].

Note: The given generator matrix enables correction of at most 1 bits.

It is possible to correct more bits , but it requires quite a lot work! No Free Lunch!

Homework

$H = [I_n \; P^T_{k\times n}]$

$G = [P_{k\times q} \; I_k]$

- Consider a (7, 4) code whose generator matrix is given by

$$G = \begin{bmatrix} 1 & 1 & 1 & 1 & 0 & 0 & 0 \\ 0 & 1 & 1 & 0 & 1 & 0 & 0 \\ 1 & 1 & 0 & 0 & 0 & 1 & 0 \\ 1 & 0 & 1 & 0 & 0 & 0 & 1 \end{bmatrix}$$

$k = 4$, $n = 3$

$CL = 4 + 3 = 7$

(a) Find all the codewords of the code

(b) Find the parity-check matrix

(c) Find the syndrome for the received vector [1 1 0 1 0 1 0]. Is it a valid codeword?

codeword for $[0\,1\,0\,1] = [0\,1\,0\,1] \times G$

$= [1\;0\;0\;0\;1\;0\;1]$

References

[1] W. Stallings, *Data and Computer Communication*, 10th ed., Pearson Education, Inc., 2014, USA, pp. 194 - 196.

[2] B. Sklar, *Digital Communications*, 2nd ed., Prentice Hall. 2017, USA, pp. 328 - 345.

modulo 5

0 - 4

$(1+0) \bmod 5 = 1 \bmod 5 = 1$

$(1+4) \bmod 5 = 5 \bmod 5 = 0$

$(2+3) \bmod 5 = 5 \bmod 5 = 0$

$(3+4) \bmod 5 = 7 \bmod 5 = 2$

Recommended Books

1. **Data Communications and Networking**, *B. A. Forouzan*, McGraw-Hill, Inc., Fourth Edition, 2007, USA.
2. **Computer Networking: A Top-Down Approach**, *J. F., Kurose*, *K. W. Ross*, Pearson Education, Inc., Sixth Edition, USA.
3. **Official Cert Guide CCNA 200-301 , vol. 1**, *W. Odom*, Cisco Press, First Edition, 2019, USA.
4. **CCNA Routing and Switching**, *T. Lammle*, John Wily & Sons, Second Edition, 2016, USA.
5. **TCP/IP Protocol Suite**, *B. A. Forouzan*, McGraw-Hill, Inc., Fourth Edition, 2009, USA.
6. **Data and Computer Communication**, *W. Stallings*, Pearson Education, Inc., Tenth Education, 2013, USA.