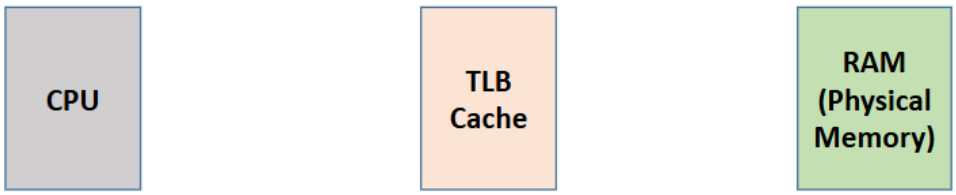
CSE 4509: Operating Systems
Class Test 3, Time: 1 hour

1. Consider a 64-bit system running an OS that uses hierarchical page tables to manage virtual memory. Assume that logical and physical pages are of size 4KB. The system has 8GB of physical RAM.Assume that each page table entry requires an additional 10 bits (beyond the frame number) to store various flags. Assume page table entries are rounded up to the nearest byte. Now answer the following questions:

   a) What is the size of the offset? [1]
   b) How many virtual pages are there in the virtual memory? [1]
   c) How many bits are required for a VPN? [1]
   d) How many bits are required for a PFN? [1]
   e) Find the size of a single page table. [2]
   f) What is the maximum number of levels in the page table of a process, including both the outermost page directory and the innermost page tables? [2]
   g) Design a multi level page table for the above virtual memory. [2]
   h) Calculate the maximum number of pages that may be required to store all the page table entries of a process across all levels of the page table. [3]

2. Consider the following block diagram:



   Using the block diagram, show what happens when the CPU generates a virtual address that causes a TLB miss. [3]

3. Imagine a computer system with a physical memory that can hold up to 4 pages. This system uses virtual memory management with a page replacement policy based on the Least Recently Used (LRU) algorithm. You are provided with a sequence of page references and **must simulate the behavior of the system as it processes this sequence.**

   The sequence of page references is as follows:
   3, 2, 3, 7, 0, 7, 3, 4, 2, 7, 4 **[4]**