

Q-1

Given,

$$\text{Virtual address} = 256 \text{ MB} = 2^{28} \text{ bytes}$$

$$\text{Page Size} = 2 \text{ KB} = 2^{11} \text{ bytes}$$

$$\text{Physical RAM} = 4 \text{ GB} = 2^{32} \Rightarrow \text{Physical Address} = 32 \text{ bits}$$

$$\text{Flash Size} = 7 \text{ bits}$$

$$\text{Maximum processes run} = 256$$

$$\textcircled{a} \text{ offset} = \log_2 (\text{page size in bytes}) = \log_2 (2^{11}) = 11 \text{ bits}$$

$$\textcircled{b} \text{ Number of virtual pages} = \frac{\text{Virtual memory size}}{\text{Page size}}$$
$$= \frac{2^{28}}{2^{11}} = 2^{17}$$

$$\text{Number of physical frames} = \frac{\text{Physical memory size}}{\text{Page size}}$$
$$= \frac{2^{32}}{2^{11}} = 2^{21}$$

Or,

$$\text{Physical frame no} = \text{Physical Address} - \text{Offset} = 32 - 11 = 21 \text{ bits}$$

③ Page table size = No. of virtual pages \times PTE size

$$= 2^{17} \times 4$$

$$= 2^{19} \text{ bytes}$$

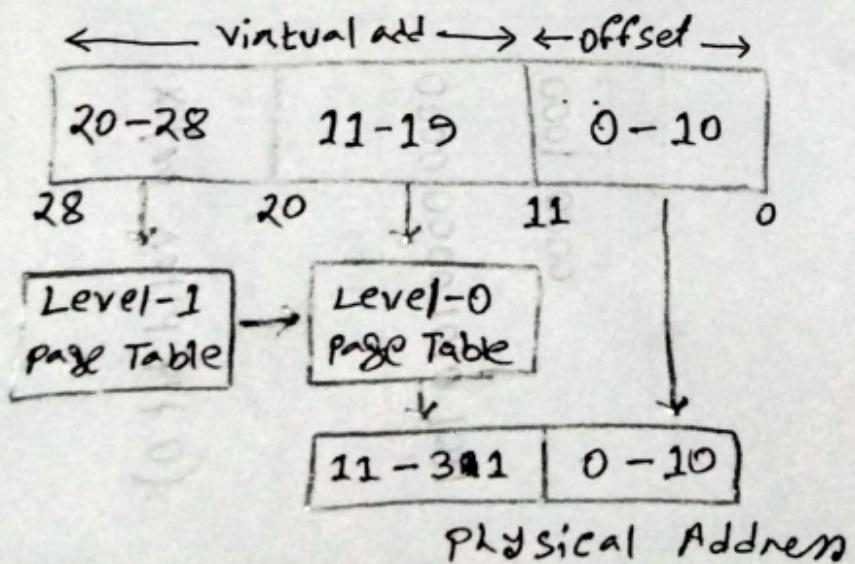
PTE size = PFN size + Flag size

$$= 2^1 + 7$$

$$= 28 \text{ bits} = \lceil 28/8 \rceil = 4 \text{ bytes}$$

④ Number of bits required at each level

$$= \left\lfloor \log_2 \left(\frac{\text{Page size}}{\text{PTE size}} \right) \right\rfloor = \left\lfloor \log_2 \left(\frac{2^{11}}{2^2} \right) \right\rfloor = 2^9 \\ = 9 \text{ bits}$$



(e) Number of pages required for each level

$$\text{Page table} = \left\lceil \frac{\text{No. of PTEs (Number of virtual pages)}}{\text{No. of PTEs per page}} \right\rceil$$

Now,

$$\begin{aligned}\text{Number of PTEs per page} &= \left\lfloor \frac{\text{Page Size}}{\text{PTE Size}} \right\rfloor \\ &= \left\lfloor \frac{2^{11}}{4} \right\rfloor = 2^9\end{aligned}$$

$$\text{For Level-0, space/pages required} = \left\lceil \frac{2^{17}}{2^9} \right\rceil = 2^8$$

$$\text{For Level-1, space/pages required} = \left\lceil \frac{2^8}{2^9} \right\rceil = 1$$

maximum memory space required to store the pages of all processes = $(2^8 + 1) \times 256$ pages

⇒

$$\begin{aligned}\text{(f) minimum memory space required to store the page tables of a process} &= \text{Number of levels} \times 1 \text{ page} \\ &= 2 \times 1 \\ &= 2 \text{ pages.}\end{aligned}$$

Q-2

- offset = **12 bits**
- Virtual address = 16 bits; \Rightarrow VPN = $16 - 12 = 4$ bits
- Physical address = 14 bits; \Rightarrow PFN = $14 - 12 = 2$ bits \Rightarrow **4 physical frames**
- Page size = **2^{12} bytes**

Access	Source (instruction · which add)	Virtual add (bin)	VPN (bin)	VPN (dec)	Hit/Miss	Memory State [Max 4]
1	Inst-1 (only add)	1100 1010 1001 1000	1100	12	Miss	[12]
2	Inst-2 (only add)	0011 1101 1011 1101	0011	3	Miss	[12, 3]
3	Inst-3 (add-1)	1101 0100 1010 0000	1101	13	Miss	[12, 3, 13]
4	Inst-3 (add-2)	1010 0110 0100 0100	1010	10	Miss	[12, 3, 13, 10]
5	Inst-4 (only add)	0001 0100 0101 0111	0001	1	Miss (evict=12)	[3, 13, 10, 1]
6	Inst-5 (add-1)	1100 1111 0101 1110	1100	12	Miss (evict=3)	[13, 10, 1, 12]
7	Inst-5 (add-2)	0111 0100 1101 0101	0111	7	Miss (evict=13)	[10, 1, 12, 7]
8	Inst-6 (only add)	1110 0001 1111 1111	1110	14	Miss (evict=10)	[1, 12, 7, 14]
9	Inst-7 (only add)	0111 0101 0010 0100	0111	7	Hit	[1, 12, 14, 7]
10	Inst-8 (only add)	1010 1100 1111 0111	1010	10	Miss (evict=1)	[12, 14, 7, 10]

11	Inst-9 (add-1)	0000 1101 0110 1110	0000	0	Miss (evict=12)	[14, 7, 10, 0]
12	Inst-9 (add-2)	1111 0000 1111 0000	1111	15	Miss (evict=14)	[7, 10, 0, 15]
13	Inst-10 (add-1)	1111 1111 1111 1111	1111	15	Hit	[7, 10, 0, 15]
14	Inst-10 (add-2)	0101 0101 0101 0101	0101	5	Miss (evict=7)	[10, 0, 15, 5]

Q-4

Process	Allocation				Max				Available				Need				Safe State	
	A	B	C	D	A	B	C	D	A	B	C	D	A	B	C	D		
T0	3	0	1	4	5	1	1	7	0	3	0	1	2	1	0	3	T2	
T1	2	2	1	0	3	2	1	1	3	4	2	2	1	0	0	1	T1	
T2	3	1	2	1	3	3	2	1	5	6	3	2	0	2	0	0	T3	
T3	0	5	1	0	4	6	1	2	5	11	4	2	4	1	0	2		
T4	4	2	1	2	6	3	2	5					2	1	1	3		

T4 is not in safe state

Maximum number of additional available resources required = {0, 0, 0, 1}