BANGLADESH UNIVERSITY OF ENGINEERING AND TECHNOLOGY
DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING

EEE 466 (January 2023)

Analog Integrated Circuit Laboratory

Final Project Report

Section: G2 Group: 07

Designing a 8:1 Analog Multiplexer

Course Instructors:

Dr. Muhammad Abdullah Arafat, Assistant Professor
Nafis Sadik, Lecturer

Signature of Instructor: _____

Academic Honesty Statement:

IMPORTANT! Please carefully read and sign the Academic Honesty Statement, below. Type the student ID and name, and put your signature. *You will not receive credit for this project experiment unless this statement is signed in the presence of your lab instructor.*

"In signing this statement, We hereby certify that the work on this project is our own and that we have not copied the work of any other students (past or present), and cited all relevant sources while completing this project. We understand that if we fail to honor this agreement, We will each receive a score of ZERO for this project and be subject to failure of this course."

Signature: _____ **Full Name: Md. Ayenul Azim** **Student ID: 1806089**	**Signature:** _____ **Full Name: Saif Ahmed Sunny** **Student ID: 1806097**
Signature: _____ **Full Name: Shahriar Khan Roudra** **Student ID:1806092**	**Signature:** _____ **Full Name: Shahriar Ahmed** **Student ID: 1806192**

Table of Contents

1 Abstract

This project aims to design, implement, and analyze the functionality of an 8-to-1 multiplexer circuit. They serve the purpose of selecting one of the eight input data lines and forwarding it to a single output line based on the control inputs. This project focuses on creating a multiplexer with eight data inputs(A,B,C,D,E,F,G,H), one output, and three control inputs (S0,S1,S2) for selecting the desired input line.

The project involves the following key components and steps:

1. Circuit Design: Designing the logic gates and interconnections required to construct the 8-to-1 multiplexer circuit. The design process includes defining the truth table and logical equations for the MUX based on the control inputs.

2. Component Selection: Choosing appropriate digital logic components such as AND gates, OR gates, NOT gates, and flip-flops to implement the designed circuit.

3. **Schematic**: Creating a schematic diagram of the multiplexer circuit using a software tool like Cadence(virtuoso).

4. Simulation: Using simulation software like Cadence(virtuoso) to verify the functionality of the designed circuit and ensure that it performs as expected under different input conditions.

5. Testing and Verification: Conducting various tests to validate the multiplexer's operation, including input combinations and control signals to ensure correct data selection.

6. Analysis and Performance Evaluation: Analyzing the multiplexer's performance in terms of speed, power consumption, and signal integrity.

2 Introduction

A multiplexer is a fundamental digital electronic circuit that plays a crucial role in data routing and selection within digital systems. It enables the selection of one of several input data signals and routes it to a single output based on a set of control signals. Multiplexers are widely used in various applications, including data communication, memory access, and arithmetic operations.

One common implementation of a multiplexer is using transmission gates, a configuration that leverages the principles of digital logic and analog electronics to efficiently switch between input signals. Transmission gates, also known as pass gates or analog switches, offer several advantages when used in multiplexers:

1. Low Resistance Path: Transmission gates provide a low-resistance path for the selected input signal to pass through, minimizing signal degradation and loss. This is particularly important for high-speed digital signals.

2. Bidirectional Operation: Transmission gates can be used for both data selection and data demultiplexing, making them versatile components in digital circuits.

3. Minimal Propagation Delay: Transmission gates typically introduce minimal propagation delay, making them suitable for applications requiring fast switching and minimal latency.

4. Wide Voltage Range: Transmission gates can handle a wide range of input voltage levels, making them compatible with various digital logic families.

The core concept behind a multiplexer using transmission gates is the use of complementary transmission gate pairs controlled by the same set of control signals. When the control signal is active, one transmission gate in the pair conducts (i.e., it's "on"), while the other is in the non-conducting state (i.e., it's "off"). This selective switching of transmission gates allows the chosen input signal to pass through while blocking the others.

3 Design

3.1 Design Method

The steps that we have followed in order to build an analog 8to1 multiplexer are given below:

1. **Selector Block**: We have designed an instance named "selector" containing diode connected MOS, inverter & amplifier. This instance converts selector pin logic high (1.4V) into 3V and logic low(0V) into -3V.The output of the selector block used to bias the MOSFETs of the transmission gate.

2. **Transmission Gate**: It is designed to implement the pass transistor logic. It consists of a PMOS and a NMOS connected in parallel combination. PMOS conducts in positive half cycle and NMOS conducts in negative half cycle. The name we have given is trans_gate in the cadence.

3. **2to1 Multiplexer:** Another instance named "2to1" was created using the selector block,CMOS inverter and transmission gate. It will be the fundamental block of the complete circuit.

4. **8to1 Multiplexer:** Finally, 8to1 multiplexer is designed by interconnecting seven 2to1 multiplexer. Then an instance was created for further analysis and verification.

3.2 Circuit Diagram

Selector Block:

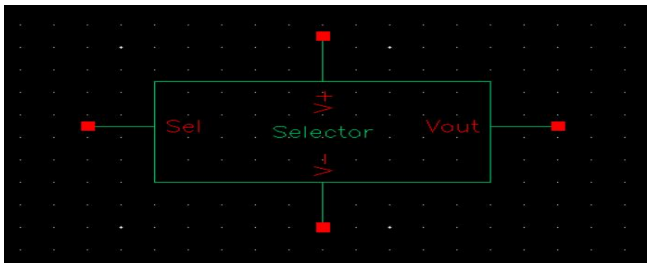


Fig1: Selector block

The above circuit diagram converts Selector pin (S0,S1,S2) logic high (1.4V) to 3V and logic low(0V) to -3V.The output of the selector block used to bias the MOSFETs of the transmission gate. The block contains diode connected loads, CMOS inverter and amplifier.

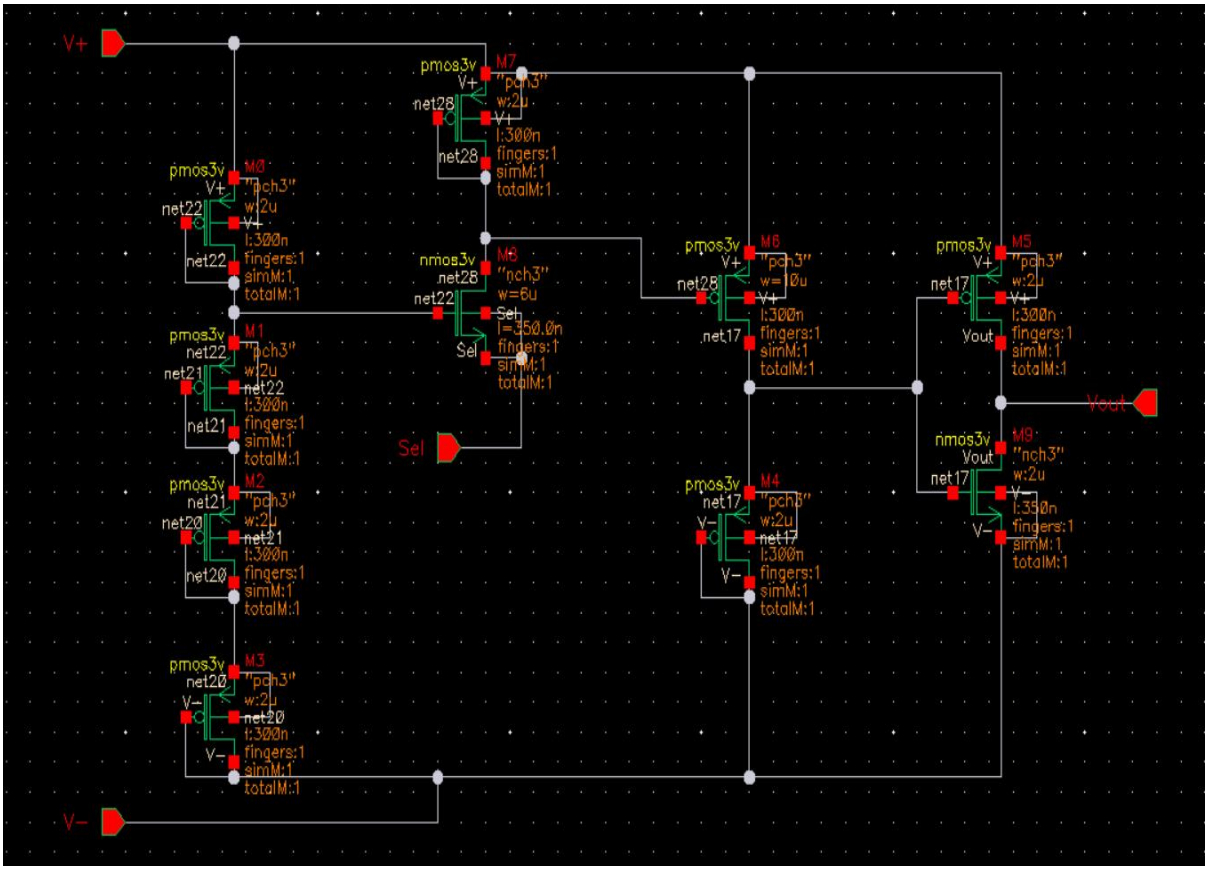
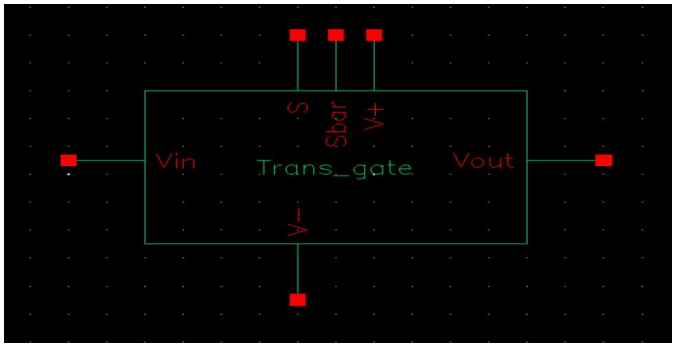


Fig2: Circuit diagram of Selector block

The diode connected load acts as resistors, which is used as voltage divider. The voltage at the drain of PMOS M0 is 1.5V, which is used to bias the NMOS M8, which acts as common gate amplifier. When we give input voltage of 1.4V into the source of the M8, M8 turns off. M7 PMOS then drives the voltage fromm V+ to M6 PMOS. In this stage , we get -3V for 1.4V input. So, we have used CMOS inverter in order to get the desired +3V voltage. Similar process happens when we put 0V into the source of the M8 NMOS. It's output is 3V when selector pin is in logic high state (1.4V) and 0V when selector pin is in logic low state (0V). It is fed into an common source amplifier following an inverter, which gives output of 3V and -3V respectively for Selector pin voltage 1.4V and 0V.

Transmission Gate:



Pass transistor logic is based on the use of transmission gates, also known as pass gates or pass transistors. These gates consist of complementary pairs of n-type and p-type MOSFET. A transmission gate allows signals to pass through when control signals are active, effectively acting as an " Analog switch."

Fig3: Transmission Gate Block

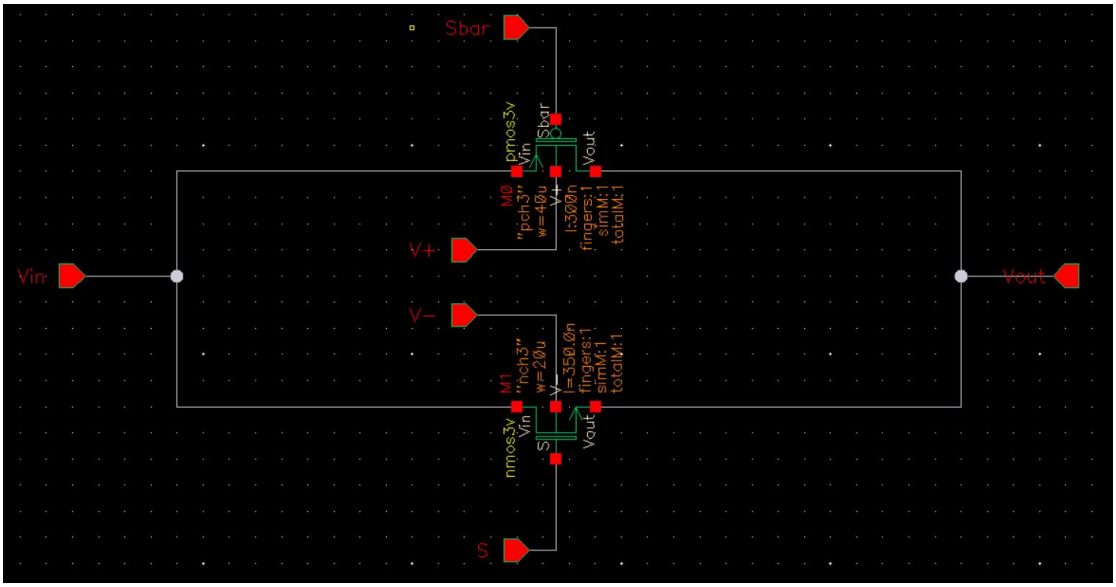


Fig4: Transmission Gate Circuit

When the control signal is high (logic 1), the NMOS transistor turns on (becomes conducting). This means that a low-resistance path is established between the input and the output of the transmission gate. As a result, signals can freely pass from the input to the output with minimal voltage drop and signal degradation. Same principle applies for PMOS when the control signal is low (logic 0).

2to1 Multiplexer:

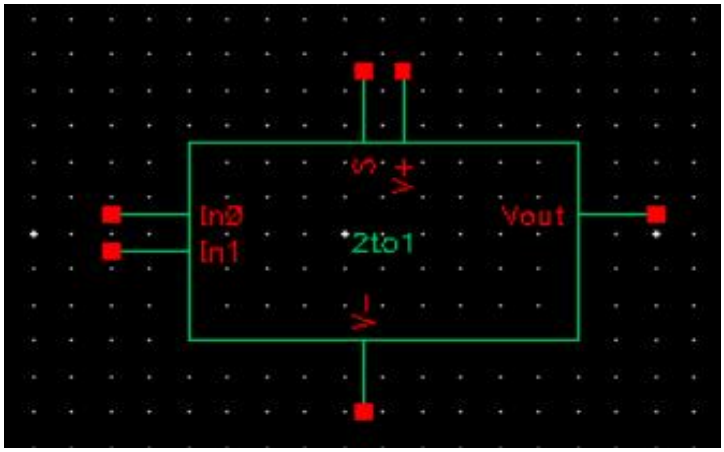


Fig5: 2:1 MUX Block

The 2:1 multiplexer is designed as a building block of our 8:1 Multiplexer.

The block is designed with 2 input pins, 1 selector pin and one output pin. It has biasing pin to bias the transistors inside.

The multiplexer chooses In0 or In1 when the S value is 0 or 1 respectively.

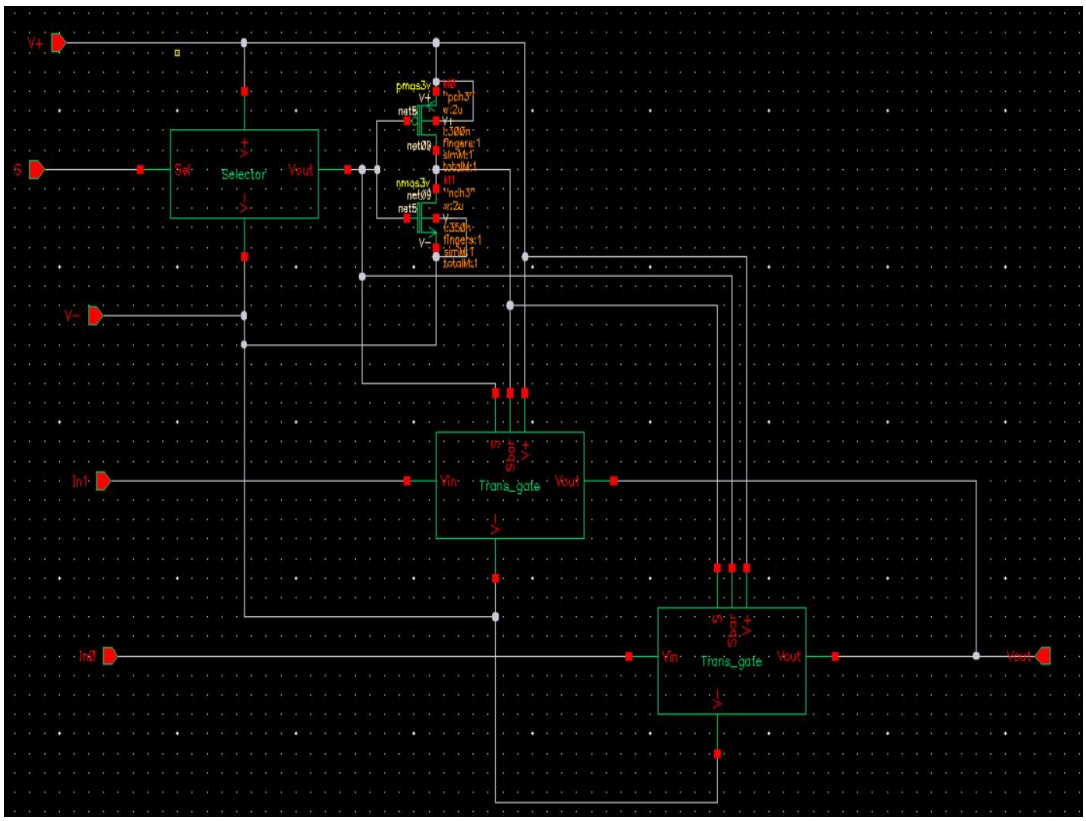


Fig6: 2:1 Multiplexer Circuit

The 2-to-1 multiplexer (MUX) is implemented using pass transistor logic (PTL) with a pair of transmission gates. In this configuration, two transmission gates are used to select one of two data inputs and pass it to the output based on a control signal. CMOS inverter were used to generate Sbar from the S output of the selector block.

When the control signal S is high (1), it enables the first transmission gate (TG1), At the same time, it disables the second transmission gate (TG2). With TG1 enabled and TG2 disabled, data input I0 is connected to the MUX output (Out) through TG1. Therefore, when S is high, the output carries the value of I0. Conversely, when the control signal S is low (0), it disables TG1 and enables TG2. This configuration connects data input I1 to the MUX output. When S is low, the output carries the value of I1.

The MUX-Out provides the selected data input (either I0 or I1) based on the state of the control signal S.

Control Signal, S	Input, I0	Input, I1	Output
0	X	X	I0
1	X	X	I1

8to1 Multiplexer:

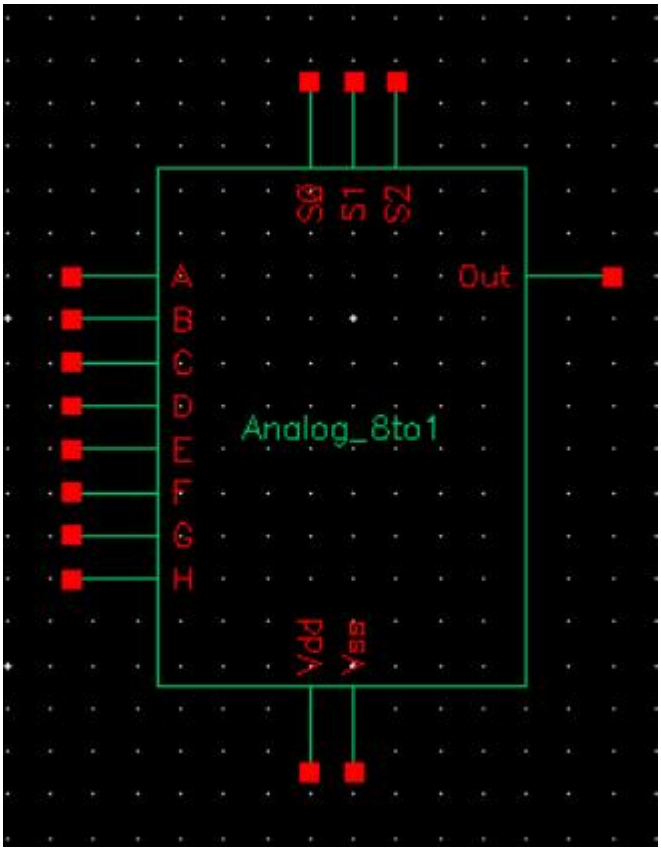


Fig7: 8:1 MUX Block

This is the final block diagram of the 8:1 analog multiplexer circuit. The block is designed with 8 input pins (A, B, C, D, E, F, G, H), 3 selector pins (S0, S1, S2) and one output pin. It has biasing pins (Vdd, Vss)to bias the transistors inside.

The multiplexer chooses input A through H when the S value varies from 000 to 111.

S0	S1	S2	Input	Output
0	0	0	X	A
0	0	1	X	B
0	1	0	X	C
0	1	1	X	D
1	0	0	X	E
1	0	1	X	F
1	1	0	X	G
1	1	1	X	H

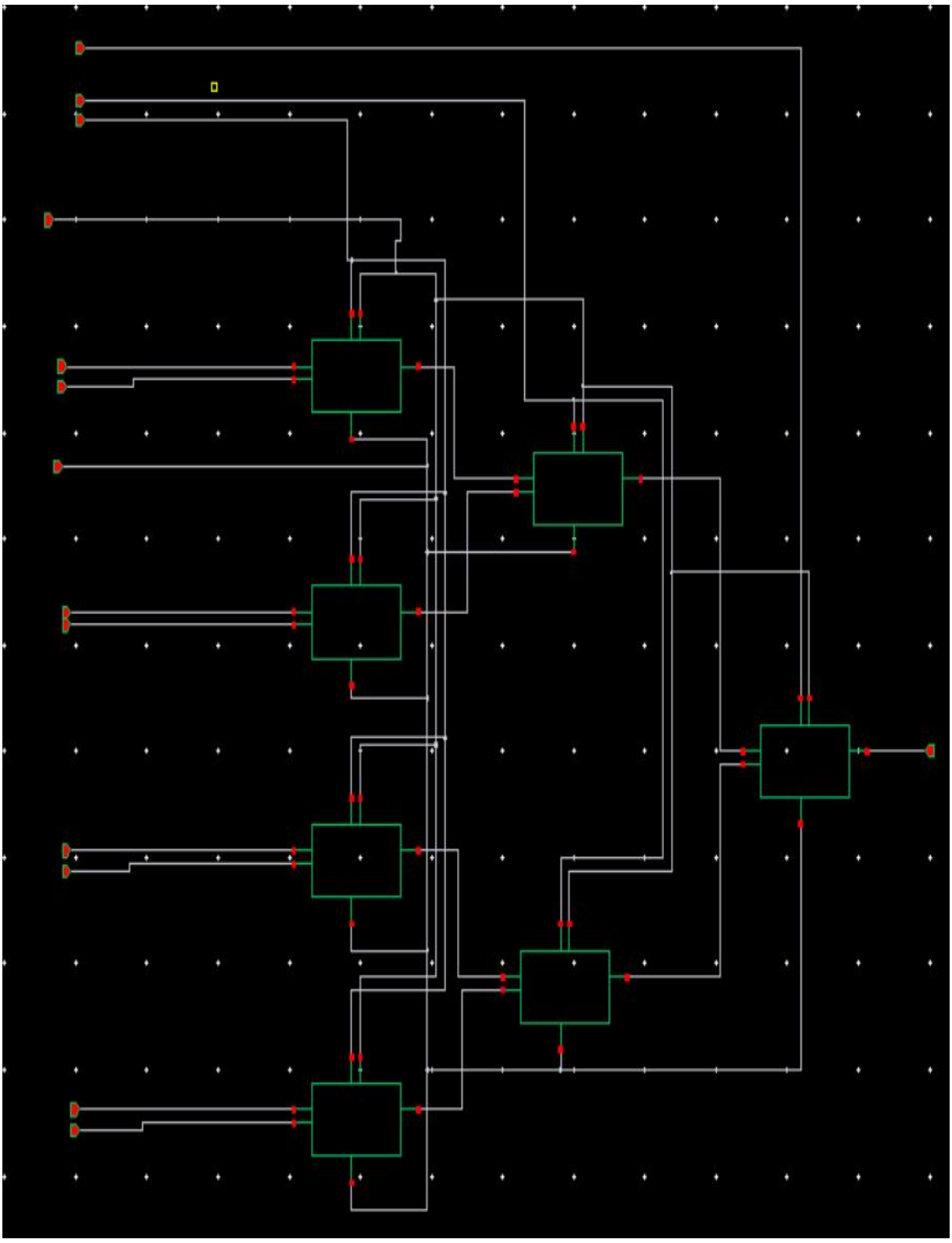


Fig8: 8:1 MUX Circuit Connection

The 8-to-1 multiplexer (MUX) is designed using 2-to-1 MUXes as building blocks. This approach is known as hierarchical design.

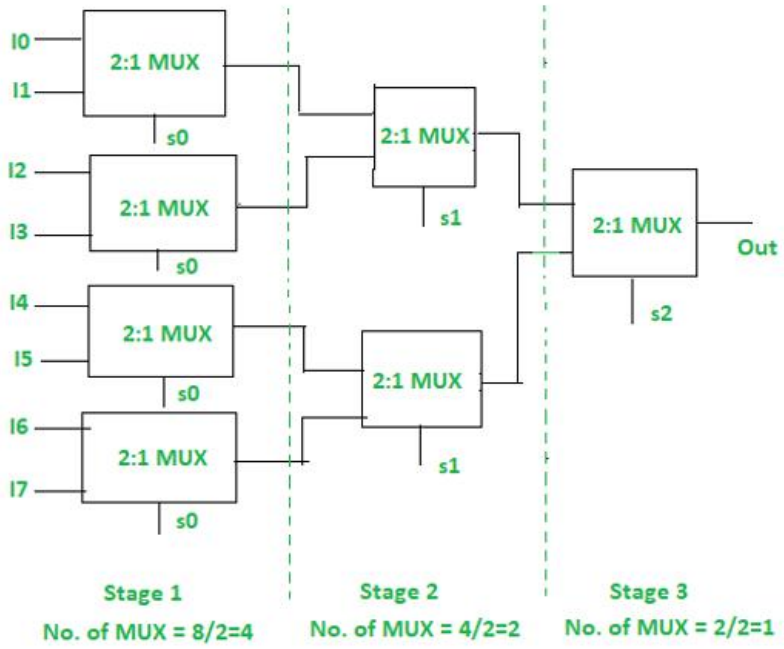


Fig9: 8:1 MUX Block by Block Circuit Connection

The 8-to-1 MUX uses three control signals, S0, S1, and S2, to select one of the eight 2-to-1 MUXes as the output path. The MSB bit of the selector bits is S0 and LSB is S2. S2 is applied to the four 2to1 MUX stage and S0 is applied to the last 2to1 MUX.

4 Analysis and Evaluation

4.1 Output Based on Selector Pin

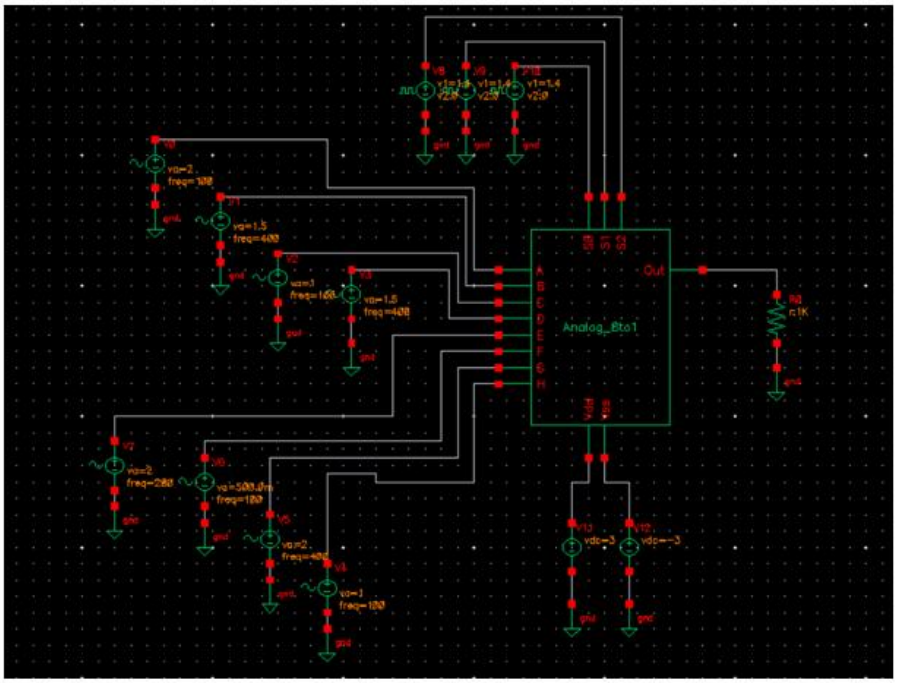


Fig10: Circuit Connection for output

Fig11: Output Signals for different selector pins

5 Specifications

5.1 Given Specifications

Supply Voltage	+/-3	V
Logic High Level	1.4	V
Logic Low Level	0	V
Input Capacitance (max)	50	pF
Charge Injection over the full signal swing range (max)	5	pC
Switching On time (t_{ON})(at R_L = 1k Ω, C_L = 10 pF) (max)	100	ns
Analog Signal Range	-2 to 2	V
Power Dissipation (max)	10	mW
On-Resistance	10	Ω
Bandwidth, -3 dB	1	MHz

Fig12: Given Specifications

5.2 Supply Voltage (Required +/-3 V)

We have biased the selector block circuit with V_{dd} = 3V and V_{ss} = -3V. And all the other circuits were biased with the selector block output. So, This specification is met.

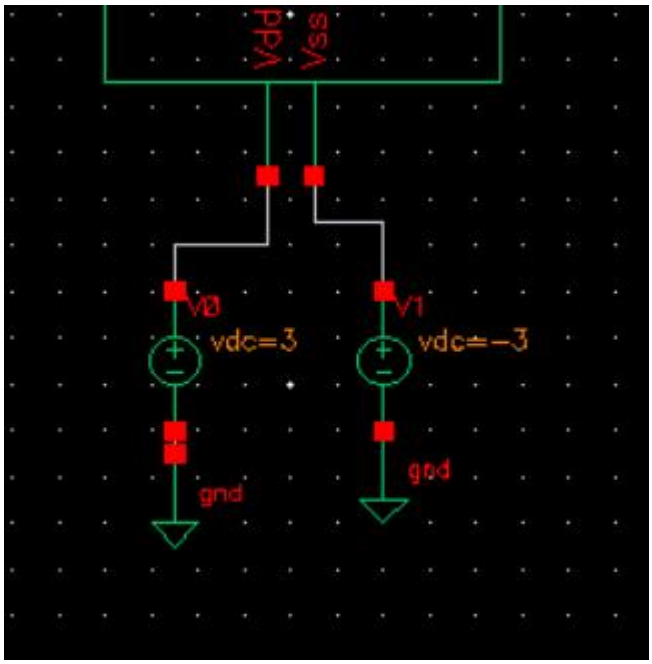


Fig13: Bias Voltages (+/-3 V)

5.3 Logic High Level (Required 1.4V)

By the "Selector Block", logic level high and low (1.4V and 0V) is converted to +/-3V. This voltage is used to bias the circuit to get the required signal swing.

5.4. Logic Low Level (Required 0V)

By the "Selector Block", logic level high and low (1.4V and 0V) is converted to +/-3V. This voltage is used to bias the circuit to get the required signal swing.

So, 1.4V is logic high and 0V is logic low. This two specifications are is met.

5.5 Input Capacitance (Required 50pF max)

Circuit Setup

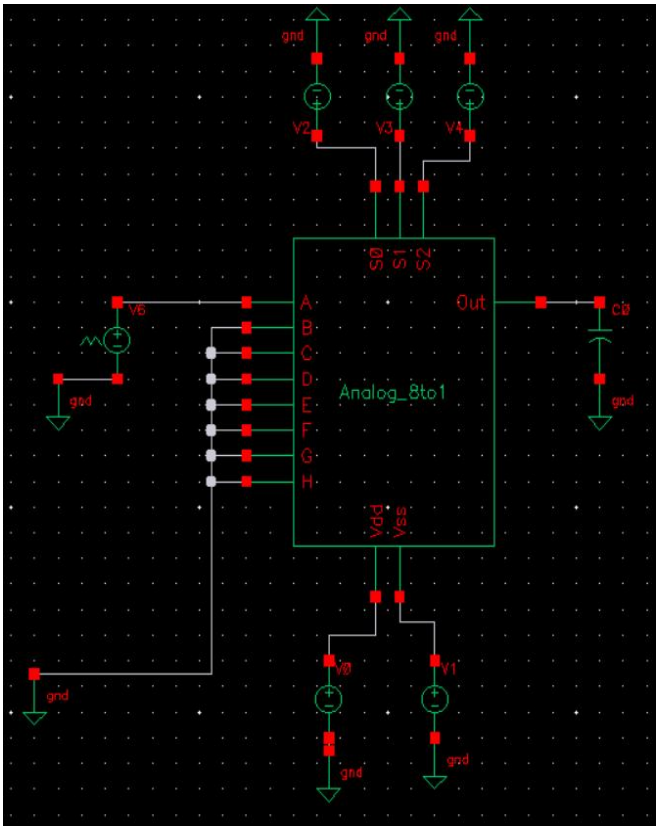


Fig14: Circuit setup for input capacitance

In order to calculate the input capacitance, we have used V_{pwl} from 'analoglib' library as our input(A). All the other inputs were shorted out to ground and selector bits were 000 to get pass the signal from A to output. Then we have conducted DC analysis. From ADE L , we have selected calculator. Then using special function "integ", we have integrated the input current from the source with respect to time. Limit of the integral is shown below. This has given us the charge. After that we got our required "input capacitance" by dividing it with the DC amplitude of the V_{pwl} source voltage.

Result

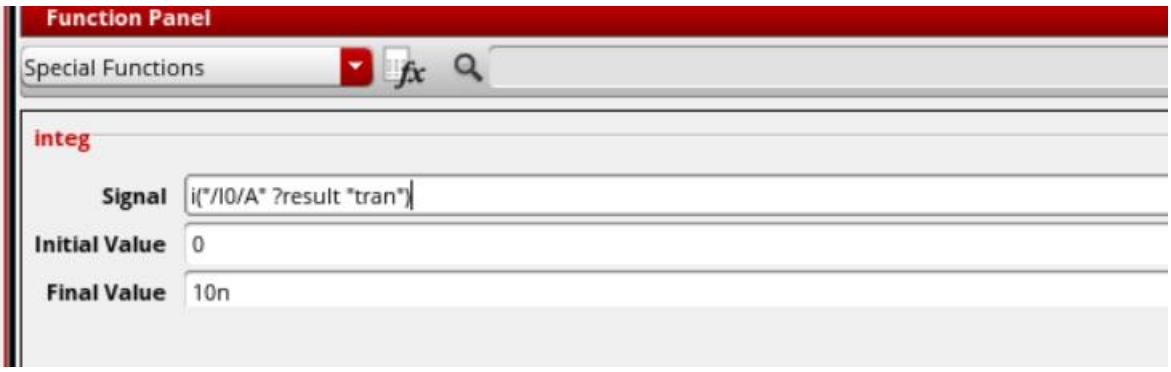


Fig15:Calculating Cin(Integral limit)

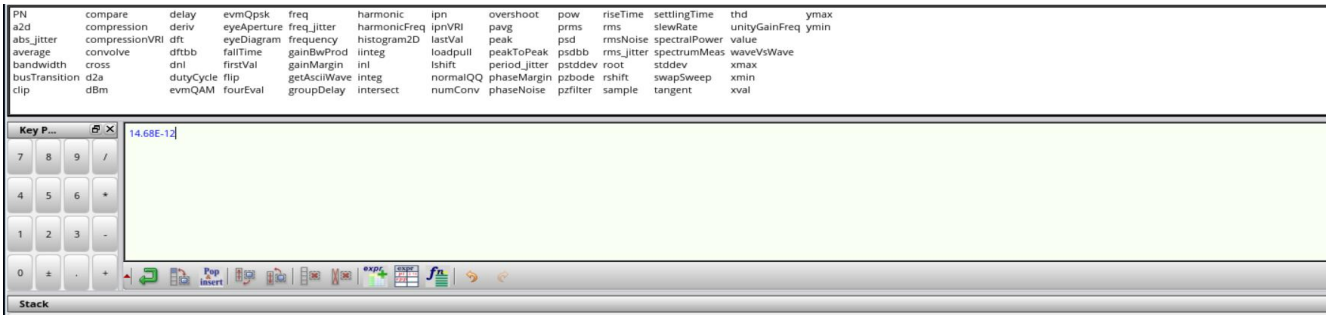


Fig16: Input Capacitance

Input capacitance is found 14.68 pF < 50pF. So, the requirement is satisfied.

5.6 Charge injection over the full signal swing range (Required 5pC max)

We could not formulate suitable circuit in order to calculate the charge injection of the circuit.

5.7. Switching on time (t_{ON}) at RL = 1k and CL = 10pF (Required 100ns max)

Circuit Setup

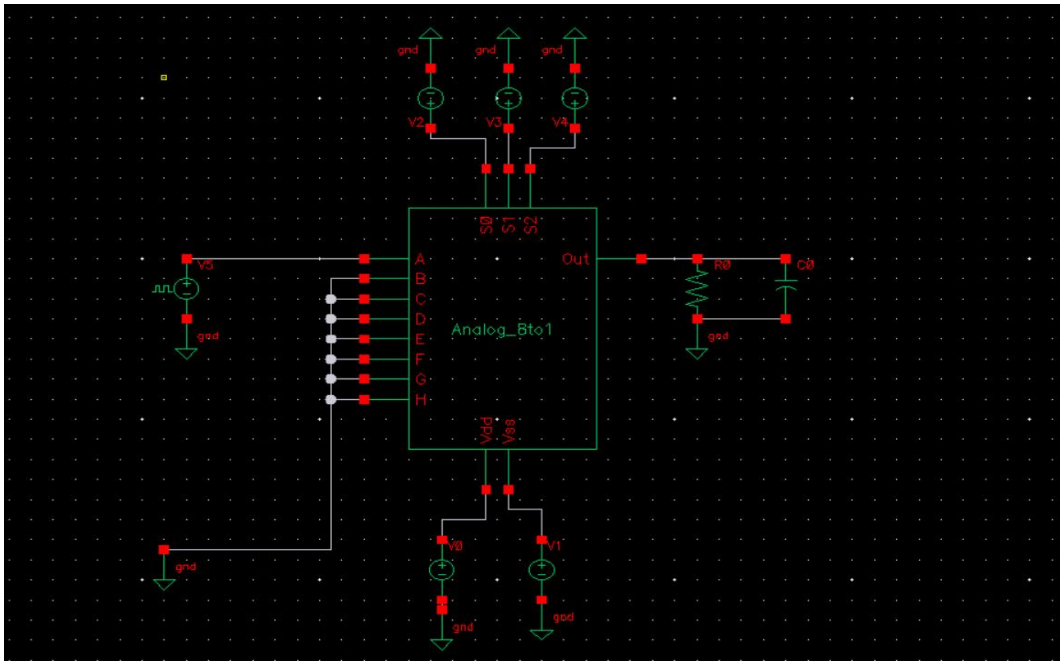


Fig17: Circuit Setup for calculating switching on time

Here we have used V_{pul} as our input voltage. R_L and C_L were also connected in parallel at the output node. We have plotted the output voltage using transient analysis in the ADE L window. From the graph, we can see that the time it takes to reach 10% of the final voltage value is close to 2ns. This is our desired switching on time.

Our circuit performed far better than the given specification sheet(almost 250 times better).

Result

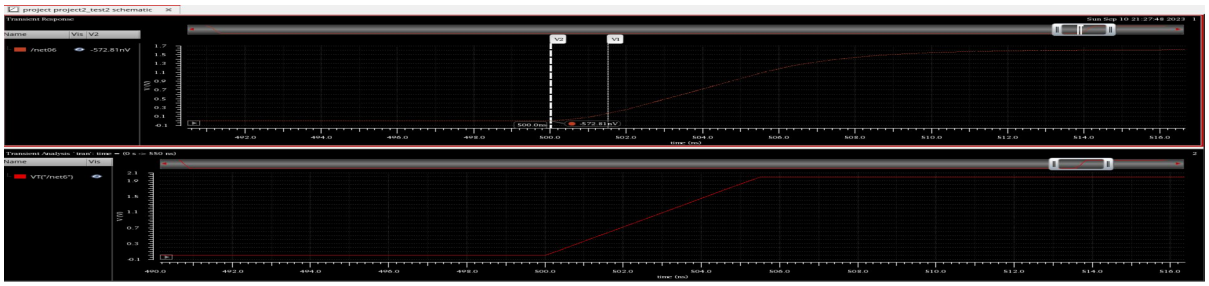
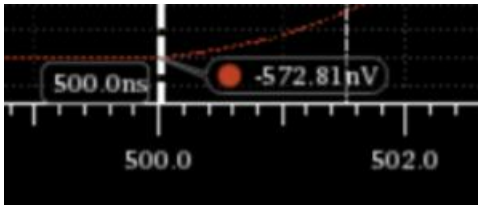


Fig18: Calculating switching in time



t_{ON} is found around 2ns < 100ns.
So, this specification is satisfied.

5.8 Analog Signal Range (Required -2V to +2V)

We have tested the circuit by giving sinusoidal input with amplitude 2V peak or below and the circuit works. The output follows the input but is a little attenuated due to the voltage in the on resistance of the channel. We have found that we got 1.6 voltage peak when we had given 2V peak analog input.

5.9 Power Dissipation (Required 10mW max)

Circuit Setup

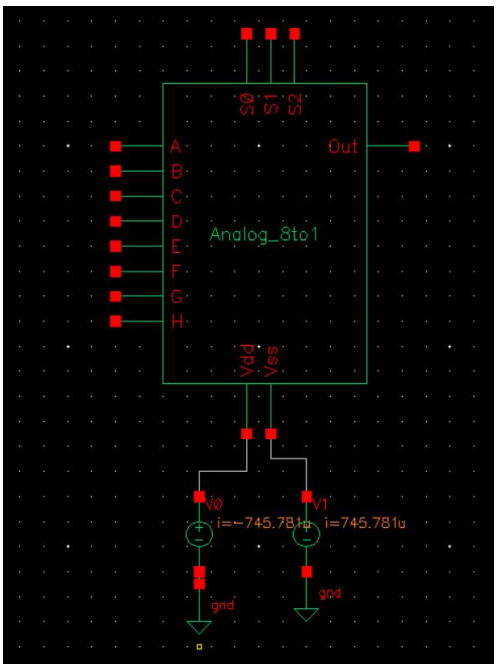


Fig19: Circuit Setup for power dissipation calculation

For this verification, we have given high impedence input to all inputs and selector pins of the MUX. The output is also kept at high impedence. Then we have taken current value by doing DC analysis in the ADE L from the bias voltage sources. Power calculation were given below.

Result

Power dissipation = V_{dd}*I_{dd} + V_{ss}*I_{ss} = 4.47 mW

So, Power dissipation < 10mW. This specification is met.

5.10 Bandwidth, -3dB (Required 1MHz)

Circuit Setup

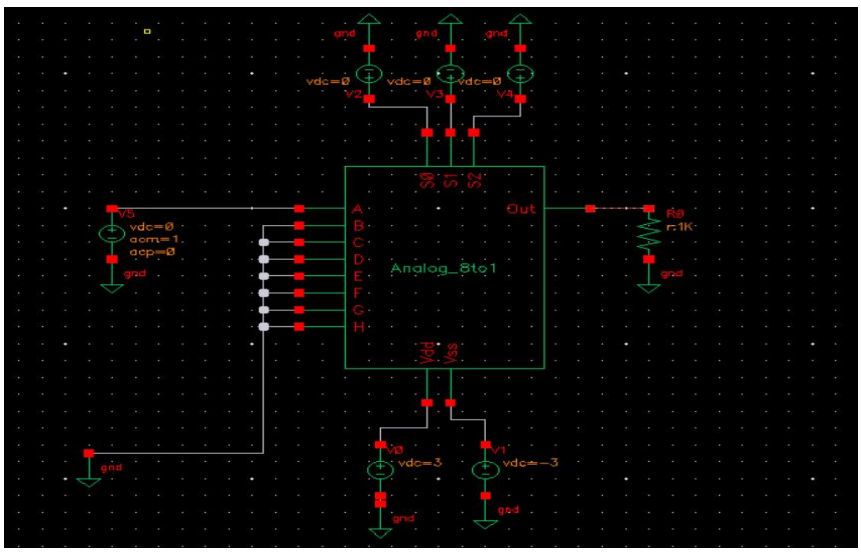


Fig20: Circuit Setup for power bandwidth calculation

For this analysis, we have taken ac voltage with magnitude 1 and plotted ac sweep(Output Voltage vs

Frequency). The plot is shown below. Our -3dB bandwidth is 1.72 GHz which is far better than required specifications. Our MUX can used in high speed applications.

Result

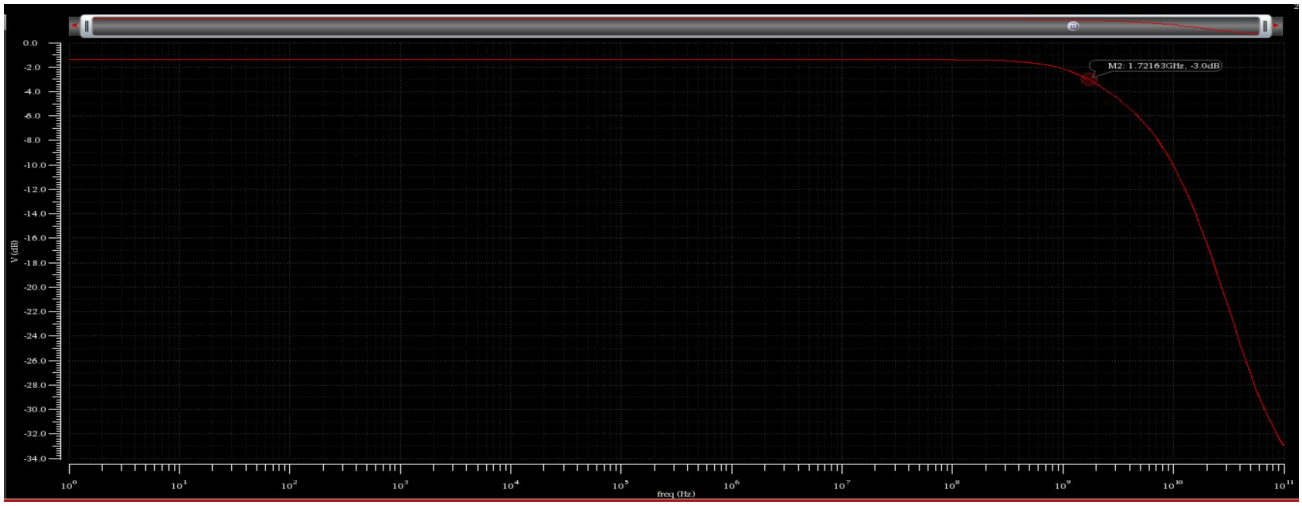
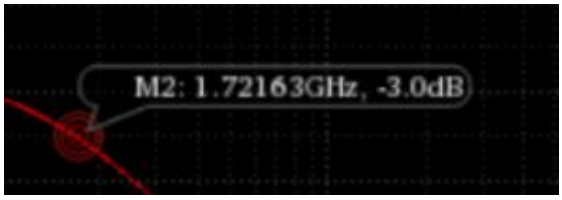


Fig 21:Frequency Sweep plot



The -3dB bandwidth is found 1.72 GHz.

So, the specification is satisfied.

5.11 On Resistance

In order to calculate on resistance, we have conducted DC analysis and got node voltage values from the schematics. The formula we have used for this is

$$R_{ON} = (v_{out} - v_{in})/i_{out}$$

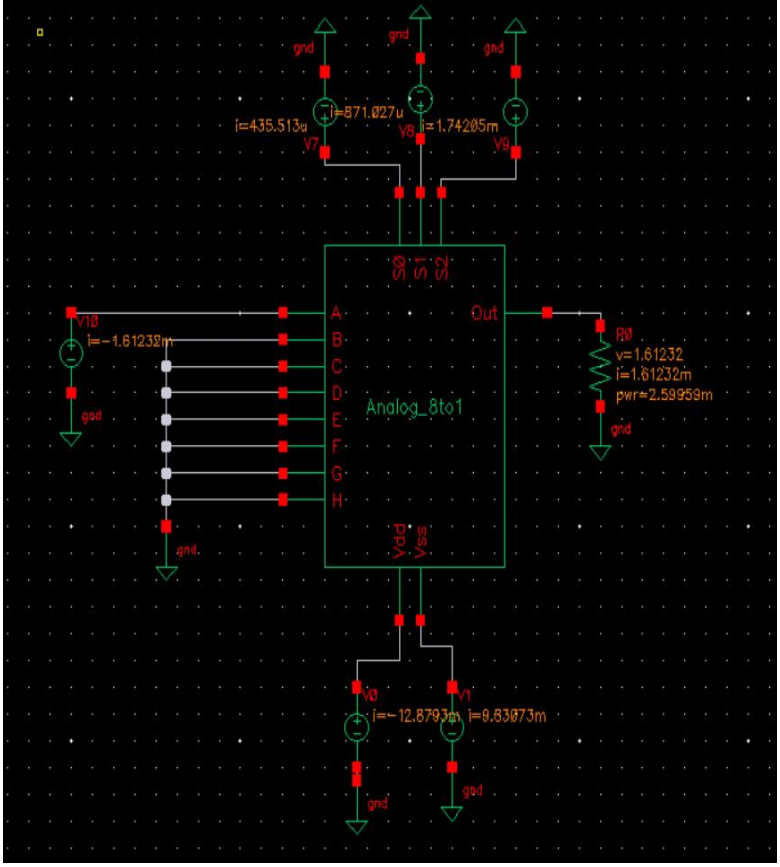


Fig : On Resistance Calculation Schematics

The output we got was 209 ohm which is above the the specification range.

5.12 Final Evaluation:

Now we will summarize the overall result of our project.

Specification	Required	Calculated
Supply Voltage	+/-3 V	+/-3 V
Logic High Level	1.4 V	1.4V
Logic Low Level	0 V	0 V
Input Capacitance (max)	50 pF	14.68 pF
Charge injection over full signal swing range	5 pC	-
Switching on Time t_{ON}	100 ns	~2 ns
Analog Signal Range	-2 to 2	-2 to 2
Power Dissipation (max)	10 mW	4.47 mW
On Resistance	10 ohm	209 ohm
Bandwidth, -3dB	1 MHz	1.72 GHz

From the table, we can see that all except two specifications were satisfied showcasing result at a far better scale. On resistance can be improved by increasing the W/L ratio of the MOSs used in the circuit. But we have taken 209 ohm as the voltage drop is tolerable (1.6V in case of 2V).

6.Limitations:

The following aspects can be considered as our limitations of the project

1. **Hardware Implementation**: We have used fairly a good number of the MOS in our circuit. So, hardware implementation would be a tedious task.

2. **Specification Sheet:**Charge injection were not calculated.

3. **Voltage Drop**:Although the voltage drop we are getting now is acceptable. It will not show desirable output if we apply small voltages as our on resistance is pretty high. Max portion of the voltage will be dropped.

4. **Process Technology:**We have used 180nm technology in our devices. This is obsolete with respect to our modern technology.

7. Future Work

1. **Performance Optimization:** Continuously work on optimizing the simulation algorithms and codebase to improve computational efficiency and reduce simulation times.

2. **Parametric Sweeps:** Implement parametric sweep capabilities to explore how different design parameters affect the multiplexer's behavior and performance.

3. **Enriched Specifications:** We can add more specification analysis to our user manual to make the MOS model more readable and usable for the enthusiasts.

8.Novelty

The key aspects that makes our project preferable are listed below:

1. Ease of Upgradability: As we have built fundamental blocks (selector blocks, transmission gate), bigger multiplexer can be easily and quickly in the future.

2. Energy Efficiency: Designing a mux simulation project with a focus on energy efficiency can be innovative, especially in the context of IoT devices and low-power applications. So. Low power consumption(4.72mW) MUX can be implemented keeping this thing in mind.

3. High Speed Application: From our analysis and design, we can say that our device can work at GHz level.

9. Mode of Teamwork

- **Timing:** We tried to progress with the project on weekends and holidays.

- **Workshop:** 4th Floor, ECE building beside our microprocessor lab was our place for project set up and storage of all materials.

- **Support:** We supported each other when any member wasn't available due to reasons.

Debugging & Verification: The debugging and verification process was a lengthy one as integrating multiple blocks was a difficult task. We had to use online resources as well as trial & error to get better outcome.

10. References

1. Input Capacitance calculation
2. On resistance calculation
3. Power consumption
4. Analog Multiplexer Documentation
5. Pass transistor logic documentation
6. Transmission gate documentation