North South University

Department of Electrical & Computer Engineering

LAB REPORT

Course Name: **CSE332L- Computer Organization and Architecture Lab**

Experiment Number:

Experiment Name: **Build a single cycle Datapath Using Control Unit**

Experiment Date: 24/08/2022

Report Submission Date: 30/08/2022

Section: 02

Group Number: 01

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Remarks:	

Exp Name: **Build a single cycle Datapath Using Control Unit**

Objectives:

- We have combined all the (R-Type, I-Type, J- Type) Datapath's into one SINGLE CYCLE DATAPATH.
- We have run Specific instructions in the Datapath (lw, sw, add, sub)
- We have run Specific instructions in the Datapath(jump)

Theory:

The simplest Datapath is the single cycle Datapath. The basic components are a register file to store the data and functional units to operate on the data such as an adder/subtractor, logical unit, and a barrel shifter. We have constructed all of these components from basic gates and switches and should be familiar with their operation. The issue now is how can we compose larger systems with these components. How large should the data be? How many bits? In our example we will pick 32 bits, a number that is compatible with Datapath's found in the majority of modern microprocessors, controllers and signal processing chips.

The control unit is responsible for taking the instruction and generating the appropriate signals for the Datapath elements.
Signals that need to be generated include
• Operation to be performed by ALU.
• Whether register file needs to be written.
• Signals for multiple intermediate multiplexors.
• Whether data memory needs to be written.

For the most part, we can generate these signals using only the opcode and funct fields of an instruction.

Control Unit Circuit Truth Table:

CSE332L - Control Unit Circuit Truth Table

Instrunctions	Opcode	RD/RT (Reg.Dst)	Reg. Write.En	ALU Src	AluOP	Sub	lw	sw	RAM_To_Reg	Jump
Add	0000	0	1	0	000	0	0	0	0	0
Sub	0001	0	1	0	000	0	0	0	0	0
Lw	0010	1	1	1	000	0	1	0	1	0
Sw	0011	0	0	1	000	0	0	1	0	0
And	0100	0	1	0	010	0	0	0	0	0
Or	0101	0	1	0	011	0	0	0	0	0
Addi	0110	1	1	1	000	0	0	0	0	0
Subi	0111	1	1	1	000	1	0	0	0	0
Ori	1000	1	1	1	011	0	0	0	0	0
Andi	1001	1	1	1	010	0	0	0	0	0
Jump	1010	0	0	0	000	0	0	0	0	1
	1011	0	0	0	000	0	0	0	0	0
	1100	0	0	0	000	0	0	0	0	0
	1101	0	0	0	000	0	0	0	0	0
	1110	0	0	0	000	0	0	0	0	0
	1111	0	0	0	000	0	0	0	0	0

R- Format	Opcode (4 bits)	RS (4 bits)	RT (4 bits)	RD (4 bits)

I- Format	Opcode (4 bits)	RS (4 bits)	RT (4 bits)	Immediate (4 bits)

J- Format	Opcode (4 bits)	Target (12 bits)

Circuit Diagrams:

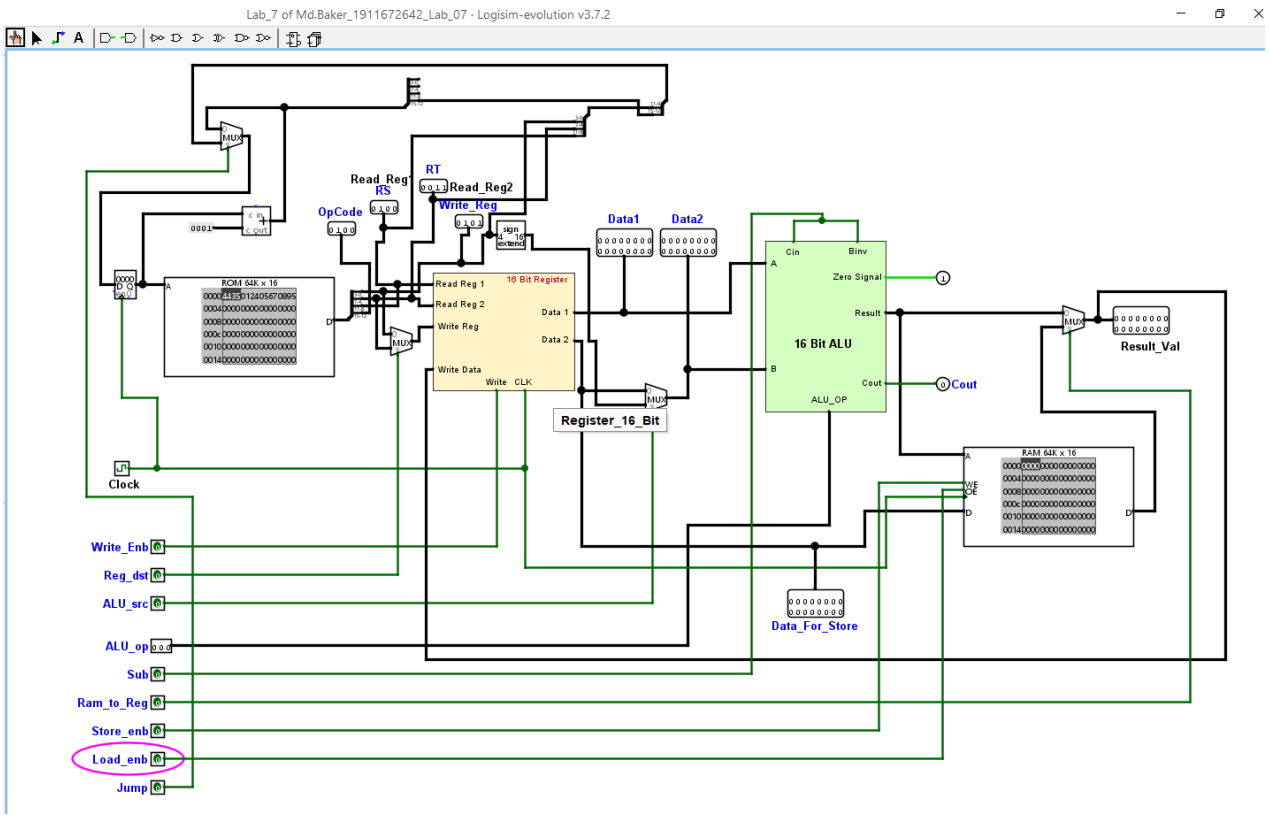

Figure: Single Cycle Datapath Without Control Unit

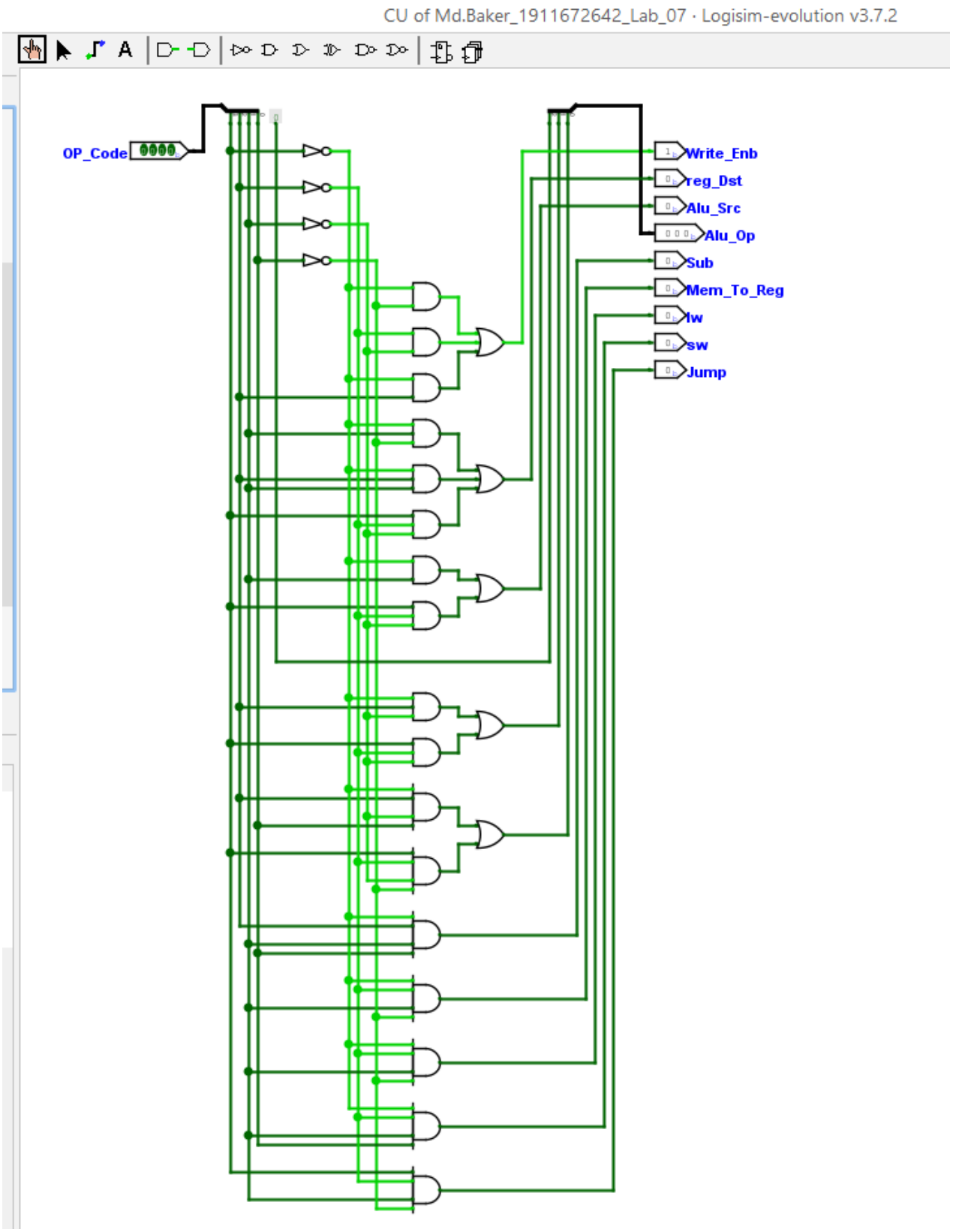

Figure: Control Unit

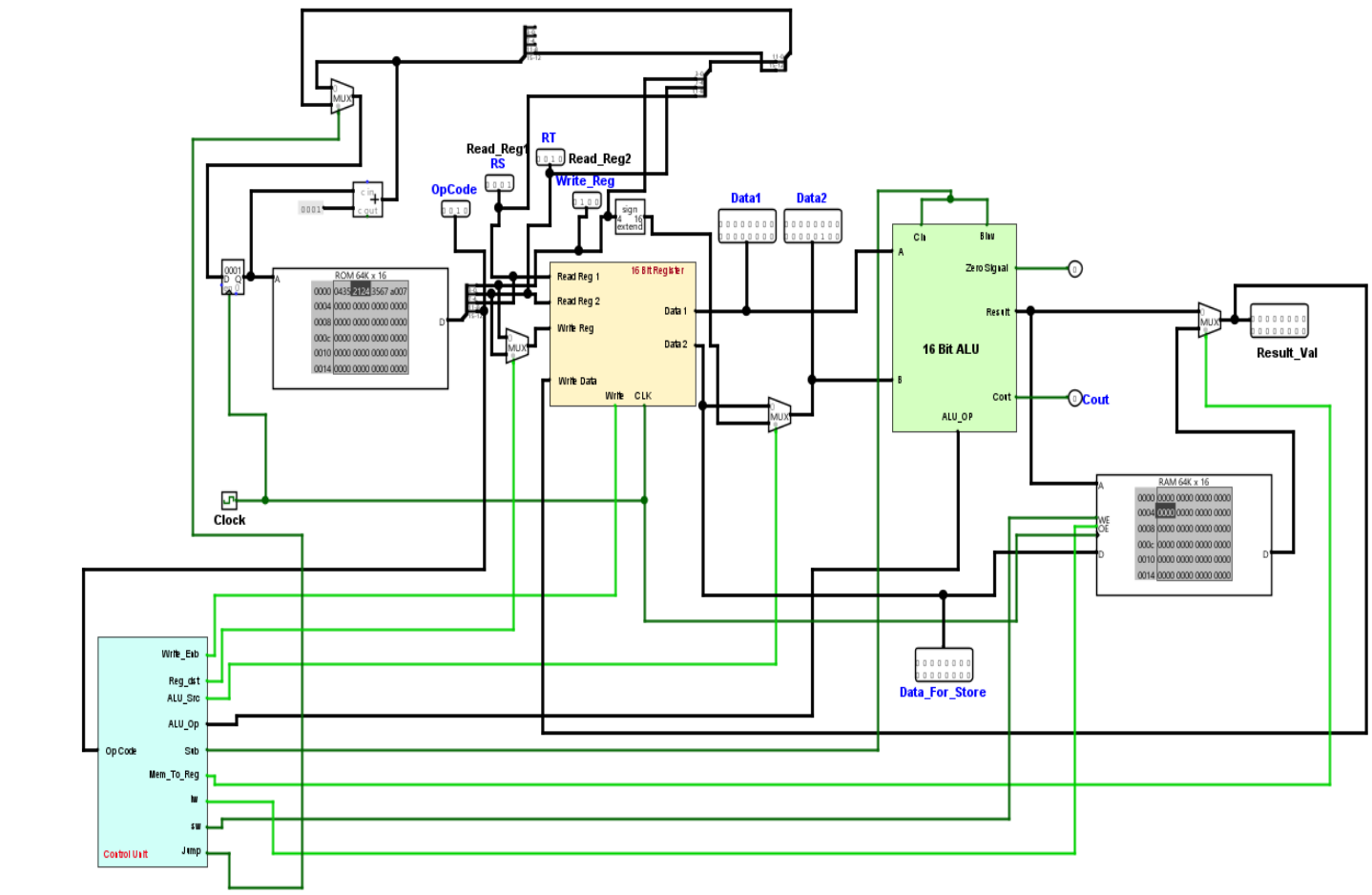

Figure: Single Cycle Datapath Using Control Unit