North South University

Department of Electrical & Computer Engineering

LAB REPORT

Course Name: **CSE332L- Computer Organization and Architecture Lab**

Experiment Number: **01**

Experiment Name: Design of a 2-bit Logic unit.

Experiment Date: 15 June,2022

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Section: 02

Group Number:

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Remarks:	

Exp: Lab 01 – Design a 2 Bit Logic Unit

Objectives:

- The objective of this experiment is to construct a 2-bit logic unit and it is a part of Arithmetic Logic Unit (ALU).
- Here I have used 4 micro-operations of this logic unit and they are AND, OR, NOT, XOR. This logic micro-operations are used for manipulating individual bits such as change value, delete or insert new bits. So, in this experiment we are observing the behavior of AND, OR, NOT, XOR micro-operation. Then one operation is selected through a Dual 4:1 Multiplexer by the select inputs S0 and S1 generating outputs Q1, Q2 corresponding to bits (A1, B1) and (A2, B2).
- Since, it is a 2-bit logic unit, we have 2 outputs in this experiment.

Equipment List:

- ✓ Trainer Board.
- ✓ IC 7404,7408,7432,7486,74LS153.
- ✓ AND, OR, NOT, XOR gates
- ✓ Wires.
- ✓ Logisim.

Theory:

Logic micro-operations specify binary operations for strings of bits stored in registers. These operations consider each bit of registers separately and treat them as binary variables.

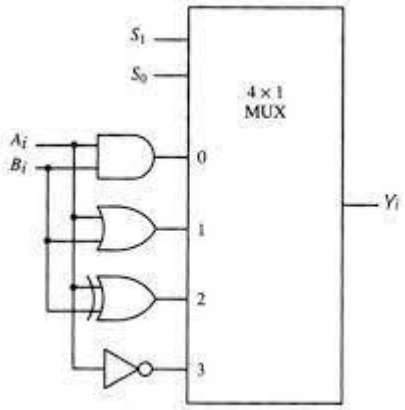


Figure 1: Schematic of 1-bit Logic Unit

Figure 1 shows one stage of a circuit that generates the four basic logic micro-operations. It consists of 4 gates and a multiplexer each of the four logic operations is generated through a gate that performs the required logic. The outputs of the gates are applied to the data inputs of the multiplexer. The two selection inputs S1 and S0 choose one of the data inputs of the multiplexers and direct it values to the output. Here in this logical block consists of two sets of such gates i.e. it performs operations on two bits (A1, B1) and (A2, B2). Then one operation is selected through a Dual 4:1 Multiplexer by the select inputs S0 and S1 generating outputs Q1, Q2 corresponding to bits (A1, B1) and (A2, B2).

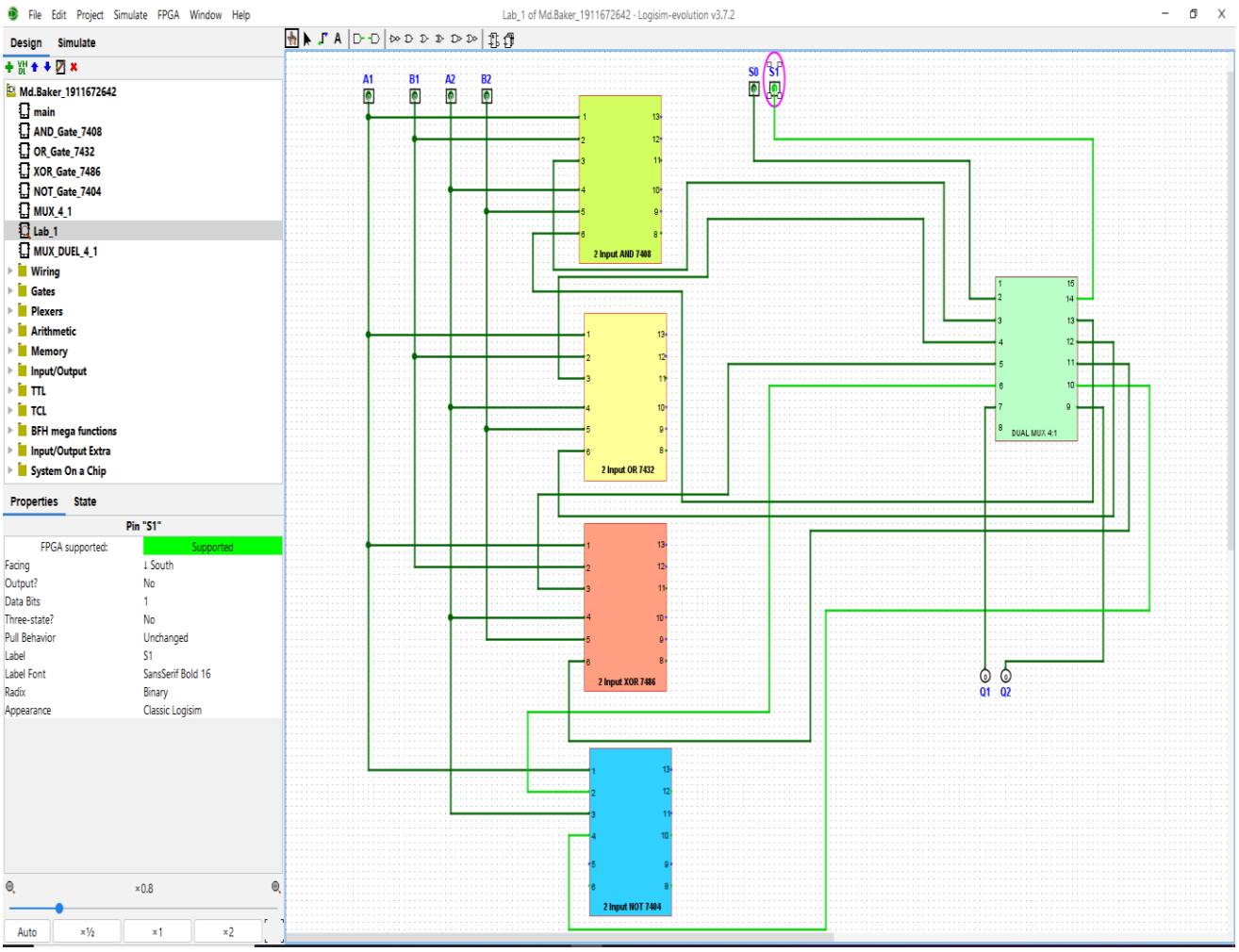
Truth Table:

Completing the Truth Table:

A1	A2	B1	B2	AND1	AND0	OR1	OR0	XOR1	XOR0	NOT A1	NOT A2
0	0	0	0	0	0	0	0	0	0	1	1
0	0	0	1	0	0	0	1	0	1	1	1
0	0	1	0	0	0	1	0	1	0	1	1
0	0	1	1	0	0	1	1	1	1	1	1
0	1	0	0	0	0	0	1	0	1	1	0
0	1	0	1	0	1	0	1	0	0	1	0
0	1	1	0	0	0	1	1	1	1	1	0
0	1	1	1	0	1	1	1	1	0	1	0
1	0	0	0	0	0	1	0	1	0	0	1
1	0	0	1	0	0	1	1	1	1	0	1
1	0	1	0	1	0	1	0	0	0	0	1
1	0	1	1	1	0	1	1	0	1	0	1
1	1	0	0	0	0	1	1	1	1	0	0
1	1	0	1	0	1	1	1	1	0	0	0
1	1	1	0	1	0	1	1	0	1	0	0
1	1	1	1	1	1	1	1	0	0	0	0

Table 1: AND OR NOT XOR truth table

IC Circuit Diagram:



Discussion:

I have designed a 2-bit logic unit in Logisim software. Since, this is a 2-bit logic unit there are 2 outputs. We, can see that in this experiment I have used 4 input which is A1, B1, A2, B2. On the other hand, S1 and S0 are the selectors of MUX IC. The first output is for showing the result of A1 and B1 input and the second one is for B2 and A2. Selector S1 and S0 is for choosing the output from multiple outputs. For example, if S1 = 0 and S0 = 0 it will show the result of AND operation. S1 = 0, S0 = 1 is for showing the output of OR operation. S1 = 1, S0 = 0 is for XOR operation and S1 = 1, S0 = 1 will show the output of inverted A. So, we can choose any output using this selector of MUX IC.

I used Logisim to simulate this experiment for that I didn't face any hardware or technical problems. Finally, I've designed a 2-bit logic unit circuit in Logisim software.