Lab Assignment 5

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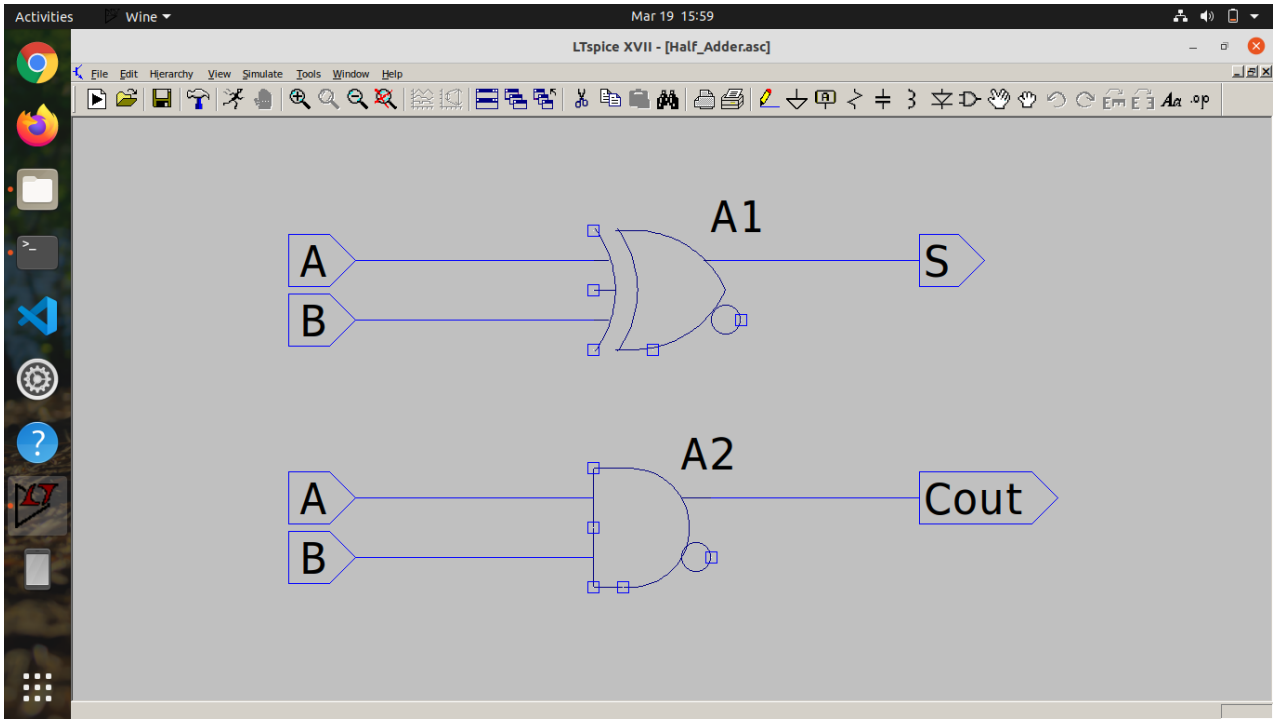
Year – 2nd Year

Part 1) Design a half adder and a full adder using minimum number of gates.

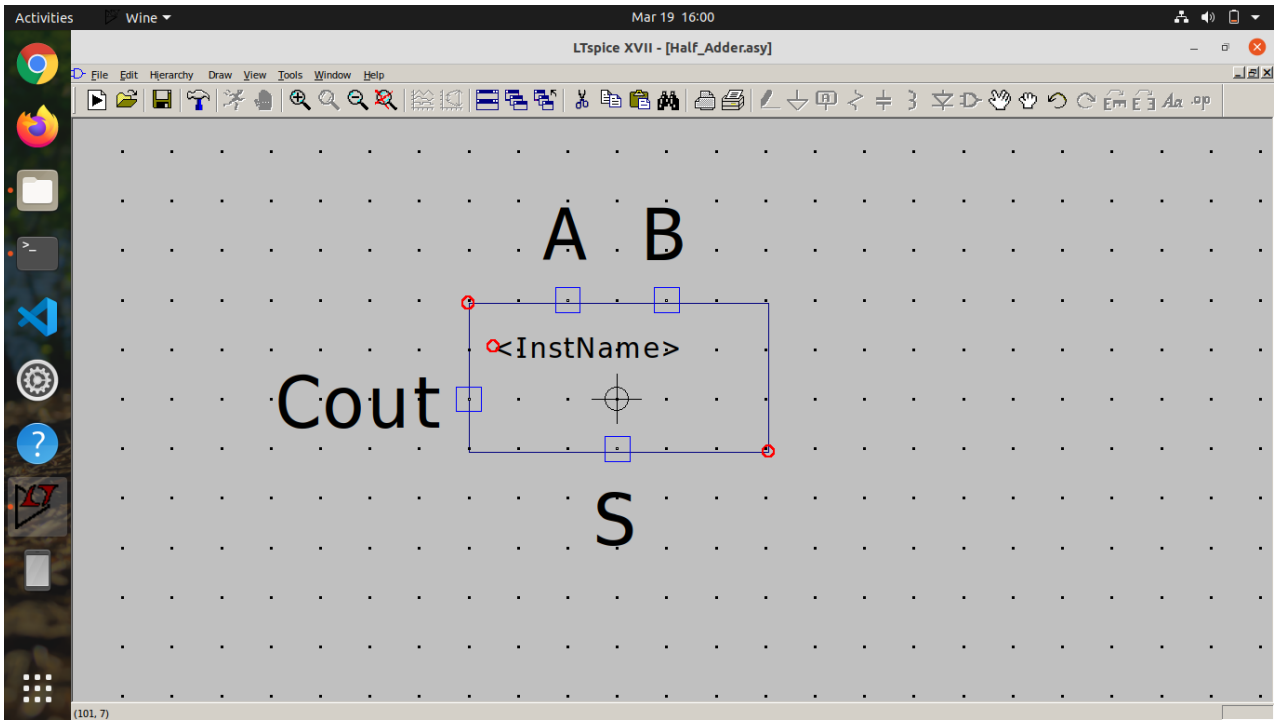
1. **Half-Adder**

   First, a circuit was created corresponding to half adder (**Half_Adder.asc** file). Then using this circuit, a symbol corresponding to half adder (**Half_Adder.asy** file) was created. Screenshots for the same are attached below:

   Circuit Diagram for Half Adder:

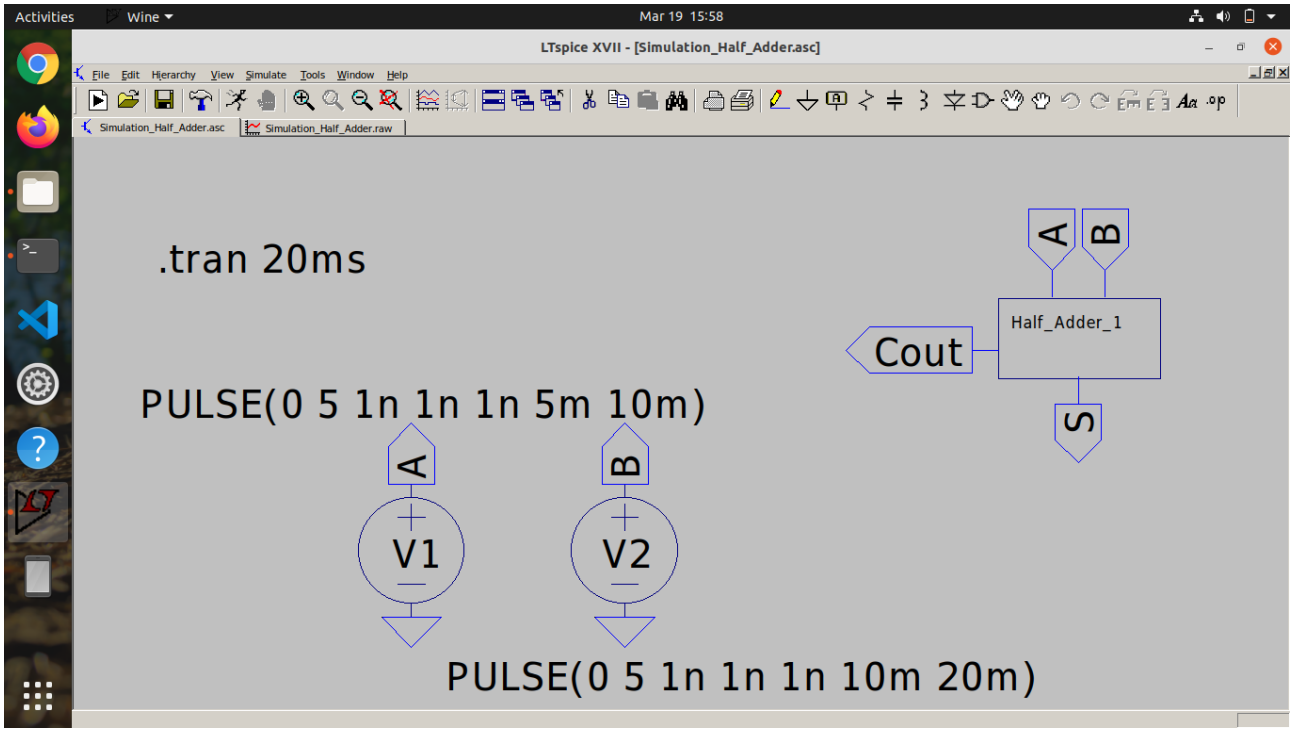


Symbol drawn for Half Adder:

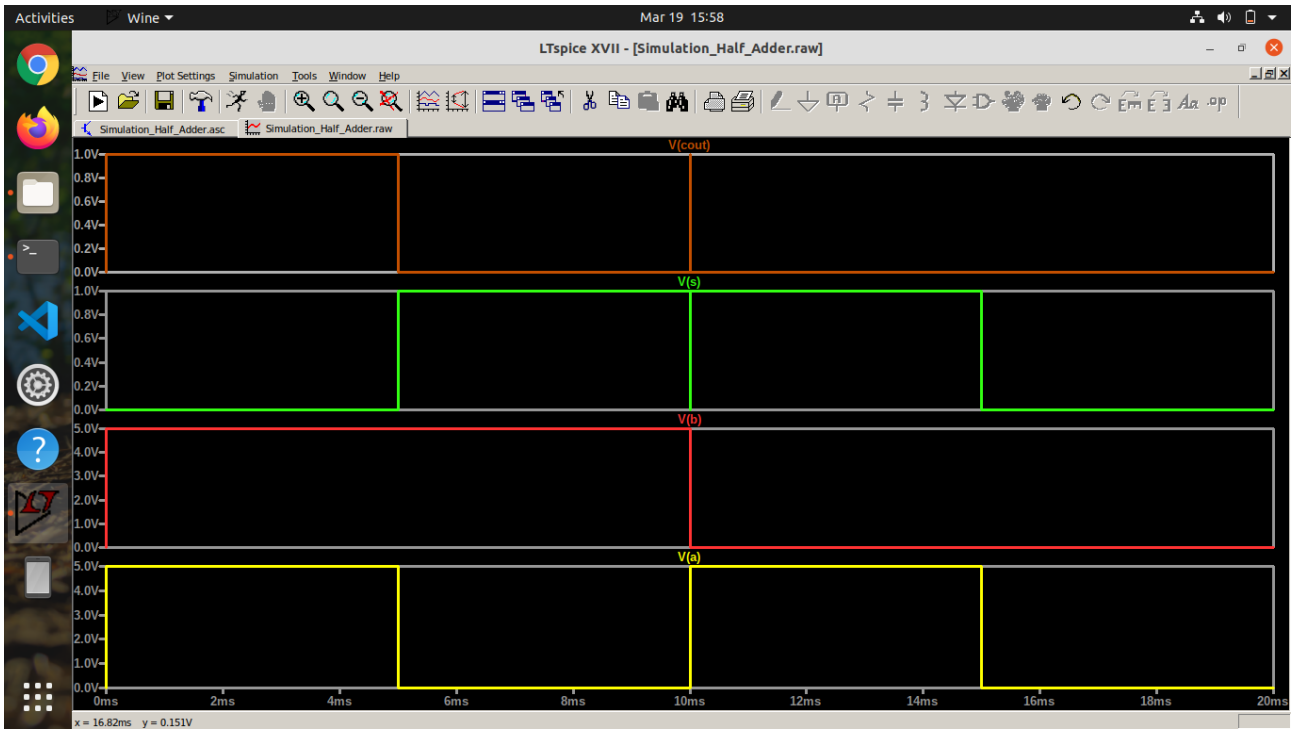


For simulation, a new circuit was created using the symbol for Half Adder (**Simulation_Half_Adder.asc** file). Then all the **four possible combinations of input voltage** were applied. The simulation was done for 20ms and the result obtained were theoretically correct.

Circuit used for Simulation:



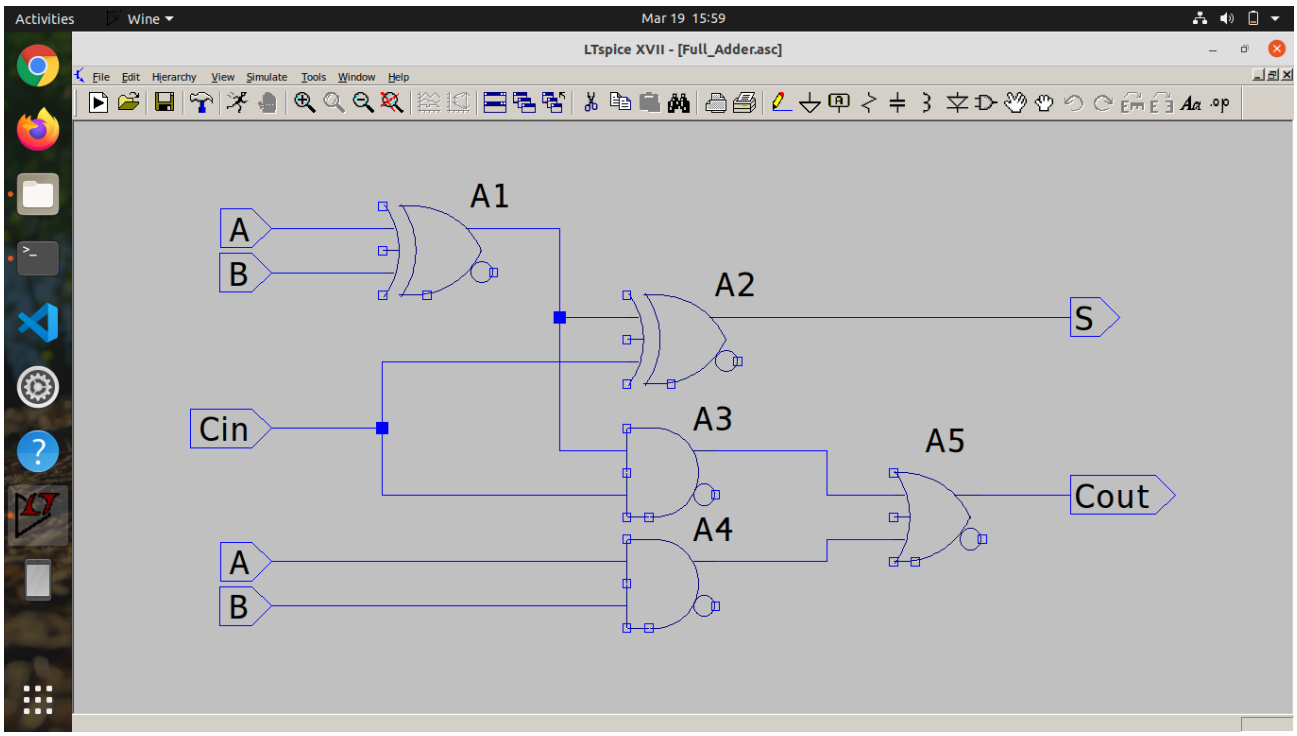
Corresponding Simulation Result:



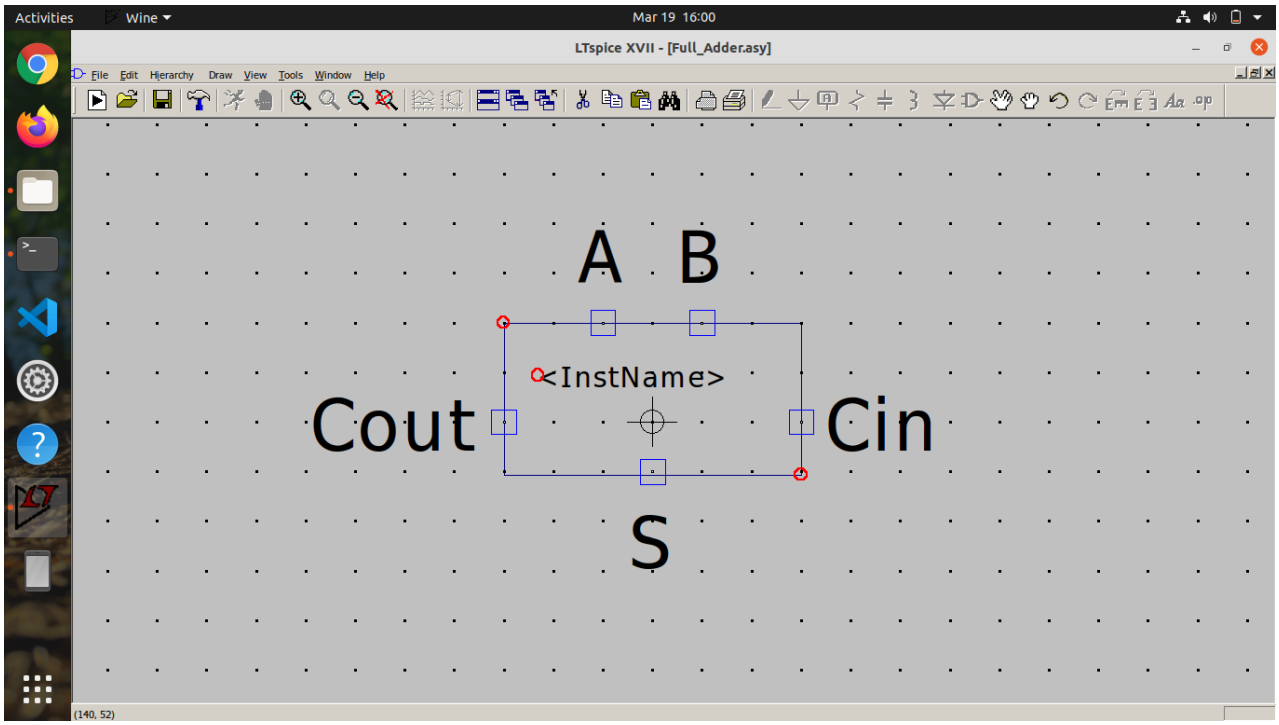
2. Full Adder

First, a circuit was created corresponding to full adder (**Full_Adder.asc** file). Then using this circuit, a symbol corresponding to full adder (**Full_Adder.asy** file) was created. Screenshots for the same are attached below:

Circuit Diagram for Full Adder:

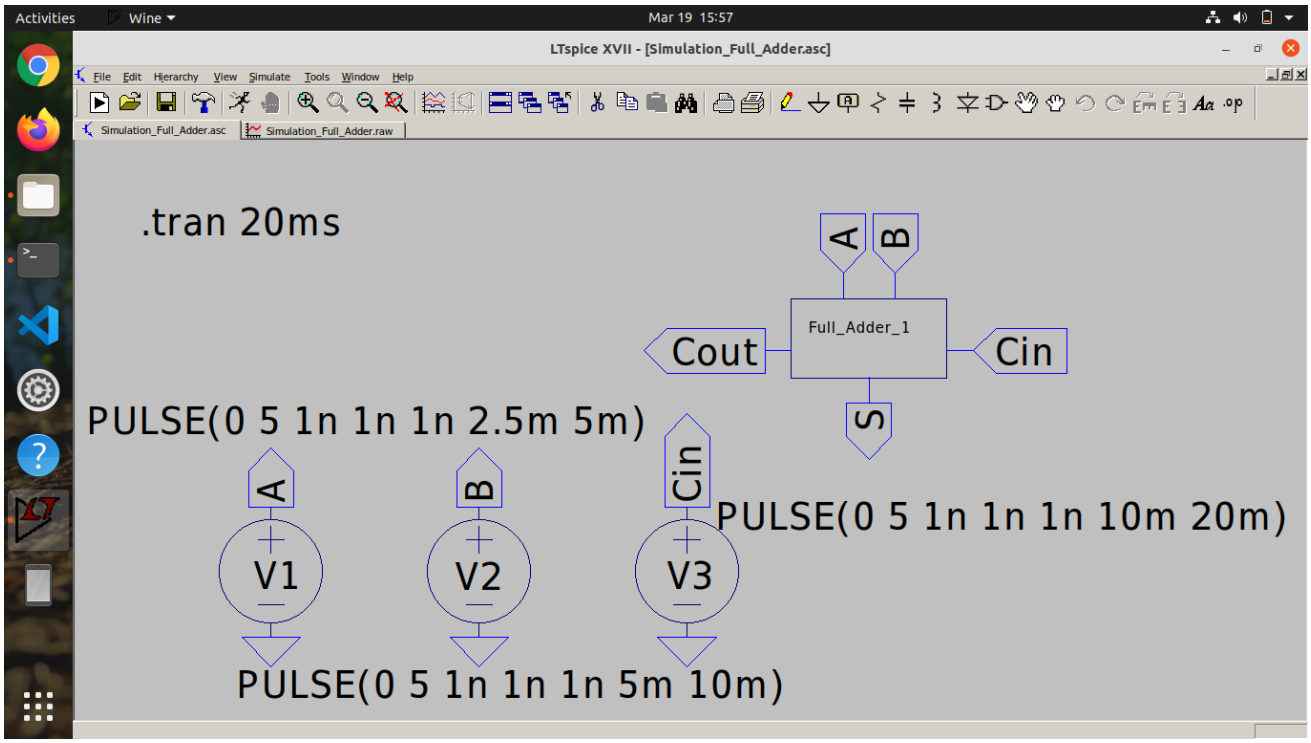


Symbol drawn for Full Adder:

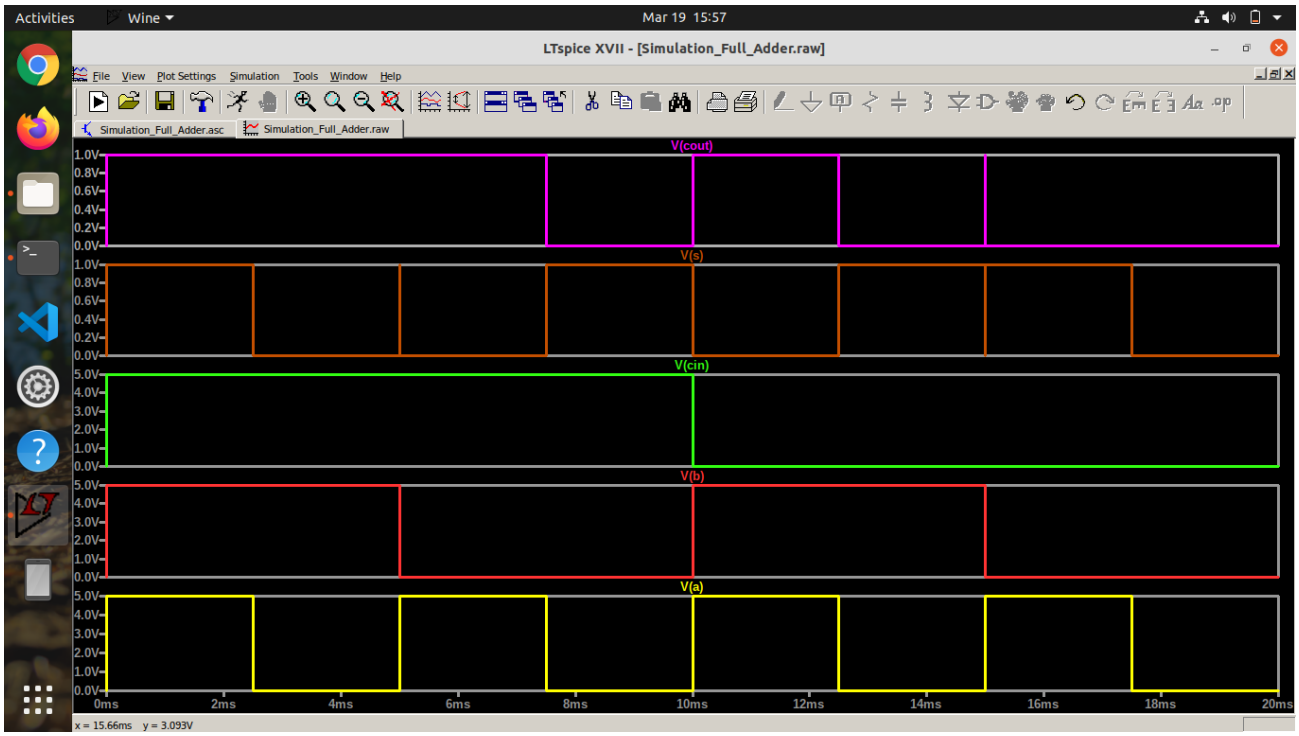


For simulation, a new circuit was created using the symbol for Full Adder (**Simulation_Full_Adder.asc** file). Then all the **eight possible combinations of input voltage** were applied. The simulation was done for 20ms and the result obtained were theoretically correct.

Circuit used for Simulation:

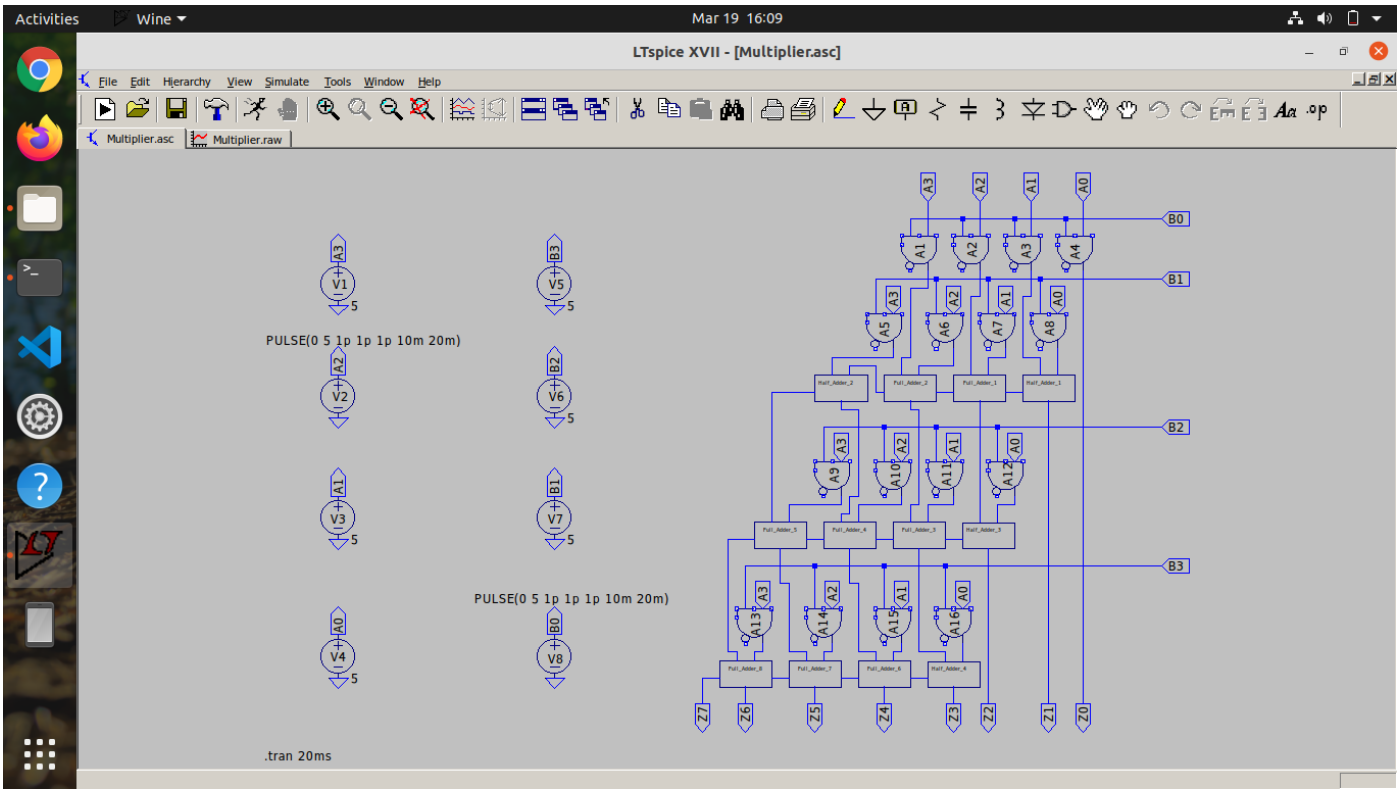


Corresponding Simulation Result:



Part 2) Desing a 4-bit multiplier using the half adders and full adders from above part.

Circuit Diagram for the 4-bit multiplier is given below. Here, same circuit diagram was used to do simulation as well. The filename in the submission is **Multiplier.asc** file. Circuit Diagram for 4-bit Multiplier:



In the above circuit, there are two 4-bit input binary number. They are:

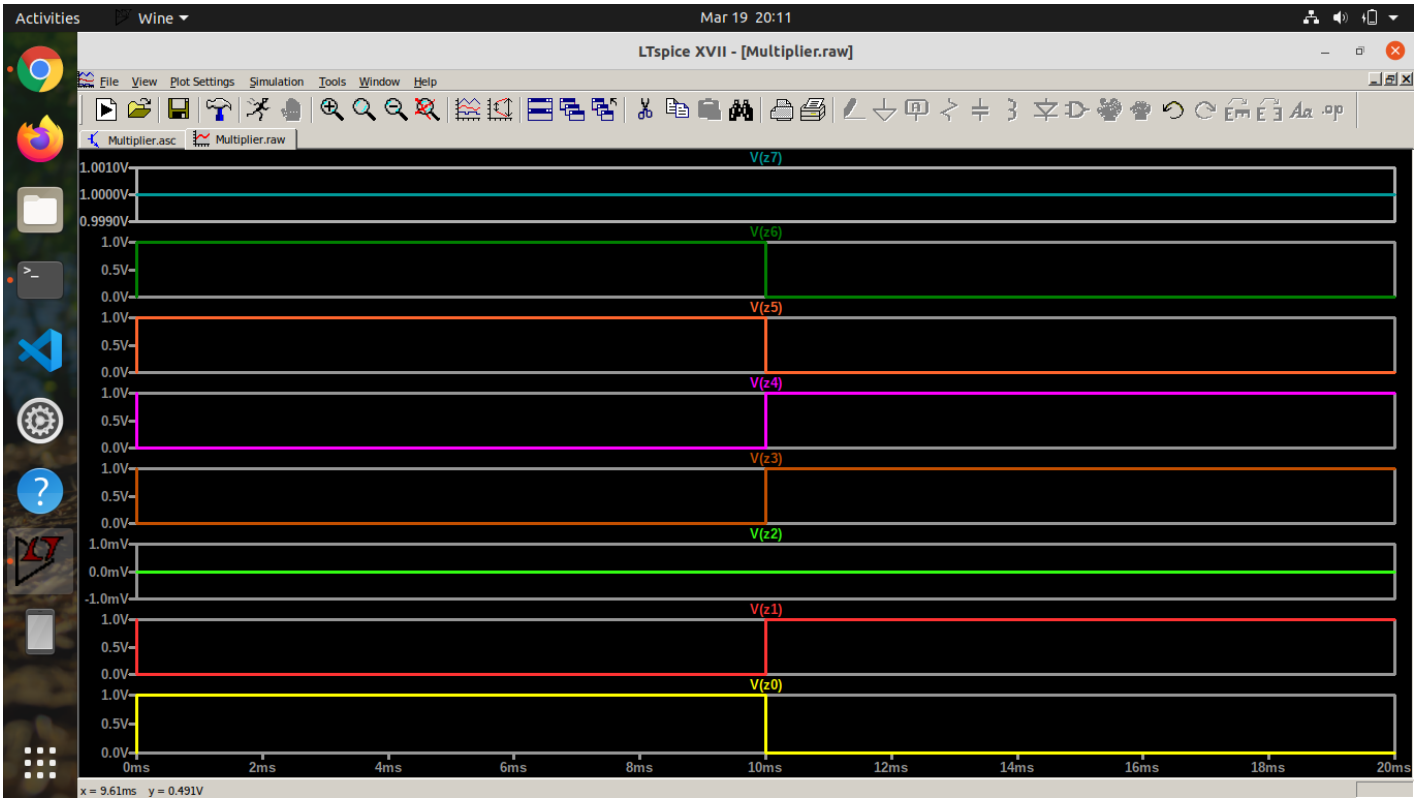
First Input (A): A3 A2 A1 A0

Second Input (B): B3 B2 B1 B0

Final output is a 8-bit number. It is given by:

Final Output (Z): Z7 Z6 Z5 Z4 Z3 Z2 Z1 Z0

Simulation was run for 20ms. For the first 10ms, all the input were kept at high voltage. This corresponds to the situation $(1111)_2$ * $(1111)_2$. For the next 10ms, voltage of A2 and B0 were kept low. Voltage for all the remaining input was kept high. This corresponds to the situation $(1011)_2$ * $(1110)_2$. Corresponding Simulation Result:



According to above simulation result:

- $(1111)_2$ * $(1111)_2$ = $(11100001)_2$
- $(1011)_2$ * $(1110)_2$ = $(10011010)_2$

Above result are theoretically correct for 4-bit unsigned binary number.