Lab Assignment-8

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Department – Computer Science & Engineering

Year – 2nd Year

Part 1) Use Verilog to design a four-bit multiplier at the behavioral level. Design a testbench to show the output for

- **1111 x 1011**
- **1100 x 1011**
- **0101 x 1001**

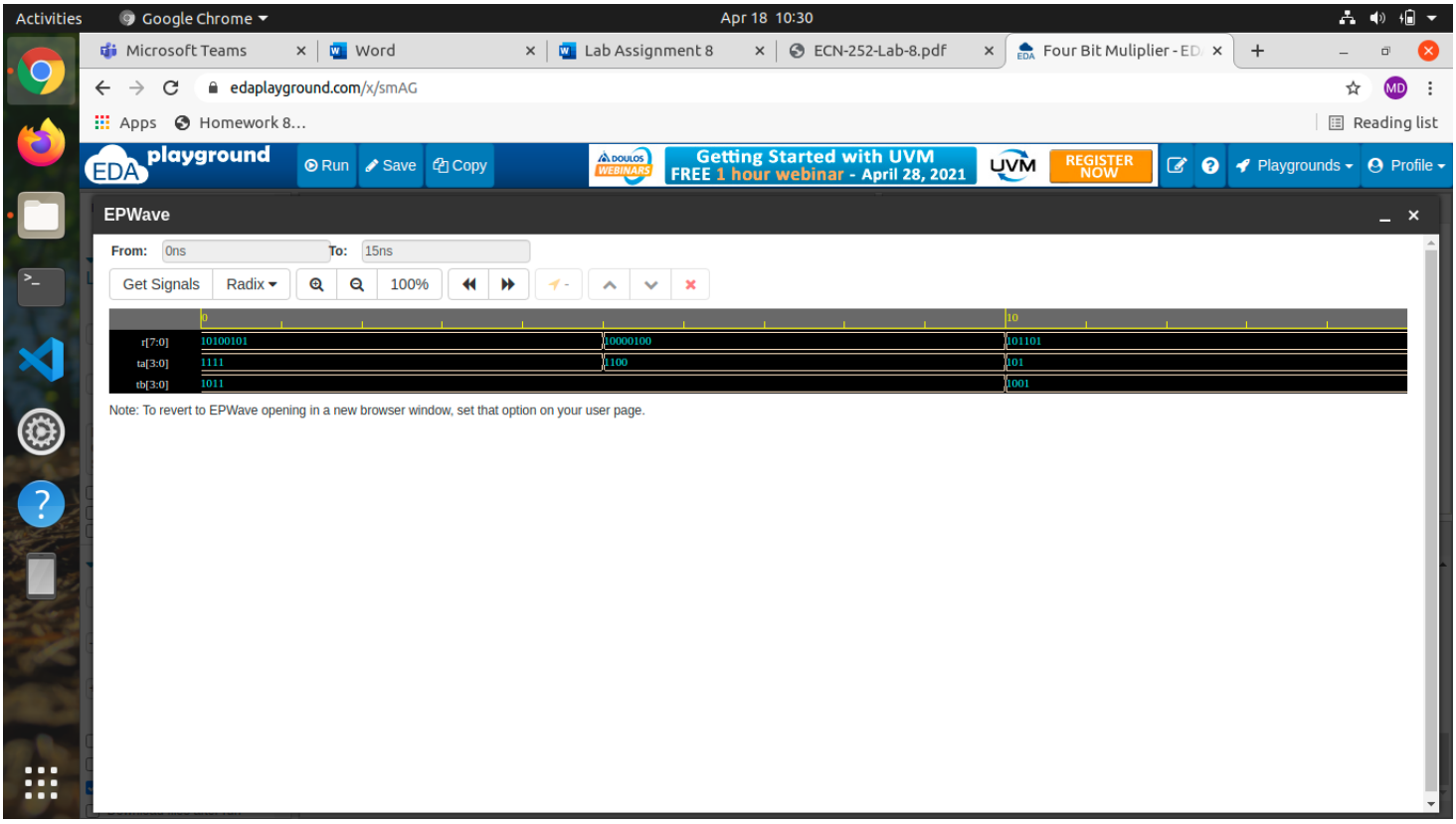
Code for the above four-bit multiplier is:

```
module fourbitmultiplier(a, b, result);
    input [3:0] a, b;
    output [7:0] result;

    assign result = a*b;

endmodule
```

Testbench designed for showing the output:

```
module main();
	reg [3:0] ta, tb;
	wire [7:0] r;

	fourbitmultiplier dut(.a(ta), .b(tb), .result(r));

	initial begin
		$dumpfile("dump.vcd");
		$dumpvars(1);
	end

	initial begin
		ta = 15;
		tb = 11;
		#5
		ta = 12;
		tb = 11;
		#5
		ta = 5;
		tb = 9;
		#5

		$finish();
	end
endmodule
```

Screenshot of the corresponding output obtained:



Part 2) Use Verilog to design a positive edge triggered Toggle(T) flip-flop with an asynchronous set and an asynchronous reset. Design a testbench to show successful operation.

In this part high-level triggering set and reset were designed. This means that set and reset functions are operational only when clock is set to 1 or high voltage. Thus,

- If set = 1
  - q = 1, if clk = 1
  - Otherwise, value of q remains as it is
- If reset = 1
  - q = 0, if clk = 1
  - Otherwise, value of q remains as it is

The toggle operation is designed to be edge triggered.

Code for the above Toggle Flip-Flop is:

```
module tff(clk, set, reset, t, q, qb);
    input clk;
    input set;
    input reset;
    input t;

    output q;
    output qb;

    reg q;
    assign qb = ~q;

    always @(posedge clk or posedge set or posedge reset) begin
        if (set) begin
            if (clk) begin
                q <= 1'b1;
            end else begin
                q <= q;
            end
        end else if (reset) begin
            if (clk) begin
                q <= 1'b0;
            end else begin
```

```
                q <= q;
            end
        end else begin
            if (t) begin
                q <= ~q;
            end else begin
                q <= q;
            end
        end
    end
endmodule
```

Testbench designed for showing the output:

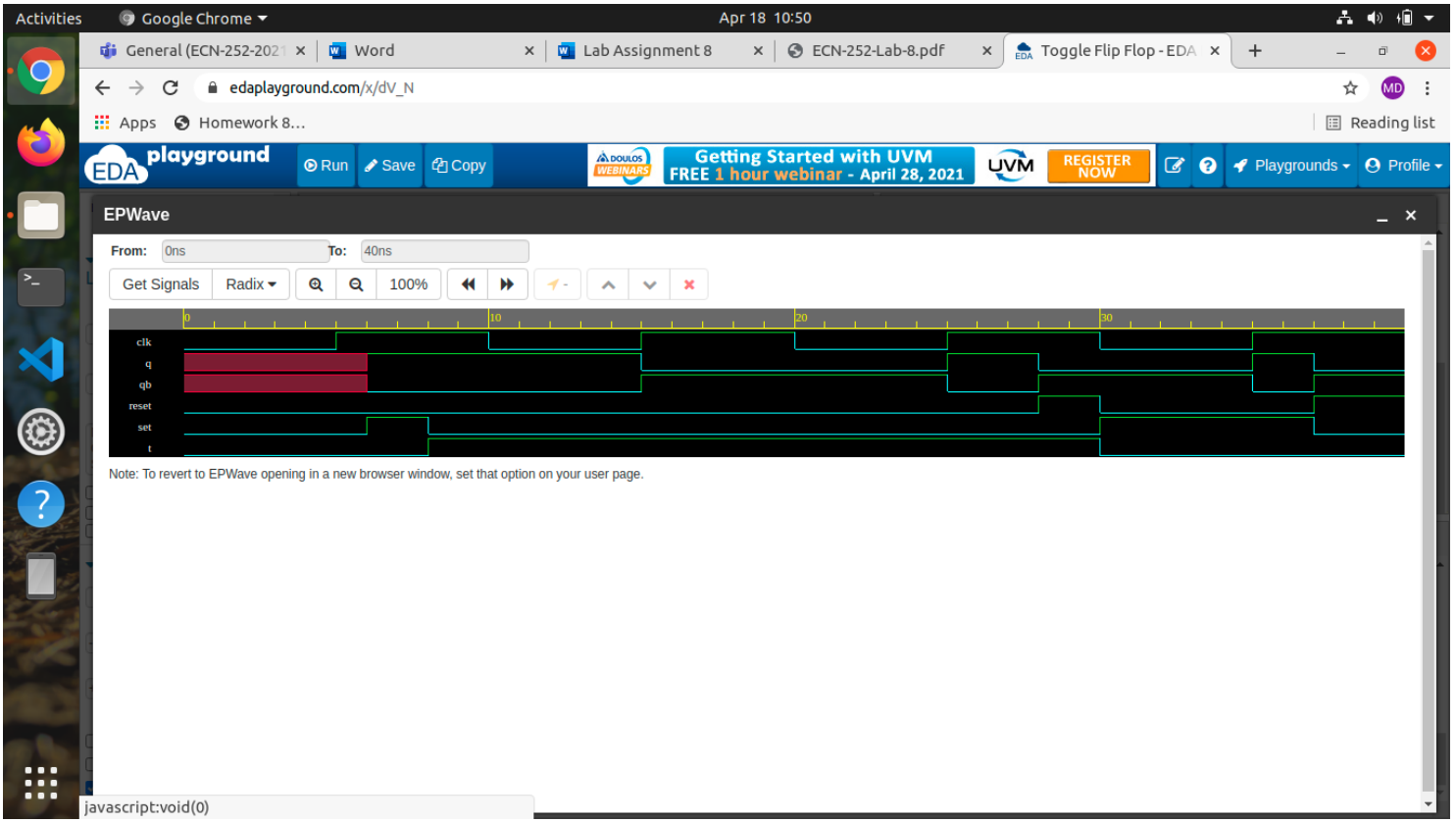
```
module test;
    reg clk;
    reg set;
    reg reset;
    reg t;

    wire q;
    wire qb;

    tff TFF(.clk(clk), .set(set), .reset(reset), .t(t), .q(q), .qb(qb));
```

```
initial begin
        $dumpfile("dump.vcd");
        $dumpvars(1);
end

initial begin
            clk = 0;
            set = 0;
            reset = 0;
            t = 0;
            #5
            clk = 1;
            set = 0;
            reset = 0;
            t = 0;
            #1
            clk = 1;
            set = 1;
            reset = 0;
            t = 0;
            #2
            clk = 1;
            set = 0;
            reset = 0;
            t = 1;
            #2
```

```
clk = 0;
set = 0;
reset = 0;
t = 1;
#5
clk = 1;
set = 0;
reset = 0;
t = 1;
#5
clk = 0;
set = 0;
reset = 0;
t = 1;
#5
clk = 1;
set = 0;
reset = 0;
t = 1;
#3
clk = 1;
set = 0;
reset = 1;
t = 1;
#2
clk = 0;
```

```
        set = 1;
        reset = 0;
        t = 0;
        #5
        clk = 1;
        set = 1;
        reset = 0;
        t = 0;
        #2
        clk = 1;
        set = 0;
        reset = 1;
        t = 0;
        #3

        $finish();
    end
endmodule
```

Screenshot of the corresponding output obtained:


Activities
Google Chrome
Apr 18 10:50
General (ECN-252-2021
Word
Lab Assignment 8
ECN-252-Lab-8.pdf
Toggle Flip Flop - EDA
edaplayground.com/x/dV_N
Apps
Homework 8...
Reading list
EDA playground
Run
Save
Copy
Getting Started with UVM
FREE 1 hour webinar - April 28, 2021
REGISTER NOW
Playgrounds
Profile
EPWave
From:
0ns
To:
40ns
Get Signals
Radix
100%
clk
q
qb
reset
set
t
Note: To revert to EPWave opening in a new browser window, set that option on your user page.
javascript:void(0)