Lab Assignment 2

Name – Md Junaid Mahmood

Enrolment Number – 19116040

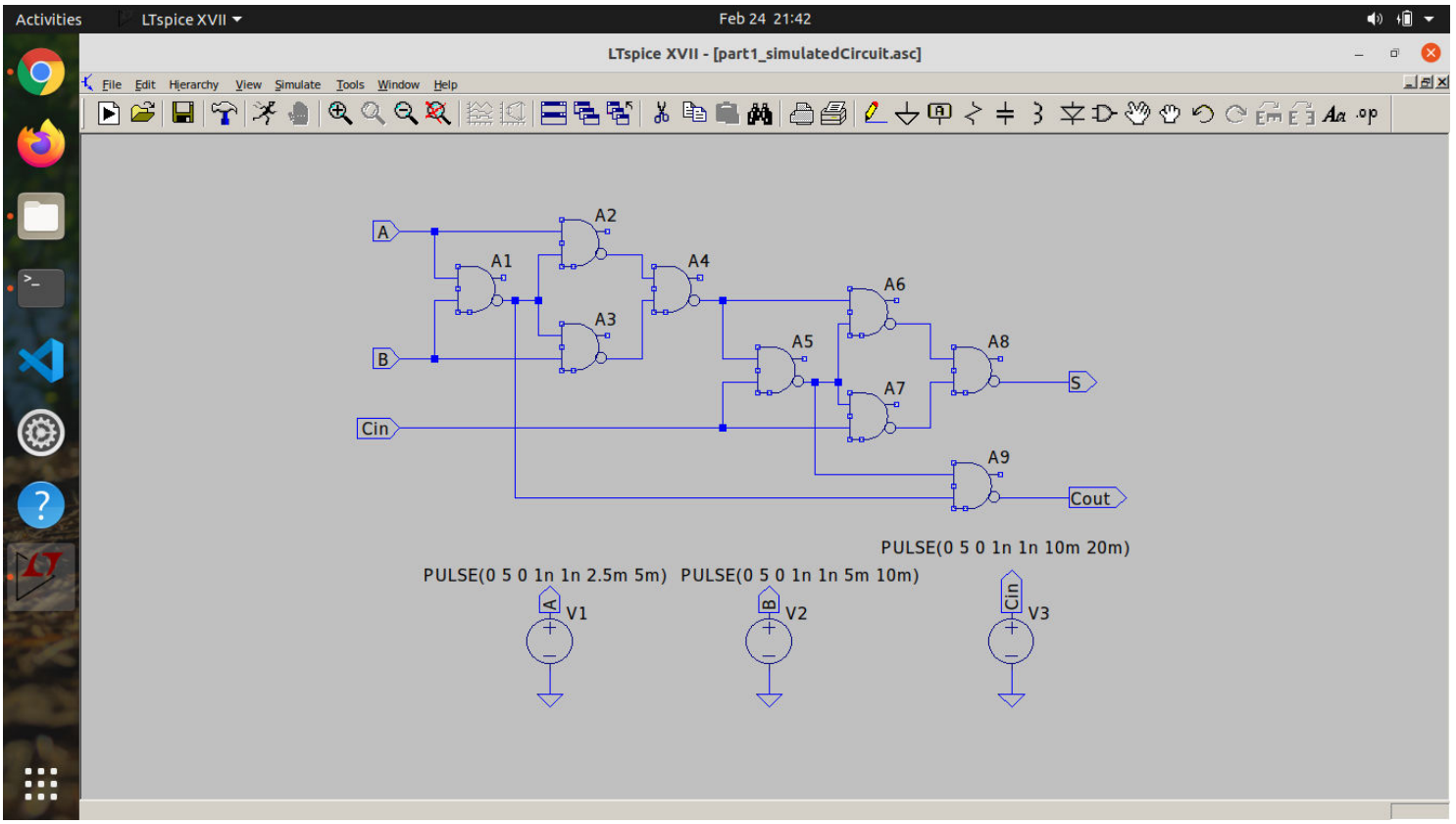
Department – Computer Science & Engineering

Year – 2nd year

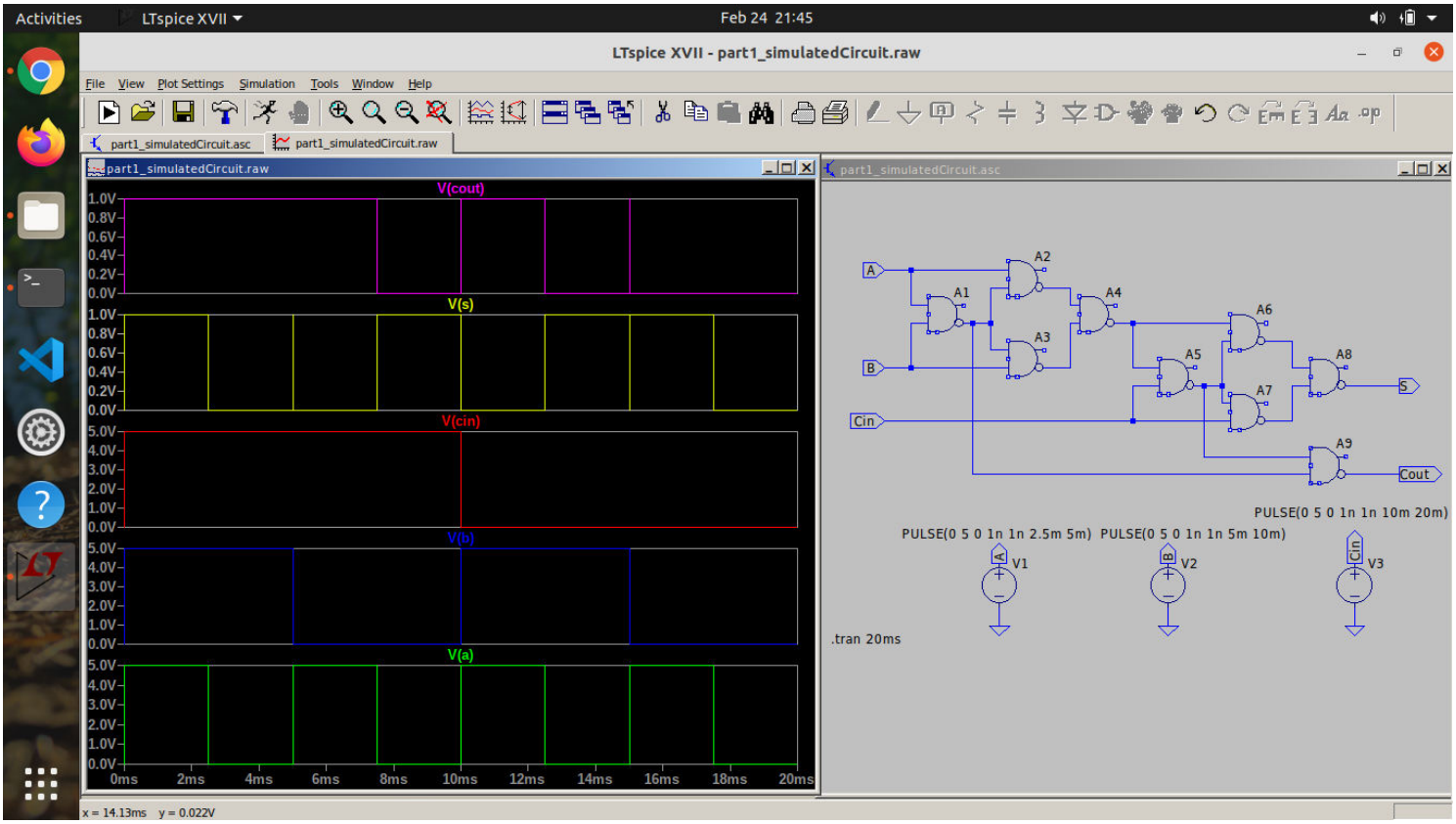
<u>Part 1)</u> Design a full adder using two input NAND gates only

The screenshot attached below provides the circuit diagram of the above part. Labels mentioned in the diagram have following meaning:

1. A & B are the bit value which are to be added
2. Cin is the input carry to the adder
3. S is the sum obtained from the adder
4. Cout is the output carry of the adder



The screenshot attached below provides the simulation result of the above circuit:



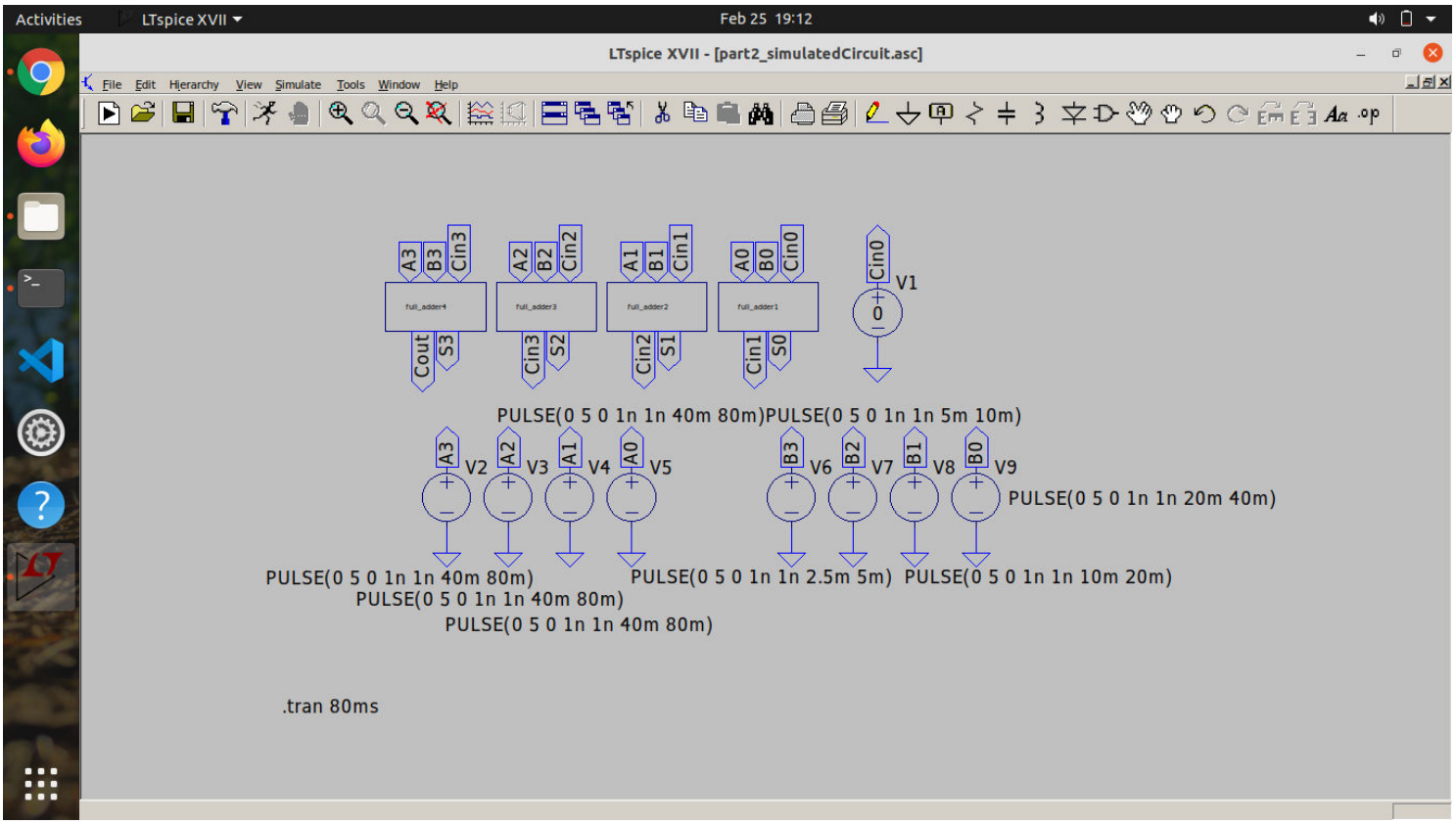
Simulation was carried for the stop time of 20ms. Bit A, bit B and bit Cin switches their value after every 2.5ms, 5ms and 10ms respectively. The signals are represented by the following colours:

1. Input bit A – green
2. Input bit B – blue
3. Input bit Cin – red
4. Output bit S – yellow
5. Output bit Cout – pink

<u>Part 2)</u> Design a 4-bit adder using full bit adder from part 1

The screenshot attached below provides the circuit diagram of the above part. Labels mentioned in the diagram have their usual meaning.

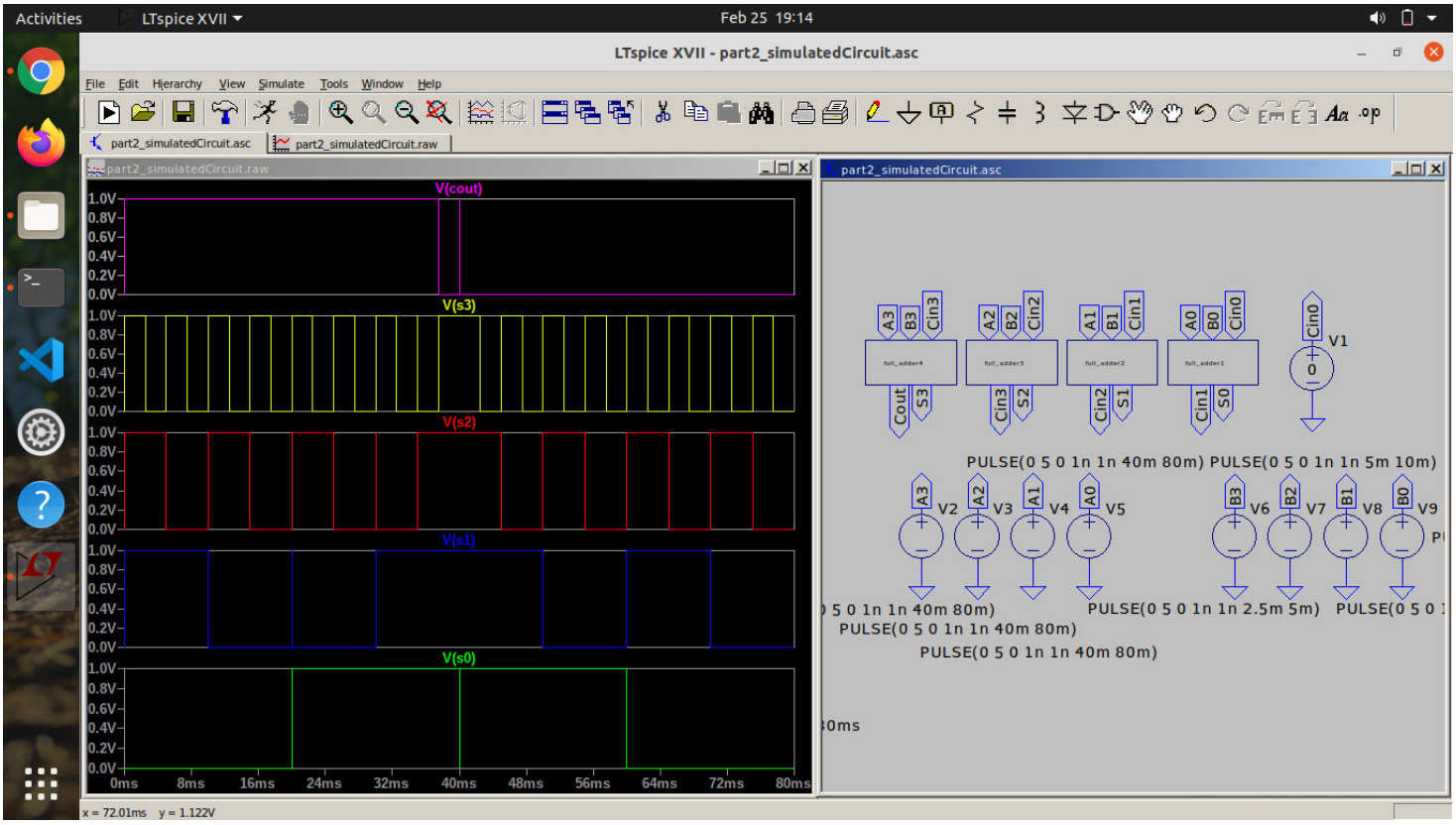
- The symbol full_adder was created using the circuit diagram of a full adder in Part 1.
- The input carry to the first adder is set to 0.



Now, for the purpose of simulation, following points are noteworthy:

1. Since, the 4-bit adder is designed from the full adder made in Part 1 which showed correct simulation results, thus, the 4-bit adder would give the correct result.
2. However, for the purpose of simulation, the number of cases (which were originally 256) were reduced by considering the symmetry between the bits of number A and number B.
    a. All the 16 combinations were considered for one of the number B.
    b. For A only two combinations were considered, which are 1111 and 0000.
    c. Thus, a total of 32 cases were used for the simulation. Using these 32 cases, most of the combinations between the bits of number A and number B were covered.
    d. The simulation for these 32 cases gave correct result.

The screenshot attached below provides the simulation result of the above circuit:

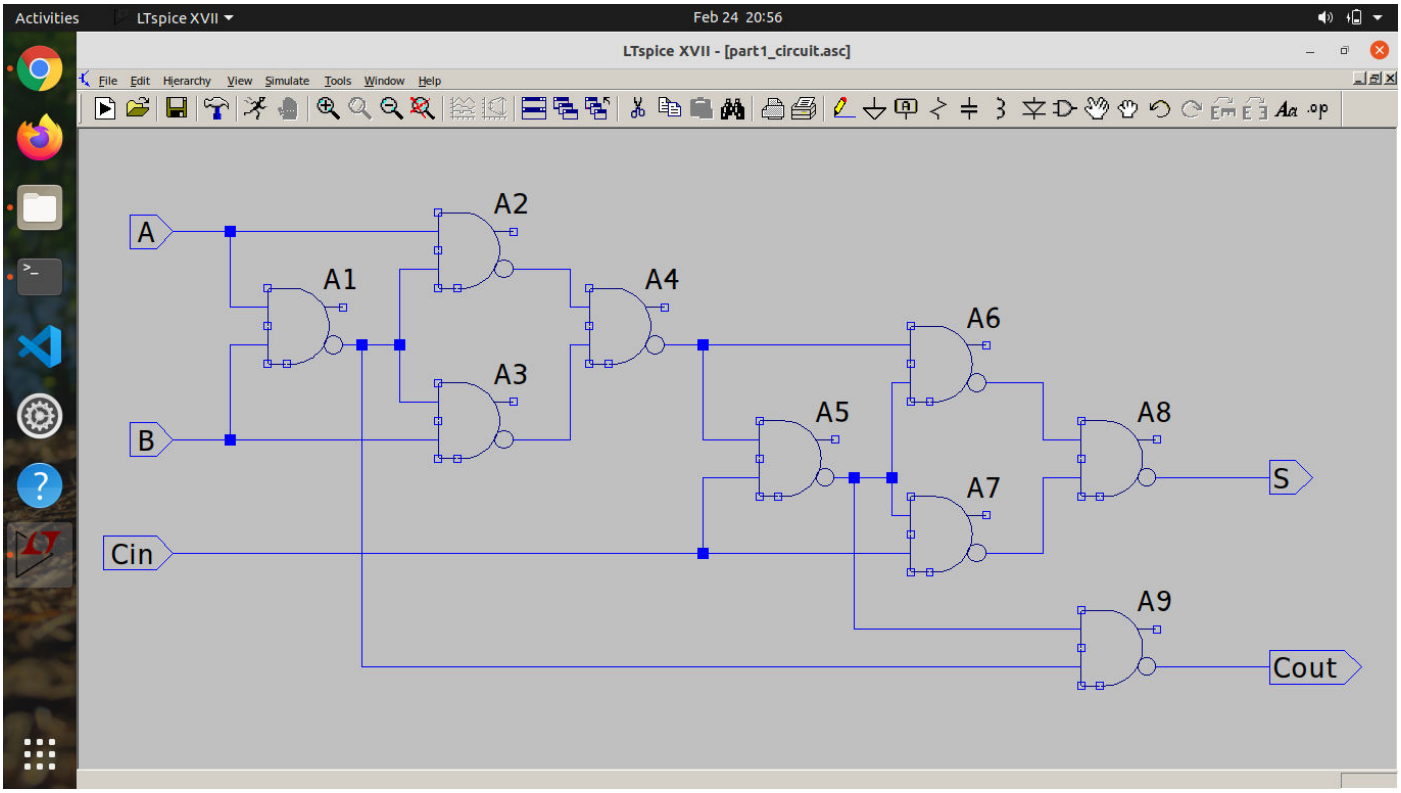


Simulation was carried for the stop time of 80ms. The signals are represented by the following colours:

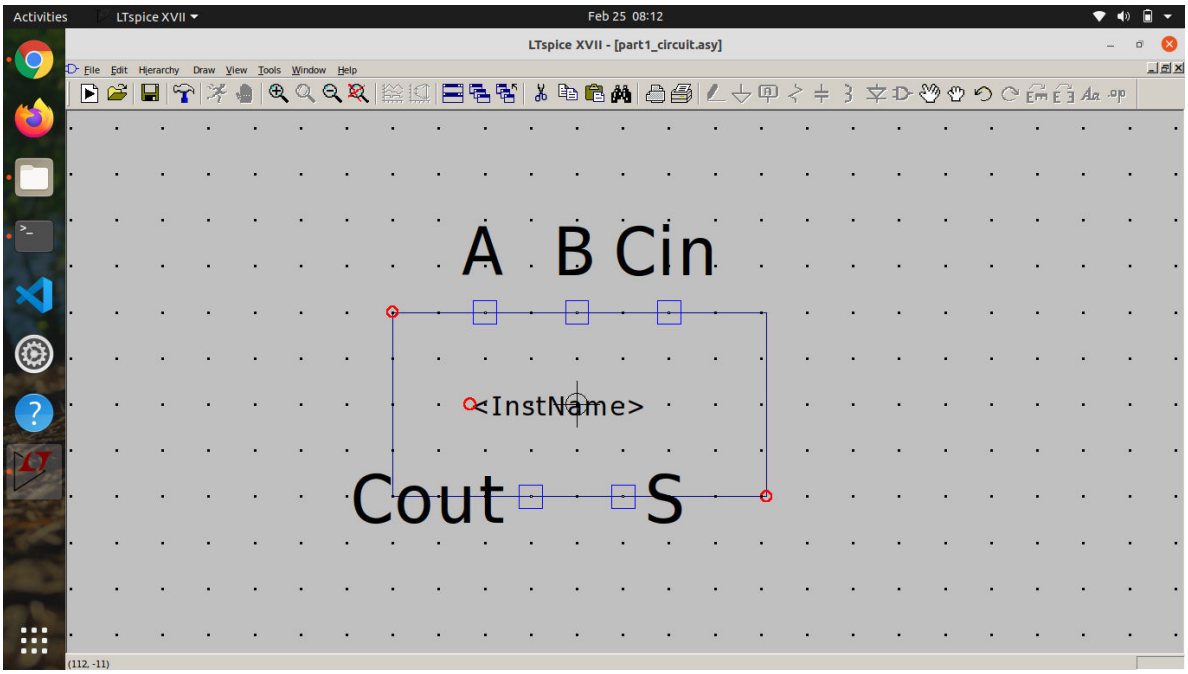
1. LSB of sum or S0 – green
2. S1 – blue
3. S2 – red
4. S3 – yellow
5. Cout – pink

Now the symbol of the full adder was created using the circuit drawn for Part 1. Its description is given below:

The circuit used for the creation of the symbol of full_adder:



The symbol created for representing above circuit:



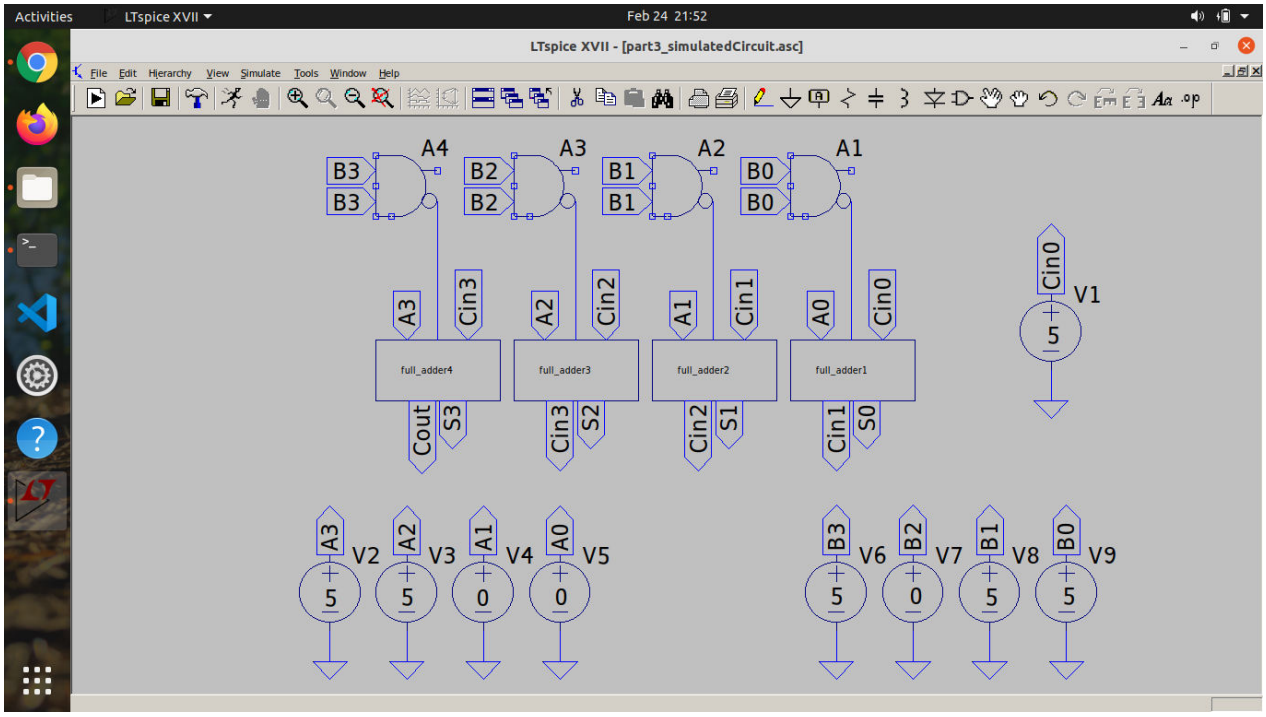
<u>Part 3)</u> To subtract number B from number A using 2's complement method using the 4-bit adder from part 2.

Now mod (19116040, 4) + 1 = 1

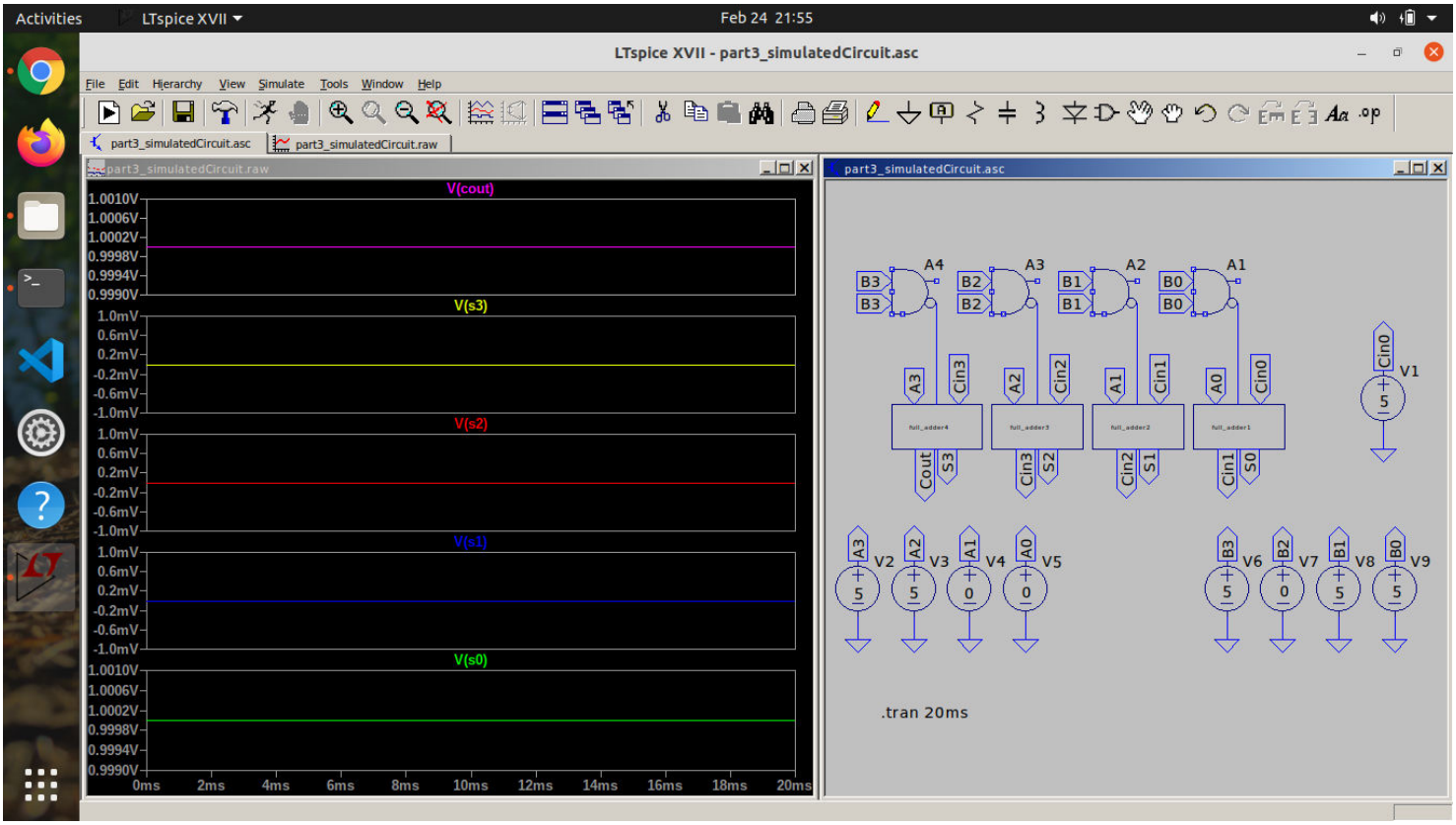
Hence, problem 1, was chosen which is A = 1100 and B = 1011

The screenshot attached below provides the circuit diagram of the above part. Labels mentioned in the diagram have their usual meaning.

1. The symbol full_adder was created using the circuit diagram of a full adder in Part 1.
2. For taking 2's complement, following was done:
    a. Complement of every bit of number B was taken
    b. The input carry to full_adder1 (Cin0) was set to 1



The screenshot attached below provides the simulation result of the above circuit:

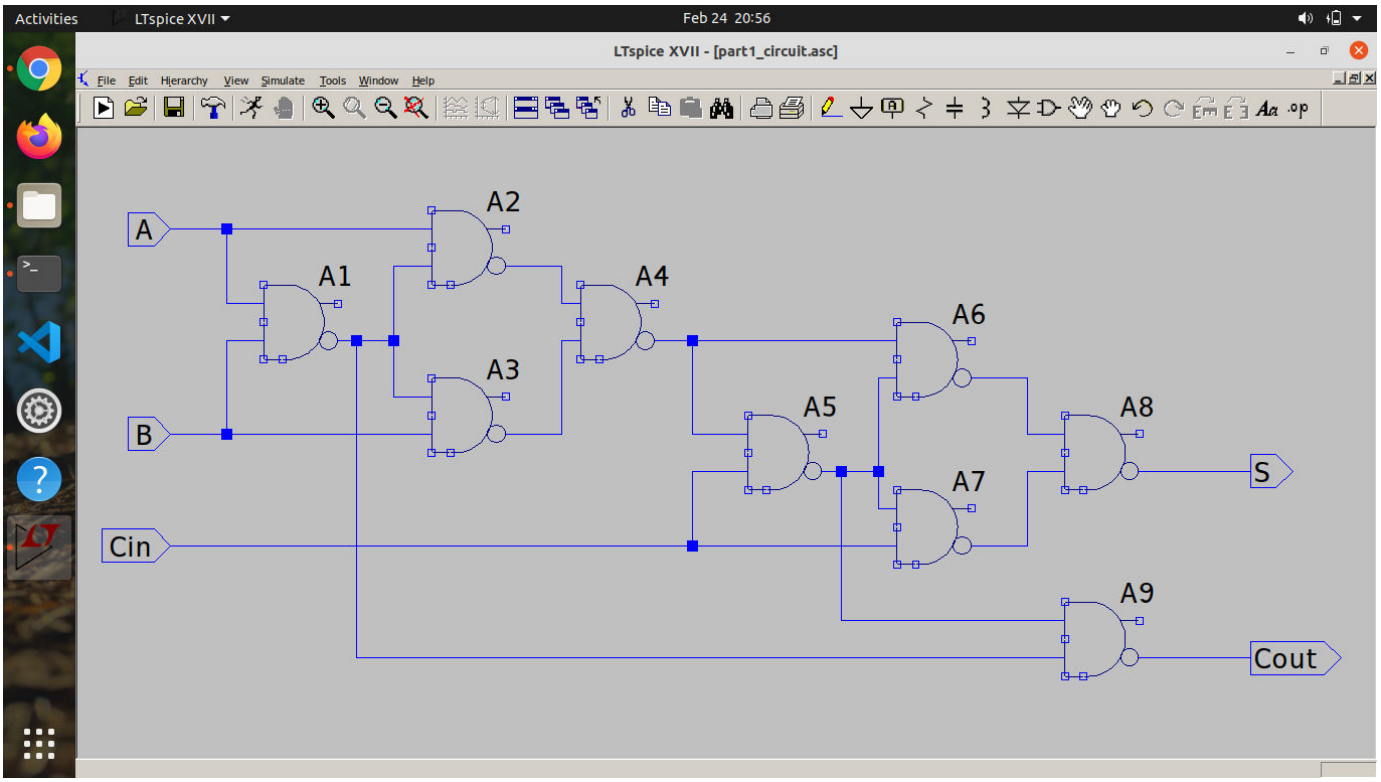


Simulation was carried for the stop time of 20ms. Binary numbers A and B was set up using the voltage source as specified in Problem 1 (A = 1100 & B = 1011). The signals are represented by the following colours:

1. LSB of sum or S0 – green
2. S1 – blue
3. S2 – red
4. S3 – yellow
5. Cout – pink

Now the symbol of the full_adder was created using the circuit drawn for Part 1. Its description is given below:

The circuit used for the creation of the symbol of full_adder:



The symbol created for representing above circuit: