# 8086 Memory Interfacing

# Memory Interfacing ( Chip Identification)

Two memory elements : EPROM and RAM

For EPROM: IC 27XX, 27XXX
For RAM: IC 61XX, 61XXX, 62XXX, 62XX

IC 2716

16 => memory size in bits 16 kbits of memory size

Memory size = 16kbits / 8 = 2kB = 2k x 1B = 2x 2^10 x 1B
Data lines = 8 bits
Address lines = log (base 2) 2^11 = 11 bits

# Memory Interfacing ( Chip Identification)

RAM IC 6264

64 kilobits => memory size
M.S = 64/8 = 8kB = 8x2^10 x 1B = 2^13 x 8

m = 13, n = 8
where m is number of address lines
n is number of data lines

IC 27128 => EPROM

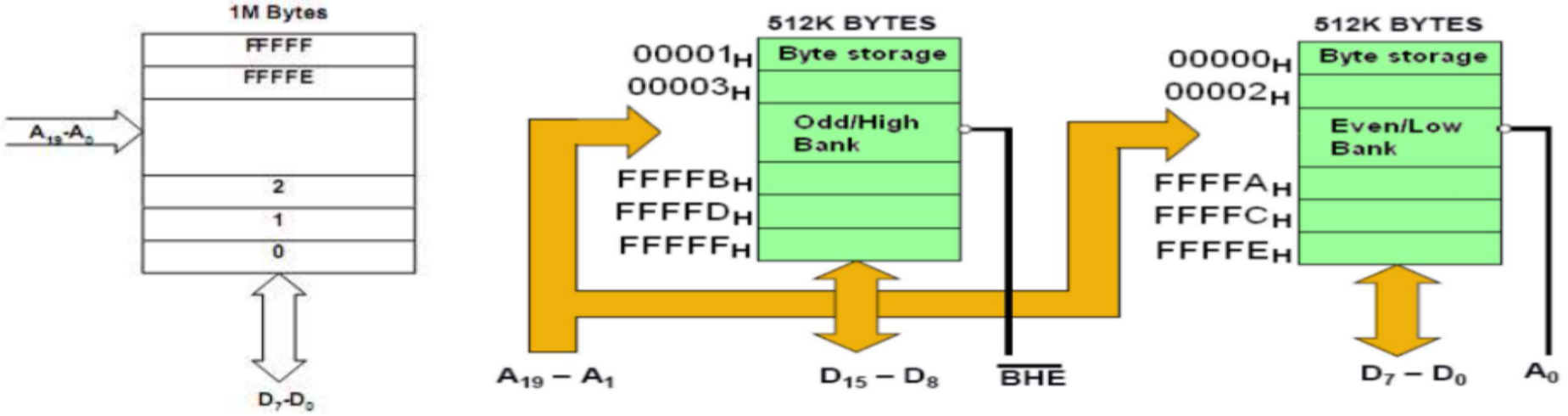
Memory size = 128 kilobits = 128/8 kB = 16 kB

16 kB = 16 x 2^10 x 1B = 2^14 x 8

m = 14, n = 8
where m is number of address lines
n is number of data lines

# 8086 Memory Organization

- The memory address space of the 8086-based microcomputers has different logical and physical **organizations**.
- **Logically**, memory is implemented as a single **1M × 8 memory bank**. The byte-wide storage locations are assigned consecutive addresses over the range from 00000H through FFFFFH
- **Physically,** memory is implemented as two independent 512 Kbyte banks: the low (even) bank and the high (odd) bank.




**(a) Logical memory organization, and (b) Physical memory organization (high and low memory banks) of the 8086 microprocessor.**

# Memory Interfacing(Odd and Even Bank)

**8086 MP**

AL = 20 => 2^20 = 1M

DL = 16 (Lower order data lines : D0-D7) => even memory bank

(Higher order data lines: D8-D15) => odd memory bank

Total memory size = 1MB

Two separate memory banks : Even bank and Odd bank

Even bank: Contains all the memory addresses which are **even** in number

00000 H, 00002 H, 00004 H....., FFFFEH

Odd bank: Contains all the memory addresses which are **odd** in number

00001H, 00003H, 00005H,....., FFFFFH

# Bank Selection

To distinguish between odd and even bytes, the CPU provides a signal called BHE’ (bus high enable).
BHE’ and A0 are used to select the odd and even byte, as shown in the table below :

| BHE' | A0 | Bank selection |
|---|---|---|
| 0 | 0 | Both the bank (16 bit data transfer) |
| 0 | 1 | data transfer from odd bank (8 bit data transfer) |
| 1 | 0 | data transfer from even bank (8 bit data transfer) |
| 1 | 1 | no data transfer (none of the banks are selected) |

# Memory Interfacing(Odd and Even Bank)

A0 and BHE' (Bus High Enable) = 0 => odd bank is selected
Address lines: A19 A18..... A1 A0
A0 = 0 **=> Even Bank is selected**

0 => 000
2 => 010
4 => 100
6 => 110
8=> 1000

1 => 001
3 => 011
5 => 101
7 => 111
9 => 1001

# Exercise: 1

- Interface microprocessor 8086 with two numbers of IC-27512 chip.

Soln:
Given:
8086 MP,
2 nos of IC 27512 (EPROM)

Memory size : 512 kilobits => 512/8 = 64kB = 2^16 x 8

AL= 16, DL = 8

**Even bank (A0 = 0)**
starting address:
final address:

**Odd bank (A0 = 1)**
starting address:
final address:

# Exercise: 1

EVEN BANK

| | | | A15 | A14 | A13 | A12 | A11 | A10 | A9 | A8 | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | A19 | A18 | A17 | A16 | A15 | A14 | A13 | A12 | A11 | A10 | A9 | A8 | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 | |
| Starting Address | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | E0000H |
| Final Address | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | FFFFEH |

ODD BANK

| | | | A15 | A14 | A13 | A12 | A11 | A10 | A9 | A8 | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | A19 | A18 | A17 | A16 | A15 | A14 | A13 | A12 | A11 | A10 | A9 | A8 | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 | |
| Starting Address | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | E0001H |
| Final Address | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | FFFFFH |

# Exercise: 1

**Even bank (A0 = 0)**
starting address: E0000H
final address: FFFFEH

**Odd bank (A0 = 1)**
starting address: E0001H
final address: FFFFFH

# Exercise: 2

- Interface 16k✖ 8 memory locations for microprocessor 8086. The starting of the microprocessor is C0000H.

Soln:

Given:
8086 MP
Number of memory locations: 16k x 8 => odd bank + even bank

# Exercise: 2

Starting address: C0000H

**Odd bank: 8k x 8 => 2^13 x 8 => 13 address lines (A0-A12)**
**Even bank: 8k x 8 => 2^13 x 8 => 13 address lines (A0-12)**

Starting address of EB = C0000H
Final address of EB = C3FFEH

Starting address of OB = C0001H
Final address of OB = C3FFFH

# Exercise: 2


EVEN BANK
A12 A11 A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0
A19 A18 A17 A16 A15 A14 A13 A12 A11 A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0
Starting Address 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 C0000H
Final Address 1 1 0 0 0 0 1 1 1 1 1 1 1 1 1 1 1 1 1 0 C3FFEH
ODD BANK
A12 A11 A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0
A19 A18 A17 A16 A15 A14 A13 A12 A11 A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0
Starting Address 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 C0001H
Final Address 1 1 0 0 0 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 C3FFFH

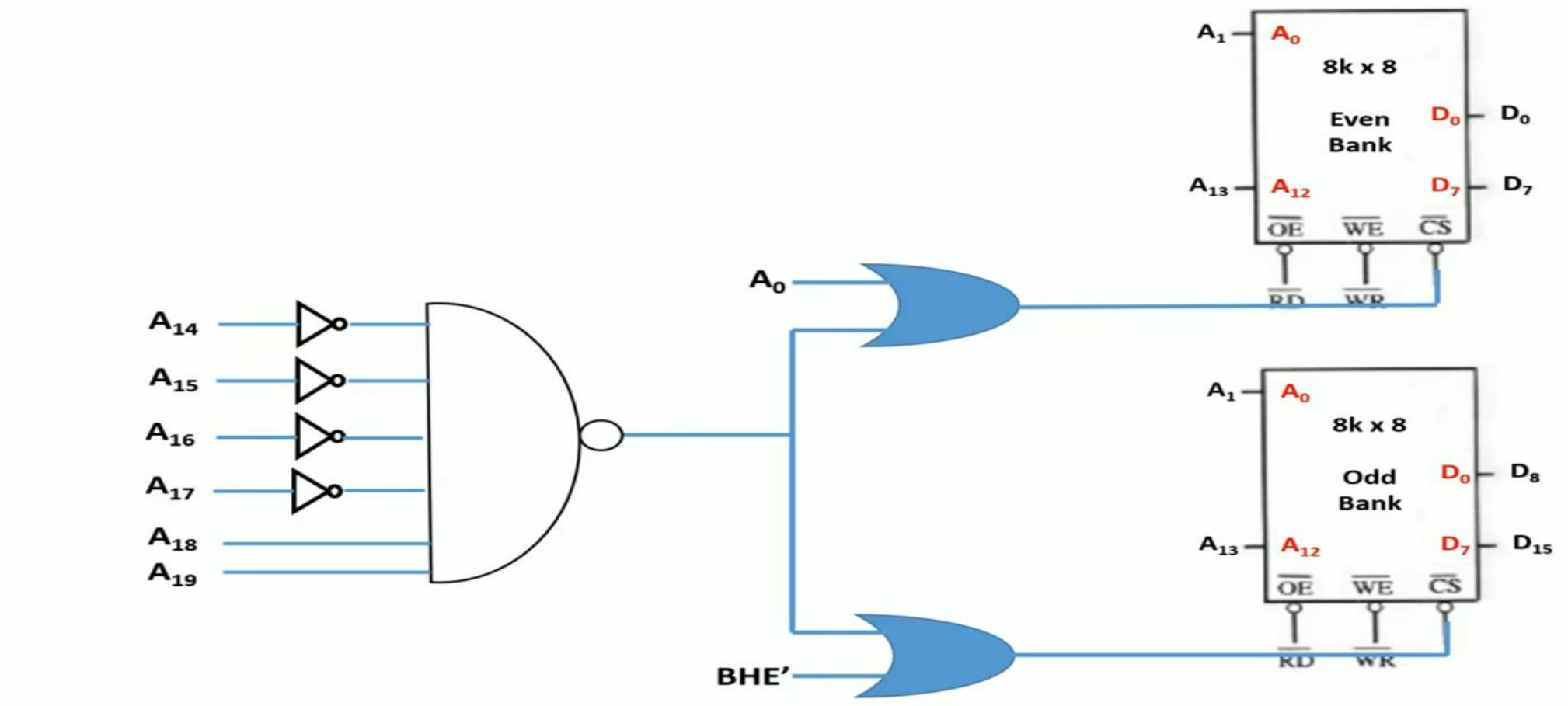
# Exercise: 3

- Interface 16k  8 memory locations for microprocessor 8086 using Multi-input NAND gate. The starting of the microprocessor is C0000H.
- 1st step: same as previous solution.

Now, the fixed line inputs are

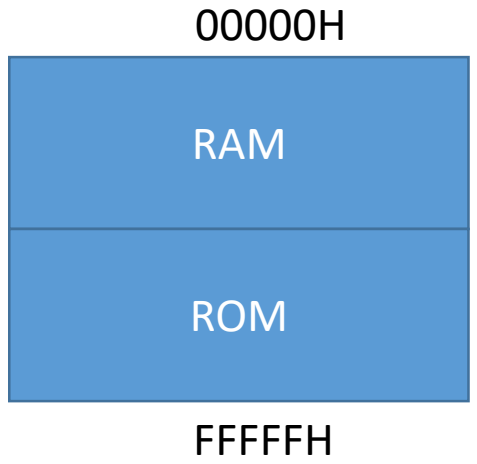
| A19 | A18 | A17 | A16 | A15 | A14 |
|---|---|---|---|---|---|
| 1 | 1 | 0 | 0 | 0 | 0 |

2nd step:


A14
A15
A16
A17
A18
A19
A0
BHE'
A1
A0
8k x 8
Even
Bank
D0
D0
A13
A12
D7
D7
OE
WE
CS
RD
WR
A1
A0
8k x 8
Odd
Bank
D0
D8
A13
A12
D7
D15
OE
WE
CS
RD
WR

# Exercise: 4

Interface two 4KX8 EPROM and two 4KX8 RAM chips with 8086.




**Solution:**

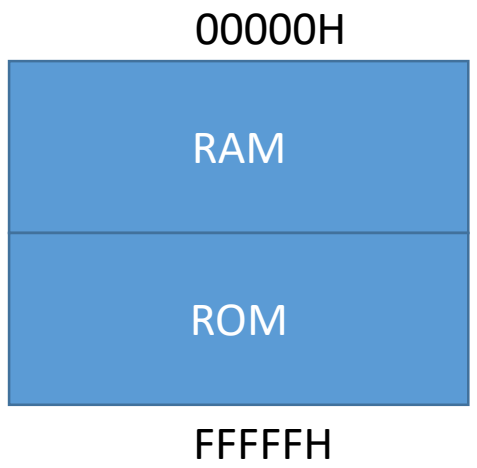
- Capacity of ROM for 2 Chips = 4K X 8 X 2 = 8K X 8 = 8KB
- Consider, Ending Address of ROM = FFFFF H
- Now, Size = 8KB = 2^3 X 2^10 = 2^13
  So, 0000 0001 1111 1111 1111 = 01FFF H
- Now, Starting Address of ROM = FFFFF H – 01FFF H = FE000 H
- Again consider, Starting Address of RAM = 00000 H
- For 4KB = 2^2X2^10 = 2^12
- So, Address Lines = A1 – A12
- A0=Bank Selection

# Exercise: 4

| | | | | | | | | | EVEN BANK | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | A19 | A18 | A17 | A16 | A15 | A14 | A13 | A12 | A11 | A10 | A9 | A8 | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 | |
| RAM1 | Starting Address | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | **00000 H** |
| | Ending Address | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | **01FFE H** |
| | | | | | | | | | ODD BANK | | | | | | | | | | | | | |
| RAM2 | Starting Address | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | **00001 H** |
| | Ending Address | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | **01FFF H** |
| | | | | | | | | | EVEN BANK | | | | | | | | | | | | | |
| ROM1 | Starting Address | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | **FE000 H** |
| | Ending Address | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | **FFFFE H** |
| | | | | | | | | | ODD BANK | | | | | | | | | | | | | |
| ROM2 | Starting Address | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | **FE001 H** |
| | Ending Address | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | **FFFFF H** |

# Exercise: 5

Interface 32KB ROM using 8 KB ROM and 32KB RAM using 16 KB chips with 8086.




**Solution:**

- Required number of ROM = 32/8 = 4
- Required number of RAM = 32/16 = 2
- So, we need four 8KB ROM and two 16 KB RAM chips for interfacing
- Consider, Ending Address of ROM = FFFFF H
- Now, Size = 32KB = 2^5 X 2^10 = 2^15

  So, 0000 0111 1111 1111 1111 = 07FFF H
- Now, Starting Address of ROM = FFFFF H – 07FFF H = F8000 H
- Again consider, Starting Address of RAM = 00000 H
- For 16KB = 2^4X2^10 = 2^14
- So, Address Lines = A1 – A14
- A0=Bank Selection

# Exercise: 5

| | | | | | | | | | EVEN BANK | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | A19 | A18 | A17 | A16 | A15 | A14 | A13 | A12 | A11 | A10 | A9 | A8 | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 | |
| RAM1 | Starting Address | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | **00000 H** |
| | Ending Address | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | **07FFE H** |
| | | | | | | | | | ODD BANK | | | | | | | | | | | | |
| RAM2 | Starting Address | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | **00001 H** |
| | Ending Address | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | **07FFF H** |
| | | | | | | | | | EVEN BANK | | | | | | | | | | | | |
| ROM1 | Starting Address | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | **F8000 H** |
| | Ending Address | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | **FBFFE H** |
| | | | | | | | | | ODD BANK | | | | | | | | | | | | |
| ROM2 | Starting Address | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | **F8001 H** |
| | Ending Address | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | **FBFFF H** |
| | | | | | | | | | EVEN BANK | | | | | | | | | | | | |
| ROM3 | Starting Address | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | **FC000 H** |
| | Ending Address | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | **FFFFE H** |
| | | | | | | | | | ODD BANK | | | | | | | | | | | | |
| ROM4 | Starting Address | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | **FC001 H** |
| | Ending Address | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | **FFFFF H** |