Experiment 1: Full Adder Experiment

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1.1 Experimental Purpose

1）How to use the experimental system.

2) Master the logical structure and circuit implementation methods of full adders.

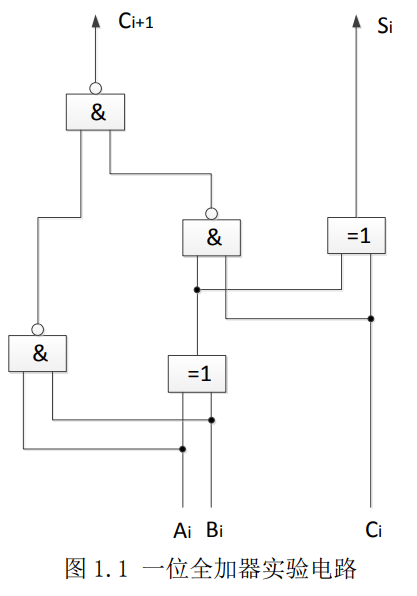
1.2 Experimental Requirements

1) Prepare for the experiment by reviewing the principles of full adders and mastering the functional characteristics of experimental components.

2) In accordance with the requirements of the experimental content and procedures, independently think and carefully complete the experiment.

1.3 Experimental Circuit

The main components used in this experiment include NAND gates, XOR gates, switches, and indicator lights.



The logic structure of a full adder is shown in Figure , where the control signals and data signals involved are as follows:

1) Ai, Bi: Two binary digital inputs.

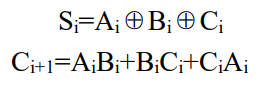
2) Ci: Carry input.

3）Si：sum output.

4） Ci+1: Carry output.

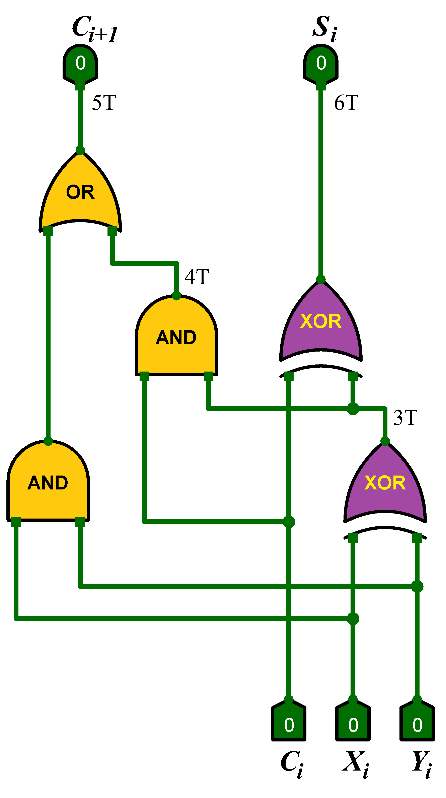
1.4 Experimental principle

A 1-bit binary adder has three inputs: two binary numbers Ai and Bi, and a carry signal Ci with a lower bit,The three values add up to produce a sum output Si and a carry output Ci+1 to the upper bit. This kind of adder unit is called a full adder, and its logic equation is as follows:



1.5 Experimental Contents and Procedures

Run the virtual experimental system, select the required components from the experimental equipment list on the left and drag them to the workspace. As shown in Figure 1.1, build the experimental circuit to obtain the experimental circuit shown in Figure.



2. Turn on the power switch, set the data switch according to the input signal in Table 1-1, and fill in the output values in Table 1-1 based on the operational results displayed on the indicator light.

**Report of My Full Adder Experiment:**

**Truth Table:**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| input | | | output | |
| Ai | Bi | Ci | Si | Ci+1 |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 |

Table 1-1: Truth Table for an Full Adder

**Full Adder Circuit Diagram**

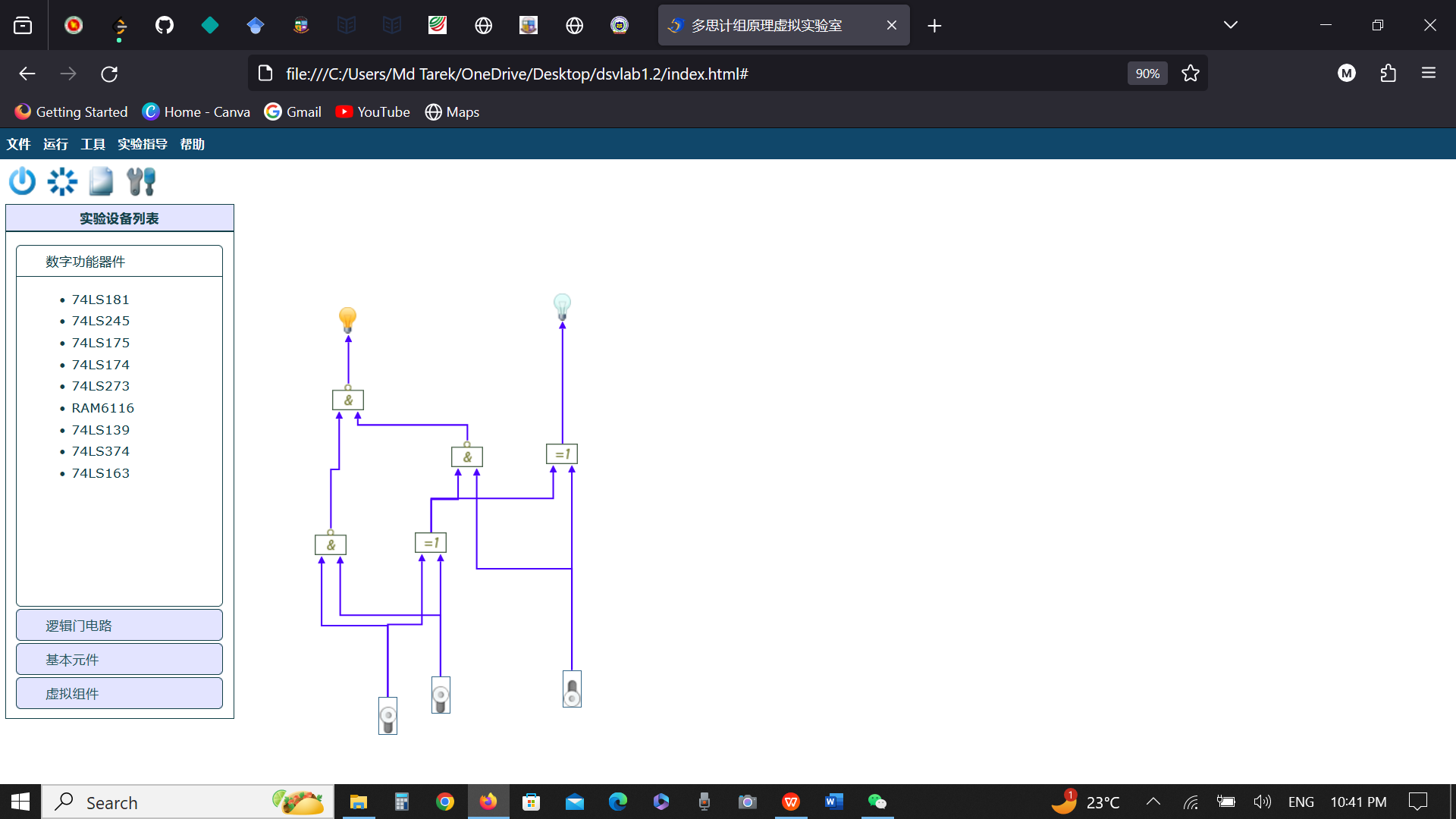


Figure: Full Adder