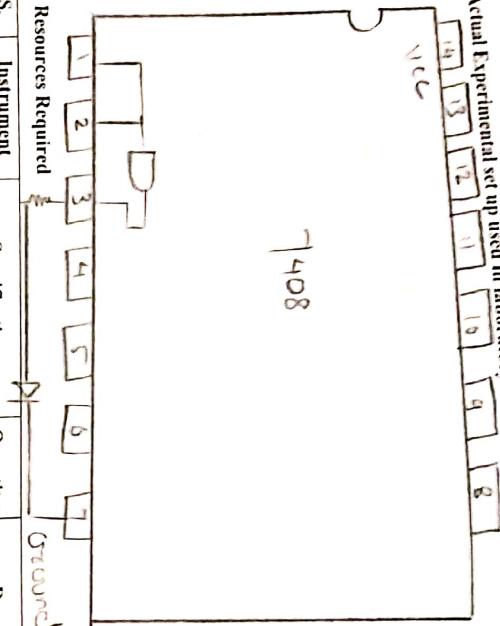


c) Actual Experimental set up used in laboratory



S. No.	Instrument Components	Specification	Quantity	Remarks
1	Digital Multimeter	Digital Multimeter: 3 1/2 digit display.	2	
2	Digital IC Tester	Tests a wide range of Digital IC's such as 74 Series, 4045 Series of CMOS IC's.	1	
3	DC power supply	+5 V Fixed power supply	1	
4	Breadboard	5.5cm X 17 cm	1	
5	IC	7486, 7404, 7432, 7408	1 Each	
6	LED	Red/Yellow color 5 mm	1	
7	Connecting wires	Single strand 0.6 mm Teflon coating required	As required	
8	Resistor	1.1 KΩ or 330Ω	As required	

XV Observations and Calculations

Table I.1: Observation table

## XII Resources used (with major specifications)

S. No.	Instrument / Components	Specification	Quantity
1.	Bread board	5cm x 17cm	1
2.	LED	Red 5mm	1
3.	Resistor	130 $\Omega$	1
4.	T <sub>C</sub>	T4041,T4087,T38	1 Each
5.	Connecting wires		6 for each

AIX

**X** **Precautions to be followed**  
Do not switch ON the power supply unless you have checked the circuit connections as per the circuit diagram.

- Make the connections as per figure 1.1 on breadboard and test with digital IC Tester.
  - Observe the LED (on or off) for each combination of input as per truth table.
  - Verify the truth table.
  - Repeat the process for IC 7404, 7432, 7486.

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**IX** **Practical Related Questions**  
*Note: Below given are few sample questions for reference. Teachers must design more such questions so as to ensure the achievement of identified CO.*

- Write down voltage at logic level 0 and 1.
- List the function of pin 7,1401C 7432.
- State the effect if pin number 14 is connected to ground and pin number 7 is connected to VCC.
- List numbers of NOT gates are available in IC 7404.
- List the name of manufacturers of Digital IC used in your lab.
- State the need for the resistor connected in series with LED. Write down the value of resistor.
- State the significance of LS of IC number 74LS00.

[Space for answer]

↳ Voltage at logic 0 & 1 as follows :

Technology logic level Voltage logic level [6]

1) CMOS 0V to 13V VCC 2) 3V VCC 10V

2) TTL 0V to 0.8V to 2V to 10V VCC

↳ Function of pin 9 in IC 7482 is providing ground to the rest of circuit.

The function of pin 14 in IC 7432 is ensuring supply to other pin.

These are based on concept of voltage rails. A ground rail is a common rail.

↳ Output can't get correctly.

↳ No - or Not gate are available in IC 7404. 6

↳ Low - power implementation using the same technology as 74S but with reduce power. IC Not gate delay a remarkable 2 nV, deppression 4.5 - 52.5 V.

**XI**

**Assessment Scheme**

Performance indicators		Weightage
Process related:15 Marks		60%
1	Verification of voltage	10 %
2	Handling of the components/IC	10 %
3	Identification of component/IC	10 %
4	Mounting of IC on Breadboard	20 %
5	Working in team	10 %
Product related:10 Marks		40%
6	Result	10 %
7	Interpretation of result	05 %
8	Conclusions	05 %
9	Answers to Practical related questions	15 %
10	Submitting the journal in time	05 %
Total (25 Marks)		100 %

*Names of Student Team Members*

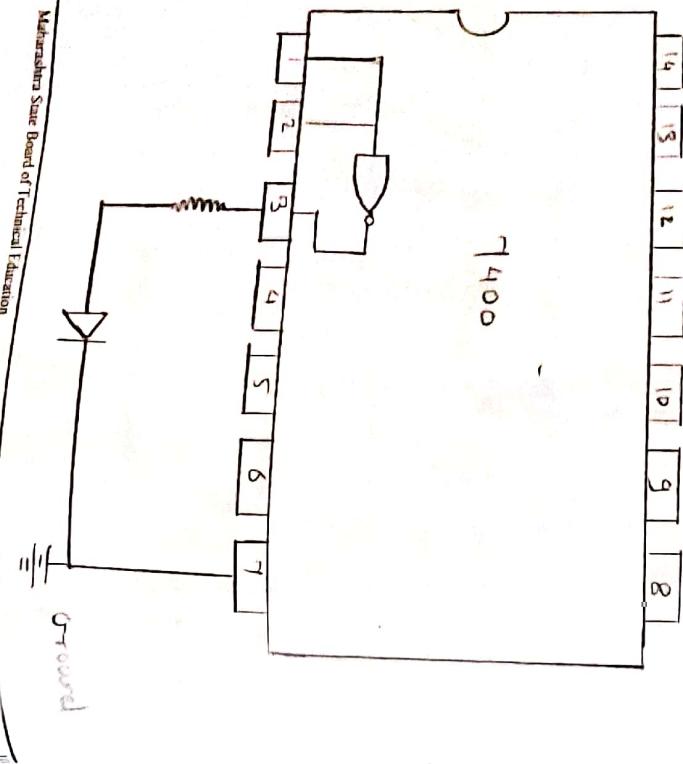
- Chougale Pranav
- Borkar Alka
- Sherdarsh Kshetra
- .....

Marks Obtained	Dated signature of Teacher
Process Related(15) Product Related(10)	Total (25)

b) Actual Circuit used in laboratory

S. No.	Instrument /Component	Specification	Quantity	Remarks
1.	Digital Multimeter	Digital Multimeter 3 1/2 digit display	1	
2.	Digital IC Tester	Tests a wide range of Digital IC's such as 74 Series, 4045 Series of CMOS IC's	1	
3.	DC power supply	+5 V Fixed power supply	1	
4.	Breadboard	5.5cm X 17 cm	1	
5.	IC	7400, 7402	1 Each	
6.	LED	Red Yellow color 5 mm	1	
7.	Connecting wires	Single strand 0.6 mm Teflon coating	As required	
8.	Resistor	1KΩ or 330Ω	As required	

c) Actual Experimental set up used in laboratory



X Precautions to be Followed  
Do not switch ON the power supply unless you have checked the circuit connections as per the circuit diagram.

XI Procedure

- Identify pin configuration of logic gate IC (7400) and test with digital IC tester.
- Make the connections as per figure 2.3 on breadboard and give supply voltage to relevant pin as per logic level.
- Observe the LED (on or off) for each combination of input as per truth table.
- Verify the truth table.
- Repeat the process for IC 7402.

XII Resources used (with major specifications)

S. No.	Instrument / Components	Specification	Quantity
1.	Bread board	5.5 X 17 cm	1
2.	LED	RED 5mm	1
3.	Resistor	130 Ω	1
4.	Connecting wire	7400, 7402 1m each	6-Ft, each IC
5.	IC	7400, 7402	1-For each

XIII Actual procedure followed (use blank sheet provided if space not sufficient)  
Identify pin configuration of logic gate IC (7400). Test with digital IC tester. Make connection as per fig. on breadboard. Give supply voltage to relevant pin, observe LED for each combination of inputs.

- XIV** Precautions followed (Use blank sheet provided if space not sufficient)
- 1) Did not switch on power supply.
  - 2) checked the connection as per diagram.
  - 3) checked that LED is grounded or not.

**XV Observations and Calculations.**

Table 2.1

		7400 (NAND)		7402(NOR)	
Inputs		LED Status (ON/OFF)	Output voltage (ON/OFF)	LED Status (ON/OFF)	Output voltage (ON/OFF)
0(V)	0(V)	ON	2.60	ON	3.19
0(V)	1(V)	ON	2.59	OFF	0.55
1(V)	0(V)	ON	2.61	OFF	0.34
1(V)	1(V)	OFF	0.21	OFF	0.23

**XVI Results**

	A	B	V	A	B	Y
Truth	0	1	1	0	1	0
Table	1	0	0	1	1	0

**XVII Interpretation of results (Give meaning of the above obtained results)**

1) Output of NAND gate is low if both inputs are high.

- 2) Output of NOR gate is low if anyone or all inputs are high.

**XVIII Conclusions & Recommendation** (Actions decisions to be taken based on the interpretation of results)

Both NAND & NOR gate has been checked.

**XIX**

**Practical Related Questions**

Note: Below given are few sample questions for reference. Teachers must design more such questions so as to ensure the achievement of identified CO.

1. List the function of pin 7 and 14 of IC 7400
2. Write down name of manufacturer of Digital IC 7400, 7402 used in practical
3. Suggest another IC used as NAND, AND, NOR Gate.
4. Write the IC no which has three input NAND & NOR gate.

[Space for answer]

→ In 7400 IC, pin 7 is grounded connected  
pin 14 B-the 15 V power supply

c) Actual Experimental set up used in laboratory

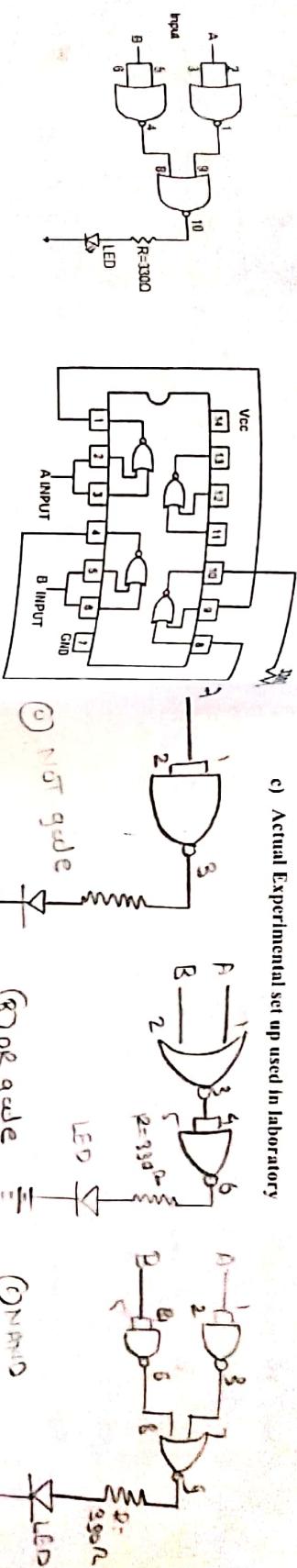


Figure (a) Figure (b)  
Figure 3.5. AND Gate using NOR a) Logic diagram b) IC Circuit diagram

Vcc

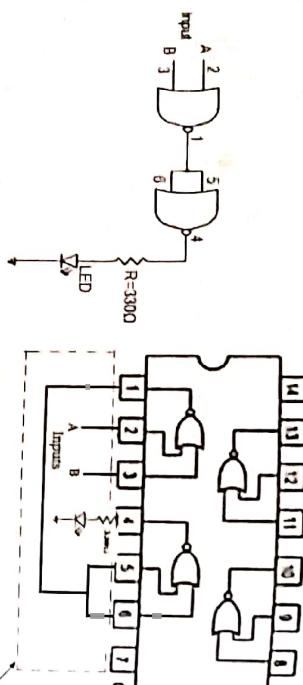
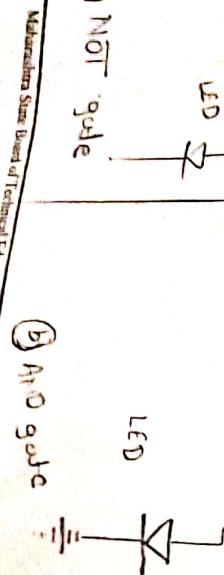
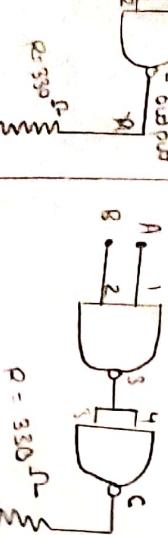


Figure (a) Figure (b)  
Figure 3.6. OR Gate using a NOR a) Logic diagram b) IC Circuit diagram

b) Actual Circuit used in laboratory



IX

Resources Required

S. No.	Instrument /Components	Specification	Quantity	Remarks
1.	Digital Multimeter	Digital Multimeter: 3 1/2 digit display.	2	
2.	Digital IC Tester	Tests a wide range of Digital IC's such as 74 Series, 40045 Series of CMOS IC's.	1	
3.	DC power supply	+5 V Fixed power supply	1	
4.	Breadboard	5.5 cm X 17 cm	1	
5.	IC	7400, 7402	1 Each	
6.	LED	Red/Yellow color 5 mm	1	
7.	Connecting wires	Single strand 0.6 mm Teflon coating	As required	
8.	Resistor	1KΩ/330Ω	As required	

X Precautions to be Followed  
Do not switch ON the power supply unless you have checked the circuit connections as per the circuit diagram.

XI Procedure

1. Identify pin configuration of logic gate IC 7400 and test with digital IC Tester
2. Make the connection as shown in figure 3.1-3 on breadboard and give supply voltage to relevant pins per logic level
3. Observe the LED (on/off) for each combination of input as per truth table
4. Verify the truth table.
5. Repeat the process for figure 3.4-16

**XII Resources Used**

S. No.	Instrument / Components	Specification	Quantity
1.	Printed board	5.5 x 17 cm	1
2.	LED	LED 5 mm	1
3.	Resistor	130 Ω	1
4.	Multimeter	7400	1

XIII Actual procedure followed (Use blank sheet provided if space not sufficient)  
Identified pin diagram at ICs made different connection  
verified through table.

XIV Precautions followed (Use blank sheet provided if space not sufficient)  
Digital switched on power supply unless  
we had checked the circuit.

**XV Observations and Calculations**

Table 3.1: Observations

Inputs	AND		OR		NOT	
	A	B	LED Status (ON/OFF)	Output voltage	LED Status (ON/OFF)	Output voltage
0(V)	0(V)	0(V)	OFF	0.4	OFF	0.18
0(V)	1(5V)	0(V)	OFF	0.04	ON	3.36
1(5V)	0(V)	0(V)	OFF	0.19	ON	3.51
1(5V)	1(5V)	0(V)	ON	3.14	ON	2.92

**XVI Results**

Output of AND gate is low if both inputs are low or either one input is low.

**XVII Interpretation of results (Give meaning of the above obtained results)**

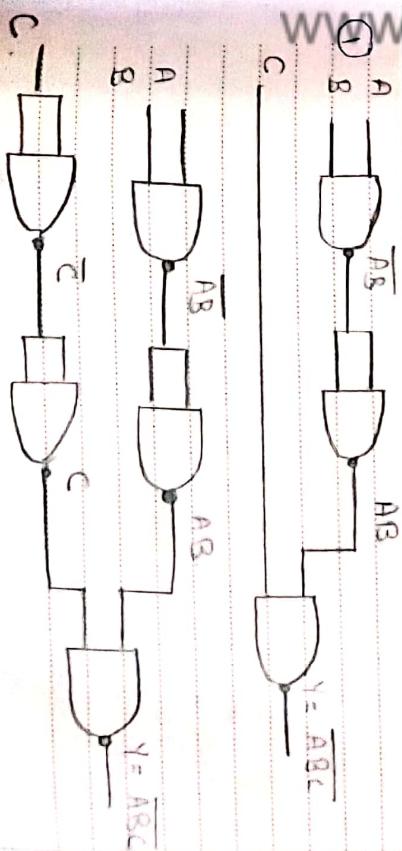
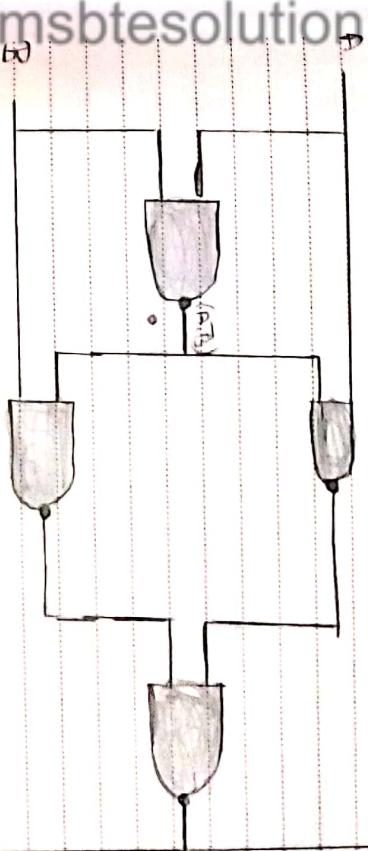
Various basic gates output can be obtained through universal gates.

**XVIII Conclusions & Recommendation** (Actions/decisions to be taken based on the interpretation of results)

Use observed various gates using NAND OR, NOR, Universal gates.

- XIX Practical Related Questions**  
*Note: Below given are few sample questions for reference. Teachers must design more such questions so as to ensure the achievement of identified CO*
1. Design 3 input NAND gate using 2 input NAND gate IC 7400.
  2. Draw EX-OR gate using NAND Gates
  3. Write name of manufacturers of Digital IC 7400, 7402 used in your lab.
  4. What is the significance of L, LS and H in the following IC 74L00, 74LS00, and 74H00?

[Space for answer]



**De Morgan's second Theorem** It states that for any two elements A and B in Boolean algebra, the complement of a product is equal to the sum of the complements.

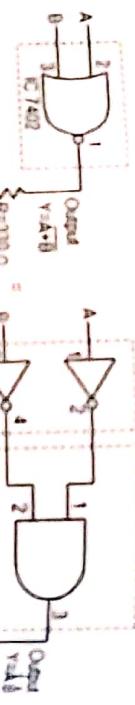
The theorem can be expressed by logic circuit as

$$\overline{AB} = \overline{A} + \overline{B}$$

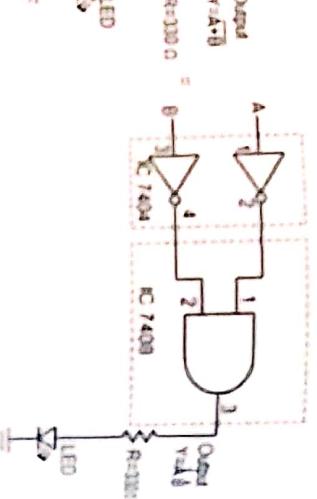
NAND gate or Bubbled OR gate

### VIII Practical Circuit diagram

#### a) Sample



#### b) De Morgan's first theorem



#### c) Actual Experimental set up used in laboratory

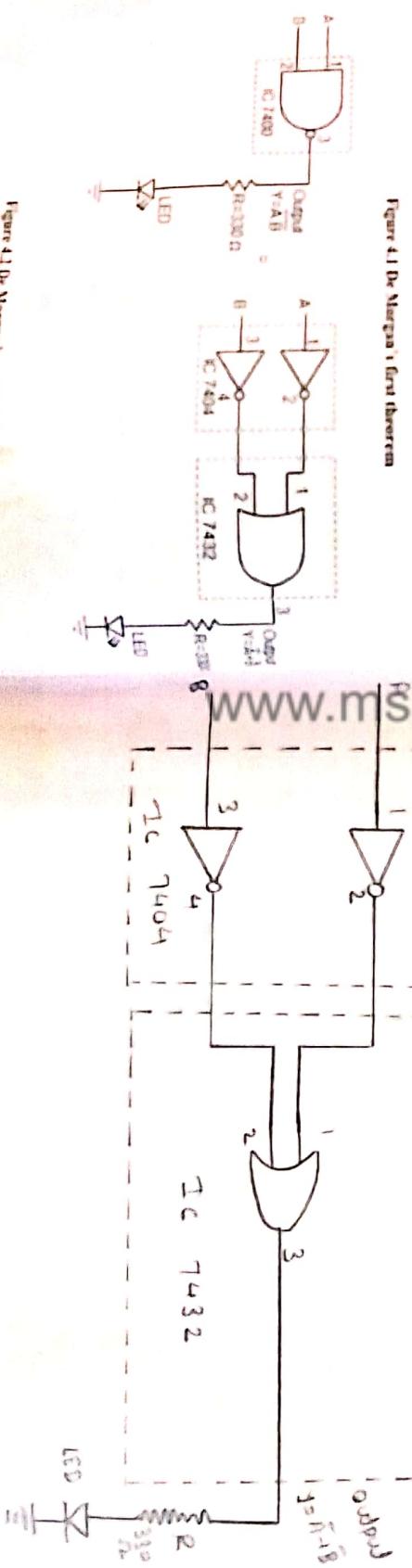
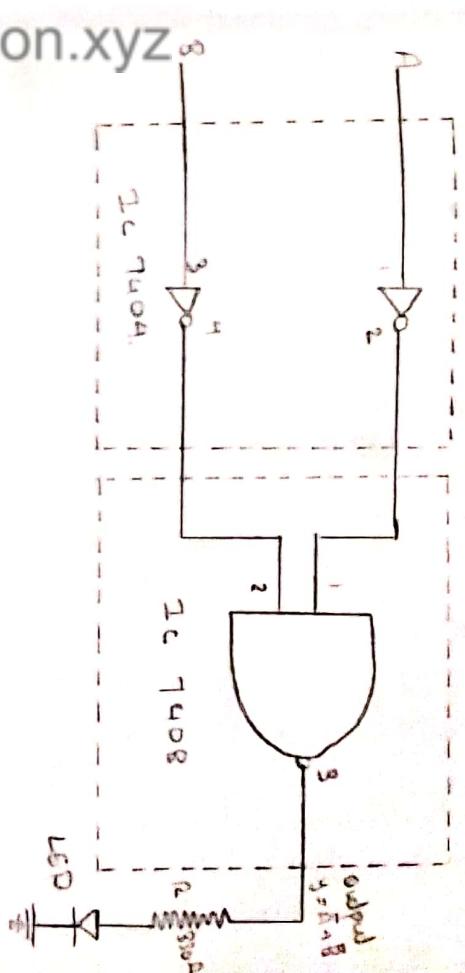


Figure 4.1 De Morgan's second theorem



IX Resources Required			XV Observations and Calculations		
S. No.	Instrument / Components	Specification	Quantity	Remarks	
1.	Digital Multimeter	Digital Multimeter: 3 1/2 digit display.	2		
2.	Digital IC Tester	Tests a wide range of Digital IC's such as 74 Series, 4045 Series of CMOS IC's.	1		
3.	DC power supply	+5 V Fixed power supply	1		
4.	Breadboard	5.5cm X 17 cm	1		
5.	IC	7404,7432,7402,7208,	1 Each		
6.	LED	Red/Yellow color 5 mm	1		
7.	Connecting wires	Single strand 0.6 mm Teflon coating	As required		

X Precautions to be Followed		
Do not switch ON the power supply unless you have checked the circuit connections as per the circuit diagram.		
XI Procedure		
1. Identify pin configuration of logic gate IC and test with digital IC Tester.		
2. Make the connections as per figure 4.1 on breadboard and give supply voltage as per the circuit diagram.		
3. Observe the LED (on or off) for each combination of input as per truth table.		
4. Verify the truth table.		
5. Repeat the process for figure 4.2.		

XII Resources Used		
1.	Instrument / Components	Specification
2.	Bread board	5.5 cm X 17 cm
3.	LED	Red 5 mm
4.	Resistor	130 $\Omega$
5.	Connecting wire	7400,7404,7432

XIII Actual procedure		
Identify pin configuration of logic IC and connection of tester observe for each combination of input.		

XIV Precautions followed		
Do not Substituted unless you have checked the power supply connection.		

XV Observations and Calculations		
Note: Below given are few sample questions for reference. Teachers must design more such questions so as to ensure the achievement of identified CO.		

Table 4.2: De Morgan's second theorem observation:

Inputs	Outputs
A      B	LHS = $\bar{A} \cdot \bar{B}$ RHS = $\bar{A} + \bar{B}$
0      0	ON      ON
0      1	OFF      ON
1      0	OFF      OFF
1      1	OFF      OFF

XVI Results		
The O/P of $\bar{A} \cdot \bar{B}$ and $\bar{A} + \bar{B}$ is same also		

XVII Interpretation of results (Give meaning of the above obtained results)		
One low the O/P of $\bar{A} \cdot \bar{B}$ & $\bar{A} + \bar{B}$ is high if both are bubbled or gated.		

XVIII Conclusions & Recommendation (Actions/decisions to be taken based on the interpretation of results)		
O/P of NOR gate is equal to bubbled & gate of O/P of NAND gate is equal to bubbled OR gate.		

XIX Practical Related Questions		
Note: Below given are few sample questions for reference. Teachers must design more such questions so as to ensure the achievement of identified CO.		

XIX Practical Related Questions		
1. List the IC numbers used in De Morgan's first theorem 2. List the IC numbers used in De Morgan's second theorem 3. Why do we reduce the expression with the help of Boolean algebra and De Morgan's theorem?		

## [Space for answer]

① 7402  
7404  
7408

② 7400  
7404  
7432

5) After wiring up a logic circuit, the  
sample the boolean expression.

## XXI Assessment Scheme

Performance indicators		Weightage
	Process related	15 Marks
1	Identification of pin configuration of logic Gate IC	10 %
2	Proper Testing of IC	10 %
3	Mounting of IC on Breadboard	20 %
4	Circuit connection	10 %
5	Working in team	10 %
Product related: 10 Marks		40 %
6	Result	10 %
7	Interpretation of result	05 %
8	Conclusions	05 %
9	Answers to Practical related questions	15 %
10	Submitting the journal in time	05 %
Total (25 Marks)		100 %

## Names of Student Team Members

1. Chougule, Maini
2. Bankale, Nitin
3. Shendurde, Akash
4. ....

	Marks Obtained	Dated signature of Teacher
Process Related(15)	Product Related(10)	Total (25)

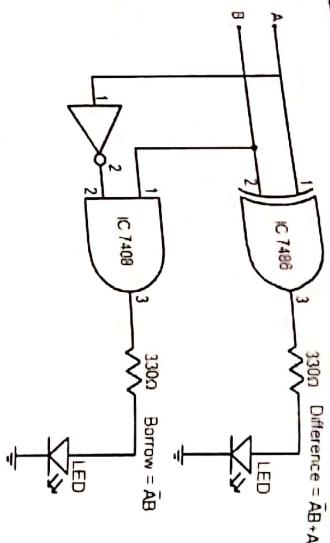


Figure 5.4 Half subtractor Circuit

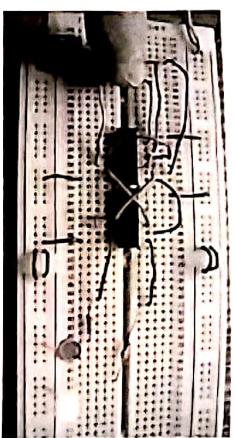
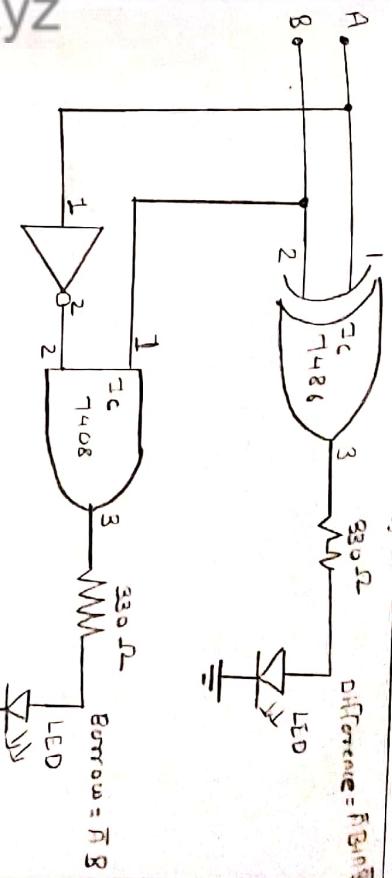


Fig 5.5 Practical Setup

## b) Actual circuit used in laboratory



## www.msbtresolution.xyz

### Fig Half Subtractor Circuit

## IX Resources Required

S. No.	Name of Resource	Suggested Broad Specification	Quantity	Remark
1.	Digital Multimeter	Digital Multimeter: 3 1/2 digital display	1	
2.	IC Tester	Digital IC Tester	1	
3.	Breadboard	5.5cm X 17 cm	1	
4.	DC power supply	+5 V Fixed power supply	1	
5.	IC 1	7404	1	
6.	IC 2	7404	1	
7.	IC 3	7408	1	
8.	LED	Red Yellow color 5 mm	2	
9.	Connecting wires	Single strand 0.6 mm Teflon coating	AS required	
10.	Resistors	330 ohm 0.25 W	2	

X Precautions to be followed  
Do not switch ON the power supply unless you have checked the circuit connections as per the circuit diagram.

## XI

## Procedure

1. Test the IC's using IC tester
2. Mount IC's on breadboard
3. Set up a half adder and half subtractor circuit and feed all the input combinations
4. Observe the outputs corresponding to input combinations on LEDs.
5. Fill up the observation table.
6. The supply voltage to the IC's should not exceed +5V.

Fig. Half subtractor Circuit

XII Resources Used		Specification	Quantity
S. No.	Instrument / Components		
1.	Bread board	5.5 cm x 17 cm T486, T408, T401	1
2.	Digital wires	0.66 mm	2
3.	Connecting wires	0.55 V 320 Ω / 5.5 V	2
4.	Resistor	5 mm LED	2
5.	LED		1

XIII Actual Procedure followed (Use blank sheet provided if space not sufficient)

Mounted 16 chip set half adder and full adder all input terminals

XIV Precautions followed (use blank sheet provided if space not sufficient)  
Didn't switch on the power supply unless we had checked circuit combination as per circuit diagram.

XV Observations and Calculations:

Observation Table for Half Adder

Input A	Input B	Output Sum	Output Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Observation Table for Half Subtractor

Input A	Input B	Output Difference	Output Borrow
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

XVI Results

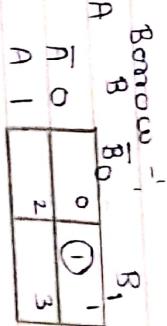
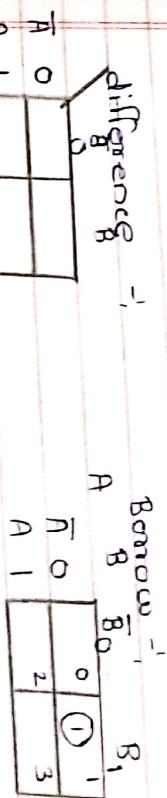
Output of half adder sum is high if any one is high. Output of half adder is carry if both inputs are high output of four adder sum is high.

$$\begin{array}{c}
 \text{difference} \\
 \begin{array}{|c|c|c|c|} \hline
 & & & \\ \hline
 \bar{A} & 0 & & \\ \hline
 & & & \\ \hline
 & & & \\ \hline
 \end{array}
 \end{array}
 \quad
 \begin{array}{c}
 \text{borrow} \\
 \begin{array}{|c|c|c|c|} \hline
 & & & \\ \hline
 A & \bar{B} & \bar{B}_1 & B_1 \\ \hline
 \bar{A} & 0 & 0 & 1 \\ \hline
 & & 1 & 0 \\ \hline
 & & 2 & 1 \\ \hline
 \end{array}
 \end{array}$$

-1 carry

$$\begin{aligned}
 S &= \bar{A}B + A\bar{B} \\
 &= A \oplus B \\
 C &= AB
 \end{aligned}$$

• K-map for full adder



full adder using half-adder

### ① Disadvantages of half adder circuit are -

- Half adder is logic that adds 2 bits of number. It neglects carry meaning.  
If you add 1+1, it gives 0 not 10 so, in that sense a half adder is incomplete.
- ↓ That is the disadvantage.

Un.  
load

, any one  
scarry  
input

[www.msbtresolution.xyz](http://www.msbtresolution.xyz)

**XVII HALF adder**

full adder

**XVIII Interpretation of Results** (Give meaning of the above obtained results)

A	B	C	D
0	0	0	0
0	1	1	0
0	1	0	1
1	0	1	0
1	0	0	1
1	1	0	1

**XVIII Conclusions and Recommendations** (Actions/decisions to be taken based on the interpretation of results)

Practical Half Adder circuit set up properly and full adder need all input combination.

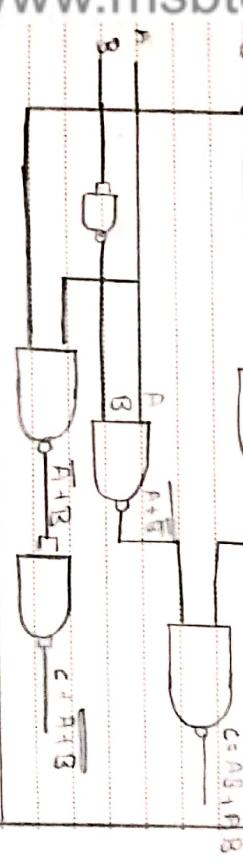
ii)

- Let us draw  
Half Adder  
circuit  
using  
NAND  
gates.
1. Write down drawback of Half Adder circuit.
  2. Draw half adder using NAND gates only.
  3. Draw Half Subtractor circuit using NAND gates.
  4. Design Half Adder/Half Subtractor using K-map.

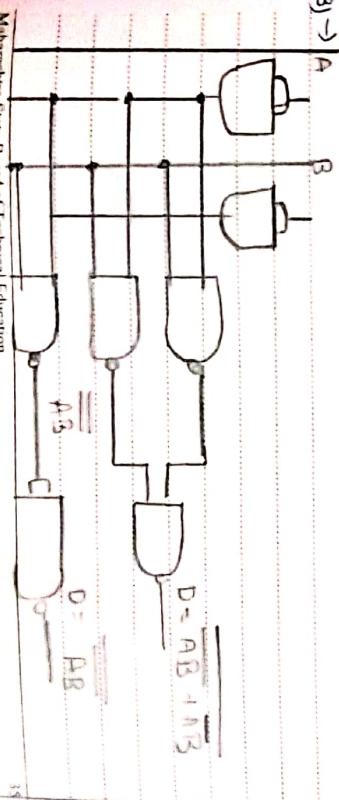
## [Space for Answers]

**XIX Practical Related Questions**  
*Note: Below given are few sample questions for reference. Teachers must design more such questions so as to ensure the achievement of identified CO*

1. Draw half adder using NAND gates only.
2. Draw Half Subtractor circuit using NAND gates.
3. Design Half Adder/Half Subtractor using K-map.



any  
; carry  
put



→ Half adder is logic that adds 2 bits of numbers. It always carry, according to you since a half adder is incomplete and that is the disadvantage.

→ Full adder is logic that adds 2 bits of numbers. It gives sum to 10, so in full adder 1+1=11 gives one. So, in full adder a half adder is incomplete and that is the disadvantage.

## XX References / Suggestions for further reading

1. <https://www.geekslonggeeks.org/half-adder-half-subtractor-using-hand-not-gates/>
2. <https://www.electronics-hub.org/binary-adder-and-subtractor/>
3. [www.sharlabs.com](http://www.sharlabs.com)
4. <https://en.wikipedia.org/wiki/Subtractor>

## XXI Assessment Scheme

Performance Indicators	Weightage
<b>Process related:15 Marks</b>	<b>60%</b>
1 Test the IC's using IC tester	10 %
2 Handling of the components/IC	10 %
3 Identification of component/IC	10 %
4 Mounting of IC on Breadboard	20 %
5 Working in team	10 %
<b>Product related:10 Marks</b>	<b>40%</b>
6 Result	10 %
7 Interpretation of result	05 %
8 Conclusions	05 %
9 Answers to Practical related questions	15 %
10 Submitting the journal in time	05%
<b>Total (25 Marks)</b>	<b>100 %</b>

## Names of Student Team Members

1. Chougule, Divyanshu
2. Bonikale, Akash
3. Shendune, Aditya
4. ....

Marks Obtained	Dated signature of Teacher
Process Related(15) Product Related(10) Total (25)	

## Practical No.6: Design Full adder and full subtractor.

### Practical Significance:

Digital computers perform variety of information tasks. Among the functions encountered are the various arithmetic operations. The most basic arithmetic operation is the addition or subtraction of binary digits. A binary adder-subtractor is a combinational circuit that performs the arithmetic operations of addition and subtraction with binary numbers. In this practical, students will build circuits and perform addition and subtraction of 3 bits.

### Relevant Program Outcomes (POs)

1. Discipline knowledge: Apply Electronics and Computer knowledge to solve broad-based Electronics and Computer engineering related problems
2. Experiments and practice: Plan to perform experiments and practices to use the results to solve broad-based Electronics and Computer engineering problems
3. Engineering tools: Apply relevant Electronics and Computer technologies and tools with an understanding of the limitations

### Competency and Practical Skills

This practical is expected to develop the following skills for the industry-identified competency through various teaching learning experiences: competency: "Build Combinational logic circuits consist of digital IC's."

- i. Testing of IC's on IC tester.
- ii. Identify pin configuration for gates
- iii. Make connections as per circuit diagram.

### Relevant Course Outcome(s)

- Build simple combinational circuits.

### Practical Outcome

- Design Full adder and full subtractor.

### Relevant Affective domain related Outcome(s)

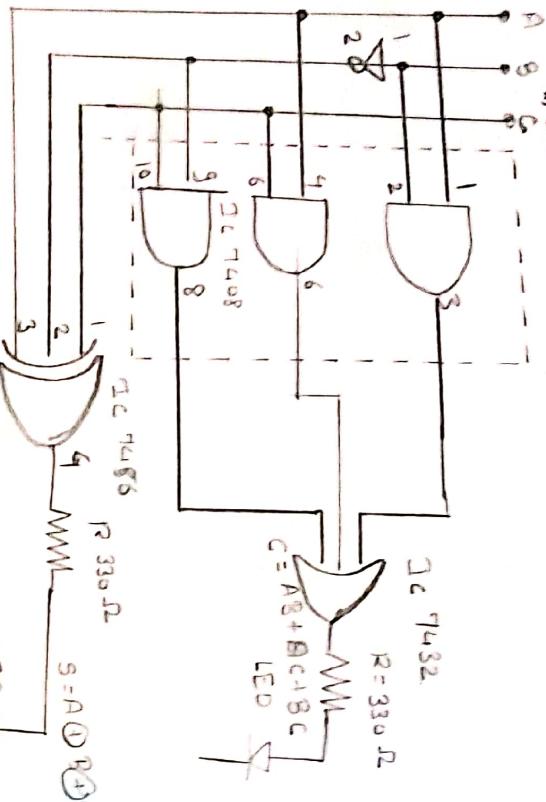
- Handle IC and equipment carefully.
- Follow safe practices.

### Minimum Theoretical Background

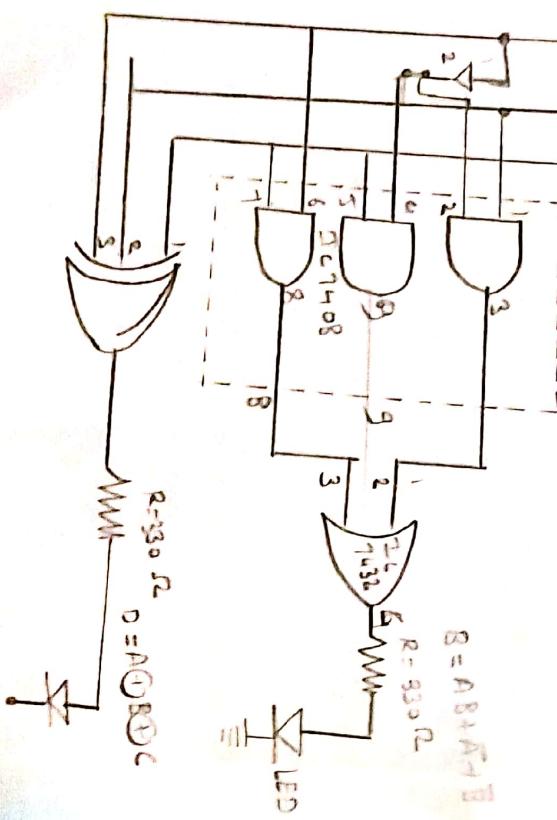
The full adder is a combinational circuit which is used to perform addition of three input bits. Full adder is difficult to implement than a half-adder. The difference between a half-adder and a full-adder is that the full-adder has three inputs and two outputs. The first two inputs are A and B and the third input is an input carry as C-IN and outputs are sum(S) and carry(C).



## a) Actual circuit used in laboratory



## b) Actual Experimental set up used in laboratory



## IX Resources Required

S. No.	Name of Resource	Suggested Board Specification	Quantity	Remark
1	Multimeter	Digital Multimeter 3 1/2 digital display	1	
2	IC Tester	Digital IC Tester	1	
3	Breadboard	5.5cm X 17 cm	1	
4	DC power supply	±5V fixed power supply	1	
5	IC 1	7486	1	
6	IC 2	7404	1	
7	IC 3	7408	1	
8	IC 4	7432	1	
9	LED	Red/Yellow color 5 mm	2	
10	Connecting wires	Single strand 0.6 mm Teflon coating	As required	
11	Resistors	330 Ω, 0.25 W	2	

**Precautions to be followed**  
Do not switch ON the power supply unless you have checked the circuit connections as per the circuit diagram.

## X Procedure

- Test the IC's using IC tester.
- Mount IC's on breadboard.
- Understand working of all the circuit
- Set up full adder and half subtractor circuit and feed all the input combinations
- Observe the outputs corresponding to input combinations on LEDs
- Fill up the observation table
- The supply voltage to the IC's should not exceed +5V.

## XI Resources Used

S. No.	Instrument / Components	Specification	Quantity
1	Bread board	5.5 x 17 cm	1
2	LED	5 mm	2
3	Resistor	1/32, 1/48, 1/96 Ω	2 for each
4	IC	7432, 7486, 7408	1 for each
5	multimeter		

## XII Actual Procedure Followed (Use blank sheet provided if space not sufficient)

- Make connection as per logic observe LED in off state to pin per logic observe LED in off condition.
  - Switch on power supply checked connection.
- XIV Precautions Followed (Use blank sheet provided if space not sufficient)
- Did not switch on power supply checked connection.
  - As per diagram checked and carboode off LED grounded or Not

XV Observations and Calculations:-

Observation Table for Full Adder:-

Input			Output	
A	B	C	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Observation Table for Full Subtractor:-

Input			Output	
A	B	C	Difference	Borrow
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

4) Full adder using K-map.

$$\begin{array}{c} A \\ \oplus \\ B \\ \hline \end{array}$$

$$\begin{array}{c} 00 \\ \oplus \\ 01 \\ \hline \end{array}$$

$$\begin{array}{c} 11 \\ \oplus \\ 10 \\ \hline \end{array}$$

$$= \text{Cin} (A \oplus B) + \text{Cin} (A \oplus \bar{B})$$

$$= A \oplus B' \oplus \text{Cin}$$

$$5) \quad \text{If } i/p = 1010 \quad \text{Ic } 7486 \text{ are } 1, 0, 1 \text{ then} \\ \text{O/p } = \text{sum} = 0, \text{ carry} = 1.$$

XVI Results  
 1. Sum & carry is high if all ip is high.  
 2. Sum & carry is low when all ip is low.

XVII Interpretation of Results (Give meaning of the above obtained results)  
 LED below when all ip are full adder of full subtractor is high & LED does not blow when all ip are off full adder of full subtractor.

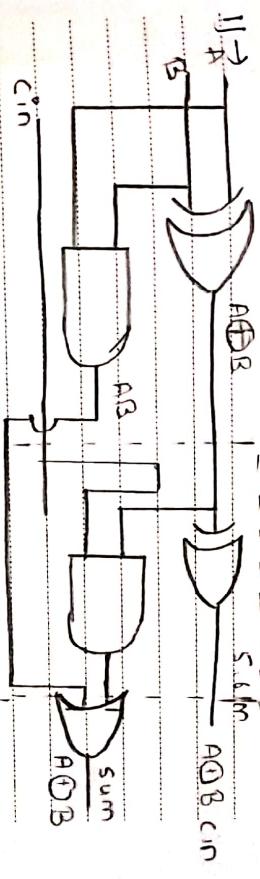
XVIII Conclusions and recommendations,  
 LED glow When all ip are full adder of full subtractor is high & LED doesn't glow when all ip full adder.

## XIX Practical Related Questions

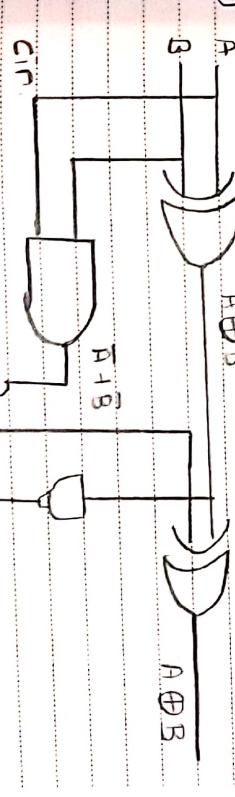
Note: Below given are few sample questions for reference. Teachers must design more such questions so as to ensure the achievement of identified CO.

1. Draw Full adder circuit using two Half adder circuits.
2. Draw full subtractor using two half subtractor circuits.
3. Write any four application of full adder circuit.
4. Design Full Adder using K-map.
5. If inputs to IC 7486 are 1, 0, 1 then what is the Output?
6. ....
7. ....

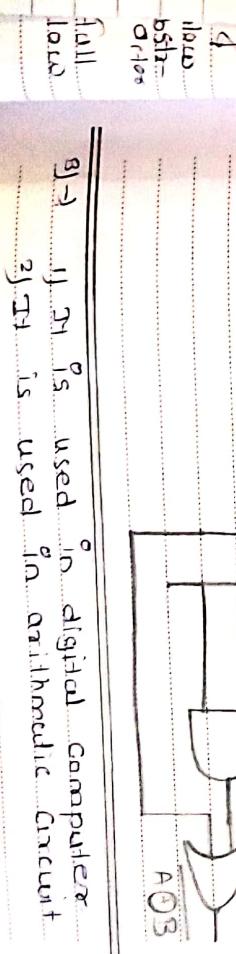
### [Space for Answers]



$$2) \quad A \quad B \quad \text{A} \oplus B \quad D = A \oplus B \quad \text{Cin}$$



$$D = A \oplus B \quad \text{Cin}$$



Q1) In Qs used in digital Computer  
Q2) T4 is used in arithmetic Circuit

full  
low

high  
b512  
a108

In pads of the ICs are 1, 0, 1, then and put will be 0.

### Practical No.7: Construct and test BCD to 7 segment decoder using IC 7447/7448.

#### XV References / Suggestions for further reading

1. <https://www.youtube.com/watch?v=RKjpw1Z2XkA>
2. <https://www.youtube.com/watch?v=mZ9VWAcTbE>
3. <https://www.slideshare.net/JaumunDarij3/design-half-full-adder-and-subtractor>

#### XVI Assessment Scheme

Performance indicators	Weightage
Process related:15 Marks	60%
1 Test the IC's using IC tester	10 %
2 Handling of the components IC	10 %
3 Identification of component IC	10 %
4 Mounting of IC on Breadboard	20 %
5 Working in team	10 %
Product related:10 Marks	40%
6 Result	10 %
7 Interpretation of result	05 %
8 Conclusions	05 %
9 Answers to Practical related questions	15 %
10 Submitting the journal in time	05%
Total (25 Marks)	100 %

#### Names of Student Team Members

1. Chaitanya Patil
2. Barvele Athuru
3. Sheaduse Aishya
4. ....

Marks Obtained	Dated signature of Teacher
Process Related(15)	Product Related(10)

**Practical Significance:** BCD is an abbreviation for binary-coded decimal. A Digital Decoder IC is a device which converts one digital format into another and one of the most commonly used devices for doing this is called the BCD to 7-Segment Display Decoder. It is used to display decimal numbers.

#### II Relevant Program Outcomes (POs)

1. Discipline knowledge: Apply Electronics and Computer knowledge to solve broad-based Electronics and Computer engineering related problems
2. Experiments and practice: Plan to perform experiments and practices to use the results to solve broad-based Electronics and Computer engineering problems.
3. Engineering tools: Apply relevant Electronics and Computer technologies and tools with an understanding of the limitations

#### III Competency and Practical Skills

This practical is expected to develop the following skills for the industry-identified competency through various teaching learning experiences competency. 'Build Combinational logic circuits consist of digital ICs.'

- i. Test seven segment display.
- ii. Assemble the circuit on breadboard.
- iii. Make connections as per circuit diagram.

#### IV Relevant Course Outcome(s):

- Build simple combinational circuits
- Practical Outcome
- Construct and test BCD to 7 segment decoder using IC 7447/7448

#### V Relevant Affective domain related Outcome(s)

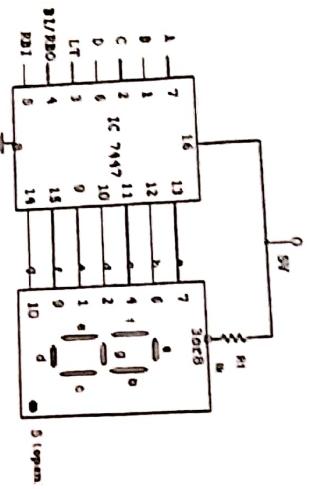
- Handle IC and equipment carefully.
- Follow safe practice

#### VI Minimum Theoretical Background

A decoder is a combinational circuit that connects the binary information from 'n' input lines to a maximum of  $2^n$  unique output lines. The IC7447 is a BCD to 7-segment pattern converter. The IC7447 takes the Binary Coded Decimal (BCD) as the input and outputs the relevant 7 segment code. A seven segment decoder is an IC decoder that can be used to drive a seven segment indicator. There are two types of 7-segment LED digital display 1. Common anode display (CAD) and 2. Common cathode display (CCD). Each decoder driver has 4 BCD inputs and 7 output pins (a to g segment).

**VIII**  
**Practical set-up / Circuit diagram**

a) Sample

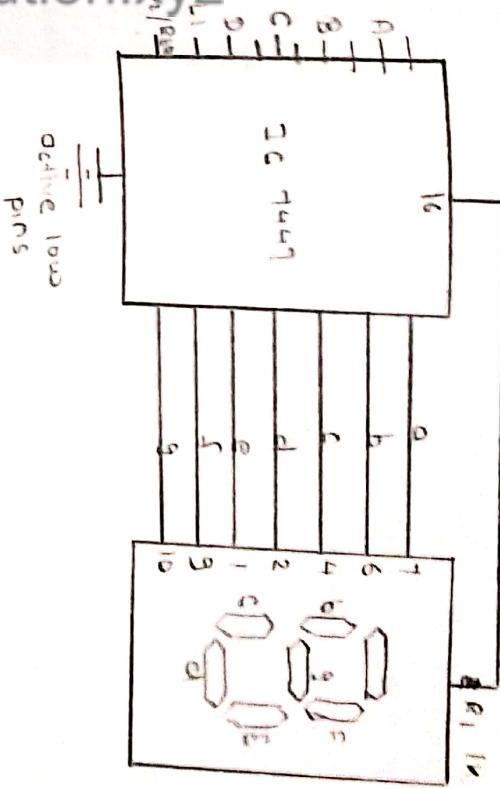


For normal functioning of IC 7447 Pin number 3, 4, 5 should be connected to logic  
 $1 \equiv V_{DD}$

Courtesy: <http://www.bogusoff.com/2013/10/hd-7-segment-decoder-driver/>

Figure 7.6: Circuit diagram

b) Actual circuit used in laboratory



c) Actual Experimental set up used in laboratory

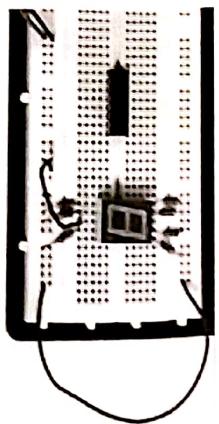


Figure 7.7 : Practical Setup

**IX Resources Required**

S. No.	Name of Resource	Suggested Broad Specification	Quantity	Remain
1	Digital Multimeter	Digital Multimeter 3 ½ digital display	1	
2	IC Tester	Digital IC Tester	1	
3	Breadboard	5.5 cm X 17 cm	1	
4	DC power supply	±5 V Fixed power supply	1	
5	IC 1	7447	1	
6	IC 2	7448	1	
7	Common anode 7-seg	IC FND 5671/T 542	1	
8	Common cathode 7-seg Display	IC LT 543	1	
9	Connecting wires	Single strand 0.6 mm Teflon coating	As required	
10	Resistors	330 Ω 0.25 W	7	

**X Precautions to be followed**

Do not switch ON the power supply unless you have checked the circuit connection as per the circuit diagram.

**XI Procedure**

- Test the IC's using IC tester
- Mount IC's on breadboard
- Connect different BCD inputs from (0000) to (1001) and note down the corresponding output on the display
- Observe the outputs on 7-segment display
- Fill up the observation table.
- The supply voltage to the IC's should not exceed +5V

**XII Resources Used**

S. No.	Instrument / Components	Specification	Quantity
1	Bread board	5.5 X 17 cm	1
2	LED	Red	1
3	Resistor	1 kΩ	1
4	IC	7447	1
5	multimeter	-	1

**XIII Actual Procedure followed (use blank sheet provided if space not sufficient)**

- made Connection as per fig. bread board
- Supply V<sub>cc</sub> to relevant pins per logic observed
- Precautions followed (use blank sheet provided if space not sufficient)
  - Don't ON power Supply unless
  - Checking the connection properly

**XIV Observations and Calculations:**  
**Observation Table for Half Adder**

BCD Inputs	7-SEGMENT CODED OUTPUTS							Display output				
	D	C	B	A	a	b	c	d	e	f	g	
0 0 0 0	0	0	0	0	0	0	0	0	0	0	0	000
0 0 0 1	0	0	0	1	0	0	0	0	0	0	0	001
0 0 1 0	0	0	1	0	0	0	0	0	0	0	0	010
0 0 1 1	0	0	1	1	0	0	0	0	0	0	0	011
0 1 0 0	0	1	0	0	1	0	0	0	0	0	0	100
0 1 0 1	0	1	0	1	1	0	0	0	0	0	0	101
0 1 1 0	0	1	1	0	0	1	0	0	0	0	0	110
0 1 1 1	0	1	1	1	1	1	0	0	0	0	0	111
1 0 0 0	1	0	0	0	0	0	0	0	0	0	0	000
1 0 0 1	1	0	0	1	0	0	0	0	0	0	0	001
1 0 1 0	1	0	1	0	0	0	0	0	0	0	0	010
1 0 1 1	1	0	1	1	0	0	0	0	0	0	0	011
1 1 0 0	1	1	0	0	1	1	1	0	0	0	0	100
1 1 0 1	1	1	0	1	1	1	1	0	0	0	0	101
1 1 1 0	1	1	1	0	0	1	1	1	0	0	0	110
1 1 1 1	1	1	1	1	1	1	1	1	0	0	0	111

BCD Input				7-Segment Coded Output						
D	C	B	A	a	b	c	d	e	f	g
0	0	0	0	0	0	0	0	0	0	0
0	0	0	1	1	0	0	0	1	1	0
0	0	1	0	0	0	0	1	0	1	0
0	0	1	1	0	0	0	1	0	1	0
0	1	0	0	1	0	0	0	0	0	0
0	1	0	1	0	0	0	0	0	0	0
0	1	1	0	0	0	0	0	1	0	1
0	1	1	1	0	0	0	0	0	1	0
1	0	0	0	0	0	0	0	1	0	1
1	0	0	1	0	0	0	0	0	1	0
1	0	1	0	0	0	0	0	0	0	1
1	0	1	1	0	0	0	0	0	0	1
1	1	0	0	0	0	0	0	0	0	1
1	1	0	1	0	0	0	0	0	0	1
1	1	1	0	0	0	0	0	0	0	1
1	1	1	1	0	0	0	0	0	0	1

- XVI Results  
 1 we get the o/p.  
 2 of 7 Segment display

XVII Interpretation of Results (Give meaning of the above obtained results)  
 All the o/p of 7 segment display will  
 give different BCD o/p from 0000  
 to 1000 how we get correct dis-  
 play.

XVIII Conclusions and recommendations (Actions/decisions to be taken based on the interpretation of results)

Then we give different ip from 0000 to  
 0001 at this time we get the cor-  
 rect o/p of 7 segment display

#### MX Practical Related Questions

Note: Below given are few sample questions for reference. Teachers must design more such questions so as to ensure the achievement of identified CO.

- Verify and write down the output for 7-segment decoder using common cathode display Practically in table.
- Write down functions of decoder.
- Write the functions of pin No. 3, 4, and 5 of IC 7447.
- List different types of decoder.

[Space for Answers]

pin no 3 [ $\overline{I\Gamma}$ ]

Lamp Test : I<sub>1</sub> is active low ip used to  
 test whether all segments of display are  
 working properly or not

BCD		I/P		7 Segment Coded O/P						
D	C	B	A	a	b	c	d	e	f	g
0	0	0	0	0	1	1	1	1	1	0
0	0	0	1	0	1	1	1	1	1	0
0	0	1	0	1	0	1	1	1	1	0
0	0	1	1	0	1	0	1	1	1	0
0	1	0	0	0	1	1	1	1	1	0
0	1	0	1	0	1	0	1	1	1	0
0	1	1	0	0	1	0	1	1	1	0
0	1	1	1	0	1	0	1	1	1	0
1	0	0	0	0	0	0	0	0	0	1
1	0	0	1	0	0	0	0	0	0	1
1	0	1	0	0	0	0	0	0	0	1
1	0	1	1	0	0	0	0	0	0	1
1	1	0	0	0	0	0	0	0	0	1
1	1	0	1	0	0	0	0	0	0	1
1	1	1	0	0	0	0	0	0	0	1
1	1	1	1	0	0	0	0	0	0	1

4) → Types of decoders  
 i) 2 to 4 line decoder  
 ii) 3 to 8 line decoder

Pin 4 - Blanking: Ripple blanking output. This pin is bidirectional with two function such as  $\overline{BI}$  or  $\overline{RBD}$ .

$\overline{BI}$ : Blanking output is active low for I<sub>D</sub>P when it is connected to GND. Segment display one blank i.e. switched off irrespective of BCD I<sub>D</sub>P of  $\overline{LT}$  to reduce power consumption of a digit or multi-digit or multiple display. This pin is used.

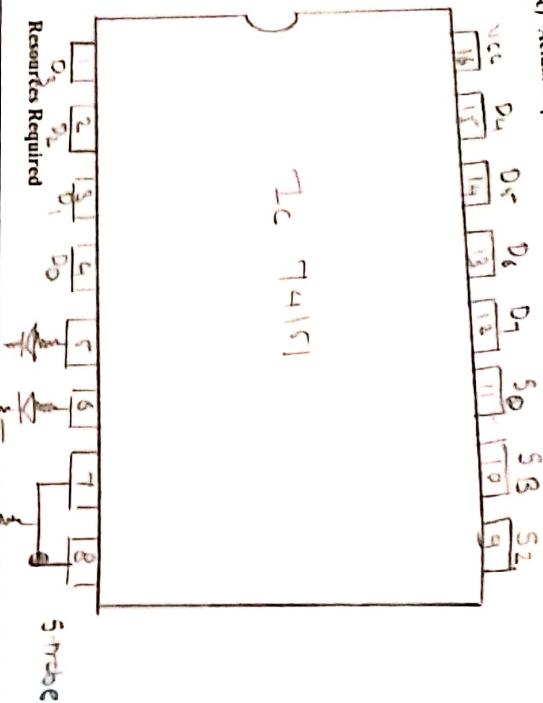
$\overline{RBD}$ : It is active low output. This output is normally connected to logic. RBO is used for cascading purpose of I<sub>D</sub>P is connected to RBD of next stage.

Pin 5 :  $\overline{RB1}$  - (Ripple blanking, I<sub>D</sub>)

Ripple blanking I<sub>D</sub>O is active in I<sub>D</sub>P pin which is driven by RBO of previous I<sub>D</sub>C to reduce power consumption in multidigit or multiplex display.  $\overline{RB1}$  is used.

2) Decoder is combinational circuit. It has input to a maximum 4:16 Decoder. Decoder directed to demultiplexer without any shades I<sub>D</sub>P perform operation which are exactly opposite to those from encodes.

- c) Actual Experimental set up used in laboratory



IX

#### Resources Required

S. No.	Instrument / Components	Specification	Quantity	Remarks
1	Digital Multimeter	3 1/2 digit display	1	
2	Digital IC Tester	Tests a wide range of Digital IC's such as 74 Series, 4045 Series of CMOS IC's	1	
3	DC power supply	+5 V Fixed power supply	1	
4	Breadboard	5.5cm X 17 cm	1	
5	IC	74151-74150	1	
6	LED	Red Yellow color 5 mm	1	
7	Resistor	330 Ω	2	
8	Connecting wires	Single strand 0.6 mm Teflon coating	As required	

X

**Precautions to be Followed**  
Do not switch ON the power supply unless you have checked the circuit connection as per the circuit diagram.

XI

#### Procedure

- Test the IC using Digital IC Tester.
- Mount the IC on the breadboard.
- Make the connections as per figure 8.3
- Give the supply voltage to IC +5V
- Observe the LED (on or off) for each combination of input as per truth table.
- Verify the truth table.

#### XII Resources used (with major specifications)

S. No.	Instrument / Components	Specification	Quantity
1.	IC	74151-74150	1
2.	LED	RED	2
3	Resistor	330 Ω	2
4			
5			

XIII

#### Actual procedure followed (Use blank sheet provided if space not sufficient)

Test the IC using Digital IC Tester  
Switch on the power supply unless you have checked the circuit connections as per the circuit diagram.

XIV

Precautions followed (Use blank sheet provided if space not sufficient)  
Switch on the power supply unless you have checked the circuit connections as per the circuit diagram.

XV

#### Observations and Calculations

Table 8.1: Observation table

Strobe	Data input	Inputs			Outputs	
		G	D <sub>n</sub>	S <sub>1</sub>	S <sub>0</sub>	Y
0	0	0	0	0	1	0
0	0	0	0	1	1	0
0	0	0	1	0	0	1
0	0	0	1	1	1	0
0	1	0	0	0	0	0
0	1	0	0	1	0	1
0	1	0	1	0	1	0
0	1	0	1	1	1	0
0	1	1	0	0	0	1
0	1	1	0	1	1	0
0	1	1	1	0	1	0
0	1	1	1	1	1	0
1	X	X	X	X	X	C

(Write the observation with respective to number of inputs)  
(Note: X - indicates the don't care conditions. It means status of select input may be any combination.)

XVI Results

74151 MAX 1 Output Y allows unappl'd

## XVII Interpretation of results (Give meaning of the above obtained results)

Interpretation of  
In 8.1 MAX. output of follows data input  
00

## XVIII Conclusions & Recommendation (Actions/decisions to be taken based on the evaluation of results)

### **Interpretation of results**

interpretation or else, we leave! To build / test function at !num also / true

XIX Practical Related Questions

**Practical Related Questions**  
*Note: Below given are few sample questions for reference. Teachers must design more such questions so as to ensure the achievement of identified CO.*

3. What is the output of IC 74151 if  $G=1$ ,  $S2S1S0=XXX$ ,  $Y=Y'=?$

[Space for answer]

1) U.P.n. S: It is used for output y

If pin 6: TA is also used output Y will print 1-1 is used to show he Genable input) which is always connected to ground and so

S1 taken ( $i=1$ ) at 7415.1c does not depend neglecting values of  $S_2, S_4, S_6$ , so should always be a then and they  $Ic$  just will respond.

$$y=0 \quad \text{if} \quad y=0$$

## **XX References / Suggestions for further reading**

1. <https://www.youtube.com/watch?v=x8N4Xh1s2M>
2. <https://razorjt.files.wordpress.com/2013/07/multiplexersdemultiplexers.pdf>
3. [Multiplexers\\_and\\_Dem](#)

Assessment Scheme

Performance Indicators		Weightage
<b>Process related:15 Marks</b>		<b>60%</b>
1	Identification of pin configuration of logic Gate IC	10 %
2	Proper Testing of IC	10 %
3	Mounting of IC on Breadboard	20 %
4	Circuit connection	10 %
5	Working in team	10 %
<b>Product related:10 Marks</b>		<b>40%</b>
6	Result	10 %
7	Interpretation of result	05 %
8	Conclusions	05 %
9	Answers to Practical related questions	15 %
10	Submitting the journal in time	05 %
<b>Total (25 Marks)</b>		<b>100 %</b>

### *Names of Student Team Members*

1. Chougue *Praevia*  
 2. Bourkale *Athraui*  
 3. Shendune *Aditya*  
 4. ....

Marks Obtained			Dated signature of Teacher
Process Related(15)	Product Related(10)	Total (25)	

## Observation & Calculation

(67)

### Practical No.9: Functionality of Demultiplexer (DEMUX)

#### I Practical Significance

A demultiplexer (or demux) is a device taking a single input signal and selecting one of many data-output-lines, which is connected to the single input. An electronic demultiplexer can be considered as a single-input, multiple-output switch. Demultiplexers are mainly used in Boolean function generators and decoder circuits.

#### II Relevant Program Outcomes (POs)

- Discipline knowledge: Apply Electronics and Computer knowledge to solve broad-based Electronics and Computer engineering related problems.
- Experiments and practice: Plan to perform experiments and practices to use the results to solve broad-based Electronics and Computer engineering problems.
- Engineering tools: Apply relevant Electronics and Computer technologies and tools with an understanding of the limitations.

#### III Competency and Practical Skills

This practical is expected to develop the following skills for the industry-identified competency: 'Build/ test digital logic circuits using digital ICs.'

- Identify pin configuration of IC.
- Test the functionality of the Demultiplexer.

#### IV Relevant Course Outcome(s)

- Build simple combinational circuits.

#### V Practical Outcome

- Build / test function of DEMUX 74154/74155 or any other equivalent.

#### VI Relevant Affective domain related Outcome(s)

- Handle IC and equipment carefully.
- Follow safe practices.

#### VII Minimum Theoretical Background

Demultiplexer has only one input and "n" number of outputs along with "m" number of select inputs. A demultiplexer performs the reverse operation of multiplexer i.e. it receives one input and distributes it over several outputs. At a time only one output line is selected by the select lines and the input is transmitted to the selected output line. Hence demultiplexer is equivalent to a single pole multiple way switch as shown in figure. The enable input will enable the demultiplexer. The relation between the n output lines and m select lines is as given below.

$$n = 2^m$$

The demultiplexer performs opposite process to a multiplexing process it performs "one to many" operation. It has only one input (D) and n number of outputs (Y0, Y1, Y2... Yn-1) as shown in the figure given below. Demultiplexer can also be used as a decoder e.g. Binary to Decimal Decoder. Data input given is 1, strobe/enable pin is used for enabling DEMUX

Select	Strobe	Data	2y0	2y1	2y2	2y3
B	A	1	X			
X	X	C <sub>2</sub>	C <sub>2</sub>	1	1	1
X	X	O	O	0	1	1
O	O	O	O	1	0	1
O	O	O	O	1	1	1
1	0	O	O	1	1	1
1	1	O	O	1	1	0
0	1	O	O	1	1	0
0	1	O	O	1	1	1
0	0	O	O	1	0	1
1	0	1	1	1	1	1
1	1	1	1	1	0	1
0	1	1	1	0	1	0
0	0	1	1	0	0	1

DEMUX - 2

S/P

SELECT	Strobe	Data	2y0	2y1	2y2	2y3
B	A	Cr <sub>2</sub>	C <sub>2</sub>			
X	X	1	X	1	1	1
X	X	O	O	0	1	1
O	O	O	O	1	1	1
O	O	O	O	1	0	1
O	O	O	O	1	1	1
1	0	O	O	1	1	1
1	1	O	O	1	1	0
0	1	O	O	1	1	0
0	0	O	O	1	0	1
0	1	1	1	1	1	1
1	0	1	1	1	0	1
1	1	1	1	0	1	0
0	1	1	1	0	0	1
0	0	1	1	0	0	0

## VIII Practical Circuit diagram

### a) Sample

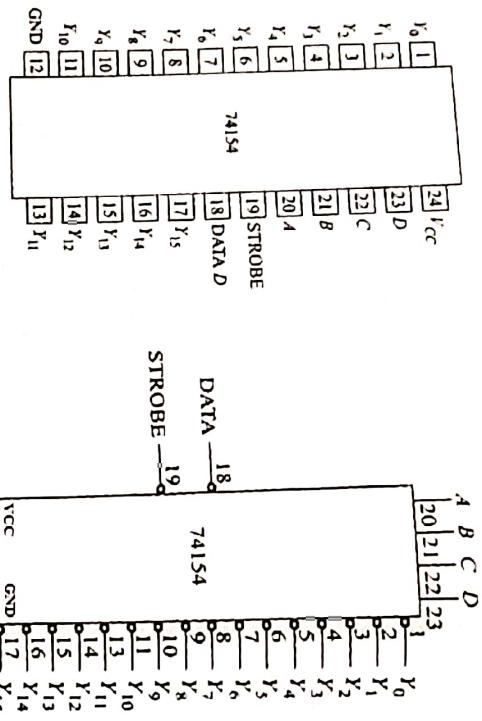
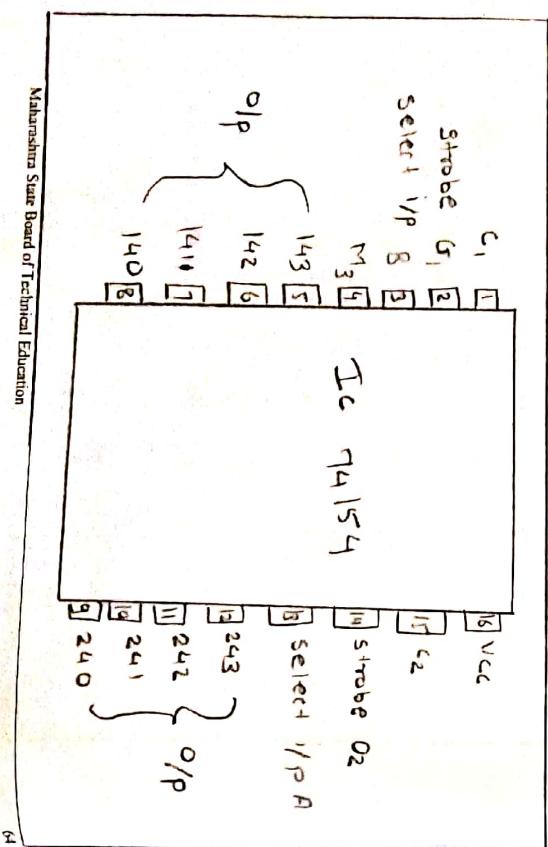


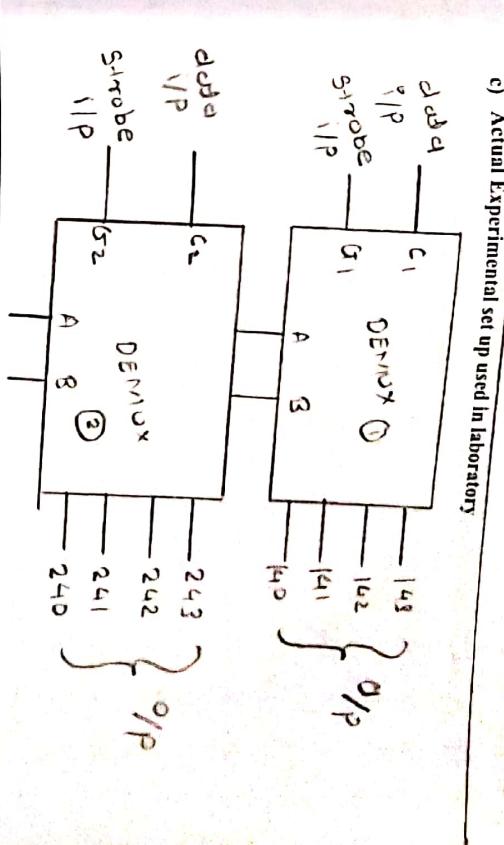
Figure 9.3 Sample circuit Diagram

### b) Actual Circuit used in laboratory



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### c) Actual Experimental set up used in laboratory



## IX Resources Required

S. No.	Instrument /Components	Specification	Quantity	Remark
1.	Digital Multimeter	Digital Multimeter: 3 1/2 digit display.	2	
2.	Breadboard	5.5cm X 17 cm	1	
3.	DC power supply	-5 V Fixed power supply	1	
4.	IC	74154/74155	Any one	
5.	LED	Red / Yellow color 5 mm	1	
6.	Resistor	330 Ω	4	
7.	Connecting wires	Single strand 0.6 mm Teflon coating	As required	

## X Precautions to be Followed

Do not switch ON the power supply unless you have checked the circuit connections as per the circuit diagram.

## XI Procedure

- Test the IC using Digital IC Tester.
- Mount the IC on the breadboard.
- Make the connections as shown in figure 9.3
- Give the supply voltage to IC +5V.
- Apply input to select lines according to the observation table.
- Observe the LED (on or off) for each combination of input as per truth table
- Verify the truth table.

**XII Resources Used (with major specifications)**

S. No.	Instrument Components	Specification	Quantity	Remark
1.	Board-based	5 cm x 7 cm	1	
2.	IC	74151	4	
3.	Resistor	330 Ω	1	
4.	LED	5 mm	1	

**XIII Actual Procedure Followed (Use blank sheet provided if space not sufficient)**

- (1) Mounted IC on bread board  
 (2) Made connections as per circuit diagram

**XIV Precautions Followed (Use blank sheet provided if space not sufficient)**

- Do not switch off power supply unless we have checked all connections as per circuit diagram

**XV Observations and Calculations**

Table 1: Observations

Inputs																Outputs							
D <sub>0</sub>	D <sub>1</sub>	S <sub>1</sub>	S <sub>0</sub>	S <sub>3</sub>	S <sub>2</sub>	S <sub>1</sub>	S <sub>0</sub>	S <sub>3</sub>	S <sub>2</sub>	S <sub>1</sub>	S <sub>0</sub>	V <sub>11</sub>	V <sub>10</sub>										
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	1	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	1	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	1	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

**XVIII Conclusions & Recommendation (Actions decisions to be taken based on the interpretation of results)**

The IC can be built to test functions for 4-to-16 DEMUX 74155.

**XIX Practical Related Questions**

Note Below given are few sample questions for reference. Teachers must design more such questions so as to ensure the achievement of identified CO.

1. List the function of pin 2, 3 and 5 of IC 74155.
2. List the name of manufacturers of Digital IC used in practical.
3. What is the role of select lines in a Demultiplexer?
4. What is the output of IC 74155 if D0=1, G=1, S1, S2, SI=XXX?
5. ....

**[Space for Answers]**

(1) If pin 2, 3 is used for output Y<sub>1</sub>, 2, 3 pin 3, 4 is used for output Y<sub>2</sub>, 3, 4 pin 5, 6 is used for output Y<sub>4</sub>.

(2) Role of select lines in demultiplexer as input.

(3) When G = 1 of IC 7415, IC does not respond. Negating value of S<sub>2</sub>, S<sub>1</sub>, S<sub>0</sub>.

A should always be 0 the and only when G = 1 IC will respond.

Thus if a = 1 & G = 1, S<sub>2</sub>, S<sub>1</sub>, S<sub>0</sub> = 0, 0, 0.

At any time.

(Note: 'X' indicates the don't care conditions. It means status of select input may be any combination.)

## Practical Circuit diagrams:-

a) Sample

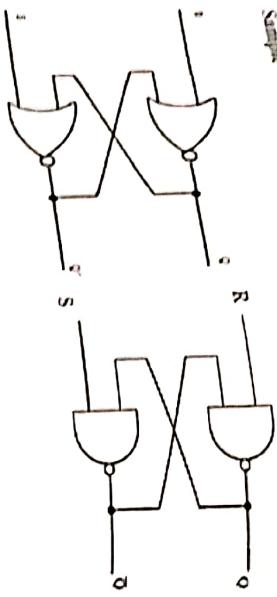


Figure 10.1 a) RS Latch Using NOR

b) RS Latch Using NAND

S	R	Q	$\bar{Q}$
0	0	Same as previous	Same as previous
0	1	0	1
1	0	1	0
1	1	Race	Race

Figure 10.1 b) Truth Table of logic diagram for figure 10.1a, b

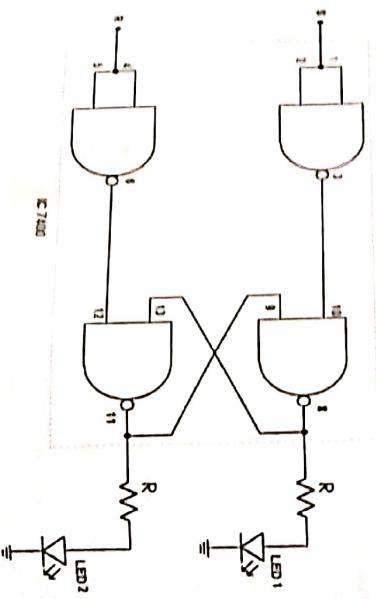
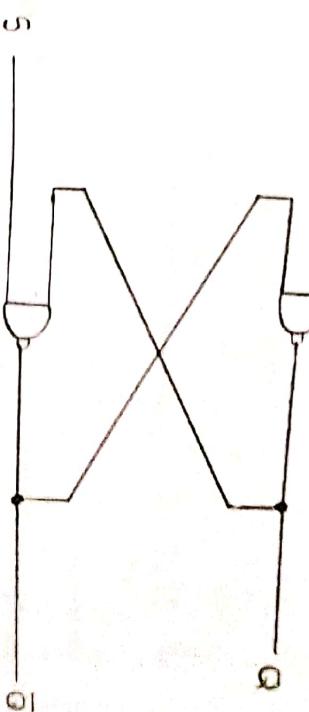


Figure 10.1 c) RS Latch Using NAND Gate

b) Actual Circuit used in Laboratory



c) Experimental setup used in Laboratory

## VIII Resources Required

No.	Instrument / Components	Specification	Quantity	Remarks
1	Digital Multimeter	Digital Multimeter : 3 1/2 digit display.	2	
2	Digital IC Tester	Tests a wide range of Digital ICs such as 74 Series, 4045 Series of CMOS ICs.	1	
3	DC power supply	+5 V Fixed power supply	1	
4	Breadboard	5.5cm X 17 cm	1	
5	IC	7400	1 Each	
6	LED	Red/Yellow color 5 mm	2	
7	Connecting wires	Single strand 0.6 mm Teflon coating	As required	
8	Resistors	330Ω	2	

- IX Precautions to be Followed**  
Do not switch ON the power supply unless you have checked the circuit connections as per the circuit diagram.

**X Procedure**

- Mount the IC-400 on the breadboard
- Make the connections as shown in figure 10.3
- Apply the supply voltage to IC +5V
- Apply inputs according to the observation table.
- Observe the LED (on or off) for each combination of input as per truth table.
- Verify the truth table.

**XI Resources used (with major specifications)**

S. No.	Instrument/ Components	Specification	Quantity
1	IC	7400	1
2	Resistor	330 Ω	1
3	LED	Red	1
4.			
5.			

**XII Actual procedure followed (Use blank sheet provided if space not sufficient)**

Mount the IC 7400 on the bread board  
make the connection as shown in fig 10.3

**XIII Precautions followed (Use blank sheet provided if space not sufficient)**

Do not switch on the power supply unless  
checked the circuit connection as per circ  
diagram.

**XIV Observations and Calculations**

Table 1: Truth Table SR flip-flop

S	R	Q	$\bar{Q}$	Comment
0	0	0	1	Initial
0	1	0	1	Set
1	0	1	0	Reset
1	1	1	0	SR = 1
1	1	0	1	SR = 1
1	1	1	1	SR = 1
1	1	0	1	SR = 1
1	1	1	0	SR = 1

**XV Results**

When the S = 0, R = 1 thus time the flip-flop is set and when S = 1 & R = 0 at that time it is reset and when S = 0, R = 0 then the flip-flop is in initial state.

**XVI Interpretation of results (Give meaning of the above obtained results)**

When S = 1 & R = 0 then S = 1 & R = 0 at that time the flip-flop is set and when S = 0, R = 1 then S = 0, R = 1 at that time the flip-flop is reset and when S = 0, R = 0 then S = 0, R = 0 at that time the flip-flop is in initial state.

**XVII Conclusions & Recommendation**

Interpretation of results (Actions decisions to be taken based on the interpretation of results)

When S = 1 & R = 0 we get set condition when S = 0, R = 1 we get reset condition.

**XVIII Practical Related Questions**

Note: Below given are few sample questions for reference. Teachers must design more such questions so as to ensure the achievement of identified CO

- List the name of manufacturer of Digital IC used in practical.
- Test the output when S-R=1
- Test the output when CLK = 1, verify truth table. (for clocked input circuit)
- Test the output when CLK = 0, verify truth table (for clocked input circuit)

(Space for answer)

When S = 1 we get Q = 1,  $\bar{Q} = 0$  which is race condition this should be avoided.

3] S = x, R = x (clock = high) this flip-flop doesn't respond not applied at the clock i/p. The

clock i/p will not change so Qn+1 = Qn and  $\bar{Q}_{n+1} = \bar{Q}_n$ .

4] S = x, R = x (clock = low level)  
as this flip-flop doesn't respond not applied at clock i/p in the

clock i/p  $\bar{Q}$  will not change so  $\bar{Q}_{n+1} = \bar{Q}_n$

2) Labben Clk=0 the output of S.R Flf is Comment

S	R	Q	Q	Reset
O	O	I	I	Set
I	O	I	O	Trace
I	I	Trace	Trace	Trace

## XX References / Suggestions for further reading

1. www.allaboutcircuits.com/datasheet-pdf
2. http://www.electronics-tutorials.ws
3. https://academo.org/demos/logic-gate-simulator

## XXI Suggested Assessment Scheme

Performance indicators	Weightage
Process related:15 Marks	60%
1 Identification of pin configuration of logic Gate IC	10 %
2 Proper Testing of IC	10 %
3 Mounting of IC on Breadboard	20 %
4 Circuit connection	10 %
5 Working in team	10 %
<b>Product related: 10 Marks</b>	<b>40%</b>
6 Result	10 %
7 Interpretation of result	05 %
8 Conclusions	05 %
9 Answers to Practical related questions	15 %
10 Submitting the journal in time	05%
<b>Total (25 Marks)</b>	<b>100 %</b>

## Names of Student Team Members

1. Chougle Pravin
2. Bankale Atman
3. Shendure Aditya
4. ....

Marks Obtained	Dated signature of Teacher
Process Related(15)	Product Related(10)

## VII Relevant Affective domain related Outcome(s)

- Handle IC and equipment carefully.
- Follow safe practices.

## VII Minimum Theoretical Background

Master Slave J K flip flop is a cascade of two S-R flip-flops, with feedback from the outputs of the second flip flop to the inputs of the first. The first part is called as master flip-flop while the next is called as slave flip-flop. Here the master flip-flop is triggered by the external clock pulse while the slave is activated at its inversion i.e. if the master is positive level triggered, then the slave is negative-level triggered and vice-versa. This means that the data enters into the flip-flop at positive/negative level of the clock pulse while it is obtained at the output pins during positive/negative level of the clock pulse. Hence a master-slave flip-flop completes its operation only after the appearance of one full clock pulse.

## VIII Practical Circuit diagram

a) Sample

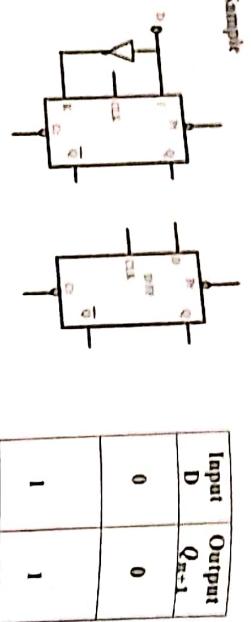


Figure 12.1a) D FF using 7476 b) Symbol c) Truth Table

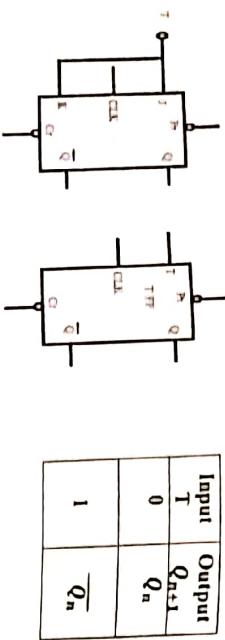


Figure 12.2a) T FF using 7476 b) Symbol c) Truth Table

IX Practical Circuit diagram

a) Sample

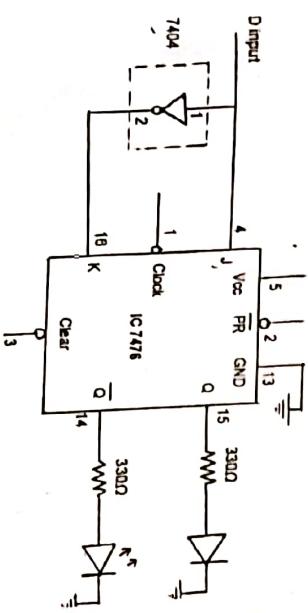


Figure 12.2b) T FF using 7476

[www.msbtresolution.xyz](http://www.msbtresolution.xyz)

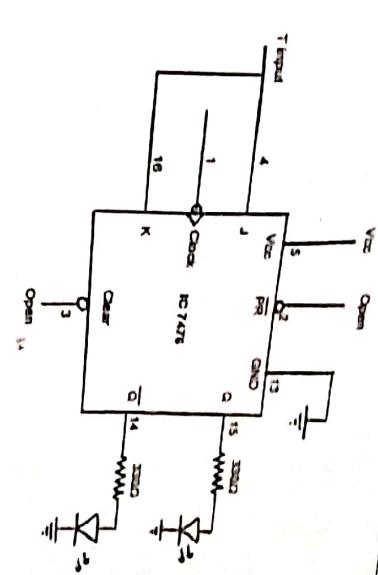
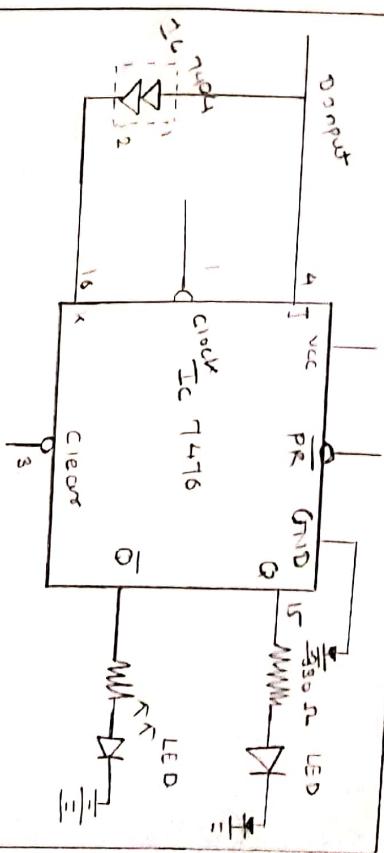
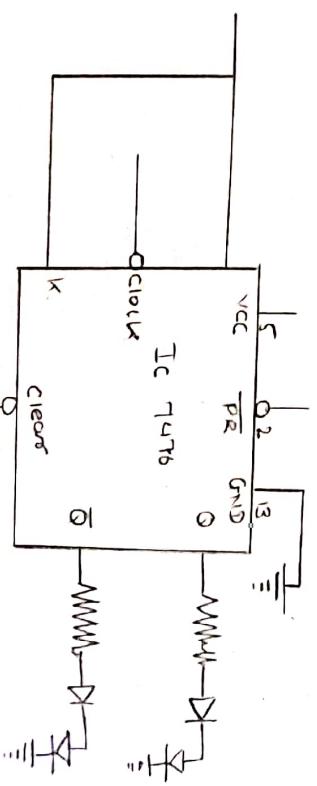


Figure 12.4 T FF using 7476

a) Actual Circuit used in laboratory



b) Actual Experimental set up used in laboratory



**X** Resources Required

S. No.	Instrument / Components	Specification	Quantity	Remarks
1	Digital Multimeter	Digital Multimeter 3 1/2 digit display	1	
2	Digital IC Tester	Tests a wide range of Digital IC's such as 74 Series, 4045 Series of CMOS IC's.	1	
3	DC power supply	+5 V Fixed power supply	1	
4	Breadboard	5.5cm X 17 cm	1	
5	IC 7476	7476	2	
6	LED	Red Yellow color 5 mm	2	
7	Connecting wires	Single strand 0.6 mm Teflon coating	As required	
8	Resistors	330Ω	2	

**XI** Precautions to be followed

Do not switch ON the power supply unless you have checked the circuit connections as per the circuit diagram.

**XII** Procedure

- Mount the IC7476 on the breadboard
- Make the connections as shown in figure 12.3 and 12.4
- Apply the supply voltage to IC +5V.
- Apply inputs according to the observation table.
- Observe the LED (on or off) for each combination of input as per truth table.
- Verify the truth table.

**XIII** Resources used (with major specifications)

S. No.	Instrument / Components	Specification	Quantity
1.	IC	7416	1
2.	Resistor	330 Ω	2
3.	LED	LED	2
4.			
5.			

**XIV**

- Actual procedure followed (Use blank sheet provided if space not sufficient)
- Mount the IC 7476 on the breadboard
  - Make the connection as shown in fig.
  - Supply the power supply as per the circuit diagram.

**XV** Precautions followed (Use blank sheet provided if space not sufficient)

- Do not switch ON the power supply unless you have checked the circuit connections as per the circuit diagram.

**XVI** Observations and Calculations

Table 3: Truth Table D, T flip-flop

Input D	Output Q <sub>n+1</sub>	Input T	Output Q <sub>n+1</sub>
0	Q	0	Q
1	1	1	Q̄

**XVII** Results

$$\text{DFF} = \overline{Q_0} \cdot P \cdot \overline{Q_1} \cdot T \cdot \overline{Q_2} \cdot P \cdot \overline{Q_3} \cdot P \cdot \overline{Q_4} \cdot T \cdot \overline{Q_5} \cdot P \cdot \overline{Q_6} \cdot P \cdot \overline{Q_7}$$

**XVIII** Interpretation of results (Give meaning of the above obtained results)

On DFF follow 1/P. If 0/P. change in logic 1/P. applied changes in logic 1/P. C. is applied.

**XIX**

Conclusions & Recommendation (Actions/decisions to be taken based on the interpretation of results)

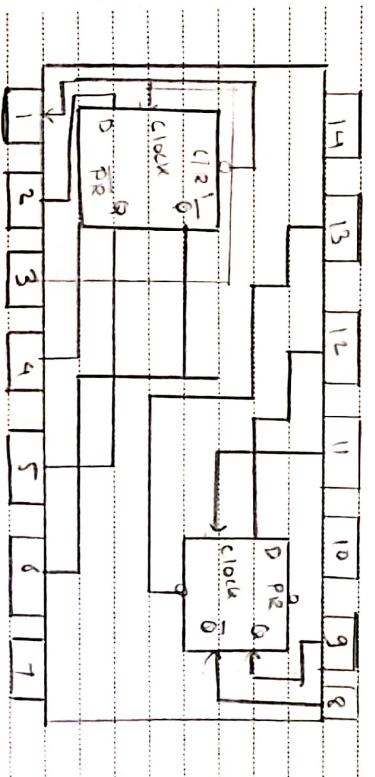
No change in trace condition are totally avoided so no more drawback in JK.

**XX** Practical Related Questions

Note: Below given are few sample questions for reference. Teachers must design more such questions so as to ensure the achievement of identified CO

- List the name of manufacturer of Digital IC used in practical.
- What is the function of IC 7474 draw its pin diagram?

[Space for answer]



Q2) - 1 Function of 74HC4017

24. Can 1 bit each add the 16-bit decimal and D and QP bit at the terminal? Or are some and H also the need to search the QP from I/P.

#### XV References / Suggestions for further reading

- www.allaboutcircuits.com/datasheet-pdf
- http://www.electronics-tutorials.ws

#### XVI Suggested Assessment Scheme

Performance indicators	Weightage
Process related:15 Marks	60%
1 Identification of pin configuration of logic Gate IC	10 %
2 Proper Testing of IC	10 %
3 Mounting of IC on Breadboard	20 %
4 Circuit connection	10 %
5 Working in team	10 %
<b>Product related:10 Marks</b>	<b>40%</b>
6 Result	10 %
7 Interpretation of result	05 %
8 Conclusions	05 %
9 Answers to Practical related questions	15 %
10 Submitting the journal in time	05%
<b>Total (25 Marks)</b>	<b>100 %</b>

#### XVII Names of Student Team Members

- Chougale, Punit
- Banerjee, Akash
- Sherude, Shelly
- .....

Marks Obtained	Dated signature of Teacher
Process Related(15) Product Related(10) (25)	

#### III Competency and Practical Skills

This practical is expected to develop the following skills for the industry-identified competency through various teaching learning experiences competency: Build test

- Identify pin configuration for IC.
- Make relevant connections as per circuit diagram.

#### IV Relevant Course Outcome(s)

- Build simple Sequential circuits.

#### V Practical Outcome:

- Implement 4 bit ripple counter using 7476

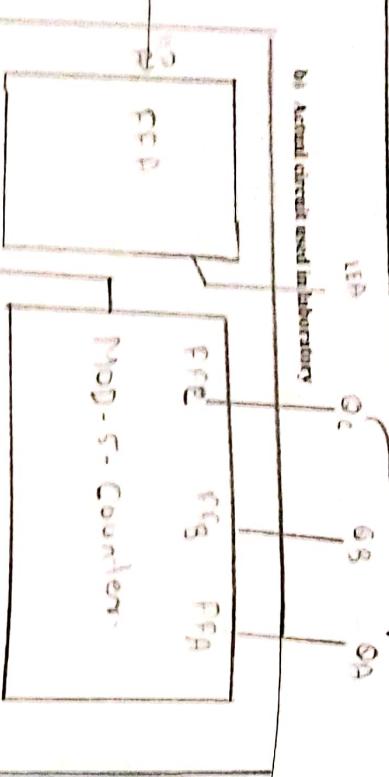
#### VI Relevant Affective domain related Outcome(s)

- Handle IC and equipment carefully.
- Follow safe practices.

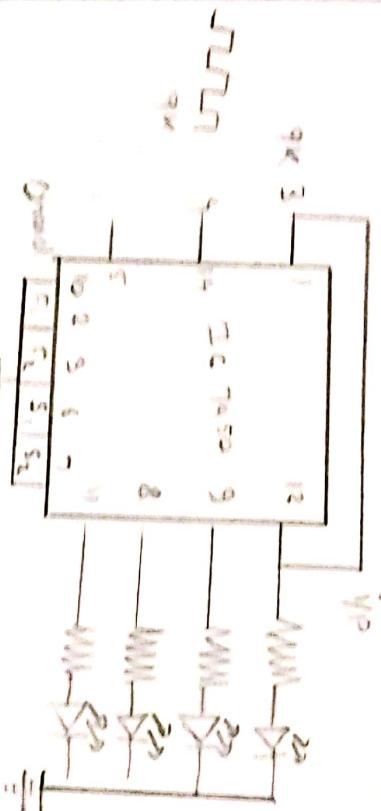
#### VII Minimum Theoretical Background:

A ripple counter is an asynchronous counter where only the first flip-flop is clocked by an external clock. All subsequent flip-flops are clocked by the output of the preceding flip-flop. Asynchronous counters are also called ripple-counters because of the way the clock pulse ripples away through the flip-flops. When decimal equivalent of the counter output increases as it receives the clock pulses, then that counter is known as Up Counter. When decimal equivalent of the counter output decreases as it receives the clock pulses, then that counter is known as Down Counter.

b) Actual circuit used in laboratory



c) Actual Experimental set up used in laboratory



- X** **Precautions to be followed**  
Do not switch ON the power supply unless you have checked the circuit connections as per the circuit diagram.

#### XI Procedure

- Mount IC 7490 on breadboard
- Make the connection for given circuit diagram (figure 14.2)
- Apply the clock input.
- Observe and record the outputs on LEDs (ON/OFF).

#### XII Resources Used

Sr. No.	Instrument / Components	Specification	Quantity
1	Decade Counter	5-Stage V <sub>H</sub> = 10V	1
2	LED	Red	1

#### XIII Actual Procedure Followed

- MOUNT IC 7490 ON BREADBOARD
- MAKE THE CONNECTIONS FOR THE CIRCUIT DIAGRAM

#### XIV Precautions Followed (Use blank sheet provided if space not sufficient)

- Switch ON THE POWER SUPPLY UNLESS YOU HAVE CHECKED THE CIRCUIT CONNECTIONS
- DO NOT TURN OFF THE CIRCUIT DURING OBSERVATION.

#### XV Observations and Calculations

Observation Table for Decade Counter

Input	Output					Decimal Equivalent
	No. of clock pulses	Q <sub>5</sub>	Q <sub>4</sub>	Q <sub>3</sub>	Q <sub>2</sub>	
0	0	0	0	0	0	0
1	0	0	0	0	0	1
2	0	0	0	0	1	2
3	0	0	0	1	0	3
4	0	0	0	1	1	4
5	0	0	1	0	0	5
6	0	0	1	0	1	6
7	0	0	1	1	0	7
8	0	1	0	0	0	8
9	0	1	0	0	1	9
10	0	1	0	1	0	10
11	0	1	0	1	1	11
12	0	1	1	0	0	12
13	1	0	0	0	0	13

#### XVI Results

- A decade counter no. of pulses is 13.
- Its output is 4.

**XVII Interpretation of Results** (Give meaning of the above obtained results)

To decode counter out pull electronic  
Examination. Same as no. of clock  
input

**XVIII Conclusions and recommendations** (Actions/decisions to be taken based on the interpretation of results)

Use IC 7490. A. o. use IC 7490. A. o. L. o. should  
decade counter (mod-10).

**XIX Practical Related Questions**

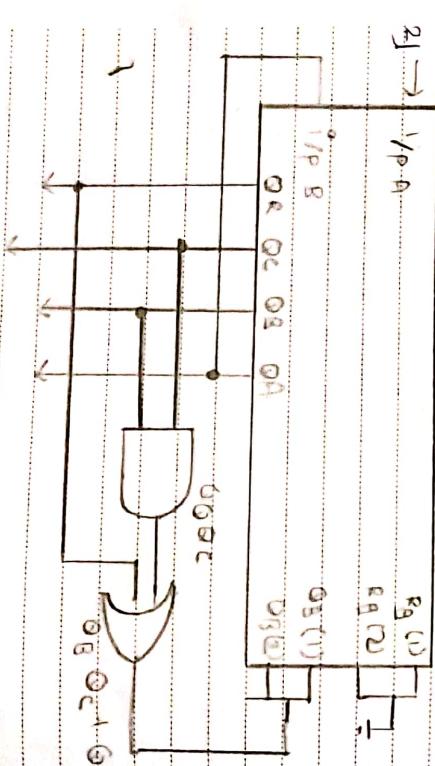
Note: Below given are few sample questions for reference. Teachers must design more such questions so as to ensure the achievement of identified CO.

1. Draw the internal circuit diagram of IC 7490.
2. Draw mod-6 counter using IC 7490
3. How many clock pulses are required for MOD 7 counter?
4. ....
5. ....

[Space for Answers]

**3] 2 clock pulses are required for**

MOA



[www.msbtesolution.xyz](http://www.msbtesolution.xyz)

**XX References / Suggestions for further reading**

1. <https://www.electronics-tutorials.ws/digital/digitalcounter.html>
2. [www.falstad.com/circuits/e-counter.html](http://www.falstad.com/circuits/e-counter.html)
3. <https://www.electronics-shub.org/Counters>

**XI Assessment Scheme**

Performance indicators		Weightage
1	Test the IC's using IC tester	60%
2	Handling of the components/IC	10%
3	Identification of component/IC	10%
4	Mounting of IC on Breadboard	10%
5	Working in team	10%
Product related:10 Marks		40%
6	Result	10%
7	Interpretation of result	05%
8	Conclusions	05%
9	Answers to Practical related questions	15%
10	Submitting the journal in time	05%
Total (25 Marks)		100%

*Names of Student Team Members*

1. Chaugule, Pratik
2. Pawar, Akshay
3. Ishendude, Aditya
4. ....

Marks Obtained	Dated signature of Teacher
Process Related(15) Product Related(10)	Total (25)

- If we proceed in this manner (Thevenin equivalent reduction), we will get

$$V_{out} = -\frac{R_f}{R_s} V_{ref} \left[ \frac{D_0}{16} + \frac{D_1}{8} + \frac{D_2}{4} + \frac{D_3}{2} \right]$$

- Note that you can build a DAC with any number of bits you want, by simply enlarging the resistor network by adding more R-2R resistor branches.

### VII Practical set-up / Circuit diagram

#### a) Sample

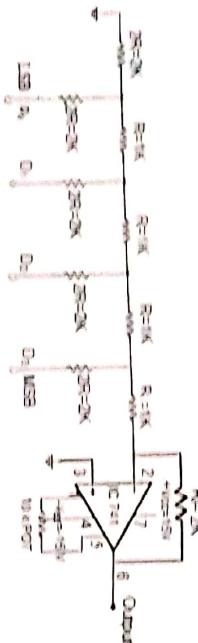
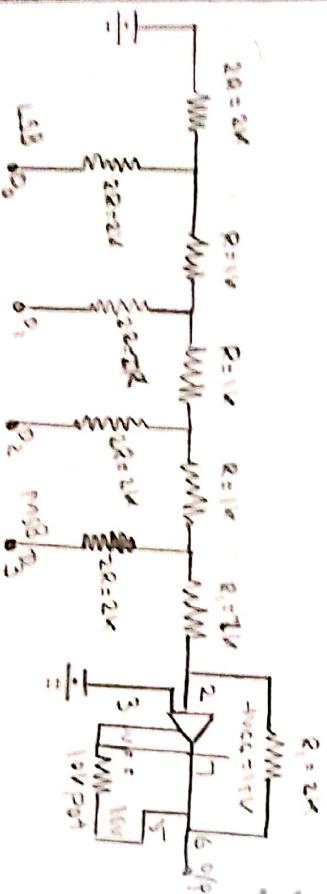


Figure 16.1 R-2R Ladder DA Network

#### b) Actual circuit Experimental set up used in laboratory



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### IX Resources Required

S. No.	Name of Resource	Suggested Board Specification	Quantity	Remark
1	Digital Multimeter	Digital Multimeter 3 ½ digital display	1	
2	IC Tester	Digital IC Tester	1	
3	Breadboards	5.5cm X 17 cm	1	
4	DC Power supply	-5 V fixed power supply, ±15 V	1	
5	Clock Pulse	Pulse/Pulse Generator	1	
6	IC 1	7404	1	
7	IC 2	741	1	
8	Connecting wires	Single strand 0.6 mm Teflon coating	As required	
9	Potentiometer	10kΩ	1	
10	Resistors	1kΩ and 2kΩ	6 (2 kΩ), 4 (1kΩ)	

### X Precautions to be followed

- Do not switch ON the power supply unless you have checked the circuit connections as per the circuit diagram.

**XI Procedure:**

- Test IC using IC tester.
- Mount IC on bread board.
- Build circuit as per circuit diagram.
- Write down observation table.
- With all inputs (D0 to D3) shorted to ground, adjust the 10KΩ POT until the output is 0V. This will nullify any offset voltage at the input of the OPAMP. (POT connected between pin 1 & pin 5 of OP-AMP)
- Measure the output voltage for all binary input states.(0000 to 1111).

**XII Resources Used**

S. No.	Instrument / Components	Specification	Quantity
1.	Bread board	5x 17cm	1
2.	IC	741	1 each.
3.	Resistors	330 Ω	6 (2x 3)
4.			
5.			

**XIII Actual Procedure Followed (Use blank sheet provided if space not sufficient)**

- Measured IC on the bread board.
- Bread board circuit Q.S. P.D. Circuit diagram

**XIV Precautions Followed**

- Supply voltage must be 5V unless otherwise checked.
- Circuit diagram

**XV Observations and Calculations:**

R-2R Ladder DAC			
D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>
0	0	0	0
0	0	0	1
0	0	1	0
0	1	0	0
0	1	0	1
0	1	1	0
0	1	1	1
1	0	0	0
1	0	0	1
1	0	1	0
1	0	1	1
1	1	0	0
1	1	0	1
1	1	1	0
1	1	1	1

Theoretical (V)      Practical (V)

$$V_o = \frac{R_1}{R_2} V_{ref} \left( \frac{D_0 + D_1 + D_2 + D_3}{16} \right)$$
**XVII Interpretation of Results (Give meaning of the above obtained results)**

Practically and theoretically obtained voltage due to successively added voltage

**XVIII Conclusions and recommendations (Actions/decisions to be taken based on the interpretation of results).**

Practically and Theoretically obtained Voltage due to successively added voltage

**XIX Practical Related Questions**

Note: Below given are few sample questions for reference. Teachers must design more such questions so as to ensure the achievement of identified CO

- Define resolution of DAC.
- State the purpose of op-amp in this circuit?
- Write the steps to nullify any offset voltage at the input of the OPAMP.
- Write down effect of number of input bits on output of DAC?

[Space for Answers]

- ① Resolution of DAC is degree to which the change can be theoretically detected in terms of bits. This relates to bits required to be actual voltage measurement.
- ② Op-amp is used in R-2R circuit because Op-amp is a DC complete a high gain electric voltage amplifier with different i/p & usually a single ended o/p.
- ④ There is no any effect on no o/p if p bits on o/p of DAC

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