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a) I/O Module Block Diagram & 2+6 Input Techniques
                                                             I/O Module Structure
                                                              I/O Module
                                                                                        External Device
                                                          I/O Module Internal Components
                                                                                                Interface to Device
                                Interface to CPU
                                 Data Registers
                                                                                              Status/Control Registers
                                                             I/O Logic & Control Unit
  I/O Module Functions:
  Control & Timing: Coordinates data transfer between CPU and peripherals
  CPU Communication: Handles data, control, and status information exchange
  Device Communication: Manages device-specific protocols and timing
  Data Buffering: Temporarily stores data during transfer operations
  Error Detection: Monitors and reports transmission errors
Input Techniques for Block Data Transfer (2+6)
 1. Programmed I/O (Polling)
                                                             CPU initiates I/O command
                                                                Check device status
                                                          Device ready? Poll continuously
                                                         Transfer data block byte by byte
  Advantage: Simple implementation, full CPU control
 Disadvantage: CPU wastage due to continuous polling
 2. Interrupt-Driven I/O
                                                              CPU issues I/O command
                                                             CPU continues other tasks
                                                              Device sends interrupt
                                                      CPU services interrupt & transfers data
  Advantage: Better CPU utilization
 Disadvantage: Overhead for each byte transfer
 Additional Techniques (6 more):
 3. Direct Memory Access (DMA): Direct data transfer between memory and I/O device
 4. Channel I/O: Dedicated processors handle I/O operations
 5. Memory-Mapped I/O: I/O devices accessed through memory addresses
 6. Isolated I/O: Separate address space for I/O operations
 7. Buffered I/O: Use of intermediate buffers for data transfer
 8. Scatter-Gather I/O: Transfer data to/from multiple memory locations
b) DMA Controller Interfacing with CPU
                                                         DMA Controller Block Diagram
                                                                  DMA Controller
                        CPU
                                                                                                                   I/O Device
                                                                 • Address Register
                    Control Bus
                                                                • Word Count Register
                                                                                                                  Disk, Network,
                    Address Bus
                                                                 • Control Register
                     Data Bus
                                                                 • Status Register
                                                                   Main Memory
  DMA Operation Steps:
  1. Initialization: CPU programs DMA controller with memory address, transfer count, and direction
  2. Bus Request: DMA controller requests bus control from CPU
  3. Bus Grant: CPU grants bus control and enters wait state
  4. Data Transfer: DMA directly transfers data between memory and I/O device
  5. Bus Release: DMA releases bus control back to CPU after transfer completion
                                                                DMA Transfer Modes
                                                                                                                Transparent Mode
                                                                   Cycle Stealing
                     Burst Mode
                 DMA takes bus until
                                                               DMA steals bus cycles
                                                                                                             DMA transfers only when
                                                              when CPU doesn't need it
               entire block transferred
                                                                                                              CPU is not using bus
c) Priority Interrupt Controller Interfacing with CPU
                                               Priority Interrupt Controller (PIC) Structure
                                                          Priority Interrupt Controller
                                                                Priority Resolver
                   Interrupt Request Register (IRR)
                                                                                                   In-Service Register (ISR)
                    Interrupt Mask Register (IMR)
                                                                   Control Logic
                                                                                                       Vector Generator
                                                             Device 1
                                         Device 0
                                                                             Device 2
                                                                                                  Device 7
                                                                                              (Lowest Priority)
                                    (Highest Priority)
  Priority Resolution Methods:
    Fixed Priority: Each interrupt source has a predetermined priority level
    Rotating Priority: Priority levels rotate after each interrupt service
    Masked Interrupts: Software can selectively enable/disable interrupt sources
                                                            Interrupt Processing Flow
                                                        Multiple devices request interrupt
                                                          PIC determines highest priority
                                                           PIC sends INTR signal to CPU
                                                      CPU sends INTA (Interrupt Acknowledge)
                                                          PIC provides interrupt vector
                                                      CPU jumps to interrupt service routine
d) DMA and Interrupt Breakpoints During Instruction Cycle
                                             Instruction Cycle with Interrupt/DMA Breakpoints
         FETCH
                                                          DECODE
                                                                                   CHECK
                                                                                                          EXECUTE
                                                                                                                                   CHECK
                                                       Instruction
                                                                                                        Instruction
                                Interrupt
                                                                                    DMA
       Instruction
                                                                                                                                  Interrupt
       from Memory
                                 Request
                                                                                                                                  Request
                                                        Operation
                                                                                  Request
                                                                                                         Operation
  Breakpoint Locations:
  1. After Fetch: Check for interrupts before decoding next instruction
  2. Before Execute: Check for DMA requests that need immediate bus access
  3. After Execute: Check for interrupts generated by the completed instruction
                                                        Priority During Instruction Cycle
                     Highest Priority
                                                                  Medium Priority
                                                                                                             Lower Priority
                                                                   DMA Requests
                                                                                                           Maskable Interrupts
                    Hardware Interrupts
                    (NMI, Machine Check)
                                                                 (Bus Arbitration)
                                                                                                              (I/O Devices)
 Interrupt vs DMA Handling:
 Interrupt Breakpoint: CPU saves context, jumps to ISR, processes interrupt, then returns
 DMA Breakpoint: CPU temporarily halts, grants bus to DMA controller, resumes after transfer
 Simultaneous Requests: Hardware interrupts typically have higher priority than DMA requests
                                                              Timing Diagram Example
                                                     Clock: |---|---|---|
                                                   CPU: FETCH |DECODE|EXEC |FETCH |INT |EXEC |
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I/O Module and Interrupt System Block Diagrams

Summary

These diagrams illustrate the key concepts of I/O interfacing, DMA operations, interrupt handling, and their integration within the CPU instruction cycle. Each component plays a crucial role in efficient computer system operation.

DMA Req: ____|__^^^|__|__|
INT Req: ____|___|____|
Bus Grant: ___|___|_^^^^|___|__|

^^^ = Active Signal | $_$ = Inactive | INT = Interrupt Service