



LMV3xx Low-Voltage Rail-to-Rail Output Operational Amplifiers

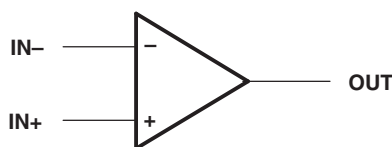
1 Features

- 2.7-V and 5-V Performance
- –40°C to 125°C Operation
- Low-Power Shutdown Mode (LMV324S)
- No Crossover Distortion
- Low Supply Current
 - LMV321: 130 μ A Typ
 - LMV358: 210 μ A Typ
 - LMV324: 410 μ A Typ
 - LMV324S: 410 μ A Typ
- Rail-to-Rail Output Swing
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model
 - 1000-V Charged-Device Model

2 Applications

- Desktop PCs
- HVAC: Heating, Ventilating, and Air Conditioning
- Motor Control: AC Induction
- Netbooks
- Portable Media Players
- Power: Telecom DC/DC Module: Digital
- Pro Audio Mixers
- Refrigerators
- Washing Machines: High-End and Low-End

4 Simplified Schematic



3 Description

The LMV321, LMV358, LMV324, and LMV324S devices are single, dual, and quad low-voltage (2.7 V to 5.5 V) operational amplifiers with rail-to-rail output swing. These devices are the most cost-effective solutions for applications where low-voltage operation, space saving, and low cost are needed. These amplifiers are designed specifically for low-voltage (2.7 V to 5 V) operation, with performance specifications meeting or exceeding the LM358 and LM324 devices that operate from 5 V to 30 V. With package sizes down to one-half the size of the DBV (SOT-23) package, these devices can be used for a variety of applications.

Device Information(1)

| PART NUMBER | PACKAGE (PIN) | BODY SIZE |
|-------------|---------------|-------------------|
| LMV324 | SOIC (14) | 8.65 mm × 3.91 mm |
| LMV321 | SOT-23 (5) | 2.90 mm × 1.60 mm |
| | SC-70 (5) | 2.00 mm × 1.25 mm |
| LMV358 | VSSOP (8) | 2.30 mm × 2.00 mm |
| | VSSOP (8) | 3.00 mm × 3.00 mm |
| | TSSOP (8) | 3.00 mm × 4.40 mm |

(1) For all available packages, see the orderable addendum at the end of the datasheet.



Table of Contents

| | | | |
|---|-----------|--|-----------|
| 1 Features | 1 | 8.1 Overview | 16 |
| 2 Applications | 1 | 8.2 Functional Block Diagram | 16 |
| 3 Description | 1 | 8.3 Feature Description | 17 |
| 4 Simplified Schematic | 1 | 8.4 Device Functional Modes | 17 |
| 5 Revision History | 2 | 9 Application and Implementation | 18 |
| 6 Pin Configuration and Functions | 3 | 9.1 Typical Application | 18 |
| 7 Specifications | 4 | 10 Power Supply Recommendations | 21 |
| 7.1 Absolute Maximum Ratings | 4 | 11 Layout | 22 |
| 7.2 Handling Ratings | 4 | 11.1 Layout Guidelines | 22 |
| 7.3 Recommended Operating Conditions | 4 | 11.2 Layout Example | 22 |
| 7.4 Thermal Information | 4 | 12 Device and Documentation Support | 23 |
| 7.5 Electrical Characteristics: $V_{CC+} = 2.7\text{ V}$ | 5 | 12.1 Related Links | 23 |
| 7.6 Electrical Characteristics: $V_{CC+} = 5\text{ V}$ | 6 | 12.2 Trademarks | 23 |
| 7.7 Shutdown Characteristics, LMV324S: $V_{CC+} = 2.7\text{ V}$ | 7 | 12.3 Electrostatic Discharge Caution | 23 |
| 7.8 Shutdown Characteristics, LMV324S: $V_{CC+} = 5\text{ V}$... | 7 | 12.4 Glossary | 23 |
| 7.9 Typical Characteristics | 8 | 13 Mechanical, Packaging, and Orderable Information | 23 |
| 8 Detailed Description | 16 | | |

5 Revision History

Changes from Revision V (December 2013) to Revision W Page

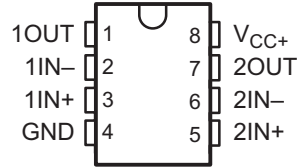
- Added Applications, Handling Rating table, Thermal Information Table, Device Functional Modes, Application and Implementation section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information section. **1**

Changes from Revision U (July 2012) to Revision V Page

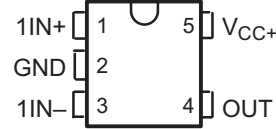
- Updated document to new TI data sheet format. **1**
- Removed Ordering Information table. **3**
- Added ESD warning. **23**

6 Pin Configuration and Functions

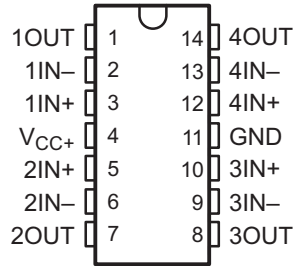
**LMV358 . . . D (SOIC), DDU (VSSOP),
DGK (VSSOP), OR PW (TSSOP) PACKAGE
(TOP VIEW)**



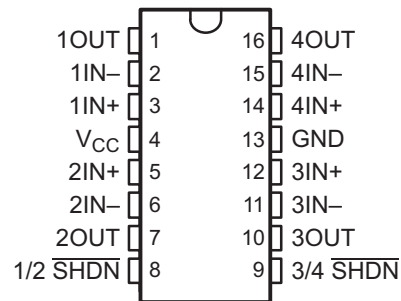
**LMV321 . . . DBV (SOT-23)
OR DCK (SC-70) PACKAGE
(TOP VIEW)**



**LMV324 . . . D (SOIC) OR PW (TSSOP) PACKAGE
(TOP VIEW)**



**LMV324S . . . D (SOIC) OR PW (TSSOP) PACKAGE
(TOP VIEW)**



Pin Functions

| NAME | PIN | | | | TYPE | DESCRIPTION |
|----------|------------------------------|----------------------|-------------------|--------------------|------|--|
| | LMV358 D, DDU, DGK, PW | LMV321 DBV or DCK | LMV324 D or PW | LMV324S D or PW | | |
| 3/4 SHDN | — | — | — | 9 | I | Shutdown (logic low)/enable (logic high) |
| 1/2 SHDN | — | — | — | 8 | I | Shutdown (logic low)/enable (logic high) |
| 1IN+ | 3 | 1 | 3 | 3 | I | Noninverting input |
| 1IN- | 2 | 3 | 2 | 2 | I | Inverting input |
| 2IN+ | 5 | — | 5 | 5 | I | Noninverting input |
| 2IN- | 6 | — | 6 | 6 | I | Inverting input |
| 2OUT | 7 | — | 7 | 7 | O | Output |
| 3IN+ | — | — | 10 | 12 | I | Noninverting input |
| 3IN- | — | — | 9 | 11 | I | Inverting input |
| 3OUT | — | — | 8 | 10 | O | Output |
| 4IN+ | — | — | 12 | 14 | I | Noninverting input |
| 4IN- | — | — | 13 | 15 | I | Inverting input |
| 4OUT | — | — | 14 | 16 | O | Output |
| GND | 4 | 2 | 11 | 13 | - | Negative supply |
| OUT | 1 | 4 | 1 | 1 | O | OUT |
| VCC+ | 8 | 5 | 4 | 4 | - | Positive supply |

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) ⁽¹⁾

| | | MIN | MAX | UNIT |
|-----------------|---|---|------|------|
| V _{CC} | Supply voltage ⁽²⁾ | | 5.5 | V |
| V _{ID} | Differential input voltage ⁽³⁾ | | ±5.5 | V |
| V _I | Input voltage range (either input) | –0.2 | 5.7 | V |
| | Duration of output short circuit (one amplifier) to ground ⁽⁴⁾ | At or below T _A = 25°C, V _{CC} ≤ 5.5 V | | |
| T _J | Operating virtual junction temperature | | 150 | °C |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values (except differential voltages and V_{CC} specified for the measurement of I_{OS}) are with respect to the network GND.
- (3) Differential voltages are at IN+ with respect to IN–.
- (4) Short circuits from outputs to V_{CC} can cause excessive heating and eventual destruction.

7.2 Handling Ratings

| | | MIN | MAX | UNIT |
|--------------------|---------------------------|--|-----|------|
| T _{stg} | Storage temperature range | −65 | 150 | °C |
| V _(ESD) | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾ | | V |
| | | Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾ | | |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions⁽¹⁾

| | | | MIN | MAX | UNIT |
|-----------------|--|--|-----|-----|------|
| V _{CC} | Supply voltage (single-supply operation) | | 2.7 | 5.5 | V |
| V _{IH} | Amplifier turn-on voltage level (LMV324S) ⁽²⁾ | V _{CC} = 2.7 V | 1.7 | | V |
| | | V _{CC} = 5 V | 3.5 | | |
| V _{IL} | Amplifier turn-off voltage level (LMV324S) | V _{CC} = 2.7 V | 0.7 | | V |
| | | V _{CC} = 5 V | 1.5 | | |
| T _A | Operating free-air temperature | I temperature (LMV321, LMV358, LMV324, LMV321IDCK) | −40 | 125 | °C |
| | | I temperature (LMV324S) | −40 | 85 | |
| | | Q temperature | −40 | 125 | |

- (1) All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number [SCBA004](#).
- (2) V_{IH} should not be allowed to exceed V_{CC}.

7.4 Thermal Information

| THERMAL METRIC ⁽¹⁾ | | LMV3xx | | | | | | | | | | UNIT |
|-------------------------------|--|--------|--------|--------|-------|-------|-------|-------|-------|--------|--------|------|
| | | D | | | DBV | DCK | DDU | DGK | PW | | | |
| | | 8 PIN | 14 PIN | 16 PIN | 5 PIN | 5 PIN | 8 PIN | 8 PIN | 8 PIN | 14 PIN | 16 PIN | |
| R _{θJA} | Junction-to-ambient thermal resistance | 97 | 86 | 73 | 206 | 252 | 210 | 172 | 149 | 113 | 108 | °C/W |

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

7.5 Electrical Characteristics: $V_{CC+} = 2.7\text{ V}$

 $V_{CC+} = 2.7\text{ V}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP ⁽¹⁾ | MAX | UNIT |
|----------------|---|--|------------|----------------|--------------------|-----|------------------------------|
| V_{IO} | Input offset voltage | | | | 1.7 | 7 | mV |
| α_{VIO} | Average temperature coefficient of input offset voltage | | | | 5 | | $\mu\text{V}/^\circ\text{C}$ |
| I_{IB} | Input bias current | | | | 11 | 250 | nA |
| I_{IO} | Input offset current | | | | 5 | 50 | nA |
| CMRR | Common-mode rejection ratio | $V_{CM} = 0\text{ to }1.7\text{ V}$ | | 50 | 63 | | dB |
| k_{SVR} | Supply-voltage rejection ratio | $V_{CC} = 2.7\text{ V to }5\text{ V}$, $V_O = 1\text{ V}$ | | 50 | 60 | | dB |
| V_{ICR} | Common-mode input voltage range | CMRR $\geq 50\text{ dB}$ | | 0 | –0.2 | | V |
| | | | | | 1.9 | 1.7 | |
| V_O | Output swing | $R_L = 10\text{ k}\Omega\text{ to }1.35\text{ V}$ | High level | $V_{CC} - 100$ | $V_{CC} - 10$ | | mV |
| | | | Low level | | 60 | 180 | |
| I_{CC} | Supply current | LMV321I | | | 80 | 170 | μA |
| | | LMV358I (both amplifiers) | | | 140 | 340 | |
| | | LMV324I and LMV324SI (all four amplifiers) | | | 260 | 680 | |
| B_1 | Unity-gain bandwidth | $C_L = 200\text{ pF}$ | | | 1 | | MHz |
| Φ_m | Phase margin | | | | 60 | | deg |
| G_m | Gain margin | | | | 10 | | dB |
| V_n | Equivalent input noise voltage | $f = 1\text{ kHz}$ | | | 46 | | $\text{nV}/\sqrt{\text{Hz}}$ |
| I_n | Equivalent input noise current | $f = 1\text{ kHz}$ | | | 0.17 | | $\text{pA}/\sqrt{\text{Hz}}$ |

- (1) Typical values represent the likely parametric nominal values determined at the time of characterization. Typical values depend on the application and configuration and may vary over time. Typical values are not ensured on production material.

LMV358, LMV321, LMV324, LMV324S

SLOS263W –AUGUST 1999–REVISED OCTOBER 2014

www.ti.com

7.6 Electrical Characteristics: $V_{CC+} = 5\text{ V}$
 $V_{CC+} = 5\text{ V}$, at specified free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | T _A ⁽¹⁾ | MIN | TYP ⁽²⁾ | MAX | UNIT |
|------------------|---|---|------------|-------------------------------|-----------------------|-----------------------|----------------------|--------|
| V _{IO} | Input offset voltage | | | 25°C | | 1.7 | 7 | mV |
| | | | | Full range | | | 9 | |
| α _{VIO} | Average temperature coefficient of input offset voltage | | | 25°C | | 5 | | μV/°C |
| I _{IB} | Input bias current | | | 25°C | | 15 | 250 | nA |
| | | | | Full range | | | 500 | |
| I _{IO} | Input offset current | | | 25°C | | 5 | 50 | nA |
| | | | | Full range | | | 150 | |
| CMRR | Common-mode rejection ratio | V _{CM} = 0 to 4 V | | 25°C | 50 | 65 | | dB |
| k _{SVR} | Supply-voltage rejection ratio | V _{CC} = 2.7 V to 5 V, V _O = 1 V, V _{CM} = 1 V | | 25°C | 50 | 60 | | dB |
| V _{ICR} | Common-mode input voltage range | CMRR ≥ 50 dB | | 25°C | 0 | −0.2 | | V |
| | | | | | | 4.2 | 4 | |
| V _O | Output swing | R _L = 2 kΩ to 2.5 V | High level | 25°C | V _{CC} − 300 | V _{CC} − 40 | | mV |
| | | | Low level | Full range | V _{CC} − 400 | | | |
| | | | | 25°C | | 120 | 300 | |
| | | | | Full range | | | 400 | |
| | | R _L = 10 kΩ to 2.5 V | | High level | 25°C | V _{CC} − 100 | V _{CC} − 10 | |
| | | | Low level | Full range | V _{CC} − 200 | | | |
| | | | | 25°C | | 65 | 180 | |
| | | | | Full range | | | 280 | |
| A _{VD} | Large-signal differential voltage gain | R _L = 2 kΩ | | 25°C | 15 | 100 | | V/mV |
| | | | | Full range | 10 | | | |
| I _{OS} | Output short-circuit current | Sourcing, V _O = 0 V | | 25°C | 5 | 60 | | mA |
| | | Sinking, V _O = 5 V | | | 10 | 160 | | |
| I _{CC} | Supply current | LMV321I | | 25°C | | 130 | 250 | μA |
| | | | | Full range | | | 350 | |
| | | LMV358I (both amplifiers) | | 25°C | | 210 | 440 | |
| | | | | Full range | | | 615 | |
| | | LMV324I and LMV324SI (all four amplifiers) | | 25°C | | 410 | 830 | |
| | | | | Full range | | | 1160 | |
| B ₁ | Unity-gain bandwidth | C _L = 200 pF | | 25°C | | 1 | | MHz |
| Φ _m | Phase margin | | | 25°C | | 60 | | deg |
| G _m | Gain margin | | | 25°C | | 10 | | dB |
| V _n | Equivalent input noise voltage | f = 1 kHz | | 25°C | | 39 | | nV/√Hz |
| I _n | Equivalent input noise current | f = 1 kHz | | 25°C | | 0.21 | | pA/√Hz |
| SR | Slew rate | | | 25°C | | 1 | | V/μs |

(1) Full range $T_A = -40^\circ\text{C}$ to 125°C for I temperature (LMV321, LMV358, LMV324, LMV321IDCK), -40°C to 85°C for (LMV324S) and -40°C to 125°C for Q temperature.

(2) Typical values represent the likely parametric nominal values determined at the time of characterization. Typical values depend on the application and configuration and may vary over time. Typical values are not ensured on production material.

7.7 Shutdown Characteristics, LMV324S: $V_{CC+} = 2.7\text{ V}$

 $V_{CC+} = 2.7\text{ V}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP ⁽¹⁾ | MAX | UNIT |
|--|---|-----|--------------------|-----|---------------|
| $I_{CC(SHDN)}$ Supply current in shutdown mode (per channel) | $\overline{\text{SHDN}} \leq 0.6\text{ V}$ | | | 5 | μA |
| $t_{(on)}$ Amplifier turn-on time | $A_V = 1$, $R_L = \text{Open}$ (measured at 50% point) | | 2 | | μs |
| $t_{(off)}$ Amplifier turn-off time | $A_V = 1$, $R_L = \text{Open}$ (measured at 50% point) | | 40 | | ns |

(1) Typical values represent the likely parametric nominal values determined at the time of characterization. Typical values depend on the application and configuration and may vary over time. Typical values are not ensured on production material.

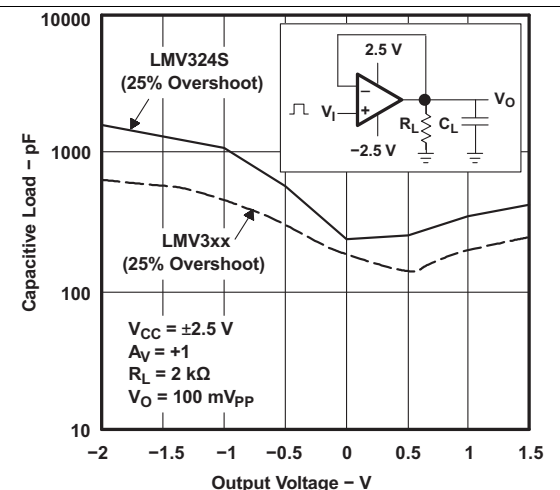
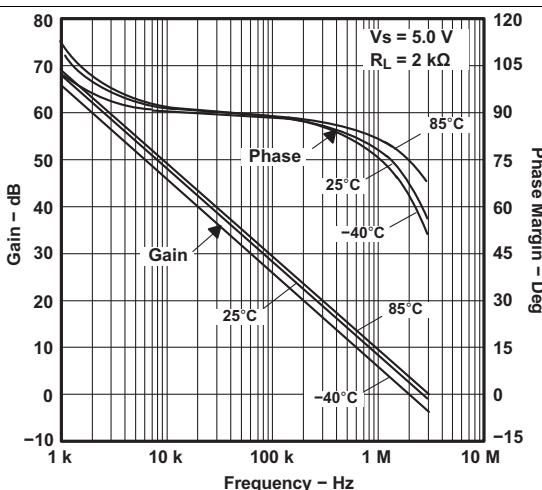
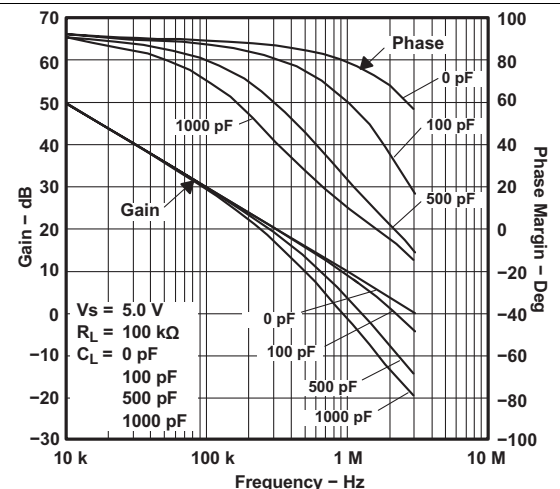
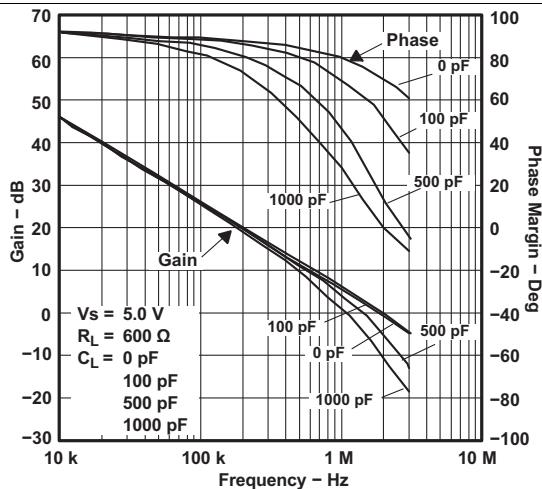
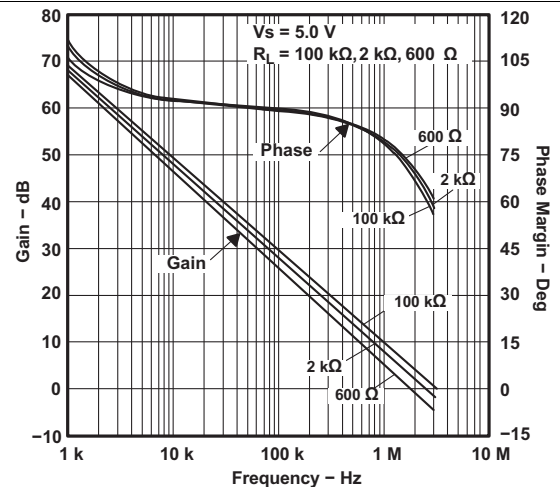
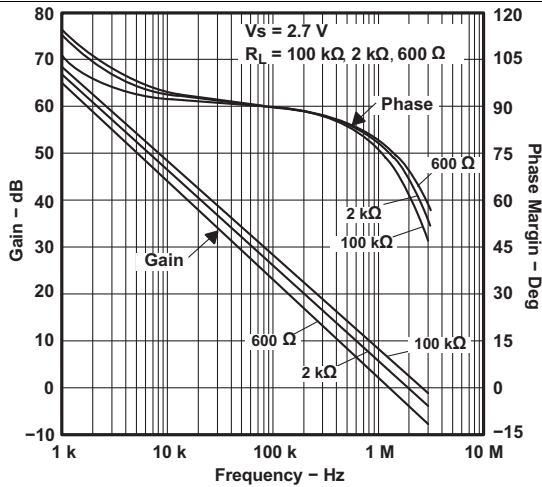
7.8 Shutdown Characteristics, LMV324S: $V_{CC+} = 5\text{ V}$

 $V_{CC+} = 5\text{ V}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

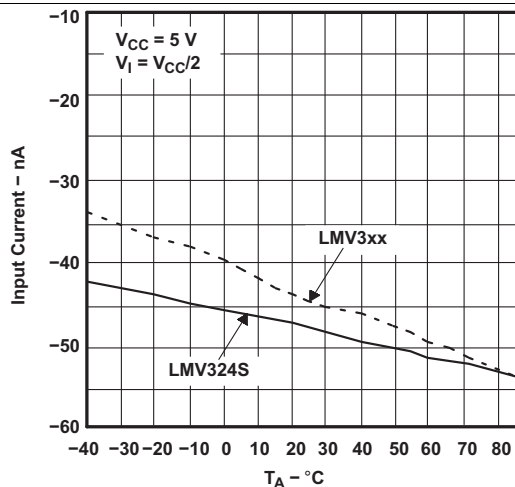
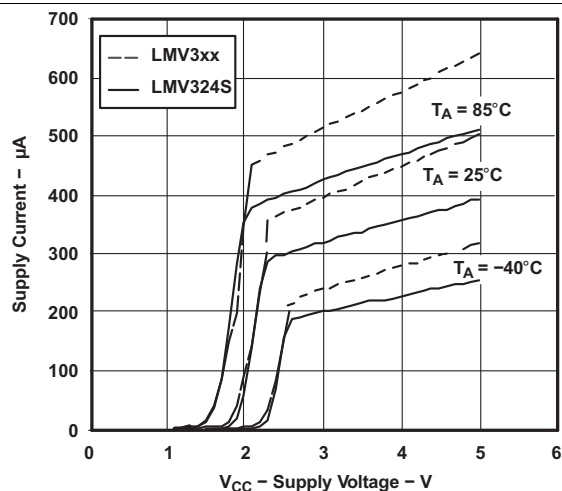
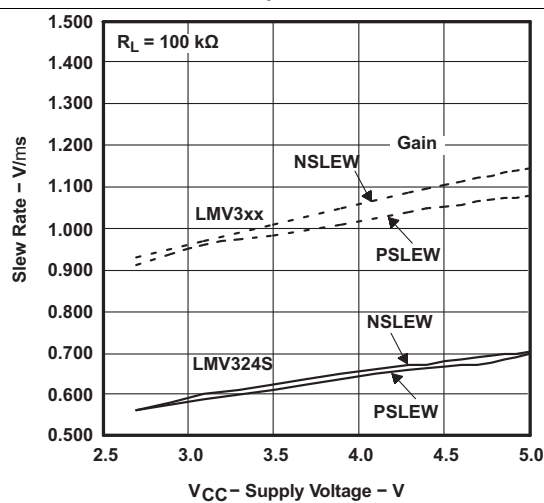
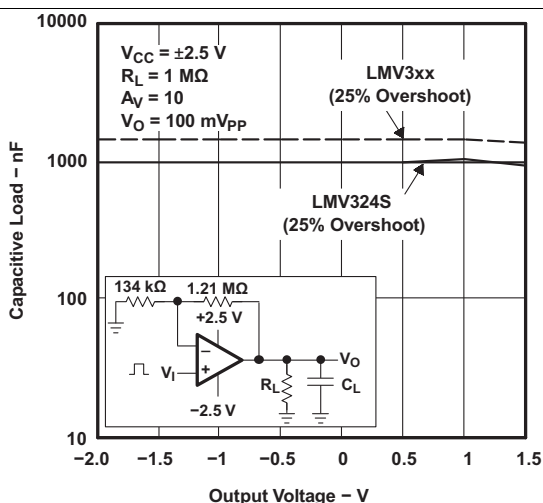
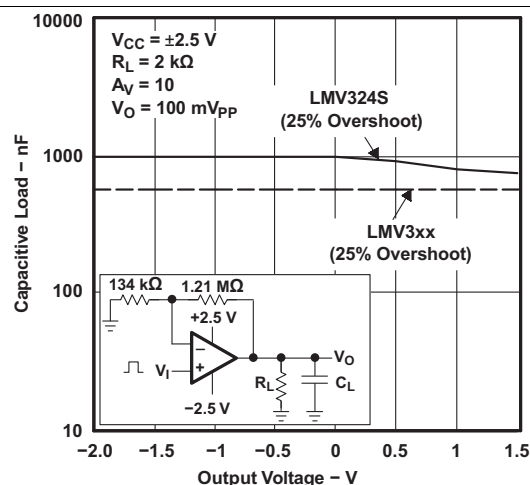
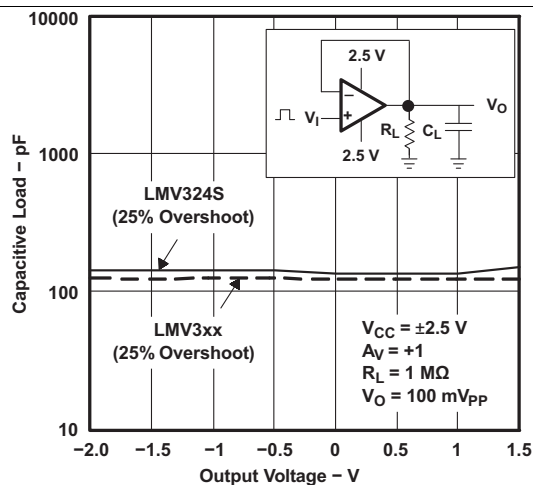
| PARAMETER | TEST CONDITIONS | MIN | TYP ⁽¹⁾ | MAX | UNIT |
|--|--|-----|--------------------|-----|---------------|
| $I_{CC(SHDN)}$ Supply current in shutdown mode (per channel) | $\overline{\text{SHDN}} \leq 0.6\text{ V}$, $T_A = \text{Full Temperature Range}$ | | | 5 | μA |
| $t_{(on)}$ Amplifier turn-on time | $A_V = 1$, $R_L = \text{Open}$ (measured at 50% point) | | 2 | | μs |
| $t_{(off)}$ Amplifier turn-off time | $A_V = 1$, $R_L = \text{Open}$ (measured at 50% point) | | 40 | | ns |

(1) Typical values represent the likely parametric nominal values determined at the time of characterization. Typical values depend on the application and configuration and may vary over time. Typical values are not ensured on production material.

7.9 Typical Characteristics



Typical Characteristics (continued)



Typical Characteristics (continued)

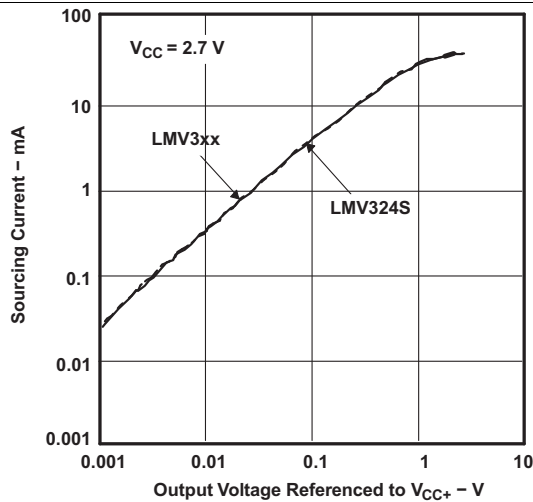


Figure 13. Source Current vs Output Voltage

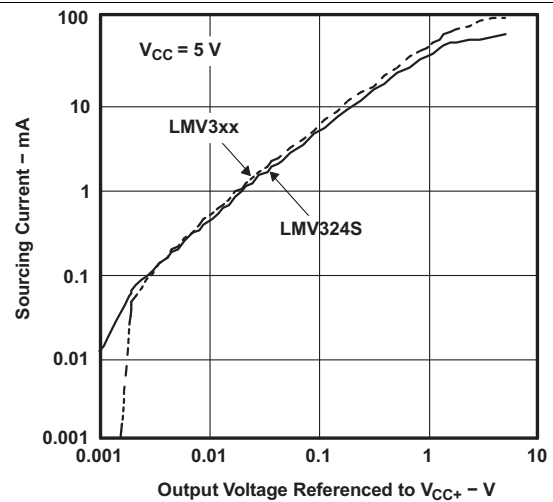


Figure 14. Source Current vs Output Voltage

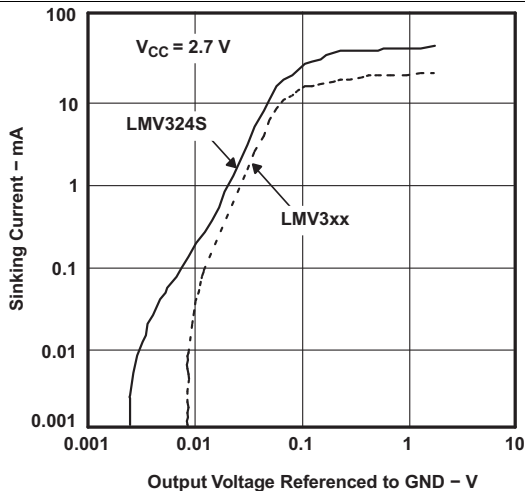


Figure 15. Sinking Current vs Output Voltage

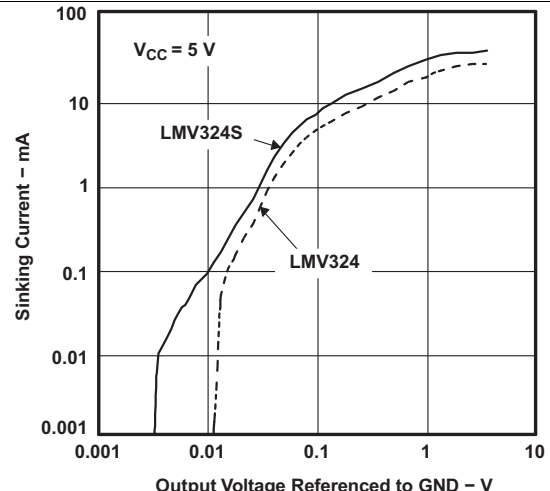


Figure 16. Sinking Current vs Output Voltage

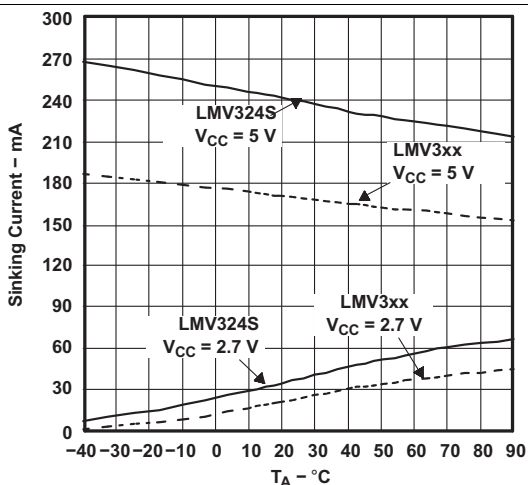


Figure 17. Short-Circuit Current vs Temperature

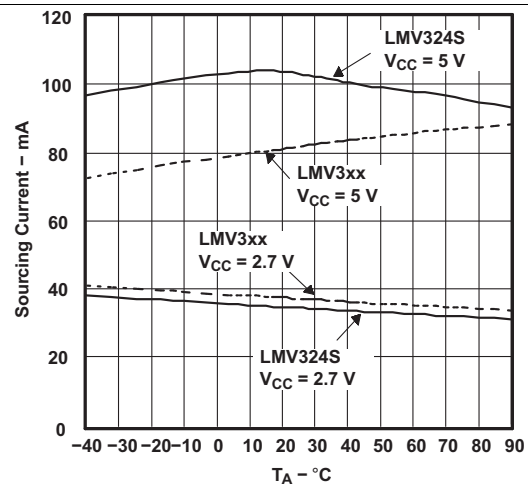


Figure 18. Short-Circuit Current vs Temperature

Typical Characteristics (continued)

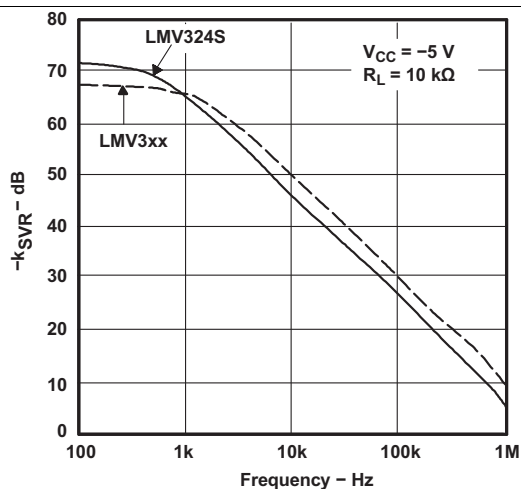


Figure 19. $-k_{SVR}$ vs Frequency

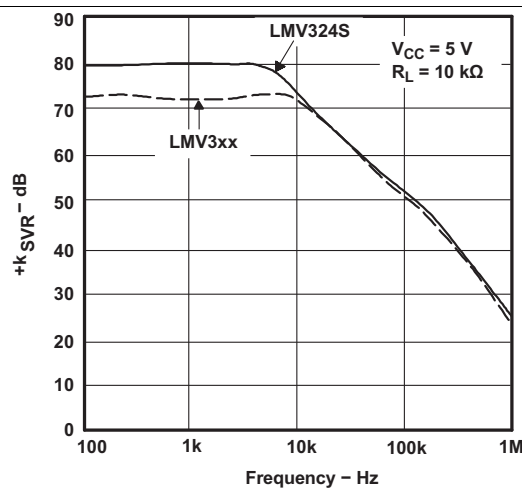


Figure 20. $+k_{SVR}$ vs Frequency

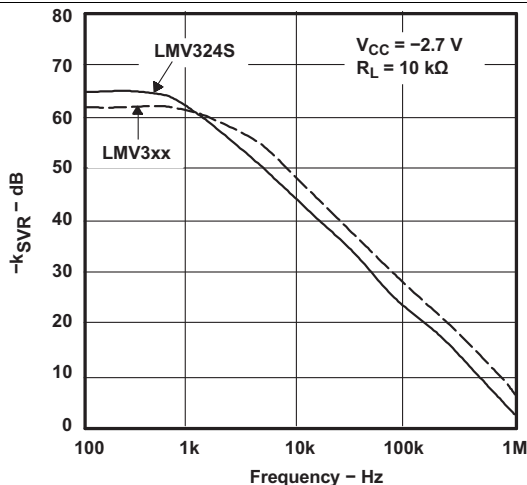


Figure 21. $-k_{SVR}$ vs Frequency

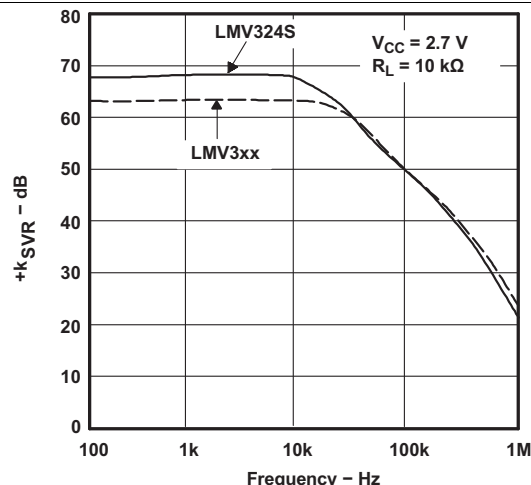


Figure 22. $+k_{SVR}$ vs Frequency

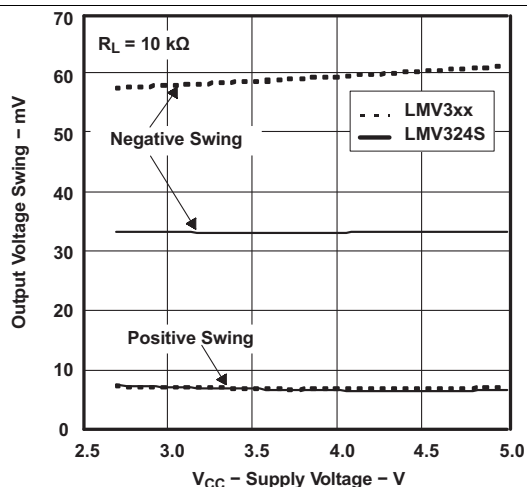


Figure 23. Output Voltage Swing From Rails vs Supply Voltage

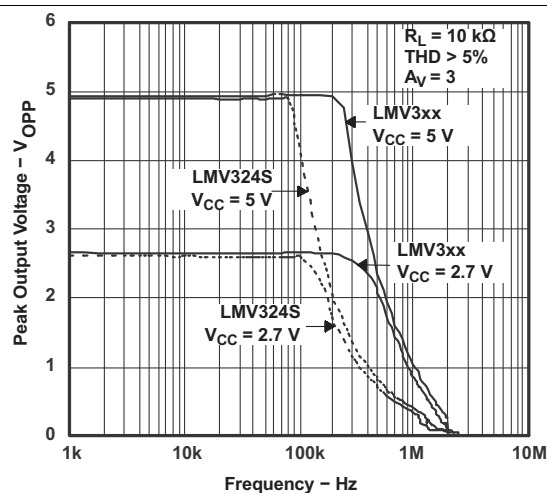


Figure 24. Output Voltage vs Frequency

Typical Characteristics (continued)

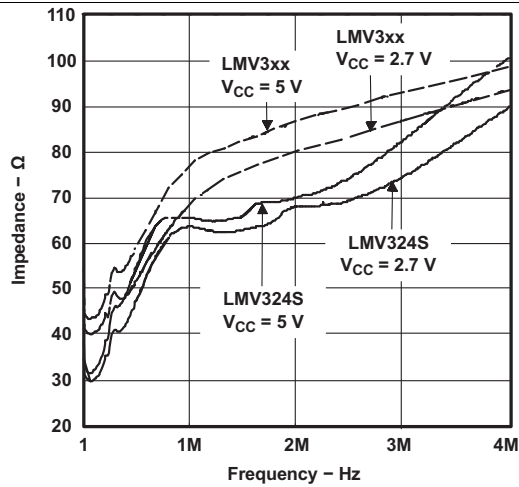


Figure 25. Open-Loop Output Impedance vs Frequency

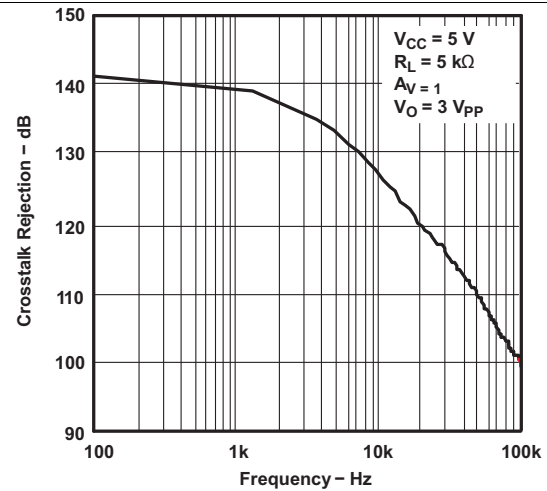


Figure 26. Cross-Talk Rejection vs Frequency

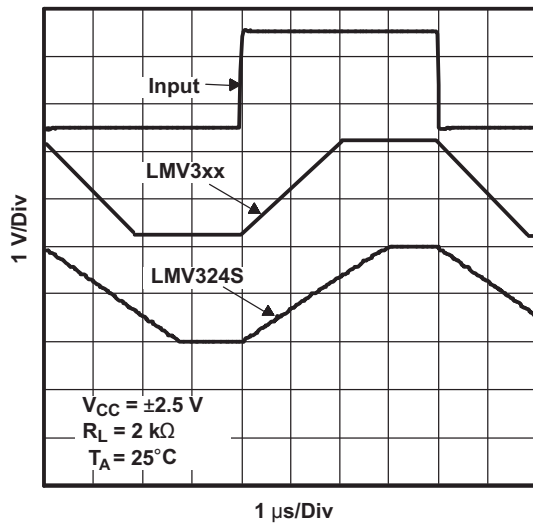


Figure 27. Noninverting Large-Signal Pulse Response

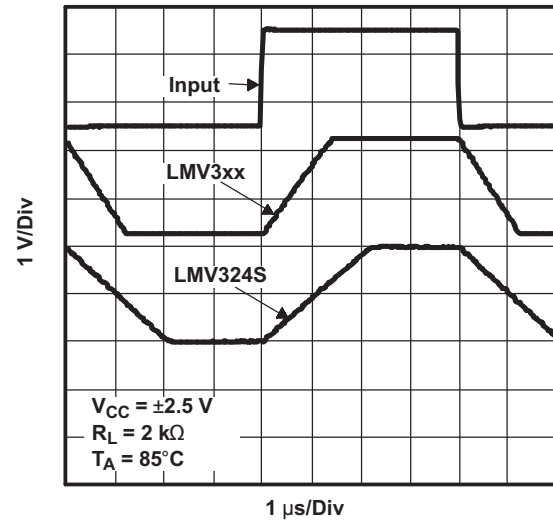


Figure 28. Noninverting Large-Signal Pulse Response

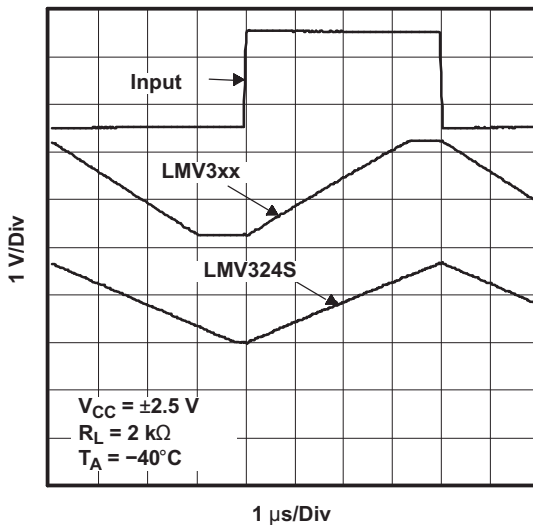


Figure 29. Noninverting Large-Signal Pulse Response

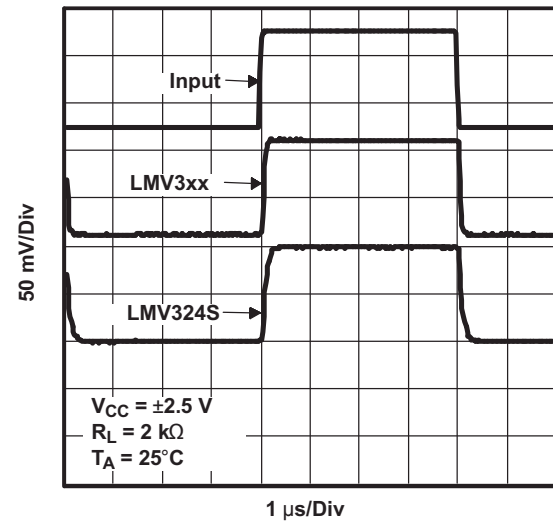


Figure 30. Noninverting Small-Signal Pulse Response

Typical Characteristics (continued)

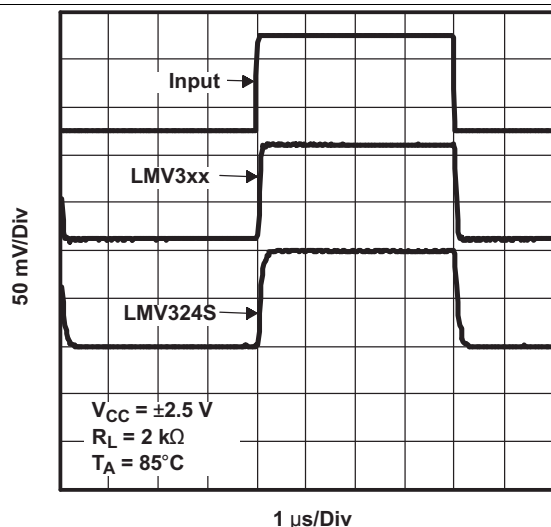


Figure 31. Noninverting Small-Signal Pulse Response

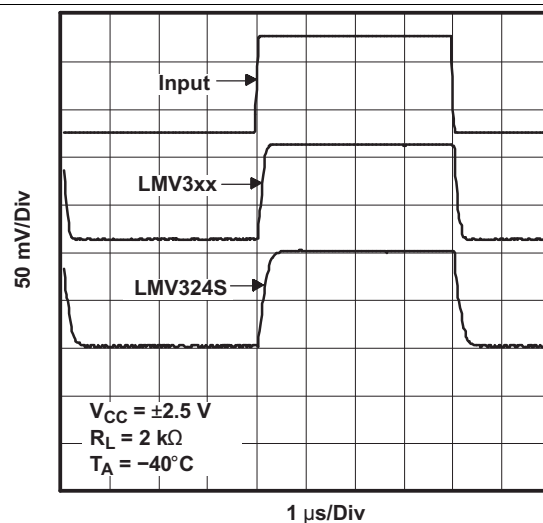


Figure 32. Noninverting Small-Signal Pulse Response

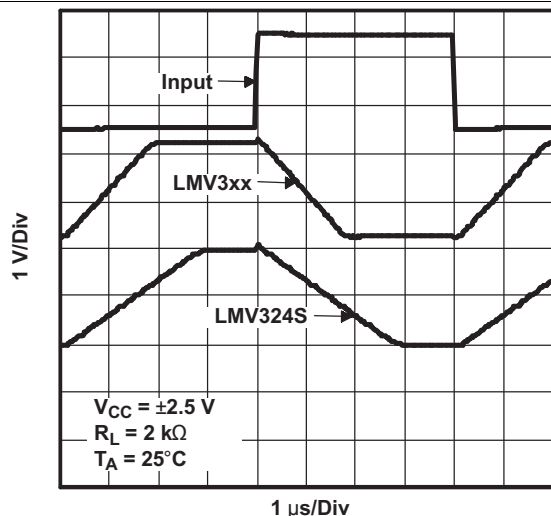


Figure 33. Inverting Large-Signal Pulse Response

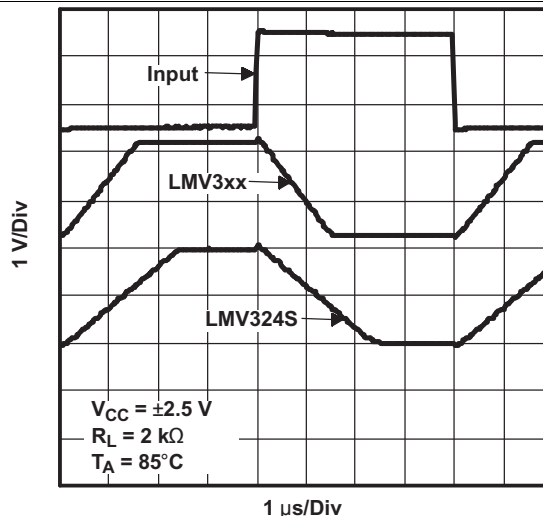


Figure 34. Inverting Large-Signal Pulse Response

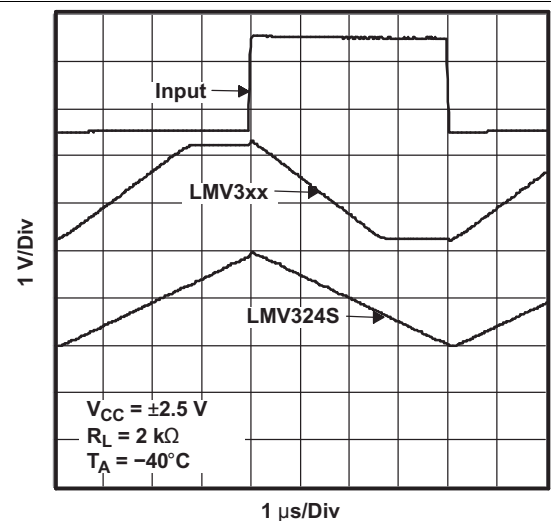


Figure 35. Inverting Large-Signal Pulse Response

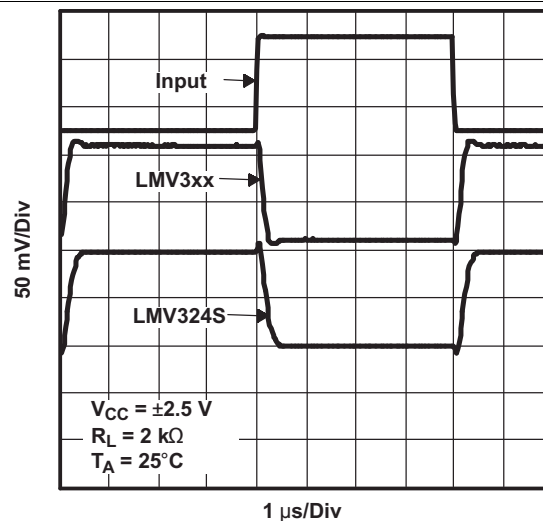
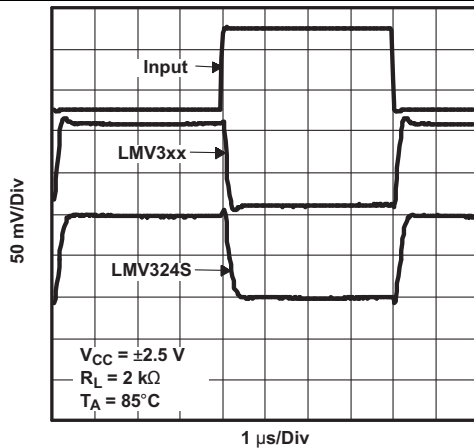
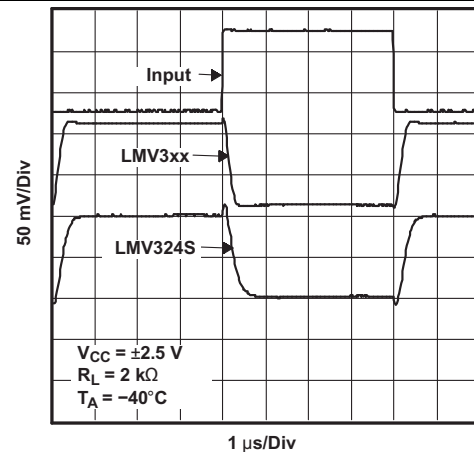
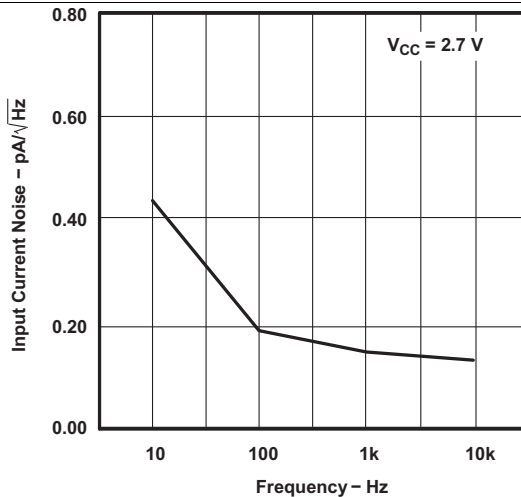
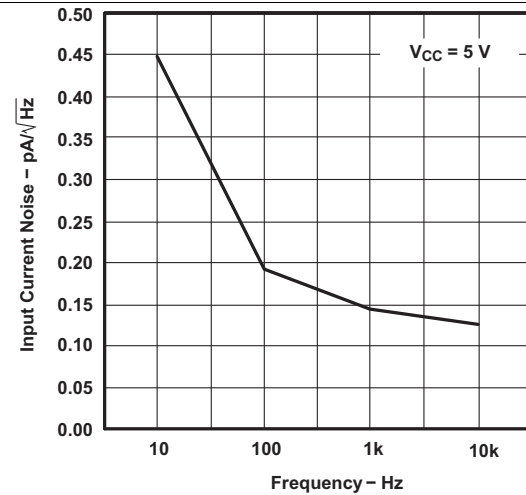
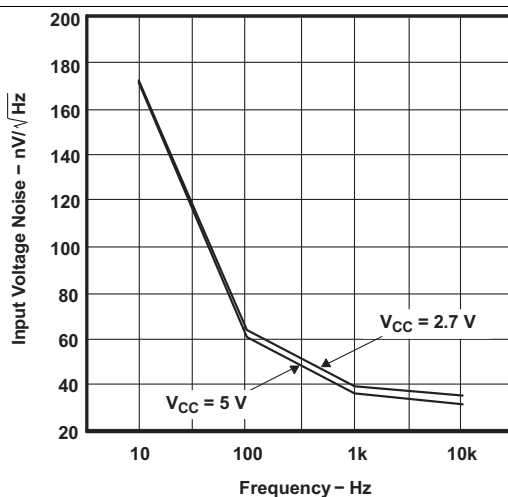
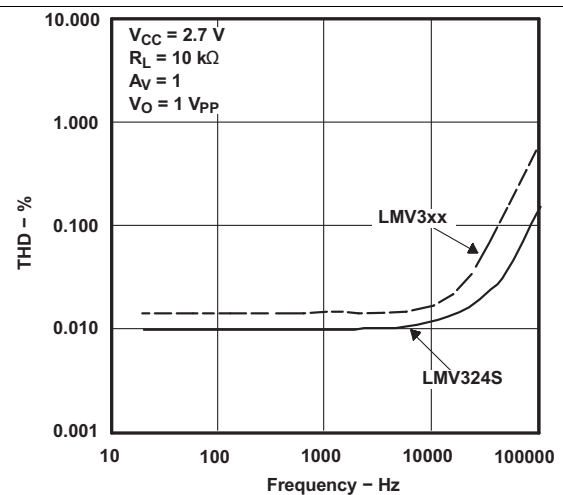
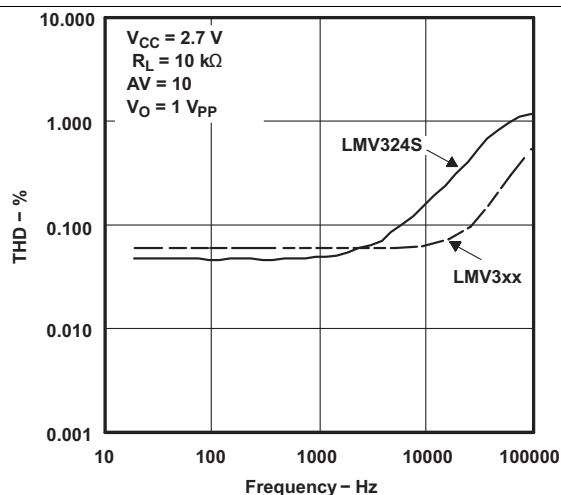


Figure 36. Inverting Small-Signal Pulse Response

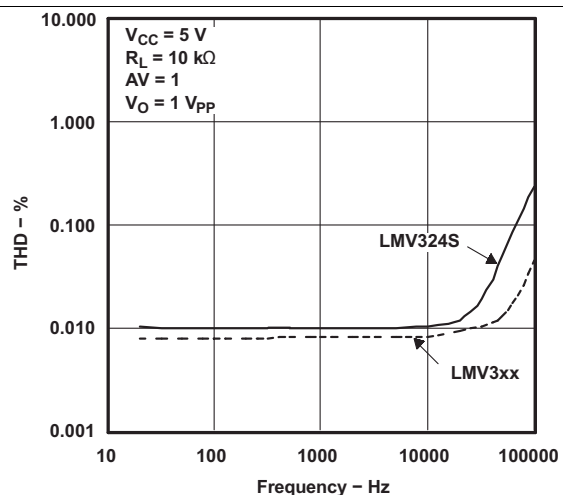
Typical Characteristics (continued)


Figure 37. Inverting Small-Signal Pulse Response

Figure 38. Inverting Small-Signal Pulse Response

Figure 39. Input Current Noise vs Frequency

Figure 40. Input Current Noise vs Frequency

Figure 41. Input Voltage Noise vs Frequency

Figure 42. THD + N vs Frequency

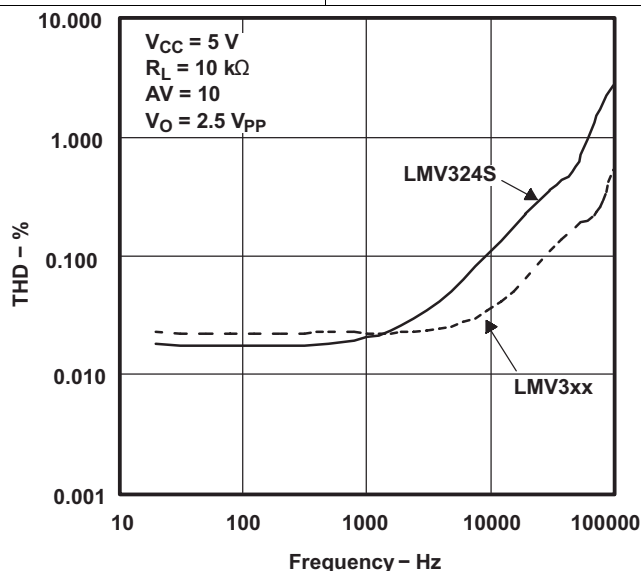
Typical Characteristics (continued)



**Figure 43. THD + N
vs Frequency**



**Figure 44. THD + N
vs Frequency**



**Figure 45. THD + N
vs Frequency**

8 Detailed Description

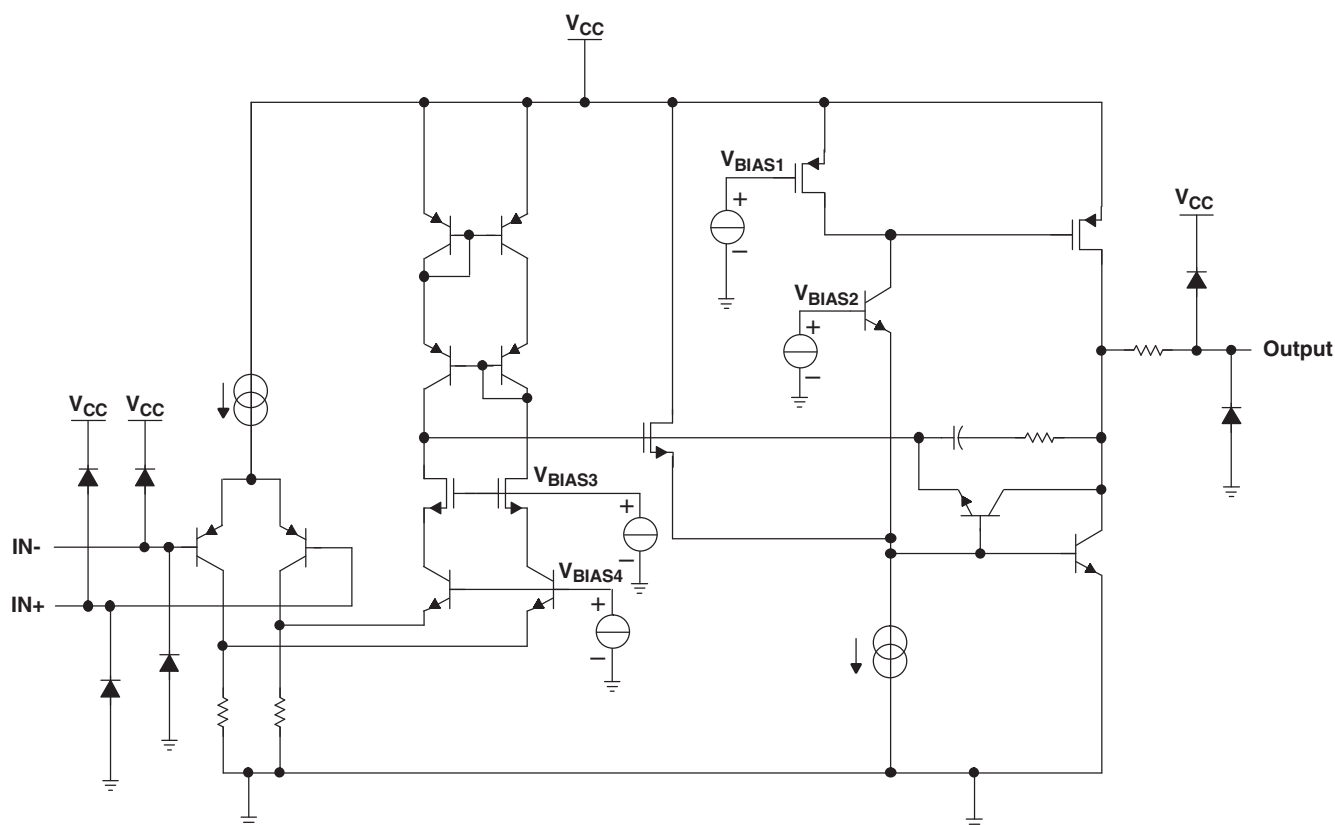
8.1 Overview

The LMV321, LMV358, LMV324, and LMV324S devices are single, dual, and quad low-voltage (2.7 V to 5.5 V) operational amplifiers with rail-to-rail output swing. The LMV324S device, which is a variation of the standard LMV324 device, includes a power-saving shutdown feature that reduces supply current when the amplifiers are not needed. Channels 1 and 2 together are put in shutdown, as are channels 3 and 4. While in shutdown, the outputs actively are pulled low.

The LMV321, LMV358, LMV324, and LMV324S devices are the most cost-effective solutions for applications where low-voltage operation, space saving, and low cost are needed. These amplifiers are designed specifically for low-voltage (2.7 V to 5 V) operation, with performance specifications meeting or exceeding the LM358 and LM324 devices that operate from 5 V to 30 V. Additional features of the LMV3xx devices are a common-mode input voltage range that includes ground, 1-MHz unity-gain bandwidth, and 1-V/ μ s slew rate.

The LMV321 device is available in the ultra-small package, which is approximately one-half the size of the DBV (SOT-23) package. This package saves space on printed circuit boards and enables the design of small portable electronic devices. It also allows the designer to place the device closer to the signal source to reduce noise pickup and increase signal integrity.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Operating Voltage

The LMV321, LMV358, LMV324, LMV324S devices are fully specified and ensured for operation from 2.7 V to 5 V. In addition, many specifications apply from -40°C to 125°C . Parameters that vary significantly with operating voltages or temperature are shown in the [Typical Characteristics](#) graphs.

8.3.2 Unity-Gain Bandwidth

The unity-gain bandwidth is the frequency up to which an amplifier with a unity gain may be operated without greatly distorting the signal. The LMV321, LMV358, LMV324, LMV324S devices have a 1-MHz unity-gain bandwidth.

8.3.3 Slew Rate

The slew rate is the rate at which an operational amplifier can change its output when there is a change on the input. The LMV321, LMV358, LMV324, LMV324S devices have a 1-V/ μs slew rate.

8.4 Device Functional Modes

The LMV321, LMV358, LMV324, LMV324S devices are powered on when the supply is connected. The LMV324S device, which is a variation of the standard LMV324 device, includes a power-saving shutdown feature that reduces supply current to a maximum of 5 μA per channel when the amplifiers are not needed. Each of these devices can be operated as a single supply operational amplifier or dual supply amplifier depending on the application.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Typical Application

Some applications require differential signals. [Figure 46](#) shows a simple circuit to convert a single-ended input of 0.5 to 2 V into differential output of ± 1.5 V on a single 2.7-V supply. The output range is intentionally limited to maximize linearity. The circuit is composed of two amplifiers. One amplifier acts as a buffer and creates a voltage, V_{OUT+} . The second amplifier inverts the input and adds a reference voltage to generate V_{OUT-} . Both V_{OUT+} and V_{OUT-} range from 0.5 to 2 V. The difference, V_{DIFF} , is the difference between V_{OUT+} and V_{OUT-} . The LMV358 was used to build this circuit.

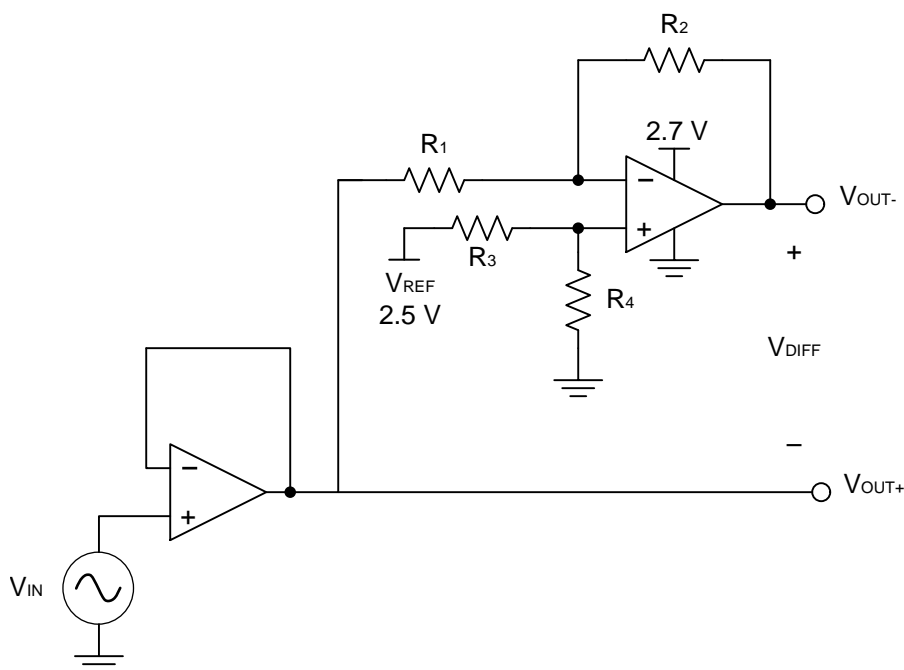


Figure 46. Schematic for Single-Ended Input to Differential Output Conversion

Typical Application (continued)

9.1.1 Design Requirements

The design requirements are as follows:

- Supply voltage: 2.7 V
- Reference voltage: 2.5 V
- Input: 0.5 to 2 V
- Output differential: ± 1.5 V

9.1.2 Detailed Design Procedure

The circuit in [Figure 46](#) takes a single-ended input signal, V_{IN} , and generates two output signals, V_{OUT+} and V_{OUT-} using two amplifiers and a reference voltage, V_{REF} . V_{OUT+} is the output of the first amplifier and is a buffered version of the input signal, V_{IN} (see [Equation 1](#)). V_{OUT-} is the output of the second amplifier which uses V_{REF} to add an offset voltage to V_{IN} and feedback to add inverting gain. The transfer function for V_{OUT-} is [Equation 2](#).

$$V_{OUT+} = V_{IN} \quad (1)$$

$$V_{OUT-} = V_{REF} \times \left(\frac{R_4}{R_3 + R_4} \right) \times \left(1 + \frac{R_2}{R_1} \right) - V_{IN} \times \frac{R_2}{R_1} \quad (2)$$

The differential output signal, V_{DIFF} , is the difference between the two single-ended output signals, V_{OUT+} and V_{OUT-} . [Equation 3](#) shows the transfer function for V_{DIFF} . By applying the conditions that $R_1 = R_2$ and $R_3 = R_4$, the transfer function is simplified into [Equation 6](#). Using this configuration, the maximum input signal is equal to the reference voltage and the maximum output of each amplifier is equal to the V_{REF} . The differential output range is $2 \times V_{REF}$. Furthermore, the common mode voltage will be one half of V_{REF} (see [Equation 7](#)).

$$V_{DIFF} = V_{OUT+} - V_{OUT-} = V_{IN} \times \left(1 + \frac{R_2}{R_1} \right) - V_{REF} \times \left(\frac{R_4}{R_3 + R_4} \right) \left(1 + \frac{R_2}{R_1} \right) \quad (3)$$

$$V_{OUT+} = V_{IN} \quad (4)$$

$$V_{OUT-} = V_{REF} - V_{IN} \quad (5)$$

$$V_{DIFF} = 2 \times V_{IN} - V_{REF} \quad (6)$$

$$V_{cm} = \left(\frac{V_{OUT+} + V_{OUT-}}{2} \right) = \frac{1}{2} V_{REF} \quad (7)$$

9.1.2.1 Amplifier Selection

Linearity over the input range is key for good dc accuracy. The common mode input range and the output swing limitations determine the linearity. In general, an amplifier with rail-to-rail input and output swing is required. Bandwidth is a key concern for this design. Because LMV358 has a bandwidth of 1 MHz, this circuit will only be able to process signals with frequencies of less than 1 MHz.

9.1.2.2 Passive Component Selection

Because the transfer function of V_{OUT-} is heavily reliant on resistors (R_1 , R_2 , R_3 , and R_4), use resistors with low tolerances to maximize performance and minimize error. This design used resistors with resistance values of 36 k Ω with tolerances measured to be within 2%. If the noise of the system is a key parameter, the user can select smaller resistance values (6 k Ω or lower) to keep the overall system noise low. This ensures that the noise from the resistors is lower than the amplifier noise.

Typical Application (continued)

9.1.3 Application Curves

The measured transfer functions in [Figure 47](#), [Figure 48](#), and [Figure 49](#) were generated by sweeping the input voltage from 0 V to 2.5 V. However, this design should only be used between 0.5 V and 2 V for optimum linearity.

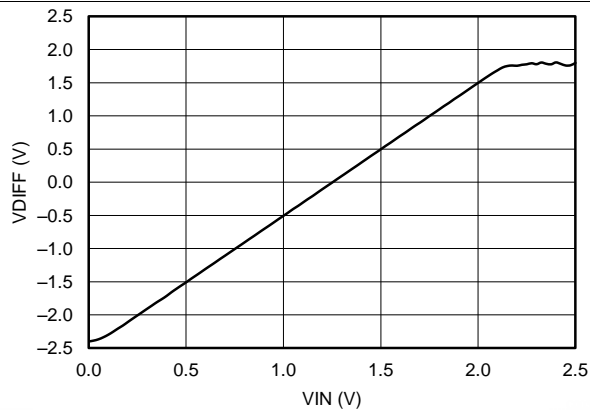


Figure 47. Differential Output Voltage vs Input Voltage

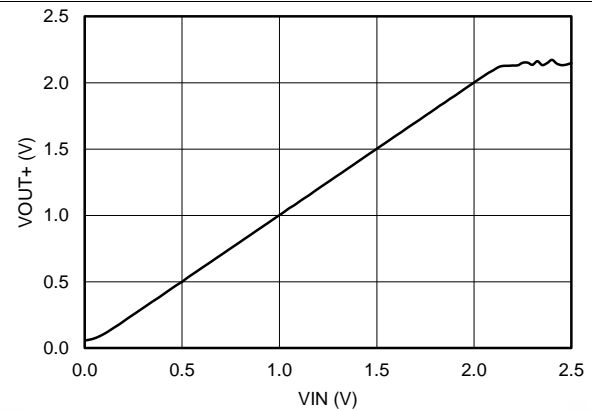


Figure 48. Positive Output Voltage Node vs Input Voltage

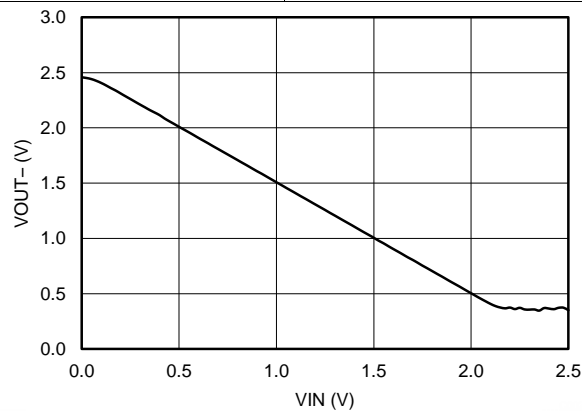


Figure 49. Positive Output Voltage Node vs Input Voltage

10 Power Supply Recommendations

The LMV321, LMV358, LMV324, LMV324S devices are specified for operation from 2.7 to 5 V; many specifications apply from -40°C to 125°C . The [Typical Characteristics](#) section presents parameters that can exhibit significant variance with regard to operating voltage or temperature.

CAUTION

Supply voltages larger than 5.5 V can permanently damage the device (see the [Absolute Maximum Ratings](#)).

Place 0.1- μF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high impedance power supplies. For more detailed information on bypass capacitor placement, refer to the [Layout](#).

11 Layout

11.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole, as well as the operational amplifier. Bypass capacitors are used to reduce the coupled noise by providing low impedance power sources local to the analog circuitry.
 - Connect low-ESR, 0.1- μ F ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds, paying attention to the flow of the ground current. For more detailed information, refer to *Circuit Board Layout Techniques*, (SLOA089).
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If it is not possible to keep them separate, it is much better to cross the sensitive trace perpendicular as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. Keeping RF and RG close to the inverting input minimizes parasitic capacitance, as shown in [Layout Example](#).
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

11.2 Layout Example

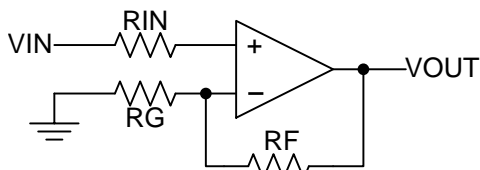


Figure 50. Operational Amplifier Schematic for Noninverting Configuration

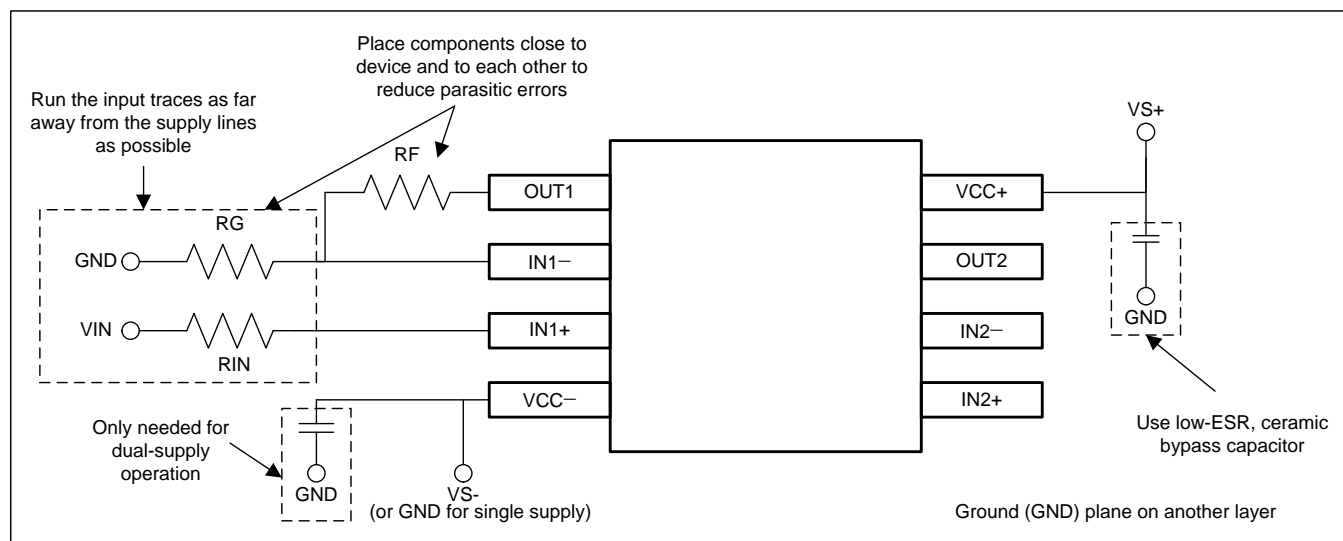


Figure 51. Operational Amplifier Board Layout for Noninverting Configuration

12 Device and Documentation Support

12.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 1. Related Links

| PARTS | PRODUCT FOLDER | SAMPLE & BUY | TECHNICAL DOCUMENTS | TOOLS & SOFTWARE | SUPPORT & COMMUNITY |
|---------|----------------------------|----------------------------|----------------------------|----------------------------|----------------------------|
| LMV321 | Click here | Click here | Click here | Click here | Click here |
| LMV358 | Click here | Click here | Click here | Click here | Click here |
| LMV324 | Click here | Click here | Click here | Click here | Click here |
| LMV324S | Click here | Click here | Click here | Click here | Click here |

12.2 Trademarks

All trademarks are the property of their respective owners.

12.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.4 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|--------------------|------|----------------|----------------------------|----------------------------|----------------------|--------------|----------------------------------|-------------------------|
| LMV321IDBVR | ACTIVE | SOT-23 | DBV | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | (RC1F ~ RC1K) | Samples |
| LMV321IDBVRG4 | ACTIVE | SOT-23 | DBV | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | (RC1F ~ RC1K) | Samples |
| LMV321IDBVT | ACTIVE | SOT-23 | DBV | 5 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | (RC1F ~ RC1K) | Samples |
| LMV321IDBVT E4 | ACTIVE | SOT-23 | DBV | 5 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | (RC1F ~ RC1K) | Samples |
| LMV321IDBVTG4 | ACTIVE | SOT-23 | DBV | 5 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | (RC1F ~ RC1K) | Samples |
| LMV321IDCKR | ACTIVE | SC70 | DCK | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU CU NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | (R3C ~ R3I ~ R3O ~ R3R ~ R3Z) | Samples |
| LMV321IDCKRG4 | ACTIVE | SC70 | DCK | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | (R3C ~ R3I ~ R3O ~ R3R ~ R3Z) | Samples |
| LMV321IDCKT | ACTIVE | SC70 | DCK | 5 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU CU NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | (R3C ~ R3I ~ R3R) | Samples |
| LMV321IDCKTG4 | ACTIVE | SC70 | DCK | 5 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAUAG | Level-1-260C-UNLIM | -40 to 125 | (R3C ~ R3I ~ R3R) | Samples |
| LMV324ID | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LMV324I | Samples |
| LMV324IDG4 | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LMV324I | Samples |
| LMV324IDR | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU CU SN | Level-1-260C-UNLIM | -40 to 125 | LMV324I | Samples |
| LMV324IDRG4 | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LMV324I | Samples |
| LMV324IPWR | ACTIVE | TSSOP | PW | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU CU SN | Level-1-260C-UNLIM | -40 to 125 | MV324I | Samples |
| LMV324IPWRG4 | ACTIVE | TSSOP | PW | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | MV324I | Samples |
| LMV324QD | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LMV324Q | Samples |
| LMV324QDG4 | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LMV324Q | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|--------------------|------|----------------|----------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| LMV324QDR | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LMV324Q | Samples |
| LMV324QDRG4 | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LMV324Q | Samples |
| LMV324QPW | ACTIVE | TSSOP | PW | 14 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | MV324Q | Samples |
| LMV324QPWG4 | ACTIVE | TSSOP | PW | 14 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | MV324Q | Samples |
| LMV324QPWR | ACTIVE | TSSOP | PW | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | MV324Q | Samples |
| LMV324SID | OBSOLETE | SOIC | D | 16 | | TBD | Call TI | Call TI | -40 to 85 | LMV324SI | |
| LMV324SIDE4 | OBSOLETE | SOIC | D | 16 | | TBD | Call TI | Call TI | -40 to 85 | | |
| LMV324SIDG4 | OBSOLETE | SOIC | D | 16 | | TBD | Call TI | Call TI | -40 to 85 | | |
| LMV324SIDR | OBSOLETE | SOIC | D | 16 | | TBD | Call TI | Call TI | -40 to 85 | LMV324SI | |
| LMV324SIDRE4 | OBSOLETE | SOIC | D | 16 | | TBD | Call TI | Call TI | -40 to 85 | | |
| LMV324SIDRG4 | OBSOLETE | SOIC | D | 16 | | TBD | Call TI | Call TI | -40 to 85 | | |
| LMV324SIPWR | OBSOLETE | TSSOP | PW | 16 | | TBD | Call TI | Call TI | -40 to 85 | MV324SI | |
| LMV324SIPWRE4 | OBSOLETE | TSSOP | PW | 16 | | TBD | Call TI | Call TI | -40 to 85 | | |
| LMV324SIPWRG4 | OBSOLETE | TSSOP | PW | 16 | | TBD | Call TI | Call TI | -40 to 85 | | |
| LMV358ID | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | MV358I | Samples |
| LMV358IDDUR | ACTIVE | VSSOP | DDU | 8 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | RA5R | Samples |
| LMV358IDDURG4 | ACTIVE | VSSOP | DDU | 8 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | RA5R | Samples |
| LMV358IDE4 | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | MV358I | Samples |
| LMV358IDG4 | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | MV358I | Samples |
| LMV358IDGKR | ACTIVE | VSSOP | DGK | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | (R5B ~ R5Q ~ R5R) | Samples |
| LMV358IDGKRG4 | ACTIVE | VSSOP | DGK | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | (R5B ~ R5Q ~ R5R) | Samples |
| LMV358IDR | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU CU SN | Level-1-260C-UNLIM | -40 to 125 | MV358I | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|--------------------|------|----------------|----------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| LMV358IDRE4 | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | MV358I | Samples |
| LMV358IDRG4 | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | MV358I | Samples |
| LMV358IPW | ACTIVE | TSSOP | PW | 8 | 150 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | MV358I | Samples |
| LMV358IPWG4 | ACTIVE | TSSOP | PW | 8 | 150 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | MV358I | Samples |
| LMV358IPWR | ACTIVE | TSSOP | PW | 8 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU CU SN | Level-1-260C-UNLIM | -40 to 125 | MV358I | Samples |
| LMV358IPWRE4 | ACTIVE | TSSOP | PW | 8 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | MV358I | Samples |
| LMV358IPWRG4 | ACTIVE | TSSOP | PW | 8 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | MV358I | Samples |
| LMV358QD | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | MV358Q | Samples |
| LMV358QDDUR | ACTIVE | VSSOP | DDU | 8 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | RAHR | Samples |
| LMV358QDDURG4 | ACTIVE | VSSOP | DDU | 8 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | RAHR | Samples |
| LMV358QDG4 | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | MV358Q | Samples |
| LMV358QDGKR | ACTIVE | VSSOP | DGK | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | (RHO ~ RHR) | Samples |
| LMV358QDGKRG4 | ACTIVE | VSSOP | DGK | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | (RHO ~ RHR) | Samples |
| LMV358QDR | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | MV358Q | Samples |
| LMV358QPWR | ACTIVE | TSSOP | PW | 8 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | MV358Q | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

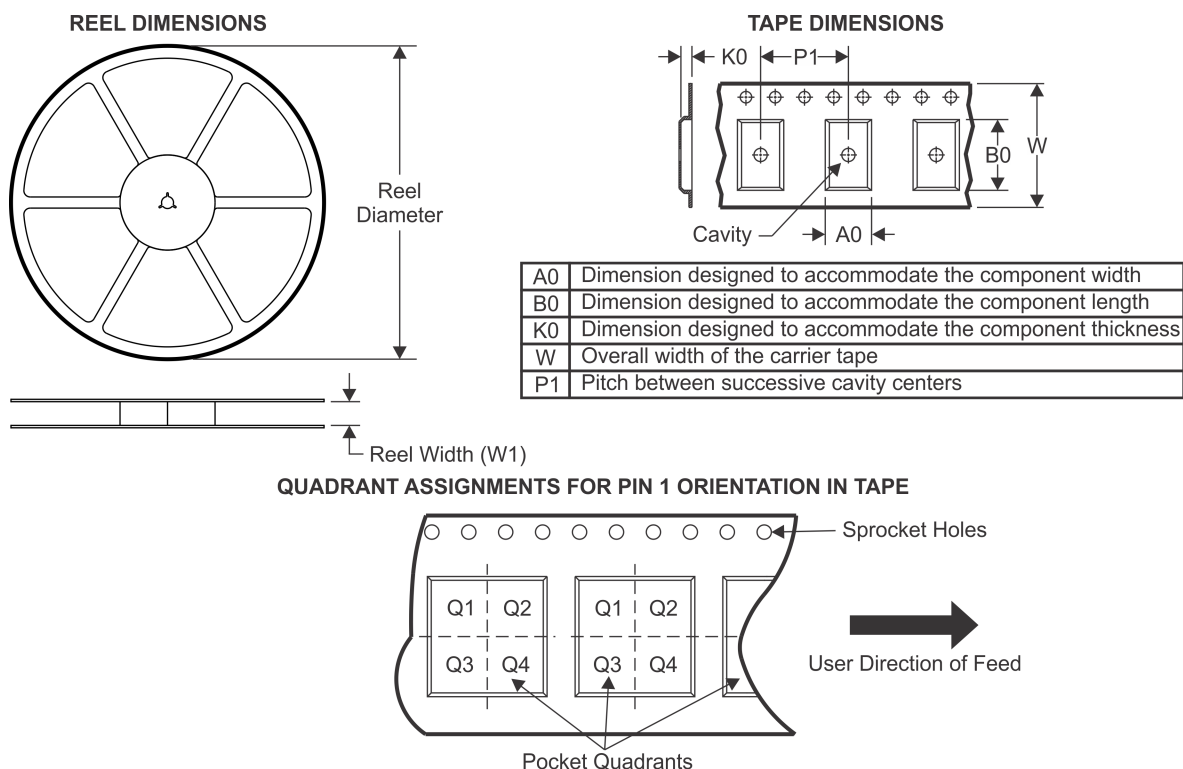
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF LMV324, LMV358 :

- Automotive: [LMV324-Q1](#), [LMV358-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

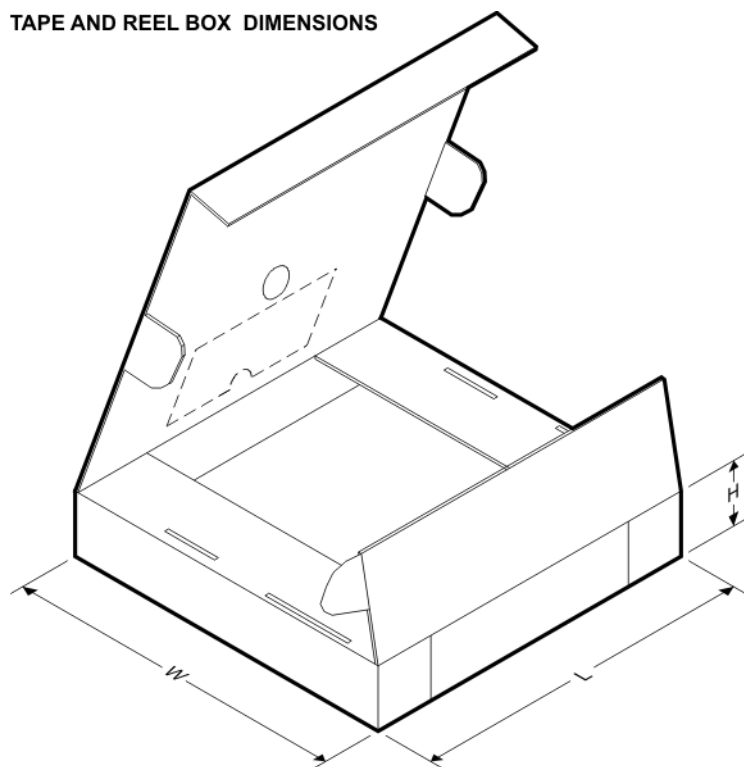
TAPE AND REEL INFORMATION


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| LMV321IDBVR | SOT-23 | DBV | 5 | 3000 | 178.0 | 9.0 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| LMV321IDBVT | SOT-23 | DBV | 5 | 250 | 178.0 | 9.0 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| LMV321IDBVT | SOT-23 | DBV | 5 | 250 | 180.0 | 9.2 | 3.17 | 3.23 | 1.37 | 4.0 | 8.0 | Q3 |
| LMV321IDCKR | SC70 | DCK | 5 | 3000 | 178.0 | 9.0 | 2.4 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |
| LMV321IDCKR | SC70 | DCK | 5 | 3000 | 180.0 | 9.2 | 2.3 | 2.55 | 1.2 | 4.0 | 8.0 | Q3 |
| LMV321IDCKT | SC70 | DCK | 5 | 250 | 180.0 | 9.2 | 2.3 | 2.55 | 1.2 | 4.0 | 8.0 | Q3 |
| LMV321IDCKT | SC70 | DCK | 5 | 250 | 178.0 | 9.0 | 2.4 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |
| LMV324IDR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| LMV324IDR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| LMV324IDR | SOIC | D | 14 | 2500 | 330.0 | 16.8 | 6.5 | 9.5 | 2.3 | 8.0 | 16.0 | Q1 |
| LMV324IDRG4 | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| LMV324IPWR | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| LMV324IPWRG4 | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| LMV324QDR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| LMV324QPWR | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| LMV358IDDUR | VSSOP | DDU | 8 | 3000 | 180.0 | 8.4 | 2.25 | 3.35 | 1.05 | 4.0 | 8.0 | Q3 |
| LMV358IDGKR | VSSOP | DGK | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| LMV358IDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| LMV358IDR | SOIC | D | 8 | 2500 | 330.0 | 12.8 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| LMV358IDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| LMV358IDRG4 | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| LMV358IPWR | TSSOP | PW | 8 | 2000 | 330.0 | 12.4 | 7.0 | 3.6 | 1.6 | 8.0 | 12.0 | Q1 |
| LMV358QDDUR | VSSOP | DDU | 8 | 3000 | 180.0 | 8.4 | 2.25 | 3.35 | 1.05 | 4.0 | 8.0 | Q3 |
| LMV358QDGKR | VSSOP | DGK | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| LMV358QDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| LMV358QPWR | TSSOP | PW | 8 | 2000 | 330.0 | 12.4 | 7.0 | 3.6 | 1.6 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-------------|--------------|-----------------|------|------|-------------|------------|-------------|
| LMV321IDBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| LMV321IDBVT | SOT-23 | DBV | 5 | 250 | 180.0 | 180.0 | 18.0 |
| LMV321IDBVT | SOT-23 | DBV | 5 | 250 | 205.0 | 200.0 | 33.0 |
| LMV321IDCKR | SC70 | DCK | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| LMV321IDCKR | SC70 | DCK | 5 | 3000 | 205.0 | 200.0 | 33.0 |
| LMV321IDCKT | SC70 | DCK | 5 | 250 | 205.0 | 200.0 | 33.0 |
| LMV321IDCKT | SC70 | DCK | 5 | 250 | 180.0 | 180.0 | 18.0 |
| LMV324IDR | SOIC | D | 14 | 2500 | 333.2 | 345.9 | 28.6 |
| LMV324IDR | SOIC | D | 14 | 2500 | 367.0 | 367.0 | 38.0 |

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| LMV324IDR | SOIC | D | 14 | 2500 | 364.0 | 364.0 | 27.0 |
| LMV324IDRG4 | SOIC | D | 14 | 2500 | 333.2 | 345.9 | 28.6 |
| LMV324IPWR | TSSOP | PW | 14 | 2000 | 364.0 | 364.0 | 27.0 |
| LMV324IPWRG4 | TSSOP | PW | 14 | 2000 | 367.0 | 367.0 | 35.0 |
| LMV324QDR | SOIC | D | 14 | 2500 | 367.0 | 367.0 | 38.0 |
| LMV324QPWR | TSSOP | PW | 14 | 2000 | 367.0 | 367.0 | 35.0 |
| LMV358IDDUR | VSSOP | DDU | 8 | 3000 | 202.0 | 201.0 | 28.0 |
| LMV358IDGKR | VSSOP | DGK | 8 | 2500 | 358.0 | 335.0 | 35.0 |
| LMV358IDR | SOIC | D | 8 | 2500 | 340.5 | 338.1 | 20.6 |
| LMV358IDR | SOIC | D | 8 | 2500 | 364.0 | 364.0 | 27.0 |
| LMV358IDR | SOIC | D | 8 | 2500 | 367.0 | 367.0 | 35.0 |
| LMV358IDRG4 | SOIC | D | 8 | 2500 | 340.5 | 338.1 | 20.6 |
| LMV358IPWR | TSSOP | PW | 8 | 2000 | 364.0 | 364.0 | 27.0 |
| LMV358QDDUR | VSSOP | DDU | 8 | 3000 | 202.0 | 201.0 | 28.0 |
| LMV358QDGKR | VSSOP | DGK | 8 | 2500 | 358.0 | 335.0 | 35.0 |
| LMV358QDR | SOIC | D | 8 | 2500 | 340.5 | 338.1 | 20.6 |
| LMV358QPWR | TSSOP | PW | 8 | 2000 | 367.0 | 367.0 | 35.0 |

DBV (R-PDSO-G5)

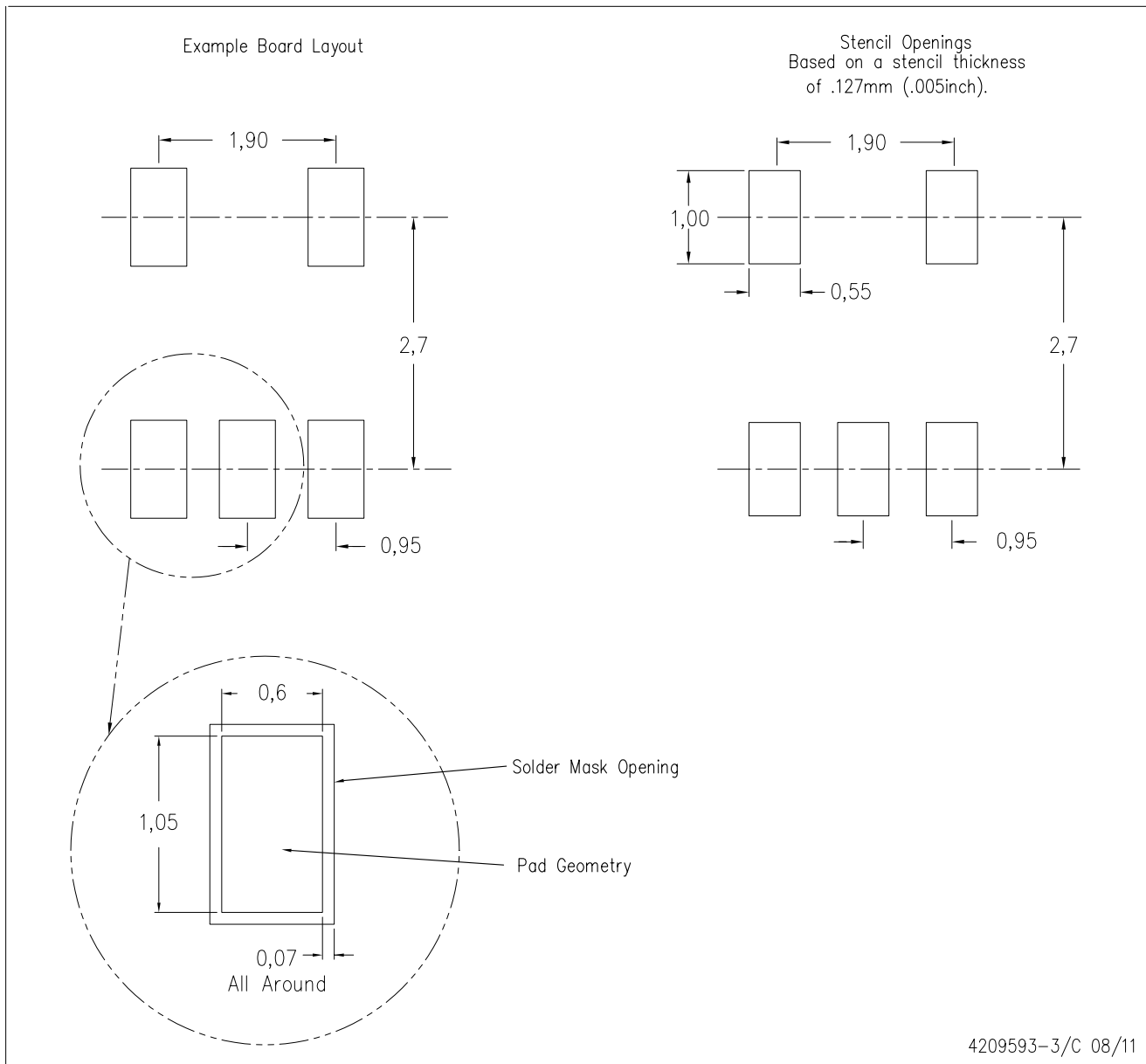
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 - D. Falls within JEDEC MO-178 Variation AA.

DBV (R-PDSO-G5)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - D. Publication IPC-7351 is recommended for alternate designs.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

DCK (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE



4093553-3/G 01/2007

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 - Falls within JEDEC MO-203 variation AA.

DCK (R-PDSO-G5)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - D. Publication IPC-7351 is recommended for alternate designs.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

DGK (S-PDSO-G8)

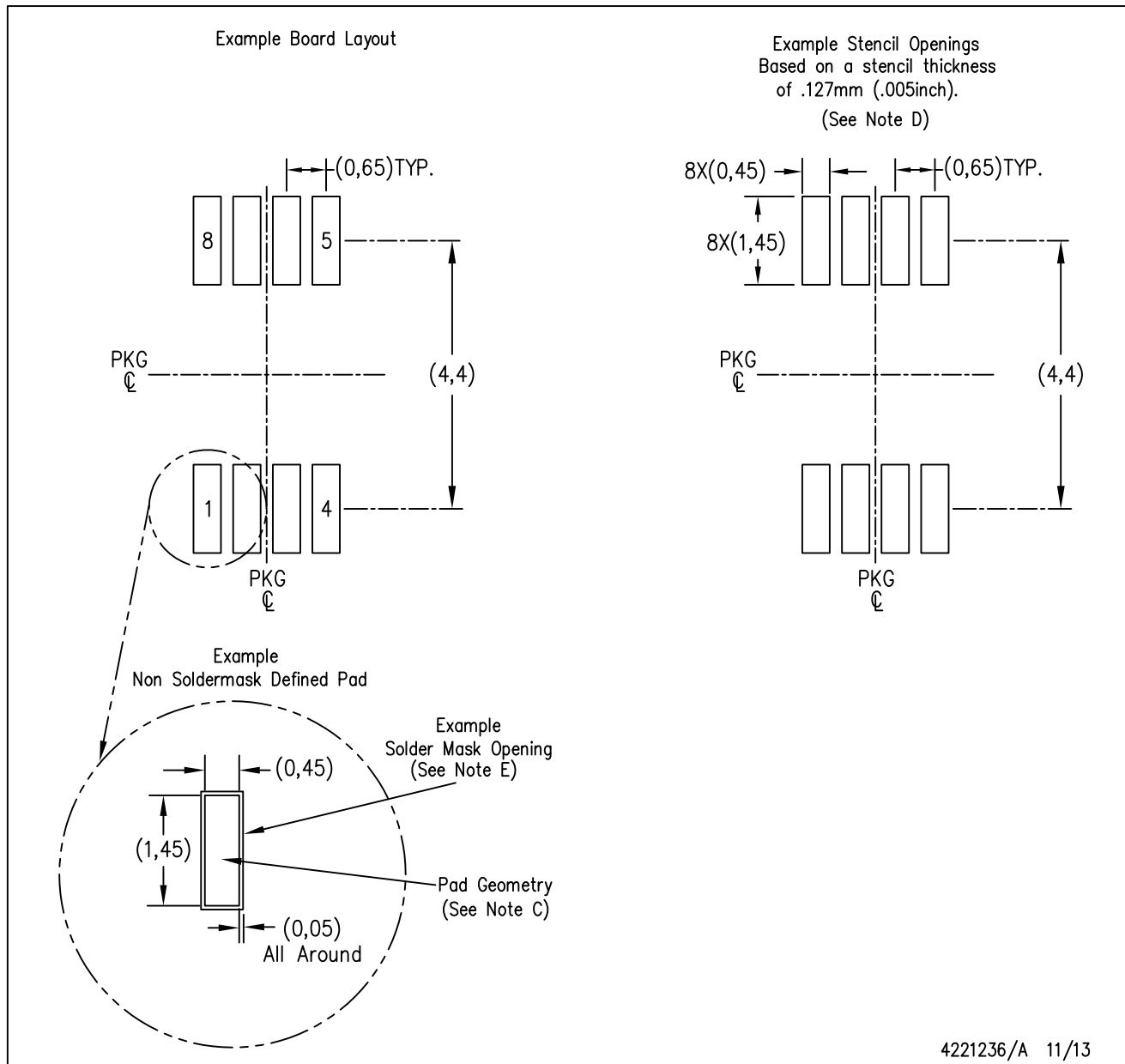
PLASTIC SMALL-OUTLINE PACKAGE



4073329/E 05/06

DGK (S-PDSO-G8)

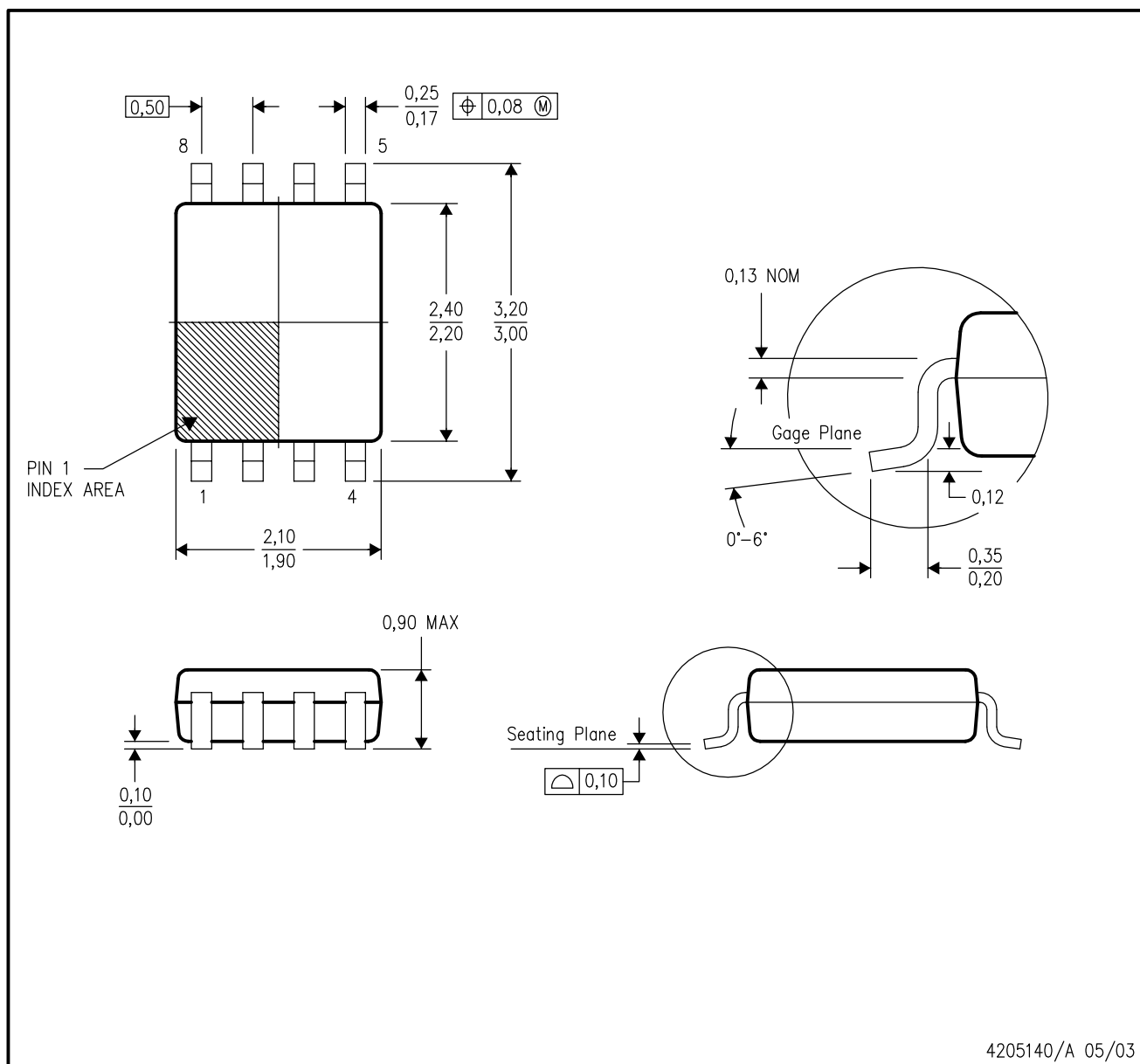
PLASTIC SMALL OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DDU (R-PDSO-G8)

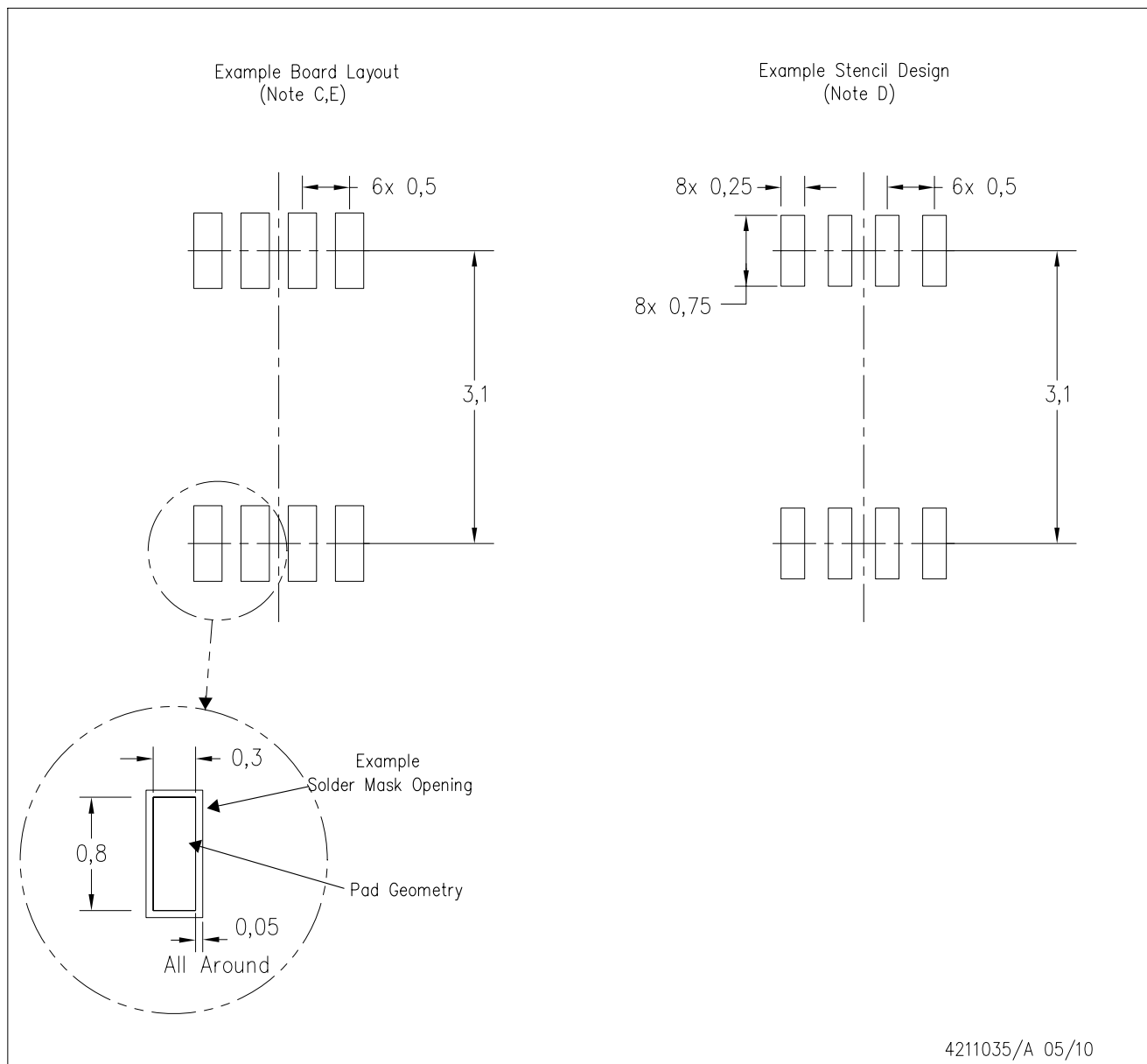
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion.
 - Falls within JEDEC MO-187 variation CA.

DDU (S-PDSO-G8)

PLASTIC SMALL OUTLINE PACKAGE (DIE UP)



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- $\triangle C$ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- $\triangle D$ Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AC.

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE

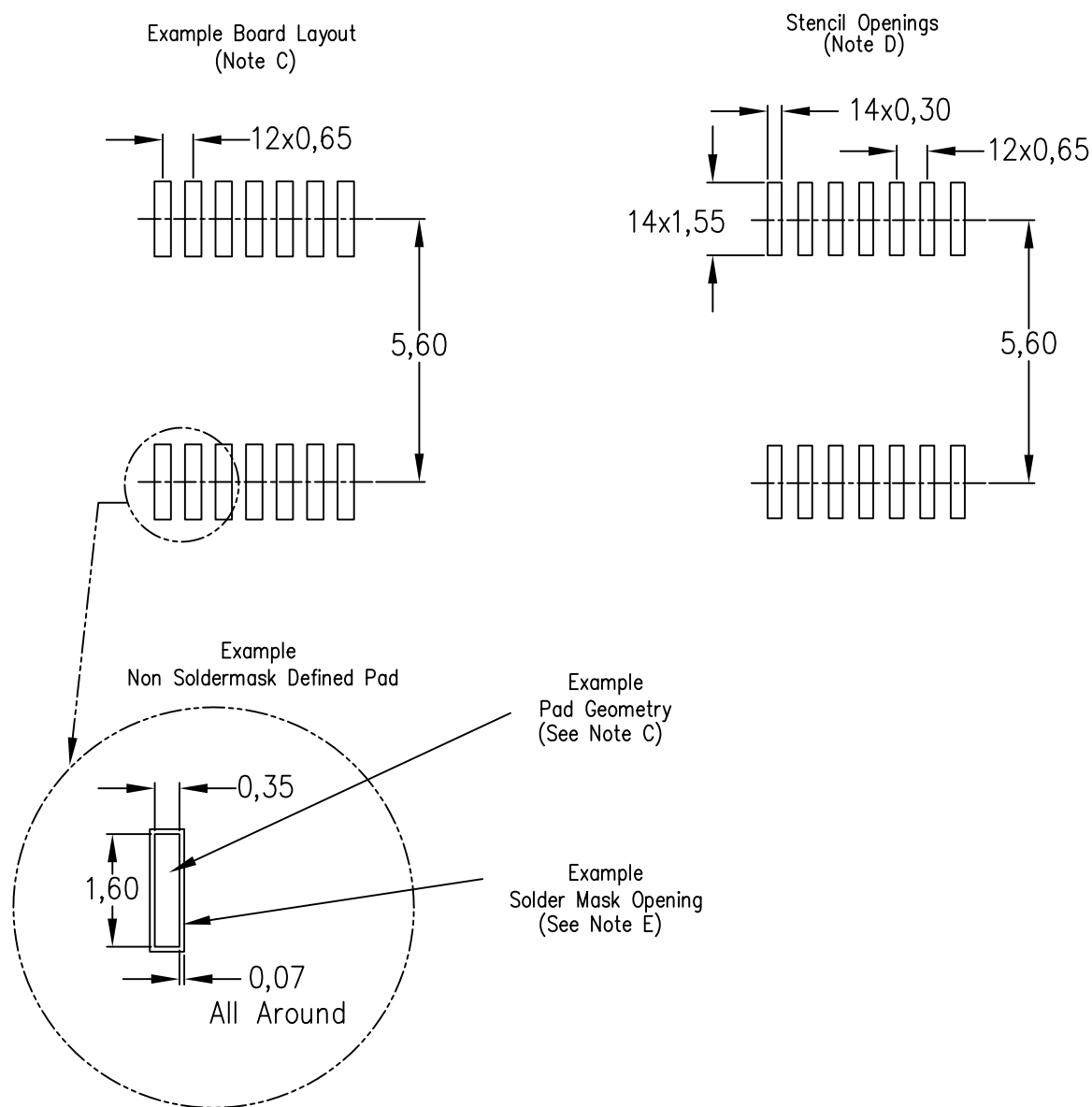


4040064-3/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4211284-2/F 12/12

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - Δ C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - Δ D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - $\triangle C$ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - $\triangle D$ Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G8)

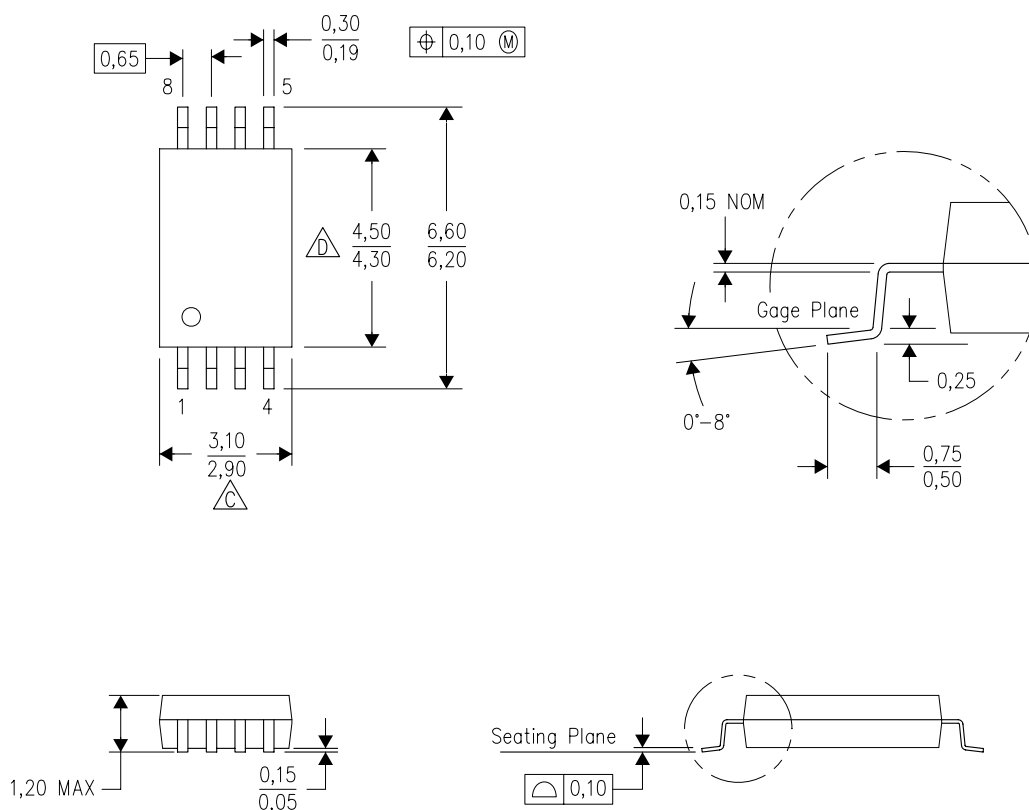
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G8)

PLASTIC SMALL OUTLINE



4040064-2/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products

| | |
|------------------------------|--|
| Audio | www.ti.com/audio |
| Amplifiers | amplifier.ti.com |
| Data Converters | dataconverter.ti.com |
| DLP® Products | www.dlp.com |
| DSP | dsp.ti.com |
| Clocks and Timers | www.ti.com/clocks |
| Interface | interface.ti.com |
| Logic | logic.ti.com |
| Power Mgmt | power.ti.com |
| Microcontrollers | microcontroller.ti.com |
| RFID | www.ti-rfid.com |
| OMAP Applications Processors | www.ti.com/omap |
| Wireless Connectivity | www.ti.com/wirelessconnectivity |

Applications

| | |
|-------------------------------|--|
| Automotive and Transportation | www.ti.com/automotive |
| Communications and Telecom | www.ti.com/communications |
| Computers and Peripherals | www.ti.com/computers |
| Consumer Electronics | www.ti.com/consumer-apps |
| Energy and Lighting | www.ti.com/energy |
| Industrial | www.ti.com/industrial |
| Medical | www.ti.com/medical |
| Security | www.ti.com/security |
| Space, Avionics and Defense | www.ti.com/space-avionics-defense |
| Video and Imaging | www.ti.com/video |

TI E2E Community

e2e.ti.com

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Texas Instruments:

[LMV324ID](#) [LMV321IDCKR](#) [LMV324SID](#) [LMV324IDR](#) [LMV358IDR](#) [LMV358IPWR](#) [LMV321IDBVT](#) [LMV321IDBVR](#)
[LMV324IPWR](#) [LMV358IDGKR](#) [LMV321IDBVTE4](#) [LMV321IDCKRG4](#) [LMV321IDCKT](#) [LMV324IPWRG4](#) [LMV324QD](#)
[LMV324QDR](#) [LMV324QPW](#) [LMV324QPWR](#) [LMV324SIDE4](#) [LMV324SIDR](#) [LMV324SIDRE4](#) [LMV324SIPWR](#)
[LMV324SIPWRE4](#) [LMV358ID](#) [LMV358IDDUR](#) [LMV358IDE4](#) [LMV358IDG4](#) [LMV358IDGKRG4](#) [LMV358IDRE4](#)
[LMV358IDRG4](#) [LMV358IPW](#) [LMV358IPWG4](#) [LMV358IPWRE4](#) [LMV358IPWRG4](#) [LMV358QD](#) [LMV358QDDUR](#)
[LMV358QDGKR](#) [LMV358QDGKRG4](#) [LMV358QDR](#) [LMV358QPWR](#) [LMV358IDDURG4](#) [LMV358QDDURG4](#)
[LMV321IDCKTG4](#) [LMV324IDG4](#) [LMV324IDRG4](#) [LMV324QDG4](#) [LMV324QDRG4](#) [LMV324QPWG4](#) [LMV324SIDG4](#)
[LMV324SIDRG4](#) [LMV324SIPWRG4](#) [LMV358QDG4](#) [LMV321IDBVRG4](#) [LMV321IDBVTG4](#)