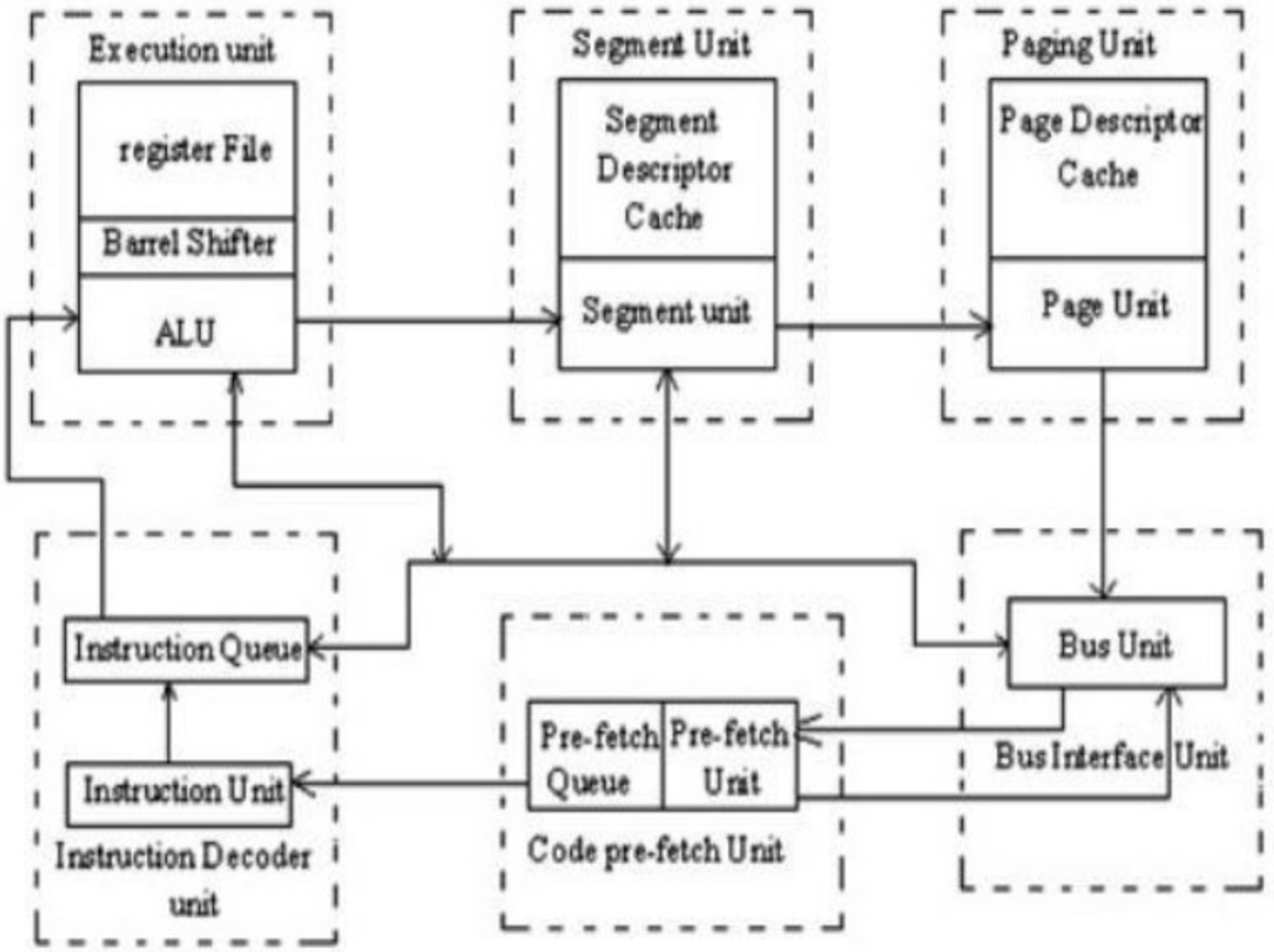
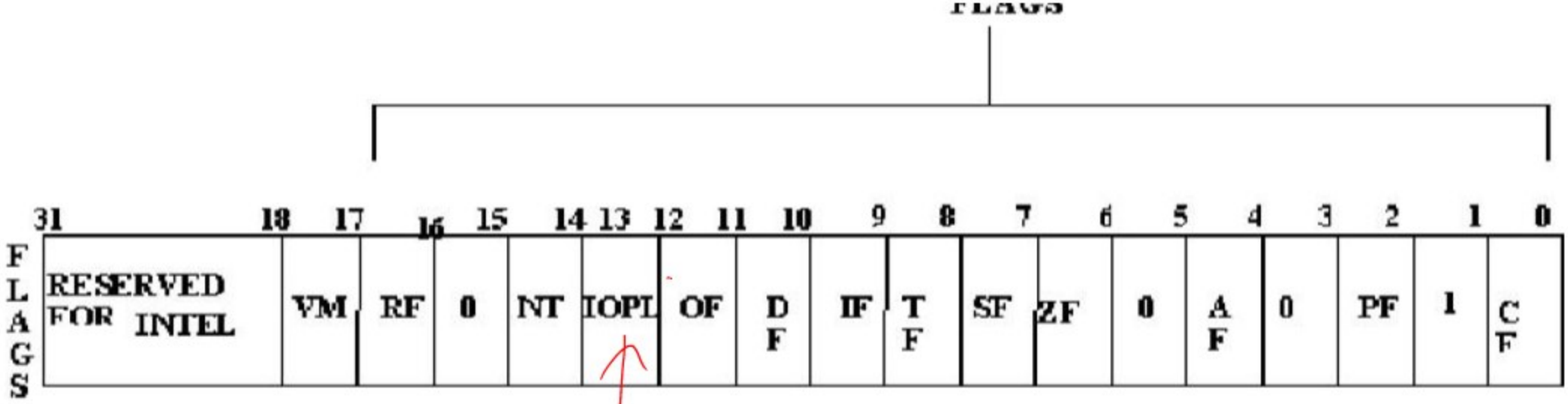
CSC405 MICROPROCESSORS

80386 GPR ,CONTROL REGISTERS AND MODES

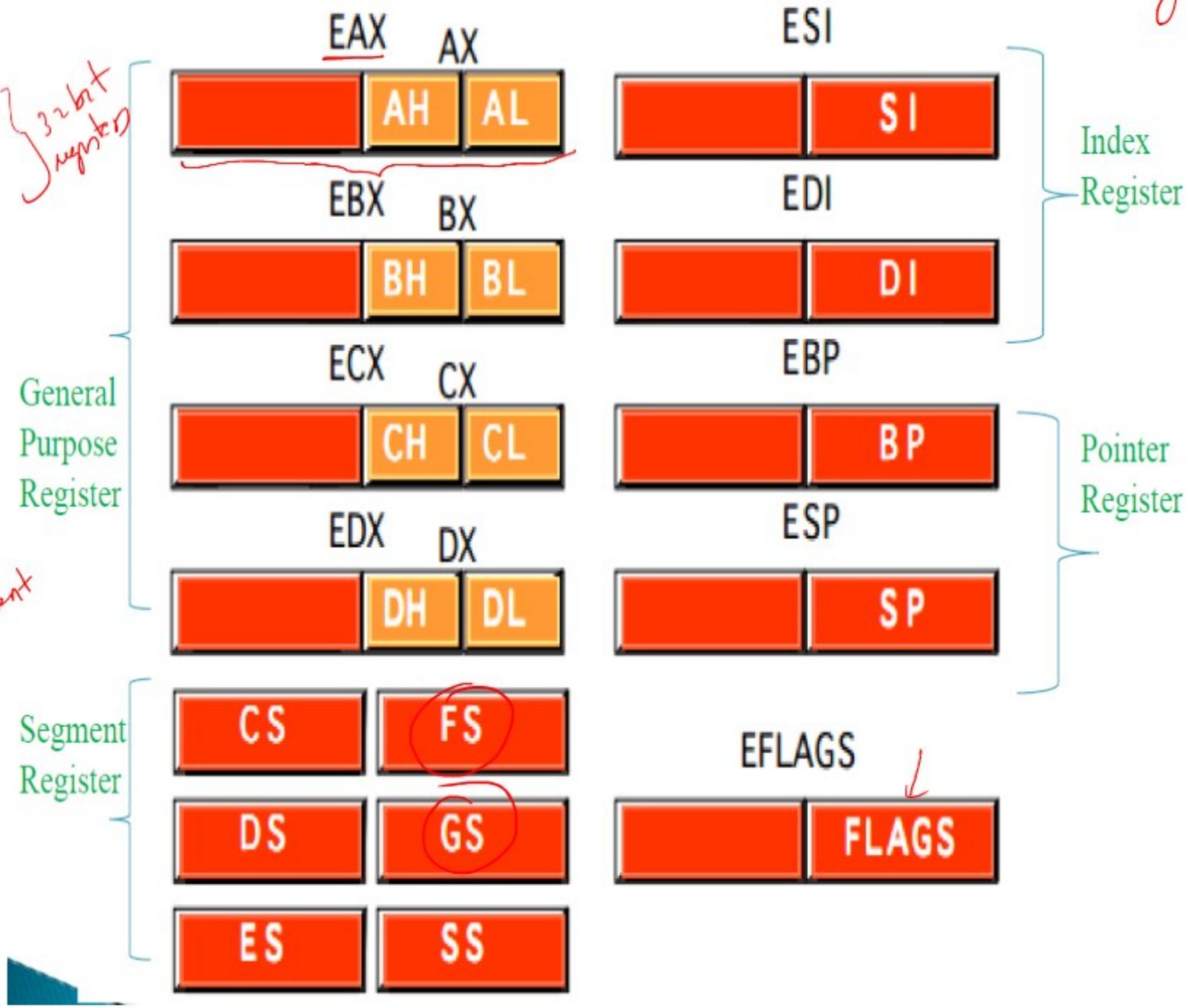
OBJECTIVE

1. (i)To understand 80386 General Purpose Registers and Control Registers.
   (ii)To understand real mode, protected mode and virtual mode in 80386.


Execution unit
register File
Barrel Shifter
ALU
Segment Unit
Segment Descriptor Cache
Segment unit
Paging Unit
Page Descriptor Cache
Page Unit
Instruction Queue
Instruction Unit
Instruction Decoder unit
Pre-fetch Queue
Pre-fetch Unit
Code pre-fetch Unit
Bus Unit
Bus Interface Unit



FLAG REGISTER OF 80386


EAX
AX
AH
AL
EBX
BX
BH
BL
ECX
CX
CH
CL
EDX
DX
DH
DL
ESI
SI
EDI
DI
EBP
BP
ESP
SP
CS
FS
DS
GS
ES
SS
EFLAGS
FLAGS
General Purpose Register
Segment Register
Index Register
Pointer Register

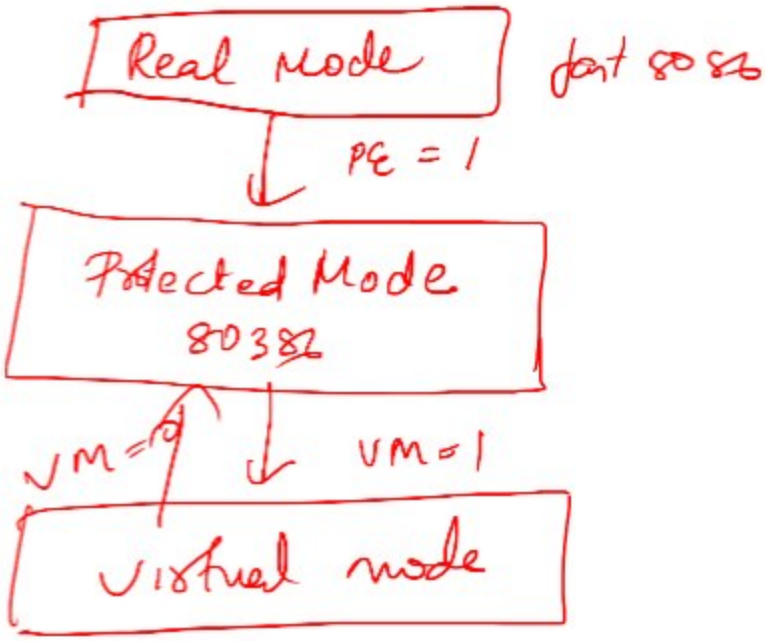
Operating Modes

1. Real mode
2. Protected mode ←
3. Virtual mode

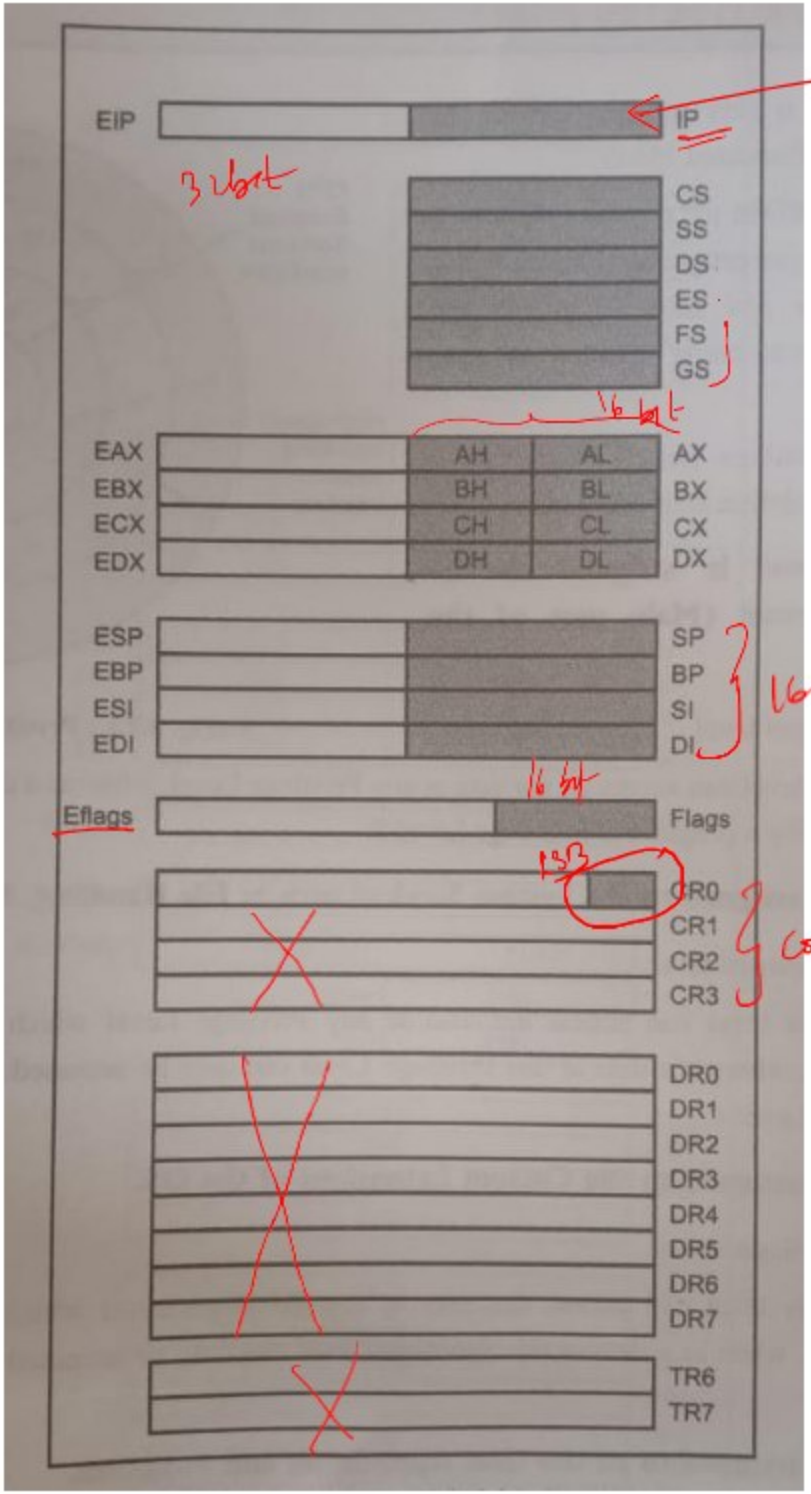
Real mode → start '8086'

environment for protected mode

PE = 1



Real Mode	Protected Mode
16 bit operations	32 bit operations
16 bit gen. purpose registers 8 bit offset flag	32 bit Extended GPR ⋮ 32 bit EFLAG register
Only 8086 flags (16 bit)	Complex segmentation & paging
PA = Seg × 10 + offset	32 bit offset: 4GB
16 bit offset → 64KB	
No control registers	Control registers.



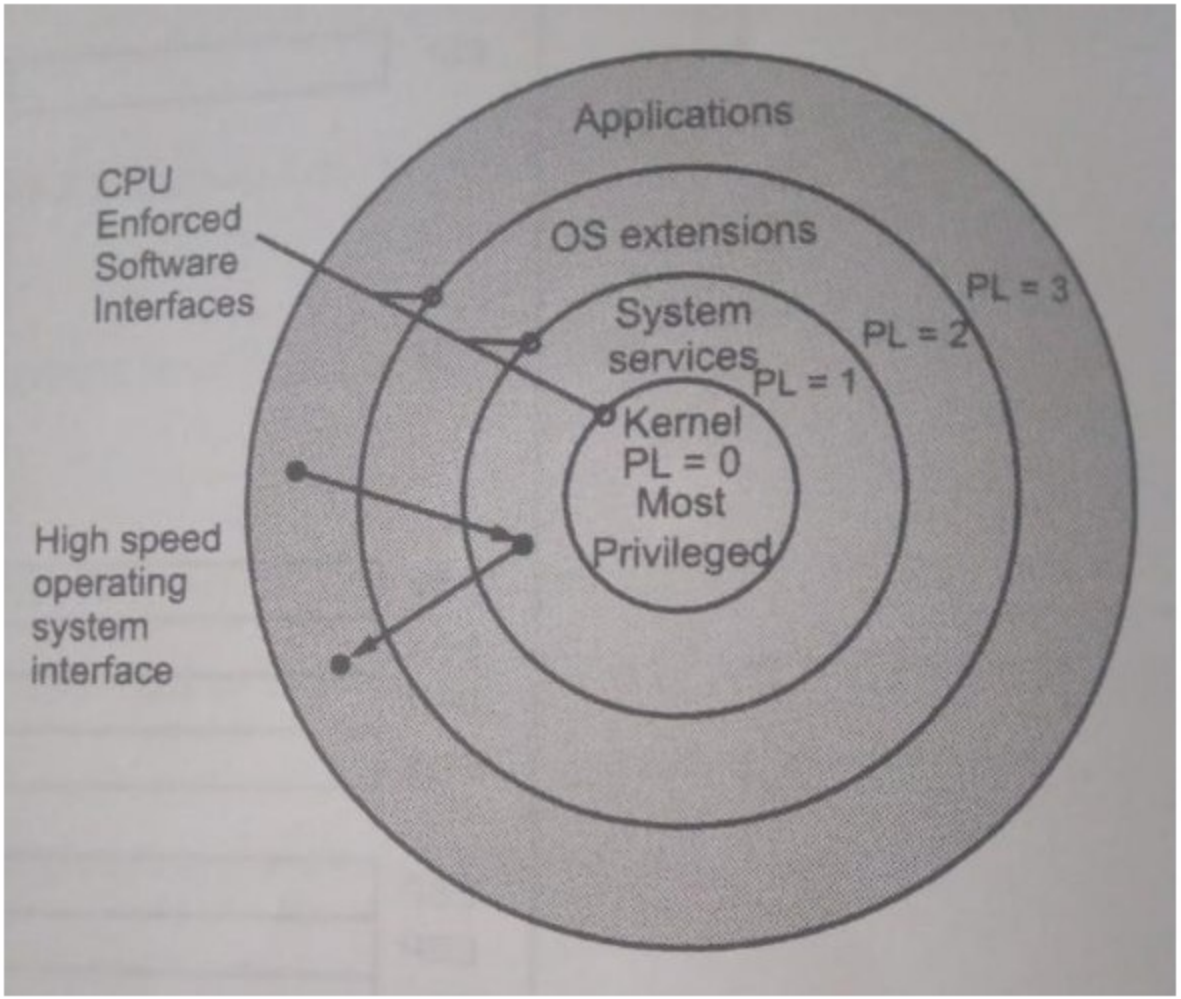
80386 reg model

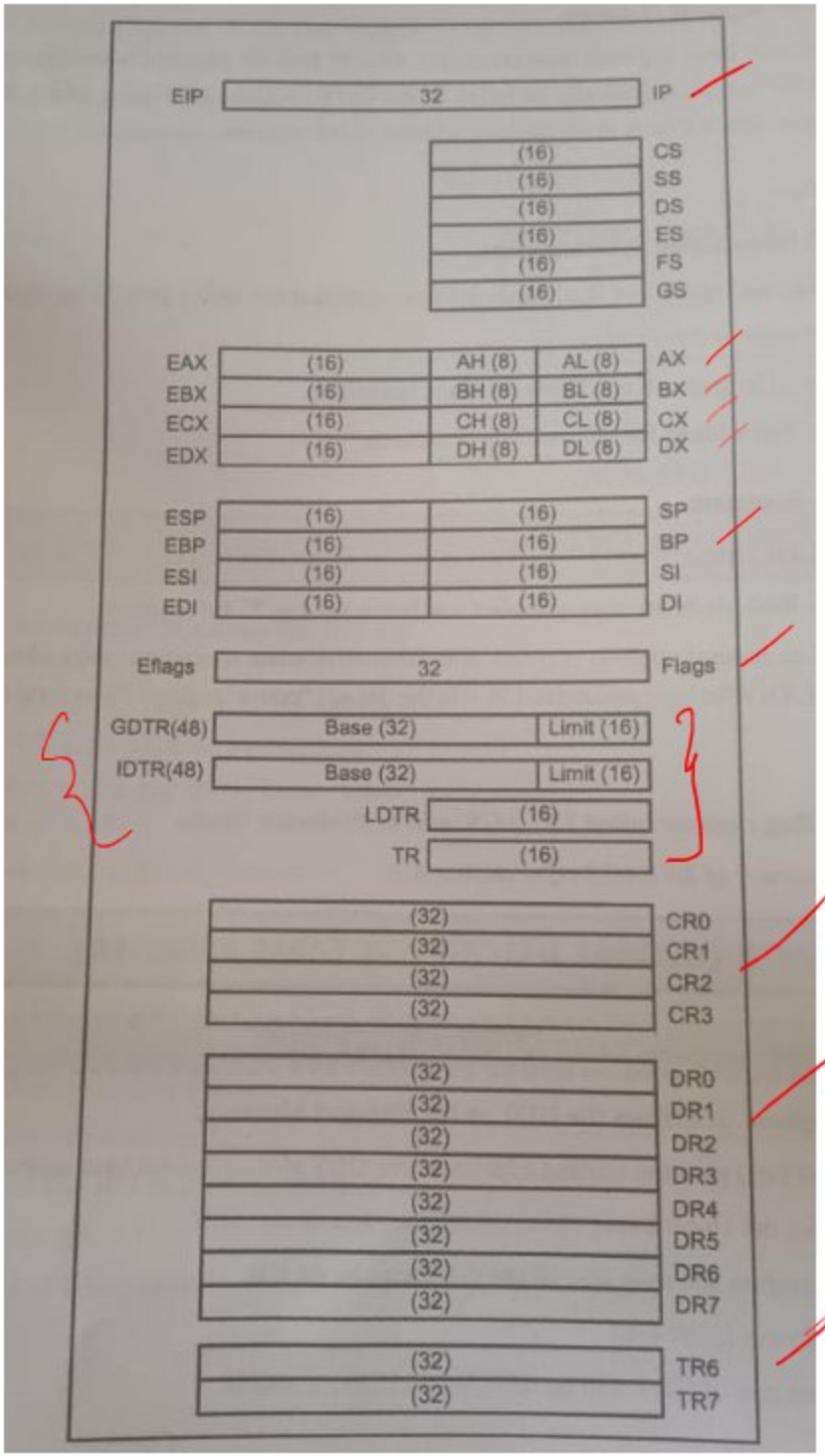
Software Mode / Register Model

Real Mode

8086

Protected Mode





4 tables in 80386

Descriptor

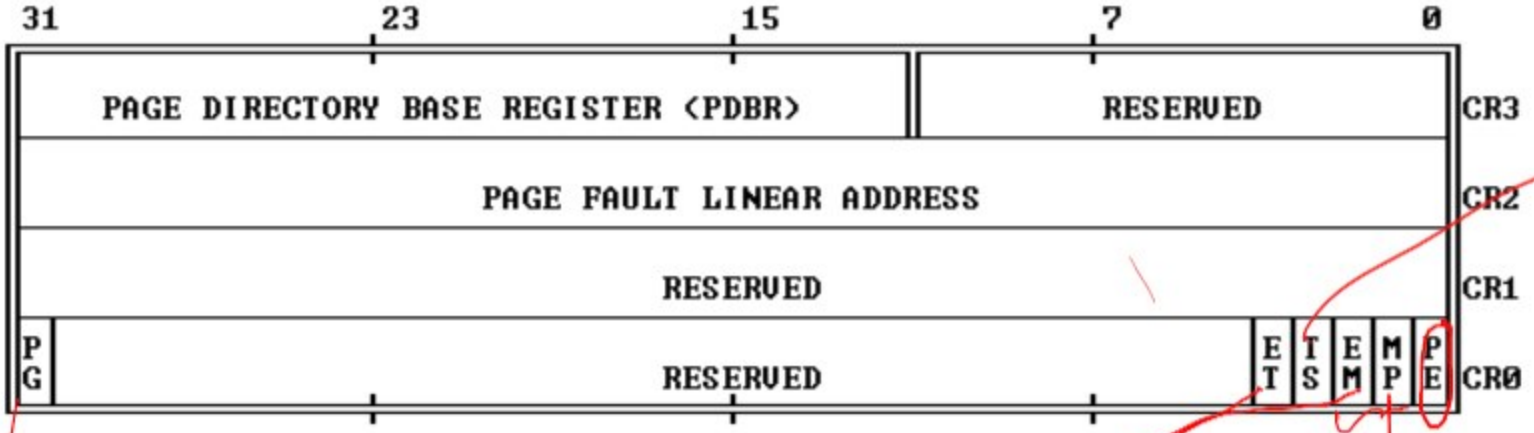
1. Global table
2. Local Descriptor table
3. Interrupt Descriptor table
4. Task Segment Descriptor table

→ GPR's
→ Flag Register
→ Control Registers

Control Register

LSB of CR0

TS = 1 ⇒ Allows
0 ⇒ NO switching



multitasking
↓
Task switching

80386
80387
ET = 1 → 80387
ET = 0 → 80386, 80287

Extension type
MP = 1

Emulate coprocessor
EM = 1 / 80386

Math coprocessor
1 = yes
0 = no coprocessor

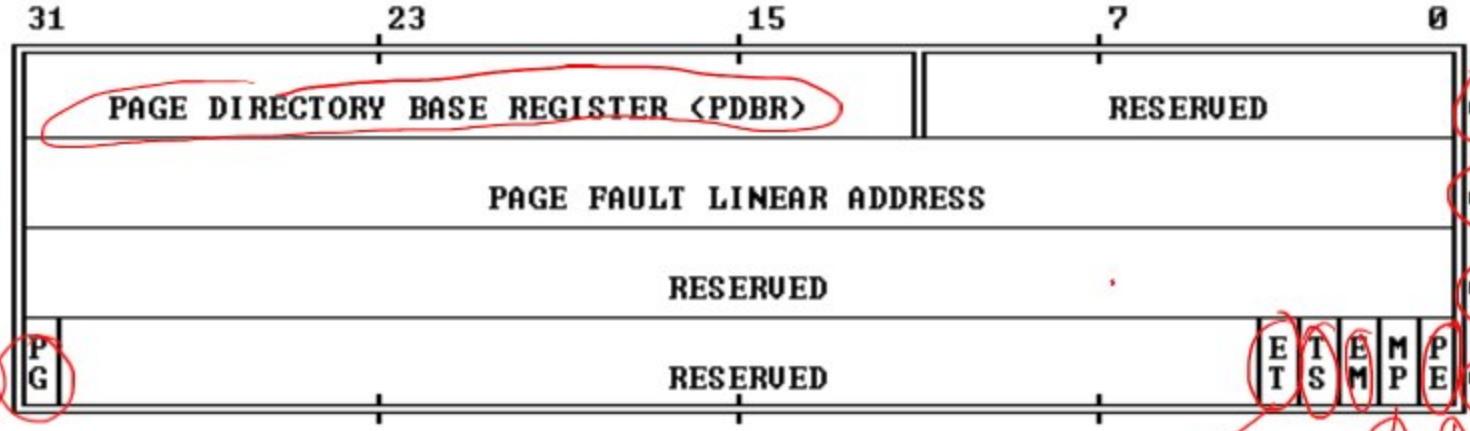
Control Registers

Virtual address → physical address

1) segmentation – linear address
2) paging – physical address

80287
80387

page fault



paging

Initially
Load page table
Page directory

64 TB

ET=1 80387
ET=0 80287

TS=1
TS=0

EM=1

MP=1 =1 ⇒ protected mode
=0 =0
↓
80386

Thank you