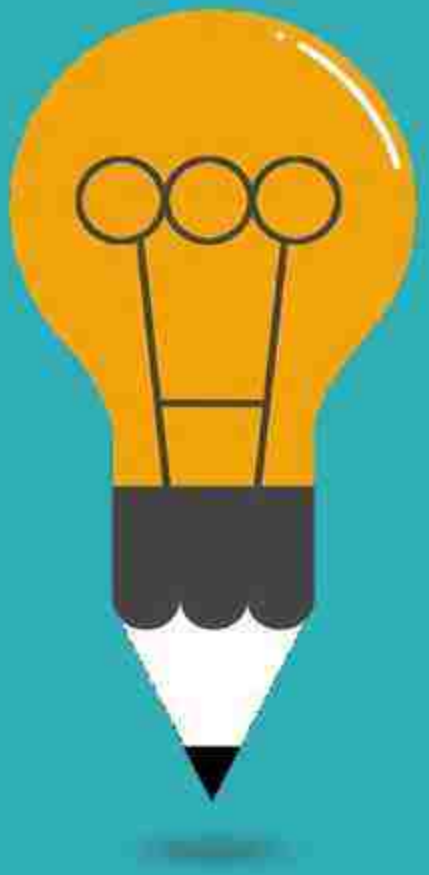


CSC405 MICROPROCESSORS

8086 IN MAXIMUM MODE

PROF.POONAM M. PANGARKAR,
ASSISTANT PROFESSOR ,
CSE DATASCIENCE ,APST TI:ANE

OBJECTIVE

1. To understand the functioning of 8086 in maximum mode.
2. To understand the timing diagrams for Read and Write operations in maximum mode.
3. To understand the functional pin diagram of 8086.

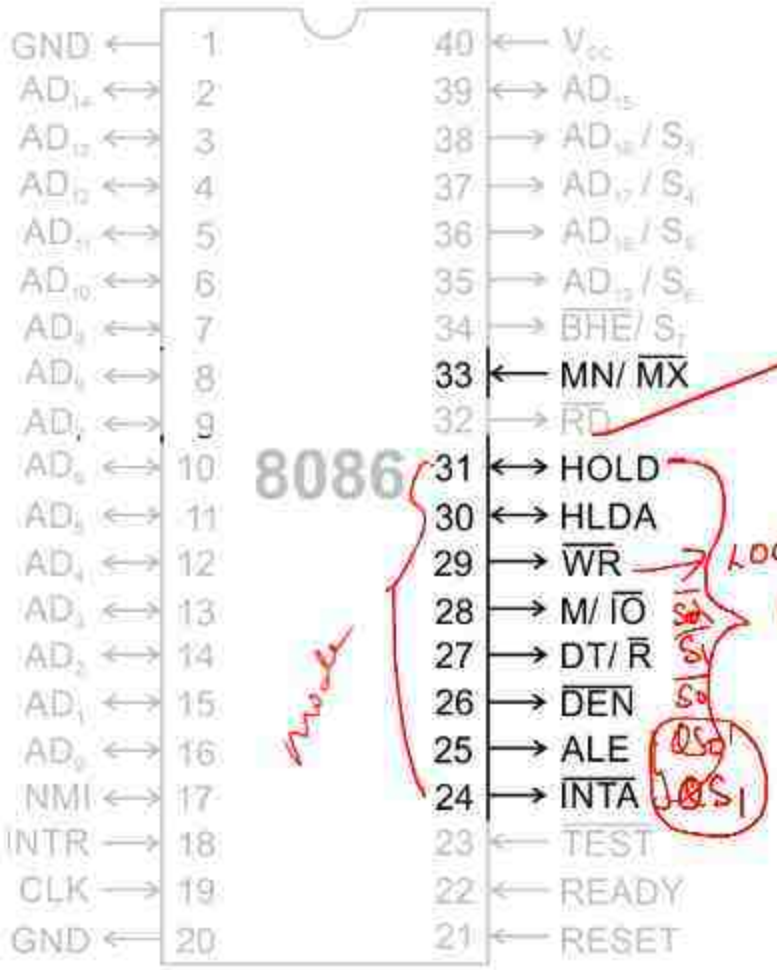
01 Difference in Control signal generation in maximum mode

02 Functioning in Maximum Mode

03 Timing diagrams for Read and Write operations in maximum mode

Min/ Max Pins

The 8086 microprocessor can work in two modes of operations : Minimum mode and Maximum mode.

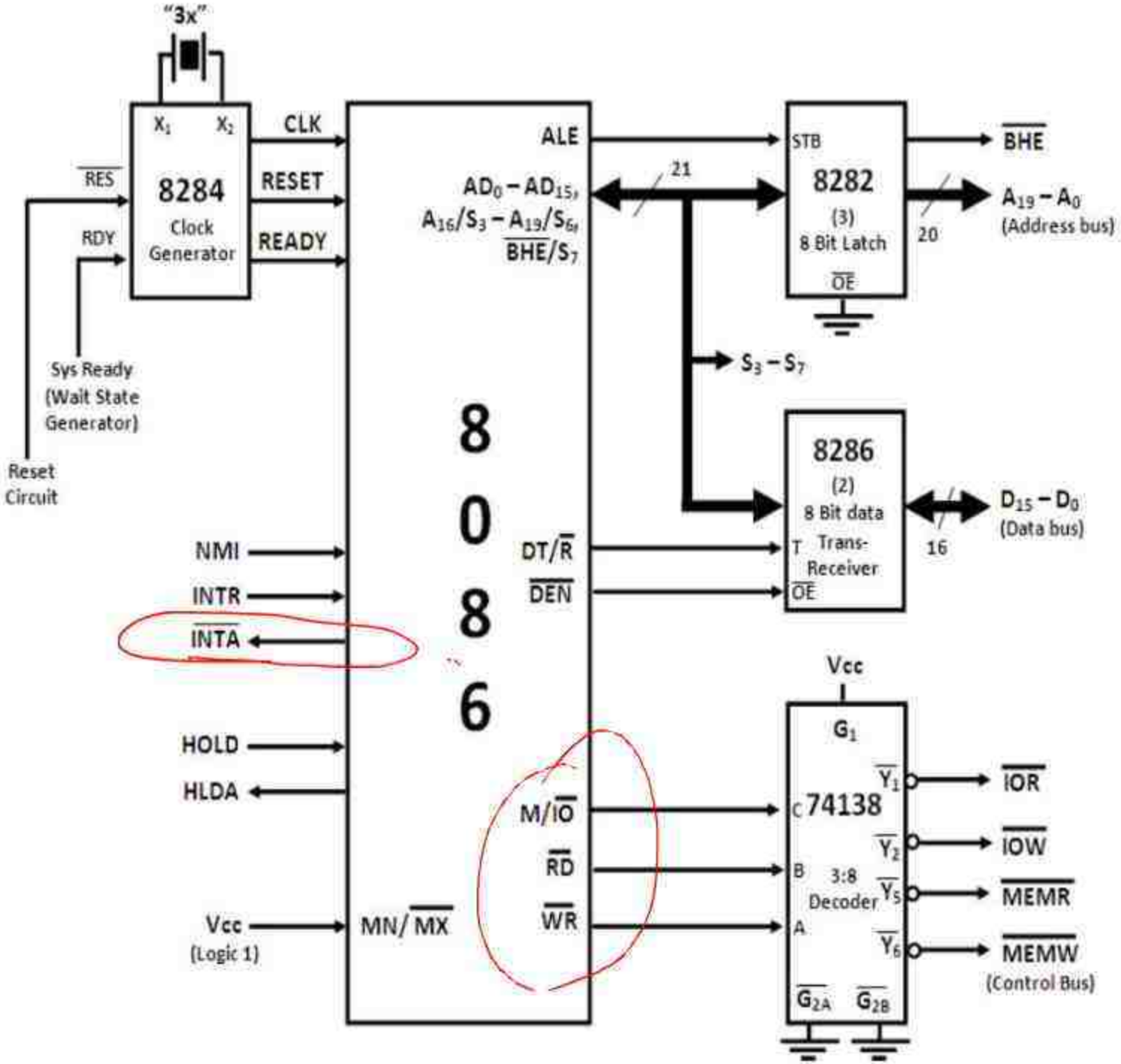


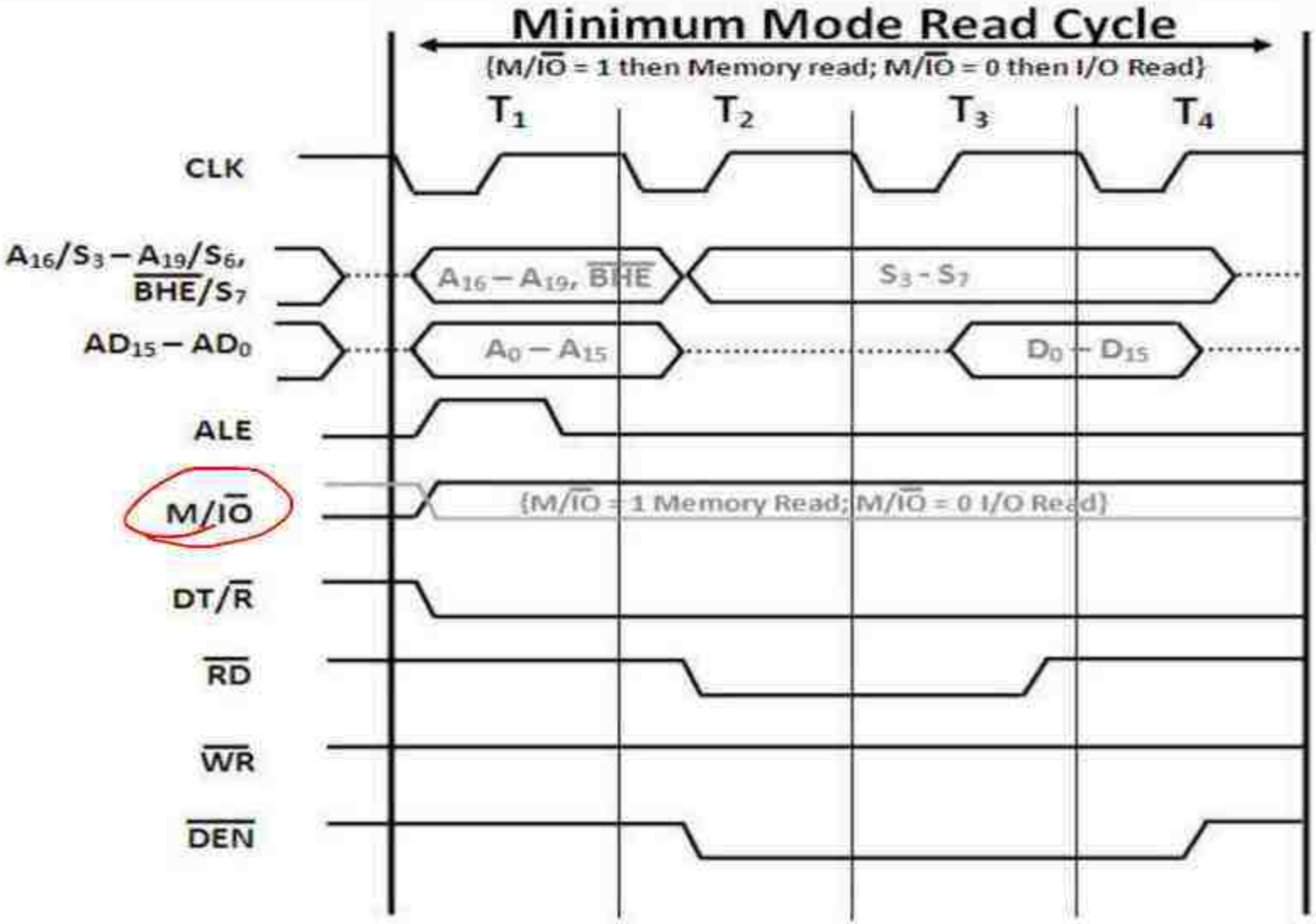
In the minimum mode of operation the microprocessor do not associate with any co-processors and can not be used for multiprocessor systems.

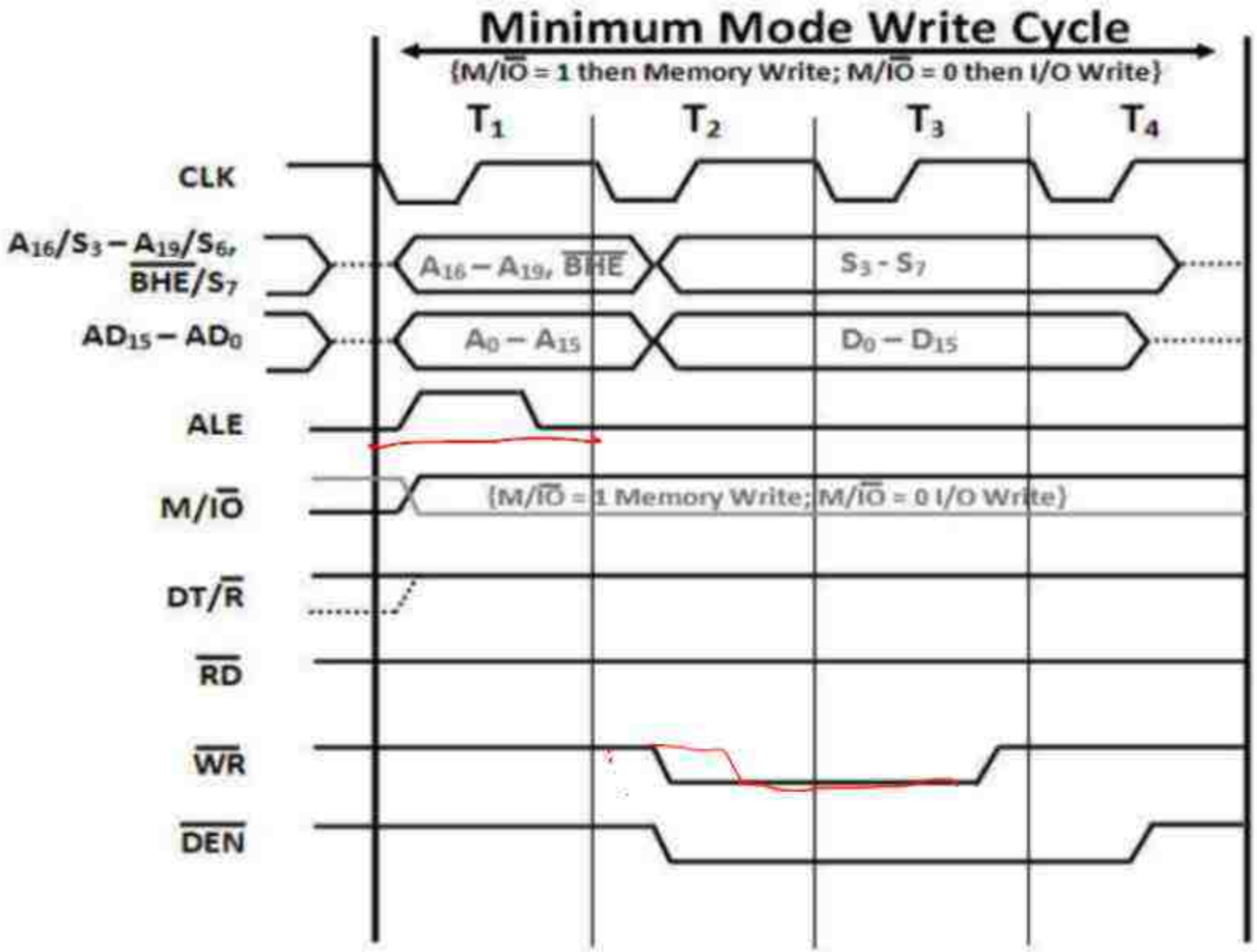
In the maximum mode the 8086 can work in multi-processor or co-processor configuration.

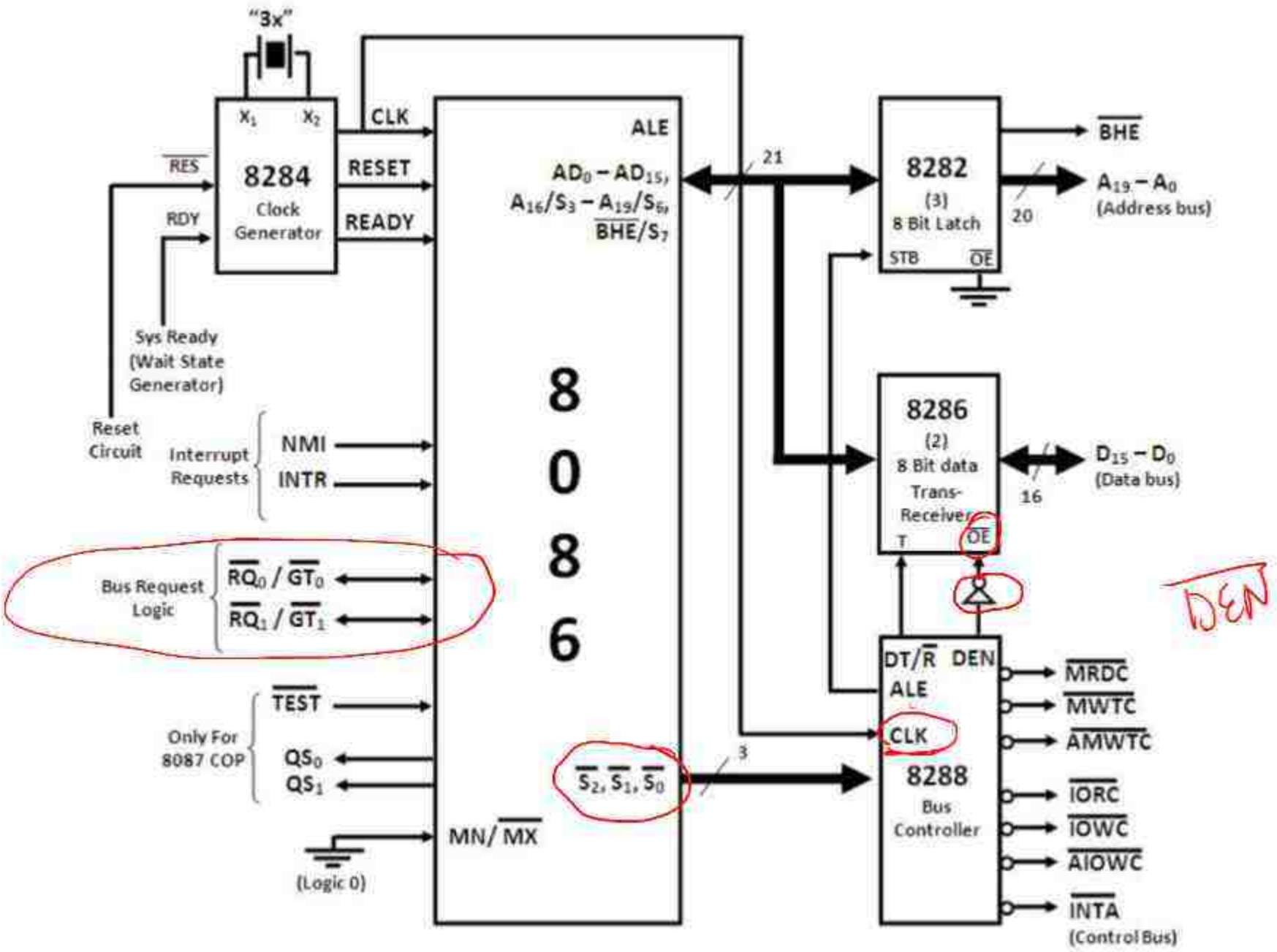
Minimum or maximum mode operations are decided by the pin MN/ MX(Active low).

When this pin is high 8086 operates in minimum mode otherwise it operates in Maximum mode.


"3x"
X1
X2
8284
Clock
Generator
CLK
RESET
READY
RES
RDY
Sys Ready
(Wait State
Generator)
Reset
Circuit
8
0
8
6
ALE
AD0 – AD15,
A16/S3 – A19/S6,
BHE/S7
DT/R
DEN
NMI
INTR
INTA
HOLD
HLDA
Vcc
(Logic 1)
MN/MX
M/IO
RD
WR
21
STB
8282
(3)
8 Bit Latch
OE
BHE
A19 – A0
(Address bus)
20
S3 – S7
8286
(2)
8 Bit data
T Trans-
Receiver
OE
D15 – D0
(Data bus)
16
Vcc
G1
C 74138
B 3:8
Decoder
A
Y1
Y2
Y5
Y6
G2A
G2B
IOR
IOW
MEMR
MEMW
(Control Bus)

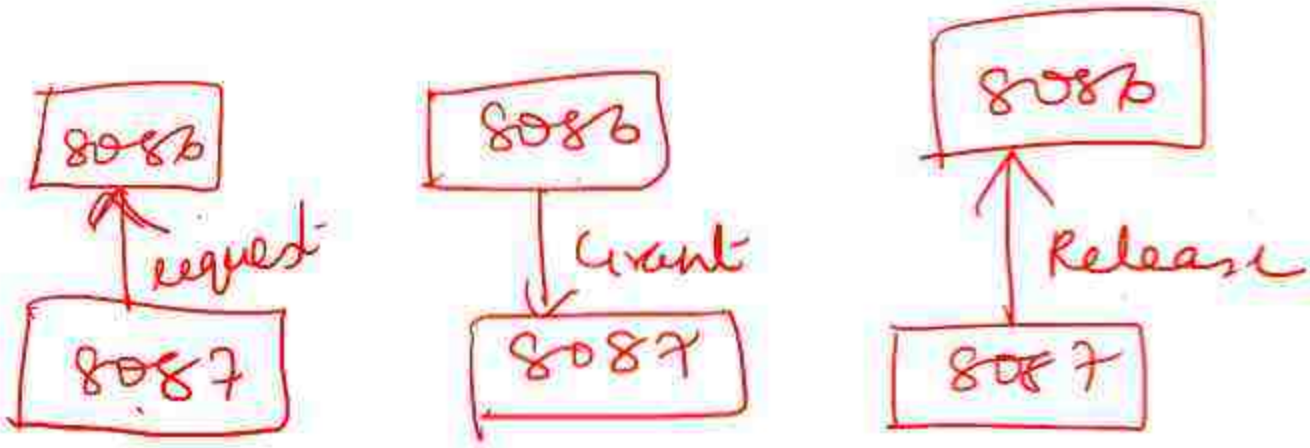

Minimum Mode Read Cycle
{M/IO = 1 then Memory read; M/IO = 0 then I/O Read}
T1
T2
T3
T4
CLK
A16/S3 – A19/S6, BHE/S7
AD15 – AD0
ALE
M/IO
DT/R
RD
WR
DEN
A16 – A19, BHE
S3 - S7
A0 – A15
D0 – D15
{M/IO = 1 Memory Read; M/IO = 0 I/O Read}


Minimum Mode Write Cycle
{M/IO = 1 then Memory Write; M/IO = 0 then I/O Write}
T1
T2
T3
T4
CLK
A16/S3 – A19/S6, BHE/S7
AD15 – AD0
ALE
M/IO
DT/R
RD
WR
DEN
A16 – A19, BHE
S3 - S7
A0 – A15
D0 – D15
{M/IO = 1 Memory Write; M/IO = 0 I/O Write}

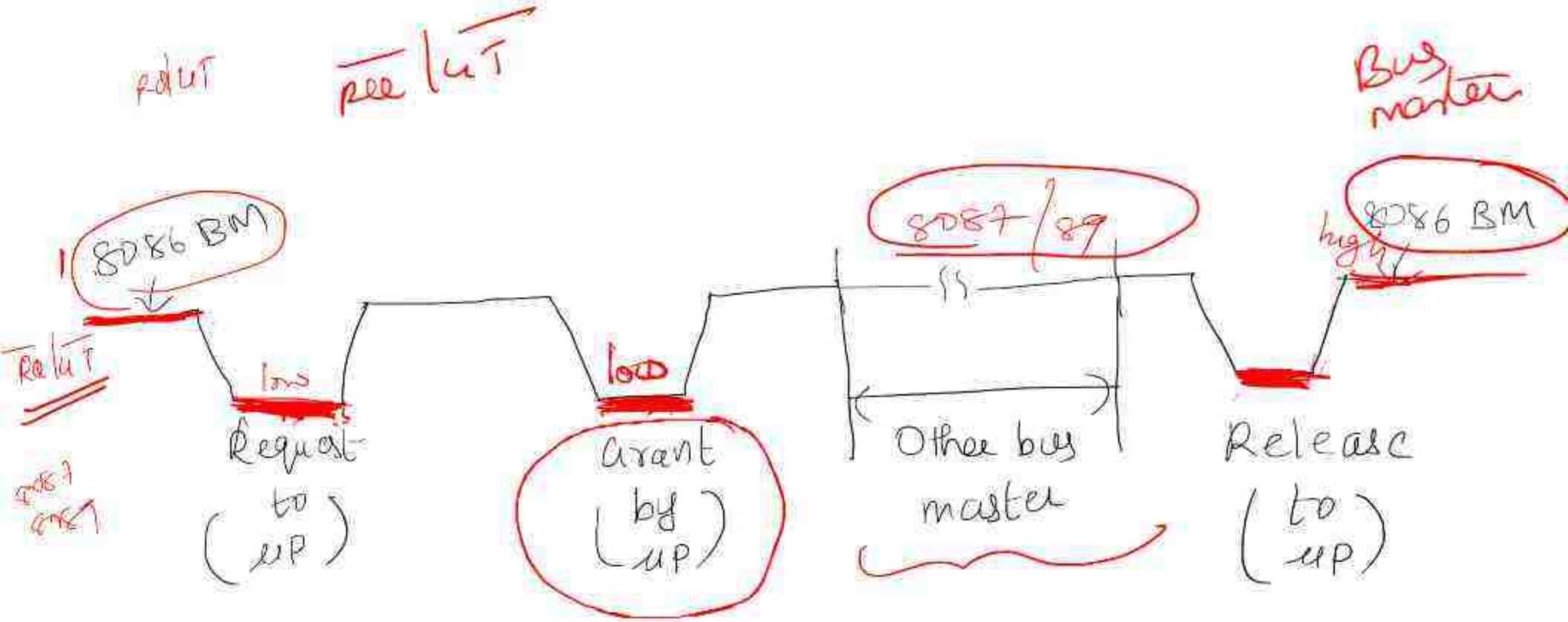

"3x"
X1
X2
8284
Clock
Generator
RES
RDY
CLK
RESET
READY
Sys Ready
(Wait State
Generator)
Reset
Circuit
Interrupt
Requests
NMI
INTR
Bus Request
Logic
RQ0 / GT0
RQ1 / GT1
Only For
8087 COP
TEST
QS0
QS1
(Logic 0)
MN/ MX
8
0
8
6
ALE
AD0 – AD15,
A16/S3 – A19/S6,
BHE/S7
S2, S1, S0
3
21
8282
(3)
8 Bit Latch
STB
OE
20
BHE
A19 – A0
(Address bus)
8286
(2)
8 Bit data
Trans-
Receiver
T
OE
16
D15 – D0
(Data bus)
DEN
DT/R
DEN
ALE
CLK
8288
Bus
Controller
MRDC
MWTC
AMWTC
IORC
IOWC
AIOWC
INTA
(Control Bus)

$\overline{RQ_0}/\overline{GT_0}$ → bidirectional

Request Grant pins



$\overline{RQ_1}/\overline{GT_1}$ - bidirectional


8086 BM
Request
(to up)
Grant
(by up)
Other bus master
Release
(to up)
8086 BM
Bus master

LOCK

Instruction cycle
Machine cycle
T states

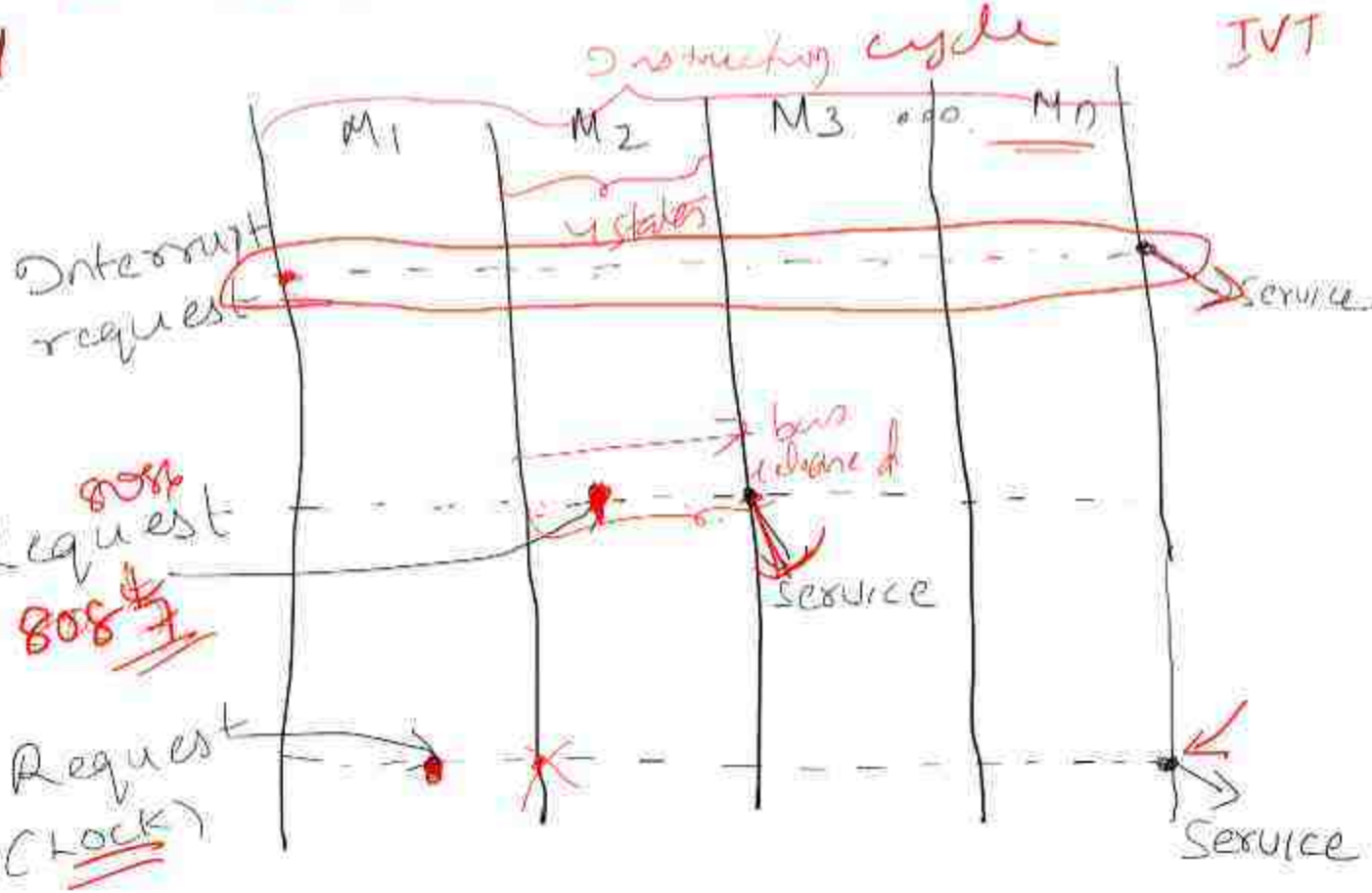
ISR

IVT

µP can be interrupted

Interrupt Request

Bus Request



MOV CX, [2000H] → Bus Request

808?

LOCK MOV CX, [2000H]

Bus Request (LOCK)

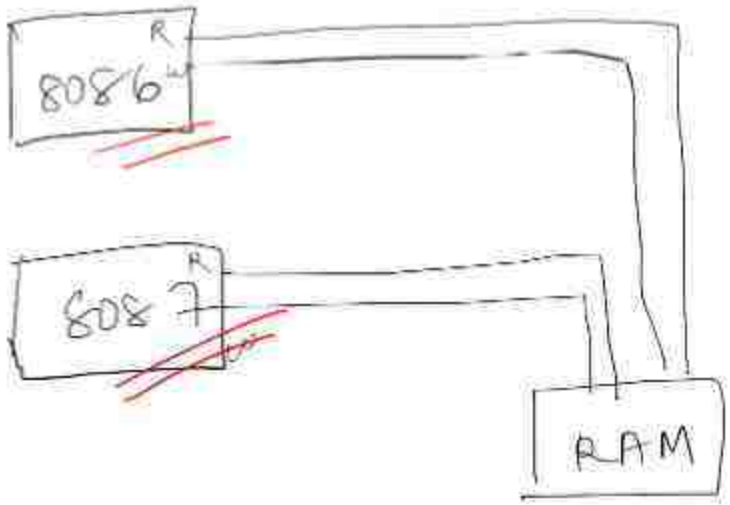
$\overline{S_2}$ $\overline{S_1}$ $\overline{S_0}$ → Status Inputs

8089

8086

8087

maximum mode



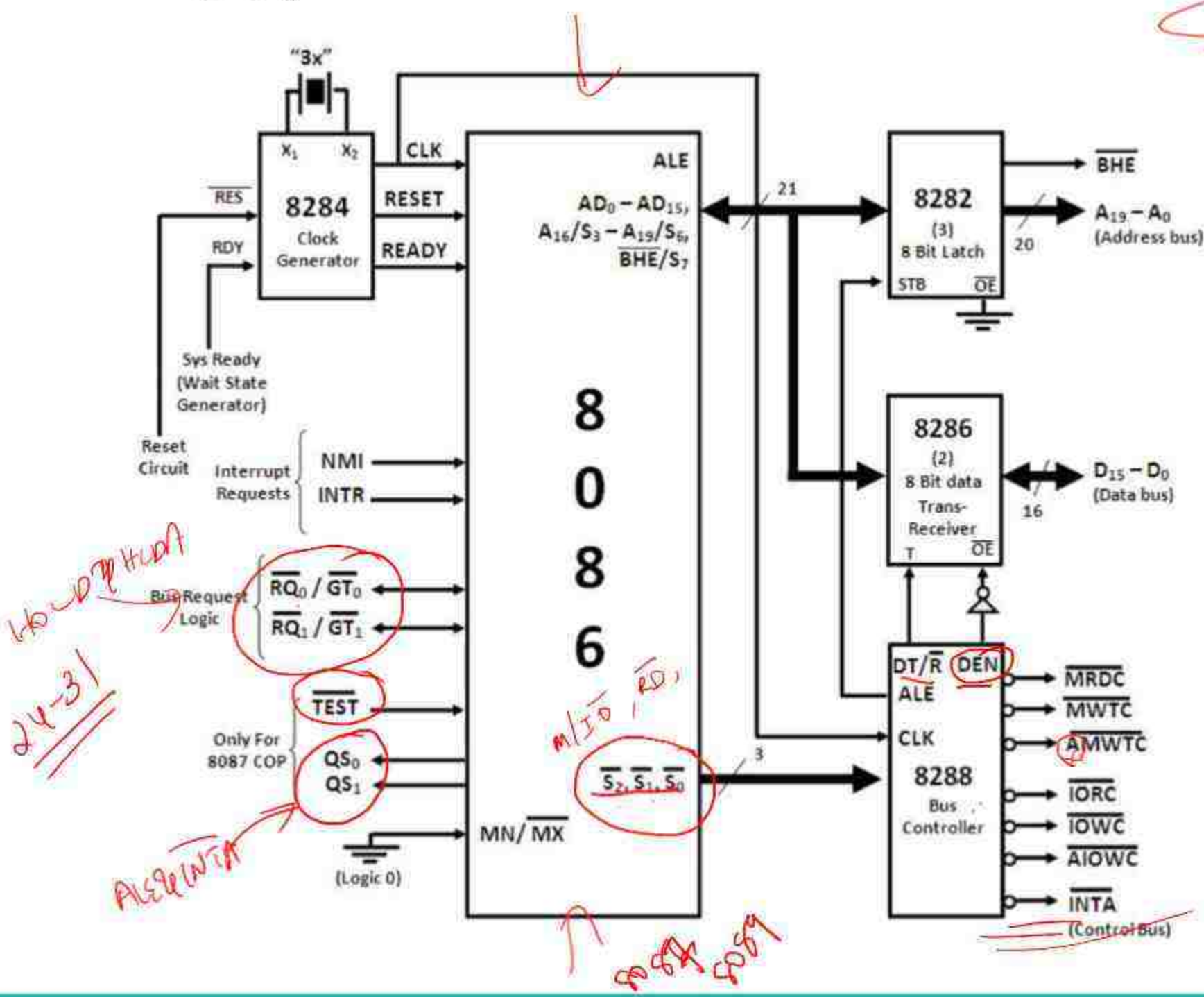
bus

bus master

Status Inputs			CPU Cycles	8288 Command
$\overline{S_2}$	$\overline{S_1}$	$\overline{S_0}$		
0	0	0	Interrupt Acknowledge	$\overline{INTA}$
0	0	1	Read I/O Port	$\overline{IORC}$
0	1	0	Write I/O Port	$\overline{IOWC}$, $\overline{AIOWC}$
0	1	1	Halt	None
1	0	0	Instruction Fetch	$\overline{MRDC}$
1	0	1	Read Memory	$\overline{MRDC}$
1	1	0	Write Memory	$\overline{MWTC}$, $\overline{AMWC}$
1	1	1	Passive	None

QS_1	QS_0	Queue Status
0 (low)	0	No Operation. During the last clock cycle, nothing was taken from the queue.
0	1	First Byte. The byte taken from the queue was the first byte of the instruction.
1 (high)	0	Queue Empty. The queue has been reinitialized as a result of the execution of a transfer instruction.
1	1	Subsequent Byte. The byte taken from the queue was a subsequent byte of the instruction.

8086 in maximum mode



Minimum Mode

1) MN/$\overline{MX}$ = 1

2) ALE given by 8086 MP

3) DT/$\overline{R}$ and $\overline{DEN}$ given by 8086

4) Control signals are generated by 8086 and decoded by 74138.

5) $\overline{INTA}$ given by 8086

6) 24-31 → HOLD / HLDA — DMA allowed

7) 3:8 decoder does not require clk

Maximum Mode

MN/$\overline{MX}$ = 0

ALE given by 8288

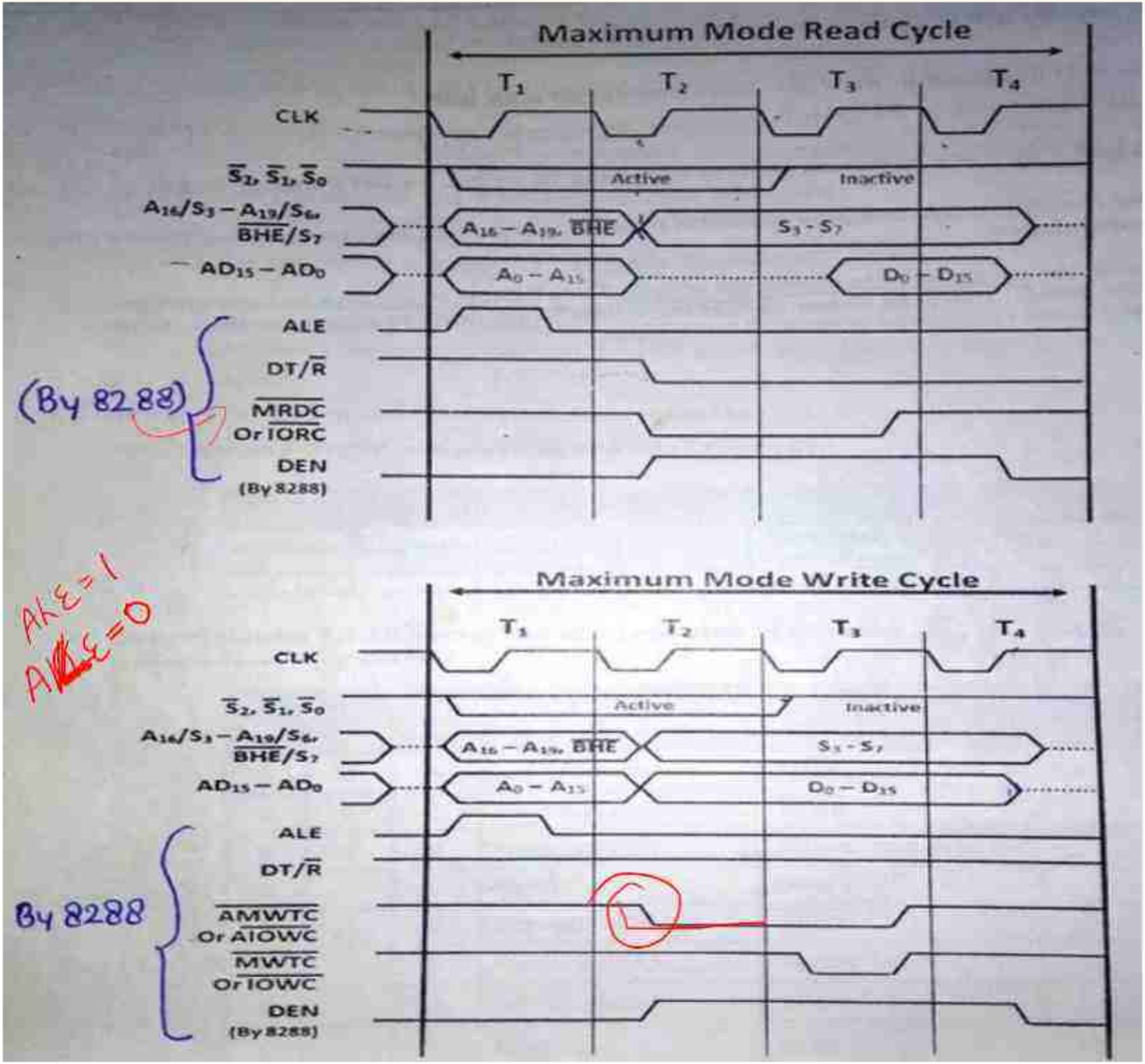
DT/$\overline{R}$ and DEN given by 8288

Control signals are generated by 8288 depending upon status signals

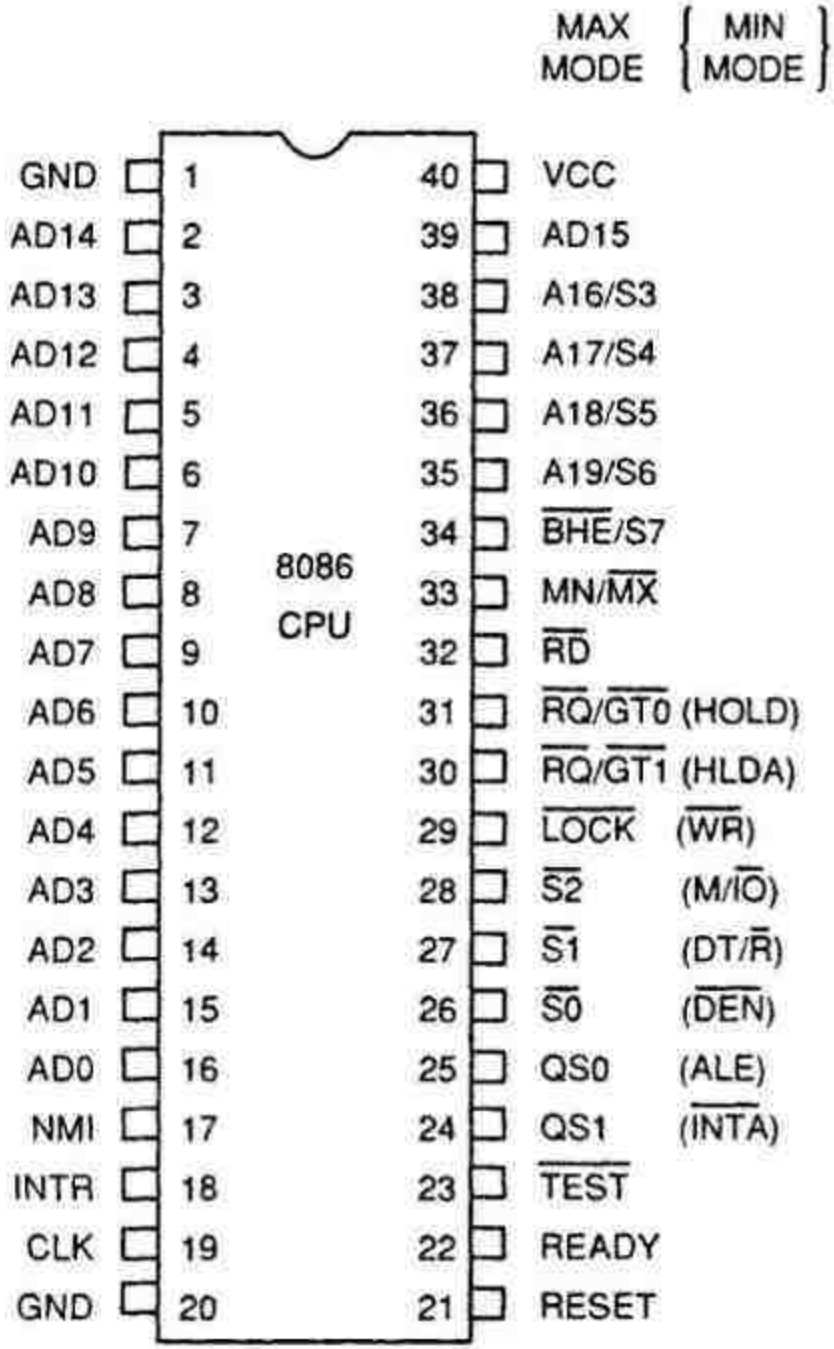
$\overline{INTA}$ given by 8288

$\overline{RQ}/\overline{GT_0}$ & $\overline{RQ}/\overline{GT_1}$ — bus request DMA

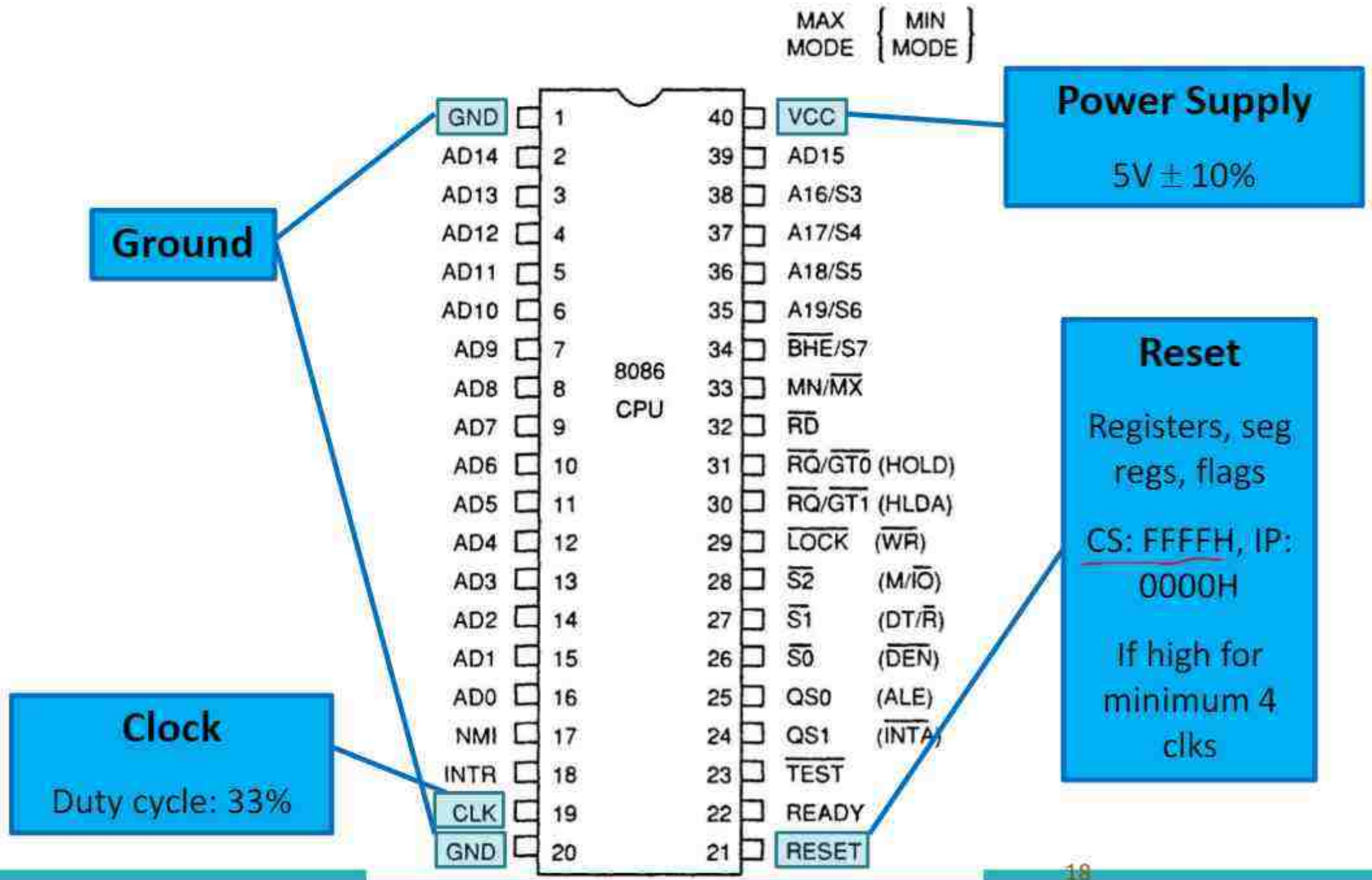
8288 needs CLK seperate

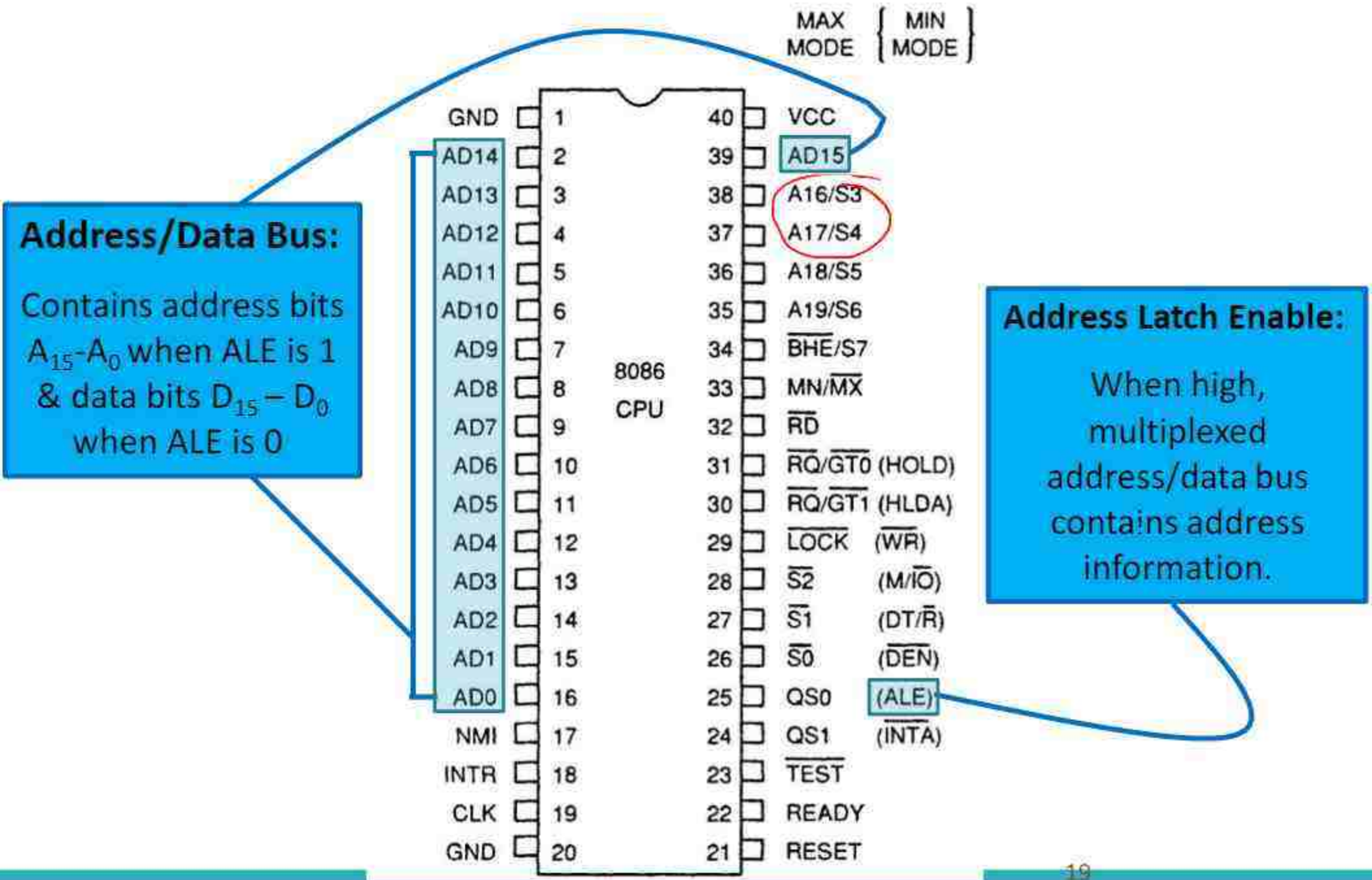

Maximum Mode Read Cycle
T1
T2
T3
T4
CLK
S2, S1, S0
Active
Inactive
A16/S3 – A19/S6, BHE/S7
A16 – A19, BHE
S3 - S7
AD15 – AD0
A0 – A15
D0 – D15
ALE
DT/R
MRDC Or IORC
DEN (By 8288)
(By 8288)
AKE=1
AKE=0
Maximum Mode Write Cycle
T1
T2
T3
T4
CLK
S2, S1, S0
Active
Inactive
A16/S3 – A19/S6, BHE/S7
A16 – A19, BHE
S3 - S7
AD15 – AD0
A0 – A15
D0 – D15
ALE
DT/R
AMWTC Or AIOWC
MWTC Or IOWC
DEN (By 8288)
By 8288

INTEL 8086 - Pin Diagram

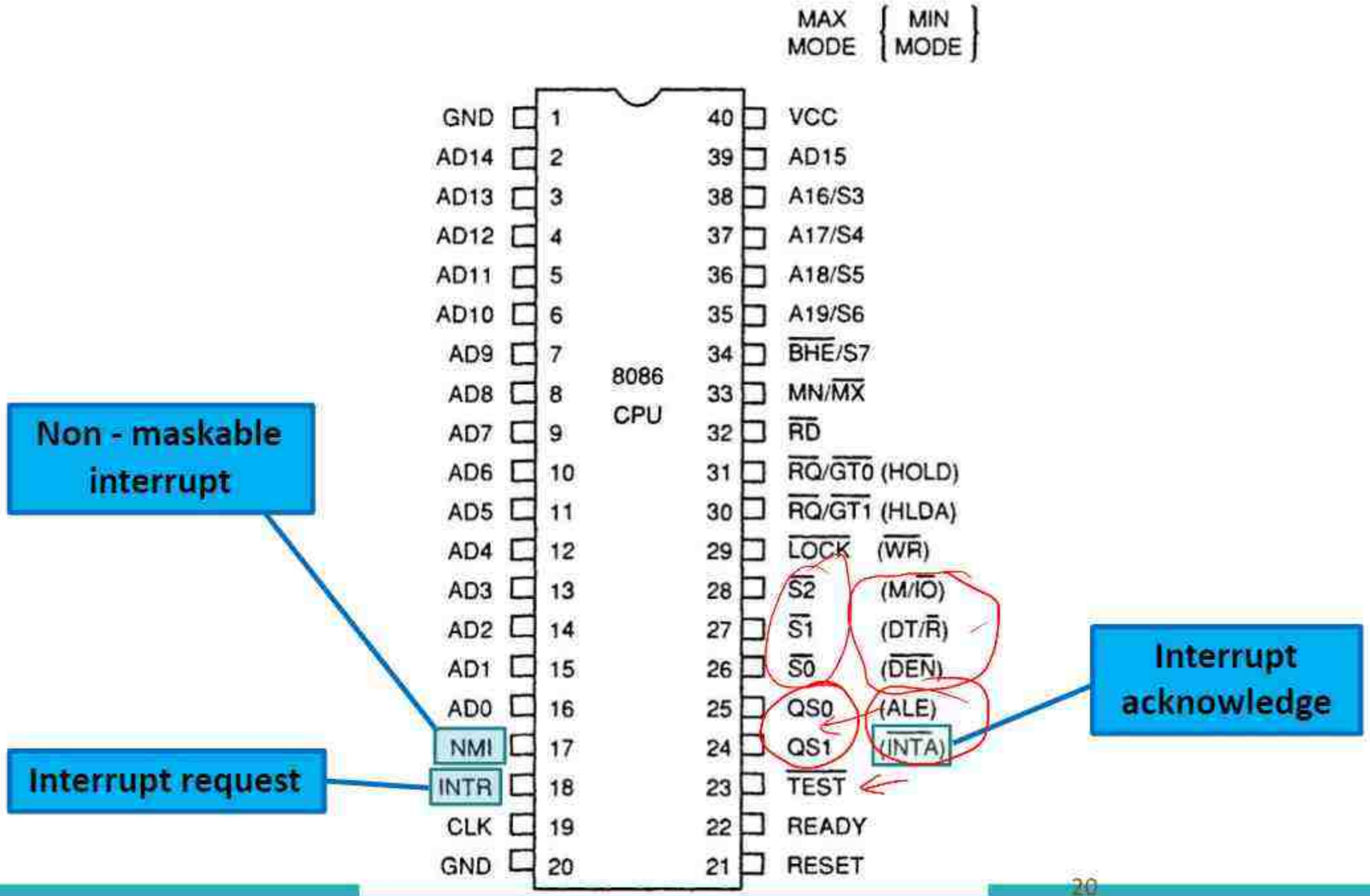


INTEL 8086 - Pin Details

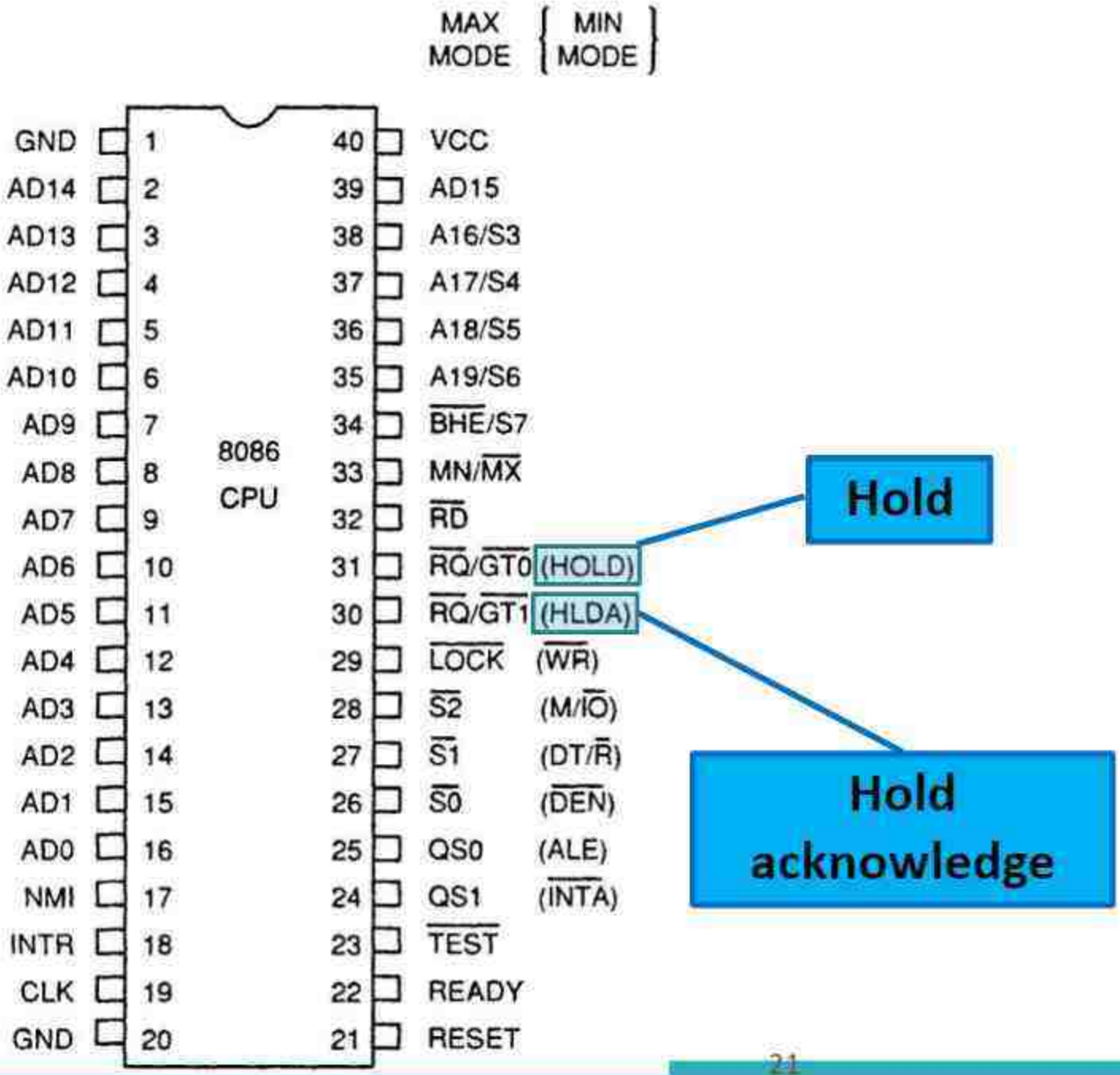



MAX MODE
MIN MODE
GND 1
AD14 2
AD13 3
AD12 4
AD11 5
AD10 6
AD9 7
AD8 8
AD7 9
AD6 10
AD5 11
AD4 12
AD3 13
AD2 14
AD1 15
AD0 16
NMI 17
INTR 18
CLK 19
GND 20
8086 CPU
40 VCC
39 AD15
38 A16/S3
37 A17/S4
36 A18/S5
35 A19/S6
34 BHE/S7
33 MN/MX
32 RD
31 RQ/GT0 (HOLD)
30 RQ/GT1 (HLDA)
29 LOCK (WR)
28 S2 (M/IO)
27 S1 (DT/R)
26 S0 (DEN)
25 QS0 (ALE)
24 QS1 (INTA)
23 TEST
22 READY
21 RESET
Address/Data Bus:
Contains address bits A15-A0 when ALE is 1 & data bits D15 – D0 when ALE is 0
Address Latch Enable:
When high, multiplexed address/data bus contains address information.

INTEL 8086 - Pin Details



INTEL 8086 - Pin Details

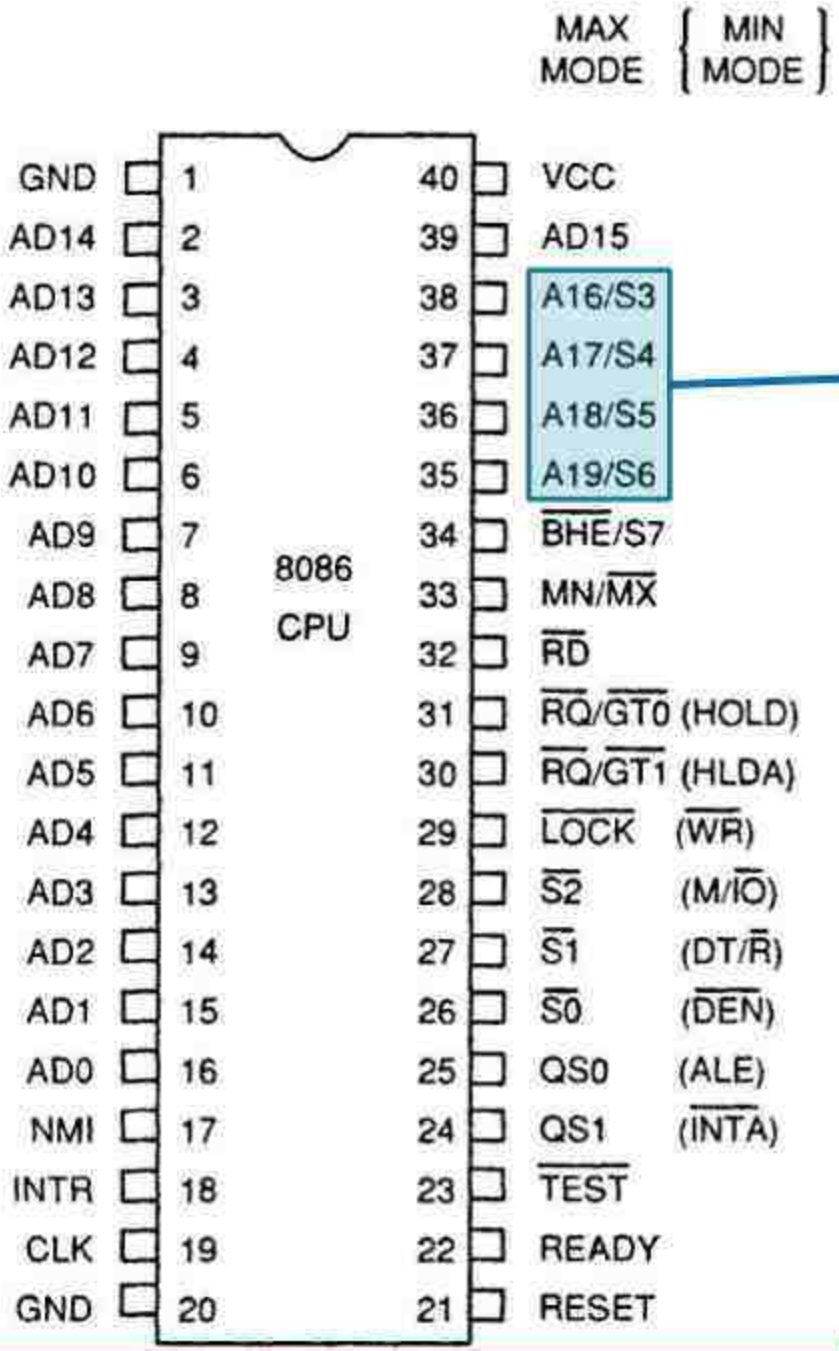


S6: Logic 0.

S5: Indicates condition of IF flag bits.

S4-S3: Indicate which segment is accessed during current bus cycle:

S4	S3	Function
0	0	Extra segment
0	1	Stack segment
1	0	Code or no segment
1	1	Data segment



Address/Status Bus

Address bits A_{19} – A_{16} & Status bits S_6 – S_3

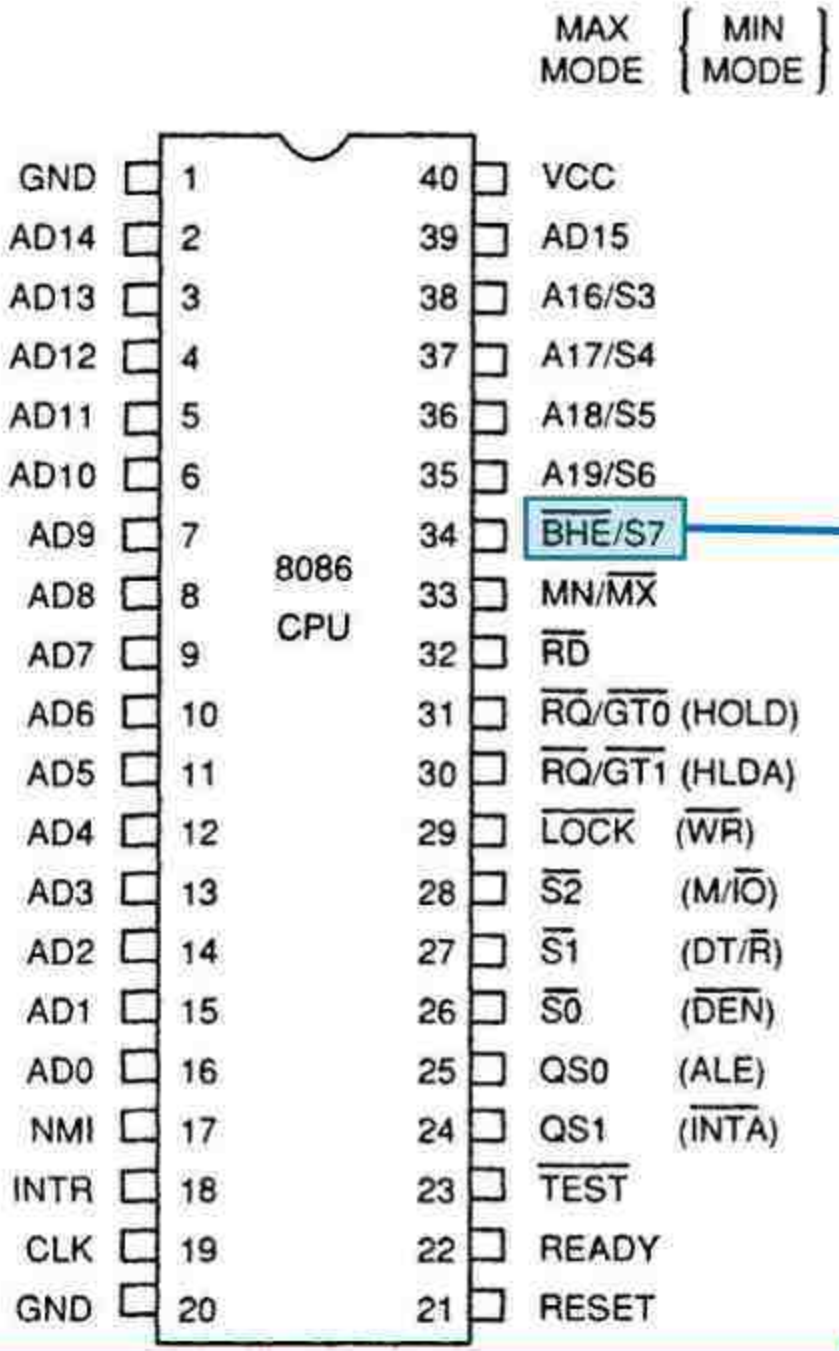
BHE#, A_0:

0,0: Whole word (16-bits)

0,1: High byte to/from odd address

1,0: Low byte to/from even address

1,1: No selection

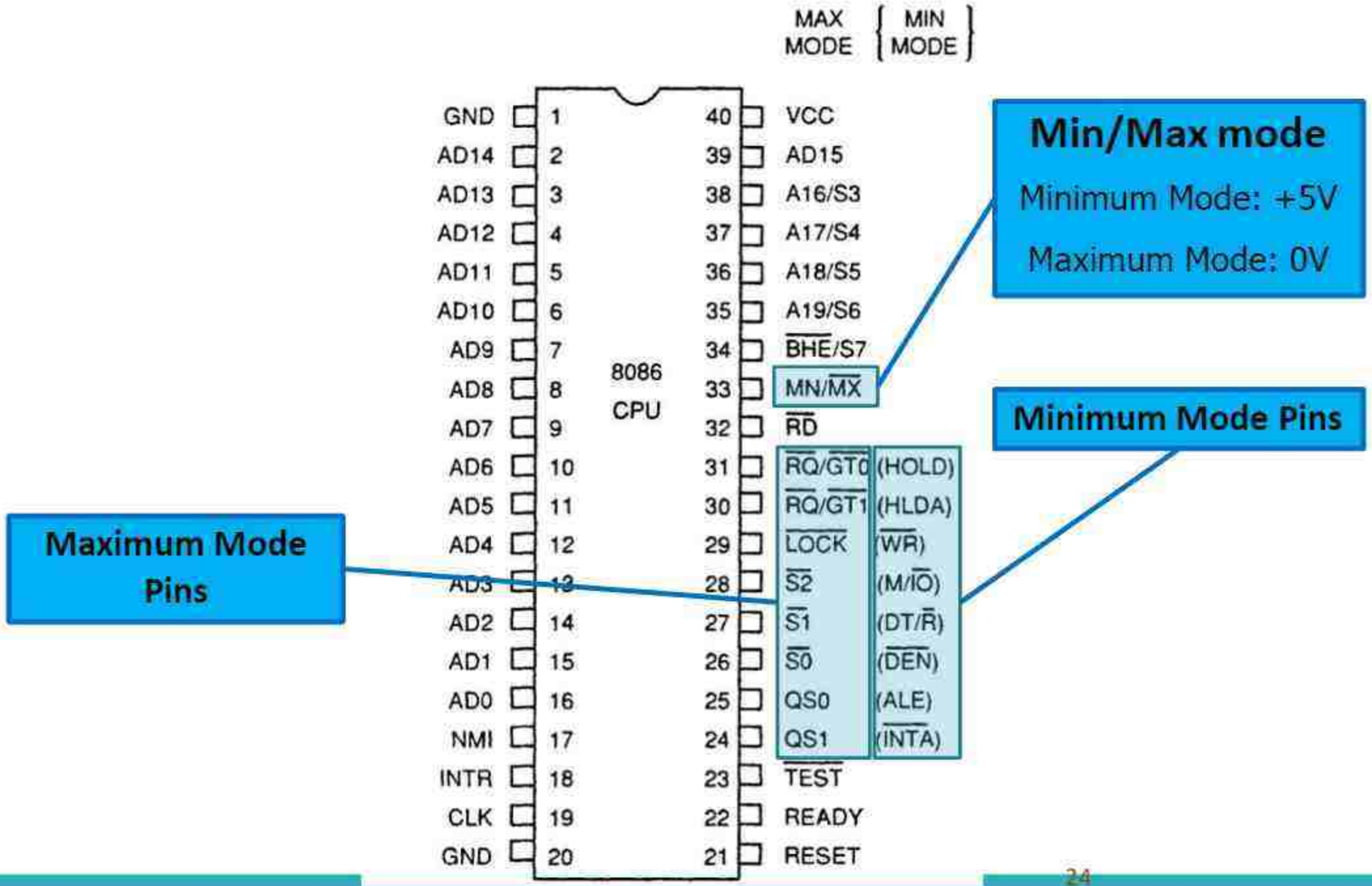


Bus High Enable/S7

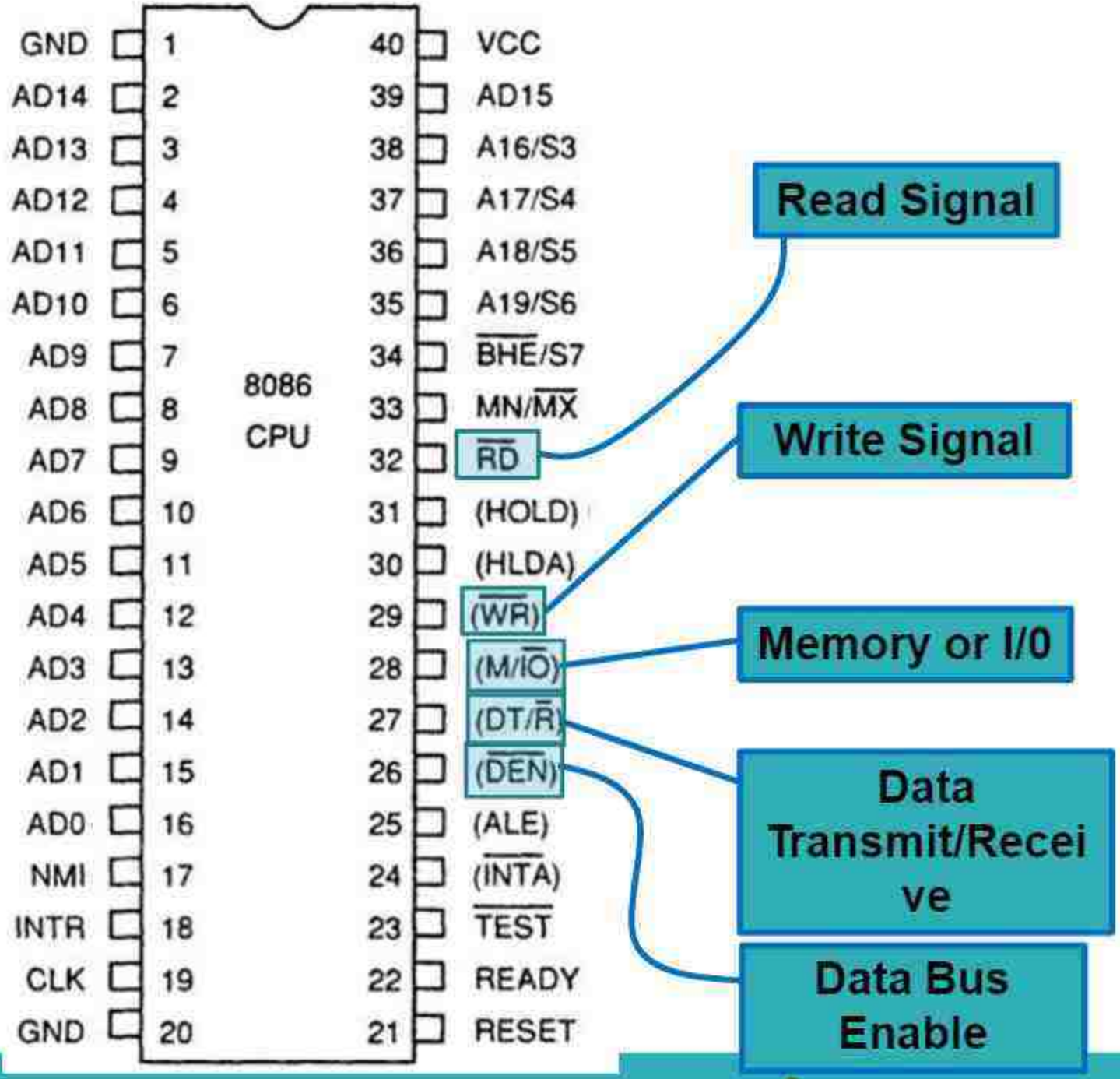
Enables most significant data bits $D_{15} - D_8$ during read or write operation.

S_7: Always 1.

INTEL 8086 - Pin Details

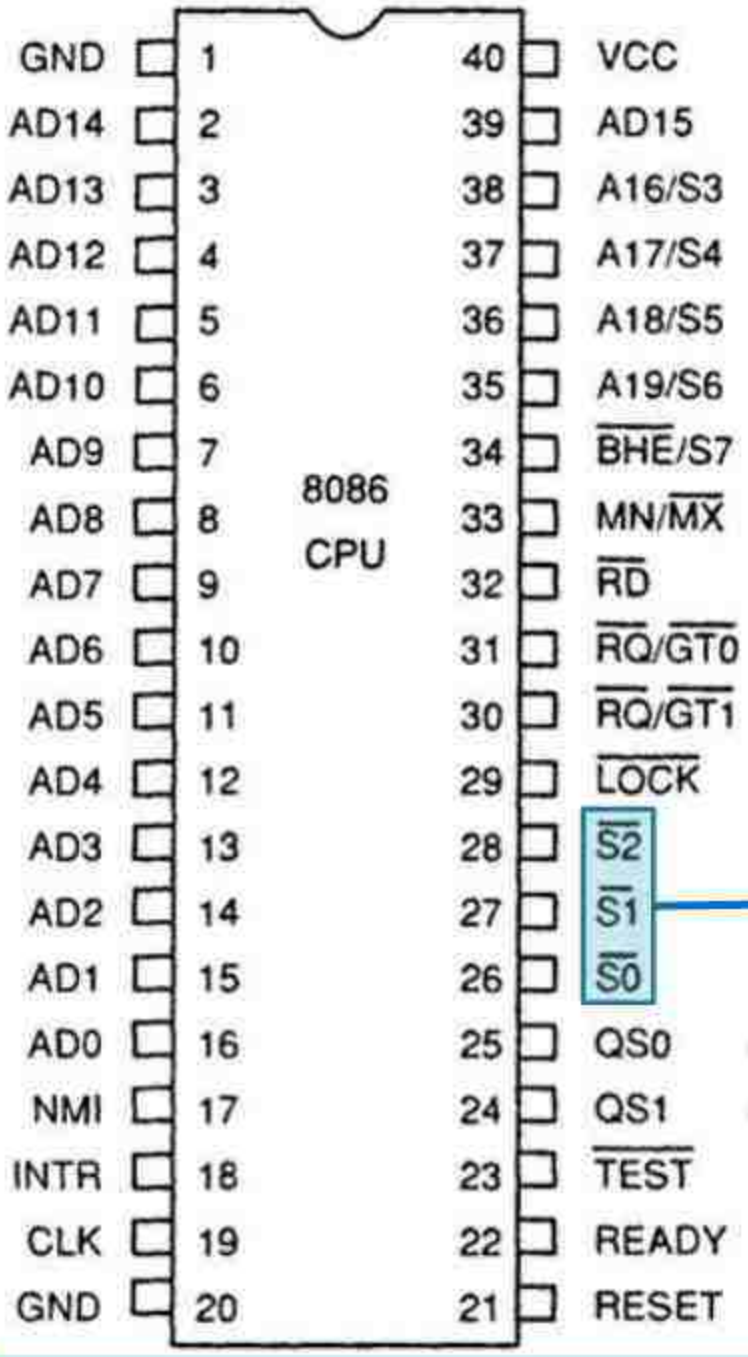


Minimum Mode- Pin Details



S2 S1 S0

000: INTA
001: read I/O port
010: write I/O port
011 hal
100: code access
101: read memory
110: write memory
111: none passive



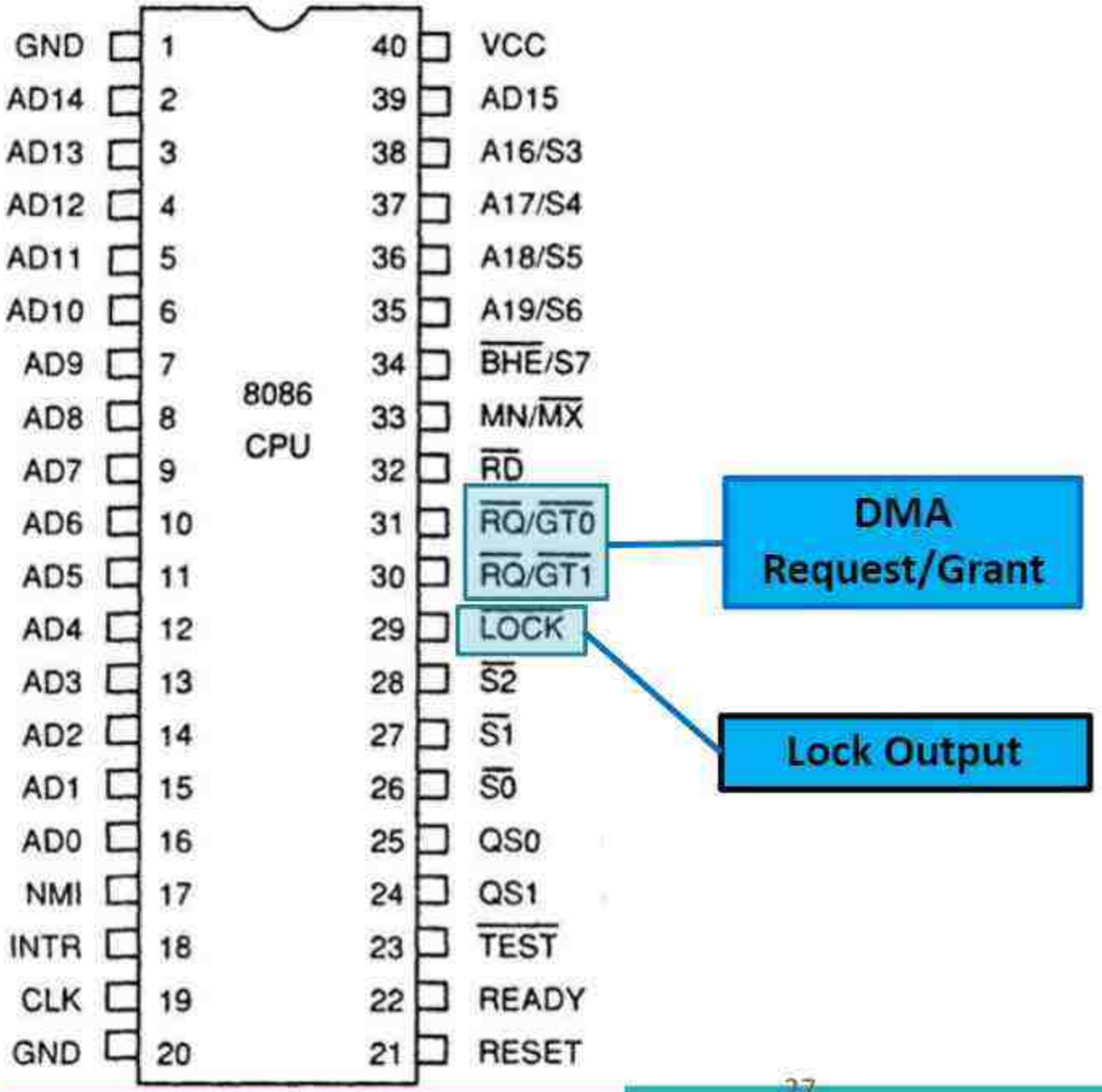
Status Signal

Inputs to 8288 to generate eliminated signals due to max mode.

Lock Output

Used to lock peripherals off the system

Activated by using the LOCK: prefix on any instruction



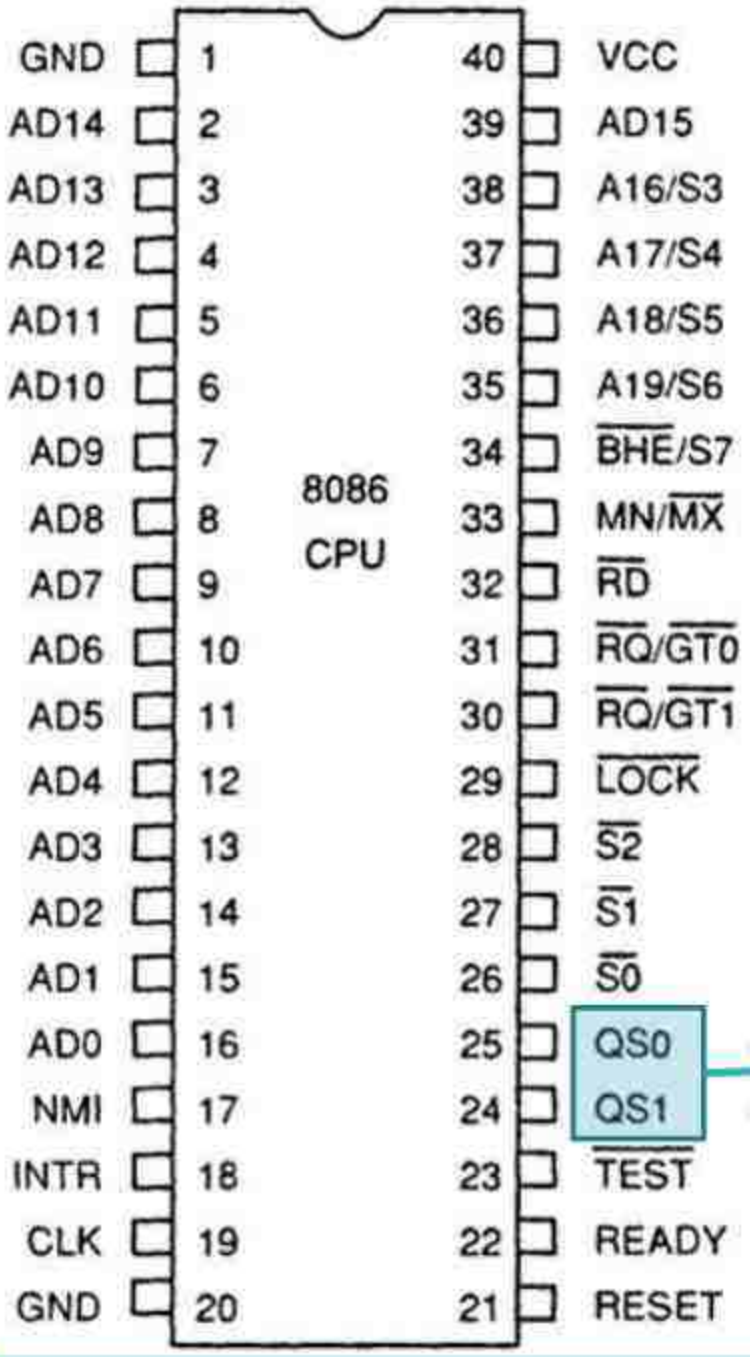
QS1 QS0

00: Queue is idle

01: First byte of opcode

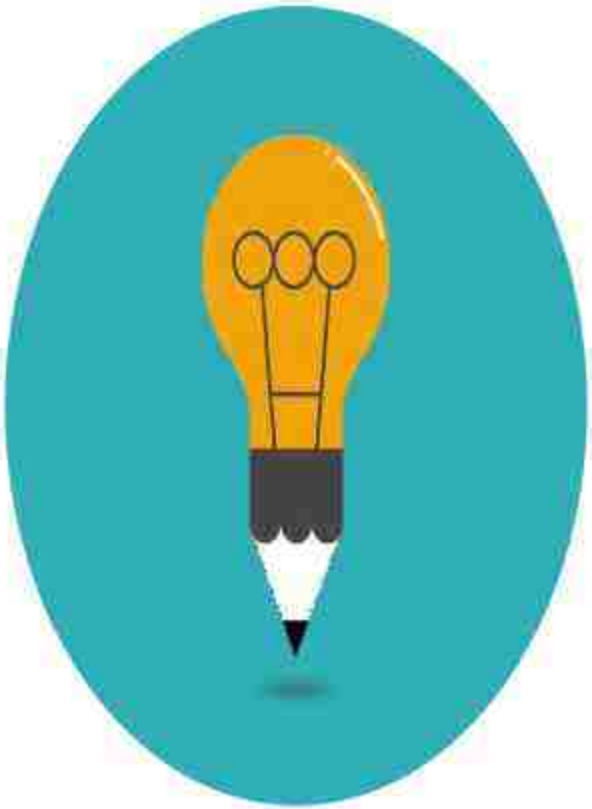
10: Queue is empty

11: Subsequent byte of opcode



Queue Status

Used by numeric coprocessor (8087)



Thank you