3.8 DIRECT MEMORY ACCESS (DMA) CONTROLLER (8257):

It is designed by Intel to transfer data at the fastest rate. It allows the device to transfer the datadirectly to/from memory without any interference of the CPU. Using a DMA controller, the device requests the CPU to hold its data, address and control bus, so thedevice is free to transfer data directly to/from the memory. The DMA data transfer is initiated only after receiving HLDA signal from the CPU.

The sequences of operations performed by a DMA are

- Initially, when any device has to send data to the memory, the device has to send DMA request (DRQ) to DMA controller.
- The DMA controller sends Hold request (HRQ) to the CPU and waits for the CPU to assertthe HLDA signal.
- Then the microprocessor tri-states all the data bus, address bus, and control bus. The CPUwill relinquish the bus and acknowledges the HOLD request through HLDA signal.
- Now the CPU is in HOLD state and the DMA controller has to manage the operations over busesbetween the memory interfaced with Microprocessor and I/O devices.

FEATURES OF 8257

- It has four channels that can be used over four I/O devices.
- Each channel has 16-bit address and 14-bitcounter.
- Each channel can transfer data up to64kb.
- Each channel can be programmed independently.

- Each channel can perform read transfer, write transfer and verify transfer operations.
- It operates in 2 modes, i.e., **Master mode** and **Slave mode**.

8257 PIN DESCRIPTION

The pin configuration of DMA Controller (8257) is shown in Figure 3.8.1 and the descriptions are as follows:

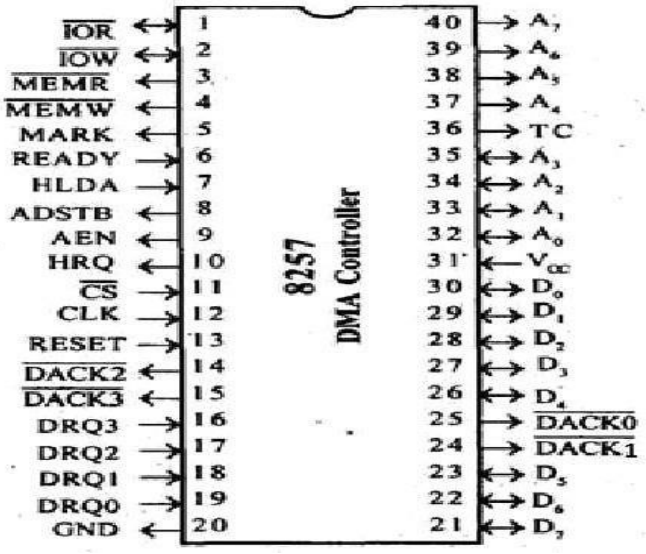

Figure 3.8.1 Pin Configuration of 8257

[Source: Advanced Microprocessors and Microcontrollers by A.K Ray & K.M.Bhurchandi]

DRQ0−DRQ3

These are the four individual channel DMA request inputs, which are used by the peripheral devices for using DMA services. When the fixed priority mode is selected, then DRQ0 has the highest priority and DRQ3 has the lowest priority.

DACKo − DACK3

These are the active-low DMA acknowledge lines, which updates the requesting peripheral about the status of their request by the CPU. These lines can also act as strobe lines for the requesting devices.

Do − D7

These are bidirectional, data lines which are used to interface the system bus with the internal data bus of DMA controller. In the Slave mode, it carries command words to 8257 and status word from 8257. In the master mode, these lines are used to send higher byte of the generated address to the latch. This address is further latched using ADSTB signal.

IOR

It is an active-low bidirectional tri-state input line, which is used by the CPU to read internal registers of 8257 in the Slave mode. In the master mode, it is used to read data from the peripheral devices during a memory write cycle.

IOW

It is an active low bi-direction tri-state line, which is used to load the contents of the data bus to the 8-bit mode register or upper/lower byte of a 16-bit DMA address register or terminal count register. In the master mode, it is used to load the data to the peripheral devices during DMA memory read cycle.

CLK

It is a clock frequency signal which is required for the internal operation of 8257.

RESET

This signal is used to RESET the DMA controller by disabling all the DMA channels.

Ao - A3

These are the four least significant address lines. In the slave mode, they act as an input, which selects oneof the registers to be read or written. In the master mode, they are the four least significant memory address output lines generated by8257.

CS

It is an active-low chip select line. In the Slave mode, it enables the read/write operations to/from 8257. Inthe master mode, it disables the read/write operations to/from 8257.

READY

It is an active-high asynchronous input signal, which makes DMA ready by inserting wait states.

HRQ

This signal is used to receive the hold request signal from the output device. In the slave mode, it is connected with a DRQ input line 8257. In Master mode, it is connected with HOLD input of the CPU.

HLDA

It is the hold acknowledgement signal which indicates the DMA controller that the bus has been grantedto the requesting peripheral by the CPU when it is set to1.

MEMR

It is the low memory read signal, which is used to read the data from the addressed memory locations during DMA read cycles.

MEMW

It is the active-low three state signal which is used to write the data to the addressed memory location during DMA write operation.

ADSTB

It is a control output line used to split data and address line through Latches.

AEN

This signal is used to disable the address bus/data bus.

TC

It stands for 'Terminal Count', which indicates the present DMA cycle to the present peripheral devices.

MARK

The mark will be activated after each 128 cycles or integral multiples of it from the beginning. It indicates the current DMA cycle is the 128th cycle since the previous MARK output to the selected peripheral device.

Vcc

It is the power signal which is required for the operation of the circuit.