PARSHVANATH CHARITABLE TRUST'S
A.P. SHAH INSTITUTE OF TECHNOLOGY
Department of Computer Science and Engineering
Data Science

Department of Computer Science Engineering Data Science

Academic Year: 2022-23 **Semester: IV**
Class / Branch: S.E.D.S. **Subject: Microprocessor Lab**

Experiment No. 10

1. **Aim: Interfacing 8255 with DYNA-86L kit. Write a program for alternate flashing, and flashing.**

2. **Hardware used:** DYNA-86L Kit ,SMPS,Keyboard,DYNA 8255 LIC,26 pin FRCcable

3. **Theory :-**

The Intel 8255A is a general purpose programmable I/O device which is designed for use with all Intel and most other microprocessors. It provides 24 I/O pins which may beindividually programmed in 2 groups of 12 and used in 3 major modes of operation.

In MODE 0, each group of 12 I/O pins may be programmed in sets of 4 and 8 to be inputs or outputs. In MODE 1, each group may be programmed to have 8 lines of input or output. 3 of the remaining 4 pins are used for handshaking and interrupt control signals. MODE 2 is a strobed bi-directional bus configuration.

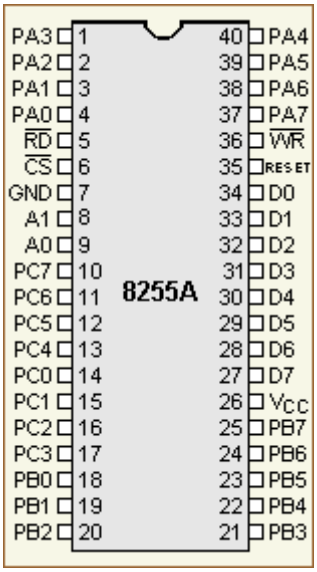
The 8255 is a 40 pin integrated circuit (IC), designed to perform a variety of interface functions in a computer environment. The 8255 wasn't originally designed to be connected to the Z80. It was manufactured by Intel for the 8080 microprocessor.

3.1 Connection:

1. Connect 26 pin FRC connector to dyna86

2. Connect keyboard and SMPS to dyna86

3.2 Pin diagram of 8255:



D0 - D7 These are the data input/output lines for the device. All information read from and written to the 8255 occurs via these 8 data lines

CS (*Chip Select Input*). If this line is a logical 0, the microprocessor can read and write to the 8255.

RD (*Read Input*) Whenever this input line is a logical 0 and the RD input is a logical 0, the 8255 data outputs are enabled onto the system data bus.

WR (*Write Input*) Whenever this input line is a logical 0 and the CS input is a logical 0, data is written to the 8255 from the system data bus

A0 - A1 (*Address Inputs*) The logical combination of these two input lines determines which internal register of the 8255 data is written to or read from.

RESET The 8255 is placed into its reset state if this input line is a logical 1. All peripheral ports are set to the input mode.

PA0 - PA7, **PB0 - PB7**, **PC0 - PC7** These signal lines are used as 8-bit I/O ports. They can be connected to peripheral devices. The 8255 has three 8 bit I/O ports and each one can be connected to the physical lines of an external device. These lines are labeled PA0-PA7, PB0-PB7, and PC0-PC7. The groups of the signals are divided into three different I/O ports labeled port A (PA), port B (PB), and port C (PC).

3.3 Block diagram of 8255

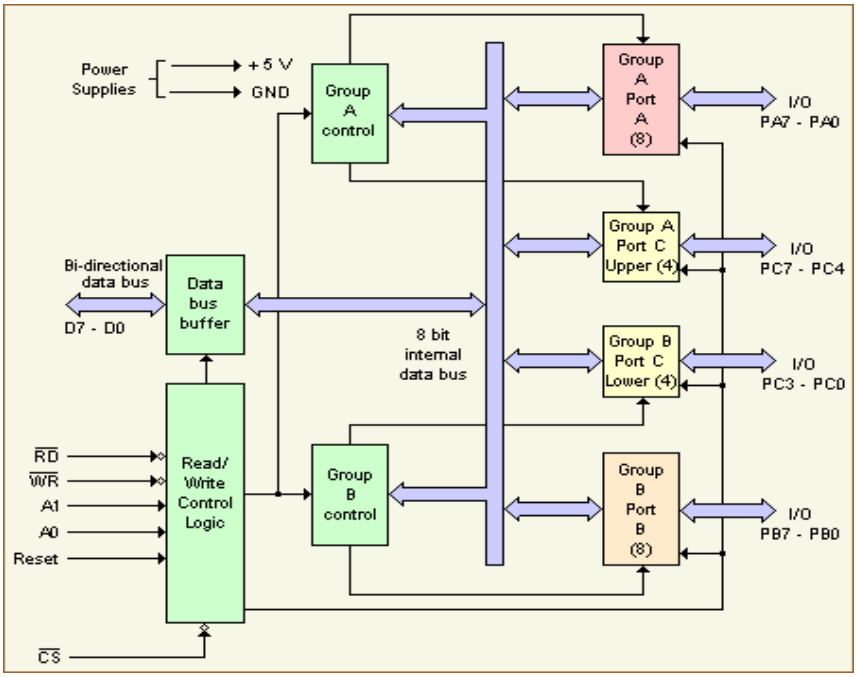
- Two control groups, labeled group A control and group B control define how the three I/O ports operate. There are several different operating modes for the 8255 and these modes must be defined by the CPU writing programming or control words to the device 8255.

- The line group of port C consists of two 4 bit ports. One of the 4 bit group is associated with group A control and the other 4 bit group with group B control device signals. The upper 4 bits of port C are associated with group A control while the lower 4 bits are associated with group B control.

- The final logic blocks are read/write control logic and data bus buffer. These blocks provide the electrical interface between the Z80 and the 8255.

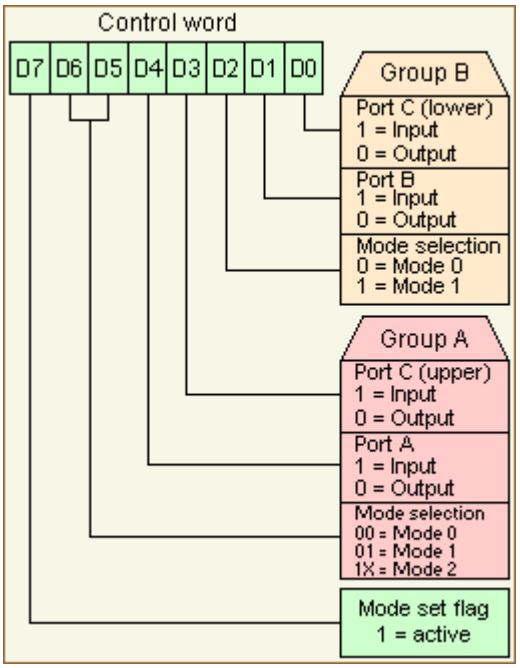
- The data bus buffer buffers the data I/O lines to/from the Z80 data bus. The read/write control logic routes the data to and from the correct internal registers withthe right timing. The internal path being enabled depends on the type of operation performed by the Z80. The type of operation can be I/O read or I/O write.

-

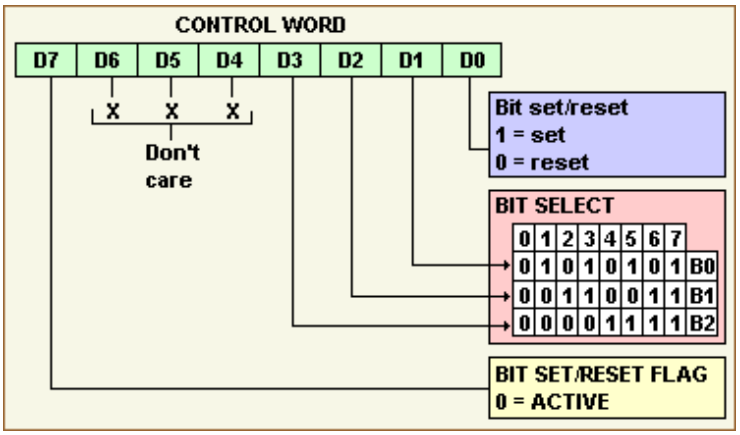


3.4 Control word of 8255:

If bit 7 of the control word is a logical 1 then the 8255 will be configured. See the picture of the practicable configurations:



If bit 7 of the control word is a logical 0 then each bit of the port C can be set or reset. See the picture of the practicable possibilities:



3.5 Program:

- Program for alternate flashing

MOV AL,89

OUT 67,AL //8255 control word

MOV AL,0FF //one side of LED,s will glow

OUT 61,AL //write 0FF on port A

MOV AL,0 //another side is off

OUT 63,AL //write 0 on port B

CALL 59E8 //call delay

MOV AL,0

OUT 61,AL //port A

MOV AL,0FF //one side of LED,s will glow

OUT 63,AL //port B

CALL 59E8 //delay

CALL F000:0CEC //check for key

JC 58AD //Main_Menu

JMP 58F7

- Program for flashing

MOV AL,89

OUT 67,AL //8255 control word

MOV AL,0 //one side of LED,s turn off

OUT 61,AL //write 0 on port A

OUT 63,AL //write 0 on port B

CALL 59E8 //call delay

MOV AL,0FF

OUT 61,AL //write 0FF on port A

OUT 63,AL //write 0FF port B

CALL 59E8 //delay

CALL F000:0CEC //check for key

JNC 5923

JMP F000:58AD //Main Menu

JMP 5923 //loop

JMP 5456

4.Conclusion :