University of Mumbai

Examinations Commencing from 10th April 2021 to 17th April 2021

Program: Bachelor of Engineering in Computer Engineering

Curriculum Scheme: Rev2019

Examination: DSE SemesterIII

Course Code: **CSC304** and Course Name: **Digital Logic & Computer Architecture**

Time: 2 hour Max. Marks: 80

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<table>
<tr><td>Q1.</td><td>Choose the correct option for following questions. All the Questions are compulsory and carry equal marks.</td></tr>
<tr><td></td><td></td></tr>
<tr><td>1.</td><td>Which of the following options represents the correct matching?
<table>
<tr><th>Addressing Mode</th><th>Description</th></tr>
<tr><td>1. Immediate</td><td>A. the address field refers to the address of a word in the memory, which in-turn contains the address of the operand</td></tr>
<tr><td>2. Direct</td><td>B. the address field contains the address (in main memory) where the operand is stored</td></tr>
<tr><td>3. Indirect</td><td>C. operand value is present in the instruction itself (address field)</td></tr>
<tr><td>4. Register Direct</td><td>D. the address field of the operand is a register</td></tr>
</table></td></tr>
<tr><td>Option A:</td><td>1->A; 2->D; 3->C; 4->B;</td></tr>
<tr><td>Option B:</td><td>1->C; 2->B; 3->D; 4->A;</td></tr>
<tr><td>Option C:</td><td>1->C; 2->B; 3->A; 4->D;</td></tr>
<tr><td>Option D:</td><td>1->A; 2->D; 3->B; 4->C;</td></tr>
<tr><td></td><td></td></tr>
<tr><td>2.</td><td>Consider an example of memory organization as shown in the figure below. Which value will be loaded into the accumulator when the instruction “LOAD DIRECT 3” is executed?
<table>
<tr><td>Memory Location address</td><td>0</td><td>1</td><td>2</td><td>3</td><td>4</td><td>5</td><td>6</td><td>7</td></tr>
<tr><td>Content</td><td>10</td><td>23</td><td>25</td><td>20</td><td>12</td><td>3</td><td>1</td><td>2</td></tr>
</table></td></tr>
<tr><td>Option A:</td><td>3</td></tr>
<tr><td>Option B:</td><td>25</td></tr>
<tr><td>Option C:</td><td>12</td></tr>
<tr><td>Option D:</td><td>20</td></tr>
<tr><td></td><td></td></tr>
<tr><td>3.</td><td>For a 0-address instruction format, what would be the top element of the stack following sequences of instructions? PUSH 20; PUSH 5; PUSH 5; ADD; SUB; PUSH 20; MULT</td></tr>
</table>

Option A:	100
Option B:	200
Option C:	10
Option D:	5
4.	What is the value of n in Booth's multiplication of 110* 1000?
Option A:	2
Option B:	3
Option C:	4
Option D:	0
5.	In restoring division algorithm, after performing operations (1) left shift operation on A,Q and (2) A=A-M, if magnitude of A > 0 then ?
Option A:	Q0=0, A=A+M
Option B:	A=A+M
Option C:	Q0=1
Option D:	A=A-M
6.	In non-restoring division algorithm, after performing left shift operation on A, Qregisters,if magnitude of A < 0 then?
Option A:	Q0=0, A=A+M
Option B:	A=A+M
Option C:	Q0=1
Option D:	A=A-M
7.	In single precision, IEEE754 floating point standard exponent represent by ___bits and mantissa represent by _____ bits.
Option A:	8, 23
Option B:	7, 24
Option C:	7, 23
Option D:	8, 24
8.	How many bits of opcode is required to implement a CPU with 10 arithmetic and logical instructions, 2 control instructions, and 5 data transfer instructions?
Option A:	2
Option B:	3
Option C:	4
Option D:	5
9.	In a J-K flip-flop, if J=K the resulting flip-flop is referred to as _____
Option A:	D flip-flop
Option B:	S-R flip-flop
Option C:	T flip-flop
Option D:	S-K flip-flop

10.	The instruction read from memory is then placed in the_____ and contents of program counter is_____ so that it contains the address of_____ instruction in the program.
Option A:	Program counter, incremented and next
Option B:	Instruction register, incremented and previous
Option C:	Instruction register, incremented and next
Option D:	Address register, decremented and next
11.	Which is the simplest method of implementing hardwired control unit?
Option A:	State Table Method
Option B:	Delay Element Method
Option C:	Sequence Counter Method
Option D:	Using combinational Circuits
12.	Which instruction does the following set of micro-operations refer to: Steps Action 1 PCout, MARin, Read, Select4, Add, Zin 2 Zout, PCin, Yin, WMFC 3 MDRout, IRin 4 R1out, Yin 5 R2out, SelectY, Add, Zin 6 Zout, R1in, End
Option A:	ADD R2, R1
Option B:	ADD R1, R2
Option C:	MOVE R1, R2
Option D:	MOVE R2, R1
13.	Which of the following statements is false?
Option A:	Diagonal micro-instructions encoding requires multiple decoders.
Option B:	In vertical micro-instructions encoding, more than one control signals cannot be activated at a time.
Option C:	Horizontal micro-instructions encoding has a lower cost of implementation.
Option D:	On one end of a spectrum, a *vertical* microinstruction is highly encoded and may look like a simple macroinstruction containing a single opcode field and one or two operand specifiers.
14.	In _____ mapping, the data can be mapped anywhere in the Cache Memory.
Option A:	Associative
Option B:	Direct
Option C:	Set Associative
Option D:	Indirect
15.	A second factor in locality of reference is the presence of loops in programs. Instructions in a loop, even when they are far apart in spatial terms, are executed repeatedly, resulting in a high frequency of reference to their addresses. This characteristic is referred to as _____.

Option A:	Spatial locality.
Option B:	temporal locality
Option C:	branch locality.
Option D:	Equidistant locality
16.	_____ consists essentially of internal flip-flops that store the binary information.
Option A:	Static RAM
Option B:	Dynamic RAM
Option C:	PROM
Option D:	EEPROM
17.	SIMD represents an organization that _____.
Option A:	refers to a computer system capable of processing several programs at the same time.
Option B:	represents organization of a single computer containing a control unit, processor unit and a memory unit.
Option C:	includes many processing units under the supervision of a common control unit.
Option D:	similar to Von Neumann architecture.
18.	In parallelization, if P is the proportion of a system or program that can be made parallel, and 1-P is the proportion that remains serial, then the maximum speedup that can be achieved using N number of processors is 1/((1P)+(P/N). This law is called _____
Option A:	Newton's law
Option B:	Ohms law
Option C:	Amdahl's law
Option D:	Flynn's law
19.	To resolve the clash over the access of the system BUS we use _____
Option A:	Multiple BUS
Option B:	BUS arbitrator
Option C:	Priority access
Option D:	DMA controller
20.	Select true statement from the following.
Option A:	USB is a parallel mode of transmission of data and this enables for the fast speeds of data transfers.
Option B:	In USB the devices can communicate with each other.
Option C:	The type/s of packets sent by the USB is/are Data.
Option D:	When the USB is connected to a system, its root hub is connected to the Processor BUS.

Q.2 Solve any Four out of Six.

a)	Briefly describe the Von Neumann Model computer architecture.	**5**
b)	Write a short note on Interleaved and Associative Memory.	**5**
c)	Differentiate between hardwired control unit and Microprogrammed Control unit.	**5**
d)	What is the meaning of delayed branch and branch prediction? Write a difference between them.	**5**
e)	Draw and explain the instruction cycle state diagram.	**5**
f)	Multiply (-10) and (-8) using Booth's algorithm.	**5**

Q.3 Solve any Two out of Three.

a)	Draw the flowchart of Restoring Division Algorithm & perform 10 /3 using this Algorithm.	**10**
b)	Explain with suitable diagrams - Flynn's Classification of Computer Architecture.	**10**
c)	Consider a Cache memory of 16 words. Each block consists of 4 words. Size of the main memory is 128 bytes. Draw the Associative Mapping and Calculate the TAG and WORD size.	**10**