CSC405 MICROPROCESSORS

80386 FUNCTIONAL BLOCK DIAGRAM/ARCHITECTURE

OBJECTIVE

1. Objective: To understand the architecture of 80386 processor.

Ques. Design 8086 based minimum mode system for following requirements :-

i) 256 KB ROM using 32 KB x8 devices
ii) 512 KB RAM using 64 KB x8 devices
iii) Support top 15 Interrupts
iv) 2-Nos., 8 bit parallel port.

I/O Map :-

8bit
for 2 parallel port → 1 8255 chip

for 15 interrupts → 2 8259 {1 master, 1 slave}

8 bit 2 ports

Chip		Addr. Bus								Address
		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	
8255 (Even Bank)	PA	1	0	0	0	0	0	0	0	80 H
	PB	1	0	0	0	0	0	1	0	82 H
	PC	1	0	0	0	0	1	0	0	84 H
	CW	1	0	0	0	0	1	1	0	86 H
8259 (Even Bank)	ICW1	0	1	1	0	0	0	0	0	60 H
	ICW2	0	1	1	0	0	0	1	0	62 H
8259 HB	ICW1	0	1	1	0	0	0	0	1	61 H
	ICW2	0	1	1	0	0	0	1	1	63 H

80386

80 x 86

1. 80386 is a 32 bit processor
2. 80386 - 32 bit ALU in one cycle
3. 32 bit data bus.
   - ↓
   - 4 mly locations
   - ↓
   - 4 chips
4. 80386 has a 32 bit address bus
   - $2^2 \times 2^{30}$
   - 4 GB //
   - 2^{32}
   - 2^{10} 2^{20} - 1MB $2^{30} \Rightarrow 1$ GB //
   - 2^{30} -

8086

16 bit up

↓

16 bit ALU

32 bit addition

2 cycles

16 bit data

↓

2 chips

20 bit

$2^{20} \approx 1$ MB

(5) 16 MHz, 20 MHz, 25 MHz, 33 MHz frequencies

16 MHz
↓
3
6 MHz

(6) 80386 was released in 2 versions SX & DX

SX (single Execution)
↓
16 bit data bus
16 bit processed

DX (Double Execution speed)
↓
32 bit data bus

2 banks

BHE & BLE

4 m/y banks

Enable $\overline{BE_3}$ $\overline{BE_2}$, $\overline{BE_1}$, $\overline{BE_0}$

2 bytes → pipelining

4 bytes were prefetched

16 bit data bus ✓

dynamic data bus → 16 bit / 32 bit

BS16

lowest m/y addr location

(7) 3 stage
- fetch
- decode
- execute

8086 → 2 stage pipelining
- Bus Interface Unit
- Execution Unit

(8) can access 64 TB of virtual m/y

80386 → 1TB, 2TB, ...

Secondary storage → hard disk

DIV / EV

(9) Segmentation
Paging

Virtual address ⇒ physical

(10) Protection Mechanism — 80386

8086 ⇒ specify address

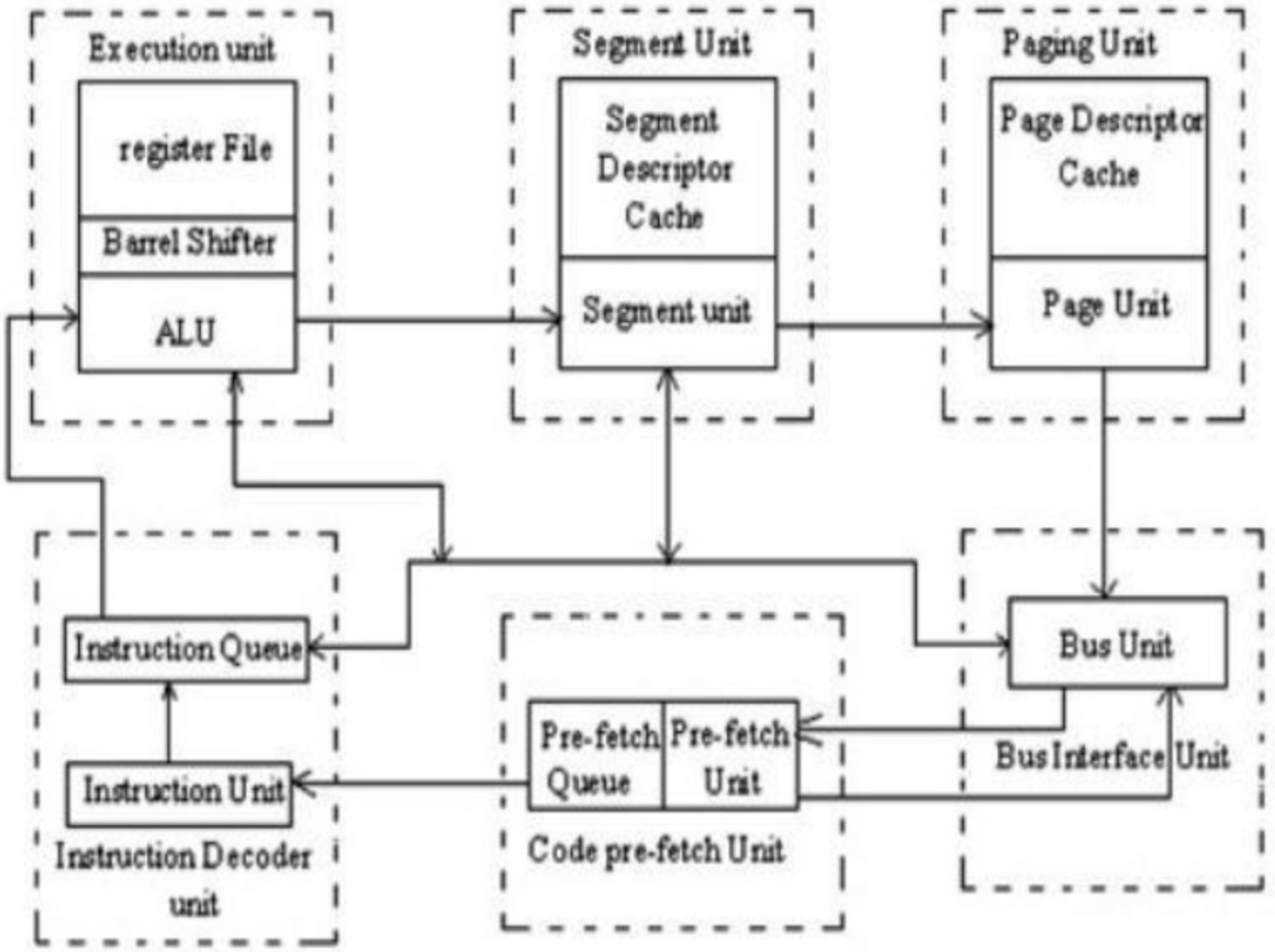
80386

Programmer is not allowed to specify address

privilege → 0 → highest ← kernel
↓ → devices
2 →
3 → lowest → user program

(11) Multitasking – higher performance

(12) – I/O addressing – 16 bit I/O address ⇒ 2^{16} ↓ 65536 I/O devices


Execution unit
register File
Barrel Shifter
ALU
Segment Unit
Segment Descriptor Cache
Segment unit
Paging Unit
Page Descriptor Cache
Page Unit
Instruction Queue
Instruction Unit
Instruction Decoder unit
Pre-fetch Queue
Pre-fetch Unit
Code pre-fetch Unit
Bus Unit
Bus Interface Unit

Thank you