CSC405 MICROPROCESSORS

8259 Programmable Interrupt Controller

OBJECTIVE

1. To understand 8259 Block Diagram and Interfacing in Single Mode – Programmable Interrupt Controller.

8259 - PIC

8086

Mly 8086
8255 - PPI
8257 - DMA C
8259 - PIC

→ accepting interrupts -

① Non Maskable Interrupt

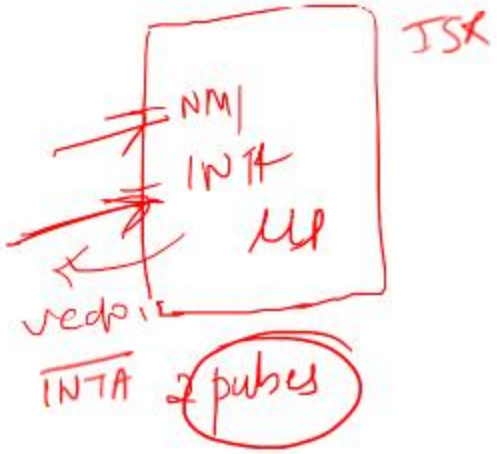
② Interrupt INTR

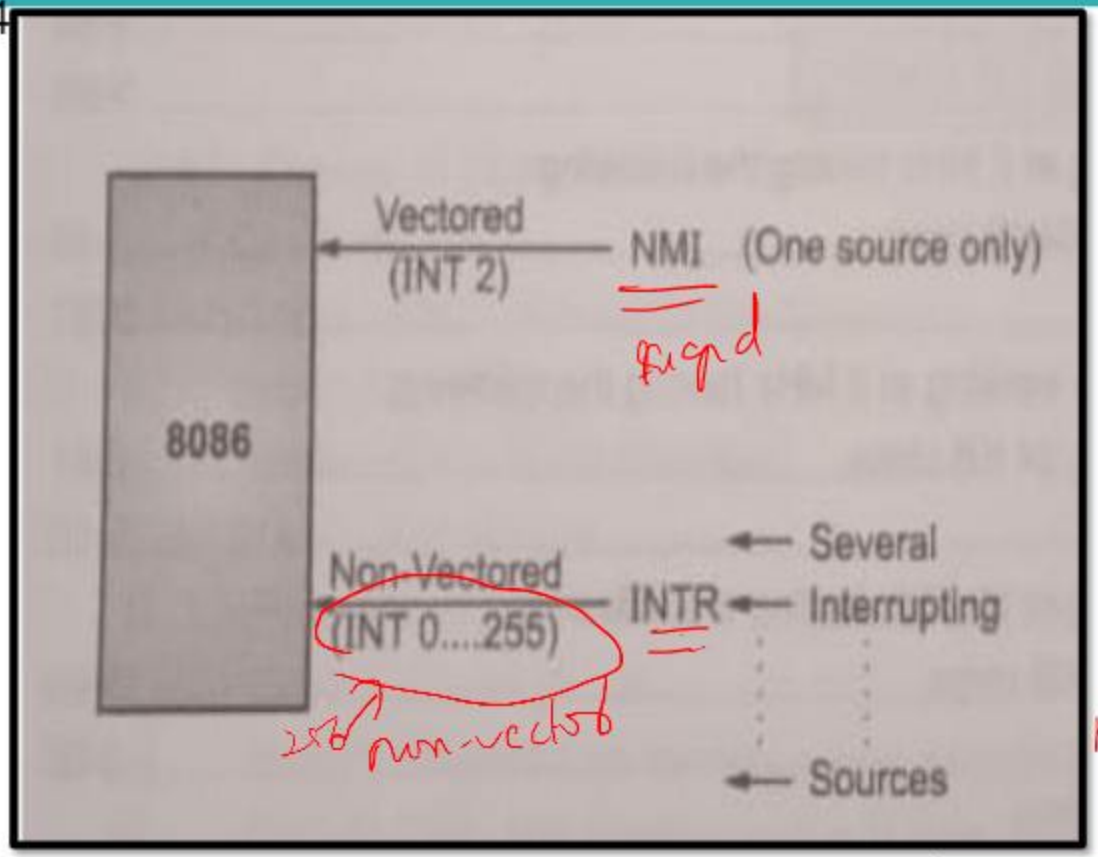
INTR - non vectored INT

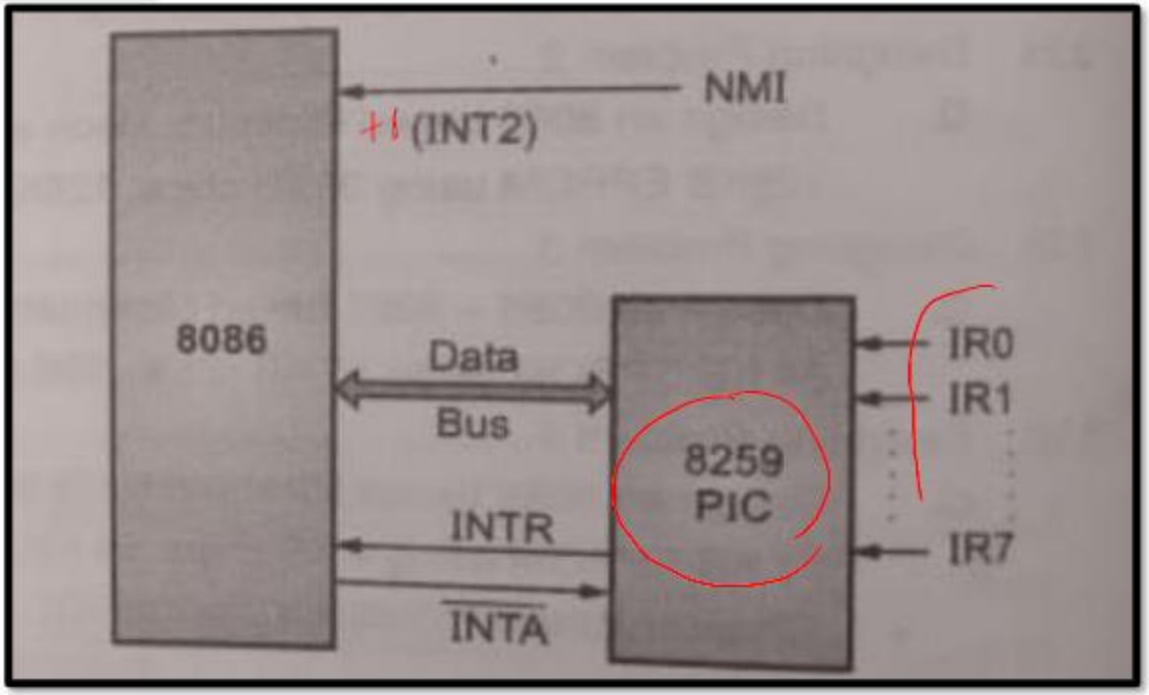
INTA

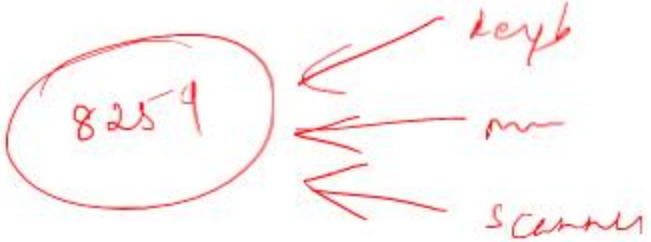
2 pins

2 interrupts




8086
Vectored
(INT 2)
NMI
(One source only)
Non Vectored
(INT 0....255)
INTR
Several
Interrupting
Sources


8086
NMI
(INT2)
Data
Bus
INTR
INTA
8259
PIC
IR0
IR1
IR7



Interrupt

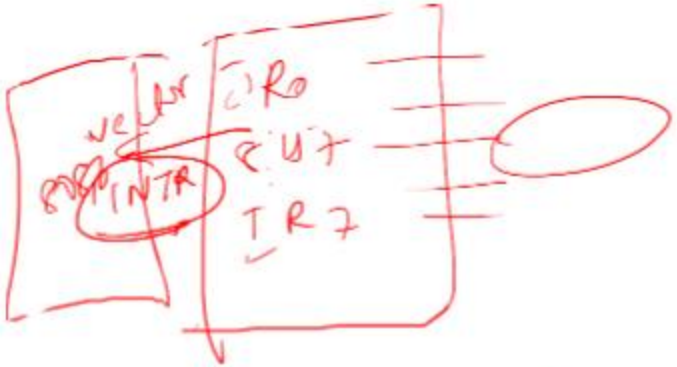
Priority

Masking

Trigger

Vector

service



INTA

2 pulses

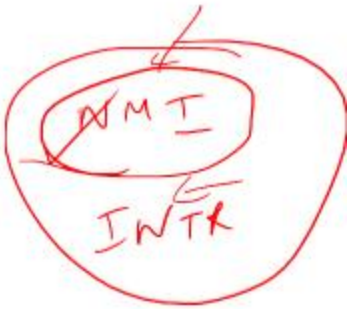
8259

Priority

8259

IR0 ←

8086

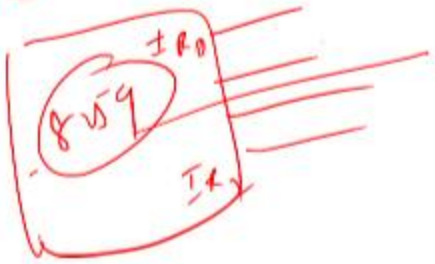


8259

commands

IR7

Masking



marked chosen to ignore

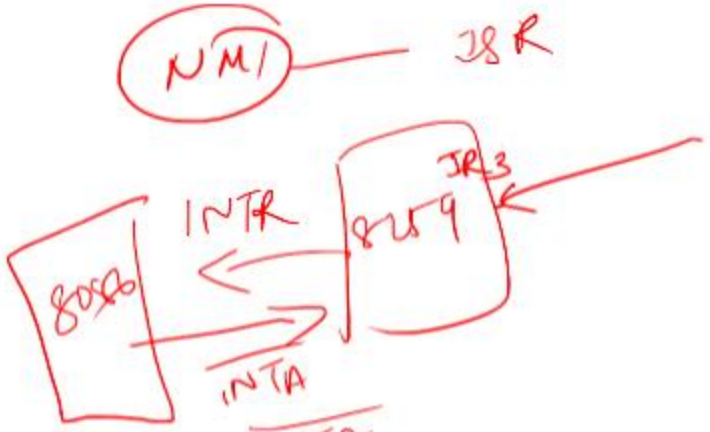
8259

Triggering:

edge triggered

level triggered

8 ← programmer



8259

Vector No

IR0 → 40H

41H

42H

IR7 - 47H

8259

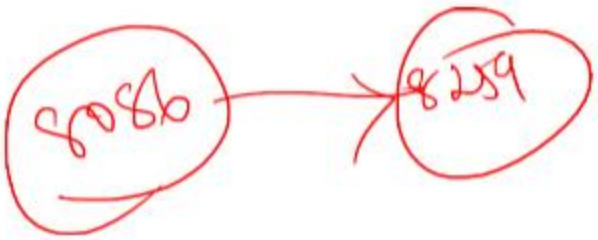
priority ← no problem

IR0
:
IR7 ✓

trigger ← no problem

masking ← unmasked

vector ← problem

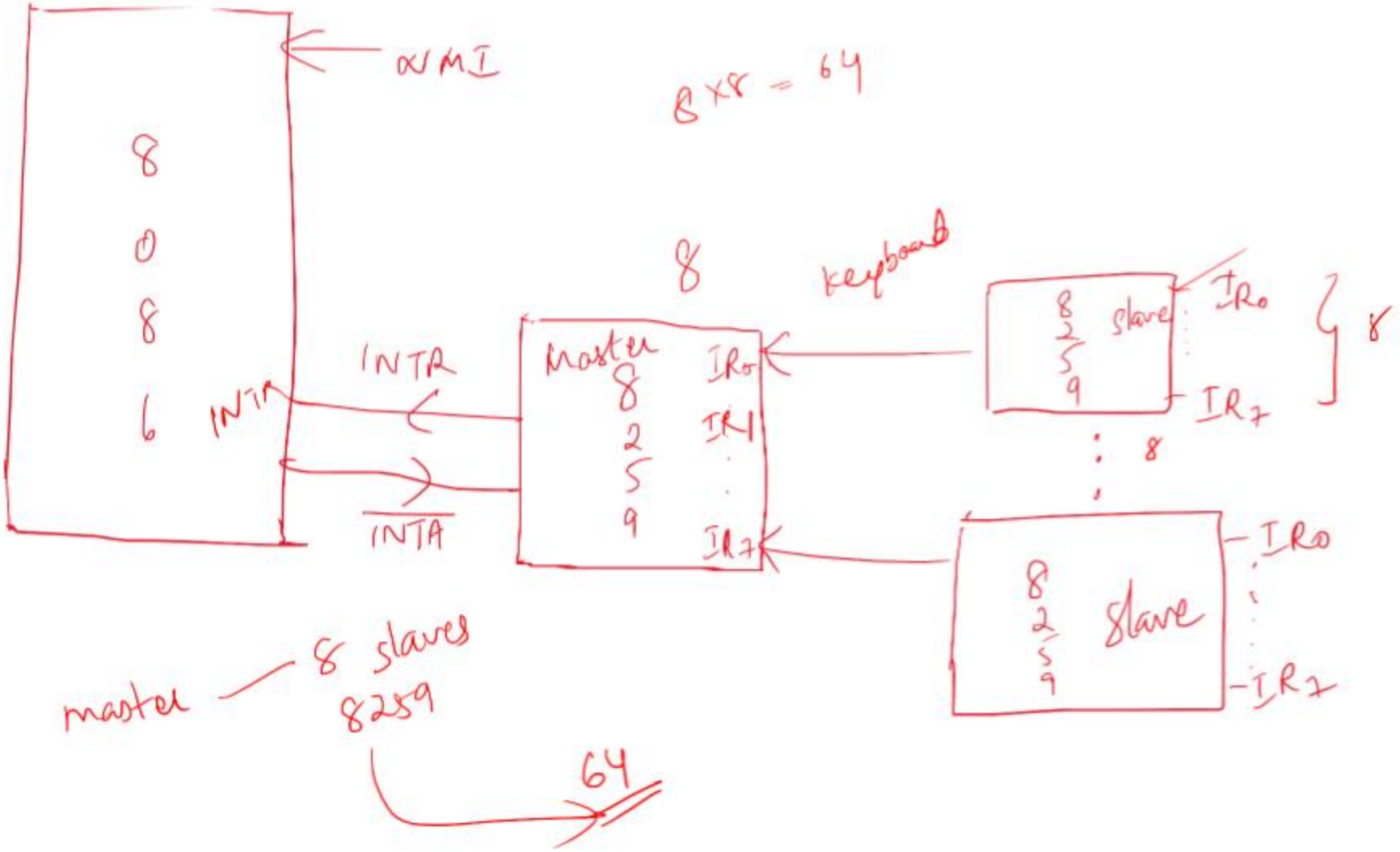


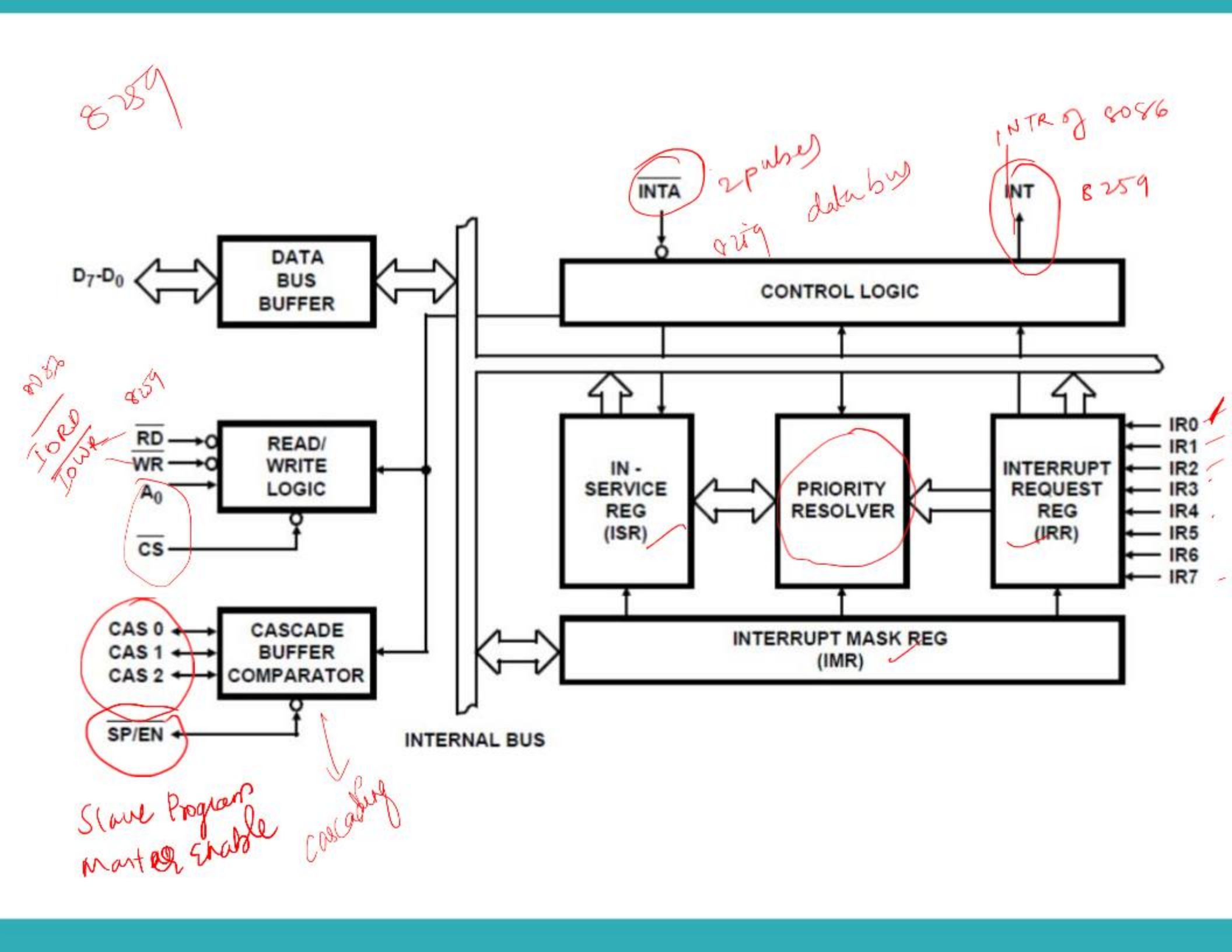
8259

8

8086

Cascading

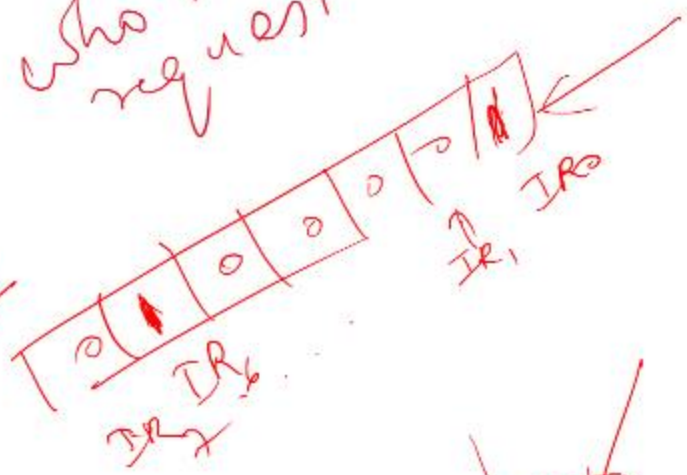



INTA
INT
D7-D0
DATA BUS BUFFER
CONTROL LOGIC
RD
WR
A0
CS
READ/ WRITE LOGIC
IN - SERVICE REG (ISR)
PRIORITY RESOLVER
INTERRUPT REQUEST REG (IRR)
IR0
IR1
IR2
IR3
IR4
IR5
IR6
IR7
CAS 0
CAS 1
CAS 2
CASCADE BUFFER COMPARATOR
SP/EN
INTERRUPT MASK REG (IMR)
INTERNAL BUS

IRR

8 bit register → 8 requests

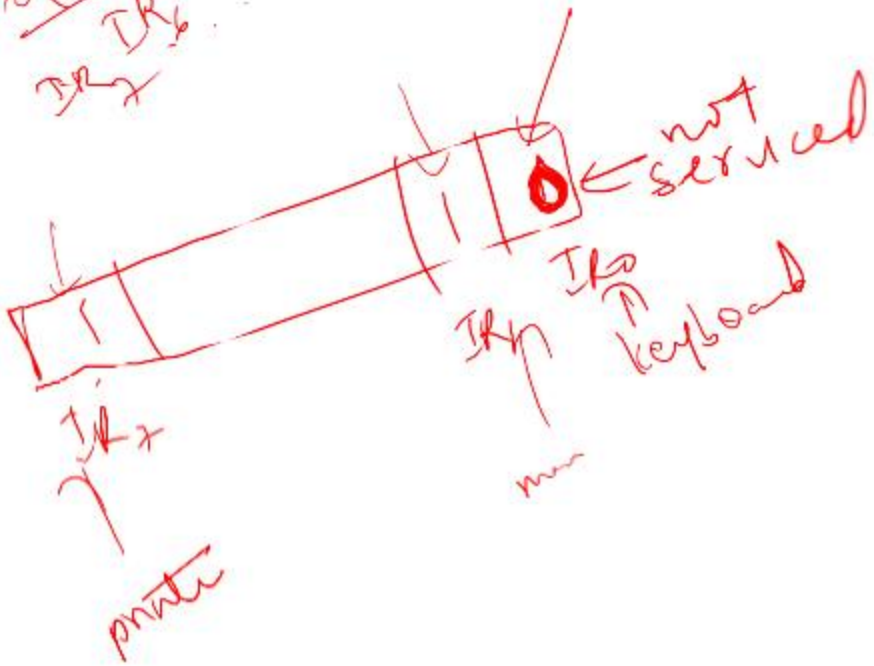
who has requested?

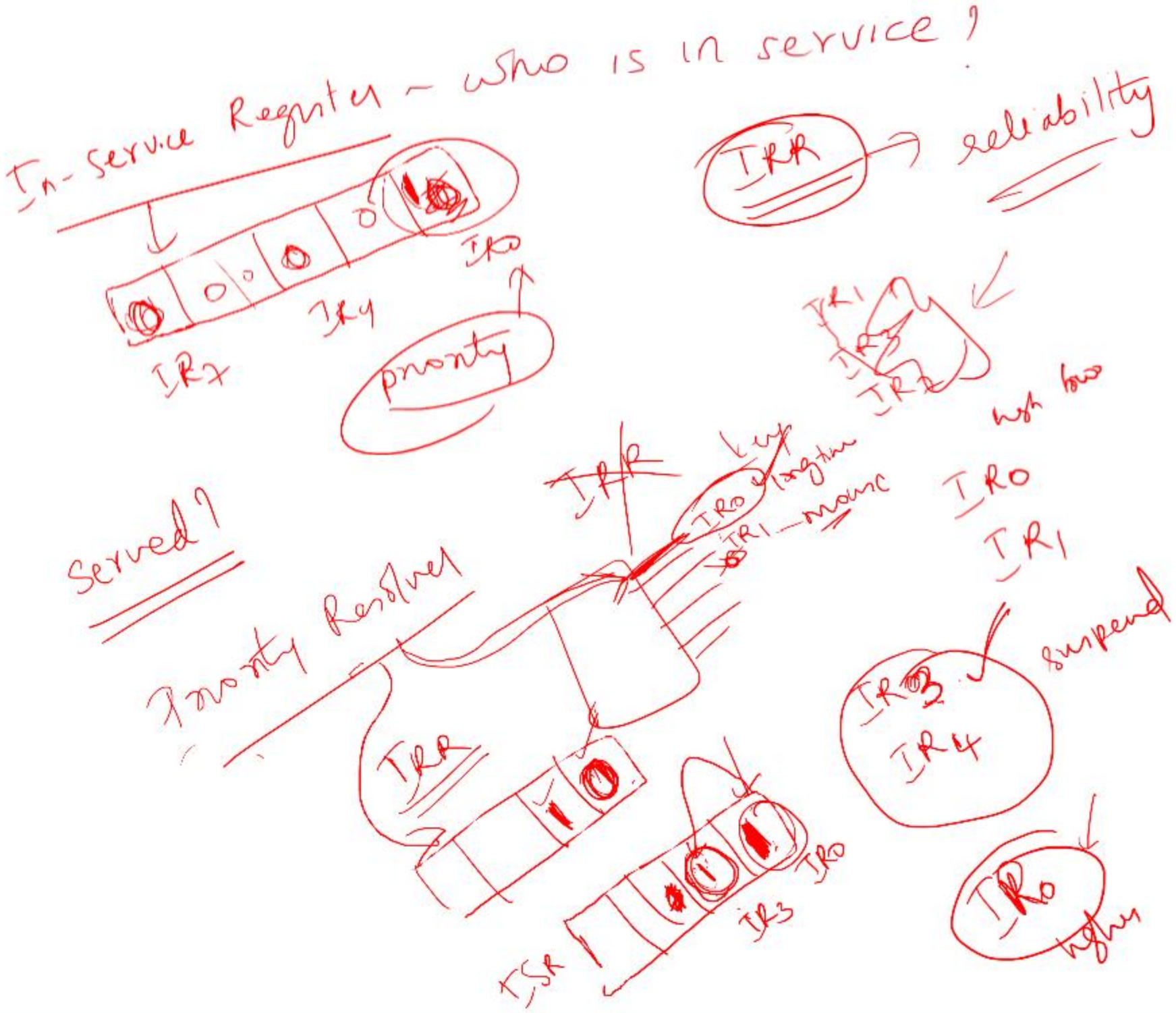


IMR

8 bit register

marked




In-Service Register - who is in service?
IRR
reliability
IR7
IR4
IR0
priority
IR1
IR2
IRR
Served?
Priority Resolver
IR0
IR1 - more
IR0
IR1
IR3
IR4
suspend
IR0
IR3
ISR
IR0
highest

In SR ⇒ 7th bit – 1

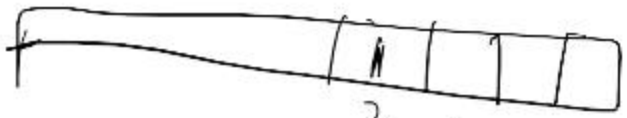
IMR ⇒ 3rd bit – 1

IRR ⇒ IR_3 & IR_5

↓

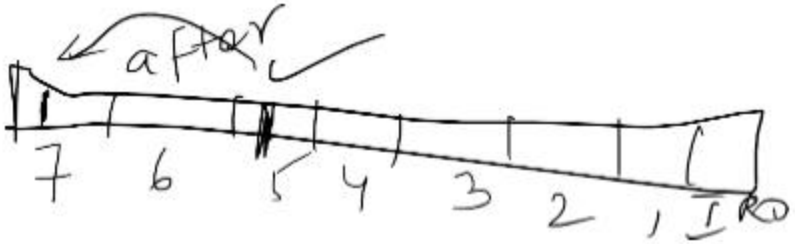
higher priority

IMR



← ignore IR3

IR5 but



↓

5 higher priority

8259 → PIC

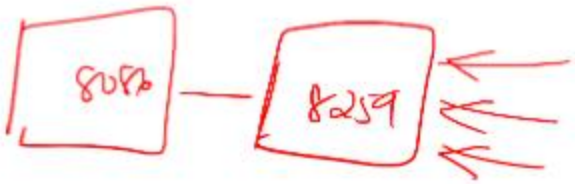
NMI
INTR

8 → IR_0 ... IR_7

0 1 2 3 ... 7

1–8

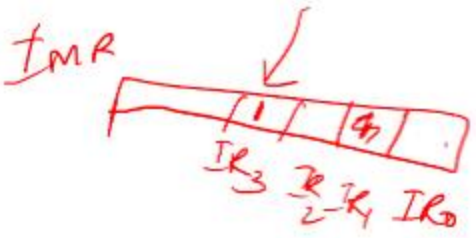
8 × 8 = 64

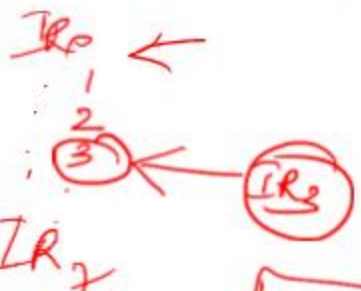


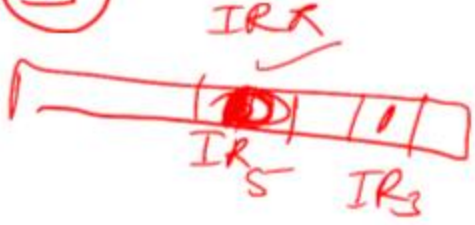
InSR → 4th bit is a 1

IMR → 4th bit is a 1

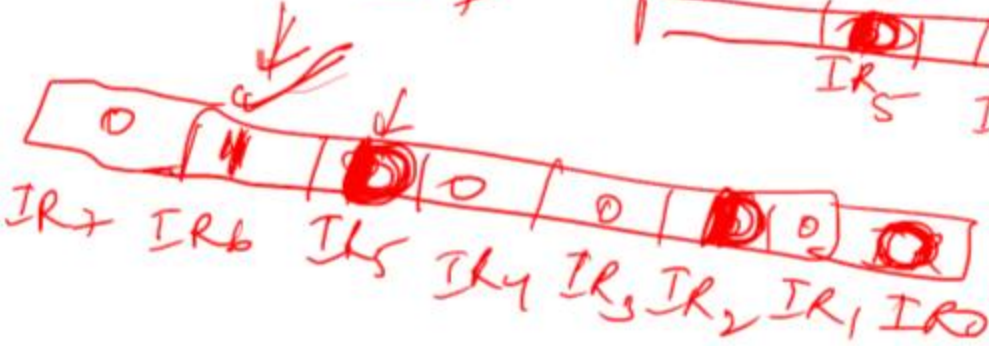
IRR → IR_3 & IR_5

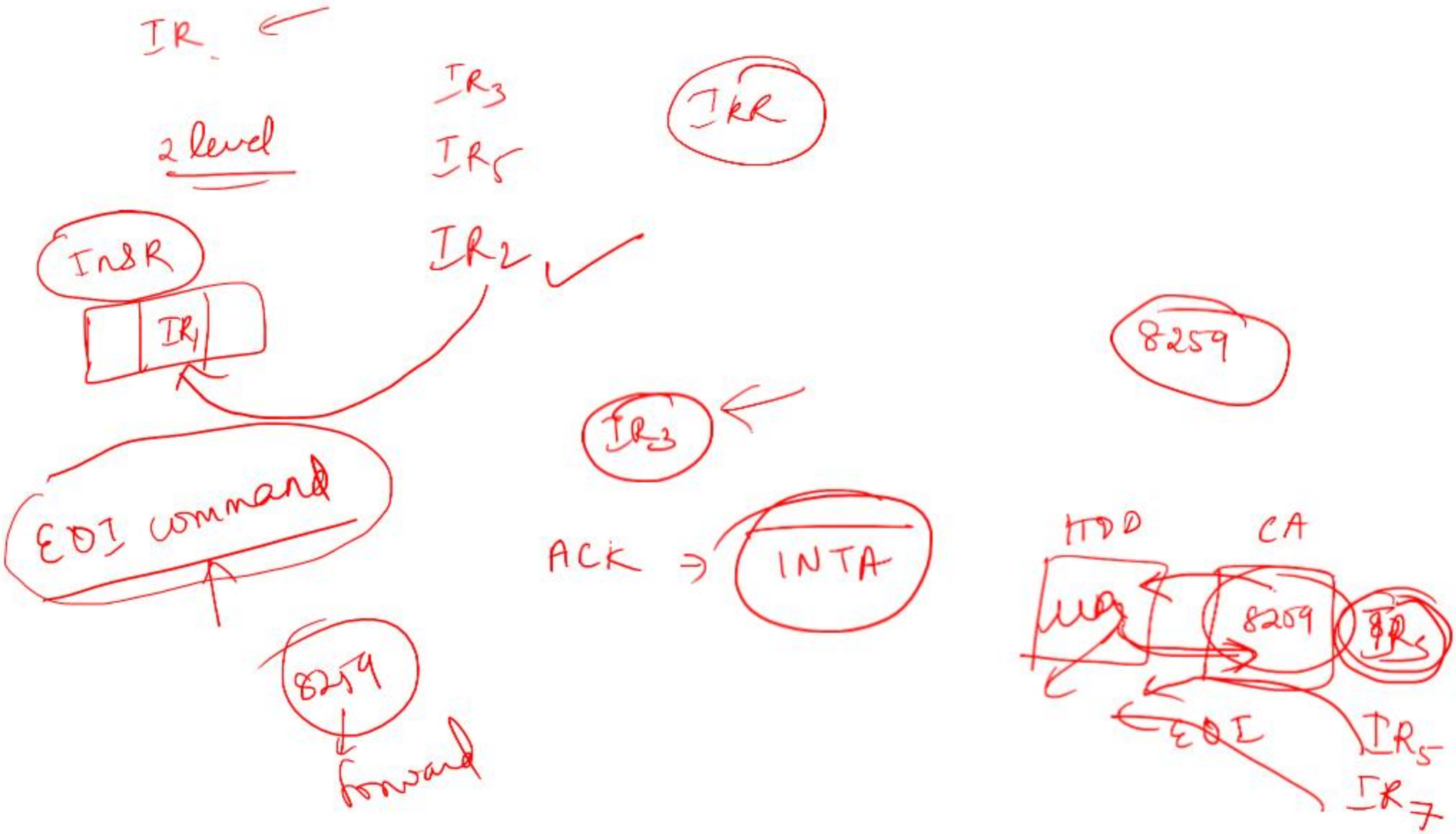


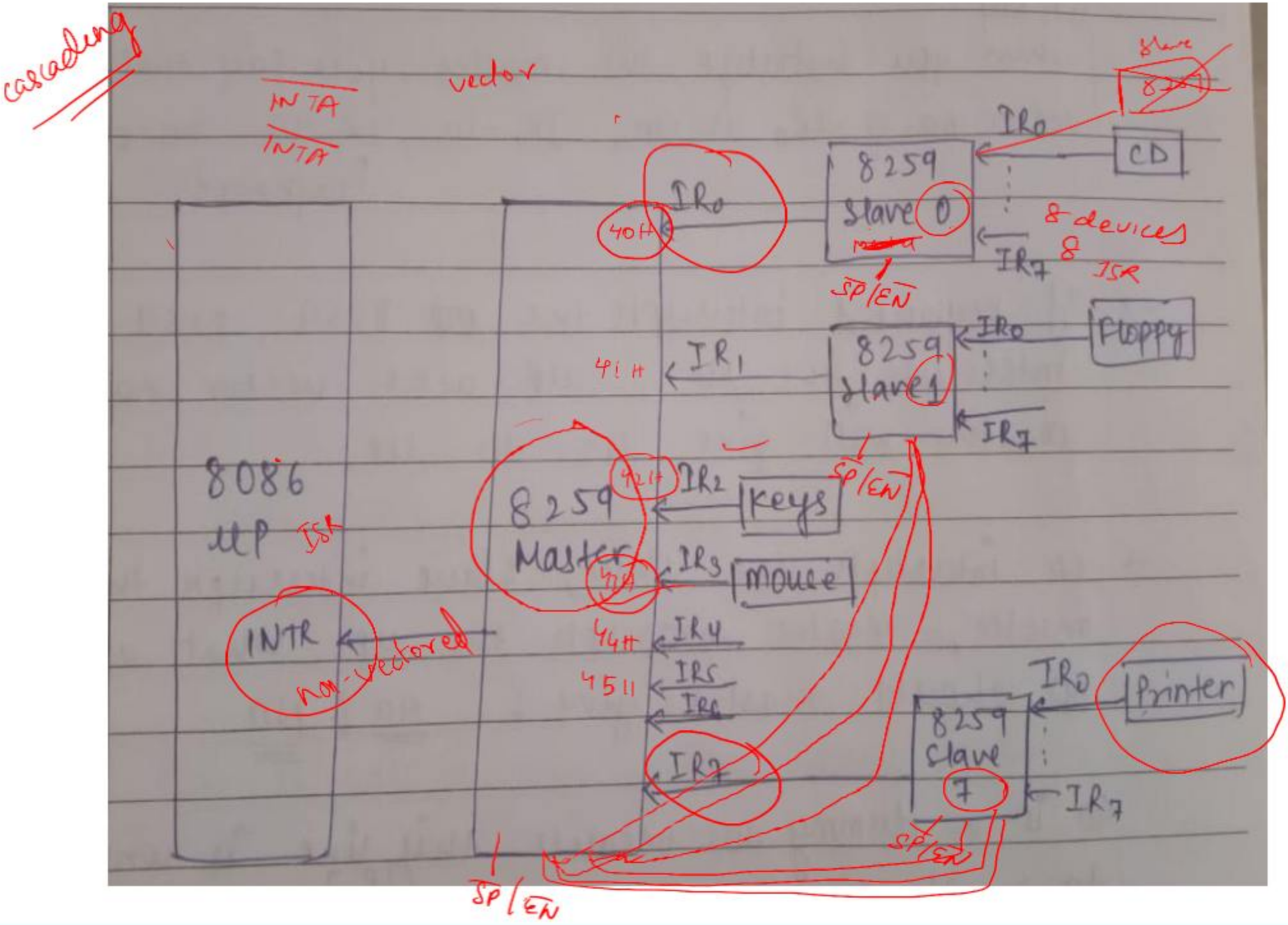




Priority Resolver




IR
2 level
IR3
IR5
IR2
IRR
INSR
IR1
EOI command
8259
forward
IR3
ACK
INTA
8259
HDD
CA
8259
IR5
EOI
IR5
IR7


cascading
INTA
INTA
vector
8086
up
ISR
INTR
Non-vectored
8259
Master
40H
41H
42H
43H
44H
45H
IR0
IR1
IR2
IR3
IR4
IR5
IR6
IR7
Keys
mouse
SP/EN
8259
Slave 0
IR0
IR7
CD
8 devices
& ISR
8259
Slave 1
IR0
IR7
Floppy
8259
Slave
7
IR0
IR7
Printer

① Initialize 8259

↓

vector no

② →

③ master → lines - slaves

④ slave → identification

$\overline{INTA}$ → asking for vector no

$\overline{INTA}$

Interfacing of 8259 with 8086 in max min

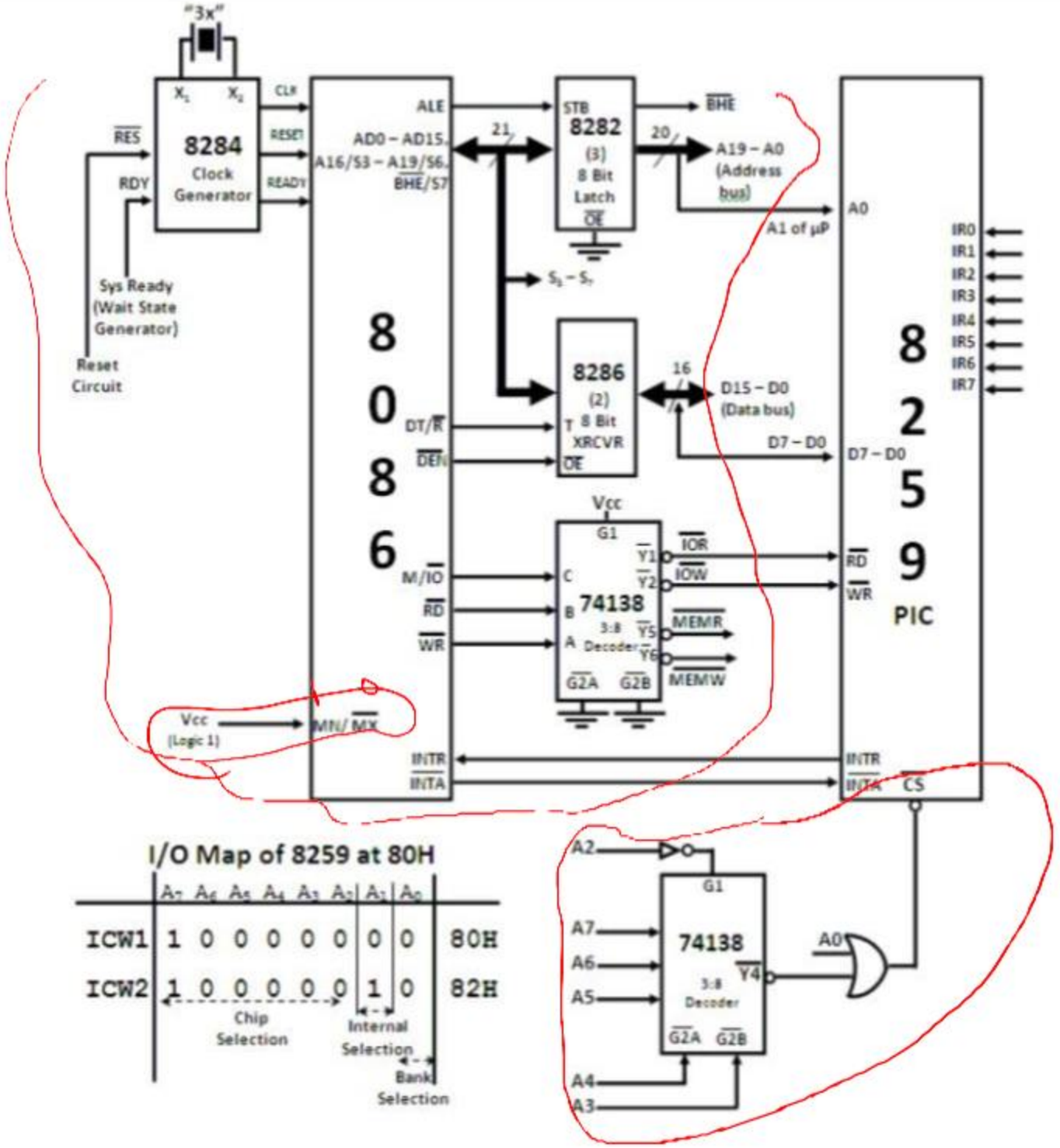
8257 → DMA → m/y → 8255 → 8259

8259 ICW & OCW

- Initialize
- Operational

ICW1
ICW2
ICW3
ICW4

OCW1
OCW2


"3x"
8284
Clock Generator
RES
RDY
Sys Ready
(Wait State Generator)
Reset Circuit
8086
8282
(3) 8 Bit Latch
8286
(2) 8 Bit XRCVR
74138
3:8 Decoder
8259
PIC
ALE
AD0 – AD15
A16/S3 – A19/S6
BHE/S7
A19 – A0 (Address bus)
A1 of µP
D15 – D0 (Data bus)
D7 – D0
IOR
IOW
MEMR
MEMW
INTR
INTA
IR0
IR1
IR2
IR3
IR4
IR5
IR6
IR7
CS
Vcc
(Logic 1)
MN/MX
I/O Map of 8259 at 80H
ICW1 1 0 0 0 0 0 0 0 80H
ICW2 1 0 0 0 0 0 1 0 82H
Chip Selection
Internal Selection
Bank Selection
A2
A7
A6
A5
A4
A3
A0
Y4

Thank you