MICROPROCESSORS

8086 IN MINIMUM MODE

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OBJECTIVE

1. To understand the fu ctioning f 8086 in minimum mode.

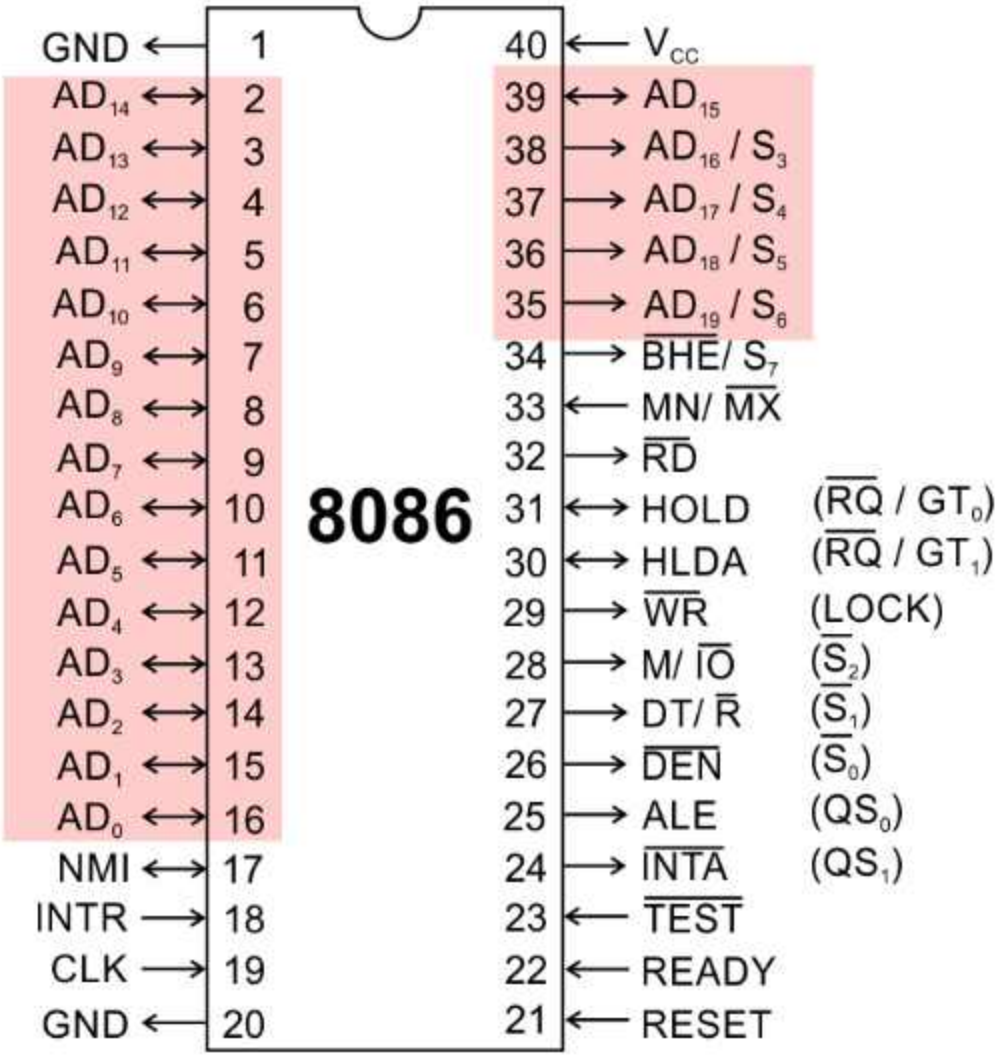
2. To understand the timing diagrams for Read and Write operations in minimum mode.

01 Demultiplexing of Address and Data Bus

02 Functioning in Minimum Mode

03 Timing diagrams for Read and Write operations in minimum mode

Address/Data Multiplexing



AD_0-AD_{15} (Bidirectional)

Address/Data bus

Low order address bus; these are multiplexed with data.

When AD lines are used to transmit memory address the symbol A is used instead of AD, for example A_0-A_{15}.

When data are transmitted over AD lines the symbol D is used in place of AD, for example D_0-D_7, D_8-D_{15} or D_0-D_{15}.

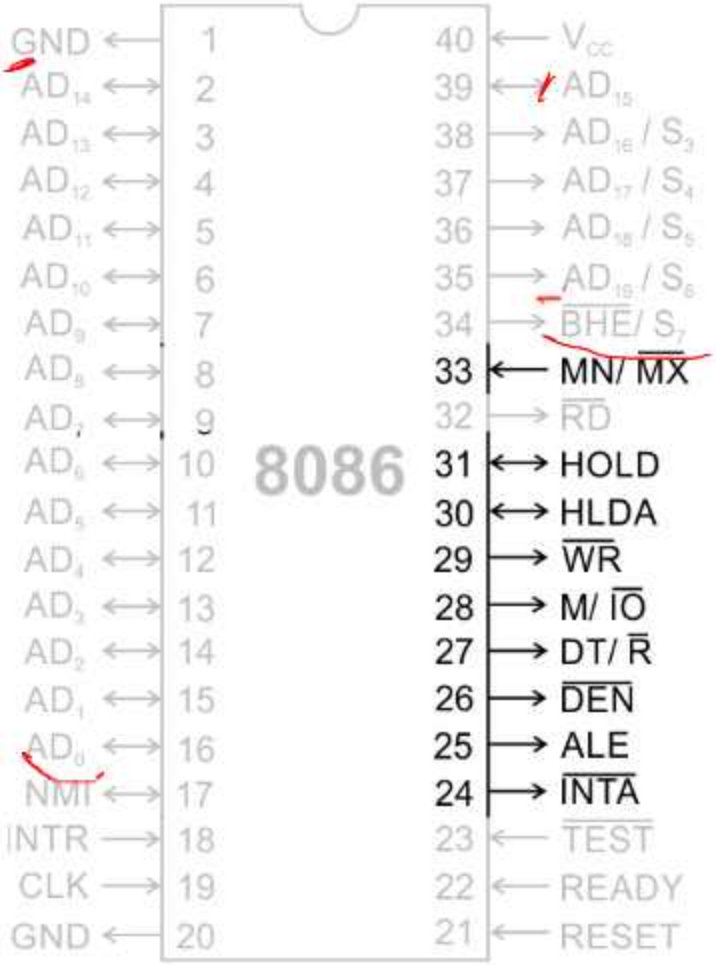
A_{16}/S_3, A_{17}/S_4, A_{18}/S_5, A_{19}/S_6

High order address bus. These are multiplexed with status signals

Min/ Max Pins

8086 in minimum mode

$AD_0 - AD_{19} \Rightarrow 20$ pins
$+ \ 1$
21 pins



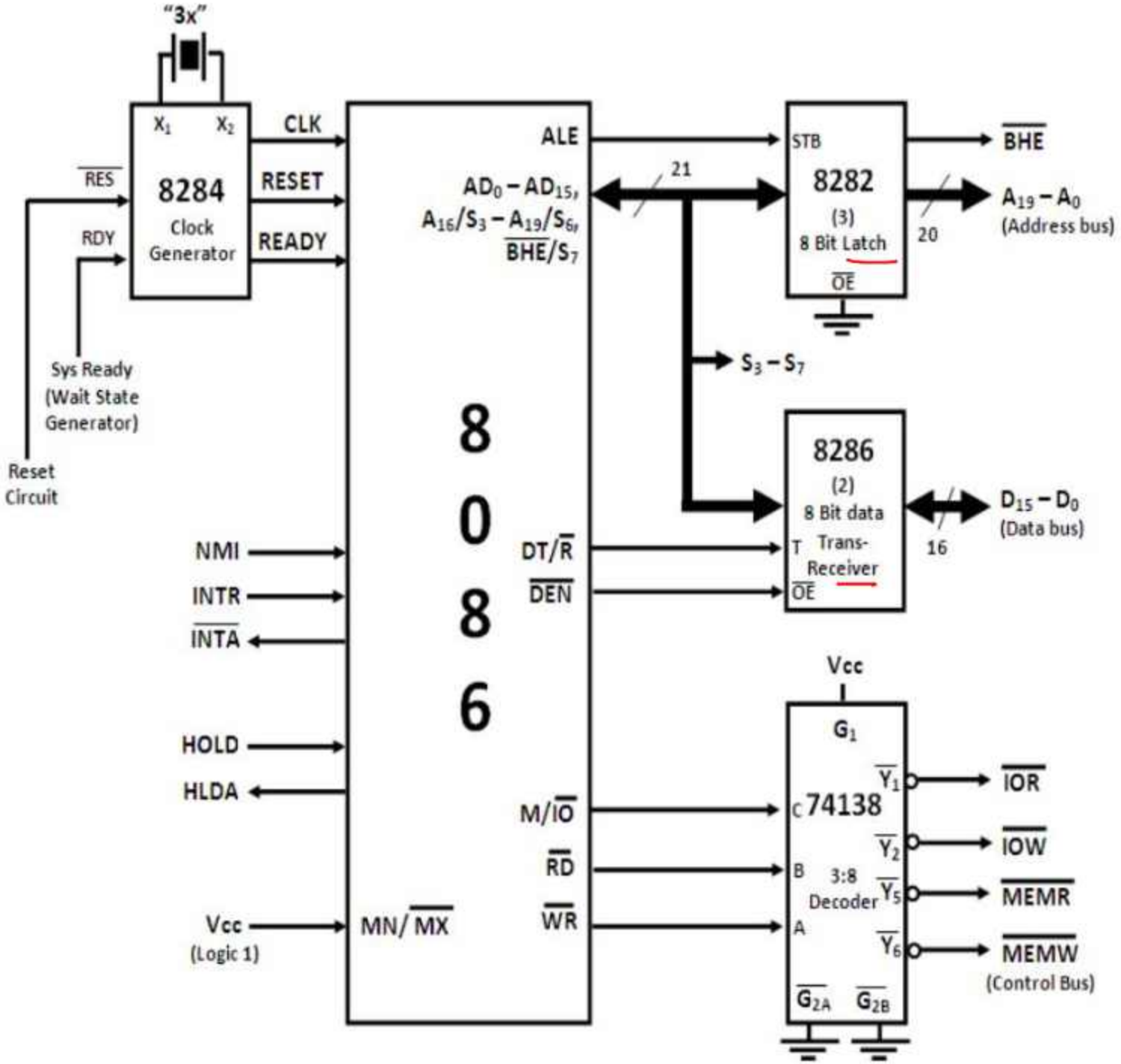
The 8086 microprocesso. can work in two modes of operations : Minimum mode and Maximum mode

In the minimum mode of operation the microprocessor do not associate with any co-processors and can not be used for multiprocessor systems.

In the maximum mode the 8086 can work in multi-processor or co-processor configuration.

Minimum or maximum mode operations are decided by the pin MN/ MX(Active low).

When this pin is high 8086 operates in minimum mode otherwise it operates in Maximum mode.


"3x"
X1
X2
8284
Clock
Generator
CLK
RESET
READY
RES
RDY
Sys Ready
(Wait State
Generator)
Reset
Circuit
8
0
8
6
ALE
AD0 – AD15,
A16/S3 – A19/S6,
BHE/S7
NMI
INTR
INTA
HOLD
HLDA
Vcc
(Logic 1)
MN/MX
DT/R
DEN
M/IO
RD
WR
21
STB
8282
(3)
8 Bit Latch
OE
BHE
A19 – A0
(Address bus)
20
S3 – S7
8286
(2)
8 Bit data
T Trans-
Receiver
OE
16
D15 – D0
(Data bus)
Vcc
G1
C 74138
B
A
3:8
Decoder
Y1
Y2
Y5
Y6
G2A
G2B
IOR
IOW
MEMR
MEMW
(Control Bus)

Multiplexing and demultiplexing of address/data bus

40 pin package

16 bits — 4 bit

$AD_0 - AD_{15}$ — $AD_{16} - A_{19}$

$AD_0 - AD_{19}$ & $\overline{BHE}$ → 21 pins

8085 — data 8 bit, address 16 bit, 8 pins

data → 16 bit address

$A_{16} - A_{19}$ status $S_3 - S_6$

$\overline{BHE}$ — S_7

$AD_{19} - AD_0$

$A_{19} - A_{16}$ (4 pins) → $S_6 - S_3$

$A_{15} - A_0$ (16 pins) — $D_{15} - D_0$ (16 pins)

$A_0 - A_{15}$

20 bit

S_6 → bus master

$S_5 = 0$ → IF = 0

$S_5 = 1$ → IF = 1

S_4	S_3	
0	0	Extra
0	1	Stack
1	0	Code
1	1	Data

minimum → 8086 → bus master

DMA – peripheral

maximum

bus master

$AD_0 - A_{19}$ → addrm, data & status

bus → data ? addrss ?

ALE

ALE = 1 ⇒ address

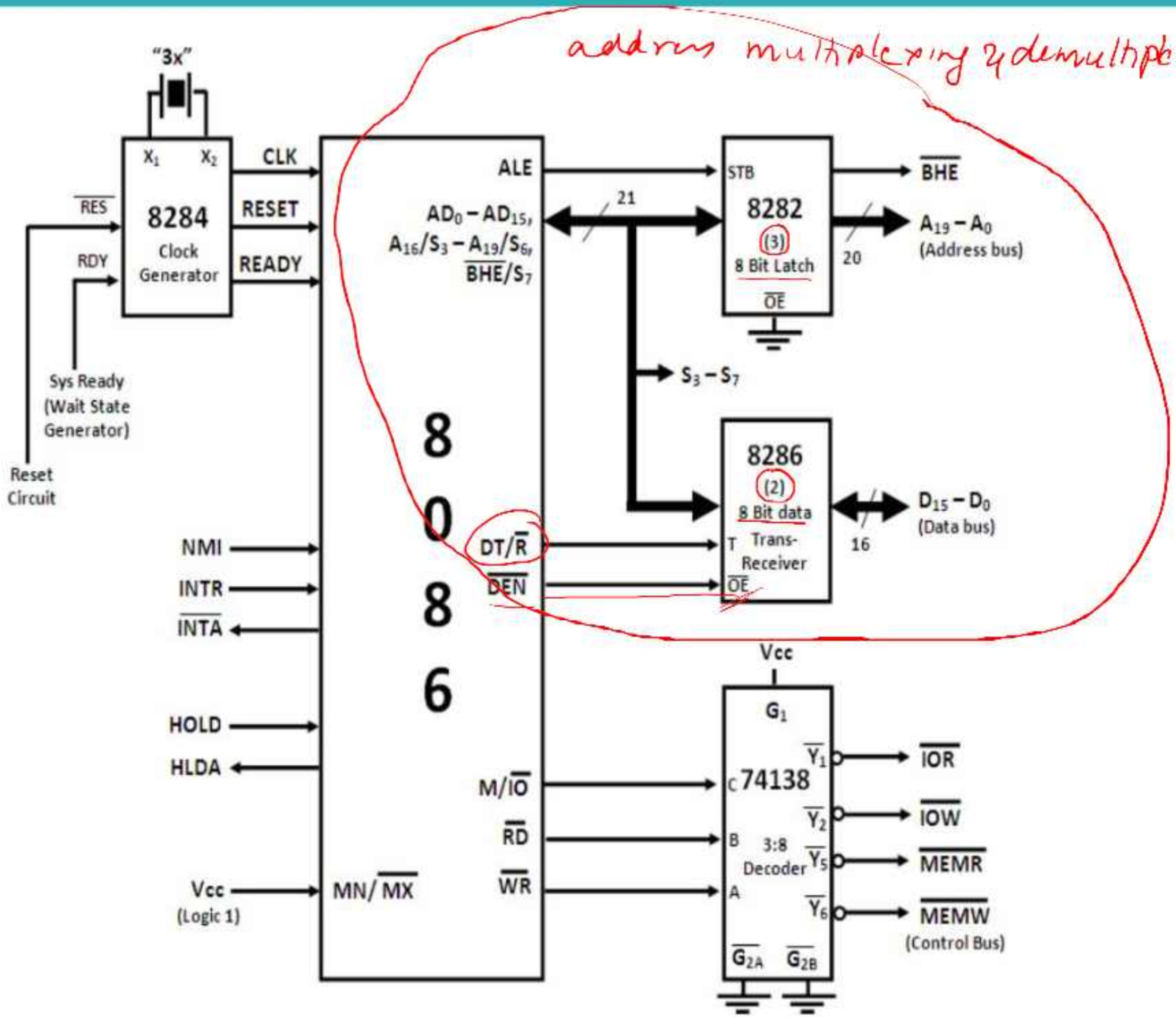
ALE = 0 ⇒ data

multiplexing

demultiplexing

① 8282 ⇒ Latch

② 8286 ⇒ trans receiver


address multiplexing & demultiplexing
"3x"
X1
X2
8284
Clock Generator
CLK
RESET
READY
RES
RDY
Sys Ready (Wait State Generator)
Reset Circuit
8086
ALE
AD0 – AD15,
A16/S3 – A19/S6,
BHE/S7
NMI
INTR
INTA
HOLD
HLDA
Vcc (Logic 1)
MN/MX
DT/R
DEN
M/IO
RD
WR
21
STB
8282
(3)
8 Bit Latch
OE
20
BHE
A19 – A0
(Address bus)
S3 – S7
8286
(2)
8 Bit data
T Trans-
Receiver
OE
16
D15 – D0
(Data bus)
Vcc
G1
C 74138
B
A
3:8
Decoder
Y1
Y2
Y5
Y6
G2A
G2B
IOR
IOW
MEMR
MEMW
(Control Bus)

8282 → latch

bus → ALE=0 ← data
ALE=1 ← address

latch

Pc remote

29

bus

30

ALE=0

1 → A0 – A19 & BHE

ALE

$AD_0 - AD_{15}$,
$A_{16}/S_3 - A_{19}/S_6$,
$\overline{BHE}/S_7$

40

21

STB

8282
(3)
8 Bit Latch

OE

$\overline{BHE}$

$A_{19} - A_0$
(Address bus)

20

D_0-D_{15}
S_3-S_7

permanently grounded

STB – Strobe
$\overline{OE}$ – Output Enable

$S_3 - S_7$

ALE=1

8
0
8

8286
(2)
8 Bit data
Trans-
Receiver

T

$\overline{OE}$

16

$D_{15} - D_0$
(Data bus)

DT/$\overline{R}$

$\overline{DEN}$

ALE=1
$\overline{DEN}$=1

ALE=0
$\overline{DEN}$=0

STB=0

DT/$\overline{R}$=1 → T=1 ⇒ transmit
DT/$\overline{R}$=0 → T=0 ⇒ receive

ALE=1
$\overline{DEN}$=1

ALE=0
$\overline{DEN}$=0

ALE=1
$\overline{DEN}$=1
↓
active low

ALE = 1 ⇒ bus address ⇒ STB = 1 ⇒ address will get latched in 8282

$\overline{OE}$ → permanently grounded

⇒ continuously A0 – A19 & $\overline{BHE}$

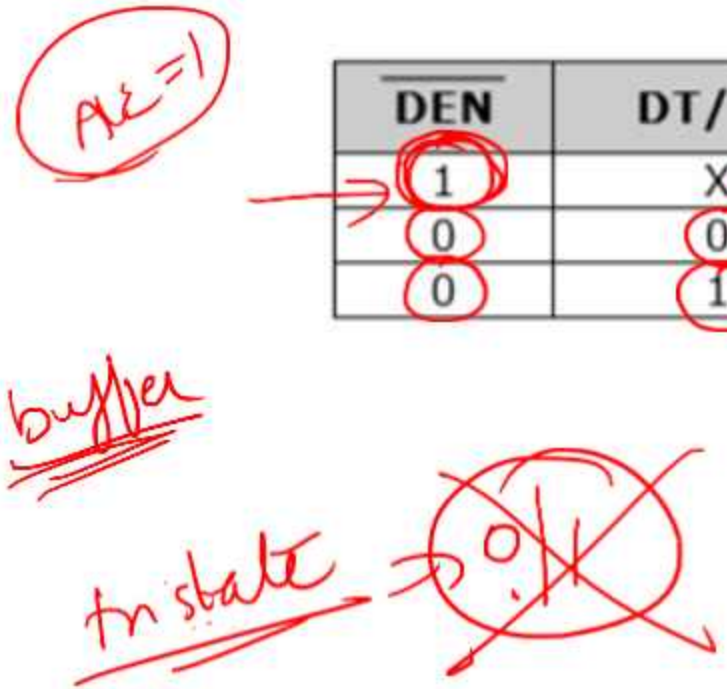
bus address ⇒ will not go transreceiver ↓ $\overline{DEN}$ = 1

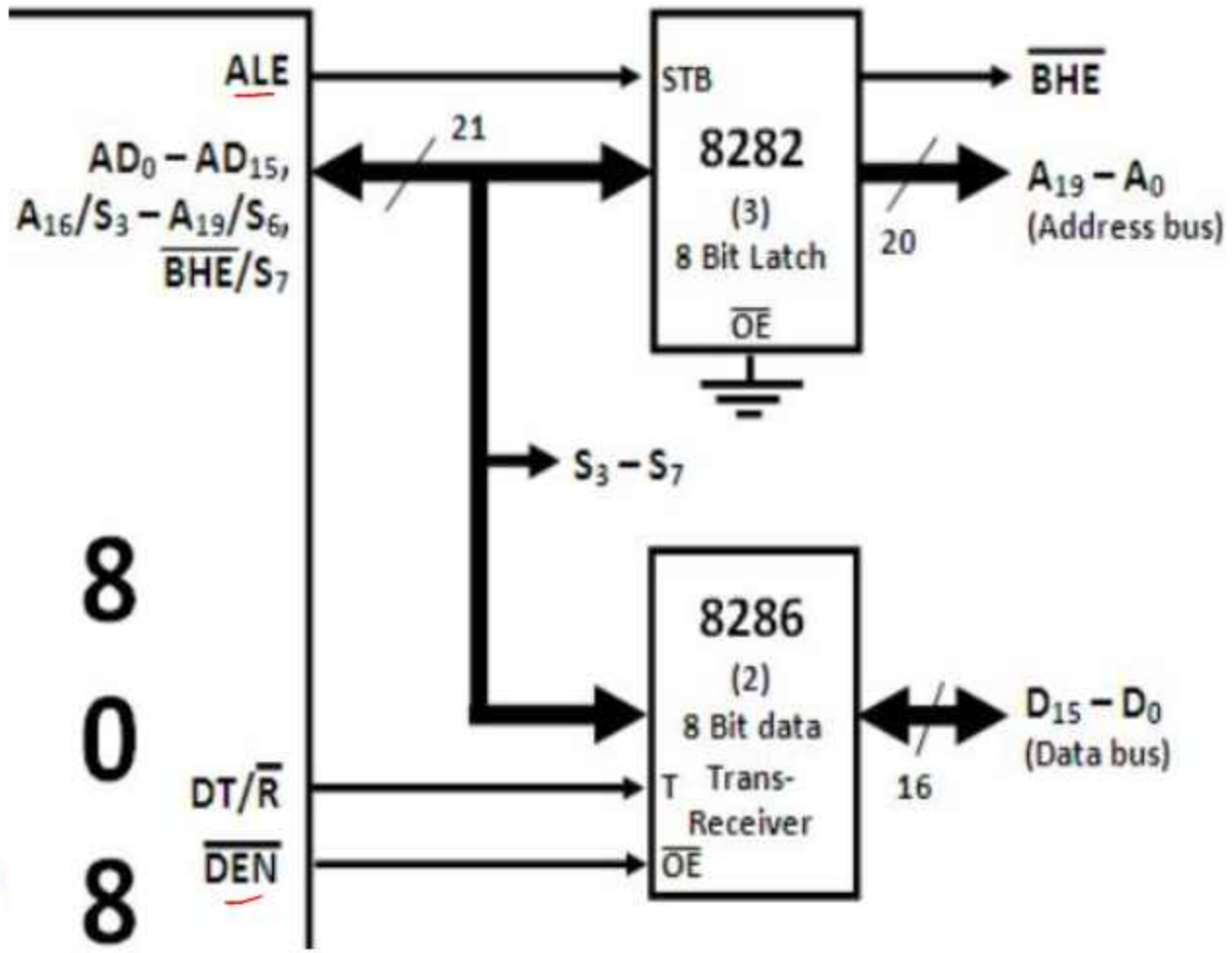
ALE = 0 ⇒ bus data ⇒ $\overline{DEN}$ = 0 → transreceiver ↓ DT/$\overline{R}$

bus data ⇒ will not go latch ⇒ STB = 0

DT/$\overline{R}$ ↓ (T) pin 0 → receiver, 1 → transmitter

$\overline{DEN}$	DT/ $\overline{R}$	Action
1	X	Transreceiver is disabled
0	0	Receive data
0	1	Transmit data





similar

ALE = 1
DEN = 1

ALE = 1
address

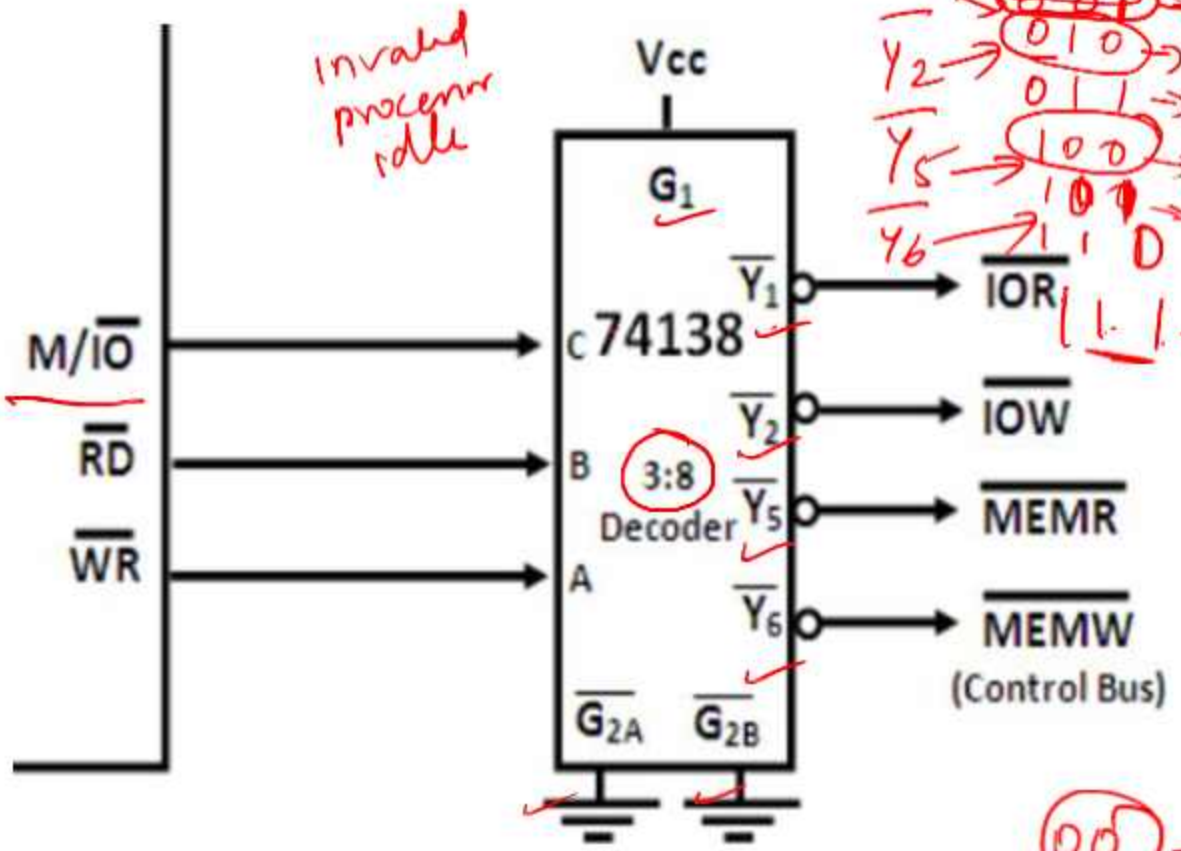
ALE = 0
DEN = 0

= 0 data = 0
DEN, bus, ALE
addrs

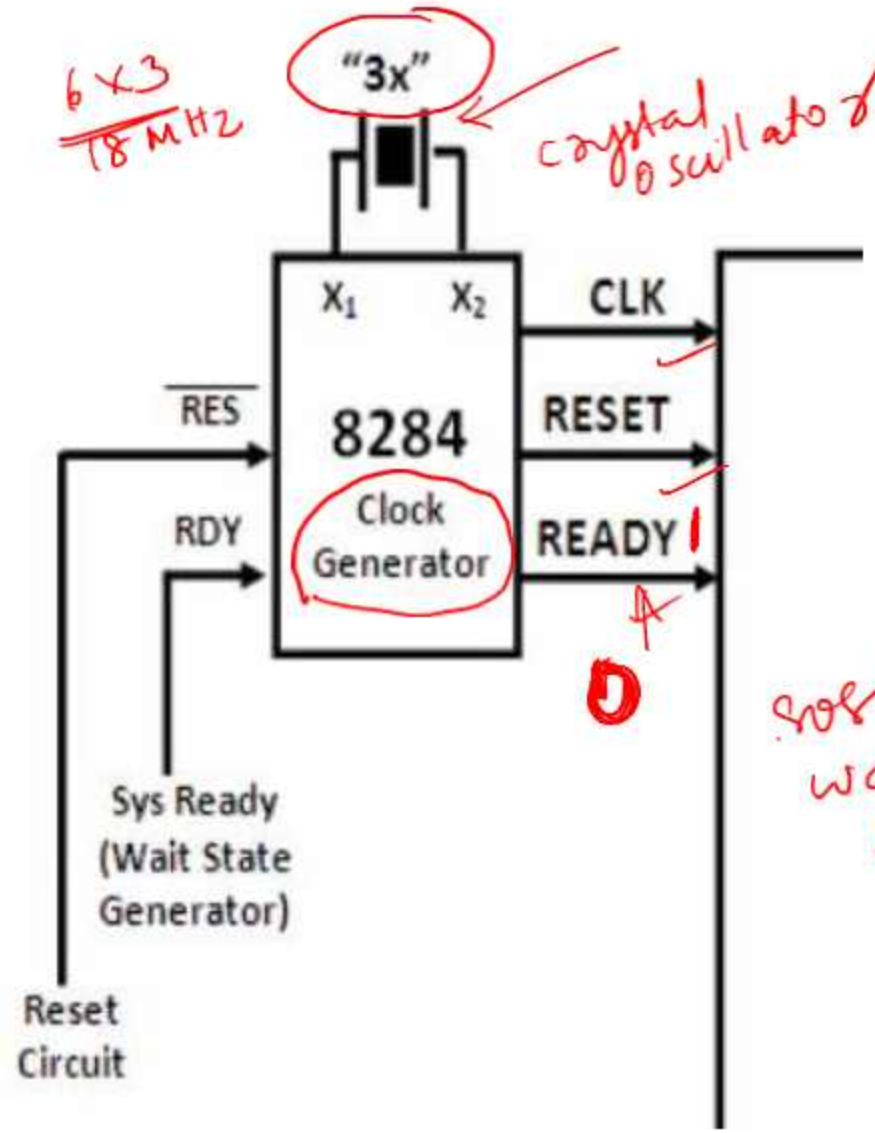
1) ALE = 0
2) data ⇒ bus
3) DEN = 0

ALE = 0

DEN = 1



M/ $\overline{IO}$	$\overline{RD}$	$\overline{WR}$	Action
1	0	1	Memory Read
1	1	0	Memory Write
0	0	1	I/O Read
0	1	0	I/O Write

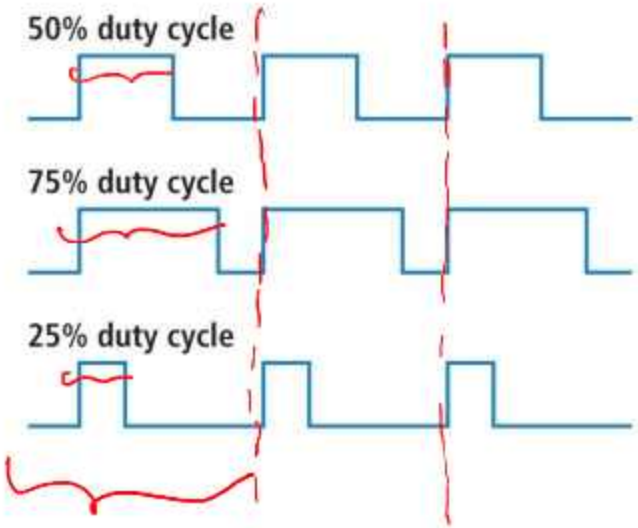


8086 up
6 MHz
with
33 %.
duty
cycle

6 x 3
18 MHz

crystal oscillator

8086
wait
state



50% duty cycle

75% duty cycle

25% duty cycle

50 MHz

33% duty cycle

70%

50%

90%

time period

$$\text{duty cycle} = \frac{\text{high time}}{\text{total period}} = \frac{\text{ON time}}{\text{total period}}$$

20%

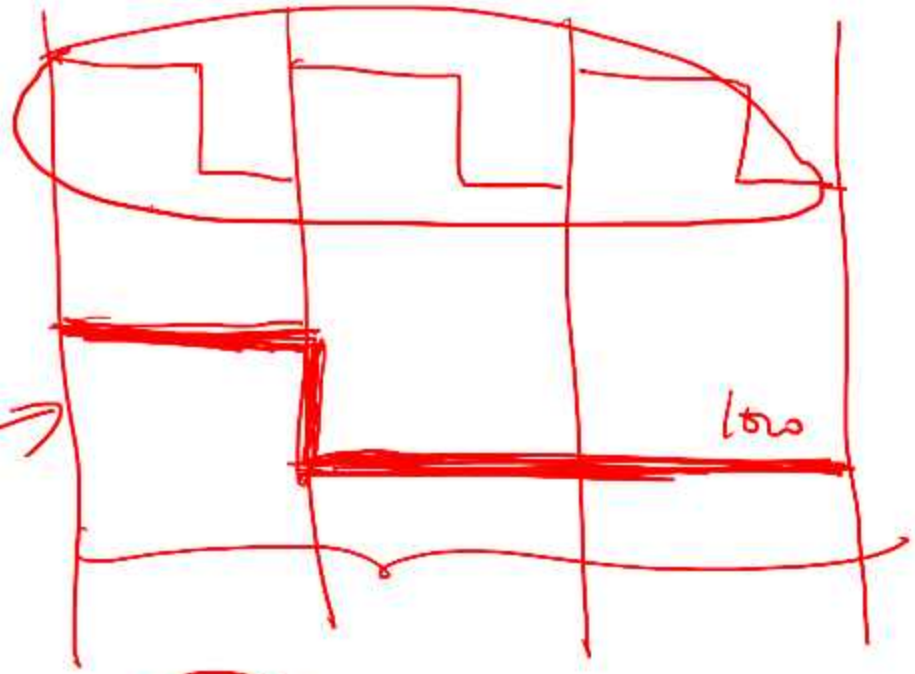
18 MHz

↓

6 MHz

3 pulses with random duty cycle

80%

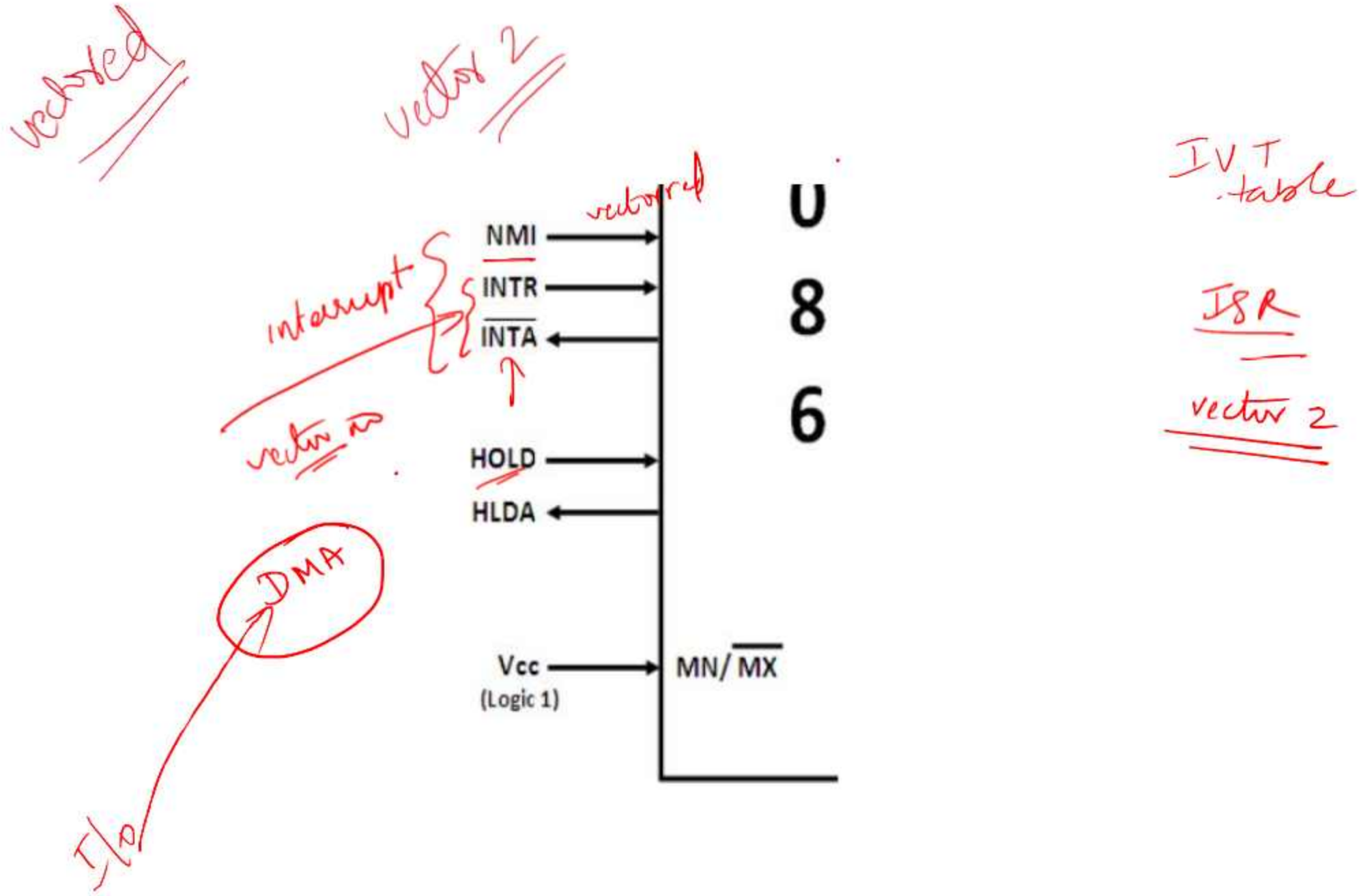


33% duty →

1 0 1 0

1/3

1/3


vectored
vector 2
interrupt
vector no
NMI
INTR
INTA
HOLD
HLDA
Vcc
(Logic 1)
MN/ MX
8086
DMA
I/O
IVT
table
ISR
vector 2

bus cycle / machine cycle

→ mly or I/O

mly read
mly write
I/O read
I/O write

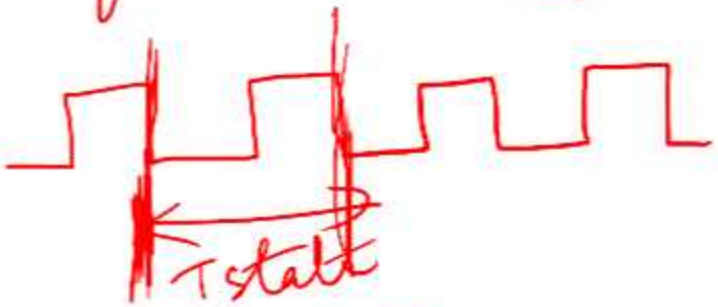
MEMR IOR
MEMW IOW

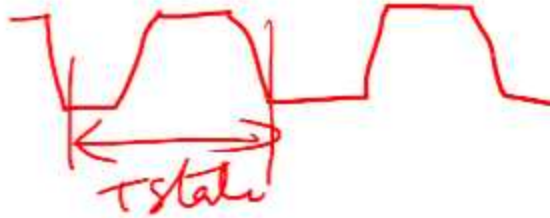
Instruction cycle & machine cycle.

One or more mc cycle

Fetch
Decode
Execute

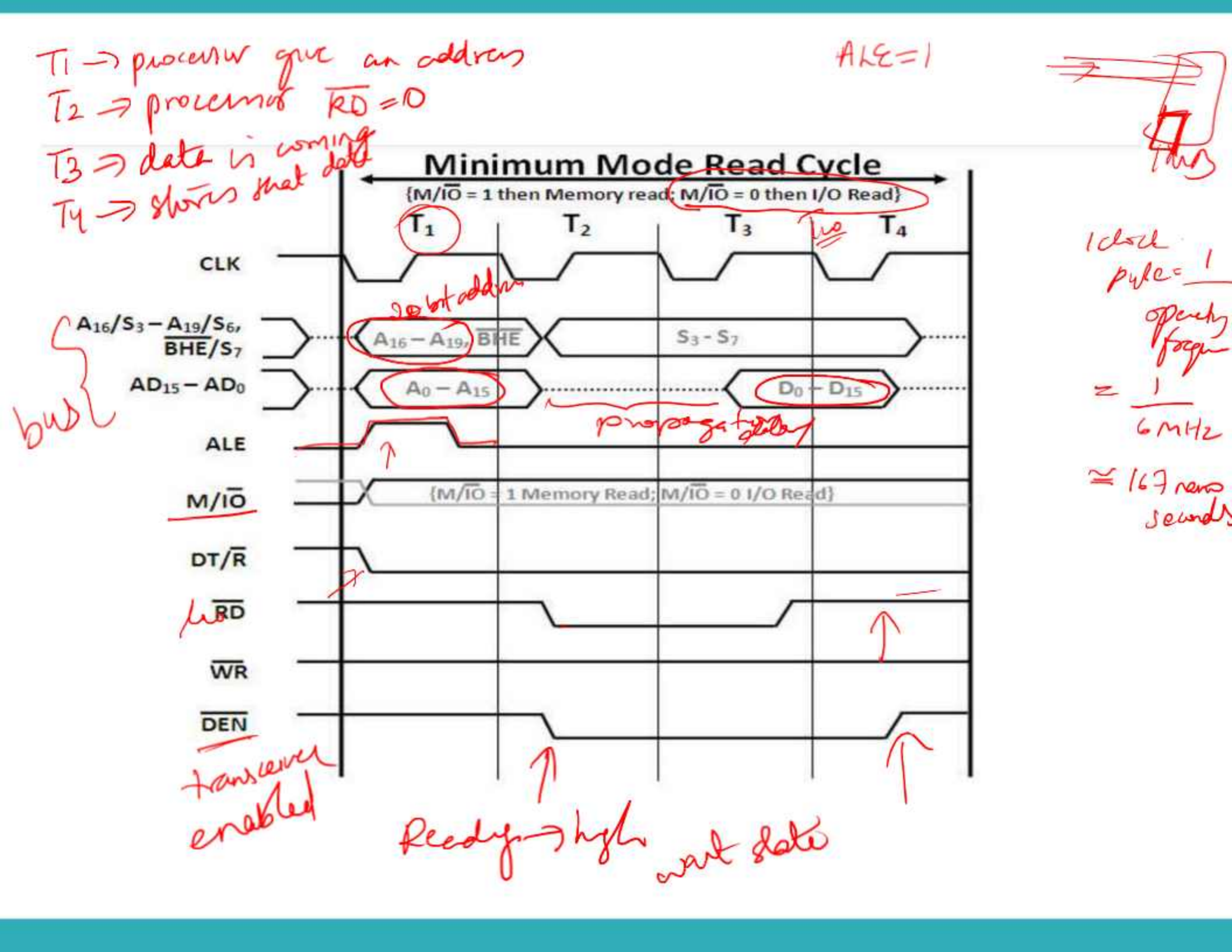
T-state

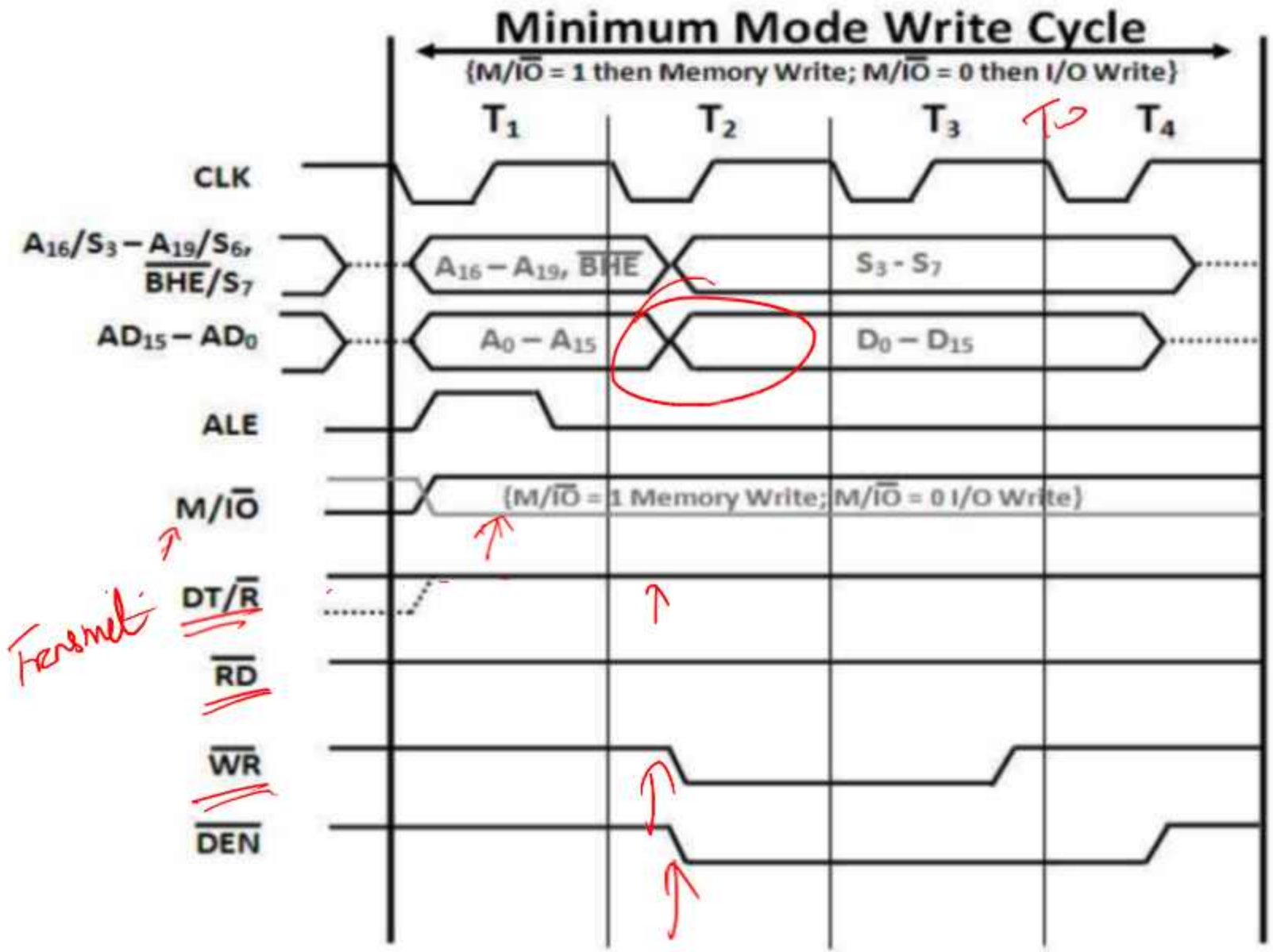




8085 MP → clock period

T1 T2 T3 and T4


Minimum Mode Read Cycle
{M/IO = 1 then Memory read; M/IO = 0 then I/O Read}
T1
T2
T3
Tw
T4
CLK
A16/S3 – A19/S6, BHE/S7
AD15 – AD0
ALE
M/IO
DT/R
RD
WR
DEN
A16 – A19, BHE
S3 - S7
A0 – A15
D0 – D15
{M/IO = 1 Memory Read; M/IO = 0 I/O Read}
T1 → processor give an address
T2 → processor RD = 0
T3 → data is coming
T4 → shows that data
ALE=1
bus
transceiver enabled
Ready → high
wait state
1 clock pulse = 1 / operating frequency
= 1 / 6 MHz
≅ 167 nano seconds


Minimum Mode Write Cycle
{M/IO = 1 then Memory Write; M/IO = 0 then I/O Write}
T1
T2
T3
T4
CLK
A16/S3 – A19/S6, BHE/S7
A16 – A19, BHE
S3 - S7
AD15 – AD0
A0 – A15
D0 – D15
ALE
M/IO
{M/IO = 1 Memory Write; M/IO = 0 I/O Write}
DT/R
RD
WR
DEN

Thank you