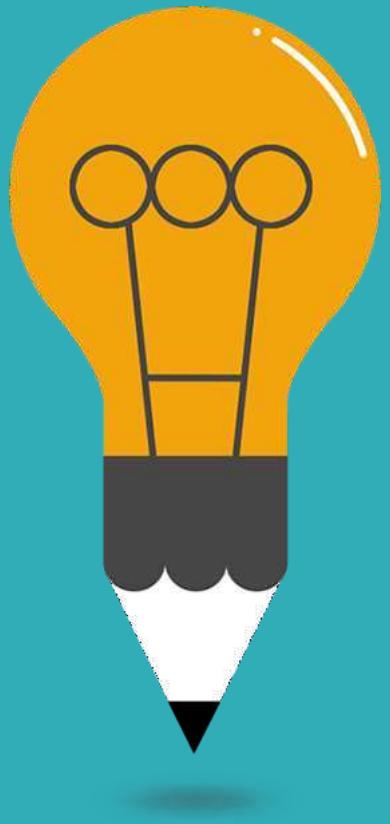


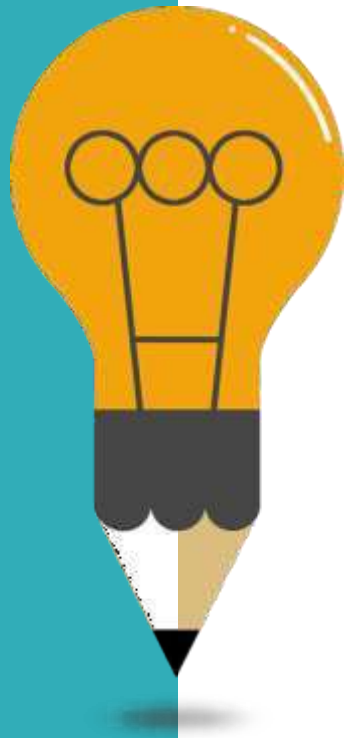
MICROPROCESSORS

INTRODUCTION

PROF.POONAM PANGARKAR , ASSISTANT PROFESSOR ,CSE DATA SCIENCE,APSIT THANE

OBJECTIVE

1. Understand why the subject microprocessor is important.
2. Understand the basic concepts of a microprocessor.



01 COURSE OBJECTIVES

02 COURSE OUTCOMES

03 SYLLABUS AND REFERENCE

04 INTRODUCTION

COURSE OBJECTIVES

1. To equip students with the fundamental knowledge and basic technical competence in the field of Microprocessors.
2. To emphasize on instruction set and logic to build assembly language programs.
3. To prepare students for higher processor architectures and embedded systems

COURSE OUTCOMES

The student will be able to:

1. Describe core concepts of 8086 microprocessor.
2. Interpret the instructions of 8086 and write assembly and Mixed language programs.
3. Identify the specifications of peripheral chip.
4. Design 8086 based system using memory and peripheral chips.
5. Appraise the architecture of advanced processors.
6. Understand hyperthreading technology

1 CHAPTER 1 The Intel Microprocessor 8086 Architecture

2 CHAPTER 2: Instruction Set and Programming

3 CHAPTER 3: Memory and Peripherals Interfacing

4 CHAPTER 4: Intel 80386DX Processor

5 CHAPTER 5: Pentium Processor

6 CHAPTER 6: Pentium 4

- SYLLABUS

Module	Detailed Contents		Hours
1	**The Intel Microprocessors 8086 Architecture**		8
	1.1	8086CPU Architecture,	
	1.2	Programmer's Model	
	1.3	Functional Pin Diagram	
	1.4	Memory Segmentation	
	1.5	Banking in 8086	
	1.6	Demultiplexing of Address/Data bus	
	1.7	Functioning of 8086 in Minimum mode and Maximum mode	
	1.8	Timing diagrams for Read and Write operations in minimum and maximum mode	
	1.9	Interrupt structure and its servicing	
2	**Instruction Set and Programming**		**6**
	2.1	Addressing Modes	
	2.2	Instruction set-Data Transfer Instructions, String Instructions, Logical Instructions, Arithmetic Instructions, Transfer of Control Instructions, Processor Control Instructions	
	2.3	Assembler Directives and Assembly Language Programming, Macros, Procedures	

3	**Memory and Peripherals interfacing**		**8**
	3.1	Memory Interfacing - RAM and ROM Decoding Techniques – Partial and Absolute	
	3.2	8255-PPI-Block diagram, CWR, operating modes, interfacing with 8086.	
	3.3	8257-DMAC-Block diagram, DMA operations and transfer modes.	
	3.4	Programmable Interrupt Controller 8259-Block Diagram, Interfacing the 8259 in single and cascaded mode.	
4	**Intel 80386DX Processor**		**7**
	4.1	Architecture of 80386 microprocessor	
	4.2	80386 registers–General purpose Registers, EFLAGS and Control registers	
	4.3	Real mode, Protected mode, virtual 8086 mode	
	4.4	80386 memory management in Protected Mode – Descriptors and selectors, descriptor tables, the memory paging mechanism	

5	**Pentium Processor**		**6**
	5.1	Pentium Architecture	
	5.2	Superscalar Operation,	
	5.3	Integer &Floating-Point Pipeline Stages,	
	5.4	Branch Prediction Logic,	
	5.5	Cache Organization and	
	5.6	MESI protocol	
6	**Pentium 4**		**4**
	6.1	Comparative study of 8086, 80386, Pentium I, Pentium II and Pentium III	
	6.2	Pentium 4: Net burst micro architecture.	
	6.3	Instruction translation look aside buffer and branch prediction	
	6.4	Hyper threading technology and its use in Pentium 4	

ASSESSMENT AND USEFUL LINKS

Assessment:	
Internal Assessment Test:	
Assessment consists of two class tests of 20 marks each. The first class test is to be conducted when approx. 40% syllabus is completed and second class test when additional 40% syllabus is completed. Duration of each test shall be one hour.	
End Semester Theory Examination:	
1	Question paper will comprise of 6 questions, each carrying 20 marks.
2	The students need to solve total 4 questions.
3	Question No.1 will be compulsory and based on entire syllabus.
4	Remaining question (Q.2 to Q.6) will be selected from all the modules.

Useful Links	
1	https://swayam.gov.in/nd1_noc20_ee11/preview
2	https://nptel.ac.in/courses/108/105/108105102/
3	https://www.classcentral.com/course/swayam-microprocessors-and-microcontrollers-9894
4	https://www.mooc-list.com/tags/microprocessors

REFERENCE TEXT BOOKS

Textbooks:	
1	John Uffenbeck, "8086/8088 family: Design Programming and Interfacing", PHI.
2	Yu-Cheng Liu, Glenn A. Gibson, "Microcomputer System: The 8086/8088 Family, Architecture, Programming and Design", Prentice Hall
3	Walter A. Triebel, "The 80386DX Microprocessor: hardware, Software and Interfacing", Prentice Hall
4	Tom Shanley and Don Anderson, "Pentium Processor System Architecture", Addison-Wesley.
5	K. M. Bhurchandani and A. K. Ray, "Advanced Microprocessors and Peripherals", McGraw Hill
References:	
1	Barry B. Brey, "Intel Microprocessors", 8th Edition, Pearson Education India
2	Douglas Hall, "Microprocessor and Interfacing", Tata McGraw Hill.
3	Intel Manual
4	Peter Abel, "IBM PC Assembly language and Programming", 5th Edition, PHI
5	James Antonakons, "The Pentium Microprocessor", Pearson Education

Sr. No.	Title of Experiments
1	Use of programming tools (Debug/TASM/MASM/8086kit) to perform basic arithmetic operations on 8-bit/16-bit data
2	Code conversion (Hex to BCD and BCD to Hex)/ (ASCII to BCD and BCD to ASCII)
3	Assembly programming for 16-bit addition, subtraction, multiplication and division (menu based)
4	Assembly program based on string instructions (overlapping/non-overlapping block transfer/ string search/ string length)
5	Assembly program to display the contents of the flag register.
6	Any Mixed Language programs.
7	Assembly program to find the GCD/ LCM of two numbers
8	Assembly program to sort numbers in ascending/ descending order
9	Any program using INT 10H
10	Assembly program to find minimum/ maximum number from a given array.
11	Assembly Program to display a message in different color with blinking
12	Assembly program using procedure.
13	Assembly program using macro.
14	Program and interfacing using 8255.
15	Program and interfacing of ADC/ DAC/ Stepper motor.

Evolution of Microprocessor

The interconnections (known as Interfacing) between the 5 units of computer system is carried by 3 basic buses i) Address Bus ii) Data Bus iii) Control Bus. A bus(from the Latin *omnibus*, meaning "for all") is essentially a set of wires which is used in computer system to carry information of the same logical functionality. The function of the 3 buses is

- ✓ The **address bus** selects memory location or an I/O device for the CPU.
- ✓ The **data bus** transfers information between the microprocessor and its memory or I/O device. Data transfer can vary in size, from 8-bits wide to 64 bits wide in various members of microprocessors.
- ✓ The **Control bus** generates command signals to synchronize the CPU operation with IO and Memory devices.

Evolution of Microprocessor

Processor	Date of Launch	Clock speed	Data Bus Width	Adress Bus	Addressable Memory Size
4004	1971	740 Khz	4 bit	12	4 KB
8-BIT PROCESSOR					
8008	1972	800 Khz	8 bit	14	16 Kb
8080	1974	2 Mhz	8 bit	16	64 kb
8085	1976	3 Mhz	8 bit	16	64 kb
16-BIT PROCESSOR					
8086	1978	5 Mhz	16	20	1M
80286	1982	16 Mhz	16	24	16 M

Processor	Date of Launch	Clock speed	Data Bus Width	Address Bus	Addressable Memory Size
32-BIT PROCESSOR					
80386	1985	33 Mhz	32	32	4 G
80486	1989	40 Mhz	32	32	4G+ 8k cache
Pentium I	1993	100 Mhz	32	32	4G+16k cache
Pentium II	1997	233 Mhz	32	32	4G+16k cache + L2 256 Cache
Pentium III	1999	1.4 Ghz	32	32	4G+32k cache + L2 256 Cache
Pentium IV	2000	2.66 Ghz	32 Internal 64 External	32	4G+32k cache + L2 256 Cache

64-BIT PROCESSOR					
Dual Core	2006	2.66 Ghz	64	36	64G+Independent L1 64 Kb+ Common L2 256 kb Cache
Core 2 Duo	2006	3 Ghz	64	36	64G+Independent L1 128 Kb+ Common L2 4 Mb Cache
I7	2008	3.33 Ghz	64	36	64G+Independent L1 64 Kb+ Common L2 256 kb Cache + 8 Mb L3 Cache

Microprocessor

Fifth Generation **Pentium**

Fourth Generation
During 1980s
Low power version of HMOS technology (HCMOS)
32 bit processors
Physical memory space 2^{24} bytes = 16 Mb
Virtual memory space 2^{40} bytes = 1 Tb
Floating point hardware
Supports increased number of addressing modes

Intel 80386

Third Generation
During 1978
HMOS technology ⇒ Faster speed, Higher packing density
16 bit processors ⇒ 40/ 48/ 64 pins
Easier to program
Dynamically relatable programs
Processor has multiply/ divide arithmetic hardware
More powerful interrupt handling capabilities
Flexible I/O port addressing

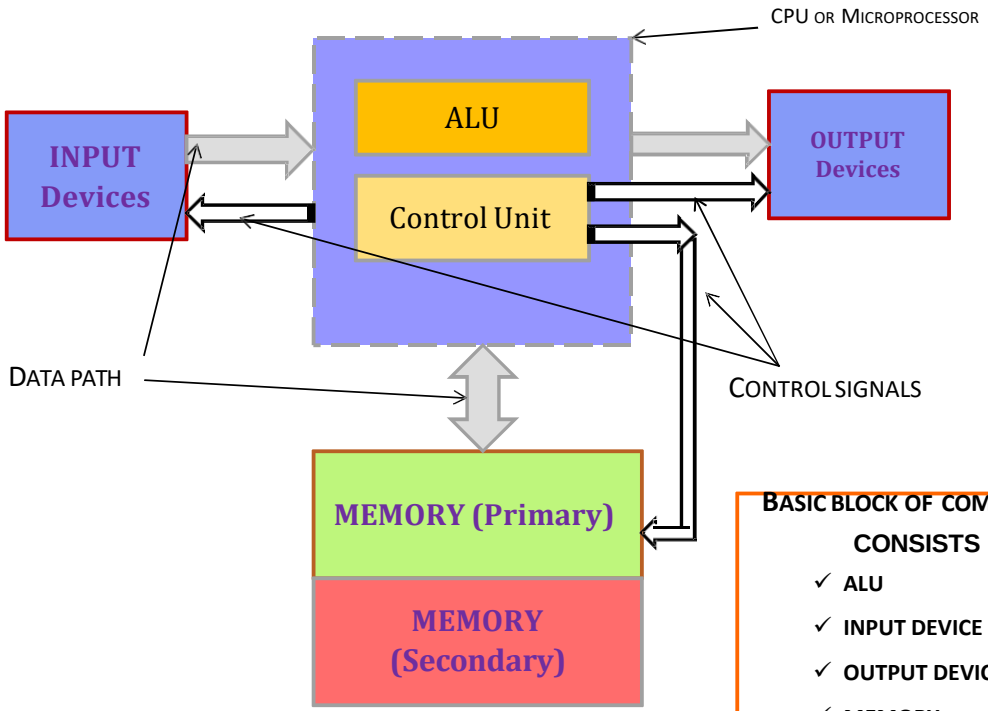
Intel 8086 (16 bit processor)

Second Generation
During 1973
NMOS technology ⇒ Faster speed, Higher density, Compatible with TTL
4 / 8/ 16 bit processors ⇒ 40 pins
Ability to address large memory spaces and I/O ports
Greater number of levels of subroutine nesting
Better interrupt handling capabilities

Intel 8085 (8 bit processor)

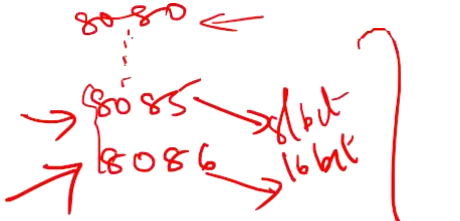
First Generation
Between 1971 – 1973
PMOS technology, non compatible with TTL
4 bit processors ⇒ 16 pins
8 and 16 bit processors ⇒ 40 pins
Due to limitations of pins, signals are multiplexed

LECTURE 1: BASIC BLOCK OF COMPUTER



BASIC BLOCK OF COMPUTERS CONSISTS

- ✓ ALU
- ✓ INPUT DEVICE
- ✓ OUTPUT DEVICE
- ✓ MEMORY
- ✓ CONTROL UNIT



8086

80186

80286

80386

80486

80586 → P1

P2

P3

P4

C2D → Core 2 Duo

i7/higher (core i7)

80x86 family.

x86 family.

multimedia &

Thank you