# CSC405 MICROPROCESSORS

## 8255 Programmable Peripheral Interface

# OBJECTIVE

1. To understand the block diagram and control word of 8255 –Programmable Peripheral Interface.

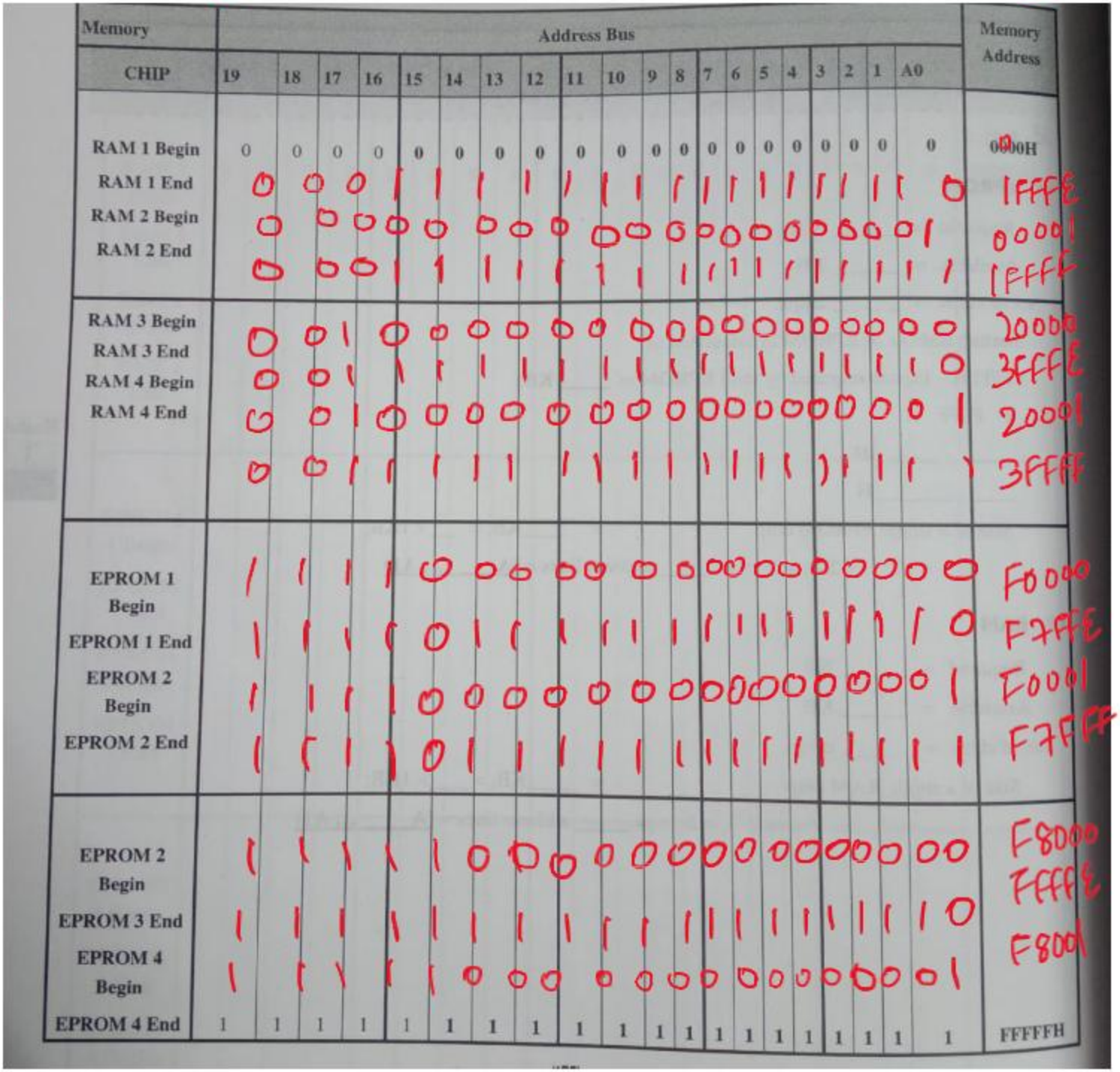
01

**8255 -** Programmable Peripheral Interface.

64 KB EPROM using 16 KB chips  256 KB ram using 64 KB chips

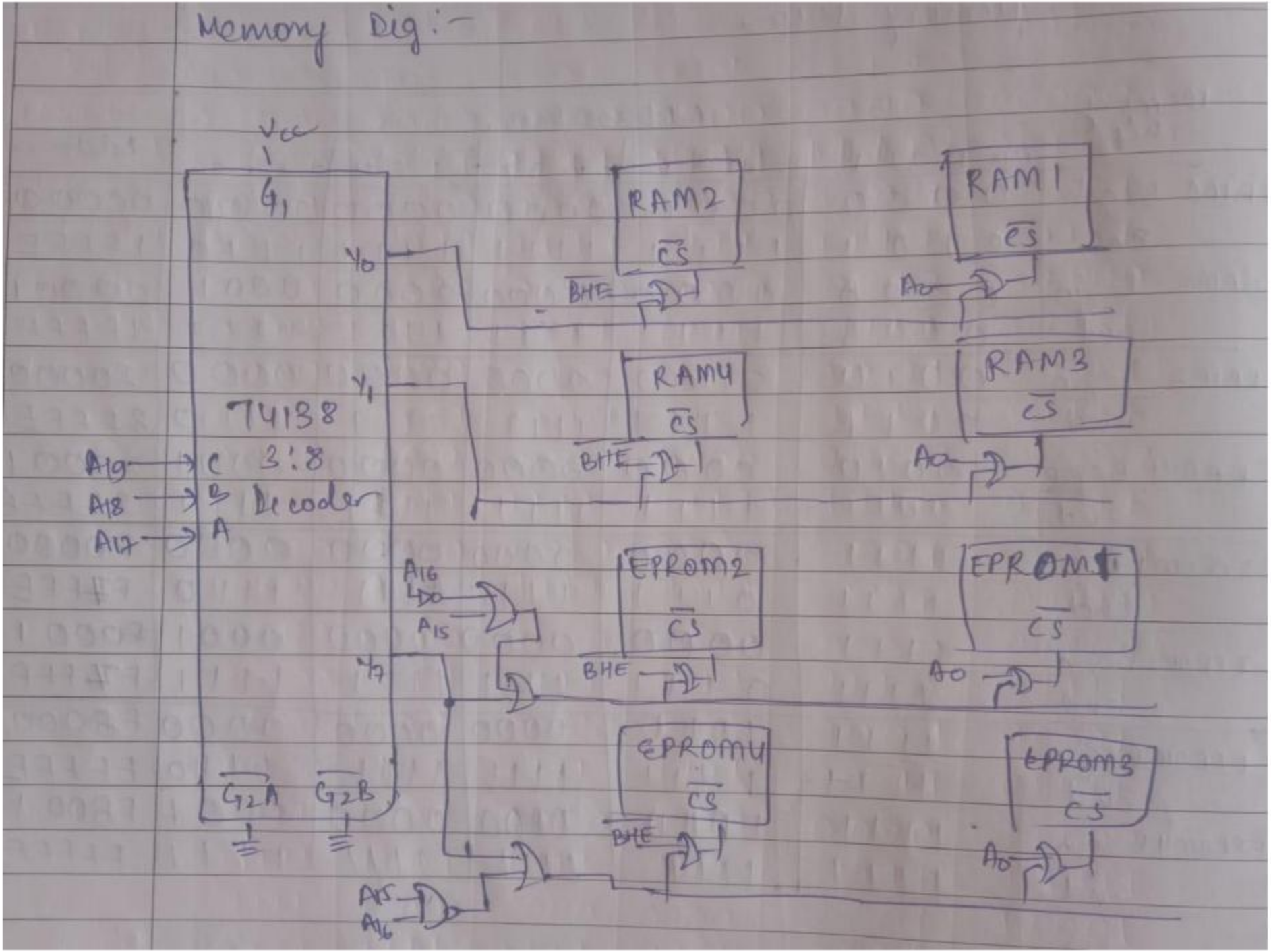
EPROM
4 chips
F0000
A1 - A14

RAM
4 chips
A1 - A15



| Memory CHIP | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | A0 | Memory Address |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RAM 1 Begin | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0000H |
| RAM 1 End | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1FFFE |
| RAM 2 Begin | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 00001 |
| RAM 2 End | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1FFFF |
| RAM 3 Begin | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 20000 |
| RAM 3 End | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 3FFFE |
| RAM 4 Begin | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 20001 |
| RAM 4 End | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 3FFFF |
| EPROM 1 Begin | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | F0000 |
| EPROM 1 End | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | F7FFE |
| EPROM 2 Begin | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | F0001 |
| EPROM 2 End | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | F7FFF |
| EPROM 2 Begin | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | F8000 |
| EPROM 3 End | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | FFFFE |
| EPROM 4 Begin | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | F8001 |
| EPROM 4 End | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | FFFFF |

Memory Dig:-


Vcc
G1
Y0
Y1
74138
3:8
Decoder
C
B
A
A19
A18
A17
G2A
G2B
RAM2
CS
BHE
RAM1
CS
A0
RAM4
CS
BHE
RAM3
CS
A0
A16
A15
EPROM2
CS
BHE
EPROM1
CS
A0
EPROM4
CS
BHE
EPROM3
CS
A0
A15
A16

128 KB EPROM using 32 KB chips  128 KB RAM using 64 KB chips

EPROM

4 chips

(A1-A15)

E0000

RAM

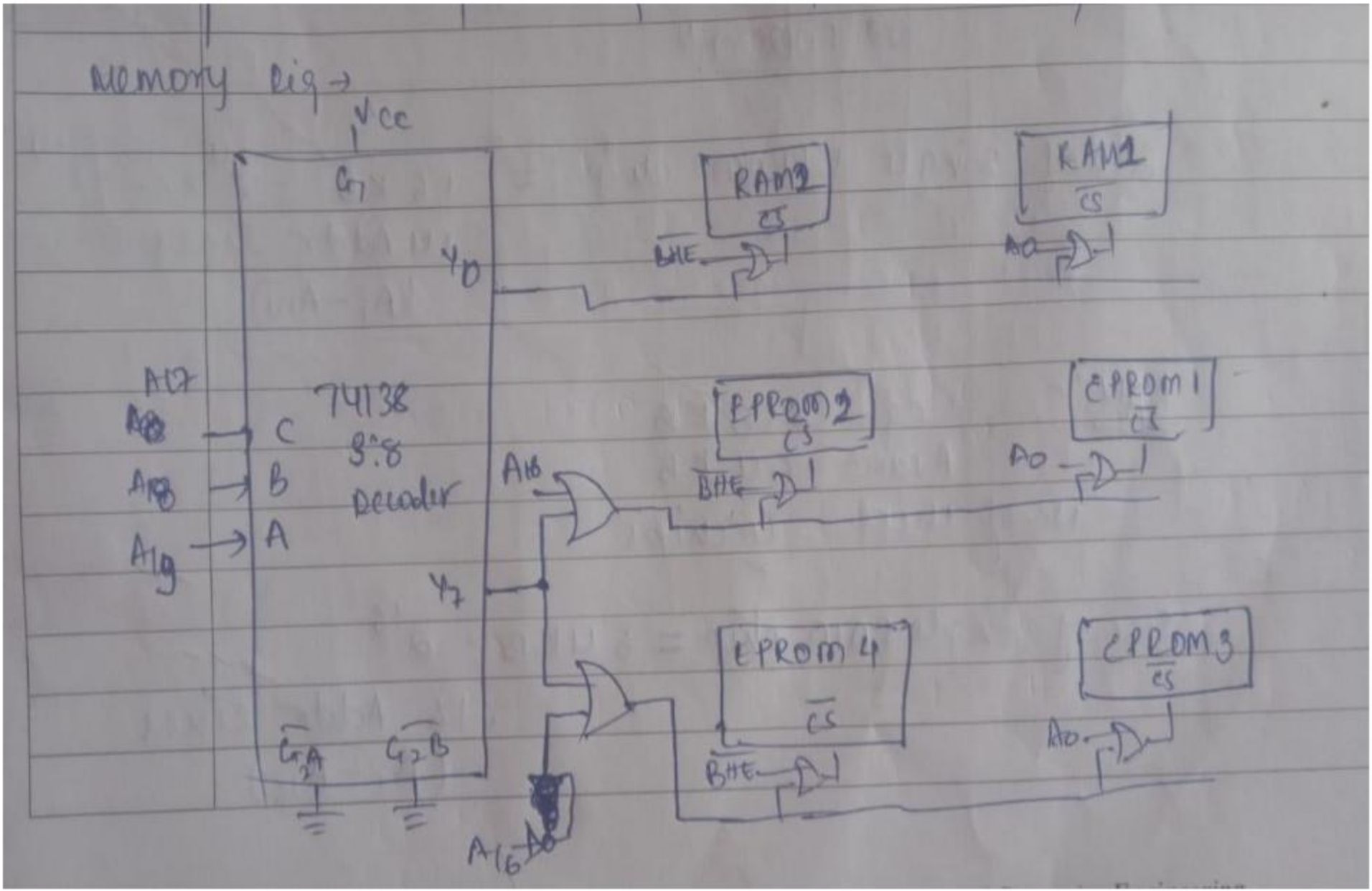
2 chips

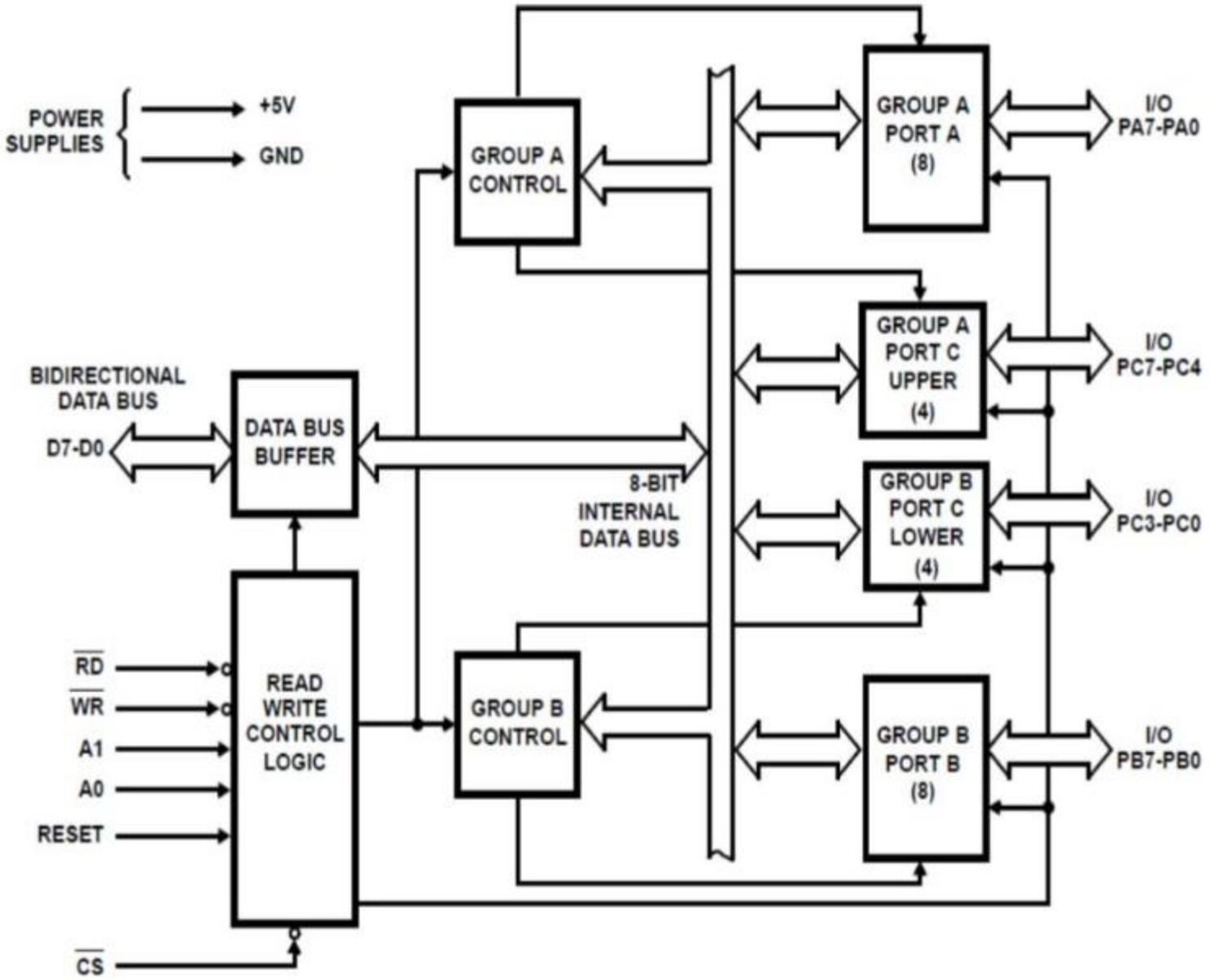
A1-A16

1FFFF=Ending

**Memory Map**

| Memory | Address Bus | | | | | | | | | | | | | | | | | | | | Memory Address |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CHIP | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | A0 | |
| RAM 1 Begin | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 00000H |
| RAM 1 End | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1FFFE |
| RAM 2 Begin | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 00001 |
| RAM 2 End | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1FFFF |
| EPROM 1 Begin | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | E0000 |
| EPROM 1 End | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | EFFFE |
| EPROM 2 Begin | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | E0001 |
| EPROM 2 End | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | EFFFF |
| EPROM 3 Begin | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | F0000 |
| EPROM 3 End | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | FFFFE |
| EPROM 4 Begin | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | F0001 |
| EPROM 4 End | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | FFFFF |
| | | | | | | | | | | | | | | | | | | | | | FFFFFH |


Memory Big →
Vcc
G1
Y0
74138
3:8
Decoder
C
B
A
A17
A18
A19
G2A
G2B
RAM2
CS
BHE
RAM1
CS
A0
EPROM2
CS
BHE
A16
EPROM1
CS
A0
Y7
EPROM4
CS
BHE
EPROM3
CS
A0
A16
A0

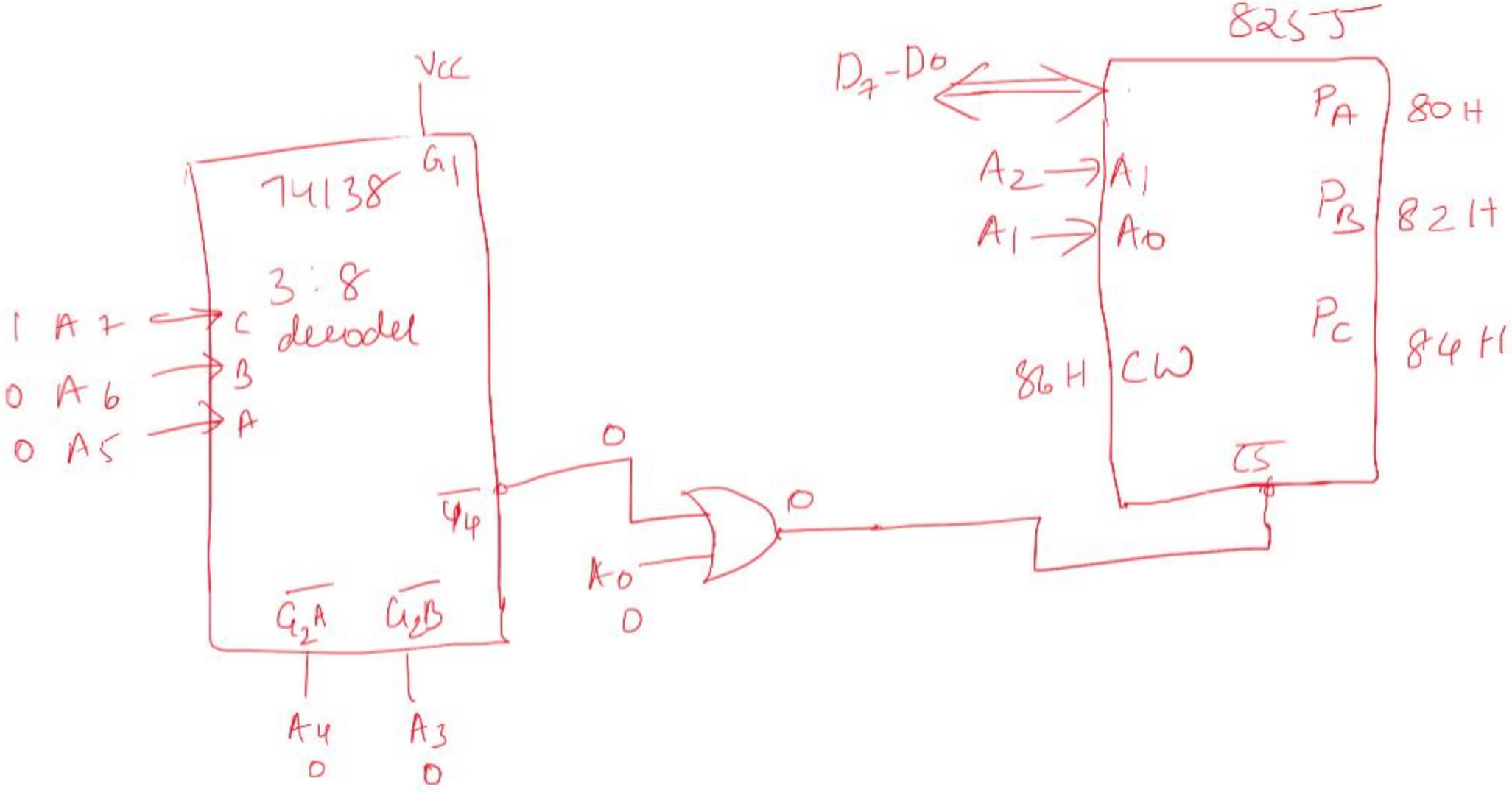

POWER SUPPLIES
+5V
GND
GROUP A CONTROL
GROUP A PORT A (8)
I/O PA7-PA0
GROUP A PORT C UPPER (4)
I/O PC7-PC4
BIDIRECTIONAL DATA BUS
D7-D0
DATA BUS BUFFER
8-BIT INTERNAL DATA BUS
GROUP B PORT C LOWER (4)
I/O PC3-PC0
RD
WR
A1
A0
RESET
READ WRITE CONTROL LOGIC
GROUP B CONTROL
GROUP B PORT B (8)
I/O PB7-PB0
CS

8255 consumes 4 addresses

There are two commands which microprocessor sends to 8255.

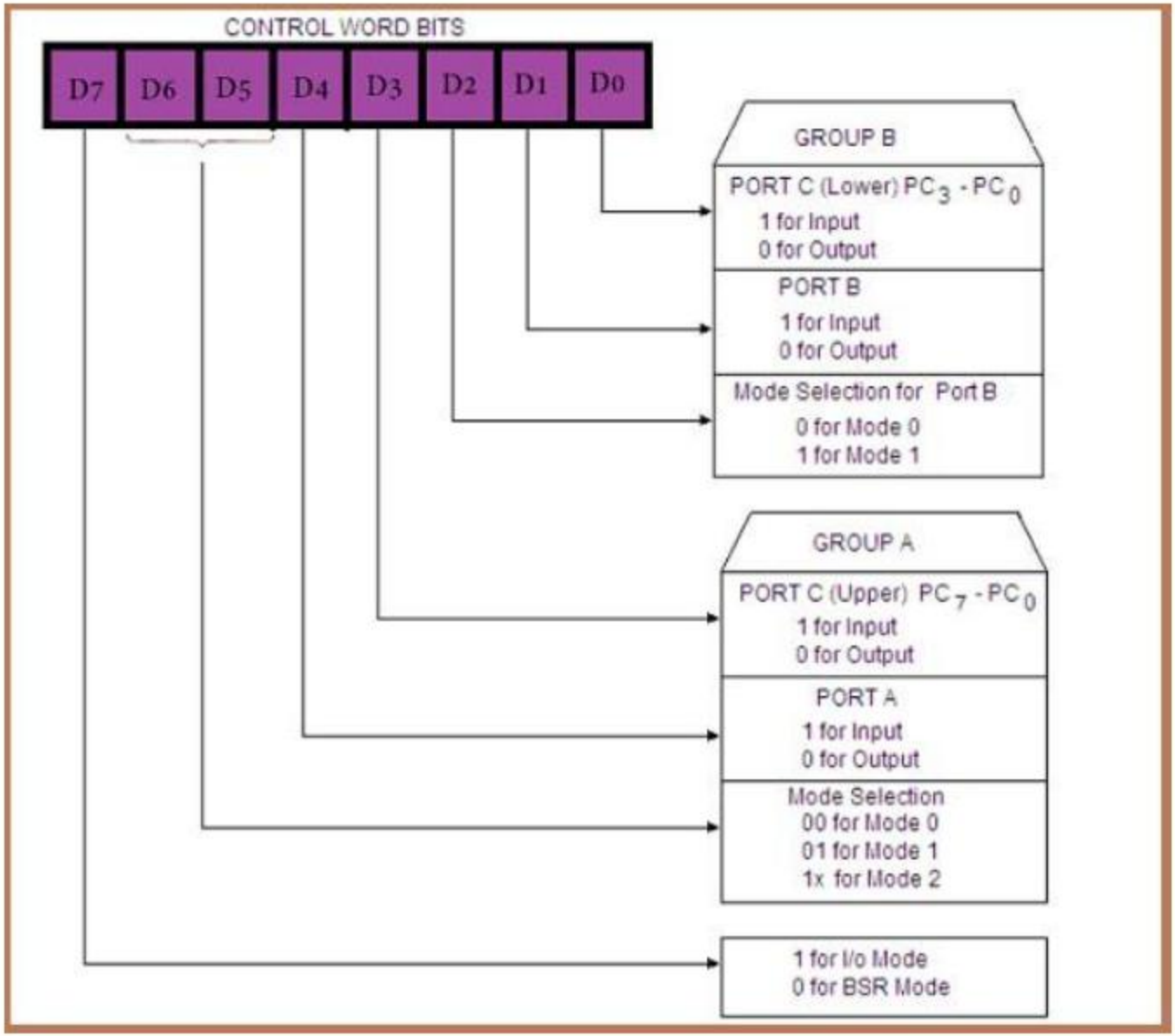
This is decided by 2 lines A1 and A0.

| For 8255 $A_1$ $A_0$ | For 8086 $A_2$ $A_1$ | Selection | Sample address |
|---|---|---|---|
| 0 0 | 0 0 | Port A | 80 H (i.e. 1000 0**00**0) |
| 0 1 | 0 1 | Port B | 82 H (i.e. 1000 0**01**0) |
| 1 0 | 1 0 | Port C | 84 H (i.e. 1000 0**10**0) |
| 1 1 | 1 1 | Control Word | 86 H (i.e. 1000 0**11**0) |

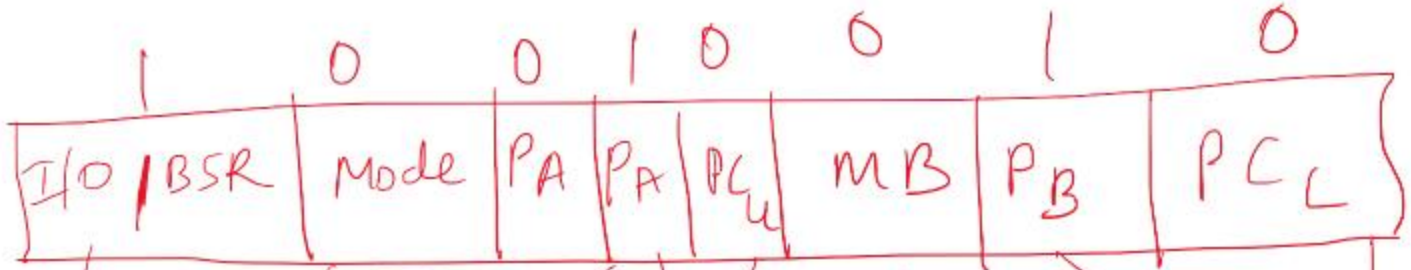


They can be programmed to wok in the various modes as follows:

| Port | Mode 0 | Mode 1 | Mode 2 |
|---|---|---|---|
| Port A | Yes | Yes | Yes |
| Port B | Yes | Yes | **No** *(Mode 0 or Mode 1)* |
| Port C | Yes | **No** *(Handshake signals)* | **No** *(Handshake signals)* |


CONTROL WORD BITS
D7
D6
D5
D4
D3
D2
D1
D0
GROUP B
PORT C (Lower) PC3 - PC0
1 for Input
0 for Output
PORT B
1 for Input
0 for Output
Mode Selection for Port B
0 for Mode 0
1 for Mode 1
GROUP A
PORT C (Upper) PC7 - PC0
1 for Input
0 for Output
PORT A
1 for Input
0 for Output
Mode Selection
00 for Mode 0
01 for Mode 1
1x for Mode 2
1 for I/o Mode
0 for BSR Mode

I/O command




1 = I/O
0 = BSR

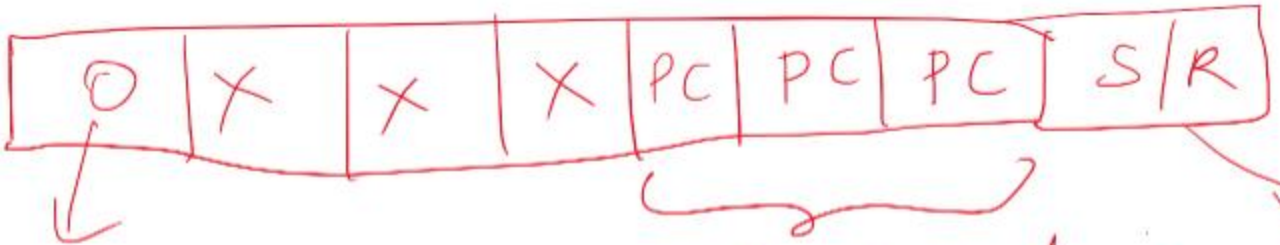
00 - mode 0
01 - mode 1
1X - mode 2

1 = I/P port
0 = O/P port

mode of port B
0 = mode 0
1 = mode 1

1 = I/P port
0 = O/P port

# BSR command




BSR

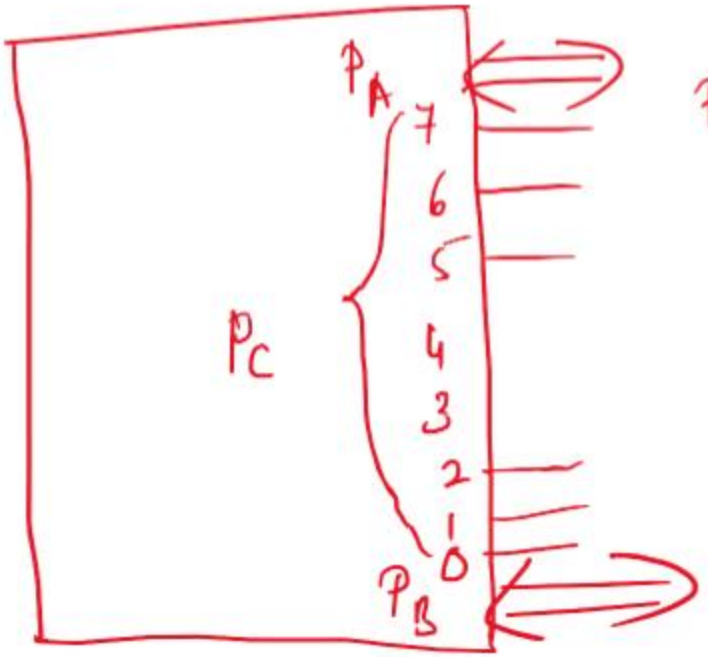
select a line of port C

000 — $PC_0$

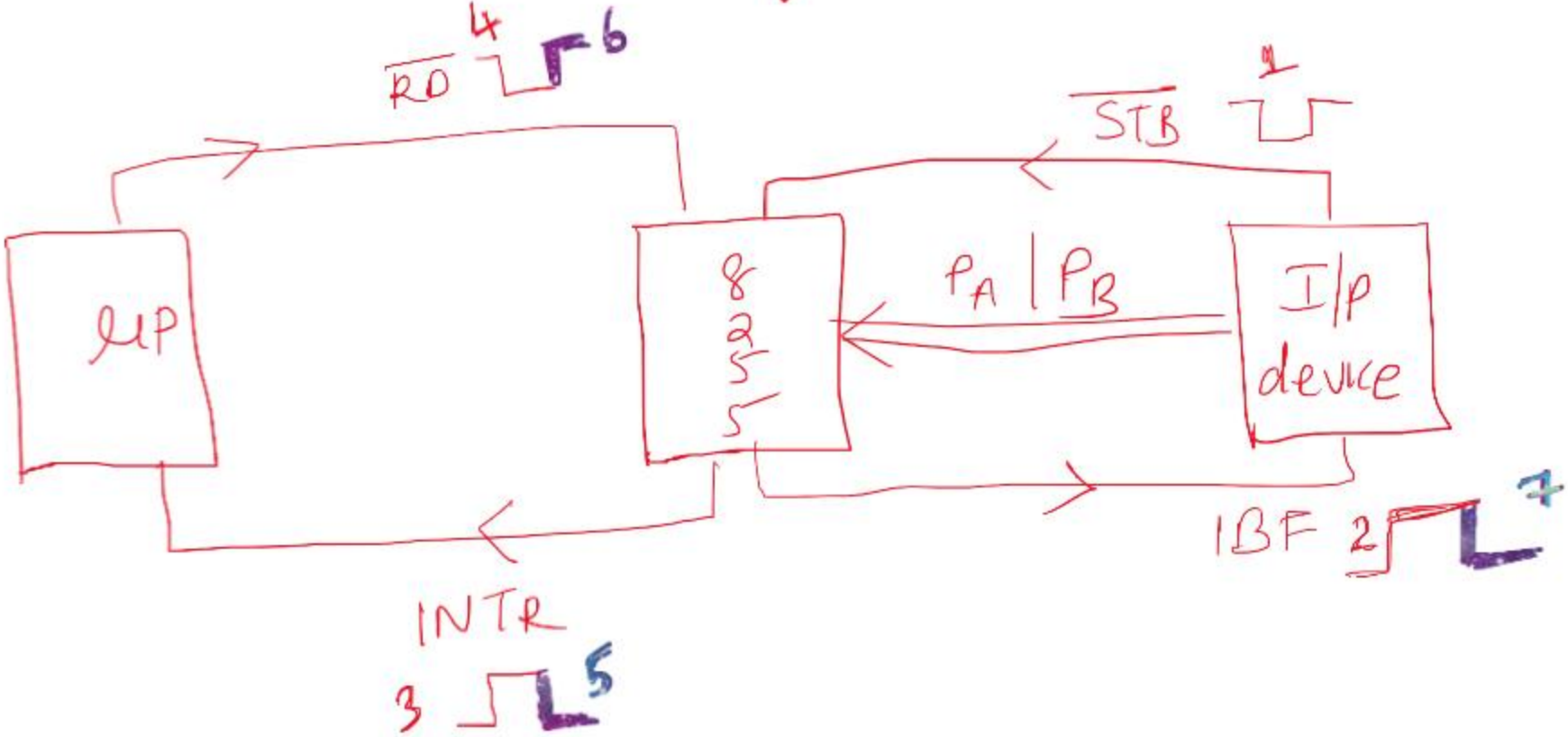
111 — $PC_7$

1 = set

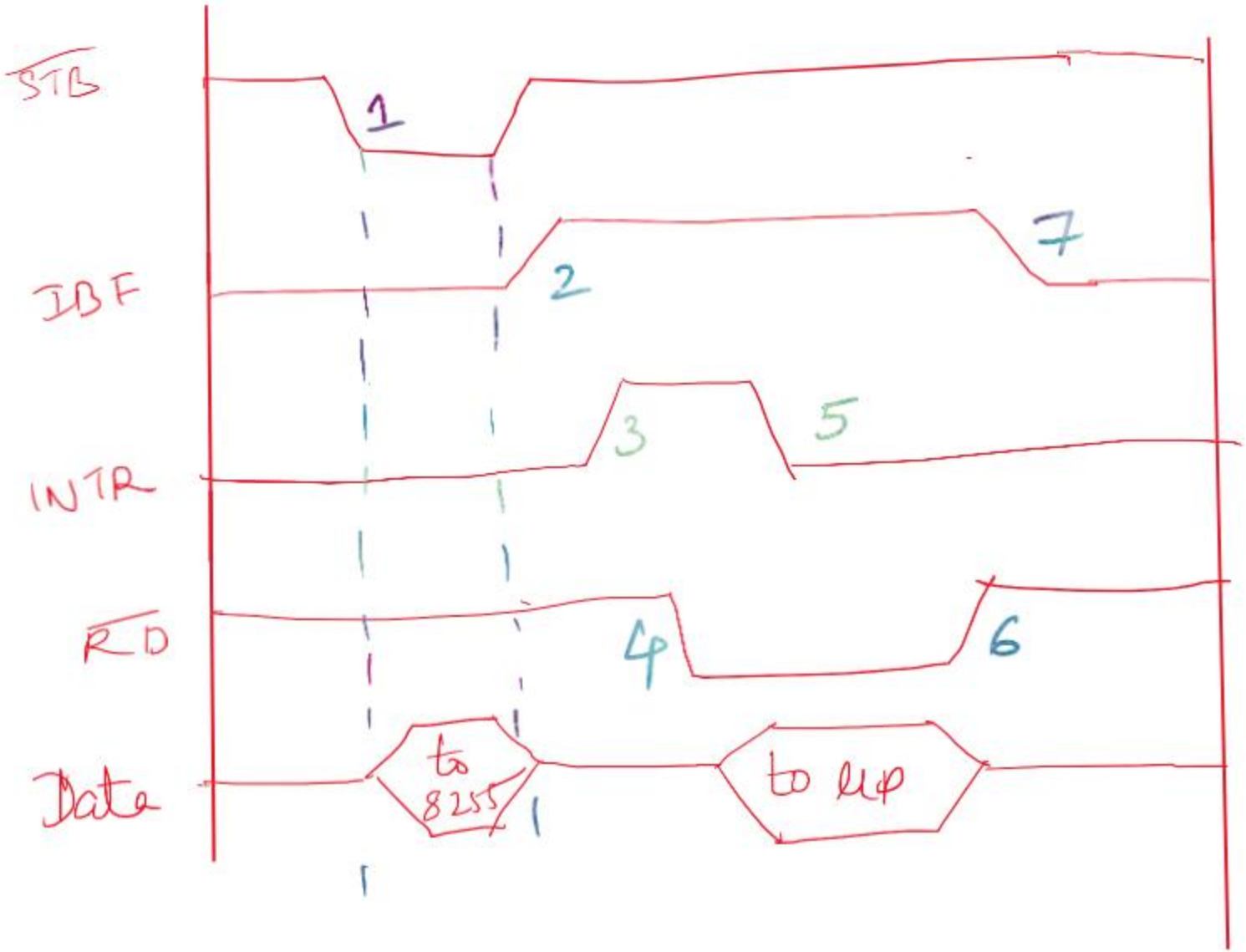
0 = reset


PA
7
6
5
PC
4
3
2
1
0
PB
PC upper
Group A
PC lower
Group B

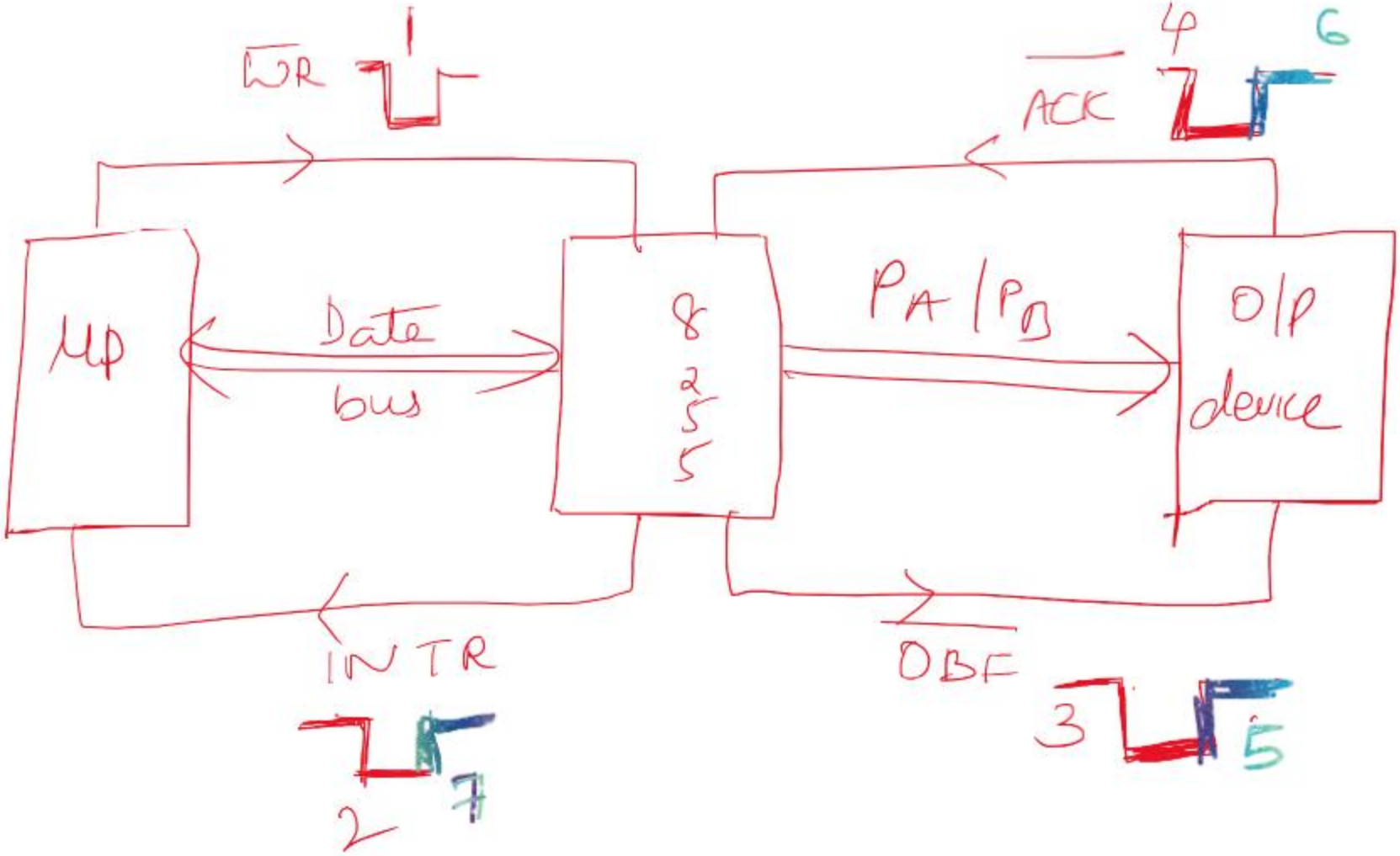
# Mode 1 – Input Handshaking

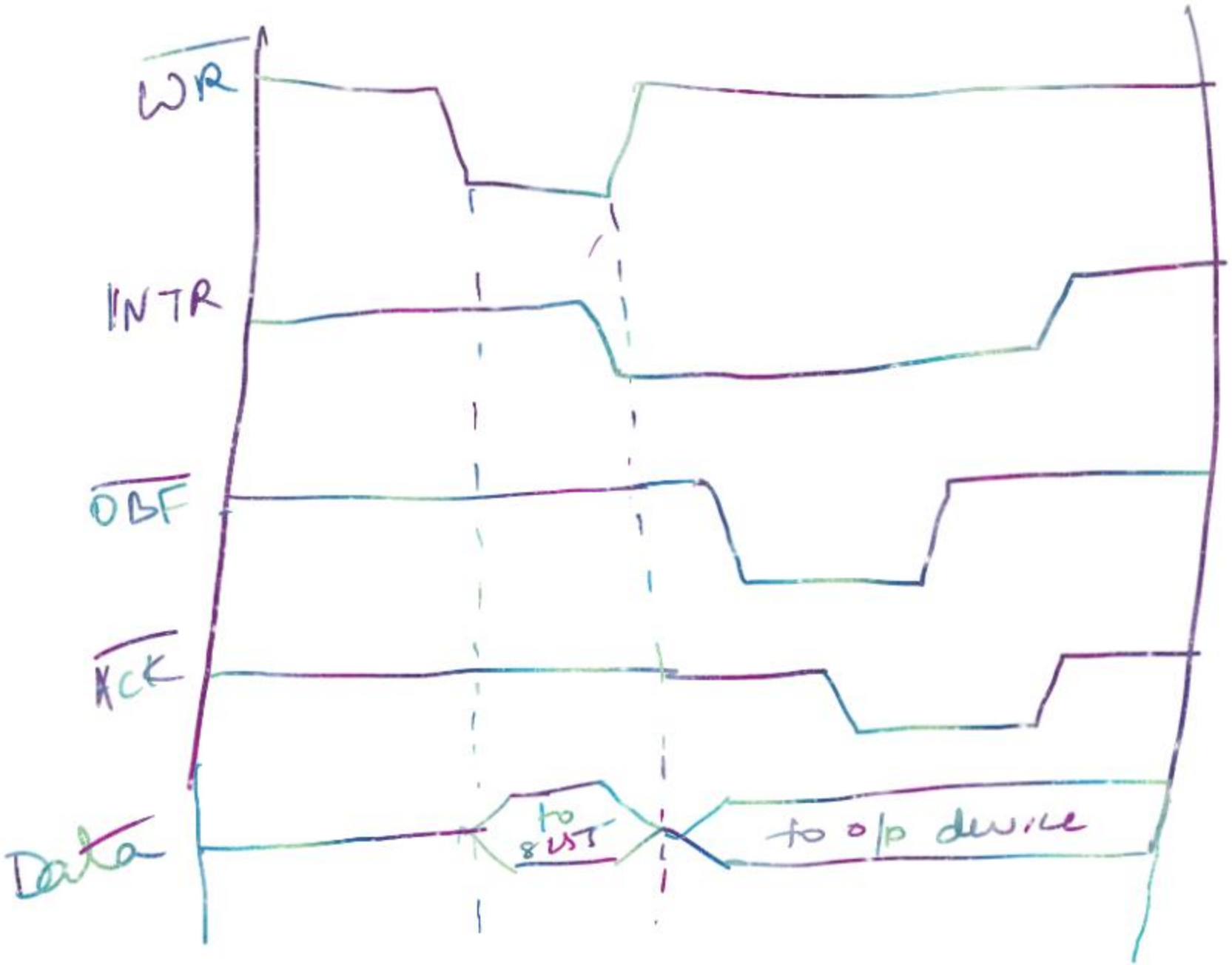



By default IBF is low


STB
IBF
INTR
RD
Data
1
2
3
4
5
6
7
to 8255
to µp

# Mode 1 - Output Handshaking




WR
INTR
OBF
ACK
Data
to 8255
to o/p device

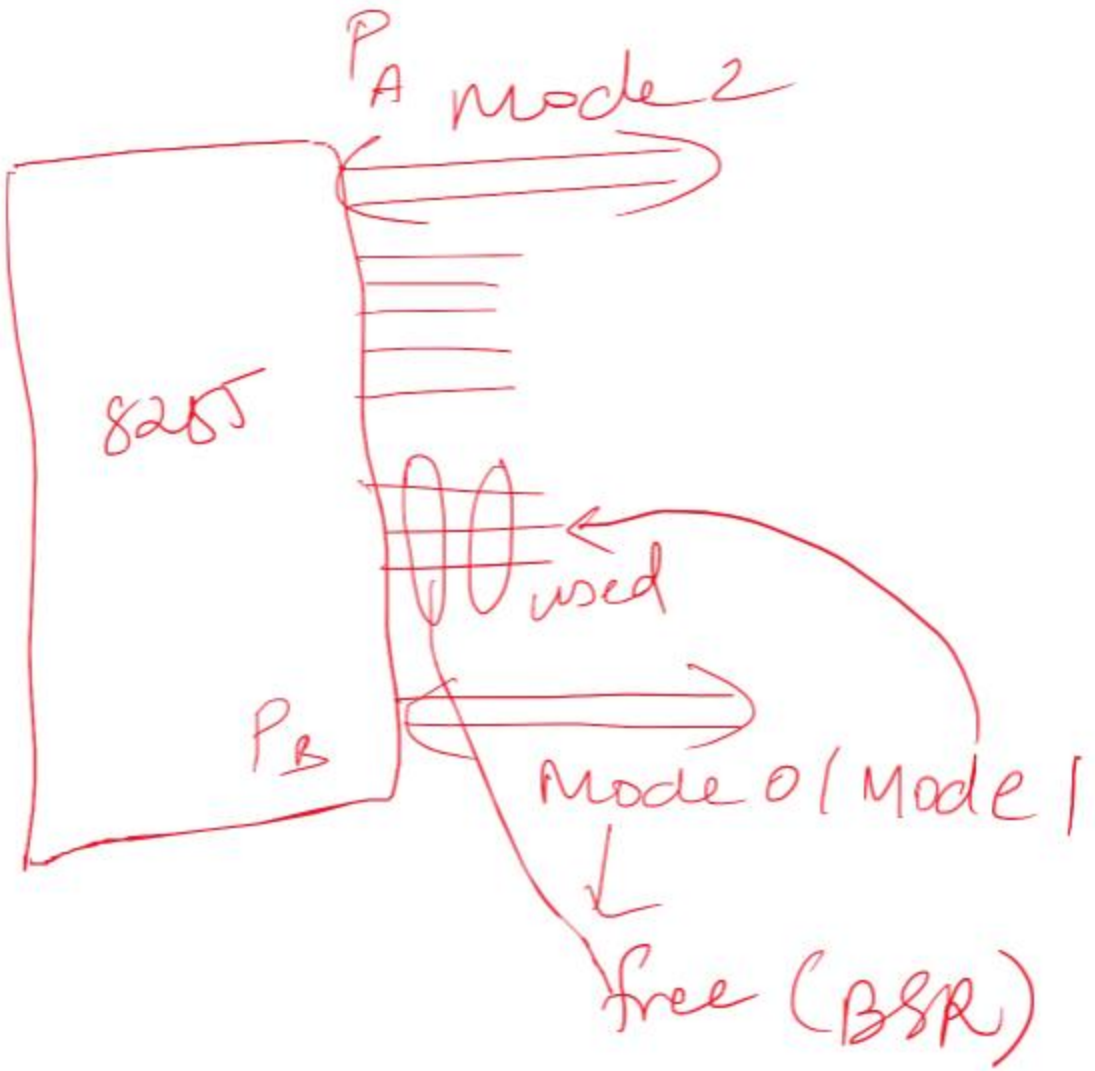
# M2 – Bidirectional Handshake

| I/p hls | O/p hls |
|---|---|
| $\overline{STB}$ | $\overline{OBF}$ |
| IBF | $\overline{ACK}$ |
| INTR | INTR |

Port A ⇒ Mode 2 (5 lines)
Port B ⇒ Mode 0 (3 lines) force used

Mode 2 (5 lines)
Mode 0 (NO hls) 3 lines force

BSR


$P_A$ mode 2
8255
used
$P_B$
Mode 0 / Mode 1
free (BSR)

Thank you