



CSC405 MICROPROCESSORS

80386 ARCHITECTURE AND EFLAG REGISTER

OBJECTIVE

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Objective: To understand 80386 Architecture and Flag Register.



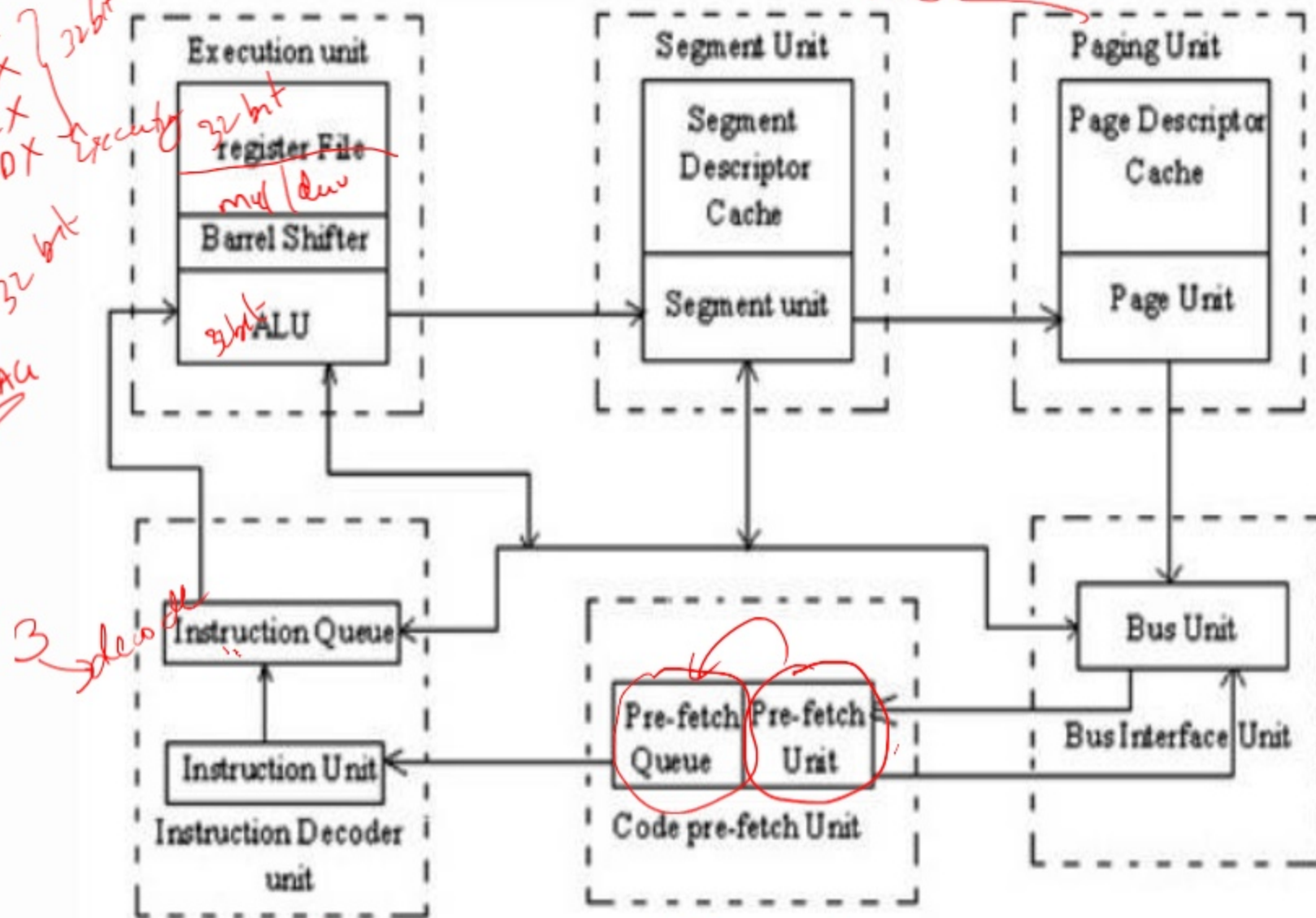
”

Architecture of 80386

EAX
EBX
ECX
EDX } 32 bit
32 bit
EFLAGS

My unit

my
64 TB



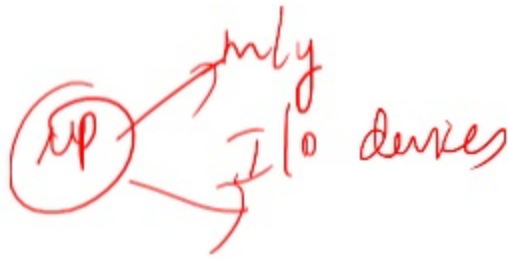
Decoding

Fetching

slm bus

① Bus Unit

transferring data in & out of MP



② Prefetch unit

next 16 bytes

↓
prefetch queue

8086 → 6 byte prefetch



execution

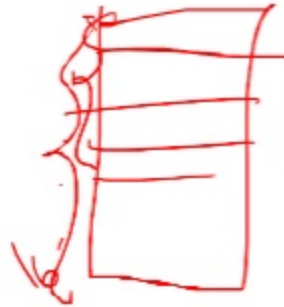
2 bytes

16 bit data bus
in 1 cycle

80386

refilled

32 bit data bus
4 bytes



decoded

Jump 2000

80386

EX

2 bytes
16 data bus

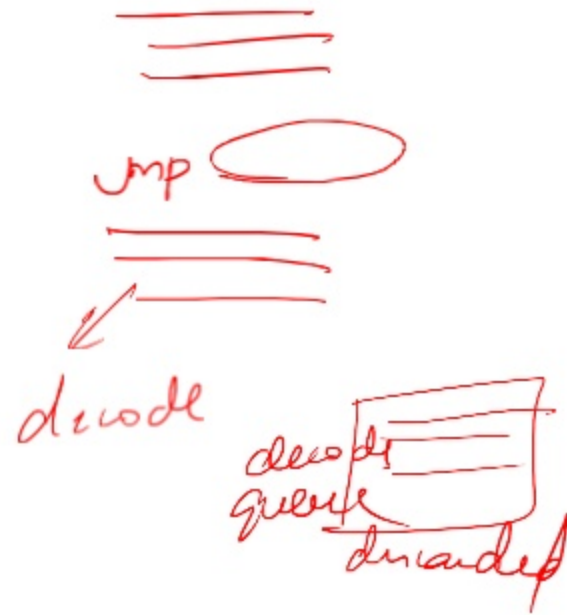
DX

4 bytes

32 bit data bus

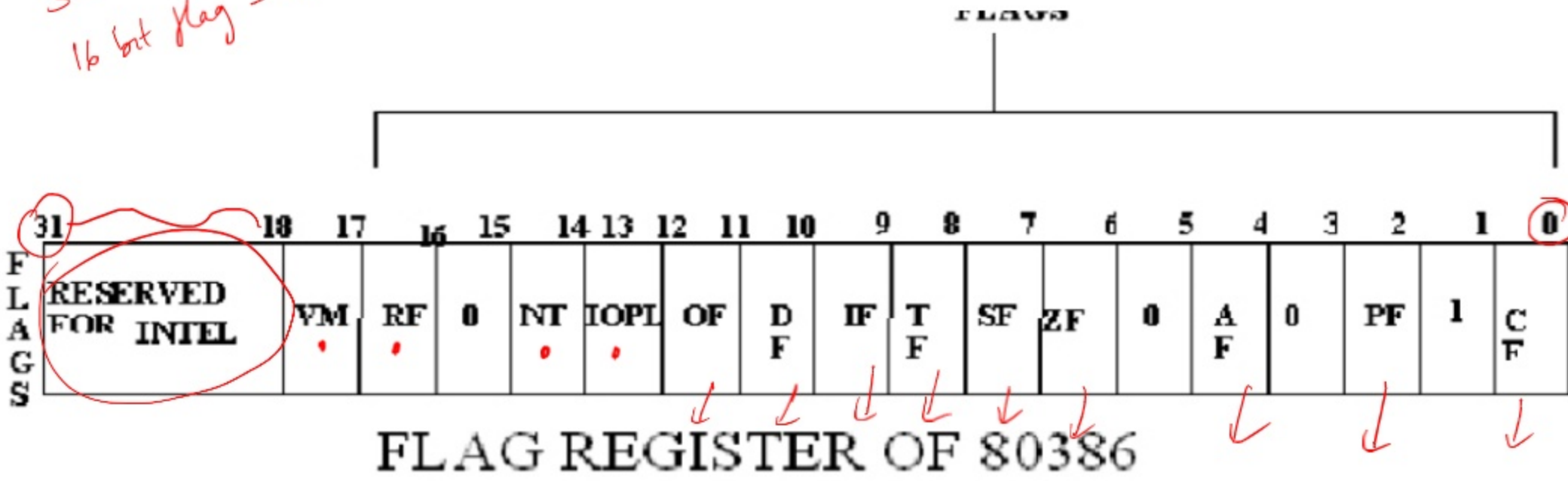
⑤ Decode Unit

④ Execution Unit



EFLAG

F0 - (3)
32 bit Flag register
16 bit flag - F0 F15



IOPL - I/O Privilege
 NT - Nested Task
 RF - Resume flag
 VM - Virtual mode

files

IOPK
↓

4 privileges

↓
code
of program

segments

I/O devices

00 → IOPK0 → highest

01 → IOPK1

10 → IOPK2

(11) → IOPK3 - lowest

IOPK = 00 → task

(I/O)

IOPK = 11 - I/O

NT - Nested task

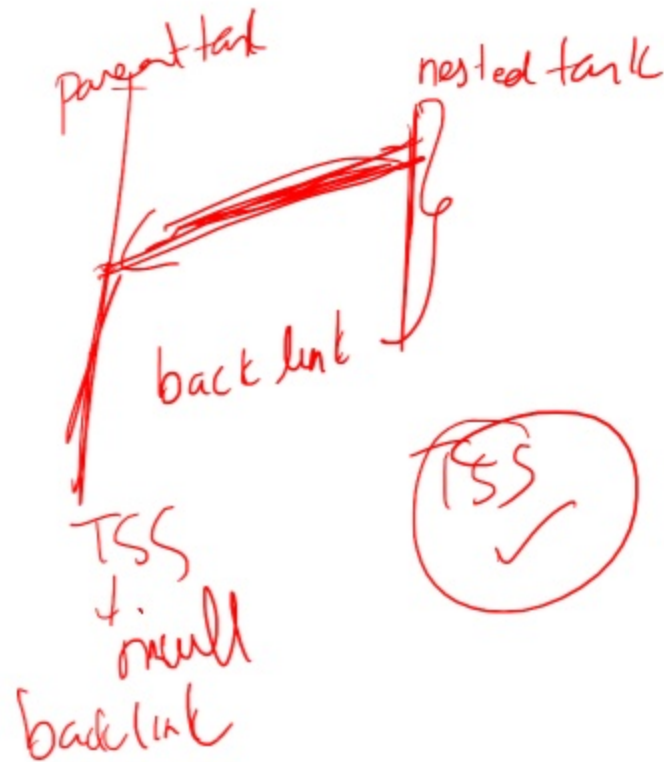
NT = 1

current task

nested

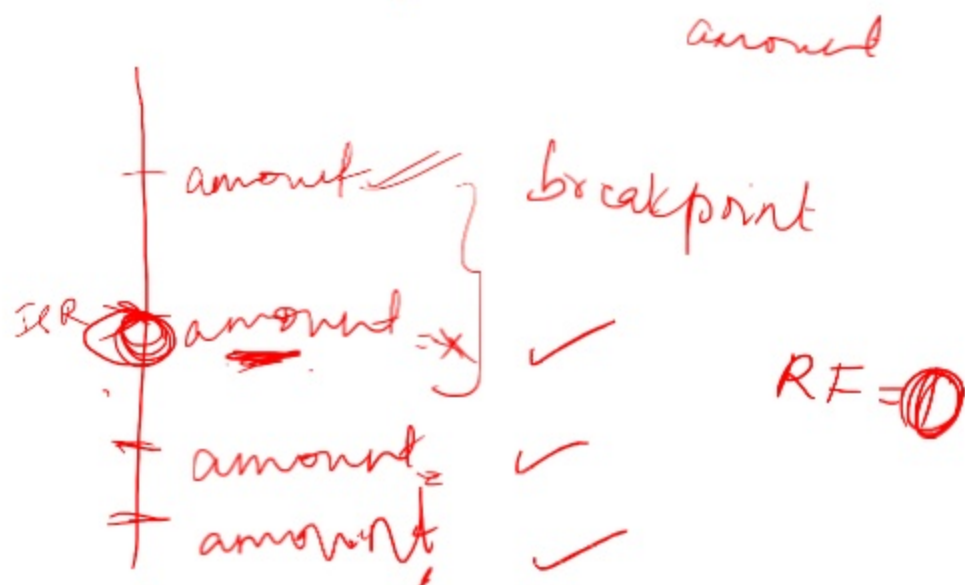
↓
task involved
child task

TSS (Task State Segment)
→ back link



RF - Resume Flag

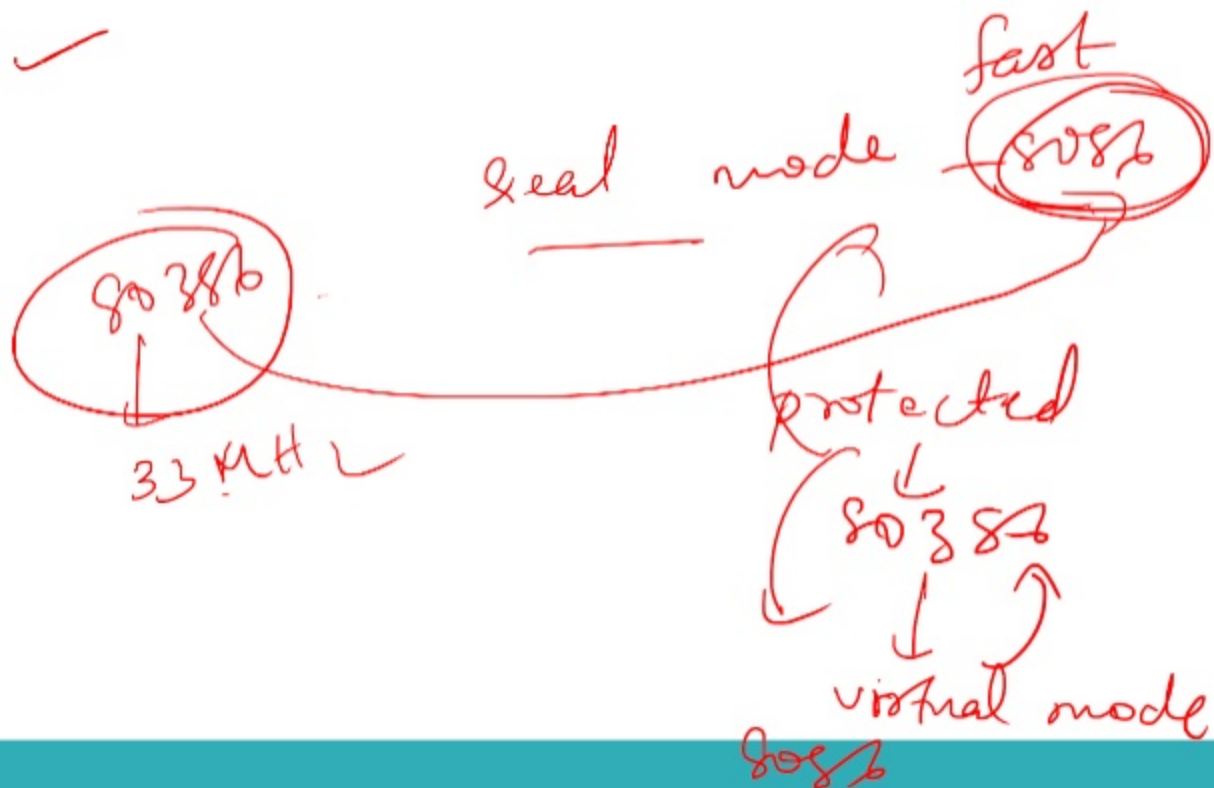
6M1+2



(skip)

80386

VM





Thank you