80386

Features:

① 80386 is a 32 bit processor. (8086 - 16 bit µP)

② 80386 has 32 bit ALU ie 32 bit operations can be performed in one cycle. {eg. Add 2 32 bit numbers}
(8086 - 16 bit ALU)

③ 80386 has 32 bit data bus. It can transfer 32 bit data in one cycle.
32 bit data is stored in 4 locations. To read these 4 consecutive locations in one cycle, they cannot be in one chip. They will be spread across in 4 chips.
So there are 4 memory banks.
(8086 - 16 bit data in one cycle ie 16 bit data bus and 2 mly banks).

④ 80386 has 32 bit address bus.
It can access 2^{32} = 4 GB memory.
8086 - 20 bit address bus
2^{20} = 1 MB memory.

⑤ 80386 can operate on 16, 20, 25, 33 MHz frequency. The higher the clock frequency, the more expensive the version is.
(8088 - 6 MHz)

(6) 80386 was released in 2 versions: SX and DX.

SX (Single Execution Speed)	DX (Double Execution Speed)
Released with a 16 bit data bus	Released with a 32 bit data bus
Due to 16 bit data bus, execution speed is lower. Hence the name SX.	Due to 32 bit data bus, the execution speed is higher. Hence the name DX.
Released for those who wanted to upgrade an 8086 processor. Since 8086 has 16 bit data bus, 80386 SX is compatible.	Released for the new customers.
16 bit transfer requires 4 memory banks.	32 bit transfer requires 4 memory banks.
Has 4 bank enable signals: $\overline{BE_3}$, $\overline{BE_2}$, $\overline{BE_1}$, $\overline{BE_0}$.	Has 2 bank enable signals $\overline{BHE}$ and $\overline{BLE}$.
2 bytes are fetched once in the pipelining queue.	4 bytes are fetched once in the pipelining queue.
Data bus is only of 16 bits. $\overline{BS16}$ signal is not useful.	Has dynamic data bus sizing of 16 bit and 32 bit databus using $\overline{BS16}$ signal.
Used for low cost mly and I/O system design.	Used for high performance

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(7) 80386 has 3 stage pipelining (8086 - 2 stage pipelining)
- Fetch
- Decode
- Execute

(8) 80386 can access 64 TB of virtual memory. Virtual memories are implemented using secondary storage devices like hard disks.

(9) 80386 implements virtual mly through segmentation and paging (address translation)

(10) 80386 has a protected model for accessing both mly and I/O. ie, the programmer is not allowed to give mly address.
It uses 4 priviledge levels - 0, 1, 2 and 3
↑ highest ↑ lowest.

If a file is stored at PL0, then only the programs which are stored at PL0 can access that file.

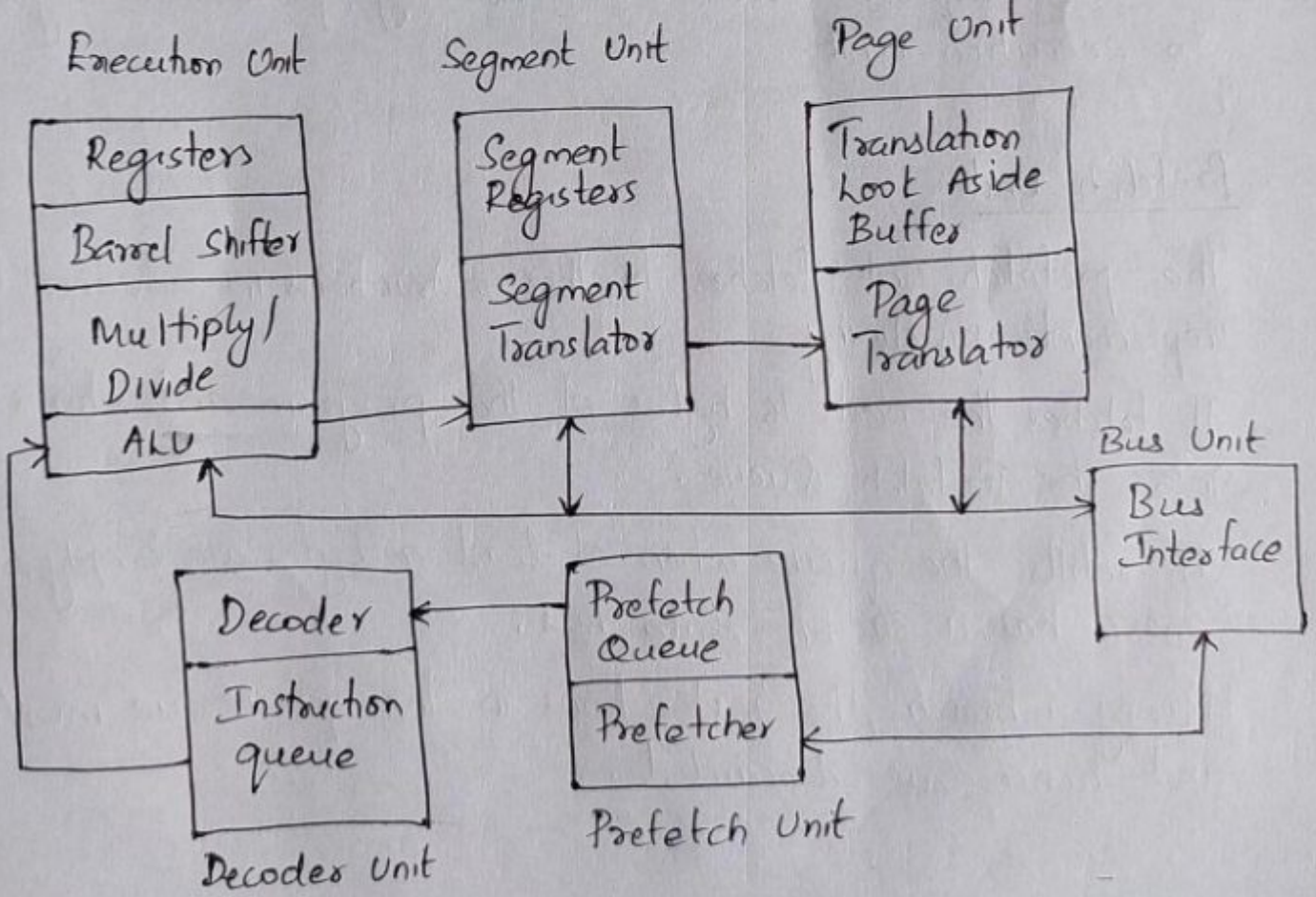
PL1 can be accessed by PL0 and PL1.
PL3 can be accessed by all.

Today when you click on a file, OS checks your priviledge level and the files' priviledge level and only if it is valid it passes the address to yous program and the file open

(11) 80386 allows multitasking using timesharing. Here several tasks can execute simultaneously by taking a small time slice of the µP, this gives higher sim performance.

(12) I/O addressing.
80386 uses a 16 bit I/O address and hence can access up to 2^{16} ie, 65536 I/O devices with address 0000h ... FFFFh.

80386 Architecture / Functional Block Diagram



80386 architecture is divided into 5 independent units.

Bus Unit (Bus Interface Unit)

The bus unit is responsible for transferring data in and out of the µP.

It is connected to the external memory and I/O devices, using the system bus.

It gets requests from Prefetch unit for fetching instructions and from execution unit for transferring data.

If both requests occur simultaneously, preference is given to execution unit

Prefetch Unit

The prefetch unit fetches further instructions in advance to implement pipelining

It fetches the next 16 bytes of the program and stores it into the Prefetch Queue.

It refills the queue when at least 4 bytes are empty as 80386 has a 32 bit data bus.

During a branch, the instructions in the queue are invalid and hence are discarded.

Decode Unit

80386 µP has a separate unit for decoding instructions called the Decode Unit.

It decodes the next three instructions and keeps them ready in the Decode Queue.

During a branch, the instructions in the queue are invalid and hence are discarded.

Execution Unit.

Execution unit performs the main task of executing instructions. Normally, execution requires arithmetic or logic operations performed by a 32 bit ALU.

It also has dedicated circuits for 32 bit multiplication and division.

A 64 bit barrel shifter is also provided for faster shifts during multiplication and division.

Operands for the ALU can either be provided in the instruction or can be taken from mly or could be taken from the 32 bit registers like EAX, EBX etc.

Additionally, there is a 32 bit flag register (EFLAGS) giving the status of the current result.

Memory Unit :

The memory unit converts Virtual Address (logical address) to Physical Address.

80386 CP implements 64 TB of Virtual Memory using Segmentation and Paging. Hence the memory unit is sub-divided into Segmentation Unit and Paging Unit.

Segmentation is compulsory, while Paging is optional.

The Segmentation Unit converts the logical Address into a Linear Address.

The Paging Unit converts the Linear Address into a physical Address.

If paging is not used, then the linear Address itself is the Physical Address.