

A.P. SHAH INSTITUTE OF TECHNOLOGY

Department of Computer Science and Engineering
Data Science

Academic Year: 2022-23 Class/Branch: SE Semester: IV

Subject: MP

8255 PPI (Programmable Peupheral Interface)

8255 provides an interface blue the processor and Ilo devices.

Why 8255 ?

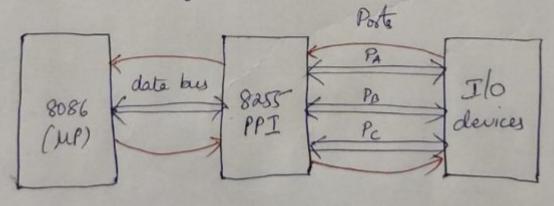
Ilo devias are never connected directly to the data bus of the Mr. They are connected to posts and these ports come from a chip like 8255.

What if we don't connect 8255 in blue and connect I/o devices directly to the data bus of MP?

Transfer is unreliable.

Ilo devices blindly sends data to UP hoping that All is in a condition to accept data. Here no permission is taken by the Ilo device and no acknowledgement taken by UP. So the data transfer is unreliable.

This reliability is given by a chip like 8255.





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8255 on one side is connected to up by the data bus and on the other side is connected to ilp ofp devices by the posts. 8255 has 3 8 bit ports which are bidirectional.

Post B 4 can transfer 8 bits data Post c] can be used as ifp post or ofp post.

Suppose an Ilo device wants to send data to up. It sends the data to 8255. How? - Blindly? - NO The Ilo device takes the permission of 8255 proor to sending the data. On receipt of data 8255 stores it and then informs the up that it has data waiting to be read. Whenever free, the UP issues a read signal asking for data.

In case the UP is busy right now and has not yet read the data. I'm the neanwhile can the Ilo device send new data? _ NO

the purious data is not lost.

Only once the previous data is transferred to up, 8255 grants permission for new data.

So will this take time? - YES will this take long time? - MAYBE How long? - 8255 does not know. There is no clock in 8255.





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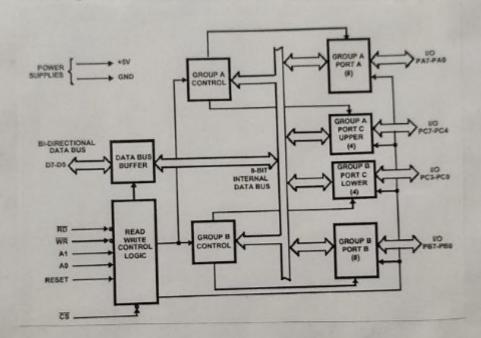
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The signals which make the toanter reliable are called hand shaling signals and this is the reason why 825T is used.

8255 Block Diagram / Architecture:



The data bus buffer is a 8-bit bidirectional buffer wed to interface the interface the internal data bus of 8255 with the system data bus.

Port A lines are called PAO - PAZ

Port B lines are called PBO - PBZ

Port C lines are called PCO - PCZ. Even though it is

Port C lines are called PCO - PCZ. Even though it is

an 8 bit post, it is divided into 2 parts:

PCO - PCZ PCZ - PCZ

PCO - PCZ



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Port B

Post C

control word





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Subject: Microprocessor

Semester IV

Interfacing with 8086

Semester: IV

Note: - A1 and 8255 are connected with A24A, gup.

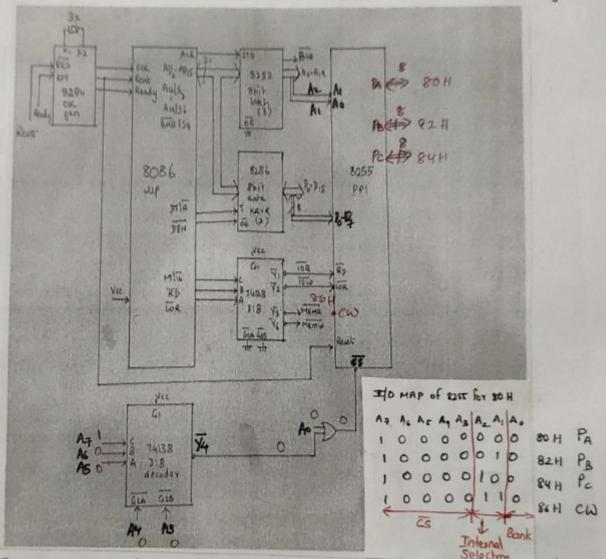


Figure: - Interfacing of 8255 with 8086 in minimum mode

Top and Iow of up are connected to RD & we of 8255. Reset of clock generator is connected to reset of 8255.



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6855	prevates in three deffer Node O (Simple I/O)	Mode 1 (Hardshake I/O)	Mode 2 (Bidisechonal) Handshake
Port A	V	to be to V	10
Port B	V 10 1 84 8		Mode 0 /Mode 1
Port c		×	×

- · In made a all sports are allowed to transfer data.
- · In mode I, only post A and B are allowed to transfer date. Post C lines are sacrificed to perform handstaking.

If port A is in mode 1, it will take the upper lines of Aost c to perform handshaking.

If pot B is in mode 1, it will take the lower lines of post c to perform handshaking.

Post c upper works with Post A, so together they are called aroup A. Post c lawer works with Post B, so together they are called aroup B. aroup A is controlled by the aroup A control logic. aroup B is controlled by the aroup B control logic.

- of mode 2, only post A can transfer date . Post B is functional but it will wort in mode 1 or mode 0. Post C will be lost in doing handshaking.
 - So, post A can work in all the 3 modes.

 post B can work in Mode 0 or Mode 1.

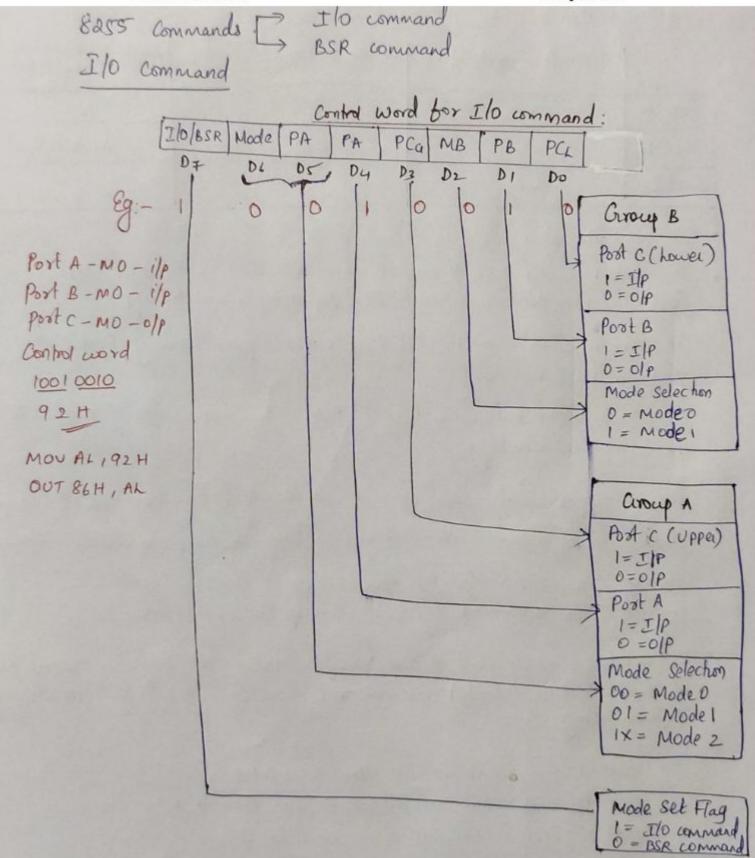
 post c can work only in mode 0.



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To do 8 bit transfer using Port A, B, C 8255 has to be in Ilo mode. The bit pattern for the control word in Ilo mode is shown above. The MSB of the command identifies whether it is an Ilo command or BSR command.

When 8255 is initialized, there are a things to be decided for every post. - which made it will work in

- which direction it will work in.

s modes, but only 1 bit is used to tell the mode of post A as it can work in only 2 modes.

The mode of post c is automatically decided by the mode of post A and Post B ie, if post A is in mode o and post B is mode o; obviously post c will also be in mode o, otherwise post c lines are used for handshaking.

of If some data is sent on the data bus. It does not stay, it comes and goes. But if something is sent to a post, it will stay as each post internally has a latch.

If the post is working as an i/p post, the latch has to be durabled so that the data which the I/o device is sending informed to the post.



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