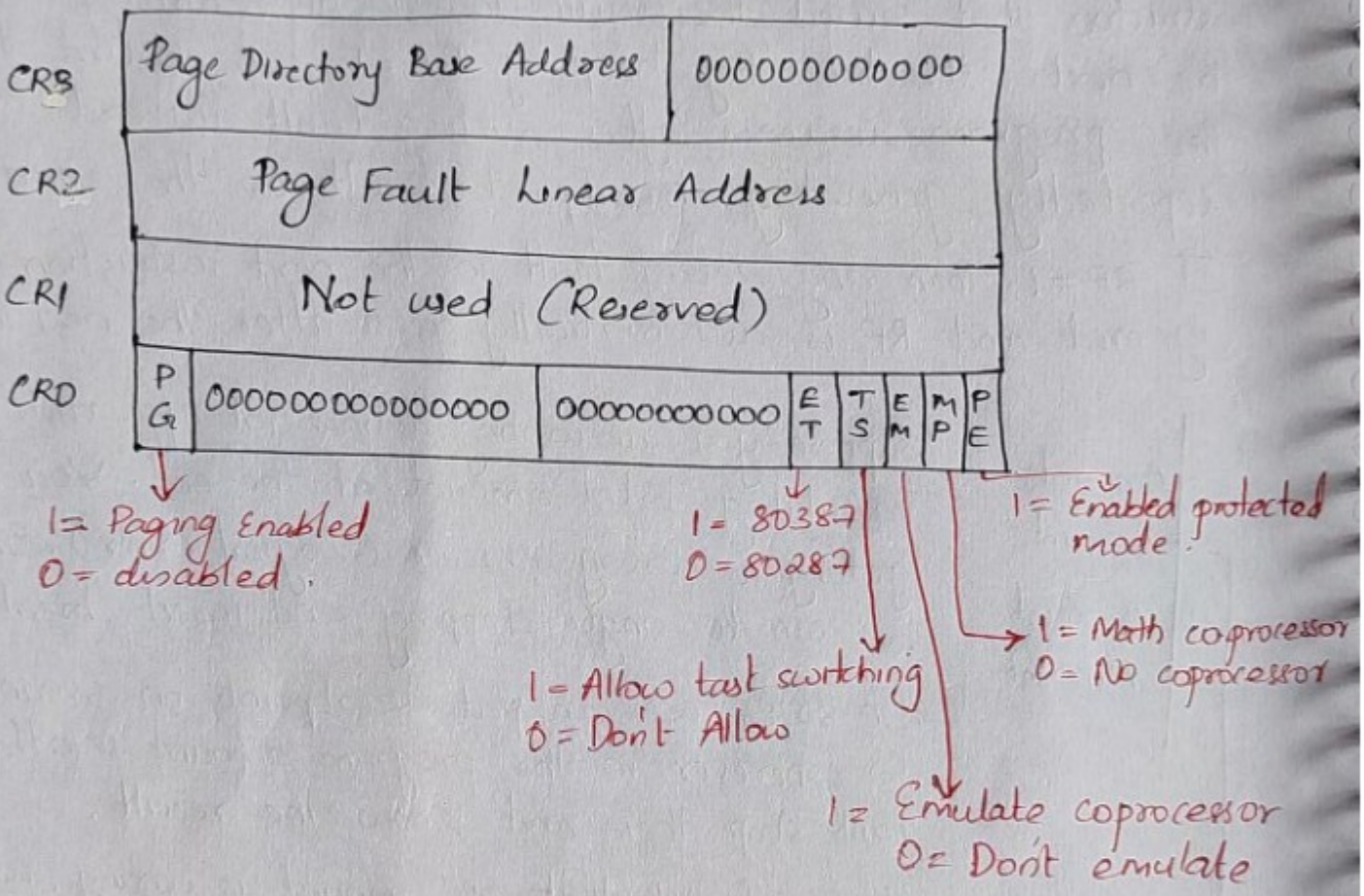
Academic Year: 2022-23 **Semester: IV**
Class/Branch: SE **Subject: Microprocessor**

80386 Control Registers :



There are 4 control registers : CR0, CR1, CR2 and CR3 (32 bits) These registers are not available in Real Mode, except one bit of CR0 (PE). The four control registers are available in protected mode.

Control Register 0.

PE: Protection Enable

This bit is made '1' to enter Protected Mode.
On reset, by default this bit is 0.

It is the only bit of CR0 which is available in Real Mode.

MP, EM : Related to coprocessor (floating point) operation.

MP : Math Coprocessor present.

This bit is made "1" to indicate that a math coprocessor like 80287 or 80387 is present.

If MP = 0, EM bit is checked.

EM : Emulate Coprocessor.

This bit is made a "1" in the absence of a Math Co-Processor so that a floating point instruction is encountered, then it will be executed by an onchip emulator.

Emulation means one processor behaving like another. So 80386 will do the instruction.

Note: Out of EM bit and MP bit, only one of them must be a "1".

MP = 1 & EM = 1 is not sensible as there is a coprocessor and there is no need for 80386 to emulate.

MP = 0 & EM = 0 ← will cause an error.

TS : Task Switching.

This bit is made a "1" to indicate if a task switch is performed. 80386 µP implements multitasking and thus it switches b/w various tasks, giving the programmer the impression that all tasks are running concurrently.

ET : Extension Type.

This bit is used to indicate the type of Math Co-Processor used with 80386.

This bit is checked only when MP = 1.

If ET = 1, 80387 Math Co-Processor is used

ET = 0, 80287 Math Co-processor is used.

80386 can work with both 80387 and 80287.

PG : Paging Enable

This bit is made "1" to enable Paging mode.

80386 µP implements Virtual Memory using the techniques of segmentation and paging. Though segmentation is compulsory paging is optional and is enabled using the PG bit of CR0.

Control Register 1 : Not Used (Reserved by Intel)

Control Registers 2 and 3 : Used only for Paging.

CR2 : (Page Fault Linear Address)

Segment translation translates Virtual Address into Linear Address Paging translates the linear address to a physical address and this is possible only when the desired page is present in the physical memory.

A page fault is said to occur when the desired page is not present in the physical memory. So the physical address translation does not happen.

So the last linear address that caused a page fault is stored in CR2.

CR3 : (Page Directory Base Register — PDBR)

While paging, there are 1 million pages. Entries for these pages are stored in 1K page tables. Information about the 1K page tables is stored inside the page directory.

The starting address of the page directory is given by Page Directory Base Register.

Note :- PDBR is only 20 bits. It just gives the upper 20 bits of the starting address of the page directory. That's because the page directory is of 4 KB and is stored at 4 KB aligned location, so the last 12 bits of the starting address are assumed to be "0".