PARSHVANATH CHARITABLE TRUST'S
A.P. SHAH INSTITUTE OF TECHNOLOGY
Department of Computer Science and Engineering
Data Science

Department of Computer Science Engineering Data Science

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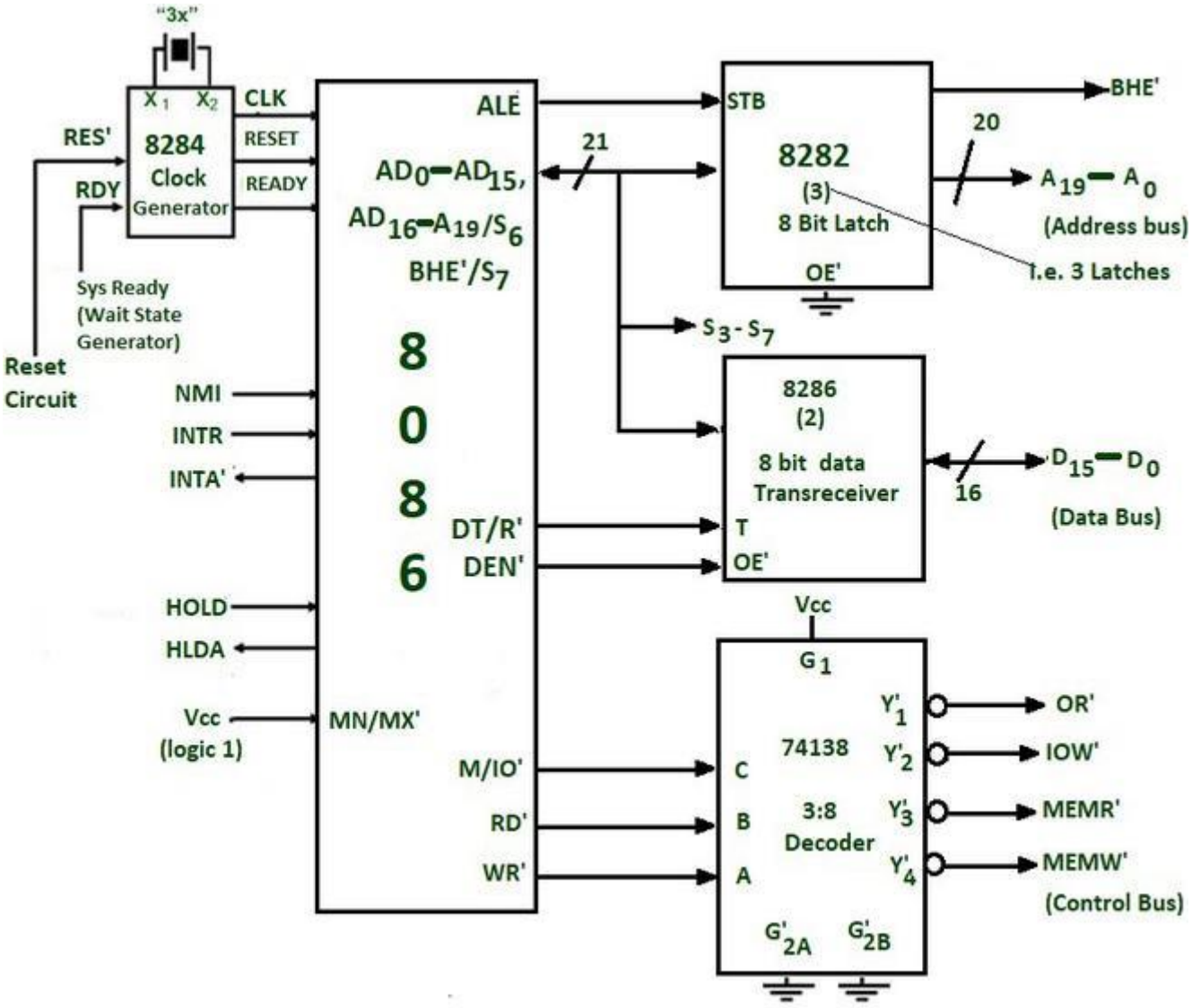
Minimum mode configuration of 8086 microprocessor (Min mode)

Overview :

- The 8086 microprocessor operates in minimum mode when MN/MX' = 1.
- In minimum mode,8086 is the only processor in the system which provides all the control signals which are needed for memory operations and I/O interfacing.
- Here the circuit is simple but it does not support multiprocessing.
- The other components which are transceivers, latches, 8284 clock generator, 74138 decoder, memory and i/o devices are also present in the system.
- The address bus of 8086 is 20 bits long. By this we can access 2^{20} byte memory i.e. 1MB . Out of 20 bits, 16 bits A_0 to A_{15}(or 16 lines) are multiplexed with a data bus. By multiplexing, it means they will act as address lines during the first T state of the machine cycle and in the rest, they act as data lines. A_{16} to A_{19} are multiplexed S_3 to S_6 and BHE' is multiplexed with S_7.

Control signals provided by 8086 for memory operations and i/o interfacing :
They are used to identifying whether the bus is carrying a valid address or not , in which direction data is needed to be transferred over the bus, when there is valid write data on the data bus and when to put read data on the system bus. Therefore, their sequence pattern makes all the operations successful in a particular machine cycle.



Min mode circuit

8282 (8 bits) latch :

The latches are buffered D FF. They are used to separate the valid address from the multiplexed Address/data bus by using the control signal ALE, which is connected to strobe(STB) of 8282. The ALE is active high signal. Here three such latches are required because the address is 20 bits.

8286 (8 bits) transceivers :

They are bidirectional buffers and also known as data amplifiers. They are used to separate the valid data from multiplexed add/data bus. Two such transceivers are needed because the data bus is 16 bits long. 8286 is connected to DT/R' and DEN' signals. They are enabled through the DEN signal .The direction of data on the data bus is controlled by the DT/R' signal. DT/R' is connected to T and DEN' is connected to OE'.

DEN'	DT/R'	Action
1	X (don't care)	Transreceiver is disabled
0	0	Receiver data
0	1	Transmit data

Direction of data flow

- 8284 clock generator is used to provide the clock.
- M/IO'= 1,then I/O transfer is performed over the bus. and when M/IO' = 0, then I/O operation is performed.

- The signals RD' and write WR' are used to identify whether a read bus cycle or a write bus cycle is performing. When WR' = 0 ,then it indicates that valid output data on the data bus.
- RD' indicates that the 8086 is performing a read data or instruction fetch process is occurring .During read operations, one other control signal is also used, which is DEN (data enable) and it indicates the external devices when they should put data on the bus.
- Control signals for all operations are generated by decoding M/IO', RD', WR'. They are decoded by 74138 3:8 decoder.

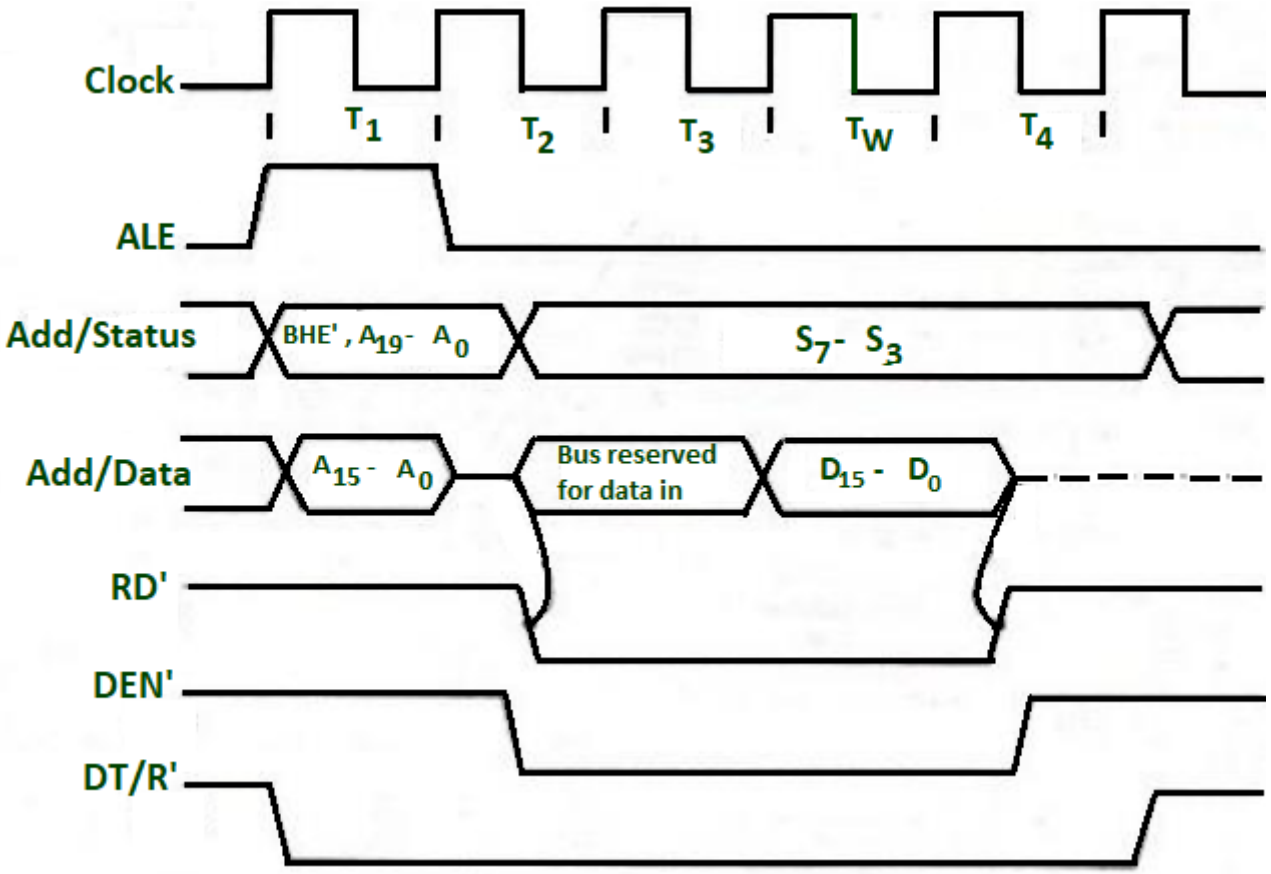
M/IO'	RD'	WR'	Action
1	0	1	Memory Read
1	1	0	Memory Write
0	0	1	I/O Read
0	1	0	I/O Write

- INTR and INTA :
  When INTR = 1,then there is an interrupt to 8086 by other devices for their service. When INTA'= 0,then it indicates that the processor is ready to service them.
- The bus request is made by other devices using the HOLD signal and the processor acknowledges them using the HLDA output signal.
- For more details about the 8086 minimum mode pins please refer(this article).

Timing diagram :

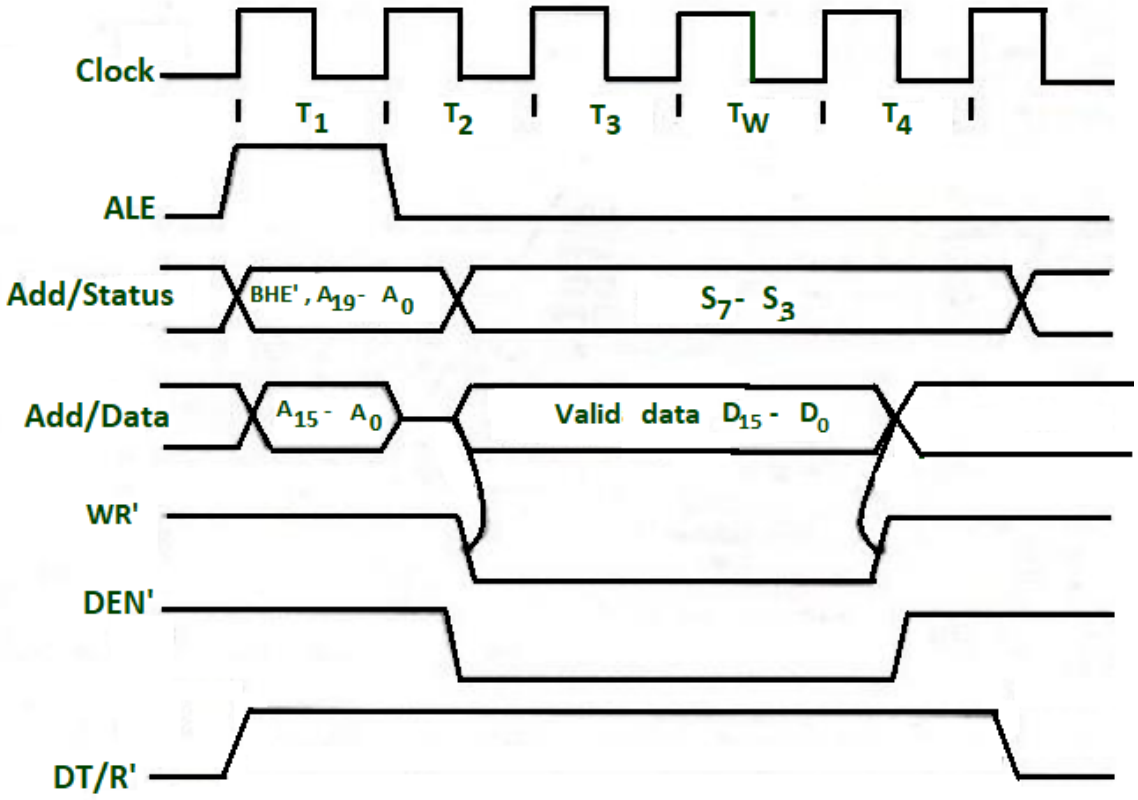
The working of min mode can be easily understood by timing diagrams.

- All processors bus cycle is of at least 4 T-states(T_1,T_2,T_3,T_4) .The address is given by processor in the T1 state. It is available on the bus for one T-state.
- In T_2, the bus is tristated for changing the direction of the bus(in the case of a data read cycle.)
- The data transfer takes place between T_3 and T_4.
- If the addressed device is slower, then the wait state is inserted between T_3 and T_4.



Opcode fetch or read timing diagram

- At T_1 state ALE =1 ,this indicates that a valid address is latched on the address bus and also M / IO'= 1, which indicates the memory operation is in progress.
- In T_2, the address is removed from the local bus and is sent to the addressed device. Then the bus is tristated.
- When RD' = 0 , the valid data is present on the data bus.
- During T_2 DEN' =0, which enables transceivers and DT/R' = 0 ,which indicates that the data is received.
- During T_3, data is put on the data bus and the processor reads it.
- The output device makes the READY line high. This means the output device has performed the data transfer process. When the processor makes the read signal to 1, then the output device will again tristate its bus drivers.



Write memory cycle

- At T_1 state ALE =1 ,this indicates that a valid address is latched on the address bus and also M / IO'= 1, which indicates the memory operation is in progress.
- In T_2, the processor sends the data to be written to the addressed location.
- The data is buffered on the bus until the middle of T_4 state.
- The WR'=0 becomes at the beginning of T_2.
- The BHE' and A0 signals are used to select the byte or bytes of memory or I/O word.
- During T_2 DEN' =0, which enables, transceivers and DT/R' = 1 ,which indicates that the data is transferred by the processor to the addressed device.

All kinds of memory and i/o operations are performed using the decoding of M/IO'and RD' WR' as shown in the table above.