Course Code	Course Name	Credits
CSC405	**Microprocessor**	**3**

Prerequisites: Digital Logic and Computer Architecture	
Course objectives:	
1	To equip students with the fundamental knowledge and basic technical competence in thefield of Microprocessors.
2	To emphasize on instruction set and logic to build assembly language programs.
3	To prepare students for higher processor architectures and embedded systems
Course outcomes: On successful completion of course, learner will be able to:	
1	Describe core concepts of 8086 microprocessor.
2	Interpret the instructions of 8086 and write assembly and Mixed language programs.
3	Identify the specifications of peripheral chip.
4	Design 8086 based system using memory and peripheral chips.
5	Appraise the architecture of advanced processors
6	Understand hyperthreading technology

Module	**Detailed Contents**		**Hours**
1	**The Intel Microprocessors 8086 Architecture**		8
	1.1	8086CPU Architecture,	
	1.2	Programmer's Model	
	1.3	Functional Pin Diagram	
	1.4	Memory Segmentation	
	1.5	Banking in 8086	
	1.6	Demultiplexing of Address/Data bus	
	1.7	Functioning of 8086 in Minimum mode and Maximum mode	
	1.8	Timing diagrams for Read and Write operations in minimum and maximum mode	
	1.9	Interrupt structure and its servicing	
2	**Instruction Set and Programming**		**6**
	2.1	Addressing Modes	
	2.2	Instruction set-Data Transfer Instructions, String Instructions, Logical Instructions, Arithmetic Instructions, Transfer of Control Instructions, Processor Control Instructions	
	2.3	Assembler Directives and Assembly Language Programming, Macros, Procedures	
3	**Memory and Peripherals interfacing**		**8**
	3.1	Memory Interfacing - RAM and ROM Decoding Techniques – Partial and Absolute	
	3.2	8255-PPI-Block diagram, CWR, operating modes, interfacing with 8086.	
	3.3	8257-DMAC-Block diagram, DMA operations and transfer modes.	
	3.4	Programmable Interrupt Controller 8259-Block Diagram, Interfacing the 8259 in single and cascaded mode.	
4	**Intel 80386DX Processor**		**7**
	4.1	Architecture of 80386 microprocessor	
	4.2	80386 registers–General purpose Registers, EFLAGS and Control	

		registers	
	4.3	Real mode, Protected mode, virtual 8086 mode	
	4.4	80386 memory management in Protected Mode – Descriptors and selectors, descriptor tables, the memory paging mechanism	
5	**Pentium Processor**		**6**
	5.1	Pentium Architecture	
	5.2	Superscalar Operation,	
	5.3	Integer &Floating-Point Pipeline Stages,	
	5.4	Branch Prediction Logic,	
	5.5	Cache Organization and	
	5.6	MESI protocol	
6	**Pentium 4**		**4**
	6.1	Comparative study of 8086, 80386, Pentium I, Pentium II and Pentium III	
	6.2	Pentium 4: Net burst micro architecture.	
	6.3	Instruction translation look aside buffer and branch prediction	
	6.4	Hyper threading technology and its use in Pentium 4	

Textbooks:	
1	John Uffenbeck, “8086/8088 family: Design Programming and Interfacing”, PHI.
2	Yu-Cheng Liu, Glenn A. Gibson, “Microcomputer System: The 8086/8088 Family, Architecture, Programming and Design”, Prentice Hall
3	Walter A. Triebel, “The 80386DX Microprocessor: hardware, Software and Interfacing”, Prentice Hall
4	Tom Shanley and Don Anderson, “Pentium Processor System Architecture”, Addison-Wesley.
5	K. M. Bhurchandani and A. K. Ray, “Advanced Microprocessors and Peripherals”, McGraw Hill
References:	
1	Barry B. Brey, “Intel Microprocessors”, 8thEdition, Pearson Education India
2	Douglas Hall, “Microprocessor and Interfacing”, Tata McGraw Hill.
3	Intel Manual
4	Peter Abel, “IBM PC Assembly language and Programming”, 5th Edition, PHI
5	James Antonakons, “The Pentium Microprocessor”, Pearson Education

Assessment:
Internal Assessment Test:
Assessment consists of two class tests of 20 marks each. The first class test is to be conducted when approx. 40% syllabus is completed and second class test when additional 40% syllabus is completed. Duration of each test shall be one hour.
End Semester Theory Examination:
1 Question paper will comprise of 6 questions, each carrying 20 marks.
2 The students need to solve total 4 questions.
3 Question No.1 will be compulsory and based on entire syllabus.
4 Remaining question (Q.2 to Q.6) will be selected from all the modules.

Useful Links	
1	https://swayam.gov.in/nd1_noc20_ee11/preview
2	https://nptel.ac.in/courses/108/105/108105102/
3	https://www.classcentral.com/course/swayam-microprocessors-and-microcontrollers-9894
4	https://www.mooc-list.com/tags/microprocessors