



CSC405 MICROPROCESSORS

8086 ADDRESSING MODES

OBJECTIVE

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To understand 8,16 Addressing modes



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01

8086 Addressing Modes

Instruction

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Opcode Operand

Addressing Mode \rightarrow operands specified in an instruction

- ① Immediate addressing mode
- ② Register addr. mode
- ③ Direct addressing mode
- ④ Indirect addressing mode \leftarrow
- ⑤ Implied addressing mode

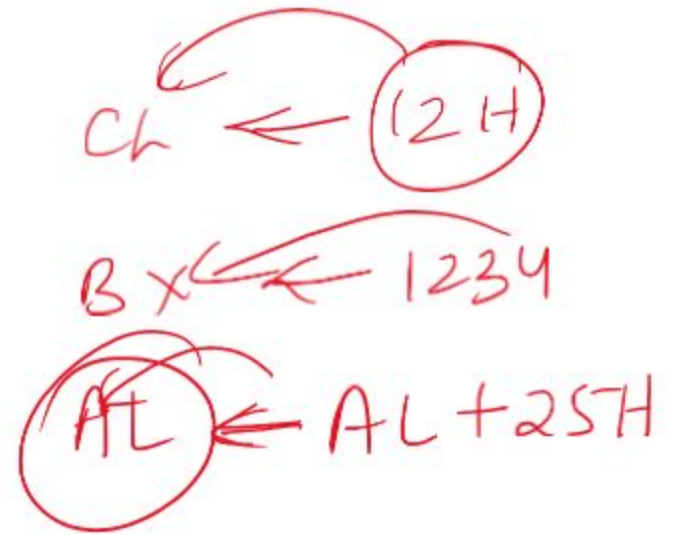
Instruction

Opcode Operand

mov AH, 05h
add AX, BX
sub (AX), [4000]
 ↑

Immediate Addressing mode

eg. `mov CL, 12H`
`mov BX, 1234H`
`ADD AL, 25H`



Register Addressing Mode

eg -
mov CL, BL
mov AX, BX
inc BX

operands \rightarrow registers

$CL \leftarrow BL$

$AX \leftarrow BX$

$BX \leftarrow BX + 1$

Direct Addressing Mode → Address is specified in the instruction

eg. - MOV CL, [2000H]
 $\text{CH} \leftarrow 78$ $\text{CL} \leftarrow \text{DS}:[2000]$

MOV CX, [2000H]
 $\text{CX} \leftarrow \text{DS}:[2000]$ (8 bit)
 $\text{CX} \leftarrow \text{DS}:[2001]$ (8 bit)
 $\text{BL} = 78$

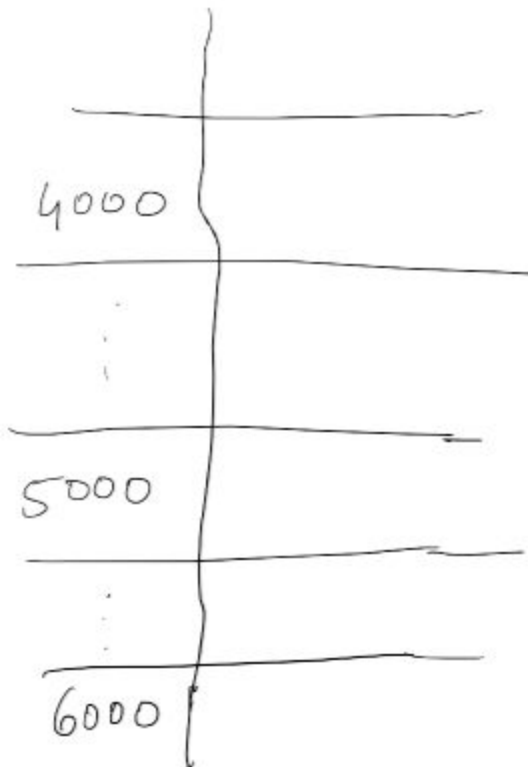
MOV CH, BL
 MOV CH, 78

$\text{CH} + \text{CL}$
 little endian rule

$\text{CH} \leftarrow \text{DS}:[2001]$
 $\text{CL} \leftarrow \text{DS}:[2000]$

0000	
...	
2000	78
2001	86
2002	12
2003	34
...	
FFFF	

Write instructions for following and indicate the addressing modes



Take the data of location 4000 into BL
`MOV BL, [4000H]` ← direct

Take the data of location 5000 into CL
`MOV CL, [5000H]` ← direct

Add the 2 no's and store result in BL.
`ADD BL, CL` ← register

Add 25H, so that result comes in BL.
`ADD BL, 25H` ← immediate

Store the result at location 6000

`MOV [6000H], BL` ← direct
source

Indirect Addressing Mode

1) Register Indirect Addressing Mode

BX, BP

SI, DI

DS \uparrow ES

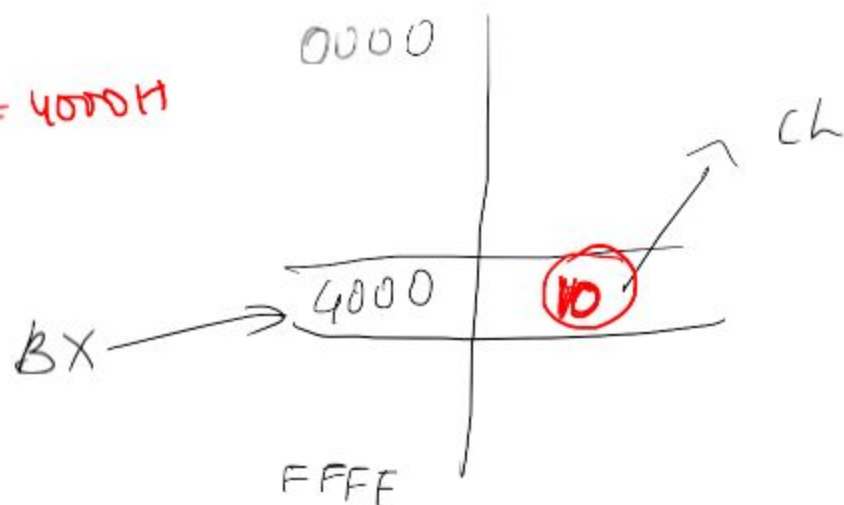
Eg:- MOV CL, [BX]

\rightarrow MOV CL, [4000H]

~~Is direct?~~

\rightarrow Is indirect?

BX = 4000H



MOV CL, [4000H]

CL \leftarrow 10

MOV BX, 4000H BX \leftarrow 4000H
MOV CL, [BX] CL \leftarrow 10

In most of the programming tasks (95% of the time)
indirect addressing mode is used

~~MOV CH, [5000H] ← direct~~

~~MOV CL, [5000H]~~

~~MOV CL, [5001H]~~

~~MOV CL, [5002H]~~

~~MOV CL, [5003H]~~

Rule: -

BX
BP, SI, DI

5000H	10
5001	20
...	
5100H	

MOV BX, 5000H

MOV CH, [BX] } loop

INC BX

CL ← 10

MOV CH, [BP]

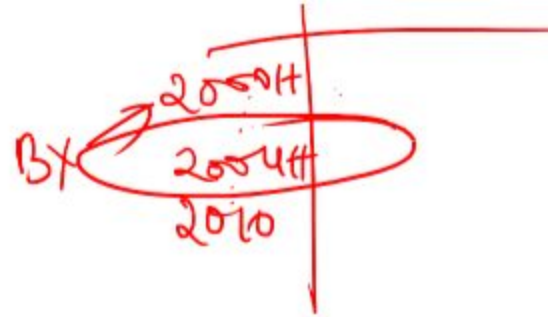
MOV CL, [BX]

Register Relative

Address \leftarrow Register + Displacement

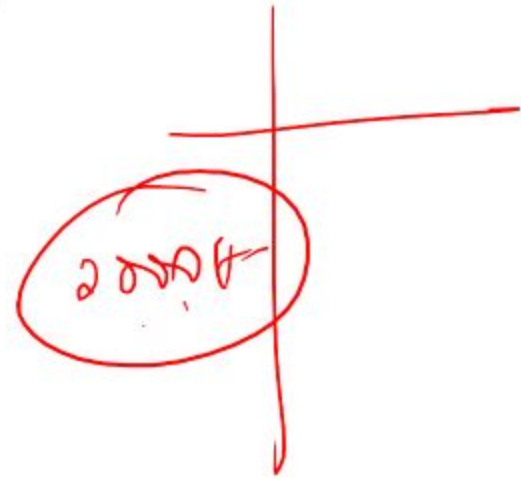
Eg. mov CL, [BX+4] \leftarrow displacement

DS
10



Eg. - mov CL, [BP+05] H

U



Base Indexed

Eg:- `MOV CL, [BX + SI]`

$BX = 2000H$

$SI = 2010H$

~~`MOV CL, [BX + 10H]`~~

~~`MOV CL, [BX + 11H]`~~

~~`MOV CL, [BX + 12H]`~~

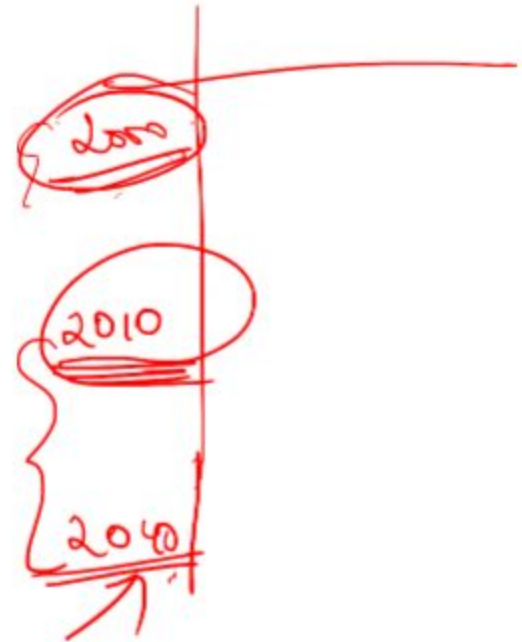
`MOV CL, [BX + SI]`
`INC SI`

} loop

2010H

2011

2012H



Based Relative plus Indexed.

Eg:- $\text{MOV CH}, [\text{BX} + \text{DI} + \text{03H}]$

$\text{MOV CH}, [2013\text{H}]$

Eg. $\text{MOV CH}, [\text{BP}, \text{SI} + \text{05H}]$

$\text{MOV CL}, [\text{DX}]$

Implied Addressing Mode:-

8086
16 bit
Flag register

STC  $C = 1$

CLC clear carry $C = 0$

CLD

STD

DAA

↓
accumulator

mov AX, @data
mov DS, AX

Imm

eg

mov BL, 05H

mov [4000H], 05H

Reg

eg

mov BL, CL

Direct

eg.

mov CL, [7000H]

Indir

Reg indirect

mov CL, [BX]

BX, BP, SI, DI

Reg Relative

mov CL, [BX + 04H]

Base Indexed

mov CL, [BX + SI]

Base Relative + Indirect mov CL, [BX + SI + 03H]

Implied

STC
DAA STD



Thank you