Title

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# Overview

## 

Figure . A basic overview block diagram for an implemented difference of Gaussian filter where a video signal is down sampled, filtered, and up sampled before it is presented to the image buffer writer module. The entire system runs on the video graphics array (VGA) clock.

## Design

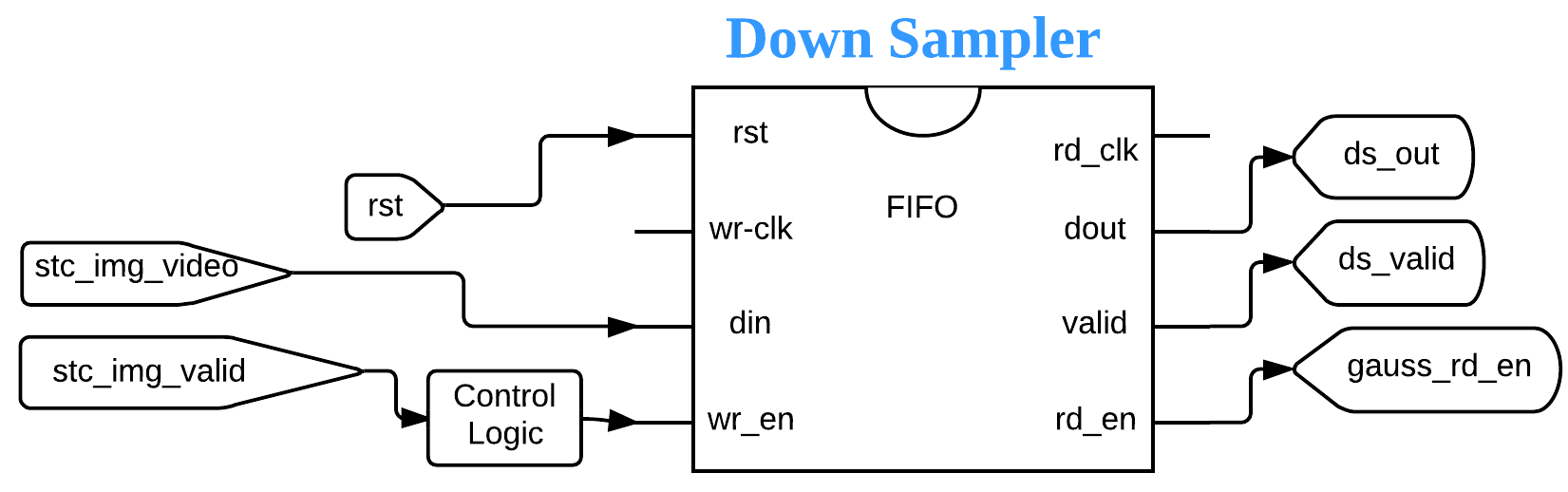


Figure . The Down Sample module takes the video input and down samples it by half.

When video data is transmitted through the down sampler it is becomes half the size and at a decreased image quality. This allows a system to need much less memory then if the image was filtered in its’ original state. Following the operation the data is temporally stored in a transitional first in, first out (FIFO) buffer.

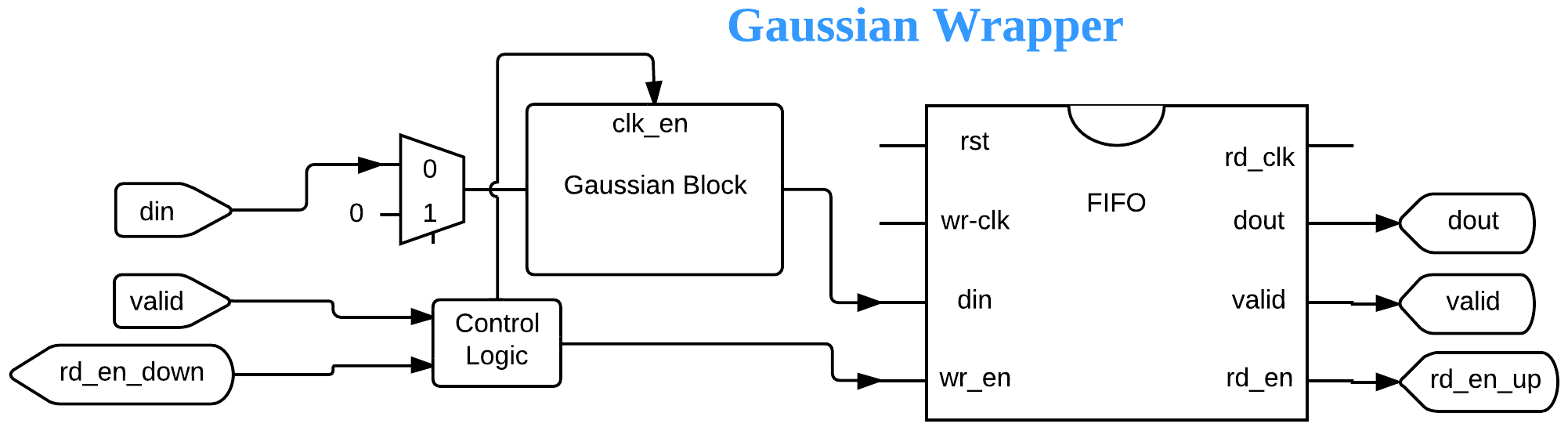
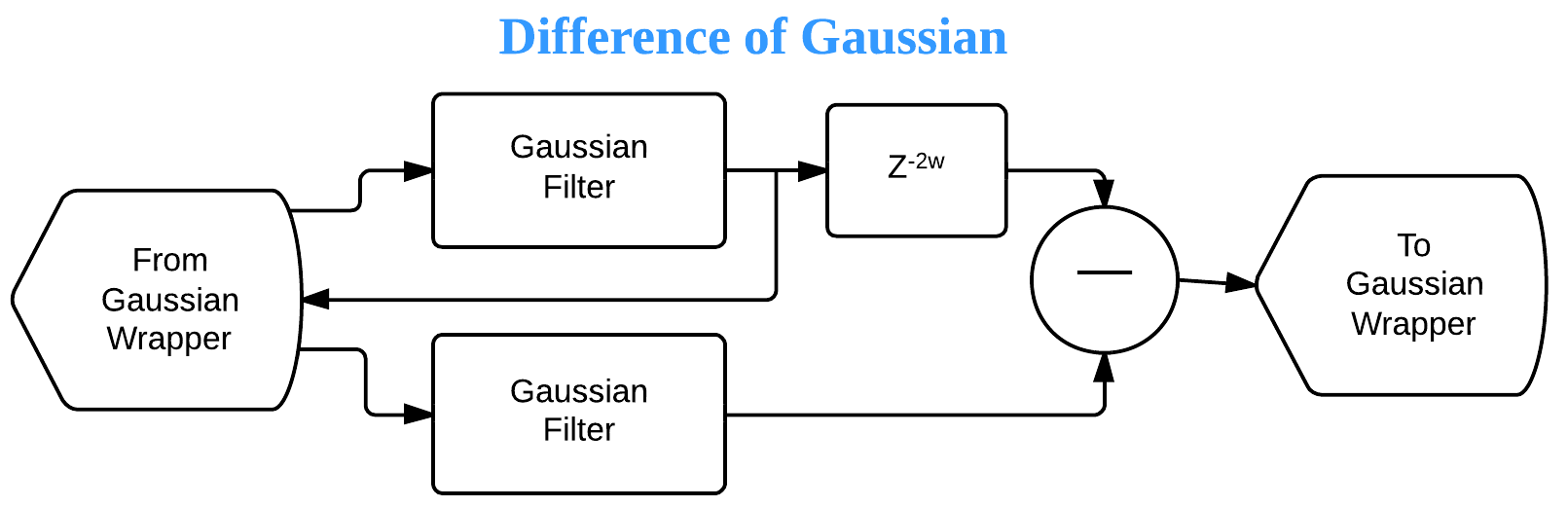
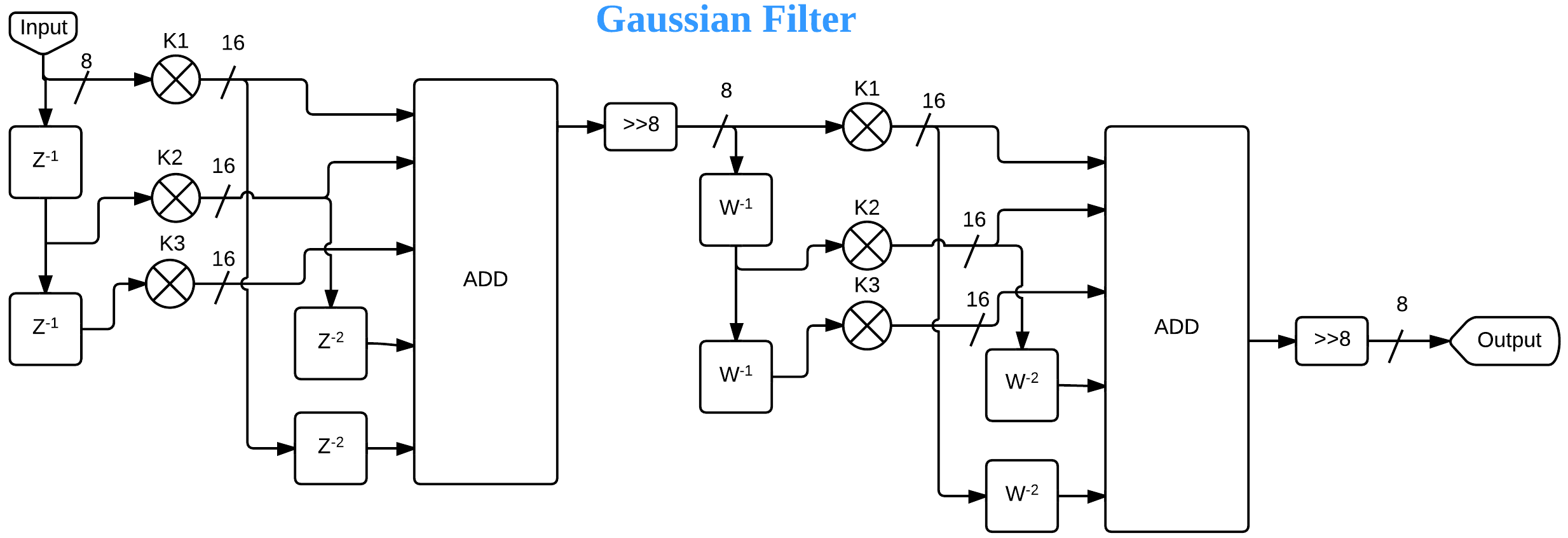
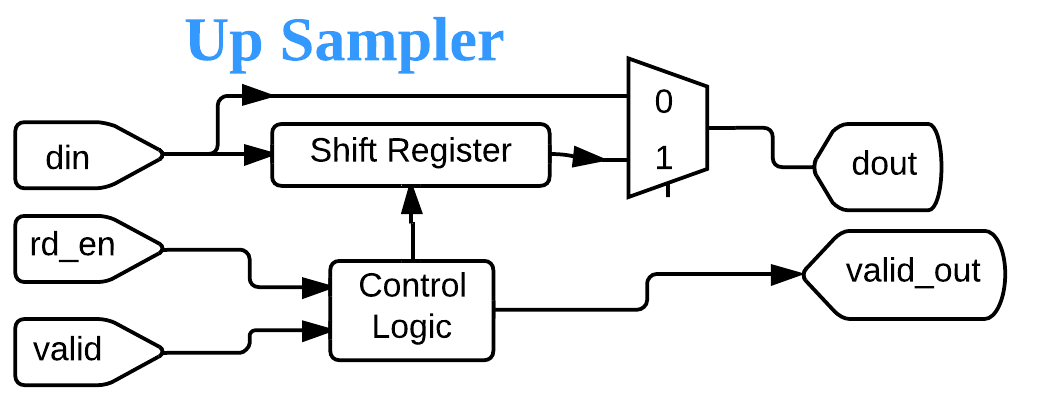


Figure . The Gaussian wrapper takes a data input which prepares the data to be filtered.







i. You may draw this by hand, but use a straight edge at least

ii. make sure to identify and label the various clock domains

## Brief Description of Major Sub-Modules

i. Keep this part short

ii. Don’t bother telling us what we already know (DVI interface, ImageBufferWriter, etc)

# Detailed System Description

The detailed system description can start with functional and input/output specifications. Modules can be described in order from input to output, or from most to least important module. Illustrate the descriptions with the block diagrams and timing diagrams you have prepared; refer to these as figures. Don’t bother going into the details of very simple modules. However, do give detailed descriptions and figures for modules like your Difference of Gaussians filter stack.

## Data Path

i. Connections to SRAM

ii. We want LOTS of details on your difference-of-Gaussians filter blocks,

connections to frame buffer and connections to ImageBufferWriter

iii. Down sampler and up sampler

## Control

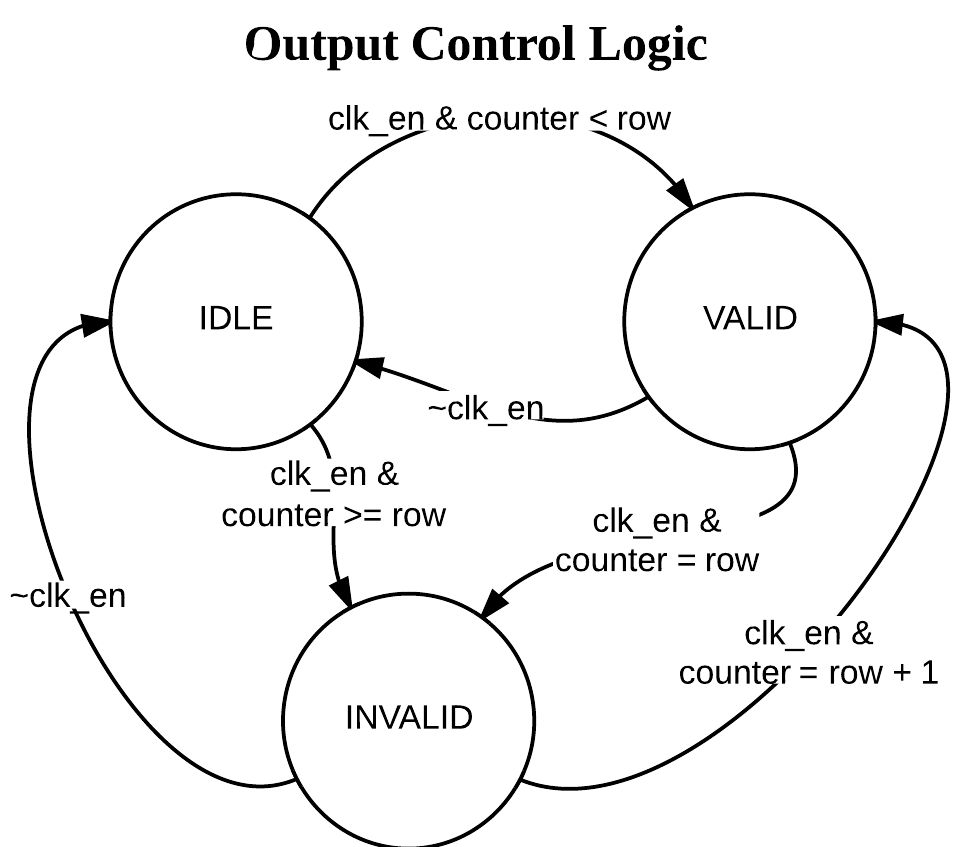
i. How do you deal with any addressing issues, including blank rows or columns?

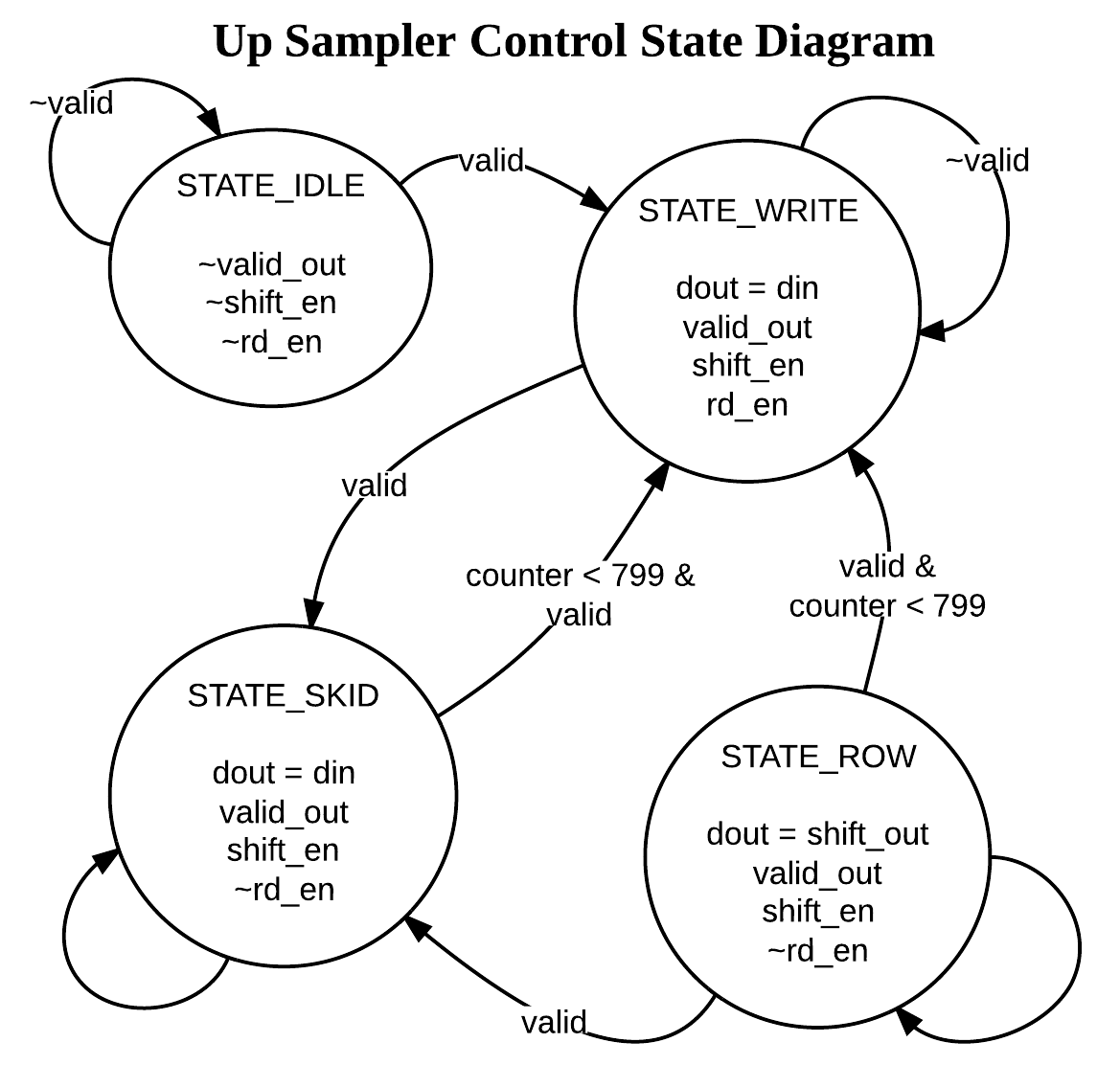
ii. What was your general control design (e.g. multiple FSM, counter based

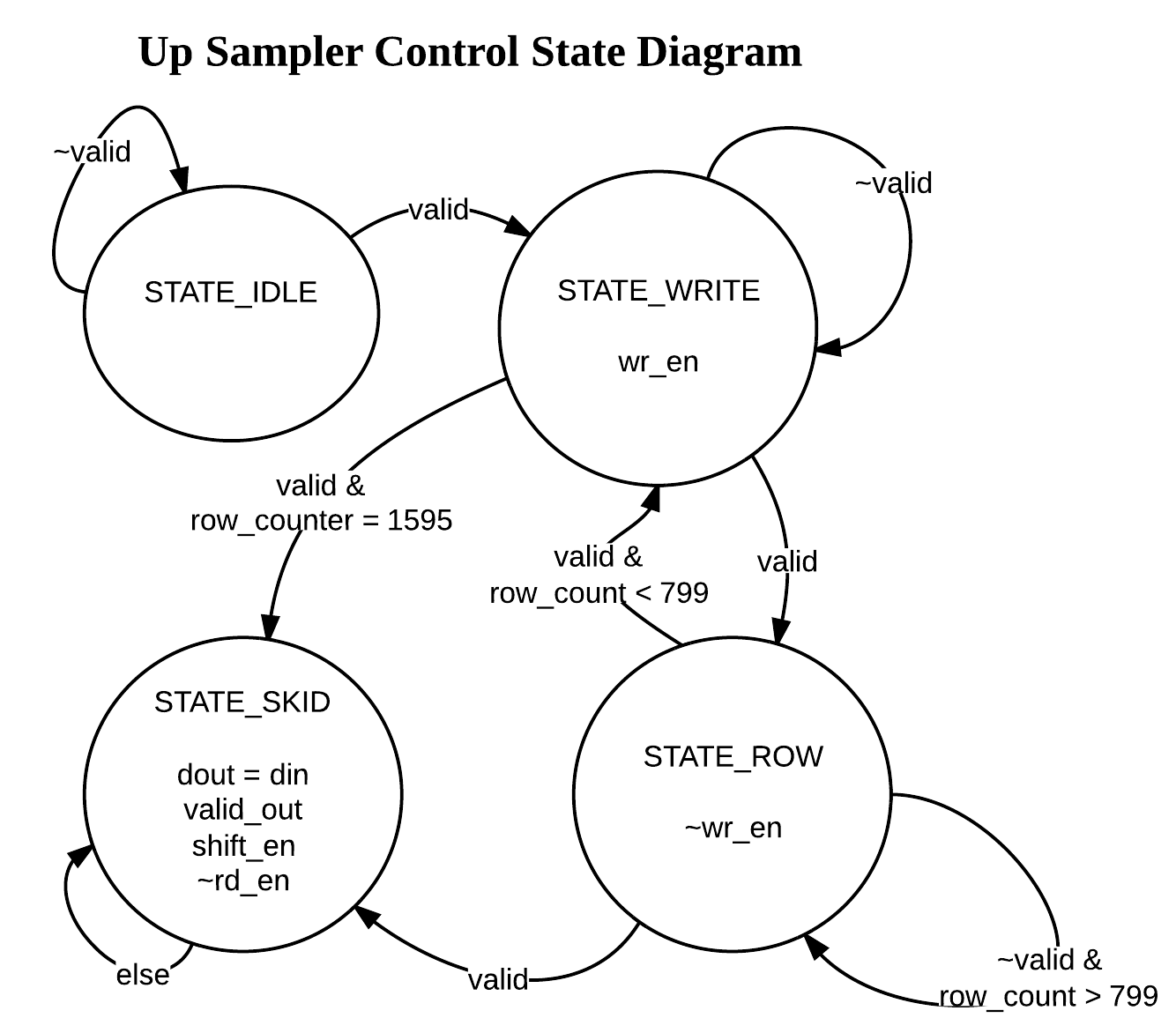
control, etc.)

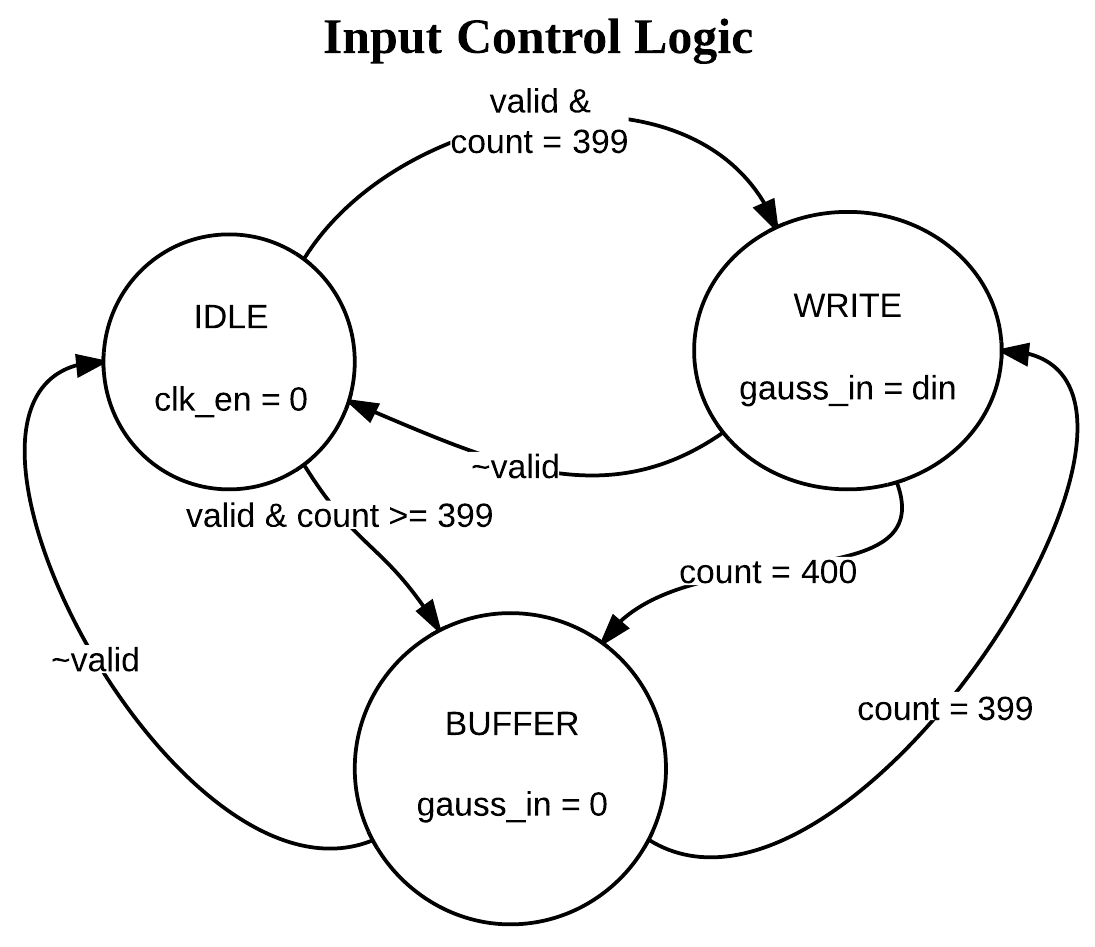
iii. State diagrams and functional timing diagrams for key operations (e.g.

Ready/Valid signals as appropriate).









## Design Decisions and Tradeoffs

Describe design decisions you made for clock rates, extra FIR padding pixels,  Moore vs. Mealy controllers, etc.

What problems did you encounter during implementation and debugging? How  did you resolve those issues or change design decisions?

# DESIGN METRICS

a. Critical timing path for your design, and maximum clock rate

b. Number of 6-LUTs, BlockRAMs

i. How many more Gaussian filter blocks could be added within available

resources?

## Division of labor

How did you organize yourselves as a team? Exactly who did what?

Estimate labor hours spent in design/debug etc.

# CONCLUSION

a. Summary of main features

b. What would you do differently next time

# ACKNOWLEDGMENTS

# REFERENCES

# APPENDICES