

Implementation of low power thermometer code to digital converter using Wallace Tree Encoder

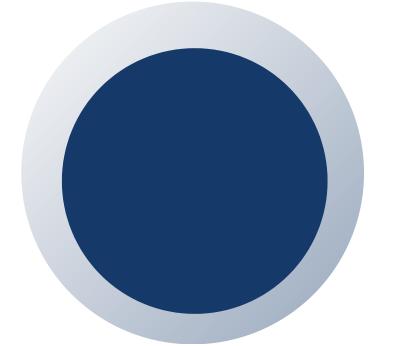
Team Members

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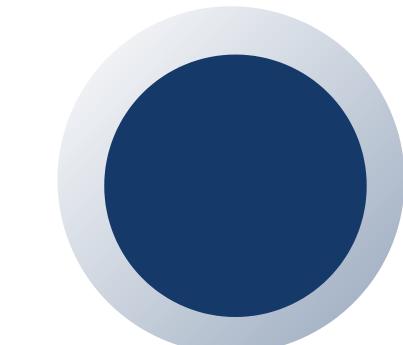
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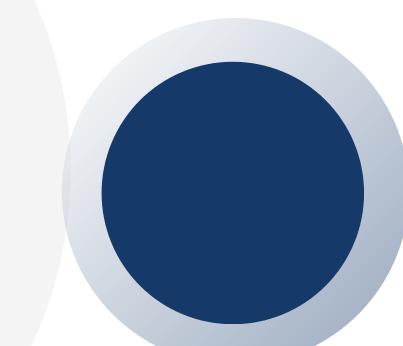
Our Objectives



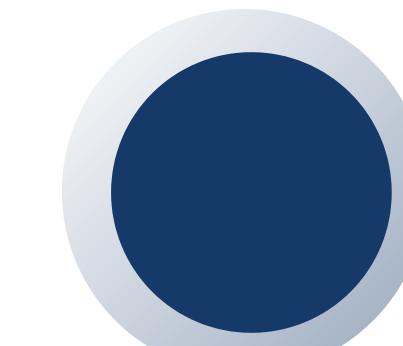
To design a low power , high speed WTE suitable for flash Analog to Digital Converters.



To minimize power,transistor count, and propagation delay in the encoder design.



To implement a modified transmission gate-based full adder to optimize the encoder's performance.



To simulate and validate the proposed design using cadence with 90nm CMOS technology.

Motivation

- **The major drawbacks**

- High power consumption
- Large transistor count
- Propagation delay

- **To overcome**

- Use of transmission gate based FA
- Minimize transistor count
- Optimize the conventional FA with transmission gate logic

Methodology

1. Study of Existing Encoder Design:

Study of existing Wallace Tree Encoder using 28-transistor CMOS full adders reveals inefficiencies in power, delay, and transistor count.

2. Design of Modified Full Adder:

Design of a modified full adder using transmission gate logic (TG) reduces transistor count from 28 to 10, optimizing area and power efficiency.

3. Design of Proposed Wallace Tree Encoder:

The proposed Wallace Tree Encoder integrates TG-based full adders into a 15:4 architecture, converting a 15-bit thermometer code to a 4-bit binary output (b_3-b_0).

4. Simulation and Verification:

Simulation and verification of the proposed 15:4 Wallace Tree Encoder using Cadence Virtuoso (90nm, 1V) includes performance analysis of delay, power, and transistor count versus the conventional design.

Working

1. Input Format:

A 15-bit thermometer code encoder converts a contiguous sequence of '1's from the LSB followed by '0's into a binary number equal to the count of '1's.

2. Wallace Tree Encoding Process:

Stage 1 – Grouping: the 15 input bits are divided into five 3-bit sets, each processed by a 10T full adder to produce one SUM bit (same weight) and one CARRY bit (passed to the next stage).

Stage 2 – Compression: SUM and CARRY outputs are repeatedly grouped into triplets and compressed using full adders until only two rows of partial sums remain.

Stage 3 – Final Summation: The final two rows are summed using a ripple carry adder to produce a 4-bit binary output representing the count of '1's in the thermometer code.

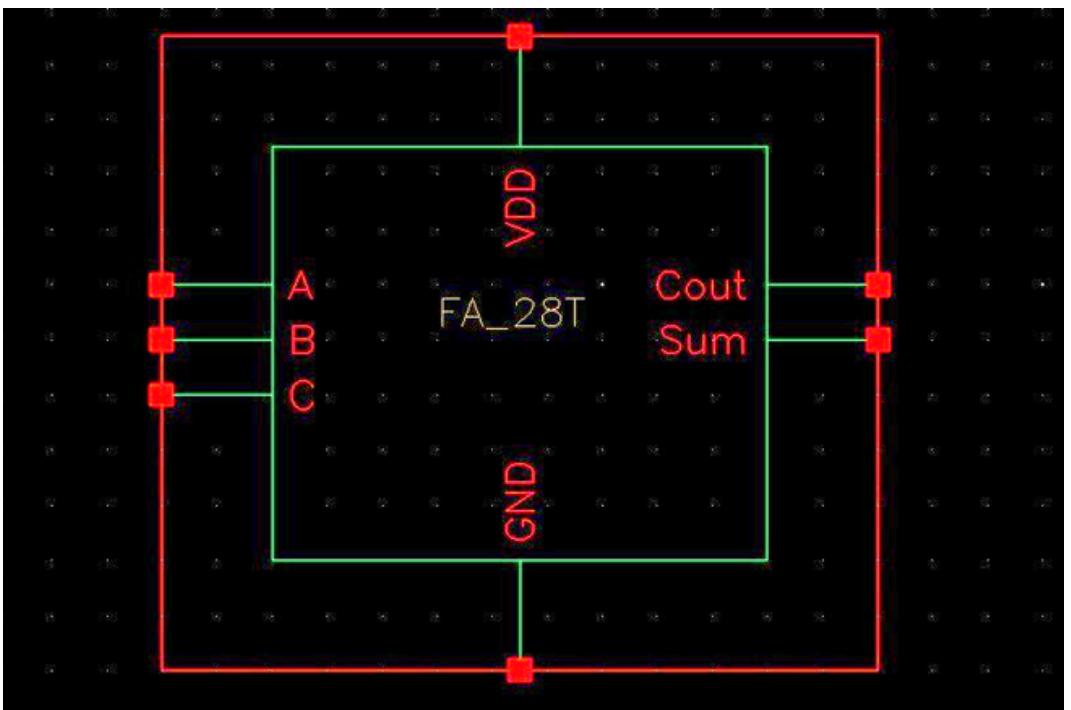
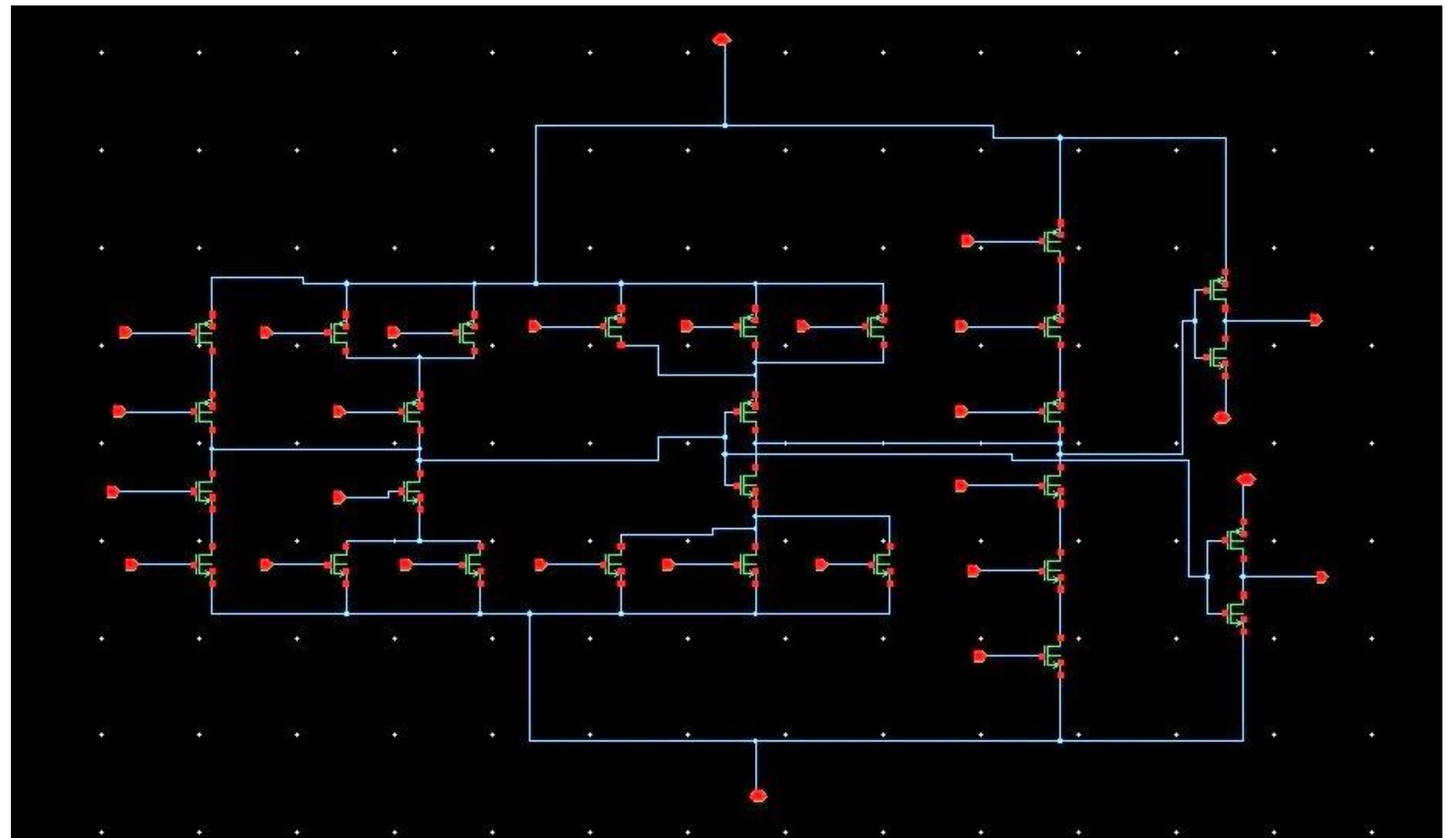
3. Hardware Design Comparison:

Feature	10T Full Adder	28T Full Adder
Number of Transistors	10	28
Power Dissipation	330.5 nW	822.4 nW
Delay	0.5115 ns	1.4 ms
Area	Smaller	Larger
Voltage Swing	Slightly Reduced	High
Efficiency	Higher	Lower
Technology Used	90nm CMOS	90nm CMOS

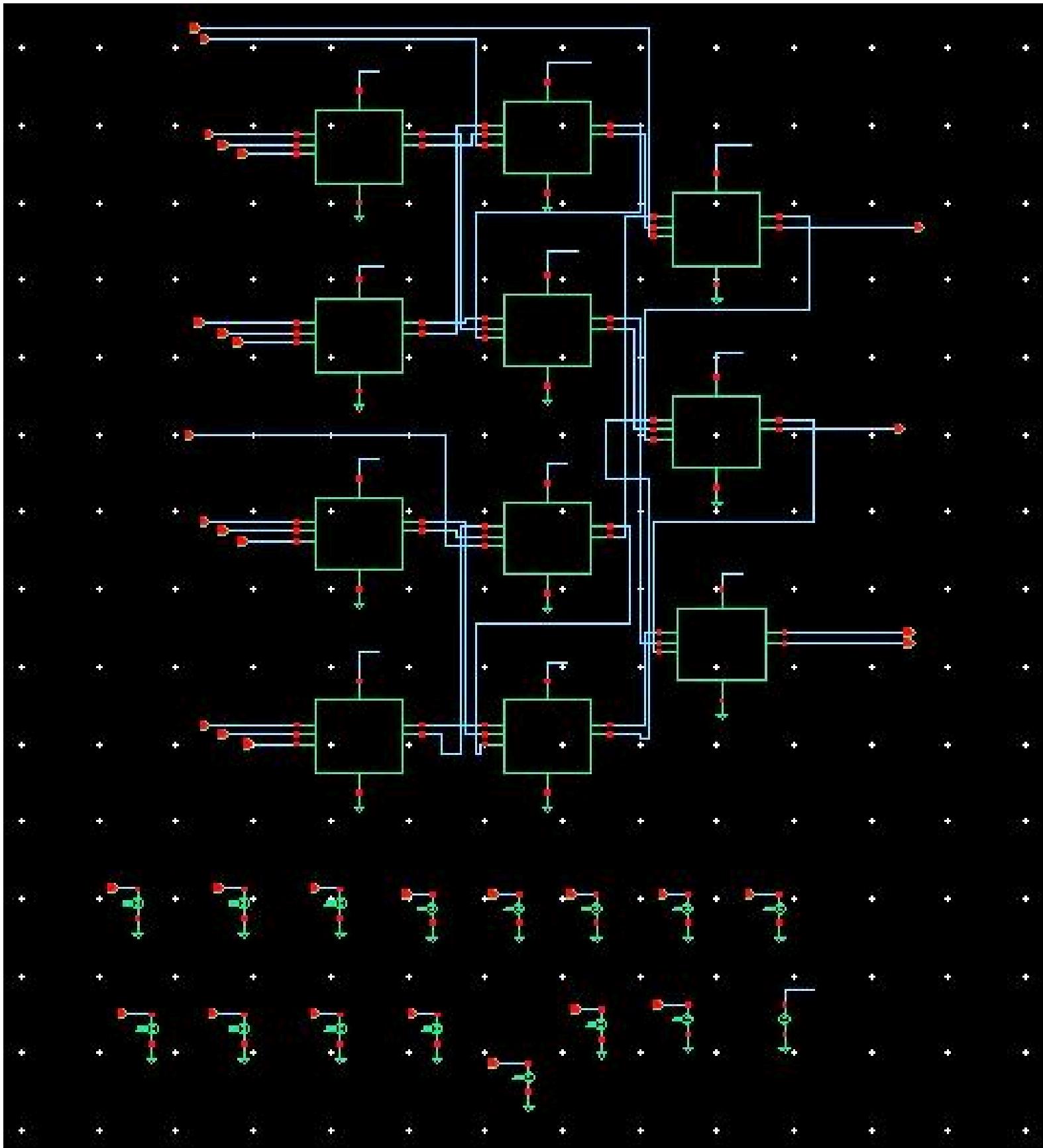
4. Tools Used:

- **Cadence Virtuoso:** Used for schematic design, simulation, and analysis of the full adder and encoder circuits.
- **90nm CMOS Technology:** Used for modeling transistor behavior, evaluating power consumption, and estimating delay characteristics of the proposed design.

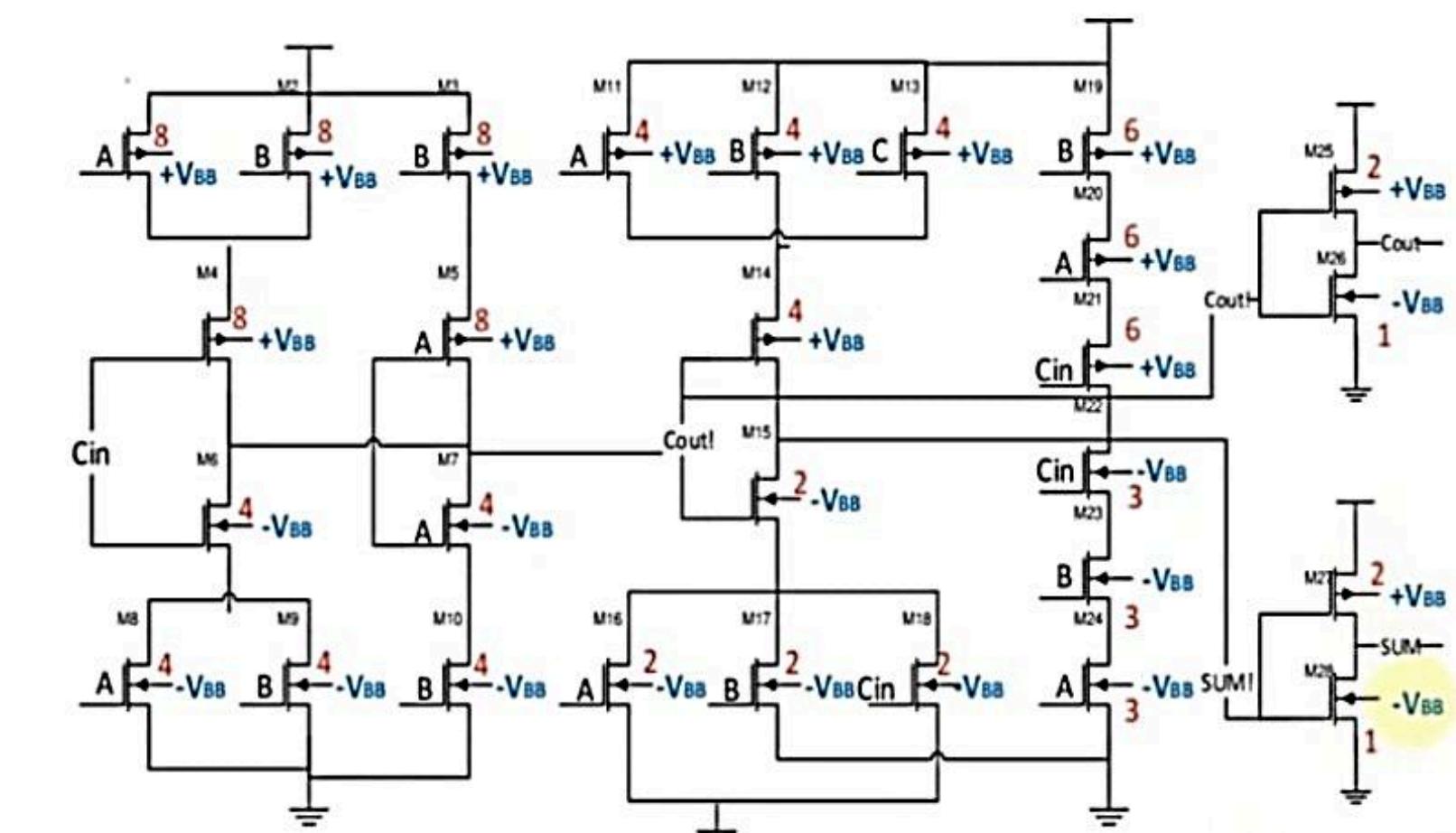
28T FullAdder Design



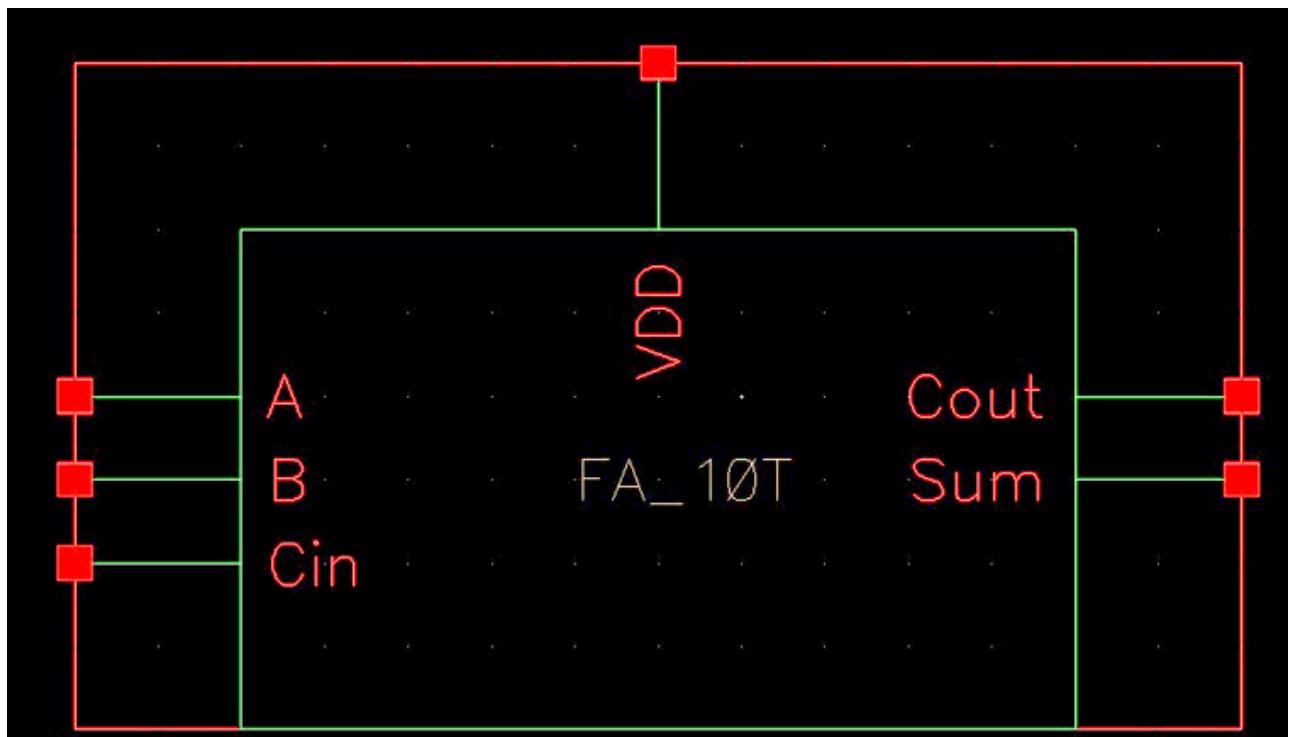
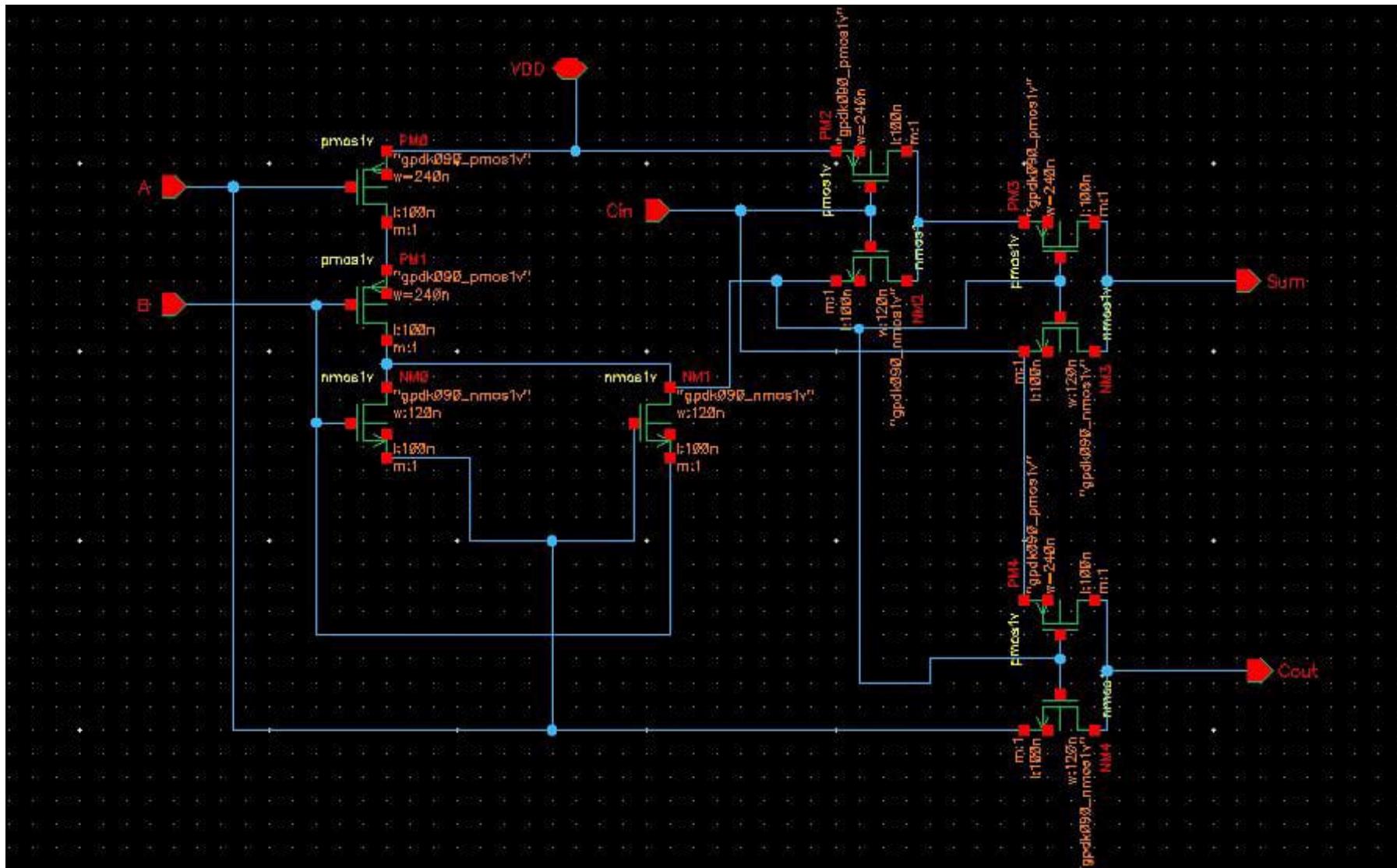
Encoder using 28T FullAdder



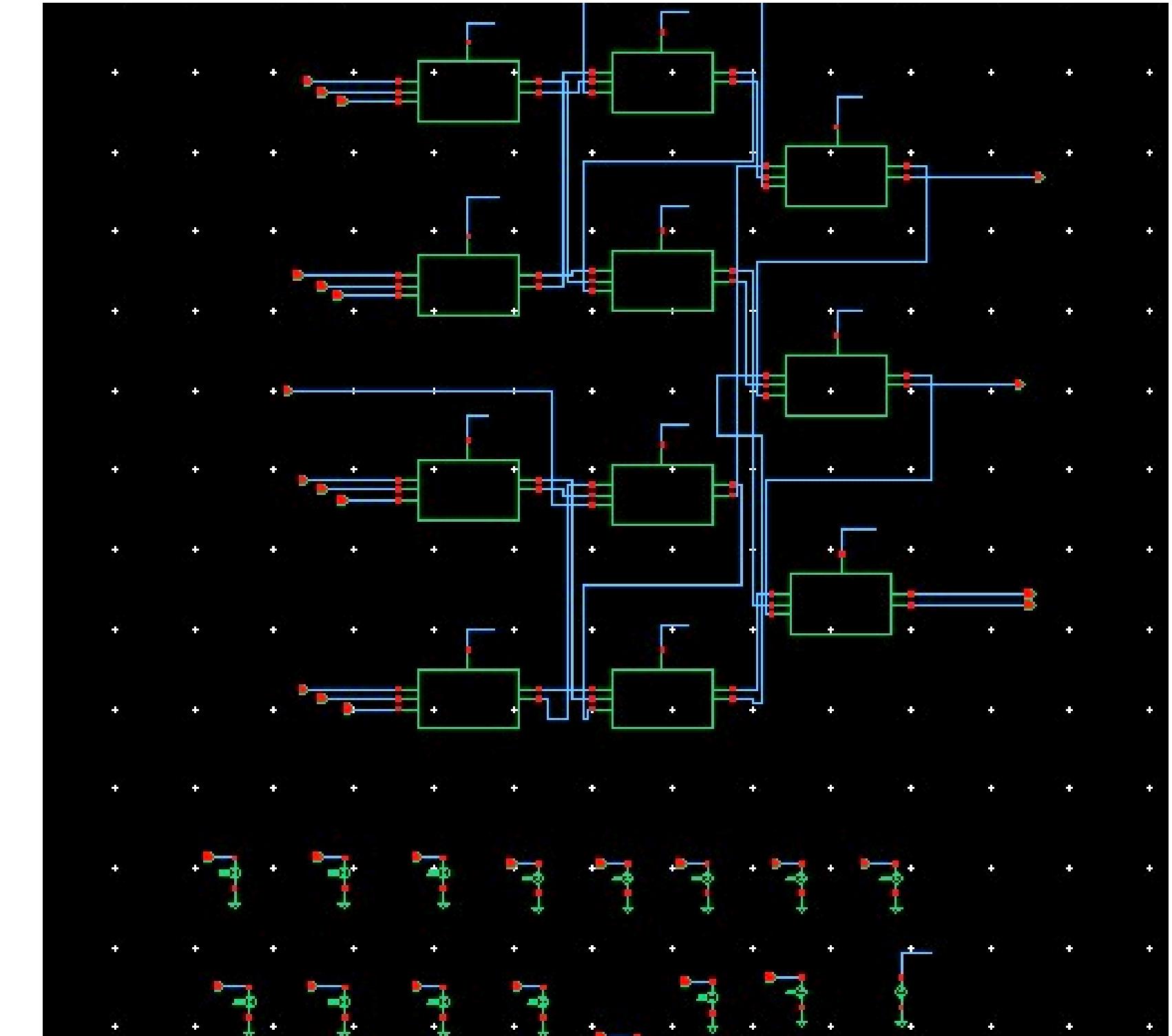
Sizing of 28T FullAdder



10T FullAdder Design



Encoder using 10T FullAdder

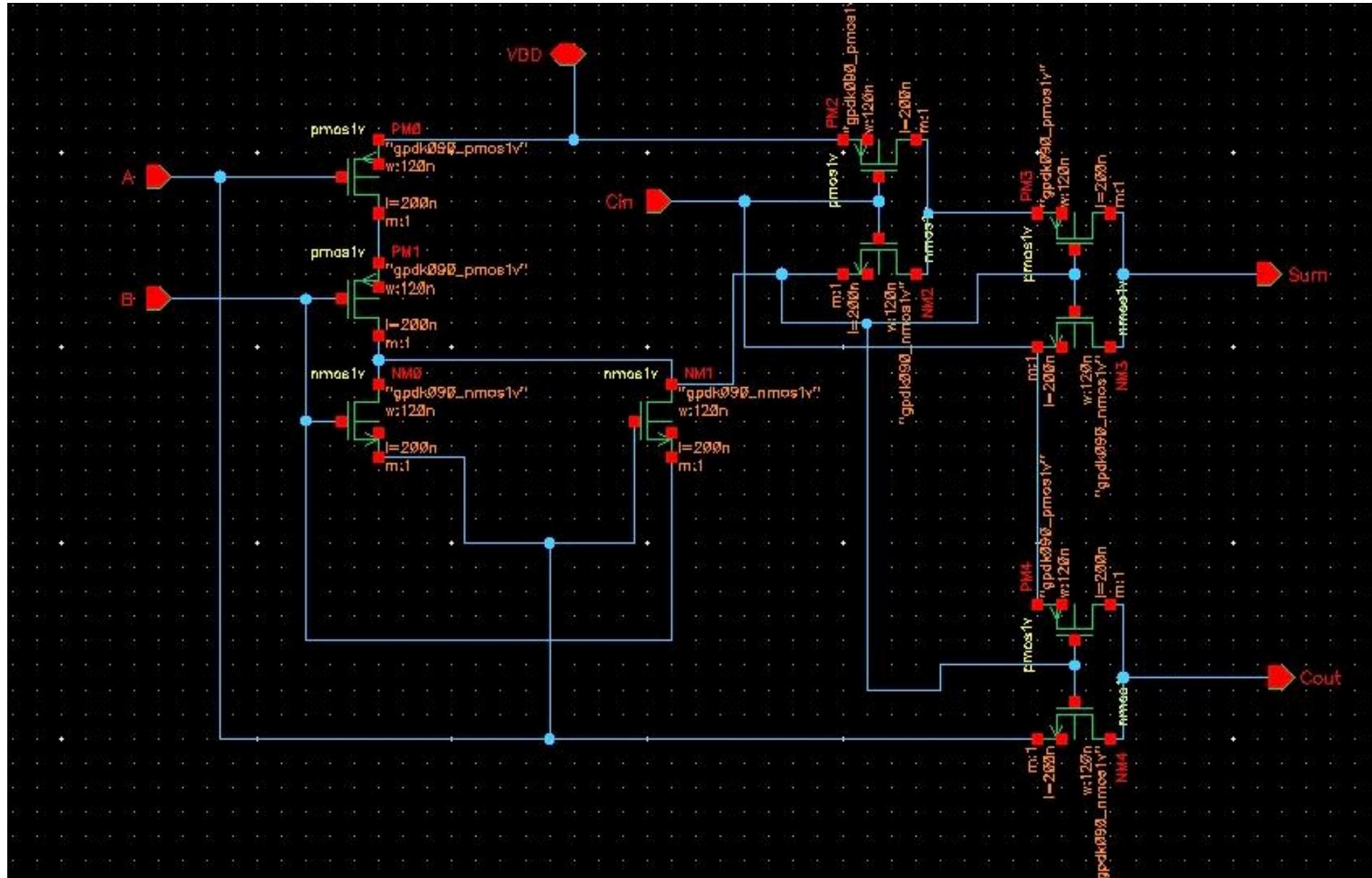


Sizing of mosfets

W_n= 120nm L_n=100nm

W_p= 240nm L_p=100nm

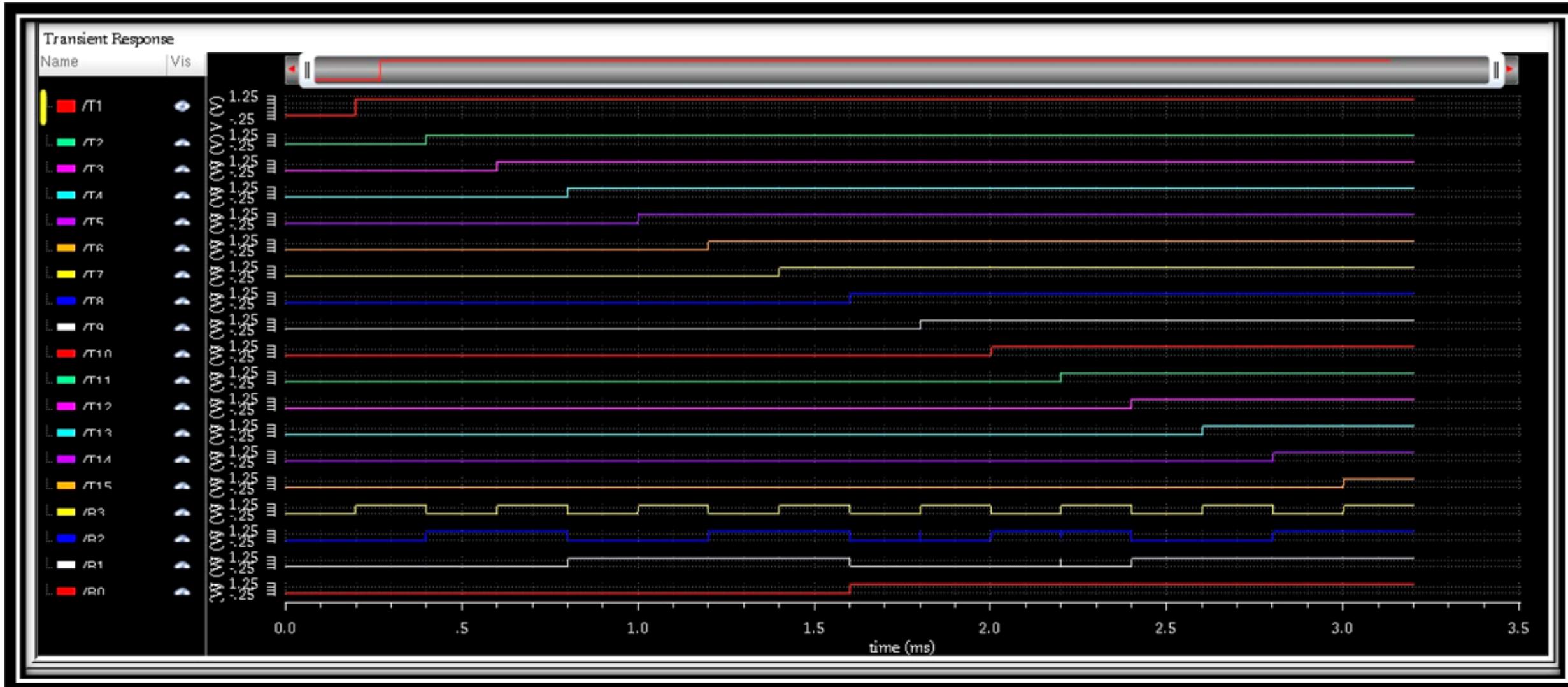
10T FullAdder(power optimised) Design



Sizing of mosfets

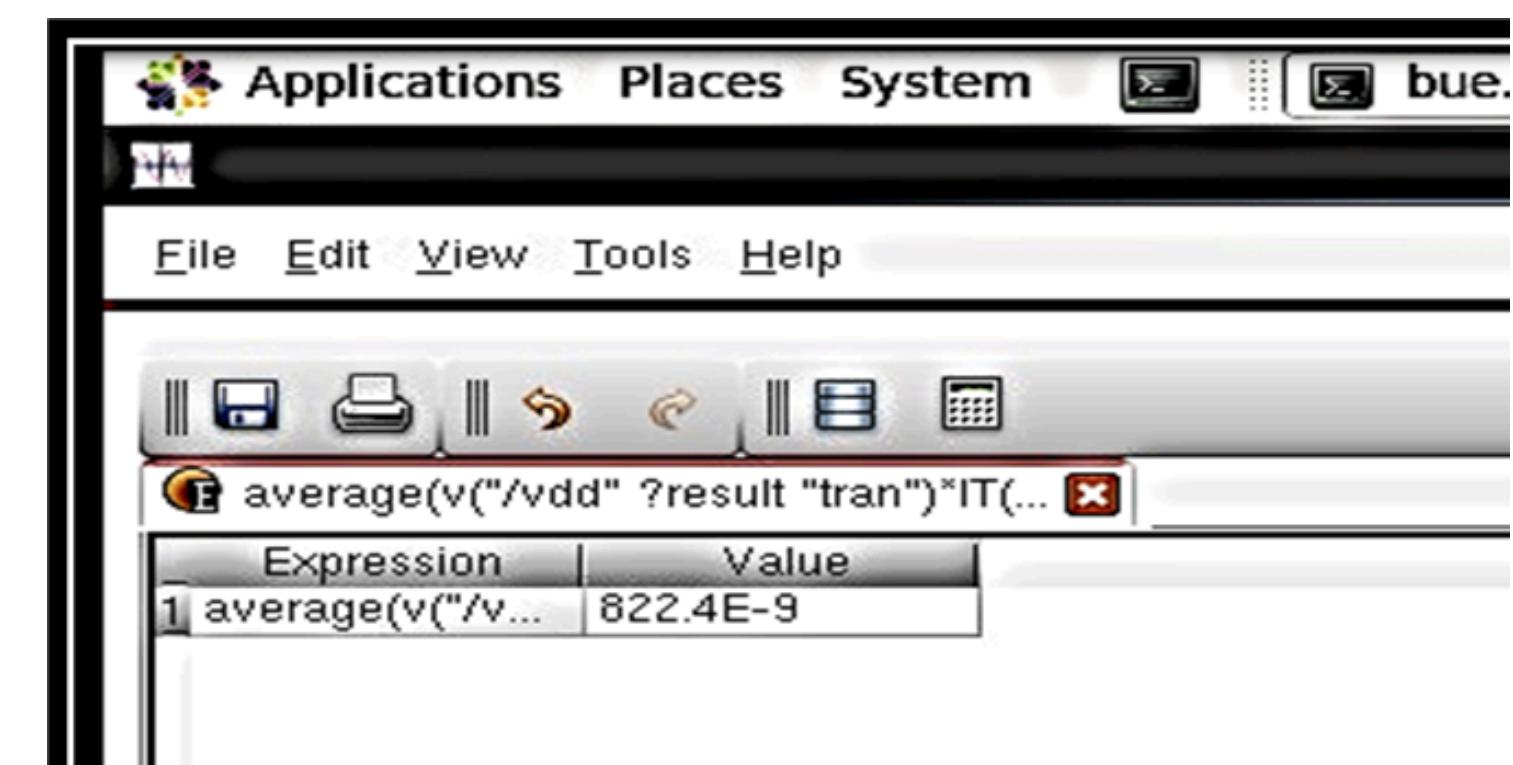
$W_n = 120\text{nm}$ $L_n = 200\text{nm}$
 $W_p = 120\text{nm}$ $L_p = 200\text{nm}$

1. Outcomes of the 28-T Wallace Encoder :

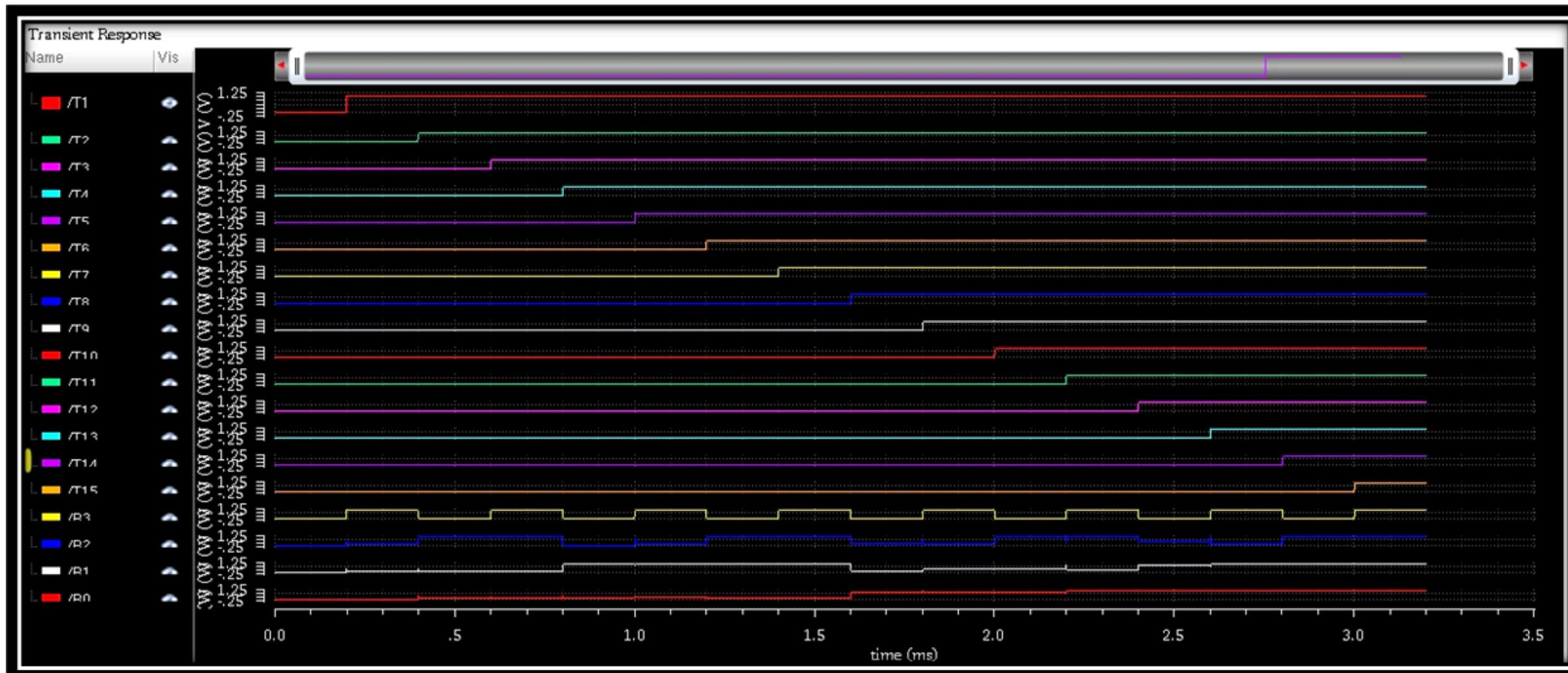


Power Calculation

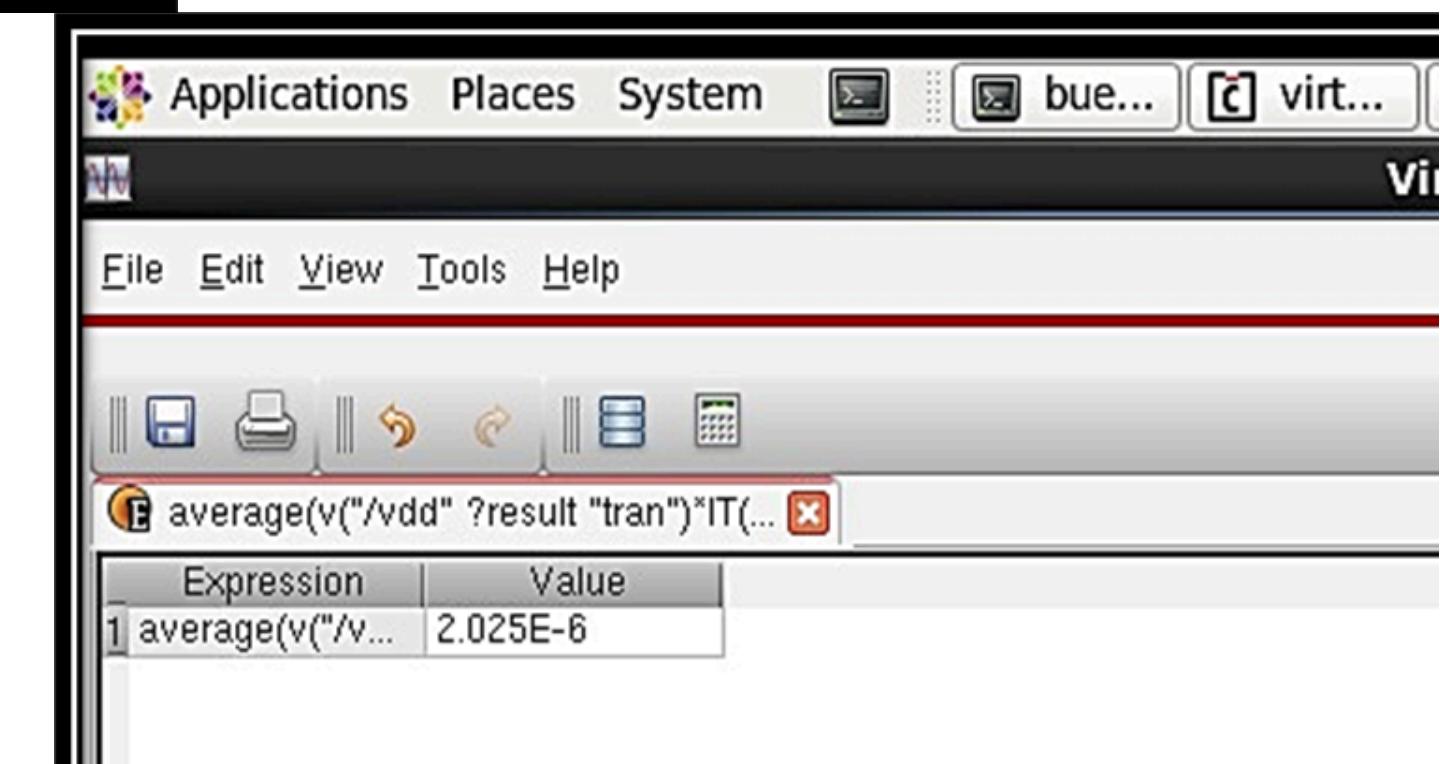
Max delay is for T1 with B0
, which is 1.4ms



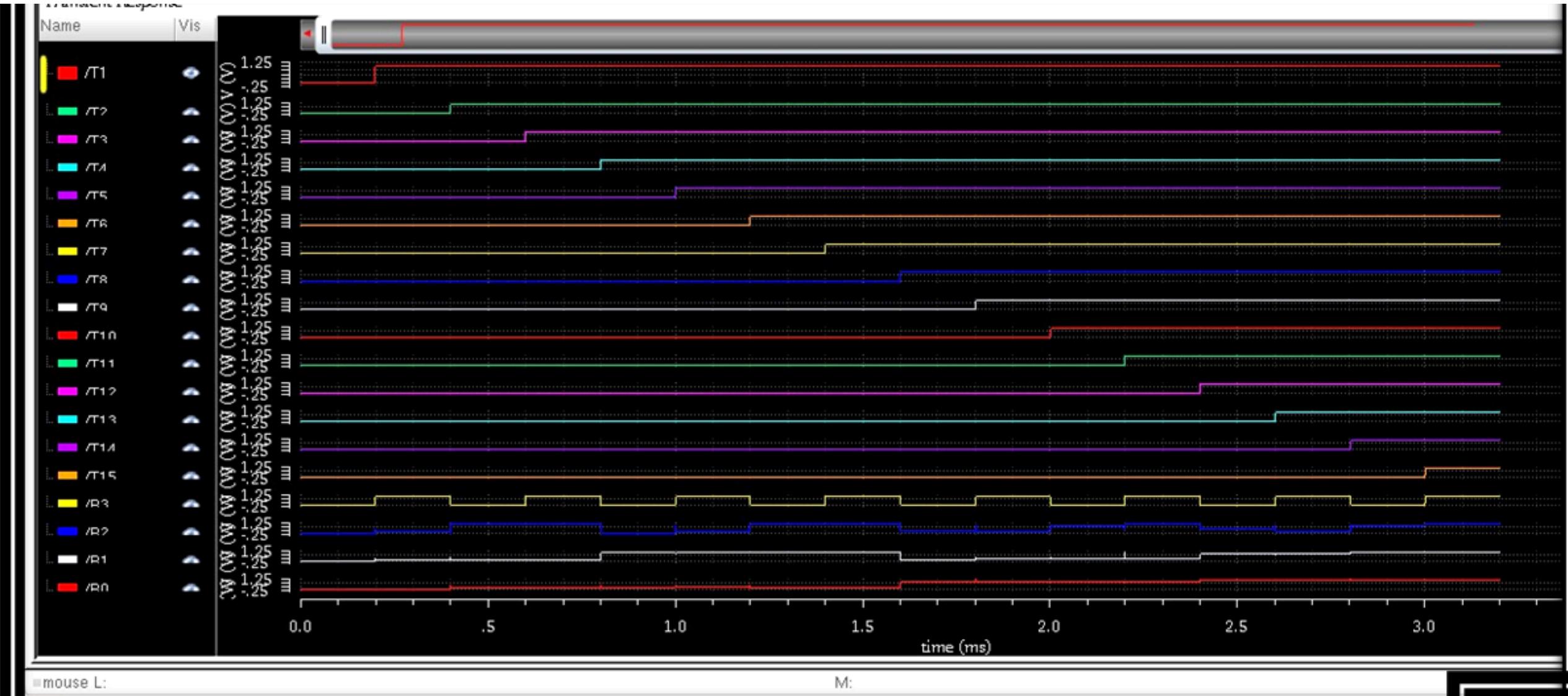
2. Outcomes of the 10-T Wallace Encoder for size $L=100\text{nm}$, $W_n=120\text{nm}$, $W_p=240\text{nm}$:



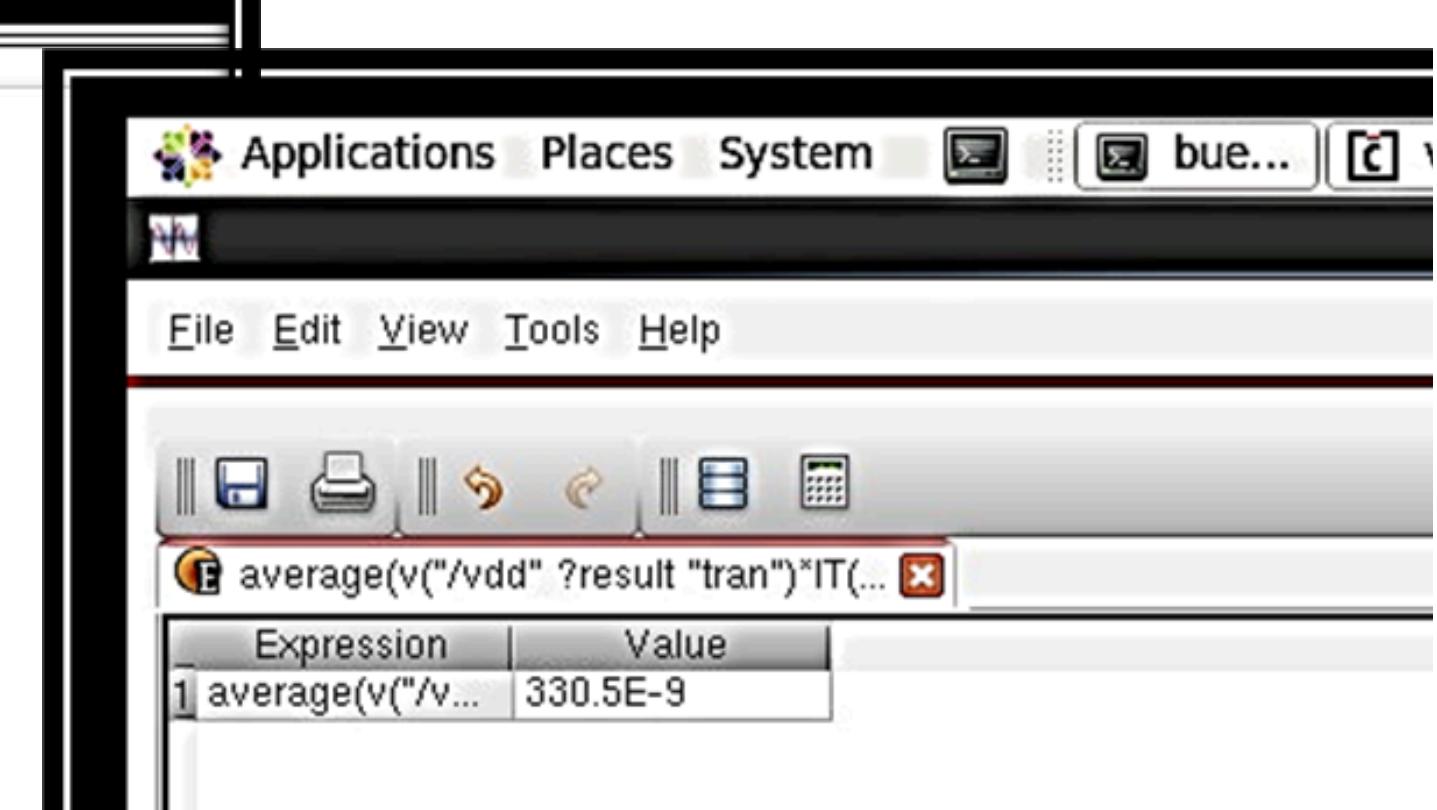
Power Calculation



3. Outcomes of the 10-T Wallace Encoder for size L=200nm,Wn=Wp=120nm :



Power Calculation



Max delay is for T1 with
B3, which is 0.5115ns

Conclusion

- The proposed Wallace Tree Encoder, implemented with a modified transmission gate-based full adder, significantly improves performance over traditional designs.
- It achieves lower power consumption (330.5nW), reduced delay (0.5115 ns), and a smaller transistor count compared to the existing design.
- This demonstrates that transmission gate logic is effective in designing high-speed, low-power VLSI circuits, making it suitable for modern Flash ADC applications.

THANK
YOU

