32 BIT RISC V PROCESSOR

A Report Submitted in partial fulfilment of the Term-Project in

VLSI CAD carried out at NITK Surathkal

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ABSTRACT:

This report presents a comprehensive overview of the RTL-to-GDSII ASIC design flow for the PicoRV32 processor core using the OpenROAD-flow-scripts framework. Covering the entire process from Register Transfer Level (RTL) Verilog description to the final generation of Graphic Data System II (GDSII) layout files, OpenROAD offers a fully open-source digital ASIC implementation platform. The report explores each stage of the digital backend flow including logic synthesis, floorplanning, placement, clock tree synthesis, and global and detailed routing. The PicoRV32, a minimal RISC-V RV32I processor core, is chosen for its simplicity and configurability, making it an ideal candidate for ASIC prototyping. This work highlights the capabilities and challenges of using open-source tools in ASIC workflows, focusing on design convergence, timing-driven placement, and layout generation.

INTRODUCTION:

With the increasing adoption of open-source IPs and tools in the hardware design industry, the development and prototyping of Application-Specific Integrated Circuits (ASICs) using fully open-source flows have gained significant traction. RISC-V, an open standard instruction set architecture (ISA), has become a cornerstone in this movement. Among its many implementations, PicoRV32 stands out as a compact, RV32I-compliant soft-core processor optimized for resource-constrained environments. This project focuses on the ASIC design of the PicoRV32 core using OpenROAD-flow-scripts, a fully automated RTL-to-GDSII flow built around the OpenROAD toolchain. Unlike traditional commercial EDA tools, OpenROAD enables a transparent and flexible environment for digital backend design. This implementation leverages PicoRV32's streamlined instruction set and compact architecture to explore the capabilities of the open-source flow.

OBJECTIVE:

The objective of this project is to design and implement a 32-bit RISC-V processor core PicoRV32 using the OpenROAD-flow-scripts RTL-to-GDSII digital design flow. The primary aim is to generate a GDSII layout from the RTL description of the processor while utilizing a fully open-source toolchain. Key goals include synthesizing the design for optimal area and performance, performing physical design steps such as floorplanning, placement, clock tree synthesis, and routing, and achieving design closure without the inclusion of physical verification stages. This project intends to demonstrate a practical understanding of the digital backend flow using open-source ASIC tools, and to provide comprehensive documentation of the process, challenges encountered, and the resulting layout metrics.

TOOLS USED:

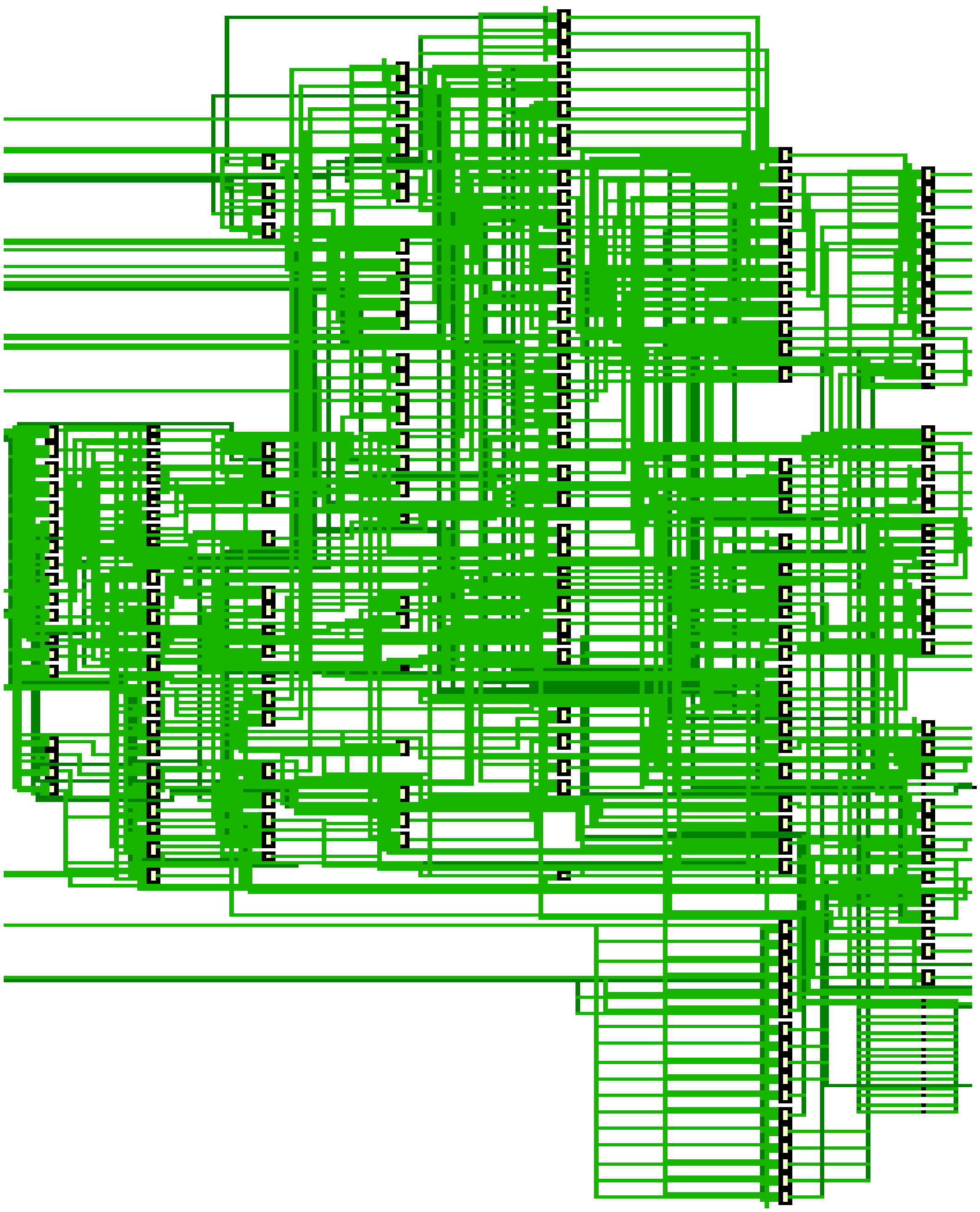
1. Xilinx Vivado
2. Yosys
3. OpenROAD
4. OpenROAD gui
5. Klayout

PICORV32:

PicoRV32 is a compact, open-source RISC-V processor core designed for minimal area and high configurability. It supports the RV32I instruction set with optional extensions like RV32M (multiply/divide) and RV32C (compressed instructions). Unlike traditional pipelined processors, PicoRV32 uses a finite state machine (FSM)-based, multi-cycle architecture, where each instruction is executed over several clock cycles. This simplifies control logic and reduces hardware resource usage, making it ideal for FPGA and low-power ASIC implementations. It also includes optional support for interrupts, co-processor integration, and interfaces like AXI4-Lite and Wishbone.

IMPLEMENTATION:

RTL Analysis – Schematic:



Synthesis(YOSYS):

1.

```
=== design hierarchy ===

   picorv32a                         1
     picorv32_pcpi_fast_mul          1

   Number of wires:              14477
   Number of wire bits:          18024
   Number of public wires:         202
   Number of public wire bits:    2451
   Number of memories:               0
   Number of memory bits:            0
   Number of processes:              0
   Number of cells:              16482
     $_ANDNOT_                    3912
     $_AND_                       1422
     $_DFFE_PP_                    957
     $_DFF_P_                      227
     $_MUX_                       1885
     $_NAND_                       747
     $_NOR_                        504
     $_NOT_                        915
     $_ORNOT_                      228
     $_OR_                        2315
     $_SDFFCE_PN0P_                 36
     $_SDFFCE_PP0P_                  9
     $_SDFFCE_PP1P_                  1
     $_SDFFE_PN0P_                 192
     $_SDFFE_PN1N_                   4
     $_SDFFE_PN1P_                  32
     $_SDFFE_PP0P_                   1
     $_SDFFE_PP1P_                   3
     $_SDFF_PN0_                   133
     $_SDFF_PP0_                    18
     $_XNOR_                       599
     $_XOR_                       2342
```

CONFIG files:

1. Clock period = 25 ns

```
export PLATFORM          = sky130hd

export DESIGN_NAME       = picorv32a

export VERILOG_FILES     = $(sort $(wildcard ./designs/src/$(DESIGN_NICKNAME)/*.v))
export SDC_FILE          = ./designs/$(PLATFORM)/$(DESIGN_NICKNAME)/constraint.sdc

export CORE_UTILIZATION = 40
export PLACE_DENSITY     = 0.60

export TNS_END_PERCENT   = 100
```

2.Clock period = 18 ns

```
export PLATFORM          = sky130hd

export DESIGN_NAME       = picorv32a

export VERILOG_FILES     = $(sort $(wildcard ./designs/src/$(DESIGN_NICKNAME)/*.v))
export SDC_FILE          = ./designs/$(PLATFORM)/$(DESIGN_NICKNAME)/constraint.sdc

export CORE_UTILIZATION = 40
export PLACE_DENSITY     = 0.60

export TNS_END_PERCENT   = 100
```

3. Clock period = 12 ns

```
export PLATFORM          = sky130hd

export DESIGN_NAME       = picorv32a

export VERILOG_FILES     = $(sort $(wildcard ./designs/src/$(DESIGN_NICKNAME)/*.v))
export SDC_FILE          = ./designs/$(PLATFORM)/$(DESIGN_NICKNAME)/constraint.sdc

export CORE_UTILIZATION = 50
export PLACE_DENSITY     = 0.65

export TNS_END_PERCENT   = 100
```

4. Clock period = 12 ns

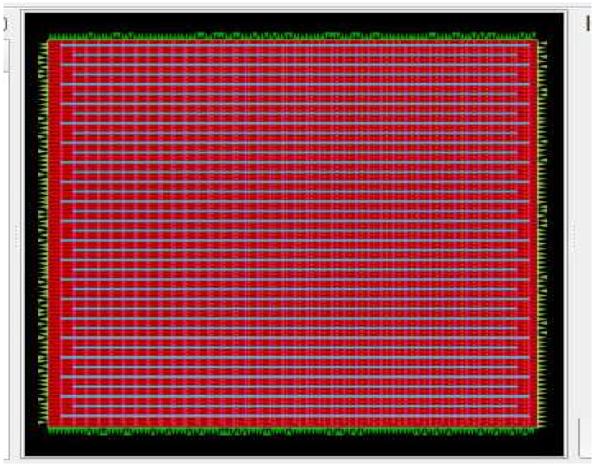
```
export PLATFORM          = sky130hd

export DESIGN_NAME       = picorv32a

export VERILOG_FILES     = $(sort $(wildcard ./designs/src/$(DESIGN_NICKNAME)/*.v))
export SDC_FILE          = ./designs/$(PLATFORM)/$(DESIGN_NICKNAME)/constraint.sdc

export CORE_UTILIZATION = 43
export PLACE_DENSITY     = 0.58

export TNS_END_PERCENT   = 100
~
```

5. Clock period = 10 ns

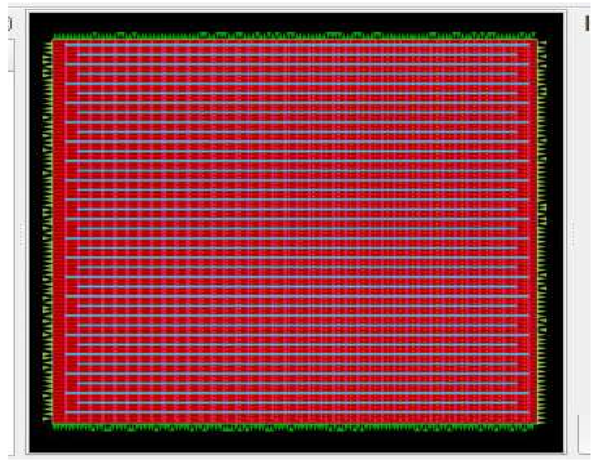
```
export PLATFORM          = sky130hd

export DESIGN_NAME       = picorv32a

export VERILOG_FILES     = $(sort $(wildcard ./designs/src/$(DESIGN_NICKNAME)/*.v))
export SDC_FILE          = ./designs/$(PLATFORM)/$(DESIGN_NICKNAME)/constraint.sdc

export CORE_UTILIZATION = 35
export PLACE_DENSITY     = 0.42
export CELL_PAD_IN_MICRON = 0.4
export SYNTH_BUFFERING = 1
export TNS_END_PERCENT   = 100
```

Floorplan:

1.



2.



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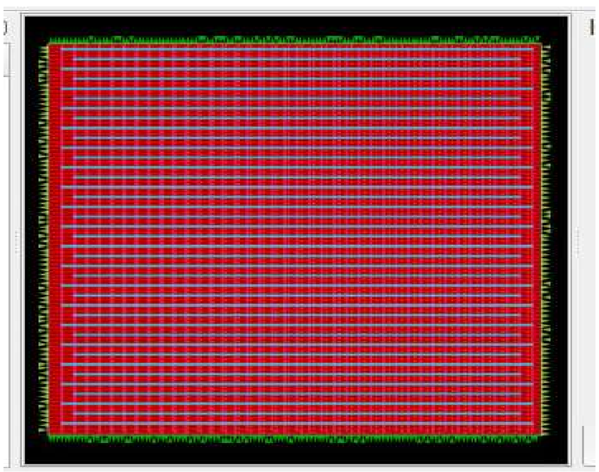

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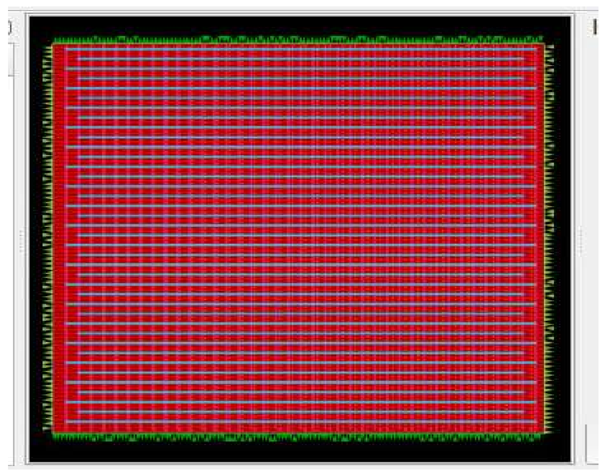

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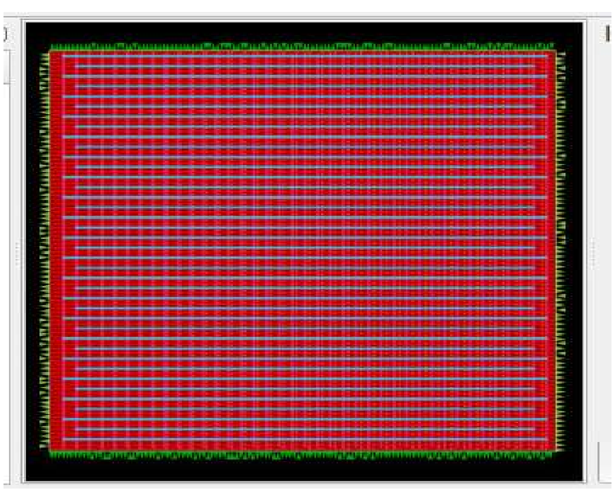
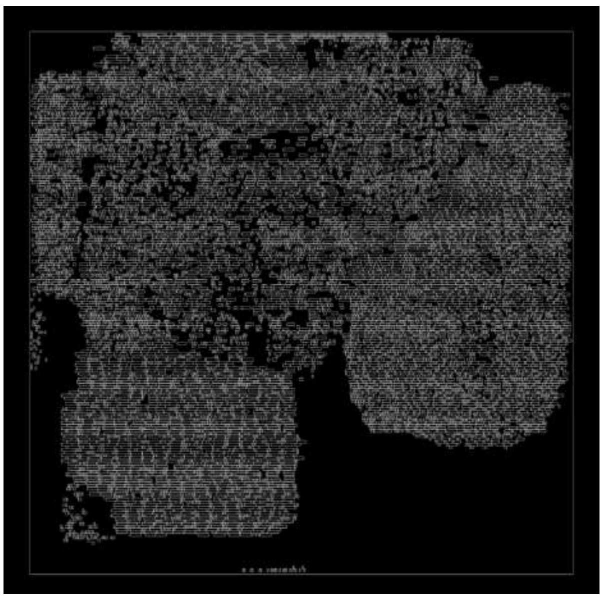


Placement:

1.



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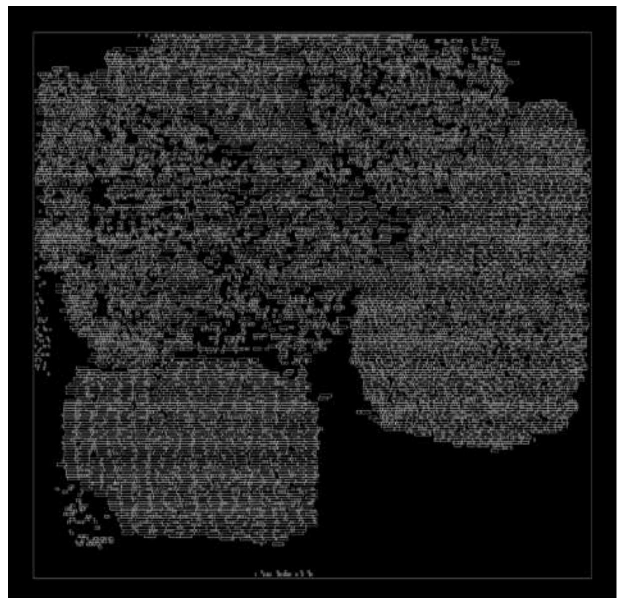

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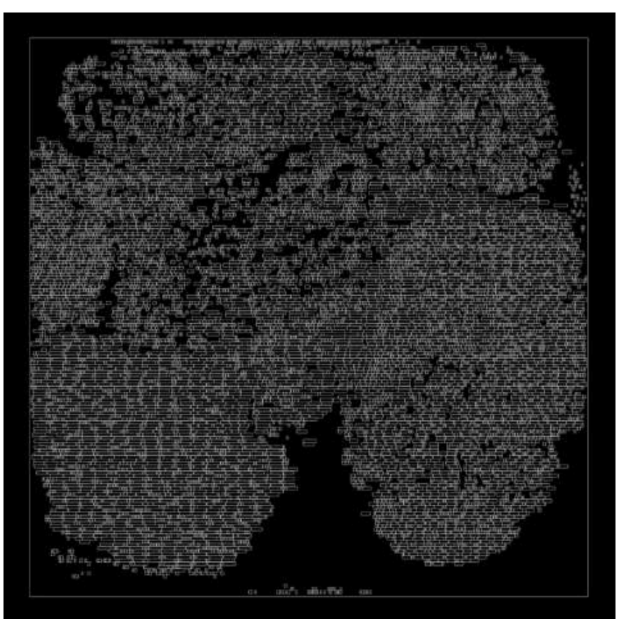

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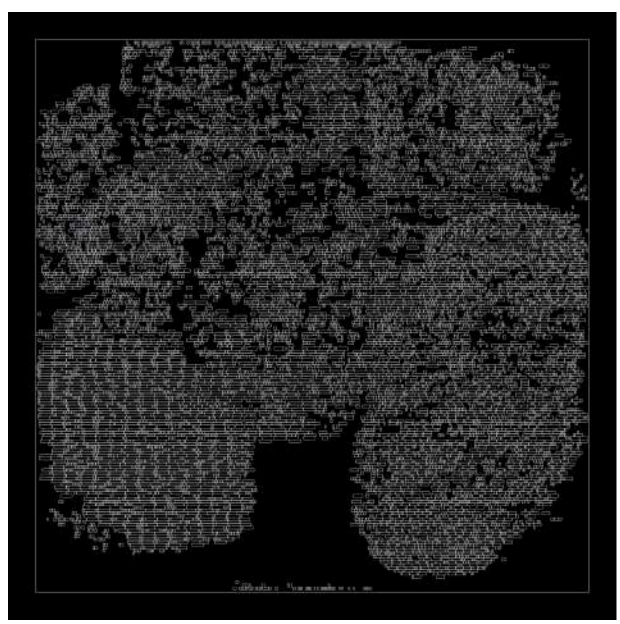

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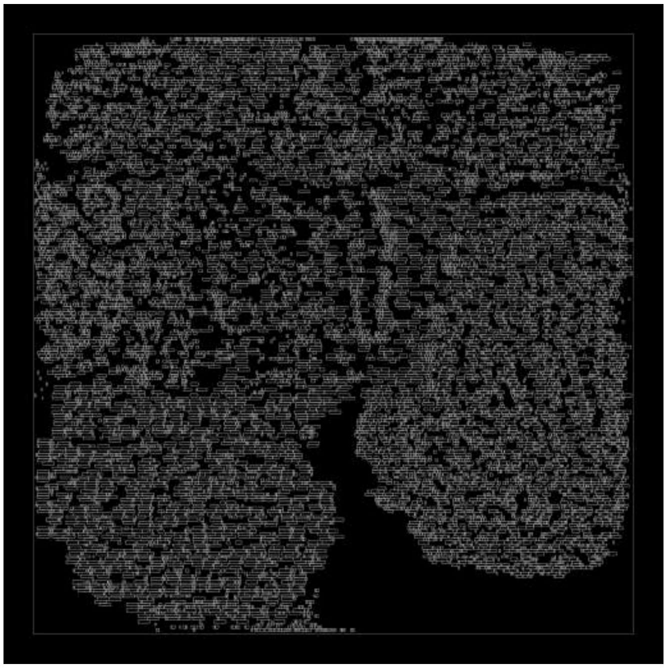
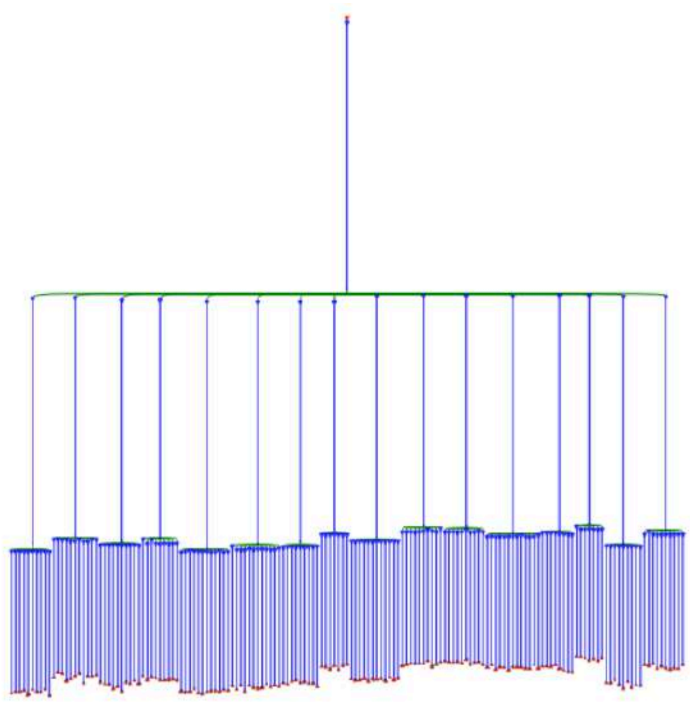
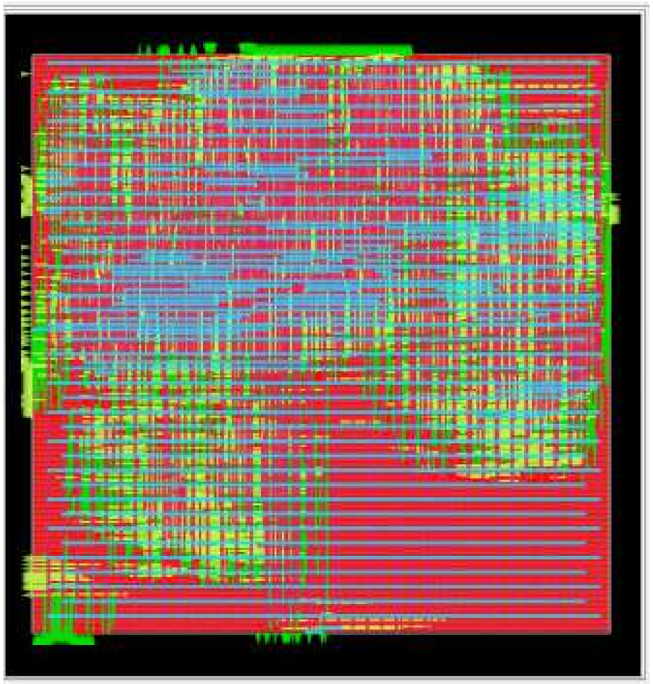


CLOCK TREE:



ROUTING:

1.



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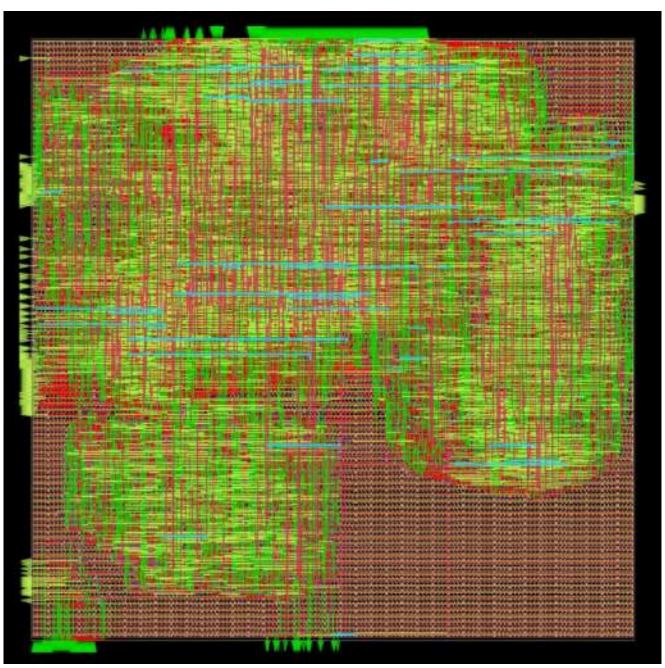

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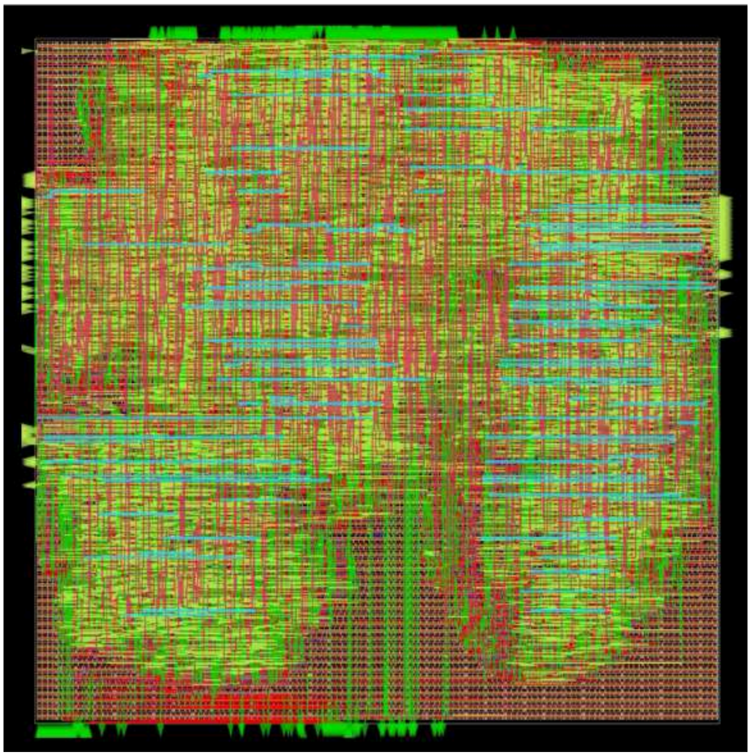

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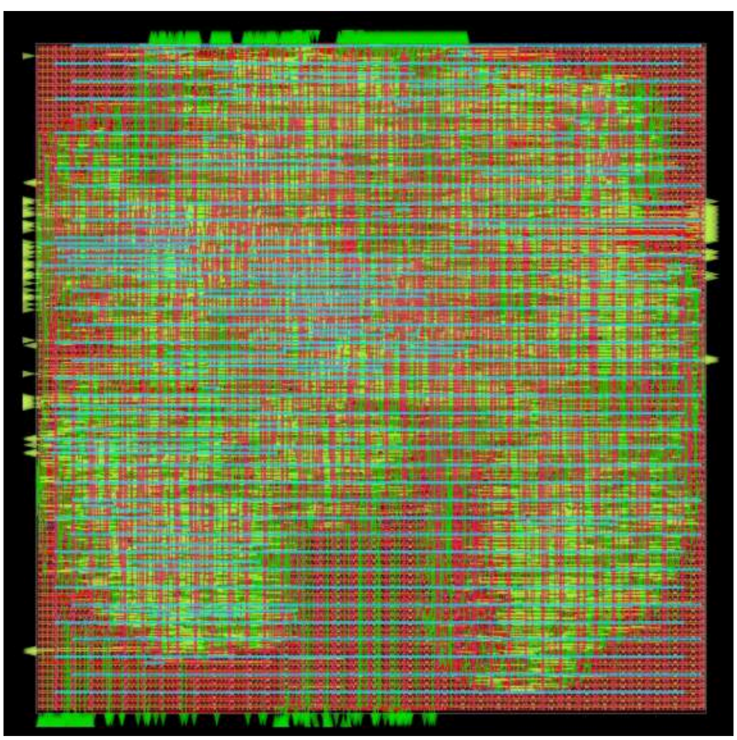

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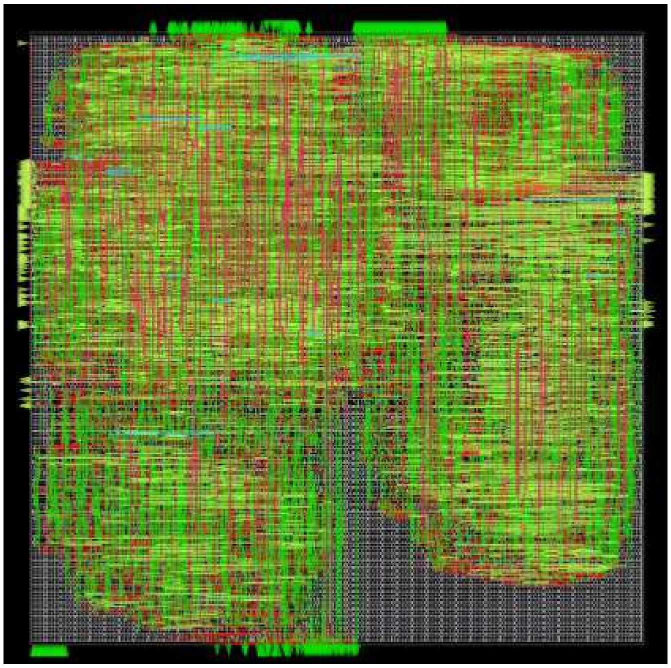
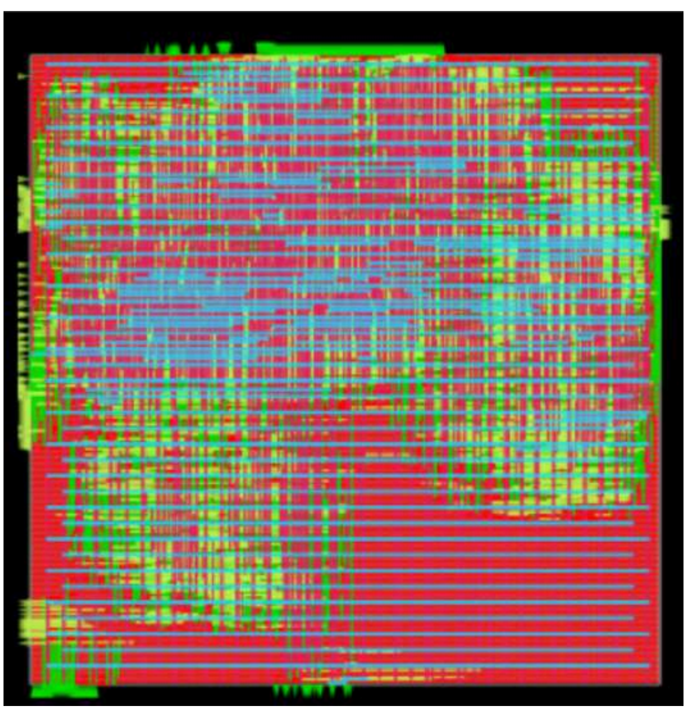


Final:

1.



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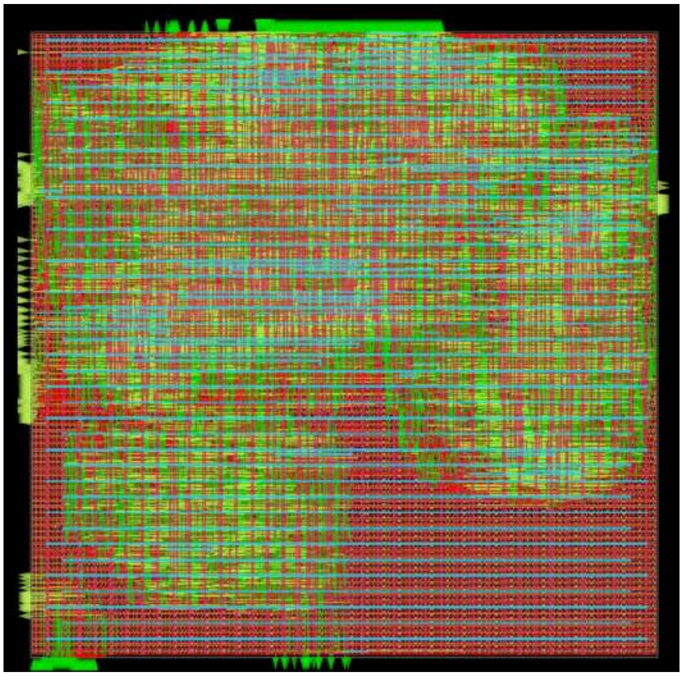
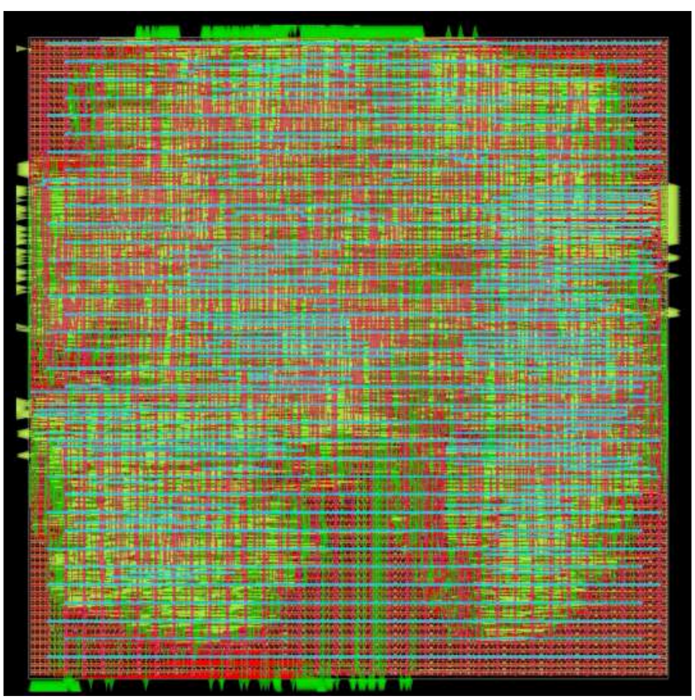
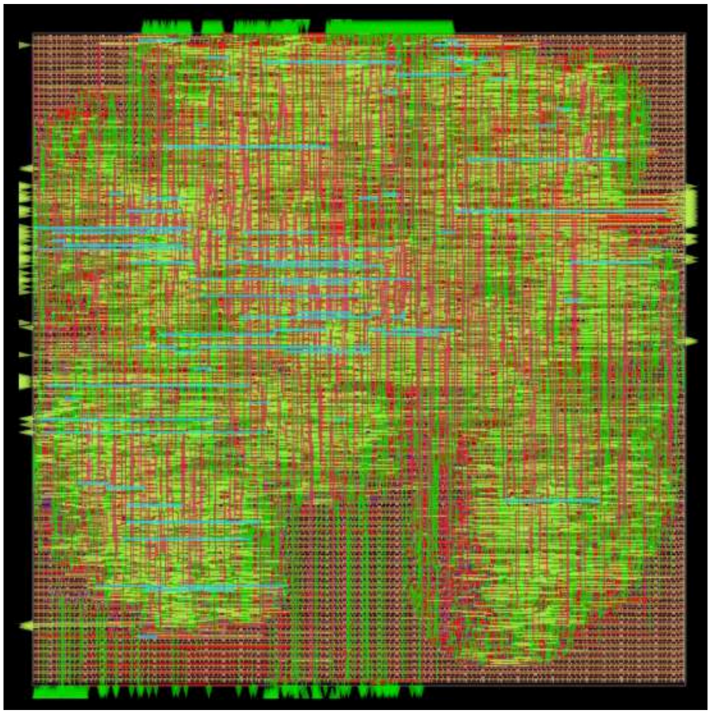


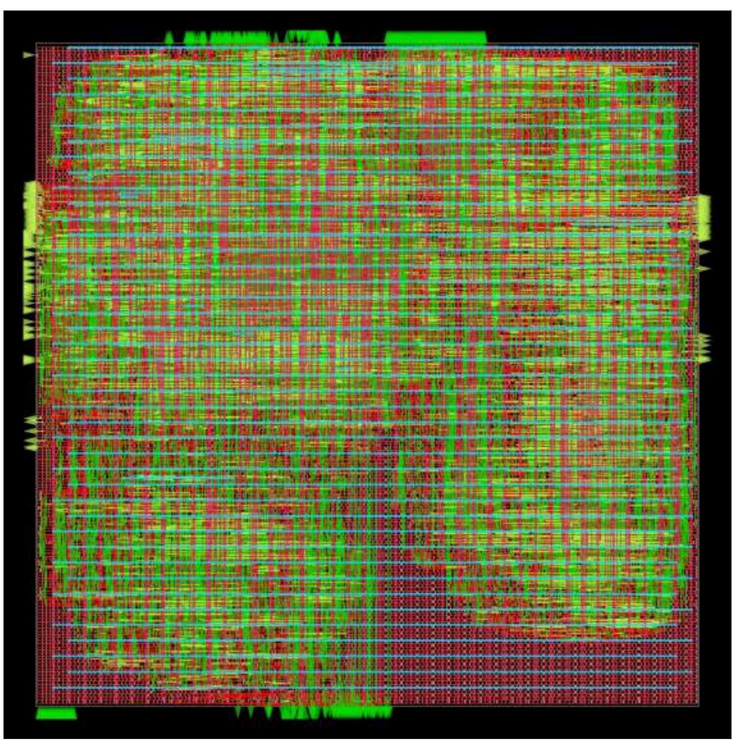
3.



4.



5.



TIMING REPORT:

1.

```
==========================================================================
finish report_tns
--------------------------------------------------------------------------
tns 0.00

==========================================================================
finish report_wns
--------------------------------------------------------------------------
wns 0.00

==========================================================================
finish report_worst_slack
--------------------------------------------------------------------------
worst slack 13.92

==========================================================================
finish report_clock_skew
--------------------------------------------------------------------------
Clock core_clock
   0.84 source latency irq_mask[26]$_SDFFE_PN1P_/CLK ^
  -0.93 target latency count_instr[5]$_SDFFE_PN0P_/CLK ^
   0.00 CRPR
--------------
  -0.10 setup skew


==========================================================================
finish report_checks -path_delay min
```

2.

```
==========================================================================
finish report_tns
--------------------------------------------------------------------------
tns 0.00

==========================================================================
finish report_wns
--------------------------------------------------------------------------
wns 0.00

==========================================================================
finish report_worst_slack
--------------------------------------------------------------------------
worst slack 9.16

==========================================================================
finish report_clock_skew
--------------------------------------------------------------------------
Clock core_clock
   0.86 source latency cpuregs[16][14]$_DFFE_PP_/CLK ^
  -0.94 target latency reg_out[14]$_DFF_P_/CLK ^
   0.00 CRPR
--------------
  -0.08 setup skew
```

3.

```
===========================================================================
finish report_tns
---------------------------------------------------------------------------
tns 0.00

===========================================================================
finish report_wns
---------------------------------------------------------------------------
wns 0.00

===========================================================================
finish report_worst_slack
---------------------------------------------------------------------------
worst slack 2.91

===========================================================================
finish report_clock_skew
---------------------------------------------------------------------------
Clock core_clock
   0.88 source latency latched_stalu$_SDFFE_PN0P_/CLK ^
  -0.97 target latency cpuregs[4][12]$_DFFE_PP_/CLK ^
   0.00 CRPR
--------------
  -0.10 setup skew
```

4.

```
=====================================================
finish report_tns
-----------------------------------------------------
tns 0.00

=====================================================
finish report_wns
-----------------------------------------------------
wns 0.00

=====================================================
finish report_worst_slack
-----------------------------------------------------
worst slack 3.39

=====================================================
finish report_clock_skew
-----------------------------------------------------
Clock core_clock
   0.98 source latency cpuregs[15][1]$_DFFE_PP_/CLK ^
  -0.87 target latency reg_op2[1]$_DFFE_PP_/CLK ^
   0.00 CRPR
--------------
   0.11 setup skew
```

5.

```
==========================================================
finish report_tns
----------------------------------------------------------
tns 0.00

==========================================================
finish report_wns
----------------------------------------------------------
wns 0.00

==========================================================
finish report_worst_slack
----------------------------------------------------------
worst slack 1.16

==========================================================
finish report_clock_skew
----------------------------------------------------------
Clock core_clock
   0.95 source latency cpuregs[12][5]$_DFFE_PP_/CLK ^
  -0.82 target latency reg_op2[5]$_DFFE_PP_/CLK ^
   0.00 CRPR
--------------
   0.13 setup skew
```

POWER AND AREA REPORT:

1.

```
>>> report_power
Group                  Internal  Switching    Leakage      Total
                          Power      Power      Power      Power (Watts)
----------------------------------------------------------------
Sequential             2.97e-03   2.35e-04   1.43e-08   3.21e-03  44.2%
Combinational          4.27e-04   8.75e-04   3.70e-08   1.30e-03  18.0%
Clock                  1.57e-03   1.18e-03   2.93e-09   2.74e-03  37.8%
Macro                  0.00e+00   0.00e+00   0.00e+00   0.00e+00   0.0%
Pad                    0.00e+00   0.00e+00   0.00e+00   0.00e+00   0.0%
----------------------------------------------------------------
Total                  4.96e-03   2.29e-03   5.42e-08   7.25e-03 100.0%
                          68.5%      31.5%       0.0%
>>> report_design_area
Design area 138574 u^2 48% utilization.
```

2.

```
>>> report_power
Group                  Internal  Switching    Leakage      Total
                          Power      Power      Power      Power (Watts)
----------------------------------------------------------------
Sequential             4.12e-03   2.86e-04   1.43e-08   4.41e-03  44.1%
Combinational          5.79e-04   1.18e-03   3.76e-08   1.76e-03  17.6%
Clock                  2.18e-03   1.66e-03   2.90e-09   3.83e-03  38.3%
Macro                  0.00e+00   0.00e+00   0.00e+00   0.00e+00   0.0%
Pad                    0.00e+00   0.00e+00   0.00e+00   0.00e+00   0.0%
----------------------------------------------------------------
Total                  6.88e-03   3.12e-03   5.48e-08   1.00e-02 100.0%
                          68.8%      31.2%       0.0%
>>> report_design_area
Design area 138852 u^2 48% utilization.
```

3.

```
>>> report_power
Group                  Internal  Switching    Leakage      Total
                          Power      Power      Power      Power (Watts)
----------------------------------------------------------------
Sequential             6.19e-03   4.07e-04   1.43e-08   6.59e-03  43.5%
Combinational          8.96e-04   1.87e-03   3.75e-08   2.76e-03  18.2%
Clock                  3.28e-03   2.51e-03   2.93e-09   5.79e-03  38.2%
Macro                  0.00e+00   0.00e+00   0.00e+00   0.00e+00   0.0%
Pad                    0.00e+00   0.00e+00   0.00e+00   0.00e+00   0.0%
----------------------------------------------------------------
Total                  1.04e-02   4.78e-03   5.47e-08   1.51e-02 100.0%
                          68.4%      31.6%       0.0%
>>> report_design_area
Design area 138662 u^2 60% utilization.
```

4.

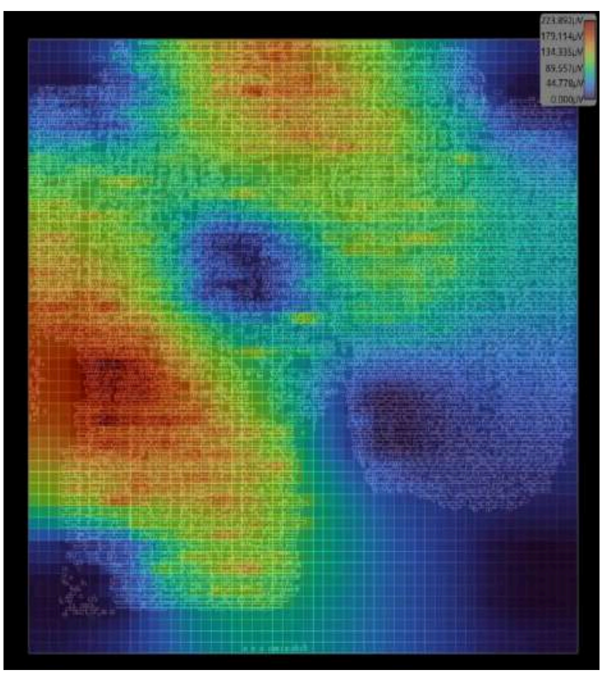
```
>>> report_power
Group                  Internal  Switching    Leakage      Total
                          Power      Power      Power      Power (Watts)
----------------------------------------------------------------
Sequential             6.19e-03   4.53e-04   1.43e-08   6.64e-03  43.7%
Combinational          9.02e-04   1.91e-03   3.76e-08   2.81e-03  18.5%
Clock                  3.17e-03   2.57e-03   2.91e-09   5.75e-03  37.8%
Macro                  0.00e+00   0.00e+00   0.00e+00   0.00e+00   0.0%
Pad                    0.00e+00   0.00e+00   0.00e+00   0.00e+00   0.0%
----------------------------------------------------------------
Total                  1.03e-02   4.93e-03   5.48e-08   1.52e-02 100.0%
                          67.5%      32.5%       0.0%
>>> report_design_area
Design area 139199 u^2 52% utilization.
```

5.

```
>>> report_power
Group                  Internal  Switching    Leakage      Total
                          Power      Power      Power      Power (Watts)
----------------------------------------------------------------
Sequential             7.43e-03   4.90e-04   1.43e-08   7.92e-03  42.2%
Combinational          1.08e-03   2.15e-03   3.76e-08   3.23e-03  17.2%
Clock                  4.45e-03   3.17e-03   3.31e-09   7.62e-03  40.6%
Macro                  0.00e+00   0.00e+00   0.00e+00   0.00e+00   0.0%
Pad                    0.00e+00   0.00e+00   0.00e+00   0.00e+00   0.0%
----------------------------------------------------------------
Total                  1.30e-02   5.81e-03   5.52e-08   1.88e-02 100.0%
                          69.1%      30.9%       0.0%
>>> report_design_area
Design area 140697 u^2 43% utilization.
```

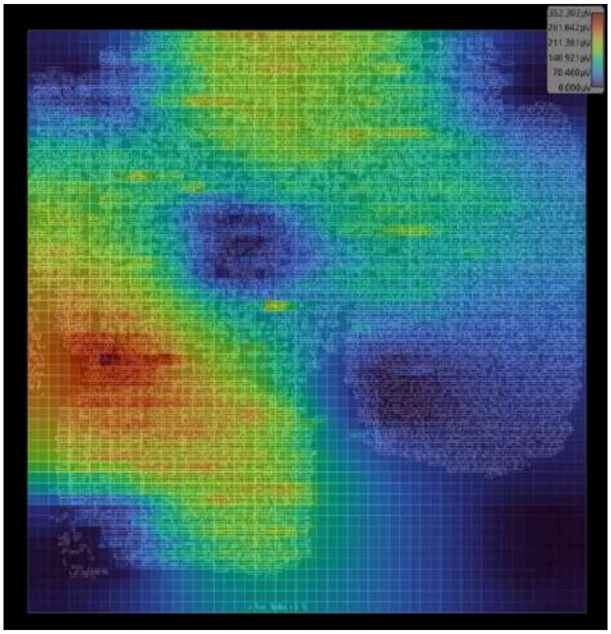
IR DROP:

1.



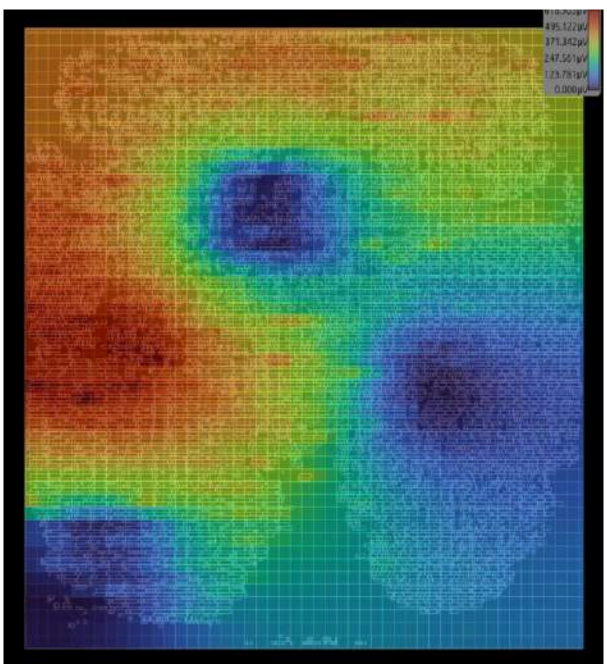
```
x.
########## IR report #################
Net                 : VDD
Corner              : default
Supply voltage      : 1.80e+00 V
Worstcase voltage: 1.80e+00 V
Average voltage     : 1.80e+00 V
Average IR drop     : 7.93e-05 V
Worstcase IR drop: 2.54e-04 V
Percentage drop     : 0.01 %
######################################
[INFO PSM-0040] All shapes on net VSS are c
[INFO PSM-0073] Using bump pattern with x-p
x.
########## IR report #################
Net                 : VSS
Corner              : default
Supply voltage      : 0.00e+00 V
Worstcase voltage: 2.24e-04 V
Average voltage     : 7.21e-05 V
Average IR drop     : 7.21e-05 V
Worstcase IR drop: 2.24e-04 V
Percentage drop     : 0.01 %
######################################
```

2.



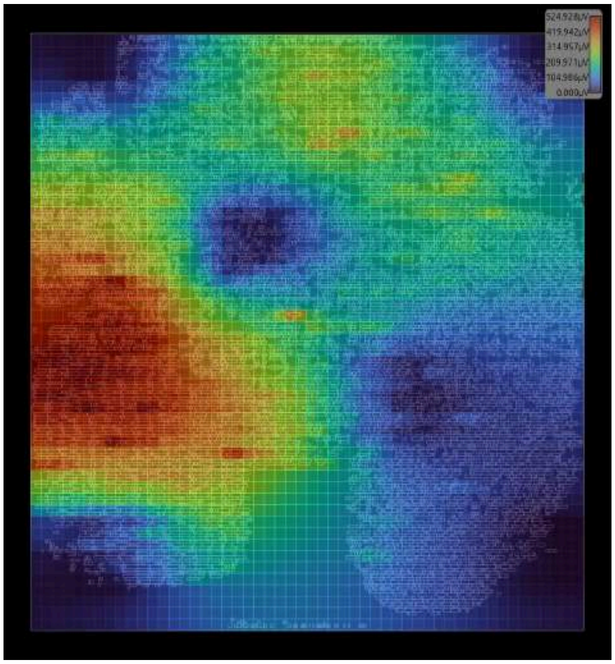
```
x.
########## IR report #################
Net              : VDD
Corner           : default
Supply voltage   : 1.80e+00 V
Worstcase voltage: 1.80e+00 V
Average voltage  : 1.80e+00 V
Average IR drop  : 1.09e-04 V
Worstcase IR drop: 3.90e-04 V
Percentage drop  : 0.02 %
######################################
[INFO PSM-0040] All shapes on net VSS are c
[INFO PSM-0073] Using bump pattern with x-p
x.
########## IR report #################
Net              : VSS
Corner           : default
Supply voltage   : 0.00e+00 V
Worstcase voltage: 3.52e-04 V
Average voltage  : 9.85e-05 V
Average IR drop  : 9.85e-05 V
Worstcase IR drop: 3.52e-04 V
Percentage drop  : 0.02 %
```

3.



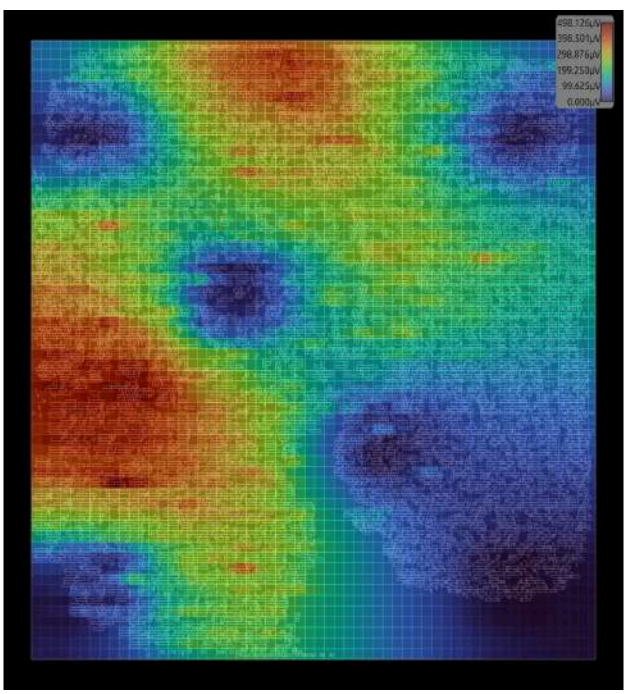
```
########## IR report #################
Net              : VDD
Corner           : default
Supply voltage   : 1.80e+00 V
Worstcase voltage: 1.80e+00 V
Average voltage  : 1.80e+00 V
Average IR drop  : 2.88e-04 V
Worstcase IR drop: 7.58e-04 V
Percentage drop  : 0.04 %
######################################
[INFO PSM-0040] All shapes on net VSS are connected.
[INFO PSM-0073] Using bump pattern with x-pitch 140.0
x.
########## IR report #################
Net              : VSS
Corner           : default
Supply voltage   : 0.00e+00 V
Worstcase voltage: 6.19e-04 V
Average voltage  : 2.56e-04 V
Average IR drop  : 2.56e-04 V
Worstcase IR drop: 6.19e-04 V
Percentage drop  : 0.03 %
######################################
```

4.



```
########## IR report #################
Net              : VDD
Corner           : default
Supply voltage   : 1.80e+00 V
Worstcase voltage: 1.80e+00 V
Average voltage  : 1.80e+00 V
Average IR drop  : 1.78e-04 V
Worstcase IR drop: 6.73e-04 V
Percentage drop  : 0.04 %
######################################
[INFO PSM-0040] All shapes on net VSS are connected.
[INFO PSM-0073] Using bump pattern with x-pitch 140.0
x.
########## IR report #################
Net              : VSS
Corner           : default
Supply voltage   : 0.00e+00 V
Worstcase voltage: 5.25e-04 V
Average voltage  : 1.61e-04 V
Average IR drop  : 1.61e-04 V
Worstcase IR drop: 5.25e-04 V
Percentage drop  : 0.03 %
######################################
```

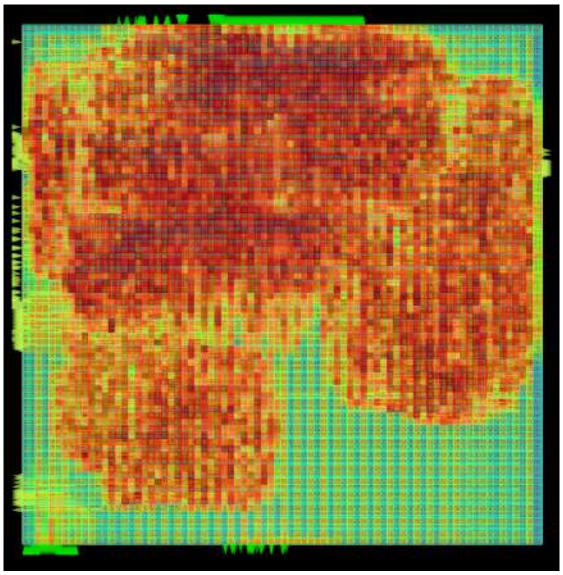
5.



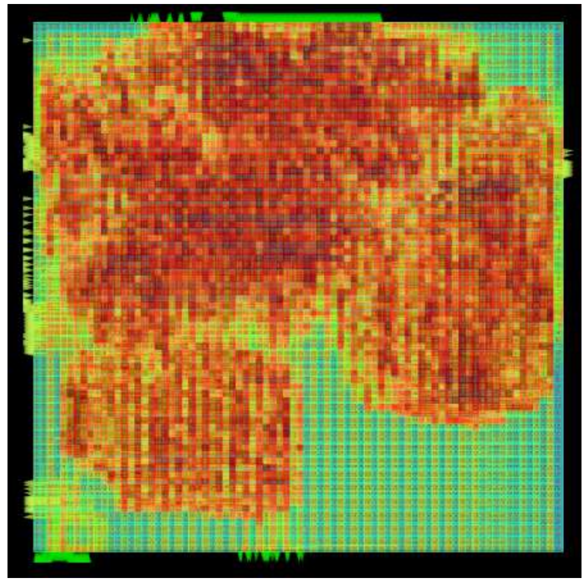
```
x.
########## IR report #################
Net              : VDD
Corner           : default
Supply voltage   : 1.80e+00 V
Worstcase voltage: 1.80e+00 V
Average voltage  : 1.80e+00 V
Average IR drop  : 1.79e-04 V
Worstcase IR drop: 5.92e-04 V
Percentage drop  : 0.03 %
######################################
[INFO PSM-0040] All shapes on net VSS are c
[INFO PSM-0073] Using bump pattern with x-p
x.
########## IR report #################
Net              : VSS
Corner           : default
Supply voltage   : 0.00e+00 V
Worstcase voltage: 4.98e-04 V
Average voltage  : 1.71e-04 V
Average IR drop  : 1.71e-04 V
Worstcase IR drop: 4.98e-04 V
Percentage drop  : 0.03 %
######################################
Cell type report:                    Co
```

ROUTING CONGESTION MAPS:

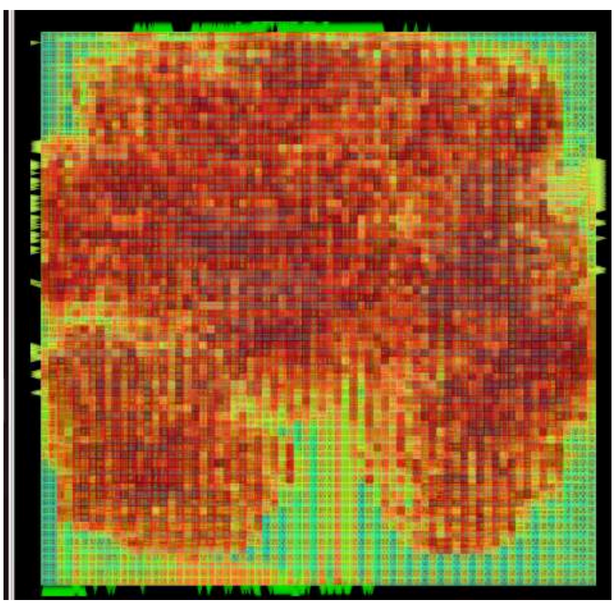
1.



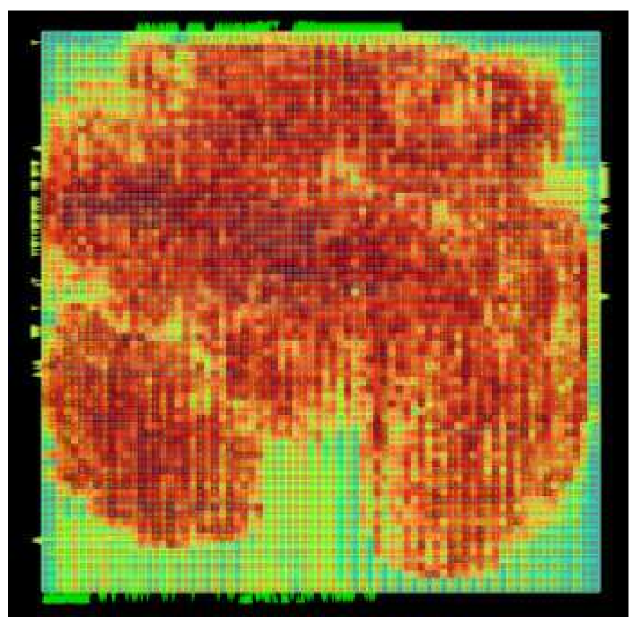
2.



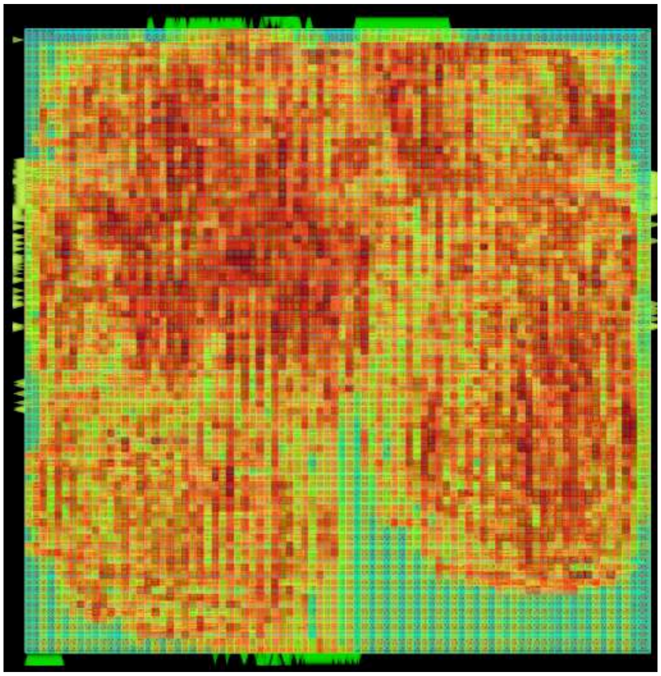
3.



4.



5.



CONGESTION REPORTS:

1.

```
[INFO GRT-0096] Final congestion report:
Layer         Resource        Demand        Usage (%)    Max H / Max V / Total Overflow
---------------------------------------------------------------------------------------
li1                  0             0            0.00%            0 /  0 /  0
met1             54620         25227           46.19%            0 /  0 /  0
met2             59675         32101           53.79%            0 /  0 /  0
met3             44185         13987           31.66%            0 /  0 /  0
met4             21329          8116           38.05%            0 /  0 /  0
met5              6006           755           12.57%            0 /  0 /  0
---------------------------------------------------------------------------------------
Total           185815         80186           43.15%            0 /  0 /  0

[INFO GRT-0018] Total wirelength: 785889 um
[INFO GRT-0014] Routed nets: 14059
```

2.

```
[INFO GRT-0096] Final congestion report:
Layer         Resource        Demand        Usage (%)    Max H / Max V / Total Overflow
---------------------------------------------------------------------------------------
li1                  0             0            0.00%            0 /  0 /  0
met1             54318         25344           46.66%            0 /  0 /  0
met2             59675         31426           52.66%            0 /  0 /  0
met3             44185         13004           29.43%            0 /  0 /  0
met4             21329          7197           33.74%            0 /  0 /  0
met5              6006           489            8.14%            0 /  0 /  0
---------------------------------------------------------------------------------------
Total           185513         77460           41.75%            0 /  0 /  0

[INFO GRT-0018] Total wirelength: 764595 um
[INFO GRT-0014] Routed nets: 14052
```

3.

```
[INFO GRT-0096] Final congestion report:
Layer         Resource        Demand        Usage (%)    Max H / Max V / Total Overflow
---------------------------------------------------------------------------------------
li1                  0             0            0.00%            0 /  0 /  0
met1             40809         23053           56.49%            0 /  0 /  0
met2             47955         30543           63.69%            0 /  0 /  0
met3             35420         15291           43.17%            0 /  0 /  0
met4             17043          8247           48.39%            0 /  0 /  0
met5              4830          1104           22.86%            0 /  0 /  0
---------------------------------------------------------------------------------------
Total           146057         78238           53.57%            0 /  0 /  0

[INFO GRT-0018] Total wirelength: 781080 um
[INFO GRT-0014] Routed nets: 14046
```

4.

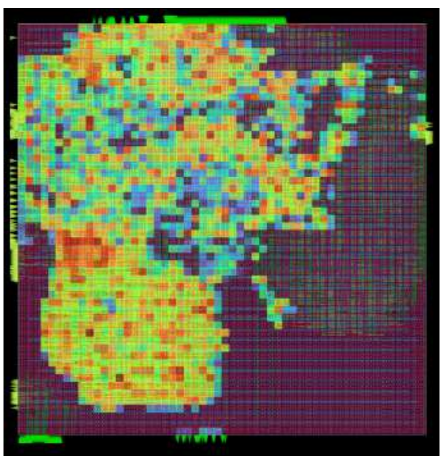
```
[INFO GRT-0096] Final congestion report:
Layer         Resource        Demand        Usage (%)    Max H / Max V / Total Overflow
---------------------------------------------------------------------------------------
li1                  0             0            0.00%            0 /  0 /  0
met1             49557         25449           51.35%            0 /  0 /  0
met2             55426         33933           61.22%            0 /  0 /  0
met3             41015         14700           35.84%            0 /  0 /  0
met4             19832          8489           42.80%            0 /  0 /  0
met5              5624           605           10.76%            0 /  0 /  0
---------------------------------------------------------------------------------------
Total           171454         83176           48.51%            0 /  0 /  0

[INFO GRT-0018] Total wirelength: 815524 um
[INFO GRT-0014] Routed nets: 14054
Perform buffer insertion and gate resizing...
repair_design
[INFO RSZ-0058] Using max wire length 2154um.
```

5.

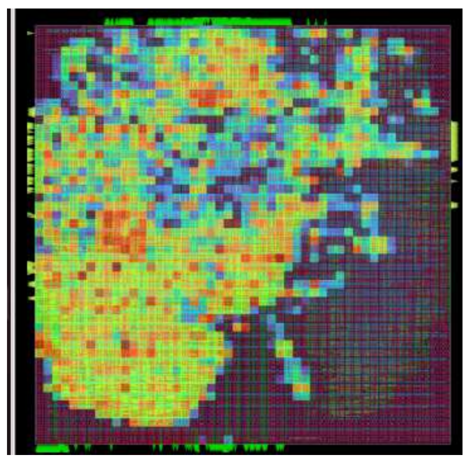
```
[INFO GRT-0096] Final congestion report:
Layer         Resource        Demand        Usage (%)    Max H / Max V / Total Overflow
---------------------------------------------------------------------------------------
li1                  0             0            0.00%            0 /  0 /  0
met1             63701         31418           49.32%            0 /  0 /  0
met2             67896         35341           52.05%            0 /  0 /  0
met3             50348         10976           21.80%            0 /  0 /  0
met4             24354          6316           25.93%            0 /  0 /  0
met5              6888            68            0.99%            0 /  0 /  0
---------------------------------------------------------------------------------------
Total           213187         84119           39.46%            0 /  0 /  0

[INFO GRT-0018] Total wirelength: 812909 um
[INFO GRT-0014] Routed nets: 14077
Perform buffer insertion and gate resizing...
repair_design
[INFO RSZ-0058] Using max wire length 2154um.
```

POWER DENSITY:

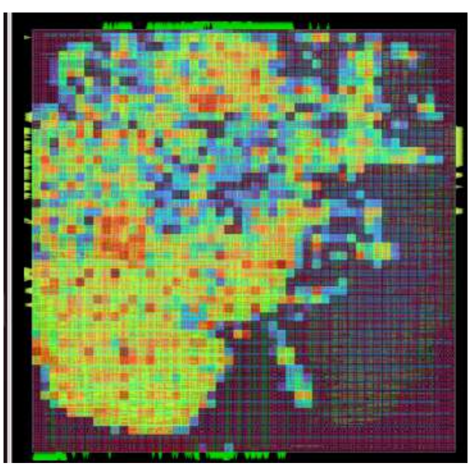
1.



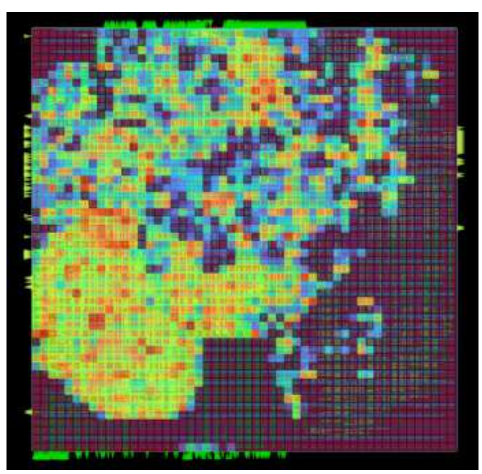
2.



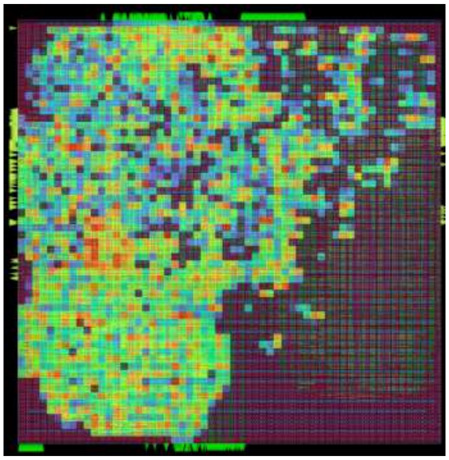
3.



4.

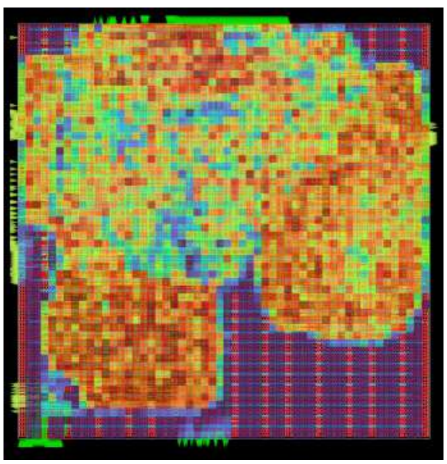


5.

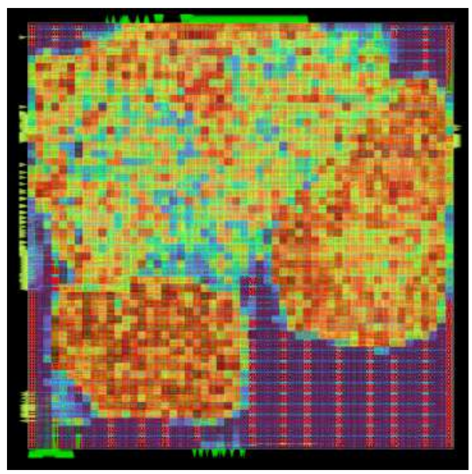


PLACEMENT DENSITY:

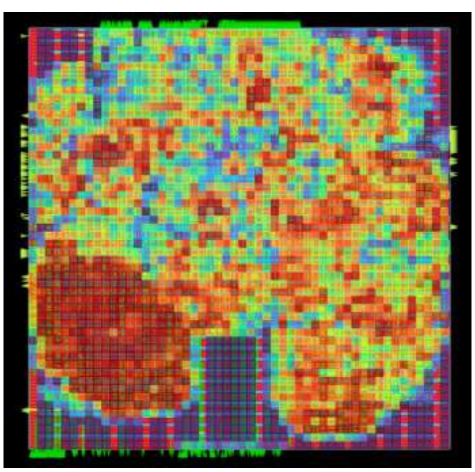
1.



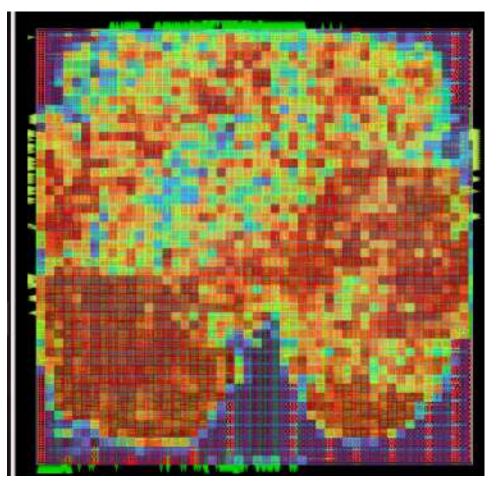
2.



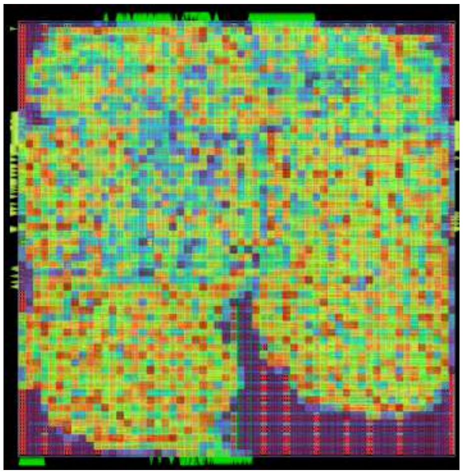
3.



4.

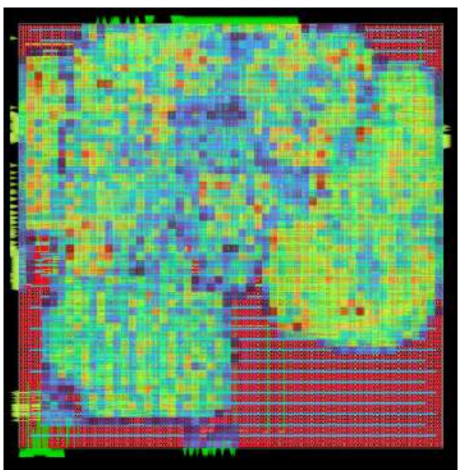


5.

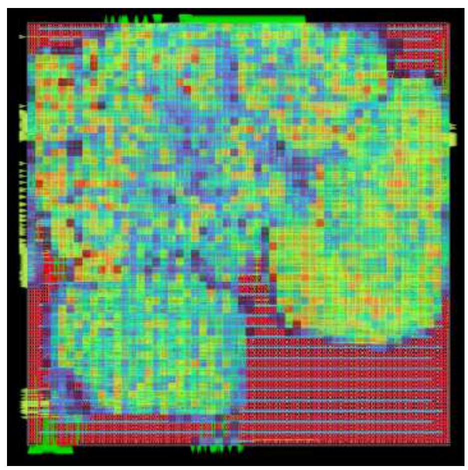


PIN DENSITY:

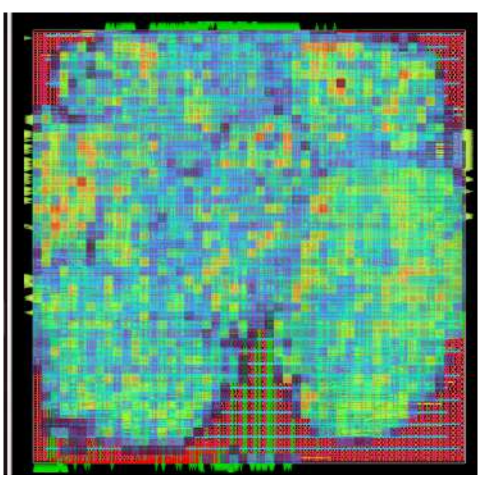
1.



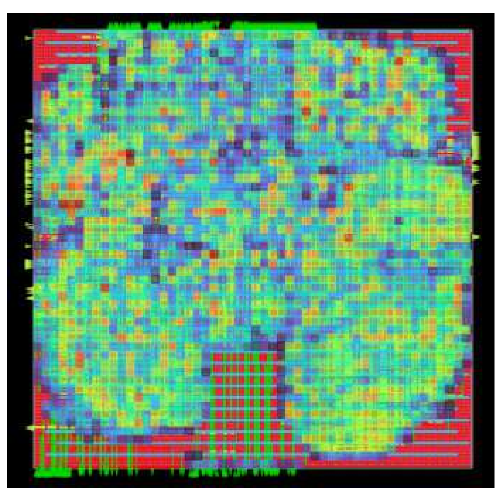
2.



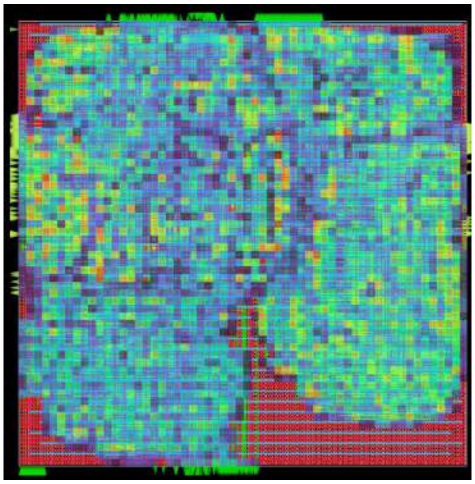
3.



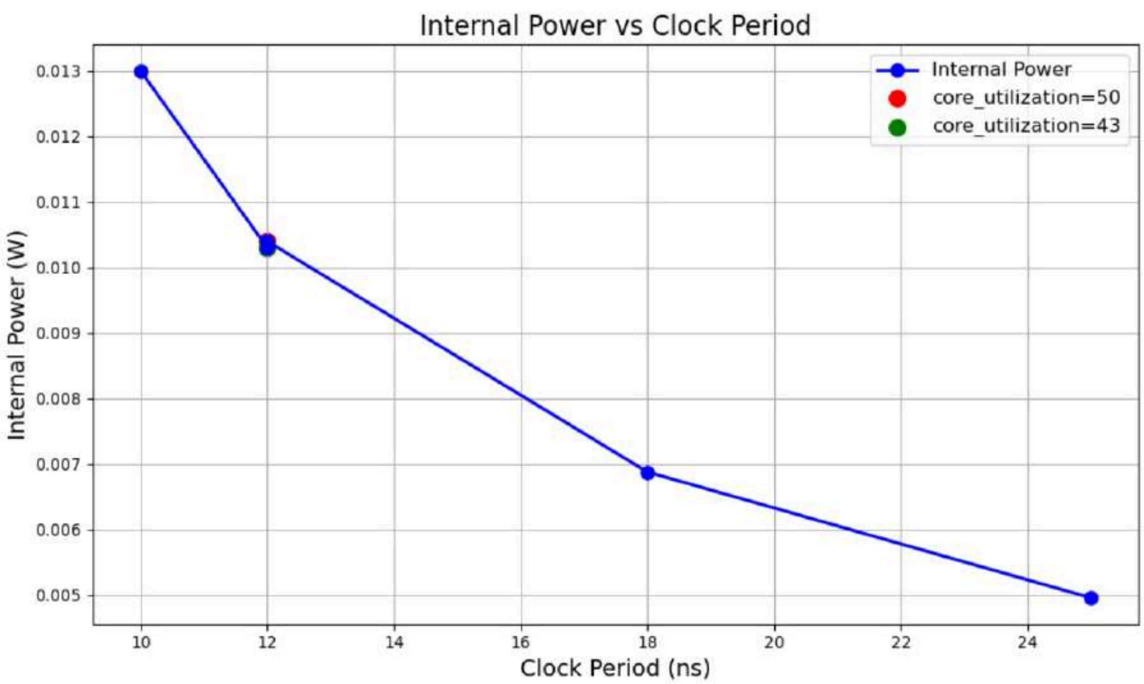
4.

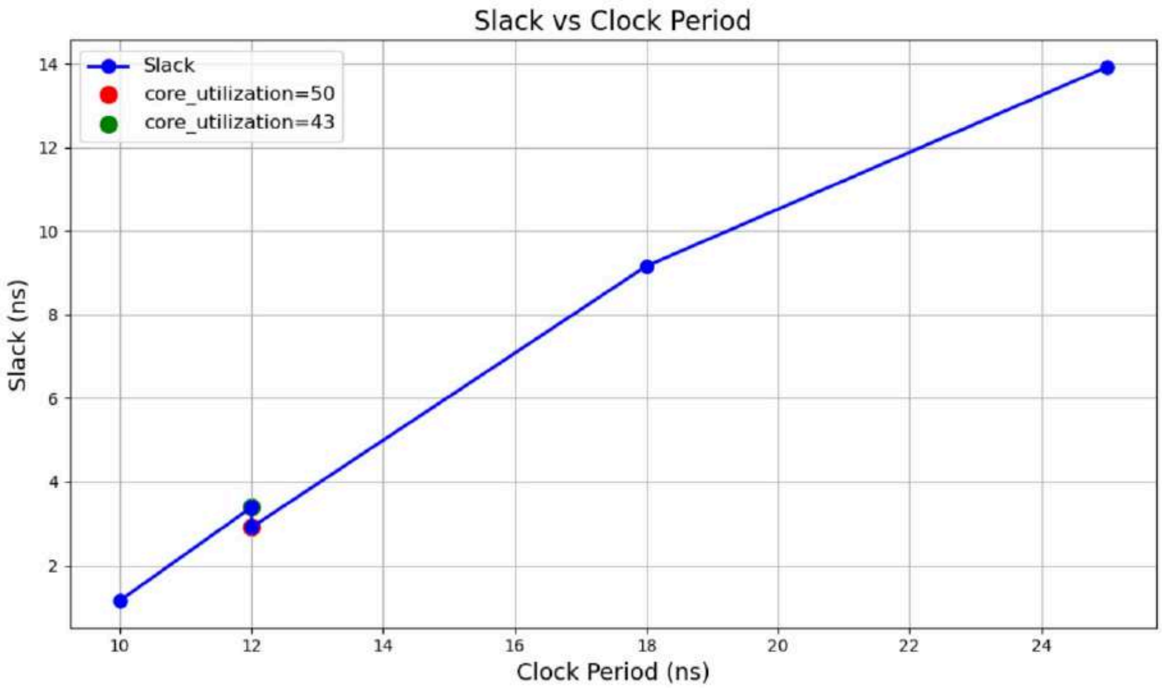


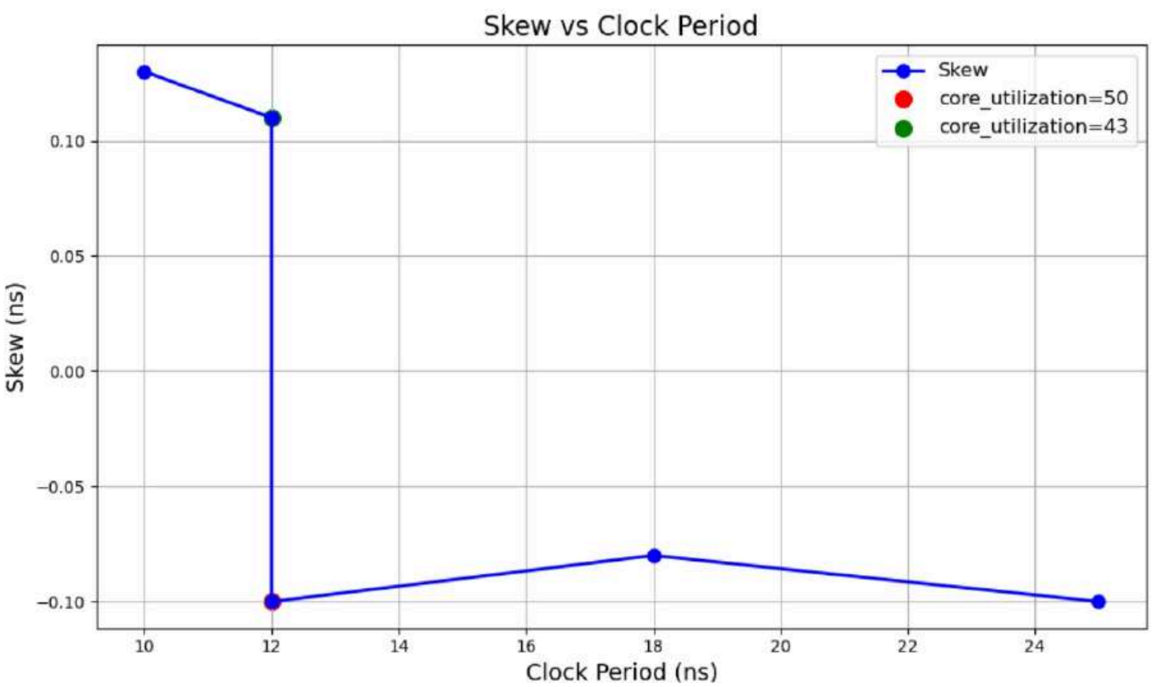
5.

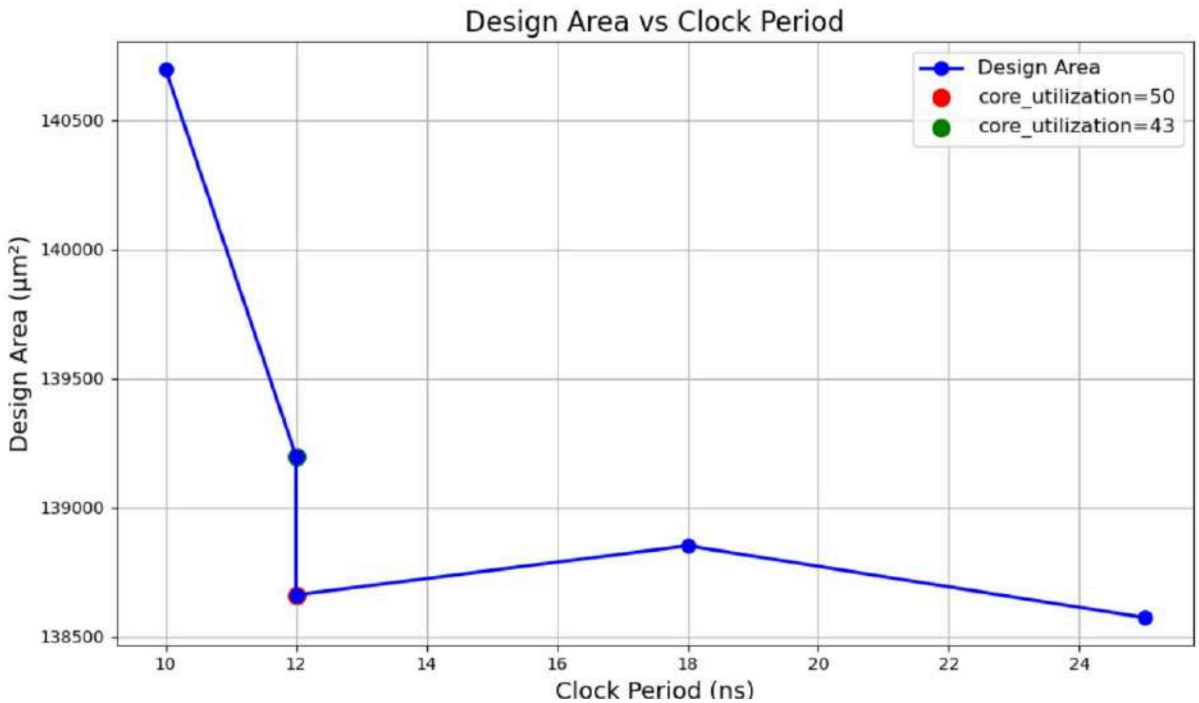


Comparison Graphs




Slack vs Clock Period
Slack
core_utilization=50
core_utilization=43
Slack (ns)
Clock Period (ns)
14
12
10
8
6
4
2
10
12
14
16
18
20
22
24


Skew vs Clock Period
Skew
core_utilization=50
core_utilization=43
Skew (ns)
Clock Period (ns)
0.10
0.05
0.00
−0.05
−0.10
10
12
14
16
18
20
22
24



Optimal clock period chosen is 12 ns. This is chosen because of Positive Skew and small Positive Slack.
According to Internal Power and Design Area ,clock period with 25 ns is best, but it does not meet timing requirements.