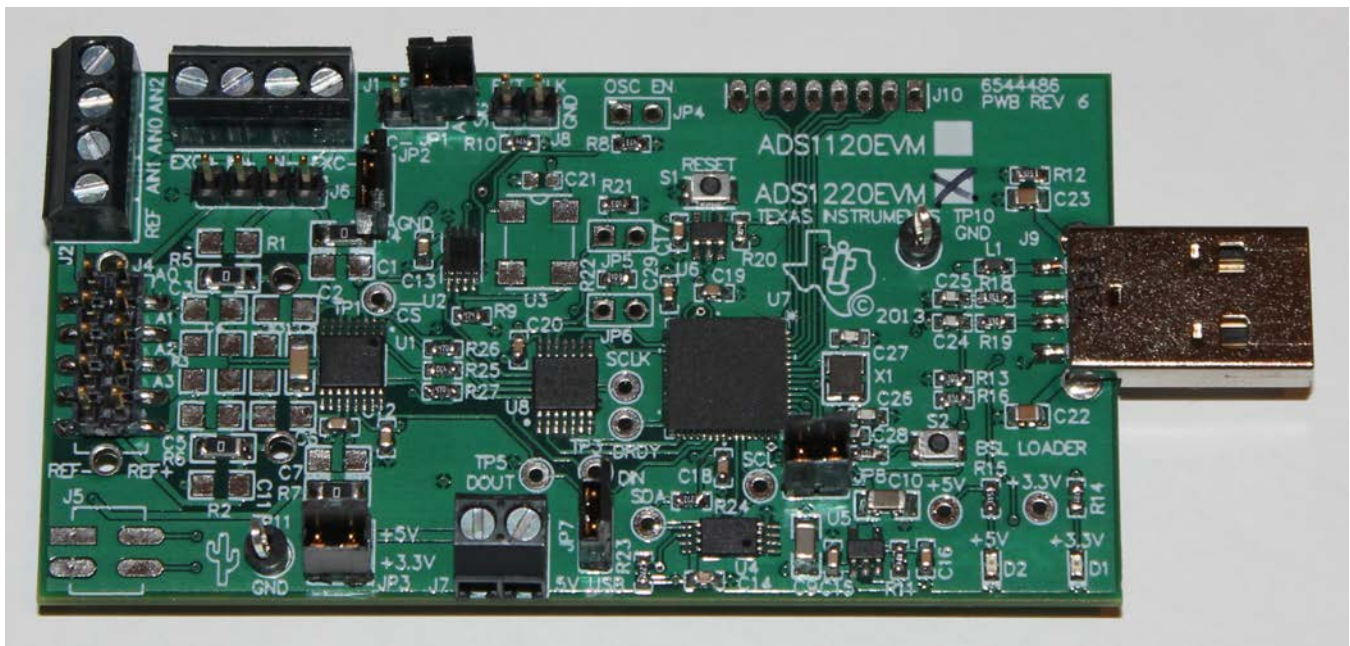# *ADS1x20EVM*

ADS1x20EVM

This user's guide describes the characteristics, operation, and use of the ADS1x20EVM. These evaluation modules are an evaluation system for the ADS1220, a 24-bit, low-power, multichannel, delta-sigma (ΔΣ), analog-to-digital converter (ADC) and the ADS1120, which is the 16-bit version of the ADS1220. The EVM allows evaluation of all aspects of the ADS1x20 devices.

This document includes an EVM Quick Start, hardware and software details, bill of materials, and schematic. Table 1 lists the related documents available through the Texas Instruments web site at www.ti.com.

Table 1. EVM-Compatible Device Data Sheets

Device	Literature Number	Device	Literature Number
ADS1120	SBAS535	MSP430F5528	SLAS590
ADS1220	SBAS501	TPS3838L30	SLVS292
SN74LVC2G157	SCES207	SN74LVC125A	SCAS290
TPS76333	SLVS181	—	—

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Contents

1   EVM Overview

The ADS1x20EVM is an evaluation module that includes an MSP430™ microcontroller and software. The ADS1x20EVM is useful for prototyping designs and firmware as well as for evaluation.

1.1   Features

ADS1x20EVM Features:

- Contains all support circuitry needed for the ADS1120 and ADS1220
- Voltage reference options: internal or external
- Clock options: internal or external
- MSP430 microcontroller with JTAG interface
- Compatible with the TI LaunchPad

The ADS1x20EVM includes an interface for serial communication that can be used with ADCPro™ to quickly evaluate the device.

This manual covers the operation of the ADS1x20EVM. Throughout this document, the abbreviation *EVM* and the term *evaluation module* are synonymous with the ADS1120EVM and ADS1220EVM. For clarity of reading, the remainder of this manual refers only to the ADS1220EVM, but operation of the EVM for the ADS1120 is identical, unless otherwise noted.

2   Quick Start

This section provides a Quick Start guide to quickly begin evaluating the ADS1220EVM with ADCPro.

2.1   Default Jumper and Switch Configuration

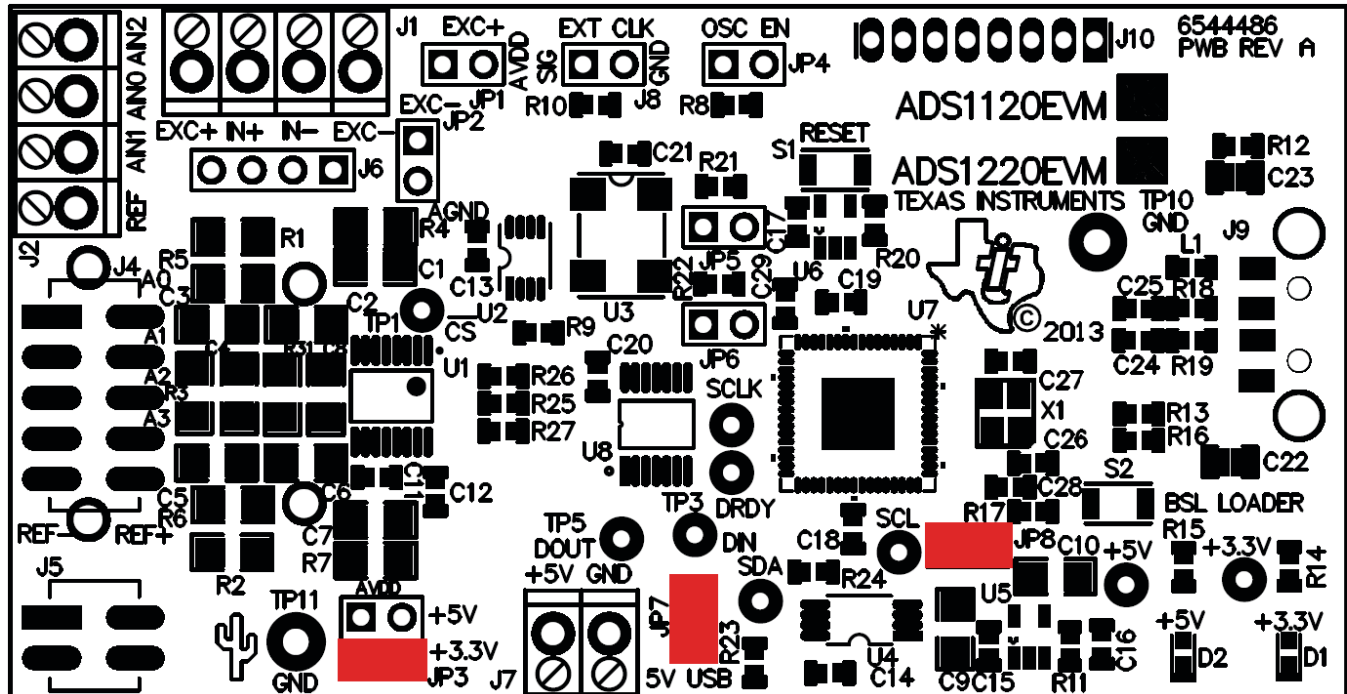Figure 1 shows the jumpers found on the EVM and the respective factory default conditions for each.

Figure 1. ADS1x20EVM Default Jumper Locations

Table 2 lists the primary jumpers and the factory default conditions.

Table 2. Default Jumper and Switch Configuration

Jumper	Default Position	Description
JP1	Open	EXC+ connected to AVDD
JP2	Open	EXC- connected to AGND
JP3	Short pins 2-4	AVDD supply connection to +5 V or +3.3 V (default to +3.3 V)
JP7	Short	USB power connected to +5 V
JP8	Short	U5 output connected to +3.3 V

2.2   ADS1220EVM Operation

To prepare to evaluate the ADS1220 with the ADS1220EVM, complete the following steps:

1. Verify the jumpers on the ADS1220EVM are as shown in Figure 1 (note that these settings are the factory-configured settings for the EVM).
2. Using ADCPro HW/SW Installation Manual, install the ADCPro and ADS1220EVM plug-in software. Plug-in software installs the necessary driver for USB communication.
3. Plug the ADS1220EVM into an available USB port. The EVM is configured to power from the USB port.

3 Quick Reference

Table 3 provides a quick summary of the key connections necessary for EVM operation. This information is helpful when using an external processor, or for monitoring EVM operation.

Table 3. Critical Connections

Function		Header (Pin)	Pin Name	Description
SPI	$\overline{CS}$	JAC.3 (TP1)	$\overline{CS}$	Chip select
	SCLK	JDB.16 (TP2)	SCLK	Serial clock
	DIN	JAC.15 (TP3)	DIN	Data in
	DOUT/$\overline{DRDY}$	JDB.18 (TP5)	DOUT	Data out
	$\overline{DRDY}$	JAC.11 (TP4)	$\overline{DRDY}$	Data ready
Power	+3.3 V	JAC.1 (TP9)	+3.3V	Digital or analog supply
	+5 V	JAC.2, J7 (TP8)	+5V	Analog supply
Analog inputs	Channel 1	J1.4, J2.2, J4.2, J6.4	AIN0/REFP1	Analog or reference input
	Channel 2	J1.3, J2.3, J3.2, J4.4, J6.3	AIN1	Analog input
	Channel 3	J1.2, J2.1, J3.1, J4.6, J6.2	AIN2	Analog input
	Channel 4	J1.1, J4.8, J6.1	AIN3/REFN1	Analog or reference input
	External reference	J2.4, J4.10	REFP0	Reference input (+)
		J4.9	REFN0	Reference input (−)

3.1 Analog Inputs

The analog inputs for the ADS1220EVM are connected to J1, J2, J3, J4, and J6. Channels 1 to 4 and the external reference, connect to header J4.

3.2 Digital Control

The digital control signals can be applied directly to connectors JAC and JDB. The connector footprints are on the bottom side of the board and the connectors are not installed.

3.3 Power Supply

The ADS1220EVM requires power rails as follows:
- +5-V analog supply: supplied by USB or from an external source connected to J7.
- +3.3-V digital or analog supply: can be supplied from the +5-V supply.

3.4 Voltage Reference

The ADS1220EVM has three options for the reference voltage: an internal reference and two possible external reference inputs (REF0 and REF1). The ADS1220 internal reference is selected at power up. Two external reference connections are available as follows:
- REF0 dedicated reference input connected to J2.4 and J4.9-10, and
- REF1 shared with analog inputs connected to J1.1, J1.4, J2.2, J4.2, J4.8, J6.1, and J6.4.

4 Using the ADS1220EVM ADCPro Plug-in

The ADS1220EVM plug-in for ADCPro provides complete control over all settings of the ADS1220. The plug-in consists of a tabbed interface (see Figure 2), with different functions available on different tabs. The tabs are:

- I/O Config
- Current & Ref
- About

The user can adjust the ADS1220EVM settings when not acquiring data. During acquisition, all controls are disabled and settings may not be changed. When a setting is changed on the ADS1220EVM plug-in, the setting immediately updates on the board. Settings on the ADS1220EVM correspond to settings described in the ADS1220 product data sheet.

4.1 Top-Level Controls

The ADS1220EVM settings can be adjusted when not acquiring data. During acquisition, all controls are disabled and settings may not be changed.

The effective data rate of the ADS1220 depends upon the frequency of the clock used. The default operating mode is the internal clock oscillator of the ADS1220, which is 4.096 MHz. The **Data Rate** indicator in the upper right corner of the plug-in interface (see Figure 2) is always visible and updates whenever a setting changes that affects the data rate. The indicated values are representative of the internal clock frequency of the ADS1220 and the operating clock mode (*Normal, Duty-Cycle, or Turbo*). The default operating mode is *Normal*. The **Data Rate** is adjusted by making the desired selection from the drop-down menu.

The **Gain** indicator in the upper left corner of the plug-in interface (see Figure 2) is always visible and updates whenever a setting changes that affects the gain. The indicated values are representative of the state of the **PGA Bypass**. If **PGA Bypass** is selected on the *I/O Config* tab (as shown in Figure 2), only gains of 1, 2, and 4 are bypassed from the PGA. All other gain settings require the PGA to be enabled. When higher gains are selected, the PGA is enabled regardless of the **PGA Bypass** state. To limit confusion regarding the state of the PGA, the only possible selections for **PGA Bypass** is 1, 2, or 4 from the drop-down menu.

The only way to view output data results is by operating the ADS1220 in continuous conversion mode. This mode is identified by the **Cont Conv** button indicator (as shown in Figure 2) on the bottom left of the ADS1220EVM plug-in. The button is lit green when in continuous conversion mode, otherwise the ADS1220 is in single conversion mode in a power-down state. No data can be collected while not in **Cont Conv** and are only useful for monitoring supply currents to determine power consumption of the ADS1220 while in power-down.

4.2   I/O Config Tab

The ADS1220 can acquire data from only one channel at a time. The **I/O Config** tab (as shown in Figure 2) provides control of the **MUX** selection. **MUX** selections correspond to settings described in the ADS1220 product data sheet. The remaining control settings discussed in this document also correspond to settings described in the product data sheet.
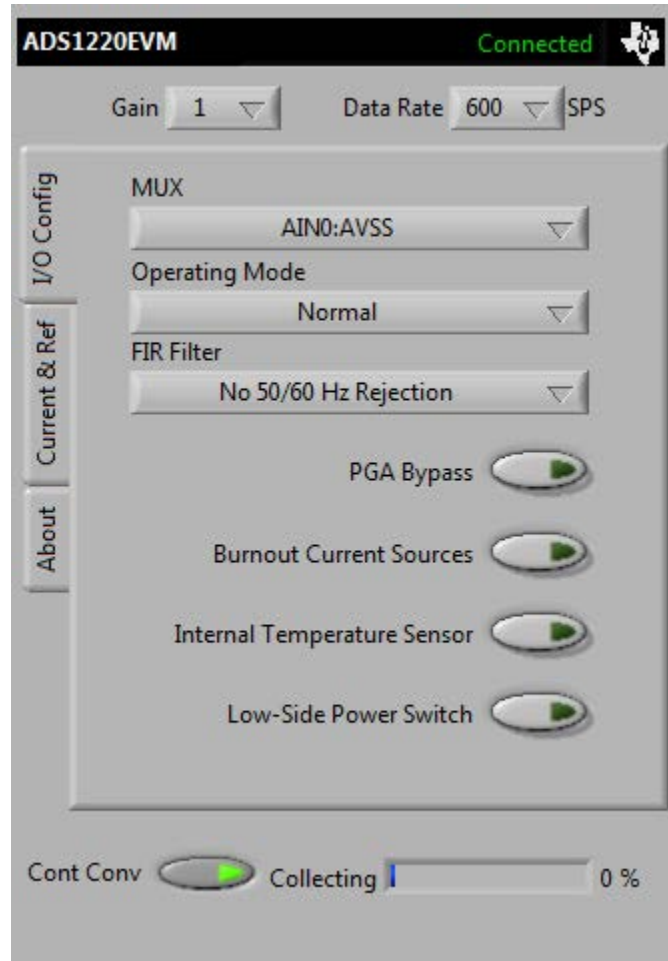
Figure 2. I/O Config

Operating Mode controls the speed of the modulator clock. Depending on the **Operating Mode** selected from the drop-down menu, the **Data Rate** changes appropriately. *Normal* is the normal operating mode of the ADS1220, *Turbo* doubles the **Data Rate** from *Normal*, and *Duty-Cycle* mode reduces the **Data Rate** from *Normal* by four.

FIR Filter settings enable changes to be made to the output response of the digital filter. The default condition is to have *No 50/60 Hz Rejection*. Other options from the drop-down menu allow for *Simultaneous 50/60 Hz Rejection*, *50 Hz Rejection Only*, or *60 Hz Rejection Only*.

Four other button options appear on the **I/O Config** tab. The first button controls the **PGA Bypass**. When the **PGA Bypass** button is active (indicated when lit green), the **Gain** choice is limited to *1, 2*, or *4*. The benefit of using **PGA Bypass** is removing the common-mode input restriction of the PGA so the full analog supply range for single-ended measurements can be used. This benefit, however, comes at the cost of lowered input impedance for the ADS1220.

The **Burnout Current Sources** button controls the 10-µA burnout current sources. When this button is lit green, the burnout current is routed through the selected **MUX** channel and detects any breaks or shorts to a connected sensor.

When the **Internal Temperature Sensor** button is activated and lit green, the output result from the ADS1220 is the response of the internal temperature sensor of the ADS1220. The temperature sensor is a precision device and can monitor the internal temperature of the ADS1220. The temperature sensor can also be used for making cold-junction temperature measurements when using thermocouples.

When lit green, the **Low-Side Power Switch** button allows for direct connection of the AIN3 input to AVSS while the ADS1220 is converting. This connection is useful when making bridge-type measurements and trying to conserve power. Power conservation is due to bridge excitation only taking place while the ADS1220 is converting. Demonstrating the usefulness of this option using the ADS1220EVM plug-in is difficult because the ADS1220 is always collecting data in the continuous conversion mode of operation. However, power savings can be calculated by comparing the total power used while converting, as compared to the total power of the power-down mode.

4.3 Current & Ref Tab

The **Current & Ref** tab allows various reference options to be selected along with the control and routing of IDAC currents, as shown in Figure 3.
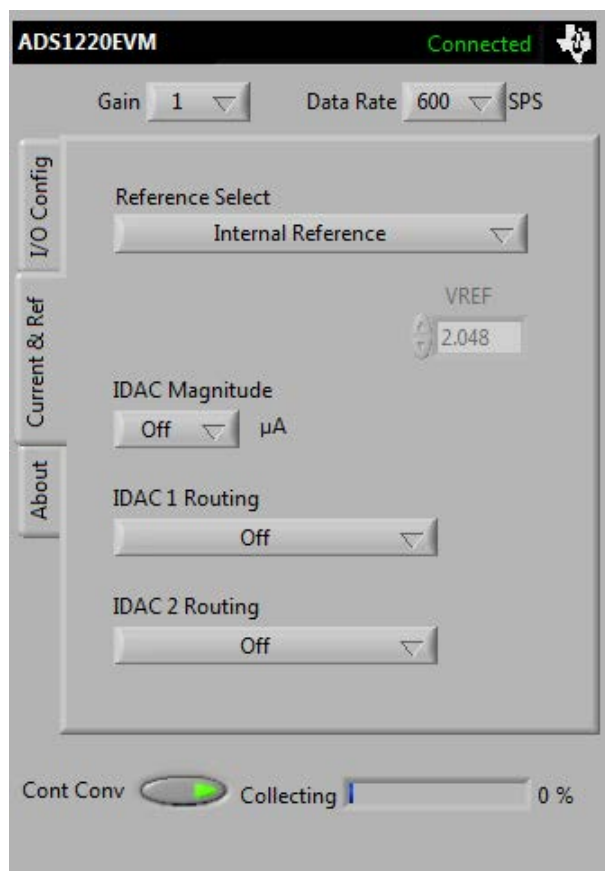

Figure 3. Current and Ref

Reference Select selects the reference for the ADS1220. The drop-down menu lists four options. The *Internal Reference* selection uses the ADS1220-derived, 2.048-V reference. The three remaining options use the voltage connected to the *REFP0*, *REFP1*, or the analog supply voltage (*AVDD*). When using a test plug-in with ADCPro, the output results displayed as volts are determined according to the **VREF** indicator voltage. The value of **VREF** defaults to 2.048 V, which is the internal voltage reference of the ADS1220. When using an external reference, change the **VREF** indicator to the appropriate reference voltage value. This adjustment ensures that the results displayed in the test plug-in of ADCPro are changed to the correct value.

The **IDAC Magnitude** drop-down menu allows the choice of current settings for the constant-current output digital-to-analog converters (DACs) of the ADS1220. Two current output DACs are available and can be routed independent of one another through the **IDAC 1 Routing** and **IDAC 2 Routing** controls. However, the **IDAC Magnitude** is the same for both current sources and the current output is not independently controlled. No current sources from the IDACs if the **IDAC Magnitude** is *Off*. This condition is true even if the IDAC routing controls have the IDACs routed to a specified output. The seven output current magnitude options are *10uA, 50uA, 100uA, 250uA, 500uA, 1000uA*, and *1500uA*. If both IDACs are routed to the same output, the IDAC current available is twice the indicated **IDAC Magnitude**.

The IDAC current sources can be routed independently or to the same output. The control for the **IDAC 1 Routing** and **IDAC 2 Routing** have the same drop-down menu options. If the IDAC routing is *Off*, then the IDAC being controlled is disabled and no current is sourced. This condition is true even if the **IDAC Magnitude** indicates an available current. The IDAC current can be routed out through any of the analog or reference input channels.

4.4 About Tab

The *About* tab provides information on the EVM hardware and software versions.

Plug-in Version is the software version of the ADCPro plug-in.

Firmware Version is the firmware version loaded and running on the processor.

5 ADS1220EVM Hardware Details

The ADS1220EVM is designed to easily interface with other control platforms. Dual-row socket options (JAC and JDB) are available on the bottom-side of the EVM, which allows for the controller connection. The pin configuration of the connectors is designed to be compatible with LaunchPad. The connector footprint conforms to Samtec™ connector SSW-110-22-F-D-VS-K, which is a dual-row, 20-pin, surface-mount socket with a 0.1-inch pitch spacing.

Another method of controlling the ADS1220 is by connecting control signals to the test points for digital communication to the ADS1220.

If using another controller other than the on-board MSP430, the control signals for this device must become inoperative. To deactivate the on-board processor, short the JP5 pins, which places the output of buffer U8 into a 3-state condition. Jumper JP5 is not installed by default. A wire can be soldered to the terminals of JP5, or a standard 0.1-inch pitch header with shorting block can be installed.

5.1 Jumpers and Switches

Jumpers and switches function as shown in Table 4.

Table 4. Jumper and Switch Descriptions

Jumper or Switch	Functions	Descriptions
JP1	EXC+ source	Short: Connect AIN0 (EXC+ of J1.4 and J6.4) to AVDD Open: AIN0 is not connected to AVDD (default)
JP2	EXC– source	Short: Connect AIN3 (EXC– of J1.1 and J6.1) to AGND Open: AIN3 is not connected to AGND (default)
JP3	Analog supply source	Short 1 to 2 (top): AVDD is connected to +5 V Short 3 to 4 (bottom): AVDD is connected to +3.3 V (default)
JP4	Clock source	Short: External oscillator is used as the clock source (requires installation) Open: On-board or external (J8) clock source (default)
JP5	Digital control source	Short: External controller Open: On-board controller
JP6	External clock source	Short: Controller clock (not currently available) Open: Connected J8 clock source (default)
JP7	+5-V source	Short: Powered from the USB (default) Open: +5 V supplied at J7 (also available at the JAC pin 2 and +5-V test point)
JP8	+3.3-V source	Short: Regulated LDO on-board supply (default) Open: Supplied externally at JAC or to +3.3-V test point
S1	Controller reset	Normally open SPST push-button resets controller on button press
S2	Controller BSL	Normally open SPST push-button enters controller bootstrap loader (BSL) mode with button press while +3.3-V power is applied

5.2 Analog Headers, Terminal Blocks, and J3

For maximum flexibility, the ADS1220EVM is designed for easy interfacing to multiple analog sources. These connectors provide access to the analog input pins of the ADS1220.

The EVM is designed to accept multiple sensor types. The sensor types can range from thermocouples, resistance temperature detectors (RTDs), load cells, pressure, and so forth. The analog inputs can be filtered by installing passive components in the optional filter circuitry. By default, the series input resistors are populated with 0-Ω resistors and the capacitors are not installed. No circuitry is provided to buffer these signals before connecting to the converter.

5.2.1 Primary Analog Interface, J4

All available analog pins of the ADS1220 connect to header J4. J4 can be used to connect analog signals from off-board sensors or sources to the ADS1220. Table 5 provides J4 pin descriptions. J4 is a standard 10-pin, dual-row header, with 0.1-inch pin spacing.

Table 5. J4: Primary Analog Interface Pinout

Description	Signal	Pin Number
Analog dedicated reference input, negative	REFN0	J4.9
Analog dedicated reference input, positive	REFP0	J4.10
Analog ground	AGND	J4.1[1]
	AGND	J4.3
	AGND	J4.5
	AGND	J4.7
Analog input channel 1	AIN0/REFP1	J4.2
Analog input channel 2	AIN1	J4.4
Analog input channel 3	AIN2	J4.6
Analog input channel 4	AIN3/REFN1	J4.8

[1] Pin 1 is at the top left-hand corner, located opposite of the reference designator.

5.2.2 Bridge Sensor Connectors, J1 and J6

Connectors J1 and J6 are designed to be used with bridge sensor applications. J1 is a four-position screw terminal block that can accept wire sizes AWG 28-16. J6 is a standard single-row, 4-pin header with 0.1-inch pin spacing. Both connectors allow for excitation to be connected to the outer pins while the differential signals from the sensor connect to the inner pins. Table 6 lists pin descriptions.

Bridge excitation is provided from the analog supply as needed. JP1 connects EXC+ directly to AVDD. JP2 connects EXC– directly to AGND. To conserve power, EXC– can also be connected to AGND through the low-side switch of the ADS1220.

Table 6. J1 and J6: Bridge Sensor Connectors

Description	Signal	Pin Number
Analog input, negative (IN–)	AIN2	J1.2 or J6.2
Analog input, positive (IN+)	AIN1	J1.3 or J6.3
Bridge excitation, negative (EXC–)[1] Negative reference input for ratiometric measurement (REFN1)	AIN3/REFN1	J1.1[2] or J6.1[2]
Bridge excitation, positive (EXC+)[3] Positive reference input for ratiometric measurement (REFP1)	AIN0/REFP1	J1.4 or J6.4

[1] EXC– can be connected to AGND through JP2, or through the low-side switch of AIN3/REFN1 of the ADS1220.
[2] Pin 1 is at the top right-hand corner, located next to the reference designator.
[3] EXC+ can be connected to AVDD through JP1.

5.2.3 RTD Terminal Block J2

J2 is a four-position screw terminal block that can accept wire sizes AWG 28-16. The main purpose for J2 is to provide a connection for measuring a resistance temperature device (RTD). A two-, three-, or four-wire RTD can be connected to J2. Measurement channels are AIN0 and AIN1. Current excitation is directly possible from AIN0, AIN1, and AIN2. For three-wire RTDs, any combination of two excitation sources can be used.

One problem with using a three-wire RTD is in regards to driving current through analog input filtering. This problem can be avoided by installing resistor R30, which allows AIN3 to be used as a second current source. Placing a 0-Ω resistor at R30 creates a direct connection between AIN3 and J2.3 (AIN1). Table 7 lists pin descriptions.

RTD measurement is best as a ratiometric measurement. Excitation current establishes a reference voltage at the dedicated reference REP0/REFN0. 'Establishing the reference voltage requires that a bias resistor be installed at R3. R3 should be a precision, low-drift resistor. The value chosen depends on the RTD value and excitation current, as well as maintaining IDAC voltage compliance for the ADS1220. For a complete current path, one side of R3 (REFN0 side) must connect to AGND. The easiest way to accomplish this connection is to place a shorting jumper from J4.9 to J4.7.

Table 7. J2: RTD Terminal Block Connector

Description	Signal	Pin Number
Analog input, negative (IN–)	AIN1	J2.3[1]
Analog input, positive (IN+)	AIN0	J2.2
Reference bias resistor connection[2]	REFP0	J2.4
RTD current excitation [3]	AIN2	J2.1[4]

[1] When using a three-wire RTD, AIN3 can be used as a current source by installing a 0-Ω resistor at R30.
[2] Bias resistor R3 must be installed. To complete the current path, REFN0 must also be connected to ground.
[3] Direct connection to three- and four-wire RTDs. A two-wire RTD requires a jumper between J2.1 and J2.2 as well as between J2.3 and J2.4. Three-wire RTDs require an additional excitation current.
[4] Pin 1 is at the top left-hand corner of the EVM, located opposite from the reference designator.

5.2.4 Thermocouple Connector, J3

Provision for a miniature thermocouple connector is provided on the EVM. The socket connector footprint accommodates the Omega® PCC-SMP-style connector at J3. The J3 connector should be installed on the bottom-side of the EVM. The J3 terminals connect to AIN1 and AIN2 of the ADS1220. Biasing resistors R1 and R2 can be installed to place the thermocouple into the correct common-mode input range of the ADS1220.

A cold-junction area is provided for compensation (CJC) and the ADS1220 temperature sensor can be used to measure the temperature of the cold junction. Provision for a RTD chip temperature-sensing device is located at R31. An example of what can be used at R31 is the Vishay® Beyschlag PTS120601B100RP100. When using a RTD at R31, excitation current is provided from AIN3. For a complete current path, AIN3 must connect to R31. This connection can be accomplished by placing a jumper wire at J4.2 to J4.8 of connector J4. Similar jumper options are also available at connectors J1 and J6.

5.2.5 Analog Input Filtering Options

The analog input connectors directly connect to the ADS1220 inputs using 0-Ω resistors by default. Filters, such as antialiasing or electromagnetic interference and radio frequency interference (EMI/RFI), can be installed using the resistor and capacitor pads available at the analog side of the ADS1220. These pads are found on both the top- and bottom-side of the EVM. Device pads are available to create filter combinations for both differential and common-mode filters for many different input configurations. Filtering combinations are also included for filtering the external reference inputs.

5.3   Clock Source Options

The ADS1220 clock can come from one of several sources: the internal oscillator of the ADS1220, an oscillator installed at U3, a clock supplied by a processor via U8, or an external clock source connected to J8. The default configuration is to use the internal oscillator of the ADS1220.

If a precision oscillator is installed at U3, a 10-nF capacitor should also be installed at C21. To allow the clock to pass through multiplexer U2, the enable jumper must be installed at JP4. A standard 0.1-inch pitch header and shorting block can be installed at JP4 for this purpose. A more permanent solution is accomplished by soldering a small piece of wire to the terminals of JP4. JP4 can be found near the center of the top edge of the EVM.

An external clock can also be attached to connector J8. The clock signal must conform to the 3.3-V logic used for the EVM. A clock provided by the controller is not available at this time.

5.4   Digital Interface

Primary control of the ADS1220 is via MSP430 controller U7. U7 communicates to the ADS1220 to read and write register settings as well as to retrieve conversion data. U7 also responds to commands sent from the ADS1220EVM plug-in when using ADCPro. When the EVM is plugged into an available USB port, U7 enumerates as a communications device class (CDC) peripheral operating as a virtual COM port. The USB physical connection is through J9, which is a standard type A connector located on the right side of the ADS1220EVM. J9 can be plugged directly into an available USB port connector of the computer. An extension cable can also be used instead of the direct connection.

U7 uses two hardware peripherals to control devices on the ADS1220EVM. One peripheral uses SPI™ to communicate with the ADS1220. The second peripheral is an I^2C™ master. The primary purpose for the I^2C is for communication to the EEPROM (U4) that contains specific information regarding the configuration of the EVM. I^2C devices can also be connected to J5, but additional changes to the firmware are required for communication. See Section 5.4.1 for details on these pins.

If firmware changes or updates are required for U7, two update methods are possible. One method is via JTAG connector J10 (uninstalled). See Section 5.4.2 for details on these pins. The second method is by using the bootstrap loader (BSL) of the MSP430. For further information, see the Texas Instruments web site at www.ti.com.

Alternative control of the ADS1220 from other processors is possible by either connecting the processor control signals to the test points for the digital signals, or by using the JAC and JDB connectors located on the bottom-side of the ADS1220EVM. See Section 5.4.3 for details on these pins and their operation.

5.4.1   Auxiliary Device Connector, J5

The ADS1220 allows the I^2C serial interface to be used with an external device. To use this option, the controller firmware must be modified. Optional connector J5 must be installed. The J5 connector is similar to J4. A Samtec TSM-102-01-L-DV-P or equivalent can be used. Table 8 provides details on the J5 pins.

Table 8. J5: Auxiliary Connector

Function	Signal Name	Pin Number (J5)
Analog ground	AGND	3
Analog supply	AVDD	1
Serial clock	SCL	4
Serial data	SDA	2

5.4.2 JTAG Connector, J10

Firmware downloading and debugging is possible through JTAG connector J10. The 14-pin connector of the MSP-FET430UIF debug interface is reduced to a minimum number of pins to limit connector size and space available on the EVM. The J10 logic levels are 3.3-V CMOS. A four-wire JTAG interface is available. Table 9 shows a comparison between the 14-pin debugger connections in relation to J10. The information can be used to create an adapter between J10 and the 14-pin debugger cable. The J10 footprint is a 2-mm pitch spacing if a socket or header is used.

Table 9. JTAG Interface Connections

Function	Debugger Connector	Pin Number (J10)
GND	Pin 9	8
N/C	Pin 6	n/a
N/C	Pin 10	n/a
N/C	Pin 12	n/a
N/C	Pin 13	n/a
N/C	Pin 14	n/a
$\overline{\text{RST}}$	Pin 11	7
TCK	Pin 7	5
TDI/VPP	Pin 3	3
TDO/TDI	Pin 1	2
TEST/VPP	Pin 8	6
TMS	Pin 5	4
VCC debugger	Pin 2	1
VCC target	Pin 4	n/a

5.4.3 External Control

The header and socket connectors, JAC and JDB, provide access to the digital control and serial data pins of the ADS1220. To use this option, connectors must be installed on the bottom-side of the ADS1220EVM. Also, the on-board controller must have the control functions disabled. The outputs of the on-board controller pass through 3-state buffers, U8. To disable the output of the buffers, jumper JP5 must be shorted. This jumper is not installed by default. A wire can be soldered to the terminals of JP5, or a standard 0.1-inch pitch header with a shorting block can be installed.

All logic levels on JAC and JDB are 3.3-V CMOS. Table 10 describes the JAC serial interface pins, and Table 11 describes JDB. The connector footprint conforms to the Samtec connector SSW-110-22-F-D-VS-K, which is a dual-row, 20-pin, surface-mount socket with 0.1-inch pitch spacing.

Table 10. JAC: External Interface Connector

Function	Signal Name	Pin Number (JAC)
ADS1220 data in	DIN	15
ADS1220 device select	$\overline{CS}$	3
ADS1220 interrupt output	$\overline{DRDY}$	11
Analog power supply	+5V	2
Digital power supply	+3.3V	1[1]
N/C	N/C	5-10, 12-14, 16-20
Power-supply ground	AGND/DGND	4

[1] Pin 1 is bottom-side below and to the right of the reference designator.

Table 11. JDB: External Interface Connector

Function	Signal Name	Pin Number (JDB)
ADS1220 data out	DOUT/$\overline{DRDY}$	18
I^{2}C serial clock	SCL	14
I^{2}C serial data	SDA	12
N/C	N/C	1[1], 3-11, 13, 15, 17, 19, 20
Power-supply ground	AGND/DGND	2
SPI serial clock	SCLK	16

[1] Pin 1 is at the bottom-side below and to the right of the reference designator.

5.5 Power-Supply Connections

The primary power supply is +5 V. The +5-V supply derives the +3.3 V with LDO regulator U5. +3.3 V is required for powering the digital components on the EVM. The analog supply can be either +3.3 V or +5 V, and is selectable at jumper JP3.

+5 V can be supplied via USB (default), or can be wired to the terminal block J7. If J7 is used, the USB supply can be disconnected from the EVM by removing the shorting jumper JP7. If the external controller option is used through JAC, both the +3.3 V and +5 V can be connected as either a source or target supply. If +3.3 V is supplied to the EVM, jumper JP8 should be removed so that U5 does not sink current from an external source.

6 Schematic and Bill of Materials

A complete schematic for the ADS1220EVM is appended to this user's guide. The bill of materials is provided in Table 12 and the schematic is appended to the end of this document. Gerber files are available on request. Please contact the E2E Community Forums and ask for details on how to receive the files.

6.1 Bill of Materials

NOTE: All components should be compliant with the European Union Restriction on Use of Hazardous Substances (RoHS) Directive. Some part numbers may be either leaded or RoHS. Verify that purchased components are RoHS-compliant. (For more information about TI's position on RoHS compliance, see www.ti.com.)
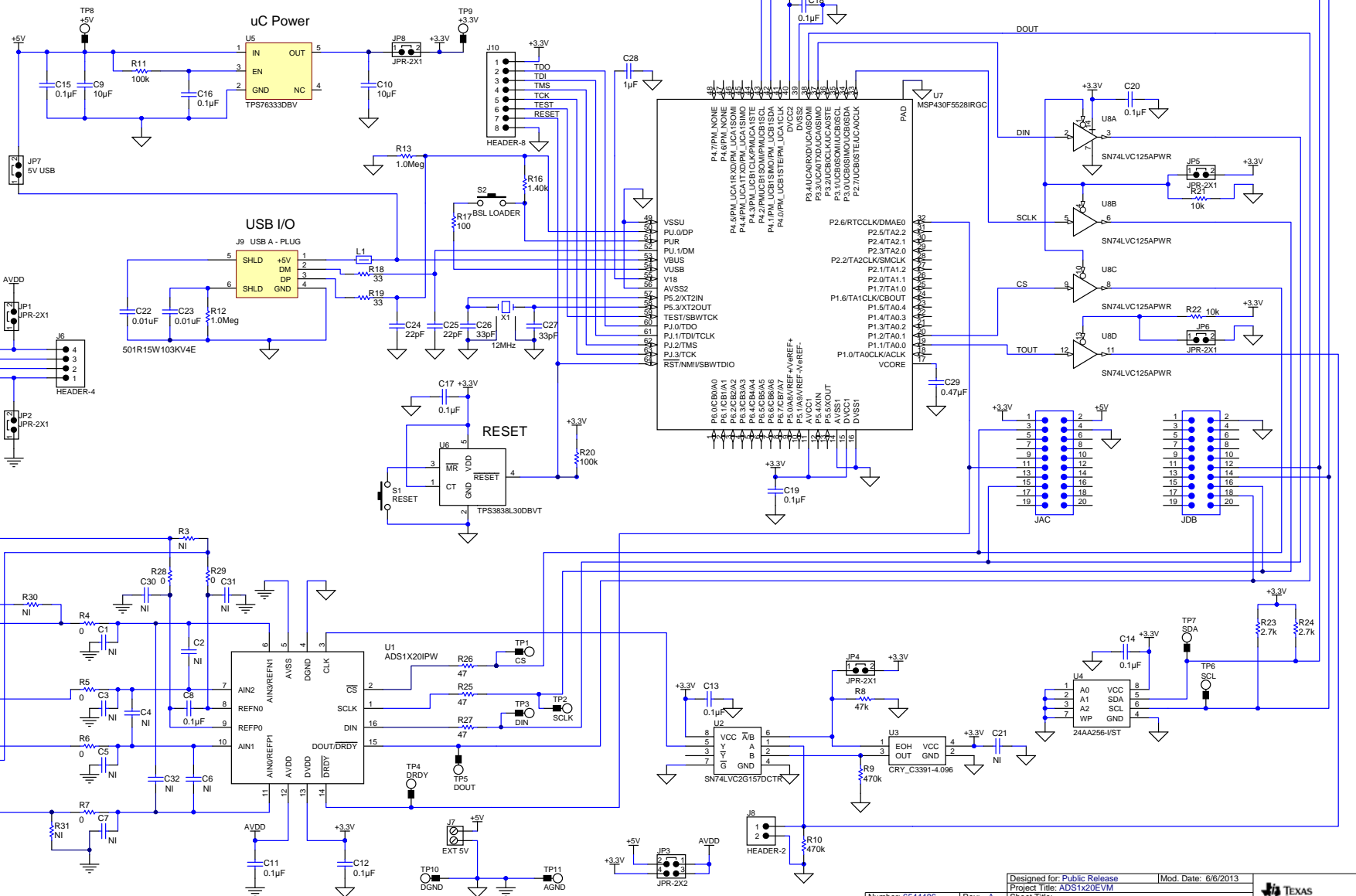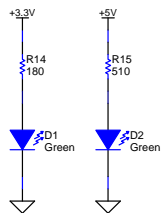

Table 12. ADS1x20EVM Bill of Materials

Item No.	Qty	Value	Ref Des	Description	Manufacturer	Part Number
1	1	0.1u	C8	Capacitor, Ceramic, X7R, 50V	Kemet	C1206C104J5RACTU
2	2	10u	C9-10	Capacitor, Ceramic, X7R, 10V	Kemet	C1206C106K8RACTU
3	10	0.1u	C11-20	Capacitor, Ceramic, X7R, 16V	Kemet	C0603C104J4RACTU
4	2	10n	C22-23	Capacitor, Ceramic, X7R, 500V	Johanson Dielectrics Inc.	501R15W103KV4E
5	2	22p	C24-25	Capacitor, Ceramic, C0G, 50V	Kemet	C0603C220J5GACTU
6	2	33p	C26-27	Capacitor, Ceramic, C0G, 50V	Kemet	C0603C330J5GACTU
7	1	1u	C28	Capacitor, Ceramic, X5R, 10V	Kemet	C0603C105K8PACTU
8	1	0.47u	C29	Capacitor, Ceramic, X7R, 10V	Kemet	C0603C474K8RACTU
9	2		D1-2	LED, Green	Lite-On	LTST-C190GKT
10	2		J1-2	Terminal Block, Miniature, 4 position	On Shore Technology Inc	ED555/4DS
11	1		J4	Header, Male, SMT Vert. 5x2 pin, 100mil spacing	Samtec	TSM-105-01-L-DV-P
12	1		J6	Header, Male 4-pin, 100mil spacing	Samtec	TSW-104-07-L-S
13	1		J7	Terminal Block, Miniature, 2 position	On Shore Technology Inc	ED555/2DS
14	5		J8 JP1-2 JP7-8	Header, Male 2-pin, 100mil spacing	Samtec	TSW-102-07-L-S
15	1		J9	Connector, USB Plug, 4 position, RA	Molex Inc	0480371000
16	1		JP3	Header, Male, 2x2 pin, 100mil spacing	Samtec	TSW-102-07-L-D
17	1		L1	Ferrite Bead, 300mA, 600 ohm @ 100MHz	Laird-Signal Integrity Products	HZ0603C601R-10
18	6	0	R4-7 R28-29	Resistor, Chip, 1/4W, 5%	Yageo	RC1206JR-070RL
19	1	47k	R8	Resistor, Chip, 1/10W, 5%	Yageo	RC0603JR-0747KL
20	2	470k	R9-10	Resistor, Chip, 1/10W, 5%	Yageo	RC0603JR-07470KL
21	2	100k	R11 R20	Resistor, Chip, 1/10W, 5%	Yageo	RC0603JR-07100KL
22	2	1.0M	R12-13	Resistor, Chip, 1/10W, 5%	Yageo	RC0603JR-071ML
23	1	180	R14	Resistor, Chip, 1/10W, 5%	Yageo	RC0603JR-07180RL
24	1	510	R15	Resistor, Chip, 1/10W, 5%	Yageo	RC0603JR-07510RL
25	1	1.4k	R16	Resistor, Chip, 1/10W, 1%	Yageo	RC0603FR-071K4L
26	1	100	R17	Resistor, Chip, 1/10W, 5%	Yageo	RC0603JR-07100RL
27	2	33	R18-19	Resistor, Chip, 1/10W, 5%	Yageo	RC0603JR-0733RL
28	2	10k	R21-22	Resistor, Chip, 1/10W, 5%	Yageo	RC0603JR-0710KL
29	2	2.7k	R23-24	Resistor, Chip, 1/10W, 5%	Yageo	RC0603JR-072K7L
30	3	47	R25-27	Resistor, Chip, 1/10W, 5%	Yageo	RC0603JR-0747RL
31	2		S1-2	Switch, Pushbutton, SPST, SMD	Omron	B3U-1000P
32	2		TP10-11	Test Point, Black, Thru Hole Color Keyed	Keystone	5011
33	1 [1]		U1	IC, 2 Differential or 4 Single Ended, Delta-Sigma, 24-Bit A-D Converter	TI	ADS1220IPW

[1] Installed for ADS1220EVM. For other EVMs, the appropriate device will be installed.

Table 12. ADS1x20EVM Bill of Materials (continued)

Item No.	Qty	Value	Ref Des	Description	Manufacturer	Part Number
34	1		U2	IC, Single 2 Line To 1 Line Data Selector/Multiplexer	TI	SN74LVC2G157DCT
35	1		U4	IC, 256K CMOS Serial EEPROM	Microchip	24AA256-I/ST
36	1		U5	IC, +3.3V LDO Regulator, 150mA	TI	TPS76333DBVR
37	1		U6	IC, Supply Voltage Supervisor	TI	TPS3838L30DBVT
38	1		U7	IC, Microcontroller	TI	MSP430F5528IRGCT
39	1		U8	IC, Quad Gate, Tri-State Buffer	TI	SN74LVC125APWR
40	1	12MHz	X1	Crystal, 20ppm, SMD	Abracon	ABM8G-12.000MHZ-18-D2Y-T
41	1			PCB, 3.28 In x 1.70 In x 0.062 In	Any	6544486
42	5			Shunt, 100-mil, Black	3M	969102-0000-DA

ADS1x20EVM schematic — ADS1x20EVM-PW.SchDoc

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Should this evaluation board/kit not meet the specifications indicated in the User's Guide, the board/kit may be returned within 30 days from the date of delivery for a full refund. THE FOREGOING LIMITED WARRANTY IS THE EXCLUSIVE WARRANTY MADE BY SELLER TO BUYER AND IS IN LIEU OF ALL OTHER WARRANTIES, EXPRESSED, IMPLIED, OR STATUTORY, INCLUDING ANY WARRANTY OF MERCHANTABILITY OR FITNESS FOR ANY PARTICULAR PURPOSE. EXCEPT TO THE EXTENT OF THE INDEMNITY SET FORTH ABOVE, NEITHER PARTY SHALL BE LIABLE TO THE OTHER FOR ANY INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES.

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REGULATORY COMPLIANCE INFORMATION

As noted in the EVM User's Guide and/or EVM itself, this EVM and/or accompanying hardware may or may not be subject to the Federal Communications Commission (FCC) and Industry Canada (IC) rules.

For EVMs **not** subject to the above rules, this evaluation board/kit/module is intended for use for ENGINEERING DEVELOPMENT, DEMONSTRATION OR EVALUATION PURPOSES ONLY and is not considered by TI to be a finished end product fit for general consumer use. It generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to part 15 of FCC or ICES-003 rules, which are designed to provide reasonable protection against radio frequency interference. Operation of the equipment may cause interference with radio communications, in which case the user at his own expense will be required to take whatever measures may be required to correct this interference.

General Statement for EVMs including a radio

User Power/Frequency Use Obligations: This radio is intended for development/professional use only in legally allocated frequency and power limits. Any use of radio frequencies and/or power availability of this EVM and its development application(s) must comply with local laws governing radio spectrum allocation and power limits for this evaluation module. It is the user's sole responsibility to only operate this radio in legally acceptable frequency space and within legally mandated power limitations. Any exceptions to this are strictly prohibited and unauthorized by Texas Instruments unless user has obtained appropriate experimental/development licenses from local regulatory authorities, which is responsibility of user including its acceptable authorization.

For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant

Caution

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

For EVMs annotated as IC – INDUSTRY CANADA Compliant

This Class A or B digital apparatus complies with Canadian ICES-003.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

Concerning EVMs including radio transmitters

This device complies with Industry Canada licence-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concerning EVMs including detachable antennas

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication.

This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Cet appareil numérique de la classe A ou B est conforme à la norme NMB-003 du Canada.

Les changements ou les modifications pas expressément approuvés par la partie responsable de la conformité ont pu vider l'autorité de l'utilisateur pour actionner l'équipement.

Concernant les EVMs avec appareils radio

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes : (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante.

Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur.

【Important Notice for Users of EVMs for RF Products in Japan】

This development kit is NOT certified as Confirming to Technical Regulations of Radio Law of Japan

If you use this product in Japan, you are required by Radio Law of Japan to follow the instructions below with respect to this product:

1. Use this product in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,

2. Use this product only after you obtained the license of Test Radio Station as provided in Radio Law of Japan with respect to this product, or

3. Use of this product only after you obtained the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to this product. Also, please do not transfer this product, unless you give the same notice above to the transferee. Please note that if you could not follow the instructions above, you will be subject to penalties of Radio Law of Japan.

Texas Instruments Japan Limited
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EVALUATION BOARD/KIT/MODULE (EVM)
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For Feasibility Evaluation Only, in Laboratory/Development Environments. Unless otherwise indicated, this EVM is not a finished electrical equipment and not intended for consumer use. It is intended solely for use for preliminary feasibility evaluation in laboratory/development environments by technically qualified electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems and subsystems. It should not be used as all or part of a finished end product.

Your Sole Responsibility and Risk. You acknowledge, represent and agree that:

1. You have unique knowledge concerning Federal, State and local regulatory requirements (including but not limited to Food and Drug Administration regulations, if applicable) which relate to your products and which relate to your use (and/or that of your employees, affiliates, contractors or designees) of the EVM for evaluation, testing and other purposes.

2. You have full and exclusive responsibility to assure the safety and compliance of your products with all such laws and other applicable regulatory requirements, and also to assure the safety of any activities to be conducted by you and/or your employees, affiliates, contractors or designees, using the EVM. Further, you are responsible to assure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard.

3. Since the EVM is not a completed product, it may not meet all applicable regulatory and safety compliance standards (such as UL, CSA, VDE, CE, RoHS and WEEE) which may normally be associated with similar items. You assume full responsibility to determine and/or assure compliance with any such standards and related certifications as may be applicable. You will employ reasonable safeguards to ensure that your use of the EVM will not result in any property damage, injury or death, even if the EVM should fail to perform as described or expected.

4. You will take care of proper disposal and recycling of the EVM's electronic components and packing materials.

Certain Instructions. It is important to operate this EVM within TI's recommended specifications and environmental considerations per the user guidelines. Exceeding the specified EVM ratings (including but not limited to input and output voltage, current, power, and environmental ranges) may cause property damage, personal injury or death. If there are questions concerning these ratings please contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, some circuit components may have case temperatures greater than 60°C as long as the input and output are maintained at a normal ambient operating temperature. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors which can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during normal operation, please be aware that these devices may be very warm to the touch. As with all electronic evaluation tools, only qualified personnel knowledgeable in electronic measurement and diagnostics normally found in development environments should use these EVMs.

Agreement to Defend, Indemnify and Hold Harmless. You agree to defend, indemnify and hold TI, its licensors and their representatives harmless from and against any and all claims, damages, losses, expenses, costs and liabilities (collectively, "Claims") arising out of or in connection with any use of the EVM that is not in accordance with the terms of the agreement. This obligation shall apply whether Claims arise under law of tort or contract or any other legal theory, and even if the EVM fails to perform as described or expected.

Safety-Critical or Life-Critical Applications. If you intend to evaluate the components for possible use in safety critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, such as devices which are classified as FDA Class III or similar classification, then you must specifically notify TI of such intent and enter into a separate Assurance and Indemnity Agreement.

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