Design and Implementation of 8X2 SRAM Array in 45nm SCMOS Technology

Deepak Harinath
Pudukodu Gopalakrishnan
Department of Electrical and Computer Engineering
University of Florida

Shang Shi
Department of Electrical and Computer Engineering
University of Florida

Medini J Aradhya
Department of Electrical and Computer Engineering
University of Florida

Neel Kanjaria
Department of Electrical and Computer Engineering
University of Florida

***Abstract*—In this paper, we have presented the design and implementation of a (8x2) Static Random-Access Memory (Static RAM or SRAM) array with a fast read and write access. This paper includes the design of the individual blocks of the 8x2 SRAM array namely read-write circuit, precharge circuit, buffers, row and column decoders and sense amplifier. The gpdk 45nm technology node in Cadence virtuoso layout suite has been used to design and implement the schematic and layout of the SRAM array. The Layouts of the individual components and the integrated circuit have passed Design Rule Checking (DRC) and Layout versus Schematic (LVS) check. Reading and Writing into multiple cells was performed successfully and the timing of the circuit has been recorded. The sensitivity of the sense amplifier has also been discussed in this paper.**

***Index Terms*—8x2 SRAM array, Read/Write, Precharge, Buffer, Sense Amplifier, Decoders, Schematic, Layout, gpdk 45nm, DRC, LVS**

I. Introduction

6T SRAM or Static Random Access Memory is a semiconductor- transistor model of a memory storage element which consists of 6 transistors, 4 of which act as a bi-stable latch to store one bit value to either a 1 or a 0 while the other two act as access switches to reach this memory element. In this project we develop an array of such structures (8x2) and control the reading and writing from each one of these SRAM cells to depict a memory element that is used in the industry and often in most consumer electronic devices. CMOS circuits tend to consume low power and have high read and write speeds. Stacking these elements into arrays give us fast low-density devices capable of reading and writing in short spans of time. Owing to this feature SRAM arrays are often used in CPU and microprocessor cache memories. This project provided us with a comprehensive understanding of CMOS circuitry and gave us a platform to develop skills in full-custom VLSI design and simulation. Additionally, this design has been optimized to run blocks such as the sense amplifier only when needed and by limiting the precharge voltage in order to decrease the power consumption.

II. Design Description

The individual blocks that were used to design and implement the 16-bit (8x2) SRAM array are

- 6T SRAM cell
- Pre-charge circuit
- Buffers
- Row and Column Decoders
- Read and Write Control Circuitry
- Sense Amplifier

A. 6T SRAM cell

The SRAM cell is the block to which we write data and read data from. The SRAM cell is made up of 6 Transistors (4 NMOS and 2 PMOS). The SRAM design shown below in figure 1 has two stable states to store either a 0 or a 1. In the figure shown below, the parallel PMOS and NMOS are used to create two cross coupled inverters. The other 2 NMOS transistors are called access transistors of the SRAM cell. These access transistors are connected to bit line and bit line bar and are used to control the access to the cell during the read and write operations. The outputs of the SRAM are Q and Qbar. The voltages on these outputs correspond to either a ”0” or ”1”.

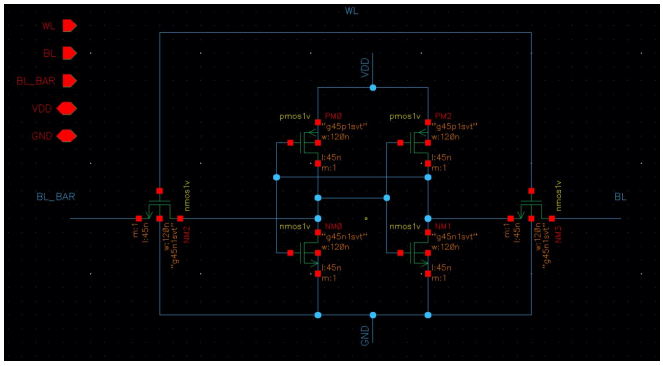

Fig. 1. SRAM Cell

B. Precharge Circuit

The precharge is an important component of SRAM array circuit and is driven by a clock. It is used to precharge the bit lines to VDD prior to the read and write operations. It uses four PMOS transistors and thus when the clock goes low, the bitlines are connected to VDD which helps in precharging BL and BL_ bar. The schematic for precharge circuit is shown in figure 2.

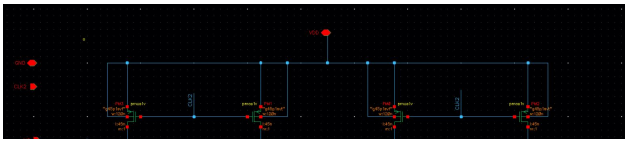

Fig. 2. Precharge Circuit

C. Buffer

The buffer is an important component for the timing of the circuit. It is not ideal for the array to read and write all the time. Hence, we introduce a clock which helps with the timing of the circuit. The buffer is an AND gate logic circuit which accepts 2 inputs. The buffer ensures the clock is synchronized for both the decoders and there is no delay during the read and write operations. The schematic of the buffer circuit is shown in figure 3.

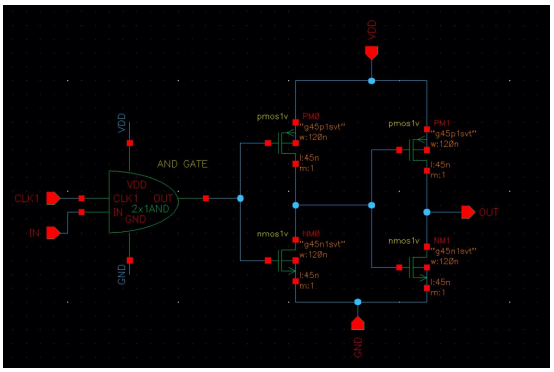

Fig. 3. Buffer

D. Row and Column Decoders

The decoder block is divided into two parts in our design: The Row decoder and the Column decoder. The row decoder is used to access the word lines in the SRAM array and the column decoder helps in differentiating the SRAM cells that use the same word lines. The row decoder accepts 3 address lines as input and uses a 3-input NOR gate logic circuit to decode them into 8-word lines as output for the SRAM array. The schematic of the row decoder is shown in figure 4. The

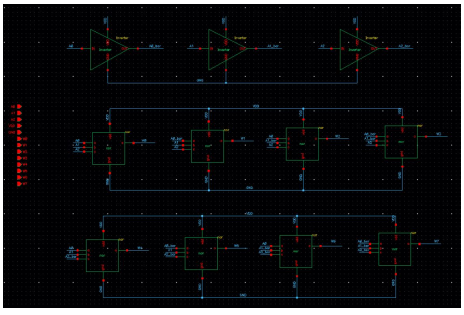

Fig. 4. Row Decoder

column decoder accepts a single input and produces 2 outputs using an inverter in its circuit. The schematic of the column decoder is shown in figure 5.

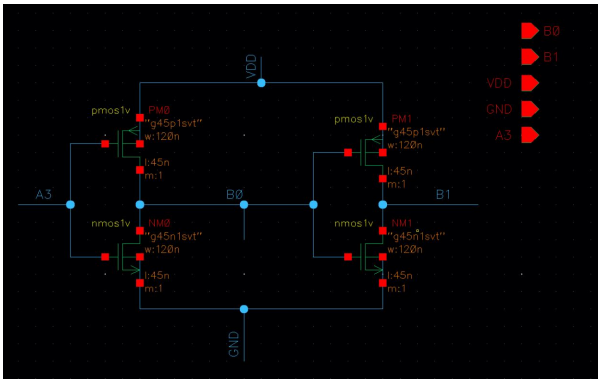

Fig. 5. Column Decoder

E. Read and Write Control Circuitry

The read and write circuitry is used to write to or read from a specific cell in the SRAM array. The desired word lines and column decoders need to be enabled first in order to access a specific cell from the array. Depending on the write and read signals, the circuit has 2 modes of operation. During the write operation, if the input data is 0, then a 1 is written onto the SRAM cell and when the input is 1, then a 0 gets written. During the read operation, both the bit lines should be precharged to VDD and the access should be ON. Similarly, during the write operation we need to precharge the bit lines to VDD and the pass gates should be open. Figure 6 shows the schematic of the read write control circuit used.

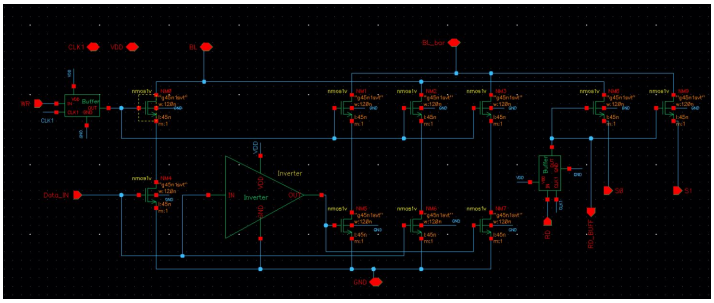

Fig. 6. Read-Write Circuit

F. Sense Amplifier

A Sense Amplifier is used to amplify the small voltage difference between the bit line and bit line bar during the read operation. This component is important as it helps in speeding up the reading process by amplifying even small differential voltages. A differential sense amplifier has been designed and implemented in this paper. The outputs of the sense amplifier during the write operation is not of any interest to us as ideally during the write operation, the read enable is switched off. The schematic of the sense amplifier used in the implementation is shown in figure 7.

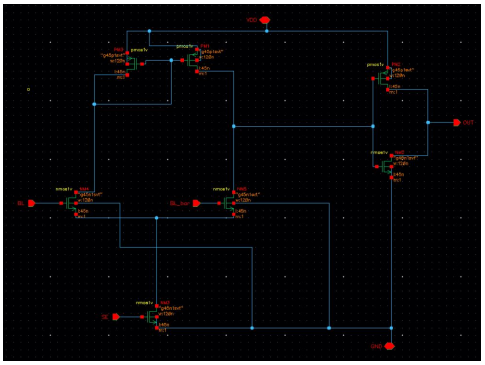

Fig. 7. Sense Amplifier

III. Implementation

The design has been implemented on 45 nm SCMOS technology in Cadence. A wide SRAM type has been used and the compactness has been taken into consideration while designing. In order to maintain uniformity, the Poly, Metal 3 and Metal 4 layers run horizontal and the connections were made with Metal 1 and Metal 2 unifying the separate blocks of the overall circuit. Write and Read has been performed to multiple cells of the SRAM array. Circuit timing, Layout areas were tabulated, and the sensitivity of the sense amplifier was determined. Individual blocks were tested for DRC and LVS checks before combining them to form the combined layout. The layout of the complete circuit is shown in figure 8.

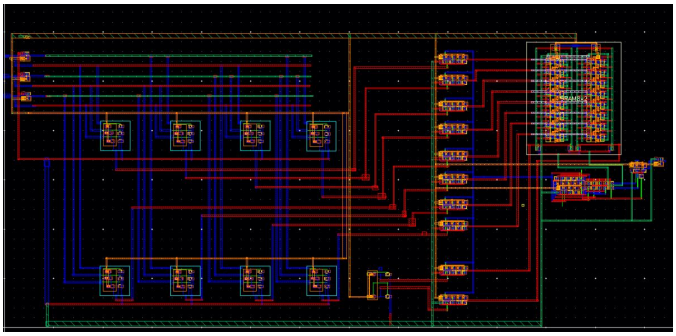

Fig. 8. Layout of Complete Circuit

IV. Results

The parameters that were measured from the design are area, timing of the circuit and the sensitivity of the sense amplifier.Table 1 represents the layout area of the individual blocks and the combined circuit. Table 2 shows the read time, write time and the precharge time for the circuit.

The definition of sensitivity of sense amplifier used in this paper is the minimum voltage difference between BL and BL_bar for which the output of the sense amplifier is 1V.For this design, the minimum voltage difference between BL and BL_bar to get an output of 1V was 0.004V.

Individual Block Name	Layout Area(in um^2)
SRAM Cell	3.29
Row Decoder	1078.62
Column Decoder	7.494
Read/Write Control	24.36
Sense Amplifier	3.437
SRAM Array	109.182
Combined Circuit	1985.3328

TABLE I
Layout Area of Blocks

Operation	Time Taken(in ns)
Precharge	0.22283
Write 0	0.1673
Write 1	3.1498
Read 0	0.4048
Read 1	0.4814

TABLE II
Timing of the Circuit

V. Conclusion

The 8X2 SRAM Array has been designed and implemented using Cadence. The individual blocks were designed and tested first before integrating them to form the array. All the blocks passed the DRC and LVS checks successfully. The timing analysis of the array was also carried out successfully. Data was successfully written to multiple cells of the SRAM arrays. Write time, read time and precharge time were calculated and tabulated. The results were satisfactory, but there is scope for improvement. The design area can be reduced and methods to decrease the write time and read time can be explored. Thus, we could say that the project was an overall success.

VI. Future Scope

Future scope for this project in terms of layout would be to reduce the area of the entire circuit by making optimizations combining the adjacent NMOS/ PMOS structures into the same N/Pwells. Particularly the SRAM cells could be flipped around to combine it in such a way. This would also reduce the number of VDD/GND connections hence eliminating excessive metal lines. Also, buffers could be arranged in parallel to the decoders to minimize the routing to and from the buffers and to the SRAM array. Secondly, in terms of simulation and performance, we could find a better fitting sense amplifier that would provide a better amplification of the signal between BL and BL_bar. Lastly, the use of FinFETs could be considered owing to their property of low leakage current and low power consumption.

VII. Acknowledgment

We are thankful to Dr. Scott Thompson for giving us the opportunity to do this project and the TAs for their guidance. We would also like to thank the University of Florida ECE department for providing the resources needed to complete the project.

REFERENCES

[1] Jan M. Rabaey, Anantha Chandrakasan, Borivoje Nikkolic, Digital Integrated Circuits, Second Edition

[2] Richard C. Jaeger, Introduction to Microelectronic Fabrication

[3] Preeti S Bellerimath and R. M Banakar, Implementation of 16X16 SRAM Memory Array using 180nm Technology, International Journal of Current Engineering and Technology

[4] https://en.wikipedia.org/wiki/Static_randomaccess_memory

[5] Vijay Kumar Enumula, Suhas Gupta, Rajani Manchukond, Nirupama Upadhyay, Design and implementation of 16X8 SRAM in 0.25u SCMOS technology