VLSI Circuits and Technology EEE5322

Design and Implementation of 8X2 SRAM Array in 45nm SCMOS Technology

Team Members

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Under the Guidance of

Dr. Scott Thompson

Yingjie Chen (TA)

Xiaodong Xu(TA)

Description of work for each team member

1) Deepak Harinath Pudukodu Gopalakrishnan

   I was responsible for the designing and implementing the Sense Amplifier. This included designing the schematic, layout and extracting the symbol for this block. I made sure that the design passed the DRC and LVS check. I was also responsible for simulating the SRAM Array and achieving the timing results for the circuit. I also performed checks on read write circuitry, making sure that the correct operation was carried out and the performance was at par with the expected outputs. I have made contribution towards completion of the report.

2) Medini J Aradhya

   I was responsible for designing the schematic and Layout of the SRAM array, the pre-charge circuitry, read-write circuit (layout) and buffer circuit. I have successfully tested the individual blocks both for functionality and Layout DRC and LVS checks. Along with this I have Integrated the Layout of the entire circuit and optimized area of cell by minimizing individual components to a certain extent. I have verified its successful DRC and LVS runs after integration of all components. I have made contribution towards completion of the report.

3) Shang Shi

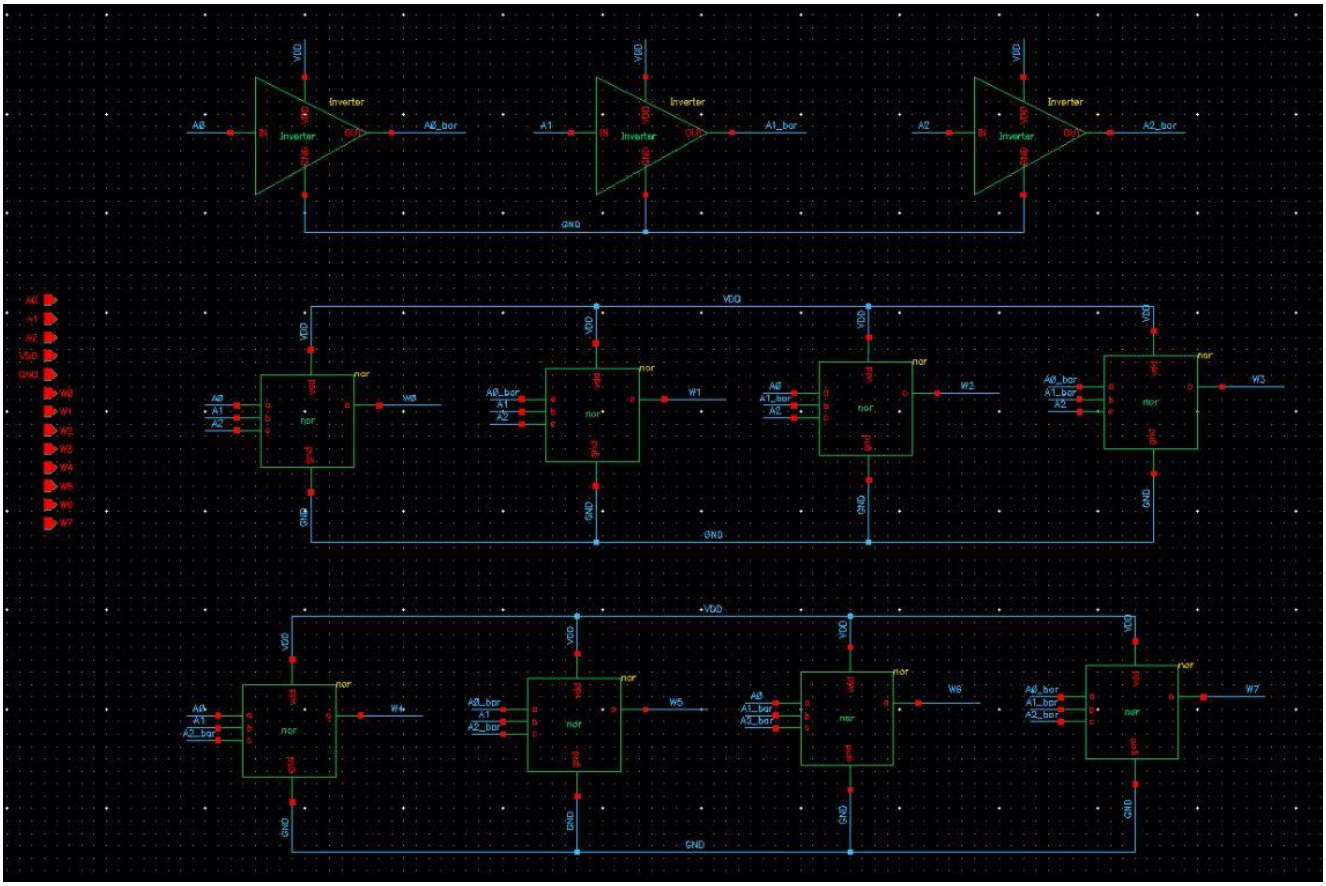
   I was responsible for designing and implementing the schematic, layout and extracting symbol for the 3:8 row decoder as well as the 1:2 column decoder. I have tested the functionality of each of the components within the decoders (NOR gate, Amplifier). I was also responsible for the integration of the schematic and provided assistance for layout integration.

4) Neel Kanjaria

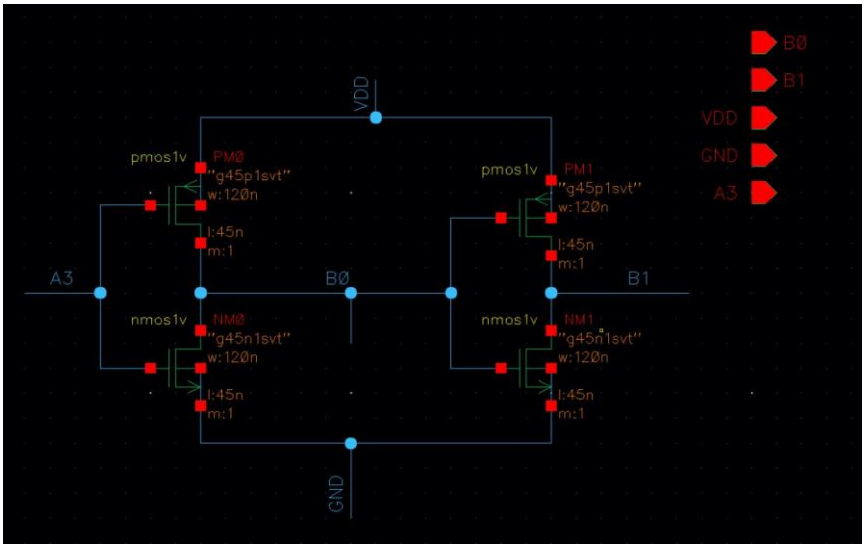
   I was responsible for designing and testing the schematic for Read-Write Circuit. I also aided with the creation of the layout for the same and ensured its correct functionality. I was also responsible for making the reports.

SCHEMATIC

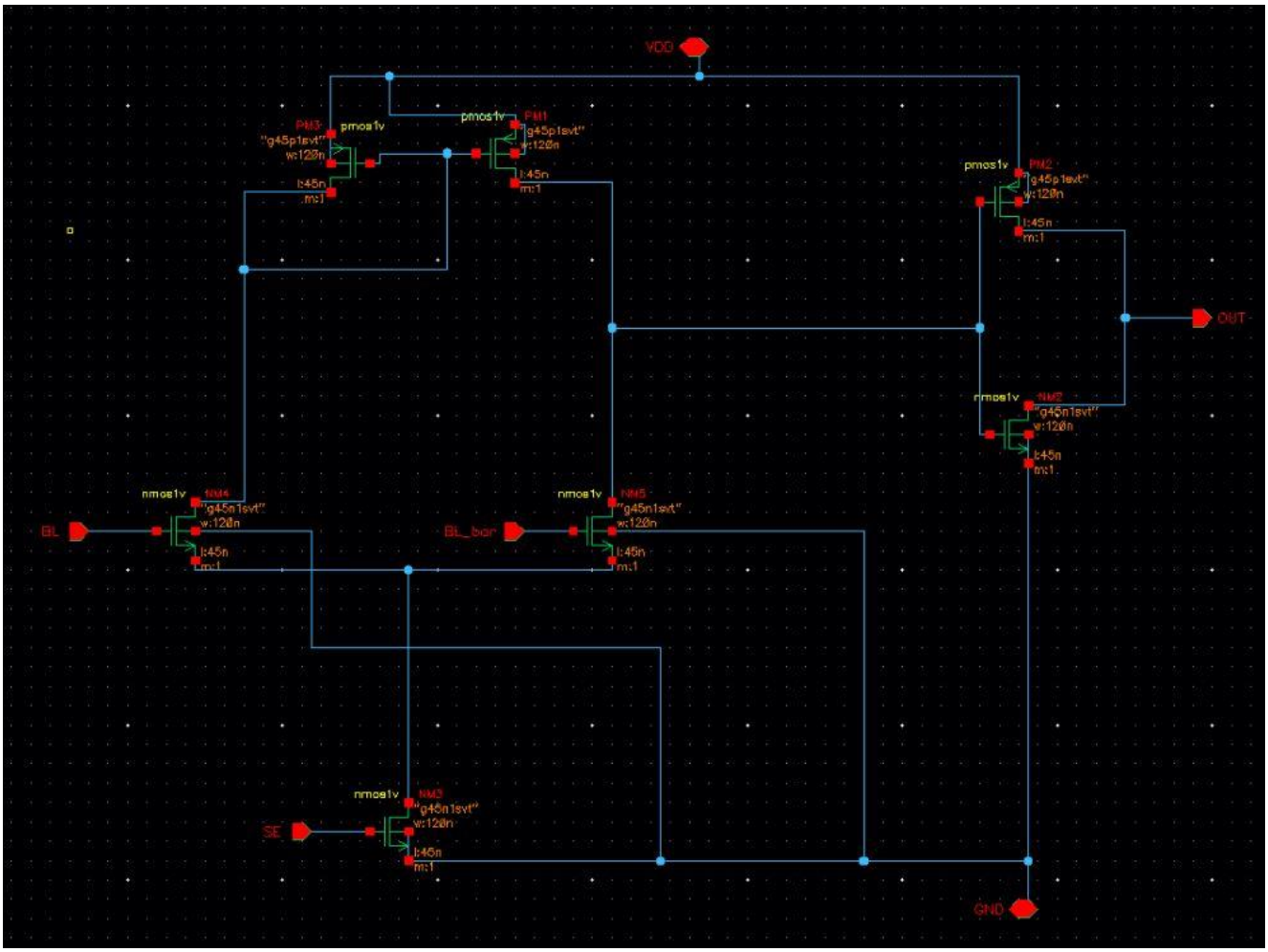
Row Decoder



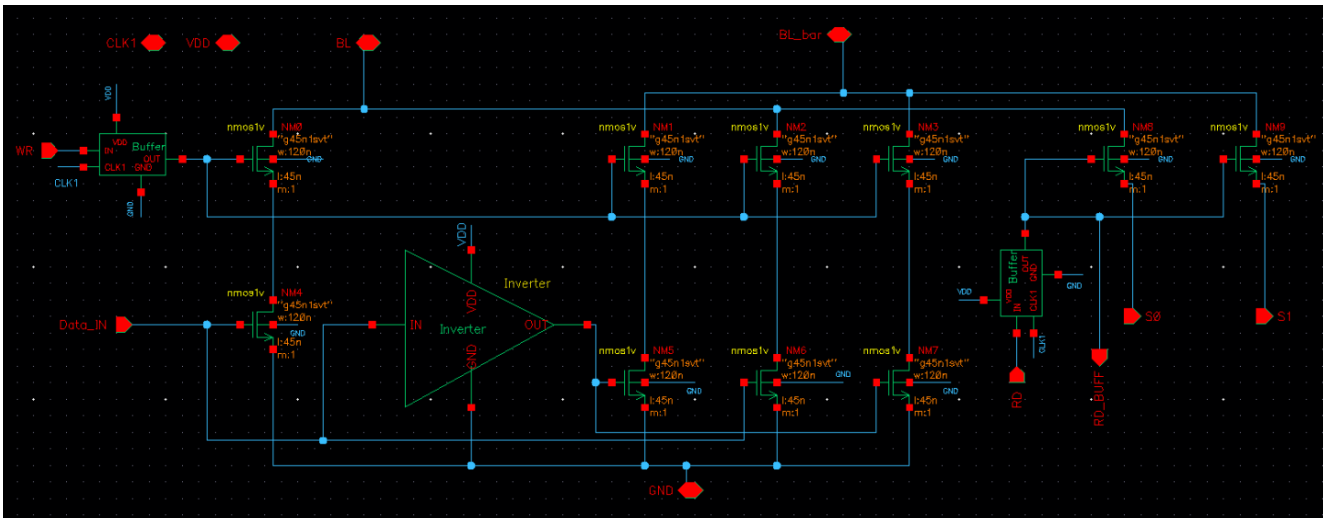
Column Decoder



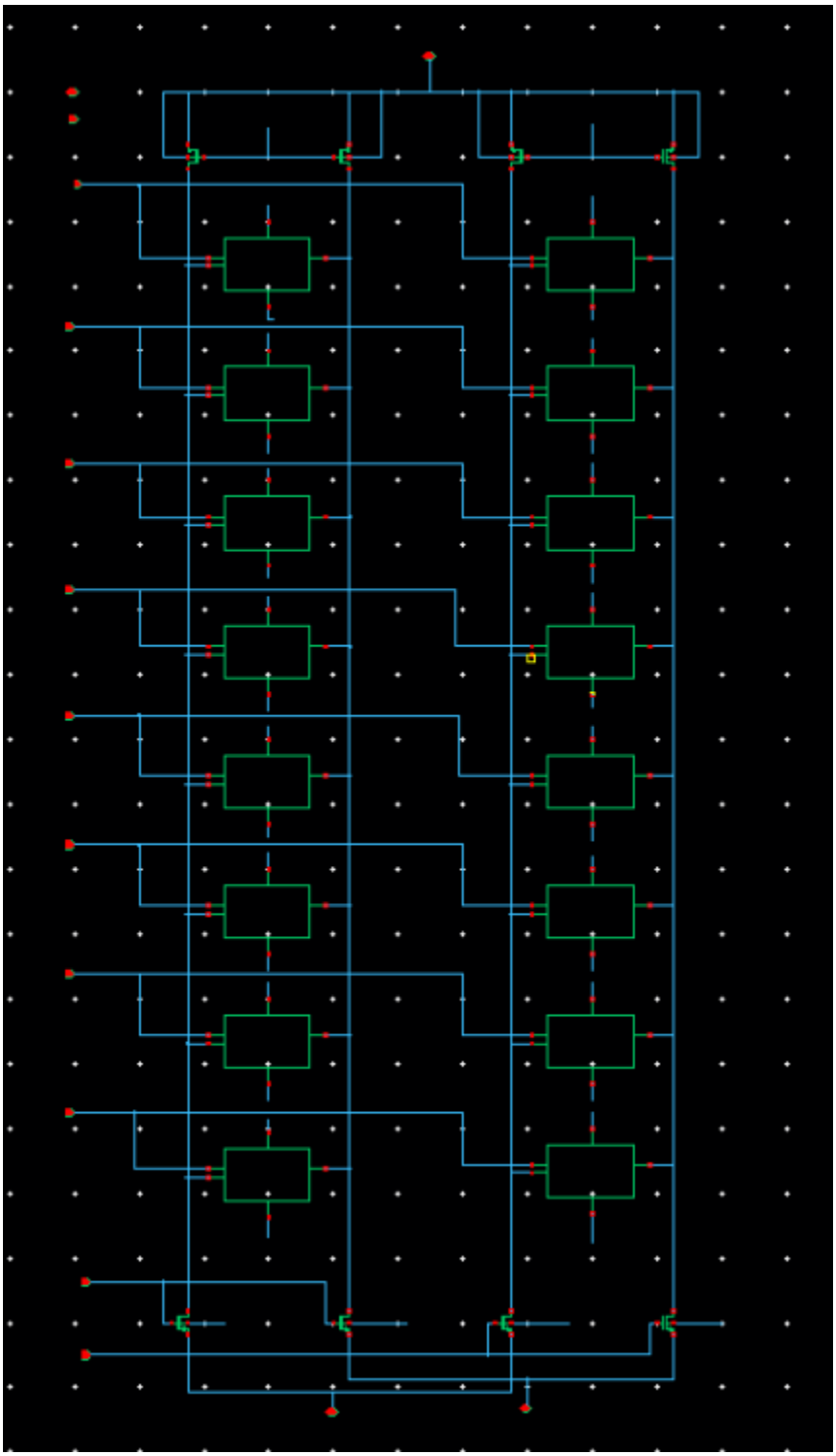
Sense Amplifier



Read Write Circuit

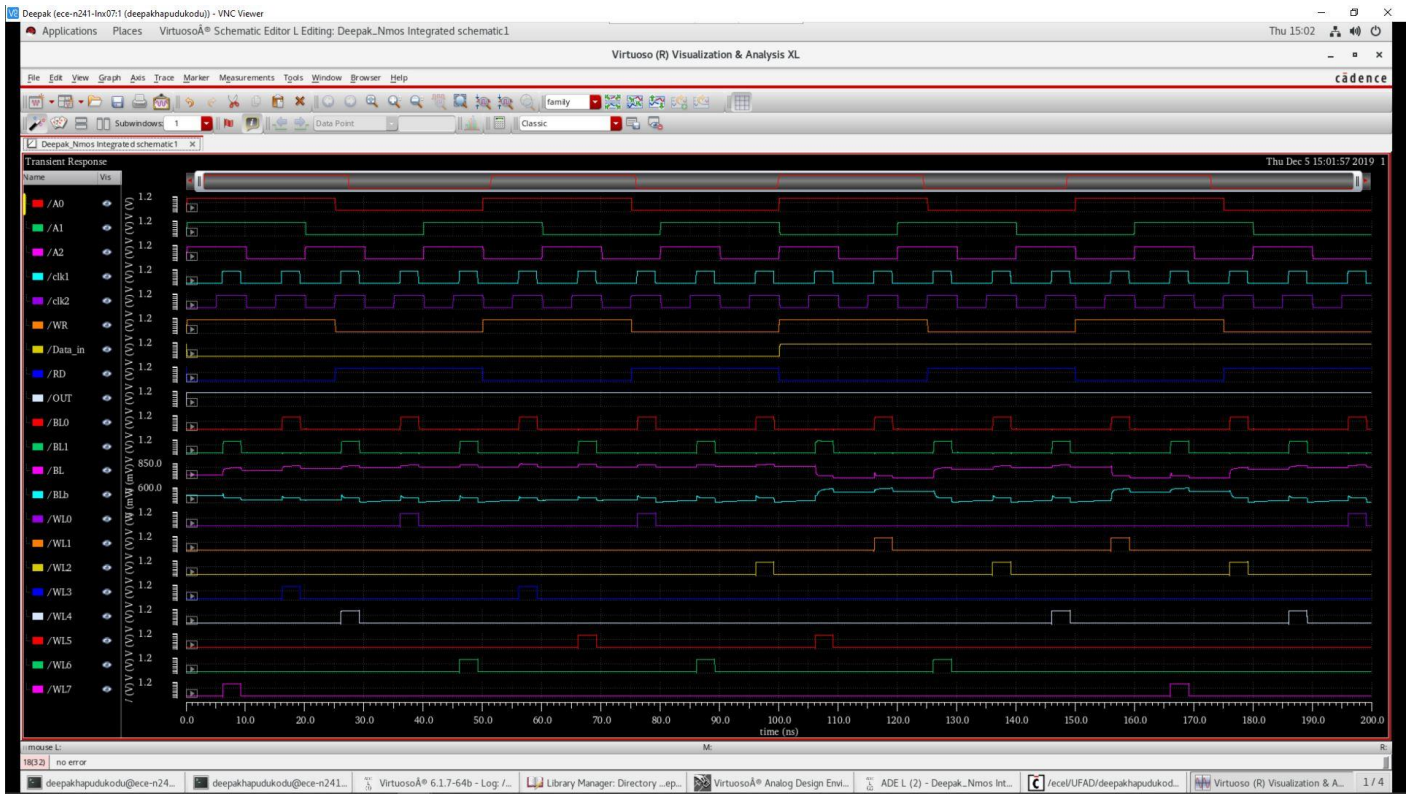


SRAM Array



Simulation Setup

- The simulations were carried out after testing the individual blocks.
- Clk 1 and Clk 2 are non-overlapping clocks with a pulse width of 3ns and 5ns respectively. The period of both the clocks was set to 10ns.
- Clk1 is used to control the buffer which is an AND gate and the timing of the circuit. CLK2 is used to precharge the bitline and bitline_bar.
- The data_in signal has a pulse width of 100ns and period of 200ns.
- The Read and write signals have a pulse width of 25ns and period of 50ns. They were opposite to each other in order to avoid both signals being high at the same time.
- A2, A1 and A0 are the wordline decoders and A3 is the column decoder. A2 corresponds to the MSB and has a pulse width of 10ns and period of 20ns. A1 has pulse width of 20ns and period of 40ns. A0 has pulse width of 25ns and period of 50ns. A3 has pulse width of 10ns and period of 20ns.
- The following figure shows the working of the full 8x2 SRAM cell with writing to and reading from multiple SRAM cells.



TIMING RESULTS

Precharge Timing:

Precharge time is the time taken by the bitlines to rise from 0 to 1.1V when the CLK2 is driven LOW. The precharge circuit is made up of 4 PMOS transistors, hence when clk2 is driven LOW, then the bitlines are connected to VDD which increases the voltage.

In this project, the precharge time has been calculated when the bitline voltage rises from 0V to 1.1V. The below shown figure is shows the voltages of the bitlines rising from 0 to 1.1V after the CLK 2 is driven LOW.

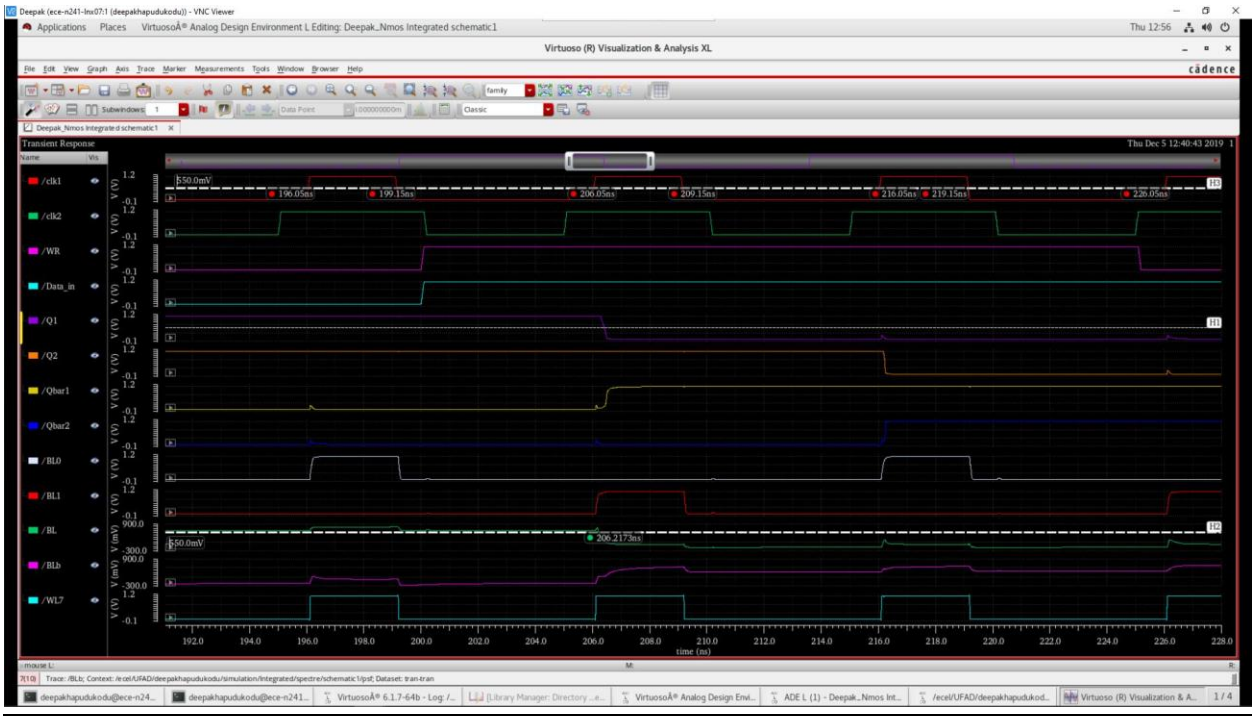
Precharge Time=20.41372-20.20.19089=<u>0.22283ns</u>

Write Simulation:

In order to write into a circuit, the Write signal must be HIGH and the CLK 1 should be HIGH in order to access the world lines. When the Data_In is 1, then we are actually writing a 0 to the SRAM cell and vice versa is also true.

For testing purposes, WL7 was chosen and in the following graph results, data has been written into SRAM (8,1) and SRAM (8,2). In this design, it should be noted that when BL1 is high, the first column of SRAM cells is selected and when BL0 is high, the second column of SRAM cells are selected.

Write '0':

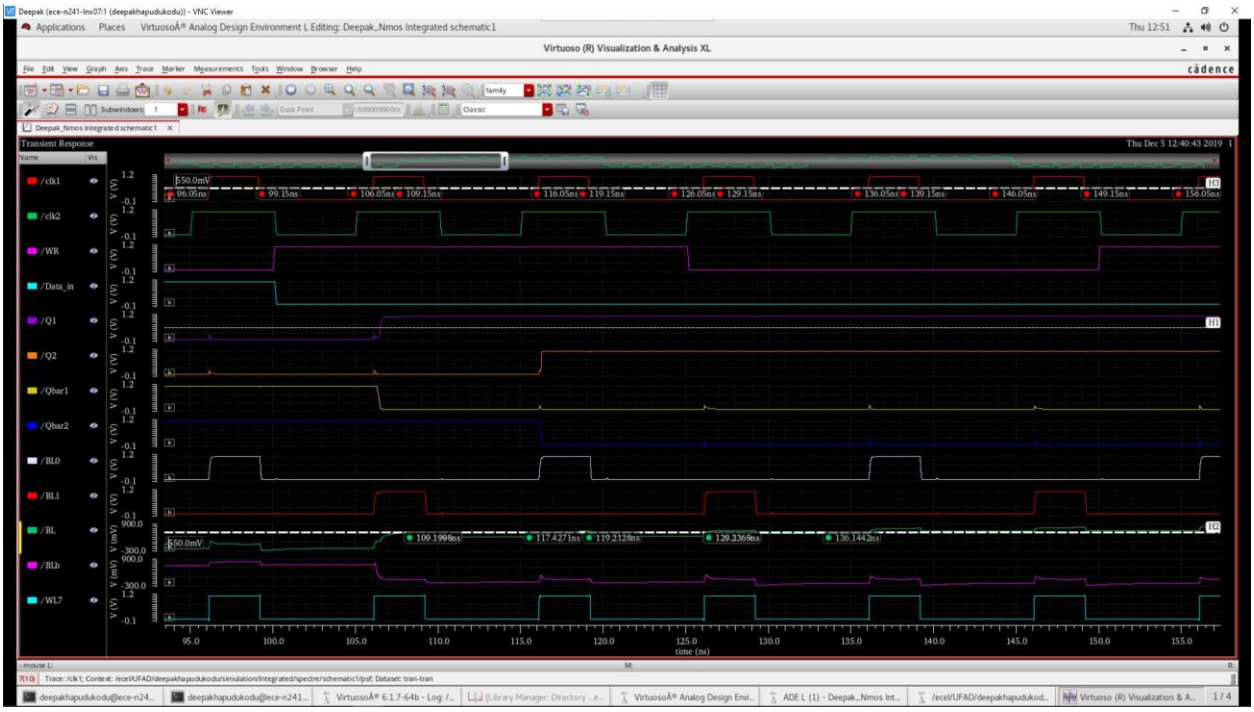


As mentioned above, "1" is written when the data_in value is "0". It can be seen from the above figure that when Write signal, CLK 1 and BL1 are high, "0" is written onto SRAM (8,1) and this can be confirmed by looking at the voltage changes in Q1 and Q1_bar. Similarly, when Write signal, CLK 1 and BL0 are high, "0" is written onto SRAM (8,2).

The write time has been calculated by subtracting the time for which the clk1 value is at 550mV from the time for which BL is at 550mV.

The calculated write time for '0' is **0.1673ns.**

Write ‘1’



Similar to write ‘0’, “1” is written when write signal and CLK1 are HIGH and data_in is “0”. From the above figure, it can be seen that when write signal, clk1 and BL1 are high, “1” is written onto SRAM (8,1) and this can be confirmed by looking at the voltage changes in Q1 and Q1_bar. Similarly, when BL0 is HIGH, “1” is written onto SRAM (8,2).

The write time for “1” is <u>3.1498ns.</u>

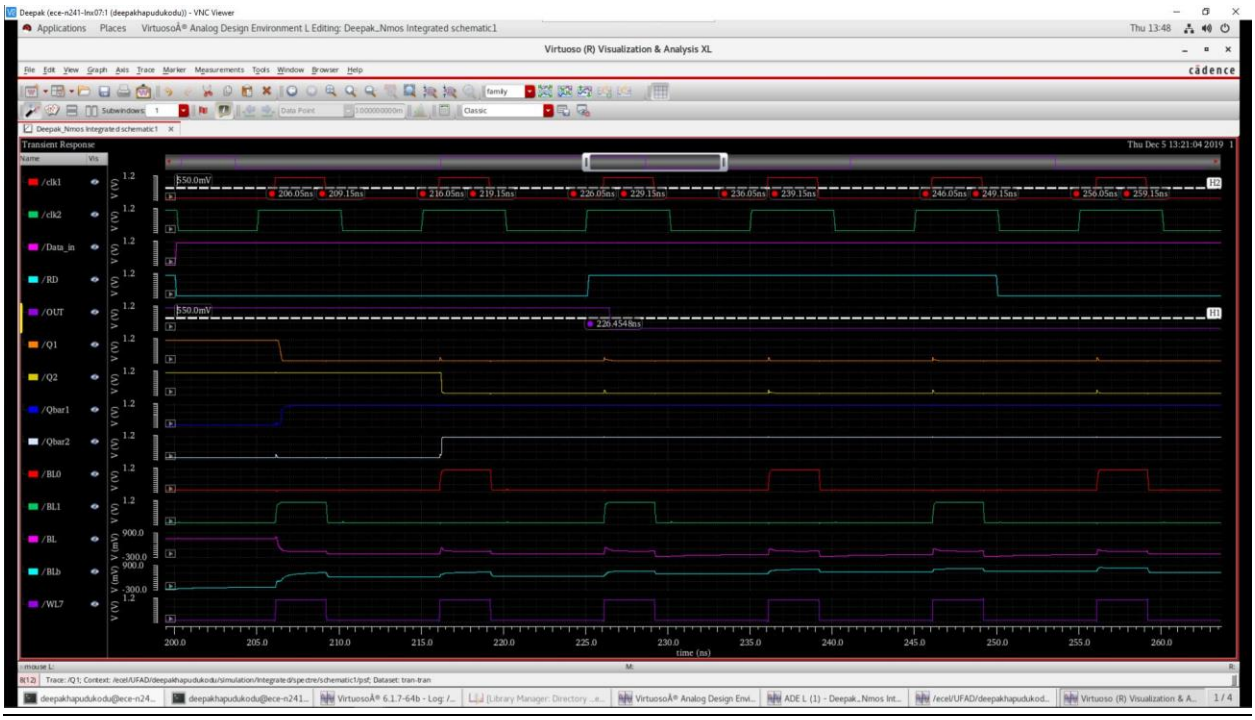
It should be noted that writing “1” takes longer than writing ”0”.

Read Simulation:

In order to read from a circuit, the Read signal must be HIGH and the clk1 should be HIGH in order to access the world lines. The output of the sense amplifier gives us the value stored in the SRAM cell that we are reading from.

For testing purposes, WL7 was chosen and in the following graph results, data has been read from SRAM (8,1) and SRAM (8,2). In this design, it should be noted that when BL1 is high, the first column of SRAM cells is selected and when BL0 is high, the second column of SRAM cells are selected.

Read "0":

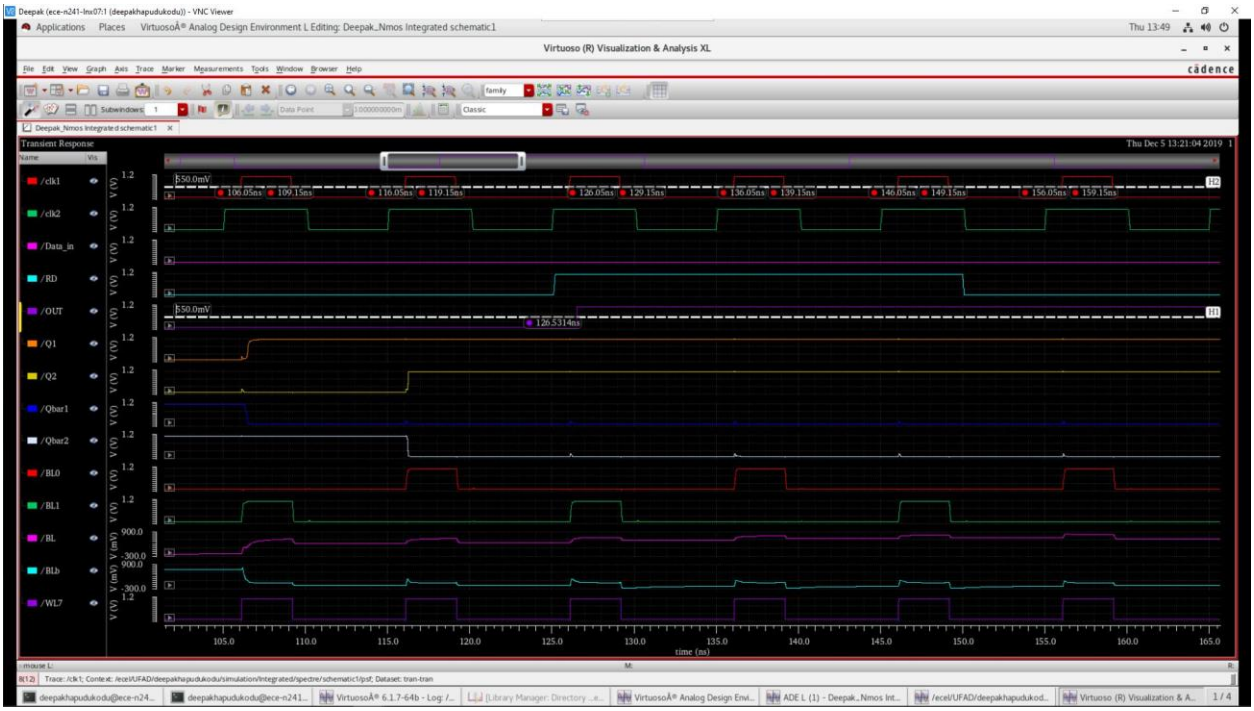


From the above figure, it can be seen that when Read signal, CLK 1 and BL1 are high, "0" is read from SRAM (8,1). Similarly, when Read signal, CLK 1 and BL0 are high, "0" is read from SRAM (8,2). The read operation from SRAM (8,2) cannot be seen properly as the OUT value is already "0" and thus no change in the voltage.

The read time has been calculated by subtracting the time for which the clk1 value is at 550mV from the time for which OUT is at 550mV.

The calculated read time for '0' is **0.4048ns.**

Read “1”



From the above figure, it can be seen that when Read signal, CLK 1 and BL1 are high, “1” is read from SRAM (8,1). Similarly, when Read signal, CLK 1 and BL0 are high, “1” is read from SRAM (8,2). The read operation from SRAM (8,2) cannot be seen properly as the OUT value is already “1” and thus no change in the voltage.

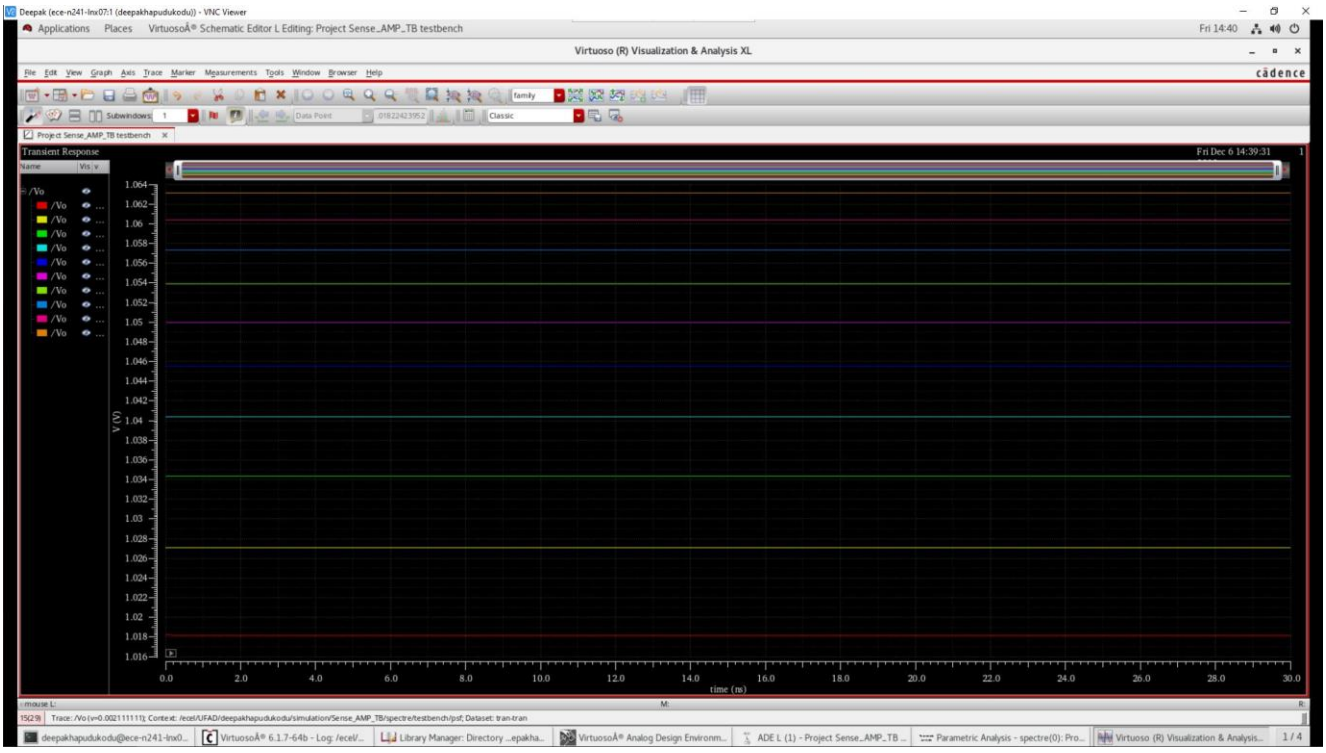
The calculated read time for ‘1’ is <u>0.4814ns.</u>

It should be noted that the read time for both 0 and 1 are similar unlike the write times.

Other Simulations and Tests:

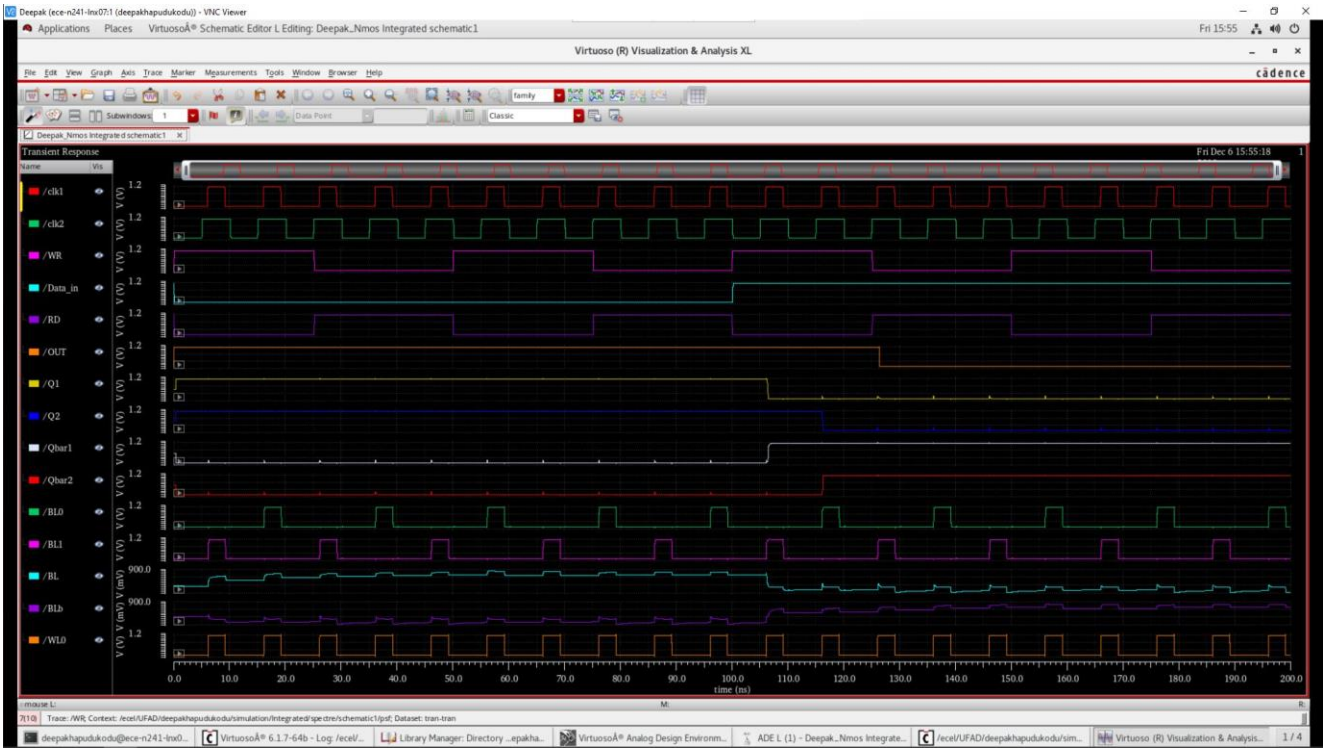
Sensitivity of Sense Amplifier

The sensitivity of the sense amplifier was tested in order to get an idea about its performance. The sensitivity definition that has been used for this design is the minimum voltage difference between BL and BL_bar for which the output of the sense amplifier is 1V. The calculated sensitivity was 0.004V. This can be seen in the below picture.



Multiple Cells

The following figure has been added just to show that the write and read operations are performed successfully for multiple cells. In the below figure, write and read operations are performed successfully for SRAM (1,1) and SRAM (1,2) cells.



NOTE:

The testing and timing results of the combined circuit were carried out after the DRC and LVS of the individual blocks had passed successfully. When trying to simulate the combined circuit, we faced a problem where the circuit was able to read/write only the first data_in. After consulting with the TAs, we changed the width of the NMOS switches in the column decoder and first row of RD/WR from 120nm to 4um. We tried to change the respective widths on the layouts as well but couldn't pass the LVS when we did so. Hence, the Layout files of precharge and RD/WR circuit in the next section have NMOS transistors with 45nm.

Layout Considerations

These are the basic rules for 45nm process taken into consideration for designing layouts.

1) Poly Rules:

- Gate width = 0.045 µm
- Poly extension from the active = 0.12 µm.

2) Active Width:

- Active width = 0.12 µm
- Min. Active Area to Implant enclosure = 0.07 µm
- Min. Active Area to N-Well = 0.16 µm

3) Metal 1 Rules:

- Minimum width =0.06 µm
- Min. Metal 1 to Mental 1 = 0.07 µm
- Min. Metal 1 to Metal 1 spacing if width of Metal 1 > 0.1 = 0.115 µm
- Min. Metal 1 to Contact enclosure on two opposite sides of the contact =0.03 µm

4) Metal 2 Rules:

- Minimum width =0.08 µm
- Min. Metal 2 to Mental 2 = 0.07 µm
- Min. Metal 2 to Metal 2 spacing if width of Metal 2 > 0.1 = 0.12 µm

5) Metal 3 Rules:

- Minimum width =0.08 µm
- Min. Metal 3 to Mental 3 = 0.07 µm
- Min. Metal 3 to Metal 3 spacing if width of Metal 3 > 0.1 = 0.12 µm

1) Metal 4 Rules:
   - Minimum width =0.08 µm
   - Min. Metal 4 to Mental 4 = 0.215 µm
2) Contact Rules:
   - Contact Width/Length = 0.06 µm
   - Minimum Poly to Contact enclosure = 0.03 µm

3) Metal 1 to Poly Via Rules:
    - Metal 1 to Poly Via Width = 0.07
    - Min. Metal 1 to Via 1 enclosure on both sides = 0.03 µm
4) Via 1 Rules:
    - Via 1 Width = 0.07
    - Min. Metal 1 to Via 1 enclosure on both sides = 0.03 µm
5) Via 2 Rules:
    - Via 2 Width = 0.07
    - Min. Metal 2 to Via 2 enclosure on both sides = 0.03 µm
6) Via 3 Rules:
    - Via 3 Width = 0.07
    - Min. Metal 3 to Via 3 enclosure on both sides = 0.03 µm

Design Practices

- We tried to ensure to the best of our abilities that poly, M3 & M4 run horizontal (one direction). While connections were made with M1 & M2 unifying the separate blocks of the overall circuit.
- We used a wide cell SRAM type and tried to make it as compact as possible.
- Thus, the SRAM array was developed keeping minimum area in mind while achieving zero DRC and LVS errors.
- The SRAM array was developed from 1x1 to 2x1 to 4x1 to 8x1 to finally 8x2 while checking for errors and connectivity issues at each stage to ease the debugging at the last stage.
- Similarly, Sense Amplifier, Read-write circuit and buffer circuits all have been designed to the minimum layout requirements individually.
- While connecting all the layouts, we have connected every block individually to the array block first, checked for the DRC and LVS with the modified schematic and when that worked, we moved on adding other blocks till completion. This helped in debugging.
- Symbols were created for repetitive blocks like Inverter, AND gate for the Buffer and the buffer itself. These were then called in larger schematics for a more concise schematic.

- Similarly, the layouts of these symbols were used as instances in the final layout that allowed us to easily connect and debug the overall layout. (keeping in mind the right naming of every instance)

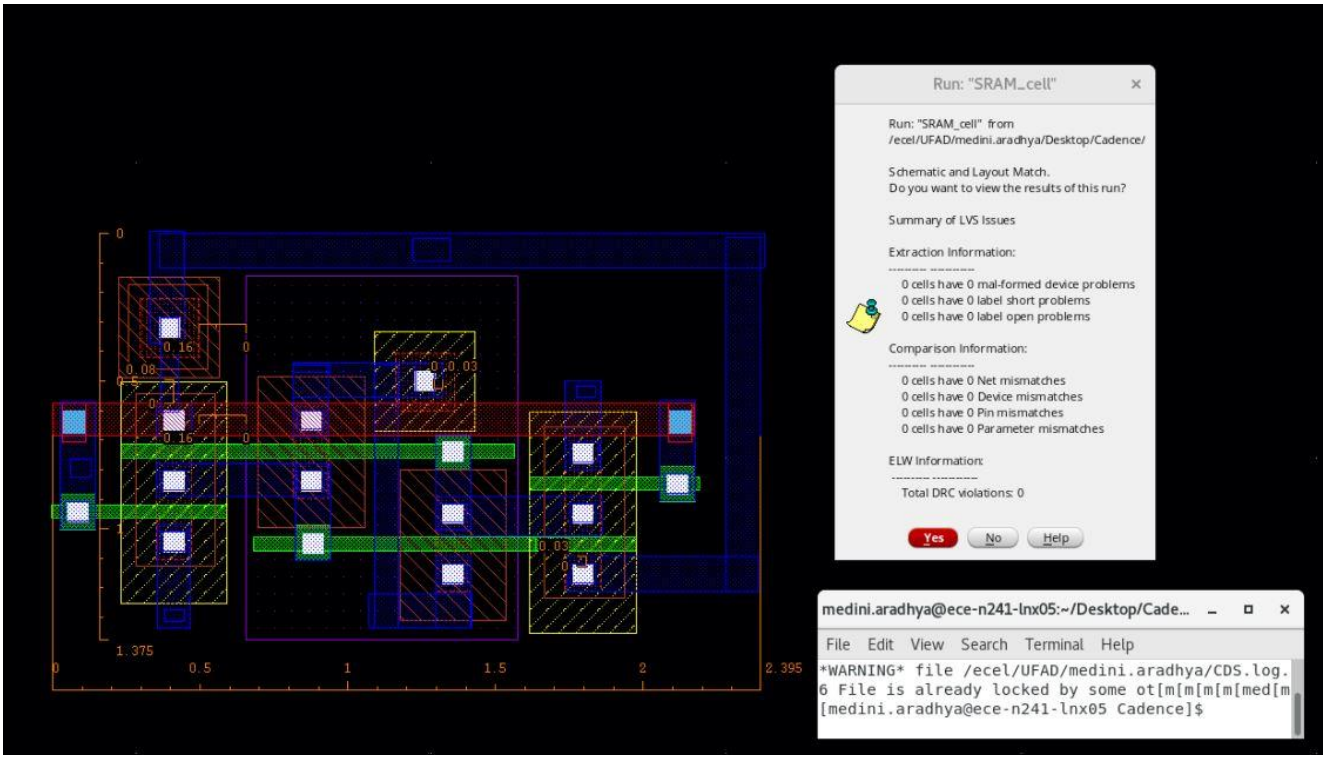
Issues

- Designing Minimum layout lead to high number of DRC errors due to 45nm design process requirements. We used Assura tool to debug the errors making note of the minimum distance required between components.
- Having designed symbols for NOR, Inverter and Buffer, the instance called in the main layout file could not have been modified. Hence increased the area of top-level connections. (fixed symbol→ instance size in overall layout)
- Designing the 8*2 SRAM array was particularly time consuming due to the 4 metal layers used. Using the Layout of the instance (Layout of SRAM Cell as an instance in SRAM_ARRAY) created a problem in terms of area of the circuit as it occupied a lot more area than necessary. So, we individually added the layout for each SRAM cell instead of the instance. During LVS we faced errors that were debugged using Assura tools.
- Connectivity of each component was checked before running the tests.
- Adding pins to the layouts needed to be done by going to create→pin and selecting manual and the shape as rectangle based on the material, we are placing the pin on. Otherwise Assura would not recognize the pin.
- Pin names mismatch was observed since VDD was used in some layouts and Vdd in others, this was made uniform to remove the error.
- Connecting the decoder to the buffers and from there to the wordlines was an arduous task and not minimum layout. We have tried to minimize area as much as possible.
- Metal spacings for different metal widths were different and so while running DRC we got this error.
- Number of contacts varied for thickness of metal. Higher thickness metals needed 2 contacts per connection.
- Vias were placed exactly overlapping each other to obtain a minimum metal area that needs to be laid out over the connection point.

The rest were all minor issues regarding few missing connections, shorts, pin mismatch, minimum spacing etc.

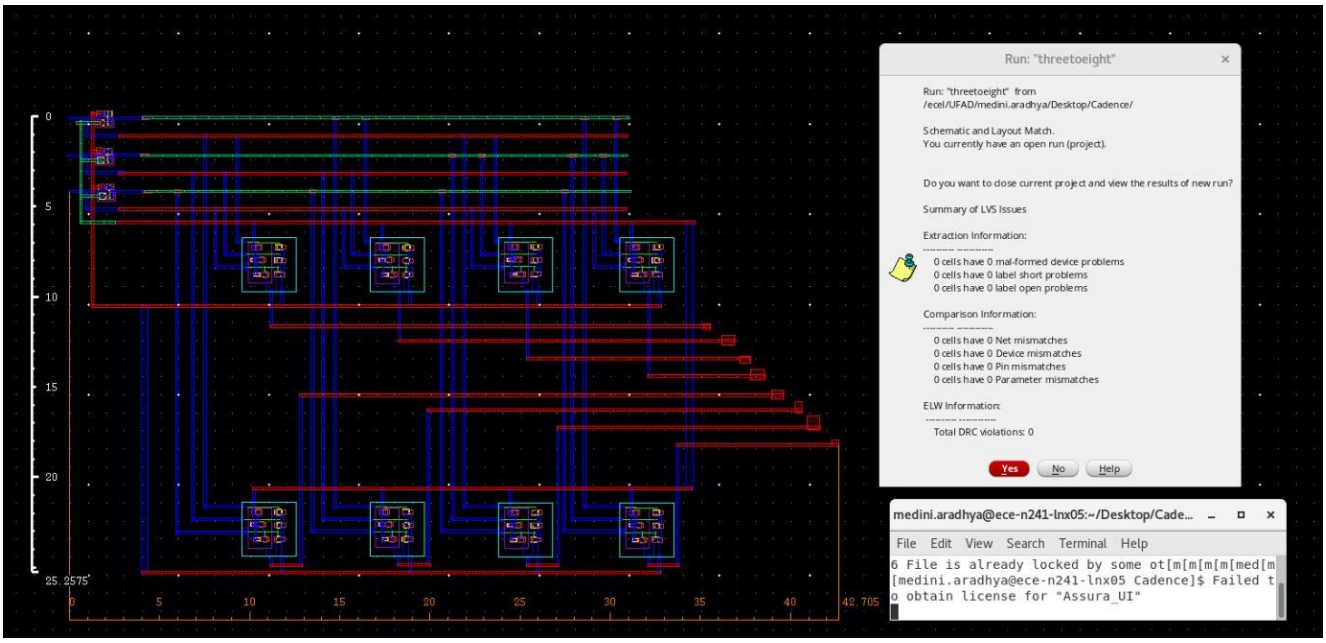
LAYOUT

SRAM cell



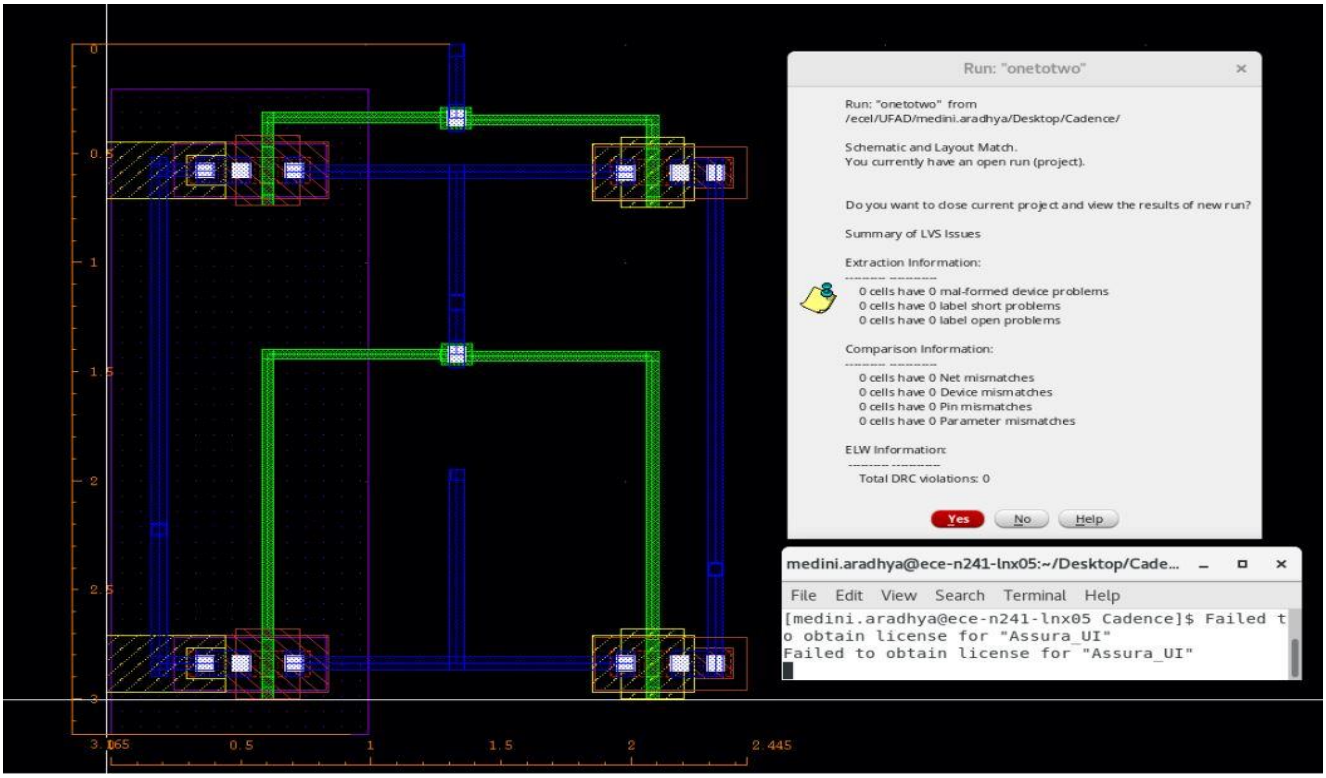
Area of SRAM Cell=2.395*1.375=**3.29um^2**

Row Decoder



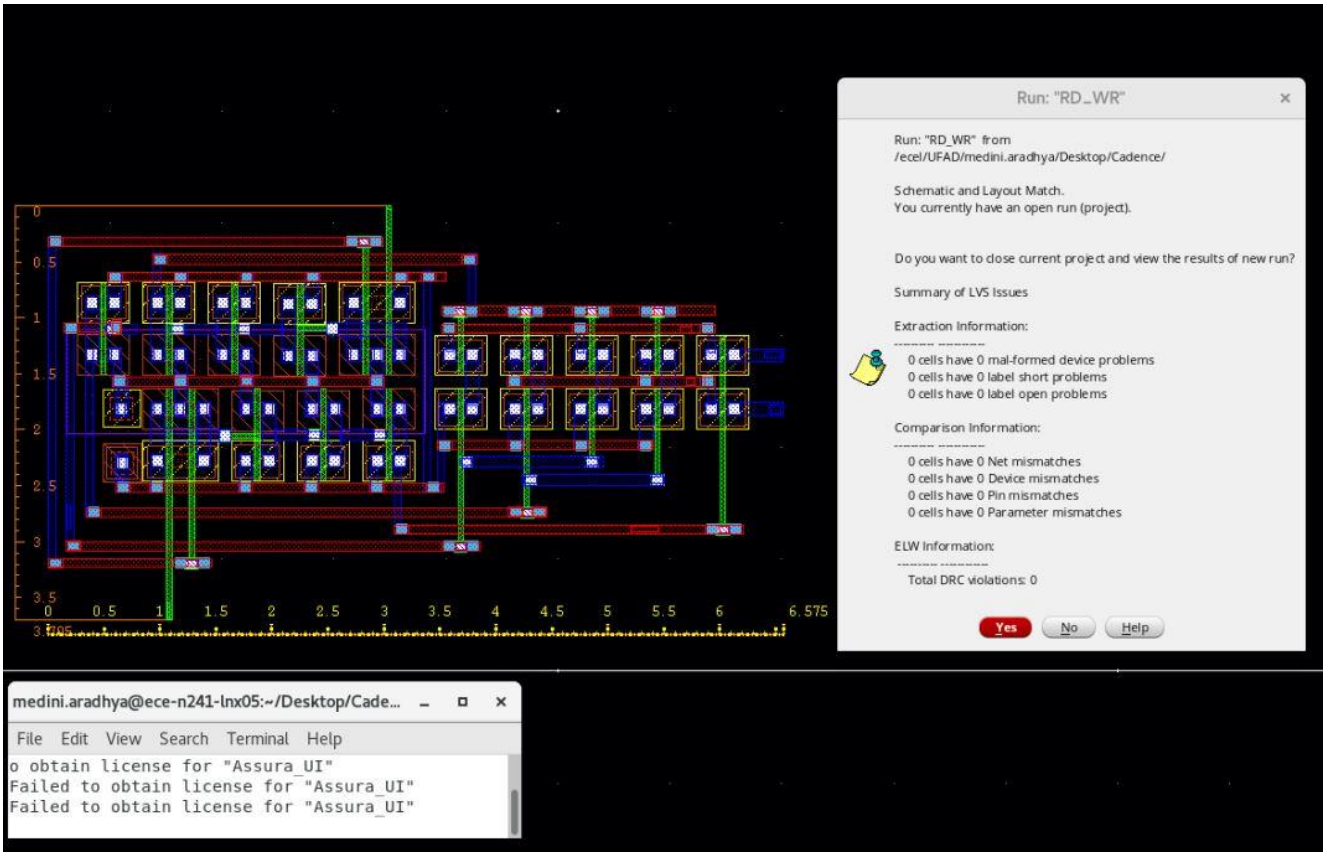
Area of Row Decoder=25.2575*42.705=<u>1078.62um^2</u>

Column Decoder



Area of Column Decoder=2.445*3.065=<u>7.494um^2</u>

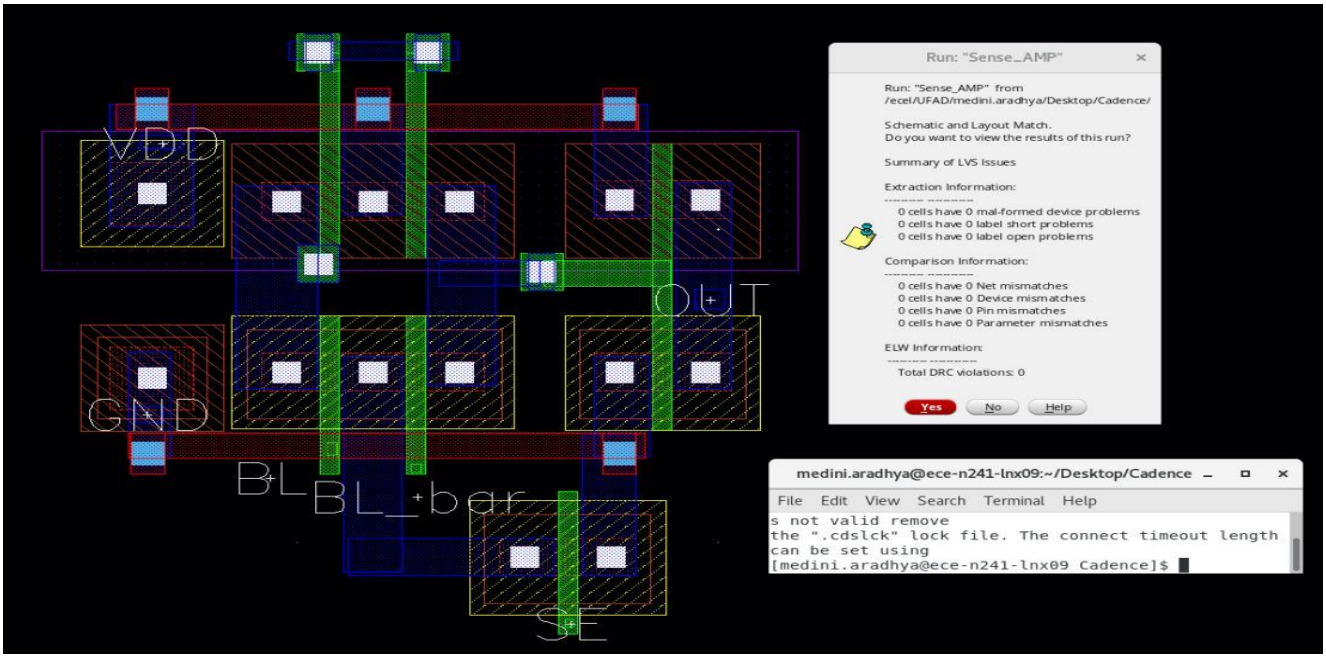
Read / Write Control Circuit



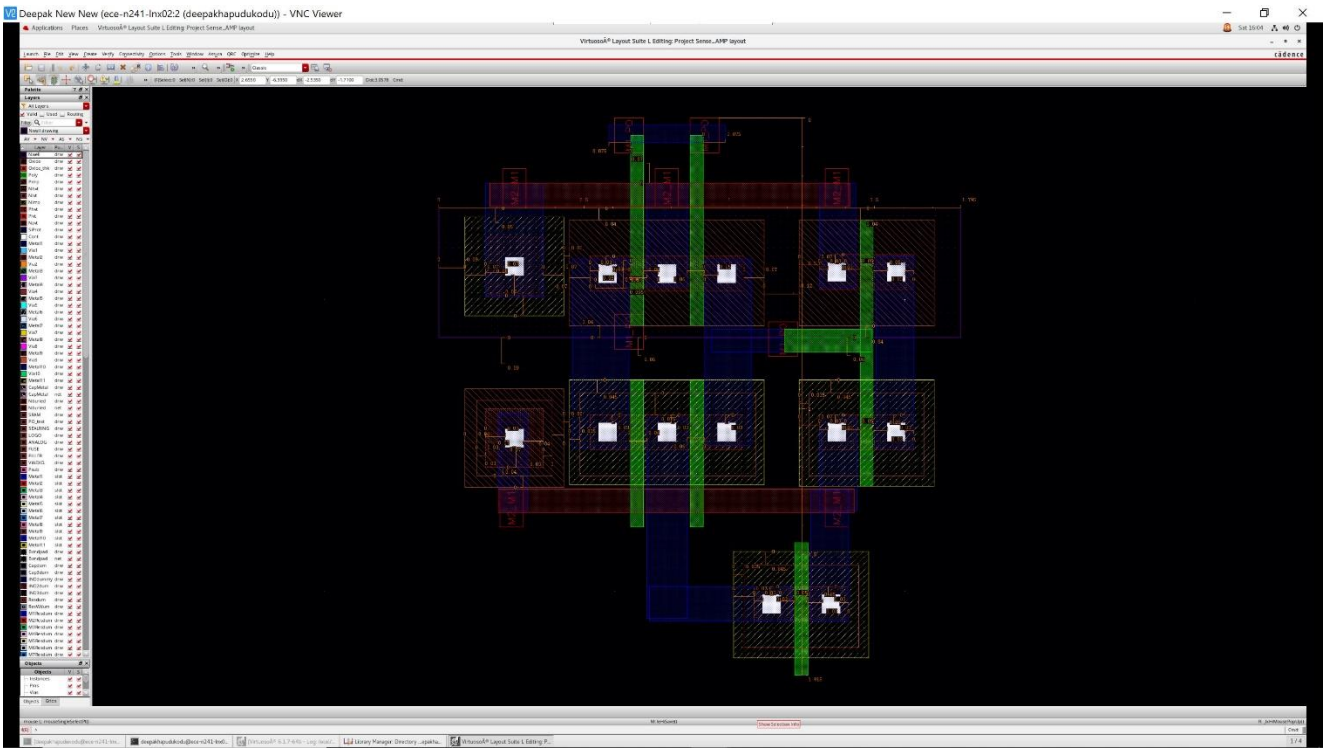
Area of Read-Write Circuit=3.705*6.575=<u>24.36um^2</u>

Sense Amplifier

DRC & LVS

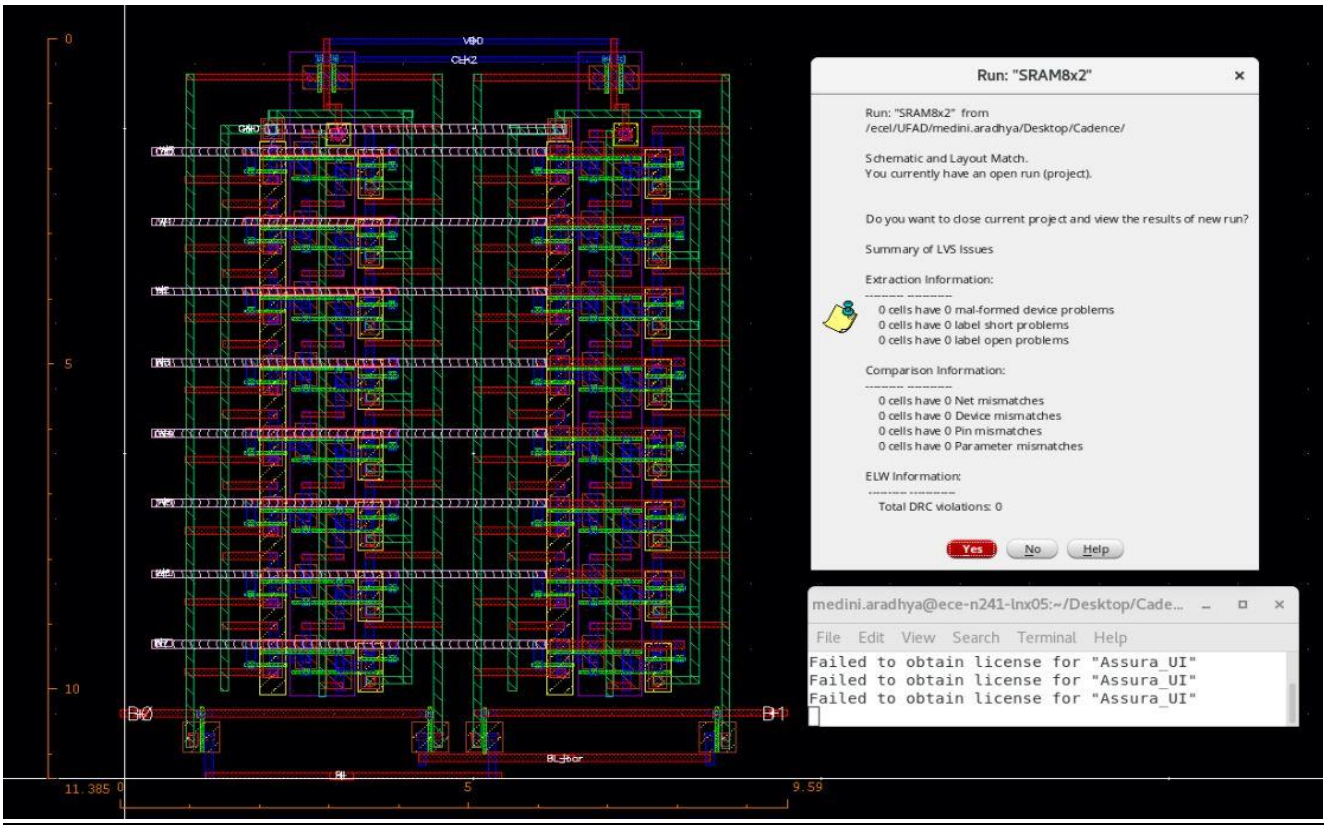


Dimensions



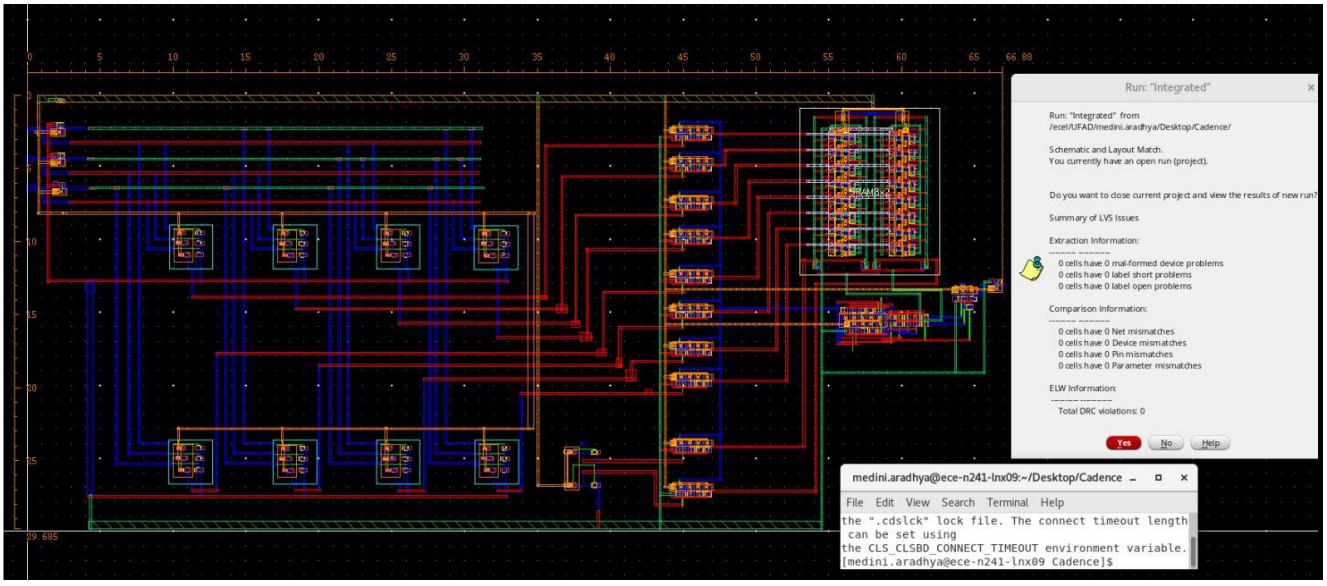
Area of Sense Amp=1.795*1.915=**3.437um^2**

SRAM Array



Area of SRAM Array=9.59*11.385=<u>109.182um^2</u>

Combined Circuit



Area of combined Circuit=66.88*29.685=<u>1985.3328um^2</u>

Conclusion

The 8X2 SRAM Array has been designed and implemented using Cadence. The individual blocks were designed and tested first before integrating them to form the array. All the blocks passed the DRC and LVS checks successfully. The timing analysis of the array was also carried out successfully. Data was successfully written to multiple cells of the SRAM arrays. Write time, read time and precharge time were calculated and tabulated. The results were satisfactory, but there is scope for improvement. The design area can be reduced and methods to decrease the write time and read time can be explored. Thus, we could say that the project was an overall success.

The project was a great opportunity to design a SRAM array. We learnt a lot during the course of designing and testing the circuit. The timing part of the SRAM array helped us to learn about its importance and achieving the results through the industry standard tool Cadence helps in bridging the gap. We would like to thank Dr. Scott Thompson for giving us this opportunity. We would like to thank the TAs Yingjie Chen and Xiaodong Xu for the guidance that they provided for the completion of the project.