1. Description

1.1. Project

Project Name	opis_zalozen
Board Name	STM32L476G-DISCO
Generated with:	STM32CubeMX 6.5.0
Date	04/02/2022

1.2. MCU

MCU Series	STM32L4
MCU Line	STM32L4x6
MCU name	STM32L476VGTx
MCU Package	LQFP100
MCU Pin number	100

## 1.3. Core(s) information

Core(s)	Arm Cortex-M4

2. Pinout Configuration
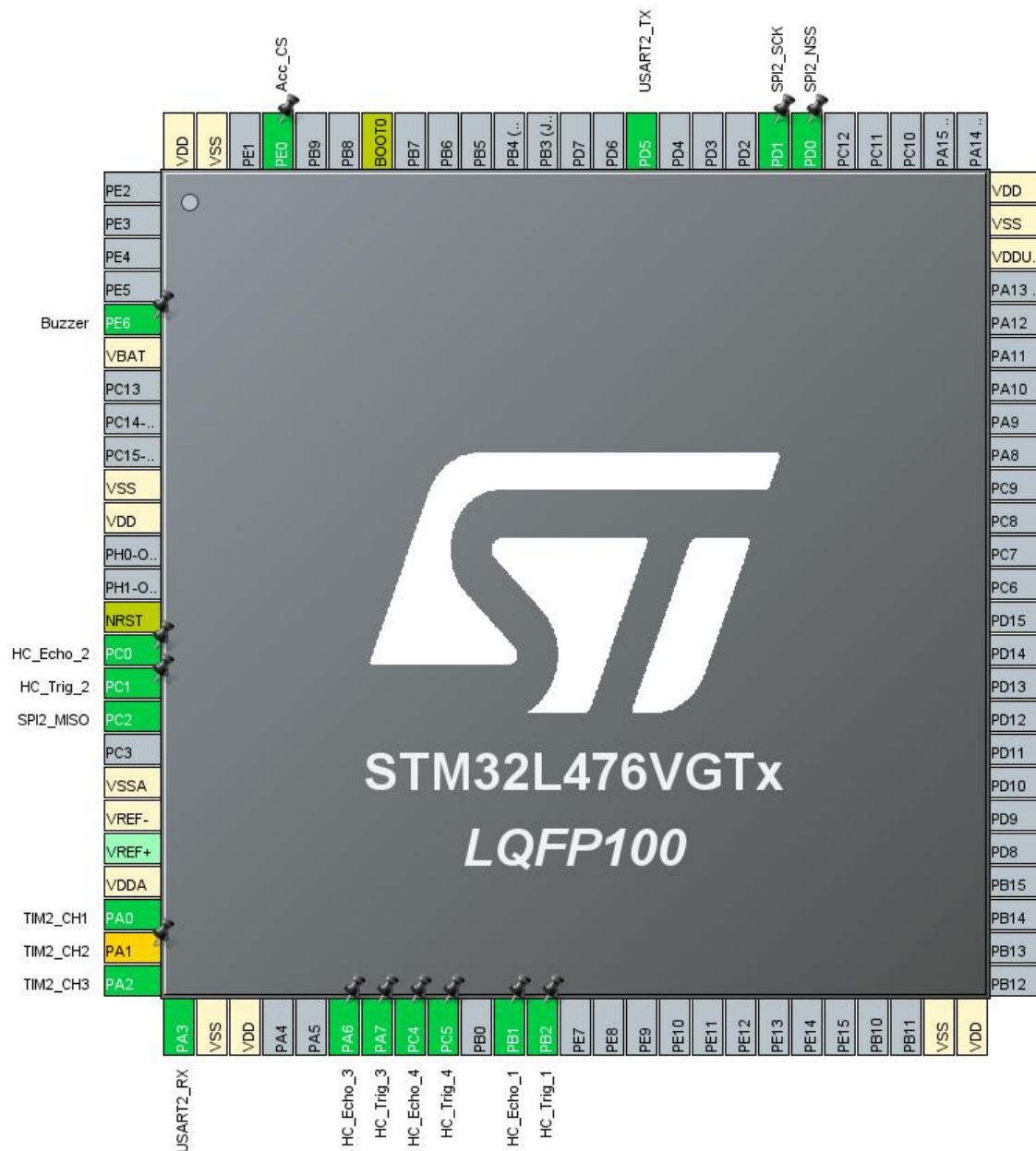
3. Pins Configuration

Pin Number LQFP100	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
5	PE6 *	I/O	GPIO_Output	Buzzer
6	VBAT	Power		
10	VSS	Power		
11	VDD	Power		
14	NRST	Reset		
15	PC0	I/O	GPIO_EXTI0	HC_Echo_2
16	PC1 *	I/O	GPIO_Output	HC_Trig_2
17	PC2	I/O	SPI2_MISO	
19	VSSA	Power		
20	VREF-	Power		
22	VDDA	Power		
23	PA0	I/O	TIM2_CH1	
24	PA1 **	I/O	TIM2_CH2	
25	PA2	I/O	TIM2_CH3	
26	PA3	I/O	USART2_RX	
27	VSS	Power		
28	VDD	Power		
31	PA6	I/O	GPIO_EXTI6	HC_Echo_3
32	PA7 *	I/O	GPIO_Output	HC_Trig_3
33	PC4	I/O	GPIO_EXTI4	HC_Echo_4
34	PC5	I/O	GPIO_EXTI5	HC_Trig_4
36	PB1	I/O	GPIO_EXTI1	HC_Echo_1
37	PB2 *	I/O	GPIO_Output	HC_Trig_1
49	VSS	Power		
50	VDD	Power		
73	VDDUSB	Power		
74	VSS	Power		
75	VDD	Power		
81	PD0	I/O	SPI2_NSS	
82	PD1	I/O	SPI2_SCK	
86	PD5	I/O	USART2_TX	
94	BOOT0	Boot		
97	PE0 *	I/O	GPIO_Output	Acc_CS
99	VSS	Power		
100	VDD	Power		

 * The pin is affected with an I/O function

** The pin is affected with a peripheral function but no peripheral mode is activated

4. Clock Tree Configuration
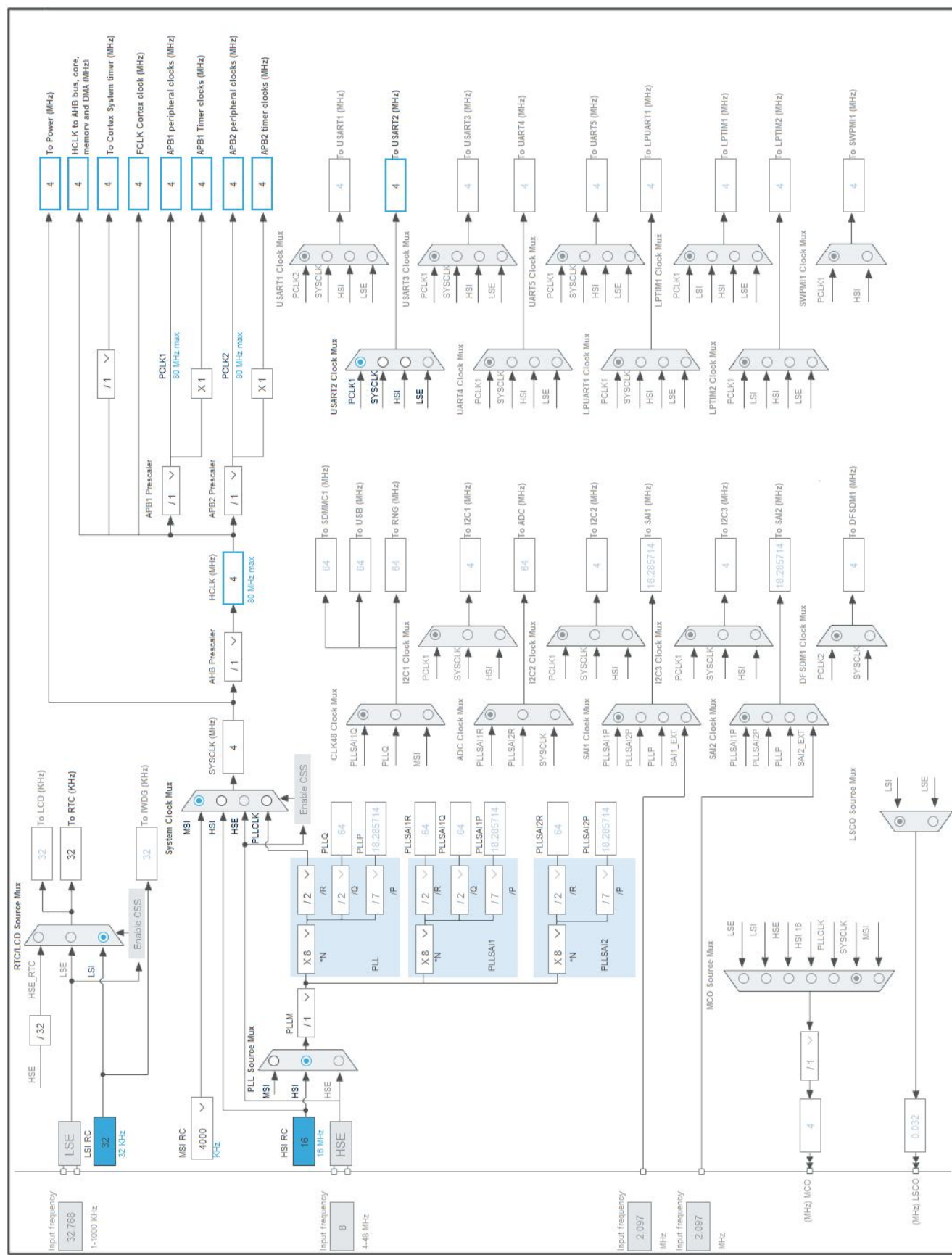
5. Software Project

5.1. Project Settings

Name	Value
Project Name	opis_zalozen
Project Folder	D:\sem6\sterowniki\projekty\opis_zalozen
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_L4 V1.17.1
Application Structure	Advanced
Generate Under Root	Yes
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x400

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No
Enable Full Assert	No

5.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	SystemClock_Config	RCC
2	MX_GPIO_Init	GPIO
3	MX_RTC_Init	RTC
4	MX_TIM2_Init	TIM2
5	MX_USART2_UART_Init	USART2
6	MX_SPI2_Init	SPI2

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32L4
Line	STM32L4x6
MCU	STM32L476VGTx
Datasheet	DS10198_Rev4

6.2. Parameter Selection

Temperature	25
Vdd	3.0

6.3. Battery Selection

Battery	Li-SOCL2(A3400)
Capacity	3400.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	100.0 mA
Max Pulse Current	200.0 mA
Cells in series	1
Cells in parallel	1

6.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP2
Vdd	3.0	3.0
Voltage Source	Battery	Battery
Range	Range1-High	NoRange
Fetch Type	SRAM2	n/a
CPU Frequency	80 MHz	0 Hz
Clock Configuration	HSE PLL	ALL CLOCKS OFF
Clock Source Frequency	4 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	10.7 mA	1.18 µA
Duration	0.1 ms	0.9 ms
DMIPS	100.0	0.0
Ta Max	103.65	105
Category	In DS Table	In DS Table

6.5. Results

Sequence Time	1 ms	Average Current	1.07 mA
Battery Life	4 months, 10 days, 3 hours	Average DMIPS	100.0 DMIPS

6.6. Chart
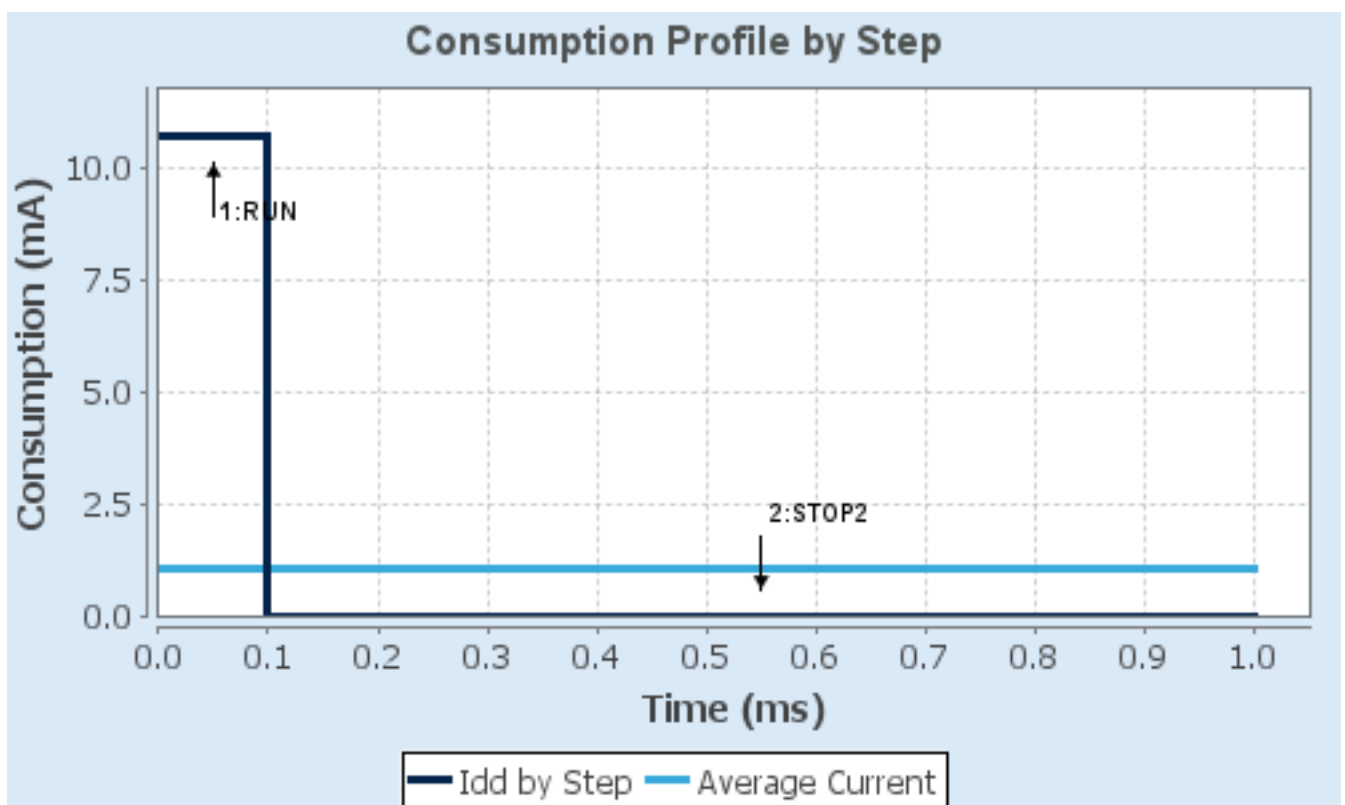
7. Peripherals and Middlewares Configuration

7.1. RCC

7.1.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Instruction Cache	Enabled
Prefetch Buffer	**Enabled ***
Data Cache	Enabled
Flash Latency(WS)	0 WS (1 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
MSI Calibration Value	0
MSI Auto Calibration	Disabled
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000

Power Parameters:

Power Regulator Voltage Scale	Power Regulator Voltage Scale 1

7.2. RTC
mode: Activate Clock Source
mode: Activate Calendar

7.2.1. Parameter Settings:

General:

Hour Format	Hourformat 24
Asynchronous Predivider value	127
Synchronous Predivider value	255

Calendar Time:

Data Format	BCD data format
Hours	**17 ***
Minutes	**35 ***
Seconds	0
Day Light Saving: value of hour adjustment	Daylightsaving None
Store Operation	Storeoperation Reset

Calendar Date:

Week Day	**Sunday ***

Month	**March ***
Date	**20 ***
Year	**22 ***

7.3. SPI2
Mode: Half-Duplex Slave
Hardware NSS Signal: Hardware NSS Input Signal
7.3.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	**8 Bits ***
First Bit	MSB First

Clock Parameters:

Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSS Signal Type	Input Hardware

7.4. SYS
Timebase Source: SysTick

7.5. TIM2
Clock Source   : Internal Clock
Channel1: Input Capture direct mode
Channel2: Input Capture indirect mode
Channel3: PWM Generation CH3
7.5.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**79 ***
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value)	**999999 ***
Internal Clock Division (CKD)	No Division

auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

Clear Input:

Clear Input Source	Disable

Input Capture Channel 1:

Polarity Selection	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter (4 bits value)	0

Input Capture Channel 2:

Polarity Selection	**Falling Edge ***
IC Selection	Indirect
Prescaler Division Ratio	No division

PWM Generation Channel 3:

Mode	PWM mode 1
Pulse (32 bits value)	**10 ***
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

7.6. USART2
Mode: Asynchronous
7.6.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable

Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

* User modified value

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
SPI2	PC2	SPI2_MISO	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	
	PD0	SPI2_NSS	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	
	PD1	SPI2_SCK	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	
TIM2	PA0	TIM2_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA2	TIM2_CH3	Alternate Function Push Pull	No pull-up and no pull-down	Low	
USART2	PA3	USART2_RX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	
	PD5	USART2_TX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	
Single Mapped Signals	PA1	TIM2_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
GPIO	PE6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	Buzzer
	PC0	GPIO_EXTI0	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	HC_Echo_2
	PC1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	HC_Trig_2
	PA6	GPIO_EXTI6	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	HC_Echo_3
	PA7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	HC_Trig_3
	PC4	GPIO_EXTI4	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	HC_Echo_4
	PC5	GPIO_EXTI5	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	HC_Trig_4
	PB1	GPIO_EXTI1	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	HC_Echo_1
	PB2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	HC_Trig_1
	PE0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	Acc_CS

8.2. DMA configuration

nothing configured in DMA service

8.3. NVIC configuration

8.3.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Prefetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
PVD/PVM1/PVM2/PVM3/PVM4 interrupts through EXTI lines 16/35/36/37/38	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
EXTI line0 interrupt	unused		
EXTI line1 interrupt	unused		
EXTI line4 interrupt	unused		
EXTI line[9:5] interrupts	unused		
TIM2 global interrupt	unused		
SPI2 global interrupt	unused		
USART2 global interrupt	unused		
FPU global interrupt	unused		

8.3.2. NVIC Code generation

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Prefetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	true	false
Debug monitor	false	true	false
Pendable request for system service	false	true	false
System tick timer	false	true	true

* User modified value

9. System Views

9.1. Category view

9.1.1. Current

Middleware

System Core	Analog	Timers	Connectivity	Multimedia	Security	Computing
DMA		RTC ✓	SPI2 ✓			
GPIO ⚠		TIM2 ✓	USART2 ✓			
NVIC ✓						
RCC ✓						
SYS ✓						

10. Docs & Resources

Type	Link
Presentations	https://www.st.com/resource/en/product_presentation/stm32-stm8_embedded_software_solutions.pdf
Presentations	https://www.st.com/resource/en/product_presentation/stm32_eval-tools_portfolio.pdf
Presentations	https://www.st.com/resource/en/product_presentation/stm32_stm8_functional-safety-packages.pdf
Presentations	https://www.st.com/resource/en/product_presentation/stm32l4_marketing-pres.pdf
Presentations	https://www.st.com/resource/en/product_presentation/stm32-stm8_software_development_tools.pdf
Training Material	https://www.st.com/resource/en/sales_guide/sg_sc2157.pdf
Flyers	https://www.st.com/resource/en/flyer/flnucleolrwan.pdf
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Product Certifications	https://www.st.com/resource/en/certification_document/sesip-2000002-01-st2.pdf
Product Certifications	https://www.st.com/resource/en/certification_document/psa-certificate_stm32l4.pdf
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Application Notes https://www.st.com/resource/en/application_note/an4616-migrating-from-stm32f401-and-stm32f411-lines-to-stm32l4-series-and-stm32l4-series-microcontrollers-stmicroelectronics.pdf

Application Notes https://www.st.com/resource/en/application_note/an4621-stm32l4-and-stm32l4-ultralowpower-features-overview-stmicroelectronics.pdf

Application Notes	https://www.st.com/resource/en/application_note/an4629-adc-hardware-oversampling-for-microcontrollers-of-the-stm32-l0-and-l4-series-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4635-minimization-of-power-consumption-using-lpuart-for-stm32-microcontrollers-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an4649-migrating-from-stm32f1-series-to-stm32l4-series--stm32l4-series-microntrollers-stmicroelectronics.pdf
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Application Notes	https://www.st.com/resource/en/application_note/an4729-stm32l0l4-firewall-overview-stmicroelectronics.pdf
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Application Notes	https://www.st.com/resource/en/application_note/an4746-optimizing-power-and-performance-with-stm32l4-and-stm32l4-series-microcontrollers-stmicroelectronics.pdf
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Application Notes https://www.st.com/resource/en/application_note/an4831-migrating-from-stm32f2x5-line-to-stm32l4-series-and-stm32l4-series-microcontrollers-stmicroelectronics.pdf

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