# ELECTROMANIA

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## 1 Introduction

Random number generators are fun circuits that have applications in games, simulations, cryptography, scientific experiments,lottery, etc. In this task, we are tasked with designing and constructing a random number generator capable of producing integers ranging from 0 to 9. The challenge is to accomplish this using only the ICs provided in the resource link. In this circuit the user is given a push button where it needs to be pressed for the number sequence to start. The number count goes from 0 to 9. When the button is pressed the circuit will increment the sequence at high speed and upon the release of this button you will have your random number. Overall, this project provides an excellent opportunity to learn about the fundamentals of electronics and programming while also developing a practical and useful tool.

## 2 Components

Components used are:-
1.555 Timer
2.D Flip Flop
3.MUX(2×1,4×1)
4.AND Gate
5.OR Gate
6.NOT Gate
7.Push Button
8.Seven Segment Display Decoder
9.Connecting Wire(Jumper Wire)

### 2.1 555 Timer

It is a useful precision timing device which can act as either a simple timer to generate single pulses or long time delays, or as a relaxation oscillator producing a string of stabilized waveforms of varying duty cycles from 50 to 100 percent. In its basic form, the single 555 Timer chip is a Bipolar 8-pin mini Dual-in-line Package (DIP) device consisting of some 25 transistors, 2 diodes and about 16 resistors arranged to form two comparators, a flip-flop and a high current output stage. A schematic diagram of 555timer is shown in Figure 1.

A brief description of its pins:
- Pin 1. – Ground, The ground pin connects the 555 timer to the negative (0v) supply rail.

- Pin 2. – Trigger, The negative input to comparator No 1. A negative pulse on this pin "sets" the internal Flip-flop when the voltage drops below 1/3 Vcc causing the output to switch from a "LOW" to a "HIGH" state.

- Pin 3. – Output, The output pin can drive any TTL circuit and is capable of sourcing or sinking up to 200mA of current at an output voltage equal to approximately Vcc – 1.5V so small speakers, LEDs or motors can be connected directly to the output.

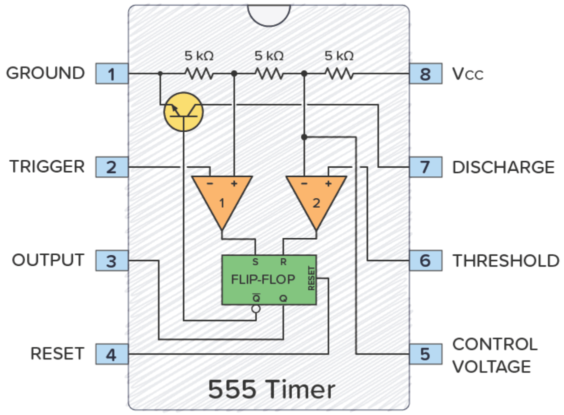


Figure 1: Schematic diagram of 555 timer

- Pin 4. – Reset, This pin is used to “reset” the internal Flip-flop controlling the state of the output, pin 3. This is an active-low input and is generally connected to a logic “1” level when not used to prevent any unwanted resetting of the output.

- Pin 5. – Control Voltage, This pin controls the timing of the 555 by overriding the 2/3Vcc level of the voltage divider network. By applying a voltage to this pin the width of the output signal can be varied independently of the RC timing network. When not used it is connected to ground via a 10nF capacitor to eliminate any noise.

- Pin 6. – Threshold, The positive input to comparator No 2. This pin is used to reset the Flip-flop when the voltage applied to it exceeds 2/3Vcc causing the output to switch from “HIGH” to “LOW” state. This pin connects directly to the RC timing circuit.

- Pin 7. – Discharge, The discharge pin is connected directly to the Collector of an internal NPN transistor which is used to “discharge” the timing capacitor to ground when the output at pin 3 switches “LOW”.

- Pin 8. – Supply +Vcc, This is the power supply pin and for general purpose TTL 555 timers is between 4.5V and 15V.

The 555 timer IC can operate in three modes: astable, monostable, and bistable.
Astable Mode: In astable mode, the 555 timer produces a continuous stream of square wave pulses. The duration of the pulse ”on” and ”off” times can be varied by adjusting the values of the resistor and capacitor connected to the timer. The frequency of the output signal can be calculated using the formula: f = 1.44 / ((R1 + 2 * R2) * C), where R1 and R2 are the resistors and C is the capacitor.

Monostable Mode: In monostable mode, the 555 timer produces a single pulse of a fixed duration when triggered. The duration of the pulse can be set by adjusting the values of the resistor and capacitor. The trigger input is usually a low-level input, and when the input is triggered, the output of the 555 timer goes high for a duration set by the RC network. The duration of the output pulse can be calculated using the formula: T = 1.1 * R * C, where R is the resistor and C is the capacitor.

## 2.2 D Flip Flop

A D (or Delay) Flip Flop is a digital electronic circuit used to delay the change of state of its output signal (Q) until the next rising edge of a clock timing input signal occurs.It is a modified Set-Reset flip-flop with the addition of an inverter to prevent the S and R inputs from being at the same logic

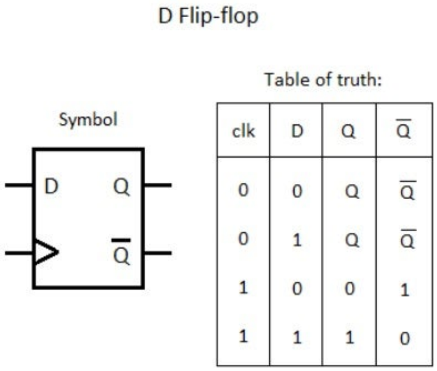


Table of truth:

| clk | D | Q | $\overline{Q}$ |
|---|---|---|---|
| 0 | 0 | Q | $\overline{Q}$ |
| 0 | 1 | Q | $\overline{Q}$ |
| 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 0 |

Figure 2: Truth table and diagram of D Flip Flop

level.It is a sequential logic circuit that stores one bit of data. It has a data input (D), a clock input (CLK), a set input (S), and a reset input (R). The output of the D flip-flop changes state (either 0 or 1) on the rising edge of the clock input. Its diagram and truth table is as shown in Figure2:

When the clock input is low, the D input is ignored, and the output remains in its previous state. When the clock input transitions from low to high, the D input is latched and appears at the output, and the output holds this value until the next rising edge of the clock input.The set input (S) and reset input (R) are used to force the output of the D flip-flop to a known state. When S is high, the output is set to 1, and when R is high, the output is reset to 0.

## 2.3 MUX (2X1 , 4X1)

A multiplexer, also known as a "mux," is a digital circuit that selects and transmits one of several input signals onto a single output line. It is used in digital systems to efficiently transmit multiple data signals over a shared communication line.

A multiplexer works by using a set of control inputs to select which of the input signals to transmit. The number of control inputs determines the number of input signals that can be selected. For example, a 2-to-1 mux has one control input and two data inputs, while a 4-to-1 mux has two control inputs and four data inputs.

It has n selection lines and 2n input lines. So, there are a total of 2N possible combinations of inputs.On the basis of the values of the selection lines, one of these data inputs will be connected to the output. There are various types of multiplexers:

**2×1 Multiplexer:** In 2×1 multiplexer, there are only two inputs, i.e., A0 and A1, 1 selection line, i.e., S0 and single outputs, i.e., Y. On the basis of the combination of inputs which are present at the selection line S0, one of these 2 inputs will be connected to the output. The block diagram and the truth table of the 2×1 multiplexer are given in Figure 3 and Figure 4 respectively.

The logical expression of the term Y is as follows:
Y=S0'.A0+S0.A1
Logical circuit of the above expression is given in Figure 5.

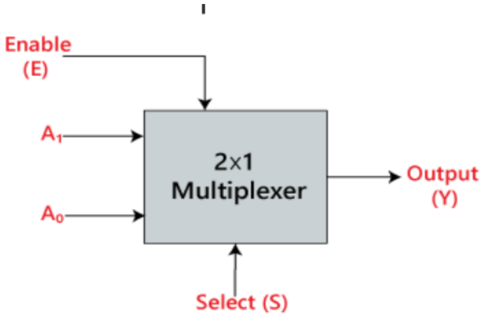
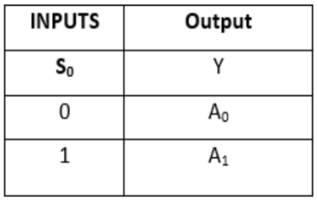


Figure 3: Block diagram of 2×1 multiplexer



| INPUTS | Output |
|---|---|
| $S_0$ | Y |
| 0 | $A_0$ |
| 1 | $A_1$ |

Figure 4: Truth table of 2×1 multiplexer

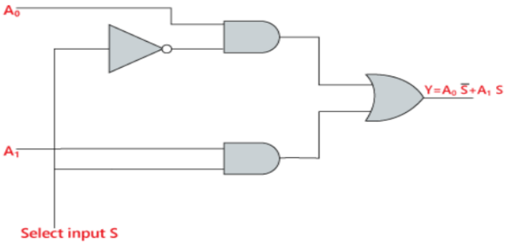


Figure 5: Logical circuit of Y=S0'.A0+S0.A1

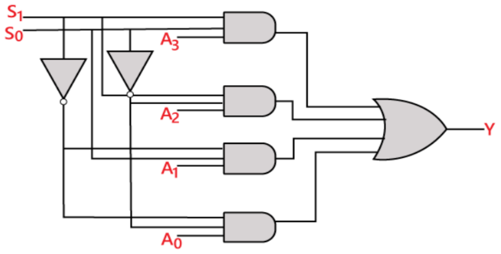
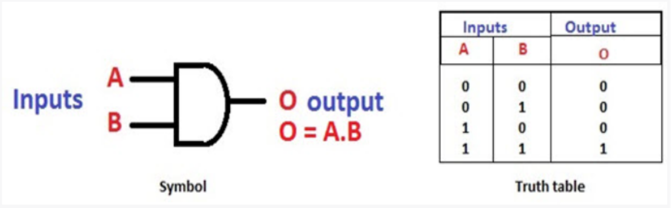


Figure 6: Logical circuit of Y=S1' S0' A0+S1' S0 A1+S1 S0' A2+S1 S0 A3



| Inputs | | Output |
|---|---|---|
| A | B | O |
| 0 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

Figure 7: Truth table of AND gate.

**4×1 Multiplexer:** A 4-to-1 multiplexer (or 4*1 mux) is a digital circuit that has four data input lines (D0, D1, D2, and D3), one output line (Y), and two control input lines (S0 and S1). The control inputs determine which of the four data inputs is selected to be transmitted to the output.

The logical expression of the term Y is as follows:
Y=S1' S0' A0+S1' S0 A1+S1 S0' A2+S1 S0 A3
Logical circuit of the above expression is given in Figure 6.

### 2.4 2 Input AND Gate(7408)

We are using 7408 AND gates .The 7408 is a common quad 2-input AND gate IC that contains four separate AND gates, each of which is capable of performing the logical AND function on two input signals. It is a popular integrated circuit used in digital electronics due to its low cost, high reliability, and ease of use.The 7408 AND gate is packaged in a 14-pin dual in-line package (DIP) and can be easily integrated into digital circuits. The inputs and outputs are designed to be compatible with a wide range of digital devices, such as microcontrollers, memory chips, and other logic gates.Schematic diagram of 2 input AND gate is as shown in Figure 8.

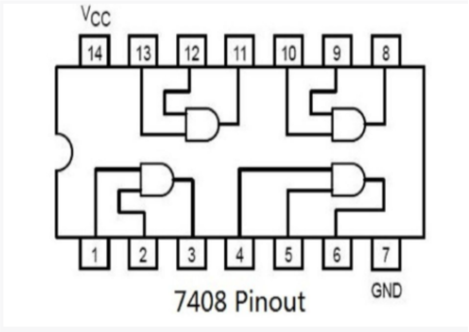
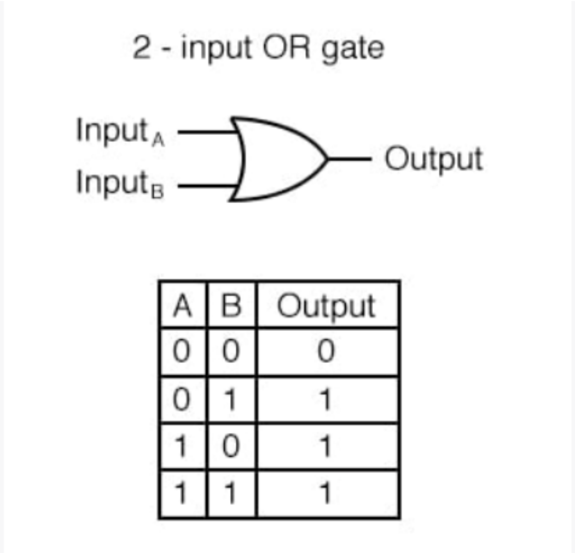


Figure 8: Schematic diagram of 7408 AND gate



| A | B | Output |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 1 |

Figure 9: Truth table of 2 Input OR Gate

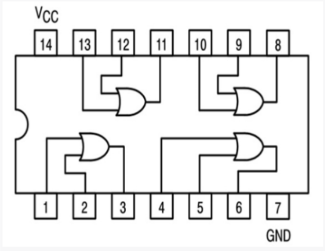


Figure 10: Schematic diagram of 7432 OR Gate

### 2.5 2 Input OR Gate(7432)

We are using 7432 OR gate.The 7432 is a commonly used quad 2-input OR gate integrated circuit (IC). It contains four separate OR gates, each of which is capable of performing the logical OR function on two input signals.The 7432 is a commonly used quad 2-input OR gate integrated circuit (IC). It contains four separate OR gates, each of which is capable of performing the logical OR function on two input signals.Schematic diagram of 2 input OR gate is as shown in Figure 10.

### 2.6 NOT gate(7404)

A NOT gate, also known as an inverter, is a fundamental logic gate in digital electronics. It is a type of electronic circuit that performs the opposite function of the input signal, as it changes a logic high (1) to a logic low (0) and vice versa.A NOT gate has one input and one output.The output of the NOT gate is the complement of the input, which means that when the input is high, the output is low, and when the input is low, the output is high.They are an essential building block in digital circuits, and are often combined with other logic gates, such as AND, OR, and XOR gates, to create more complex circuits.

We are using 7404 NOT gates , it is a common hex inverter IC that contains six NOT gates, each of which is capable of performing the logical NOT function on its input signal. The 7404 NOT gate is packaged in a 14-pin dual in-line package (DIP) and can be easily integrated into digital circuits. The inputs and outputs are designed to be compatible with a wide range of digital devices, such as microcontrollers, memory chips, and other logic gates.Schematic diagram of NOT gate is as shown in Figure 11.

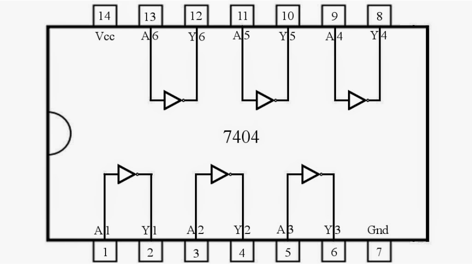


Figure 11: Schematic diagram 7404 of NOT gate

### 2.7 Seven Segment Display Decoder

A seven-segment display is an electronic display device that is commonly used to display numerical digits from 0 to 9, as well as some alphabetical characters and symbols. The display consists of seven individual LED segments arranged in a pattern that can be used to form different numbers and characters.Each segment of the display is labeled A to G, with an additional segment for a decimal point. By turning on or off the appropriate segments, different numbers and characters can be displayed.

Seven-segmentnt displays come in two main types: common anode and common cathode. In a common anode display, all the anodes of the LED segments are connected together and controlled by individual cathode connections.All the anode terminals of 7 LEDs are connected together to form a common anode terminal. This terminal should be connected with Vcc or logic ‘1’ during its operation.To illuminate any of the LED segments we need to provide logic ‘0’ to it.In a common cathode display, all the cathodes of the LED segments are connected together and controlled by individual anode connections.All the cathodes of the 7 LEDs are connected together to form a common terminal. It should be connected to GND or logic ‘0’ during its operation.

To illuminate any LED of the display, we need to supply logic ‘1’ to its corresponding input pin.
We are using the common cathode display as shown in Figure 12.

## 3 Working

### 3.1 555 Timer

The 555 timer generates clock pulses, which are used to clock the D flip-flops. The frequency of the clock pulses determines the rate at which the random numbers are generated.In this circuit 555 timer is wired as astable multivibrator where it generates square waves to feed the D flip flop .The frequency of this square wave depends upon the value of R1,R2 and C1. The formula to determine the output frequency is f = 1.44 / ( R2 + 2R1 ) C1 which gives a square wave of frequency 480hz as output.

We are keeping the frequency output high so that we cannot judge the number sequence by any means. A button is placed in the way of this signal which is fed to the D flip flop using clear input.The D flip flop counts from 0 to 9 with each individual clock pulse and resets back to 0 once it hits 9. This cycle repeats itself with the incoming clock signal. The decoder also decodes these counted values of 0 to 9 and lights up the 7 segments accordingly.

### 3.2 Seven Segment Display Decoder

The basic idea involves driving a common cathode 7-segment LED display using a combinational logic circuit. The logic circuit is designed with 4 inputs and 7 outputs, each representing an input to the display IC. 7 LED segments of the display and their pins are “a”, “b”, “c”, “d”, “e”, “f” “g” are shown in Figure 12.

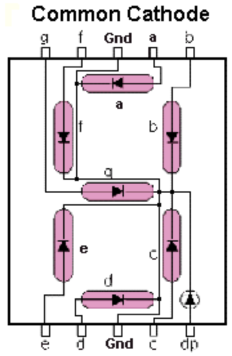
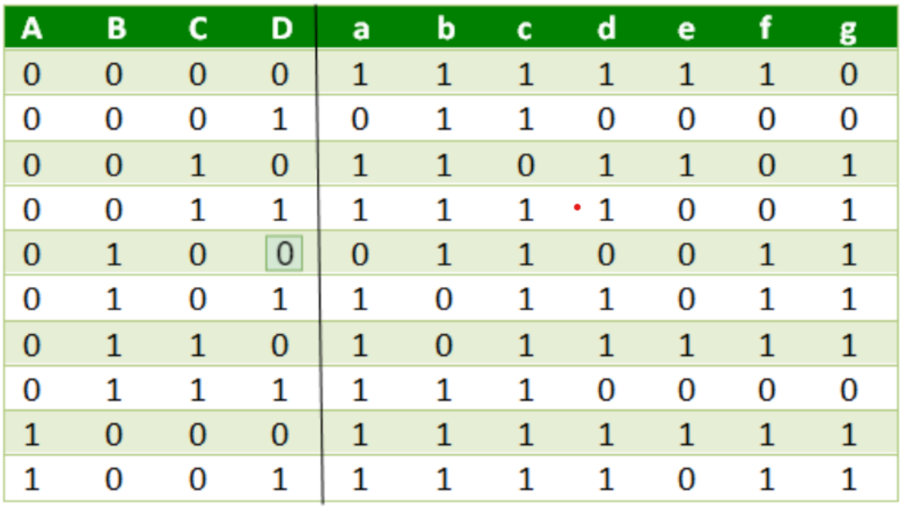


Figure 12: Schematic diagram of common cathode 7 segment LED display



| A | B | C | D | a | b | c | d | e | f | g |
|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 |
| 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 |
| 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 |
| 0 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 |

Figure 13: Truth Table of 7 segment LED display

Truth Table for 7-segment display decoder is given in Figure 13. Suppose the binary input ABCD to the decoder and output a, b, c, d, e, f,  g for the display.

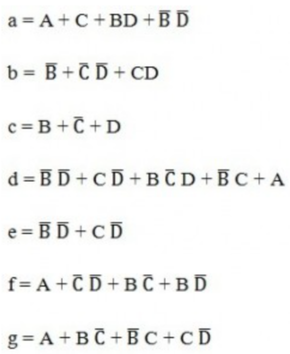
For other combinations of input, we need not care about the output as there are no more digits to display.From the karnaugh- map simplification, we get the output values as shown in Figure 14:-

Schematic diagram of 7-segment display decoder using logic gates is shown in Figure 15.

Display decoder circuit operation can be understood through the truth table .When all the inputs are connected to low logic , the output of the combinational logic circuit would be so as to drive all the output LEDs except 'g' to conduction. Thus the number 0 will be displayed. Similar operation would take place for all other combinations of the input switches.

### 3.3 D Flip Flop

In this task we use 4 flip flops.Clear input is the active low input.When signal is low it will reset all flip flops to 0.The 4 bit counter counts from 0 to 15.But we design combinational circuit in such a way that it generates a clear signal when count goes beyond 1001 and the circuit resets counter to 0000.The output should remain 1 till 1001 and when count goes to 1010,it generates a clear signal.We connect the Q output of each flip-flop to the D input of the next flip-flop in the chain. At the beginning, all the D flip-flops are reset to 0. As the clock signal changes from low to high, the first D flip-flop stores the value of 1 (or any desired initial value) on its Q output. The second D flip-flop then stores the value of the Q output of the first flip-flop, which is 1. This process continues for each subsequent D flip-flop in the chain, resulting in a binary count of 0001, 0010, 0011, 0100, and so on.



$a = A + C + BD + \bar{B}\,\bar{D}$

$b = \bar{B} + \bar{C}\,\bar{D} + CD$

$c = B + \bar{C} + D$

$d = \bar{B}\,\bar{D} + C\,\bar{D} + B\,\bar{C}\,D + \bar{B}\,C + A$

$e = \bar{B}\,\bar{D} + C\,\bar{D}$

$f = A + \bar{C}\,\bar{D} + B\,\bar{C} + B\,\bar{D}$

$g = A + B\,\bar{C} + \bar{B}\,C + C\,\bar{D}$

Figure 14: Expression dervied from karnaugh map for 7-segment LED display

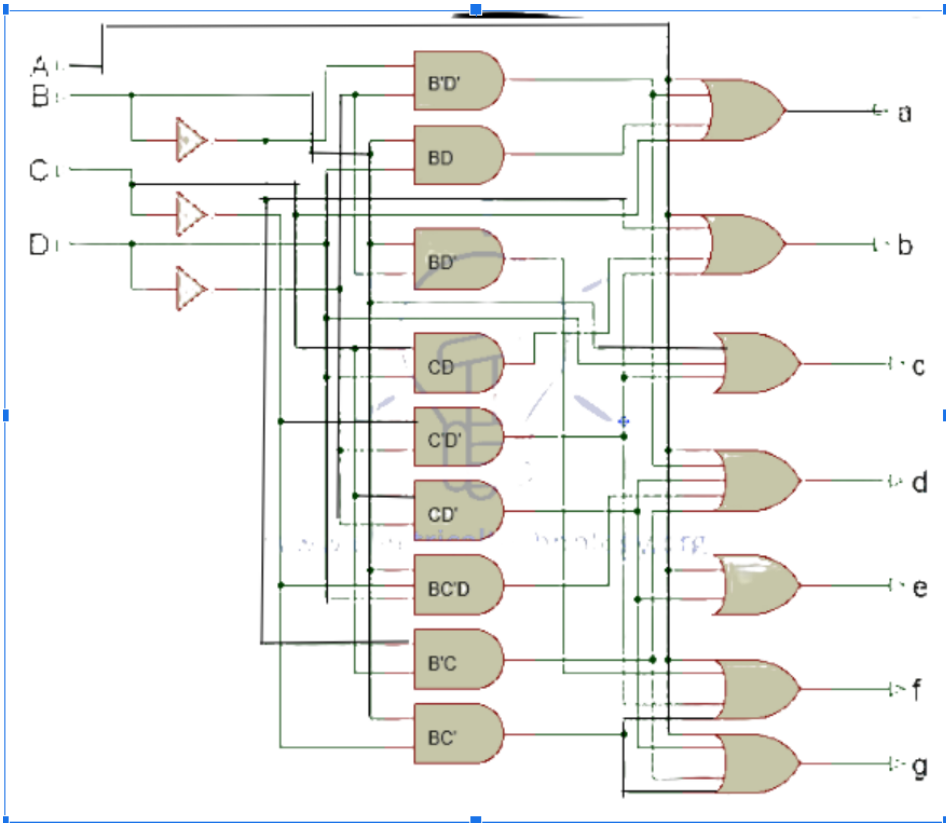


Figure 15: Schematic of 7 segment display decoder using logic gates

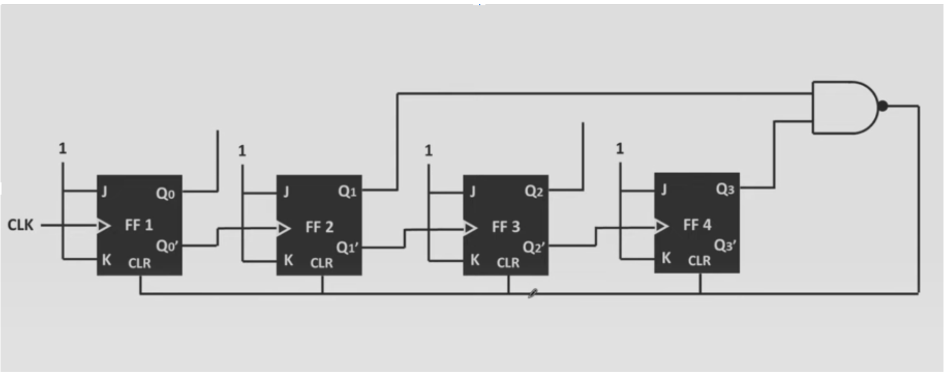


Figure 16: Schematic diagram of D-flip flops

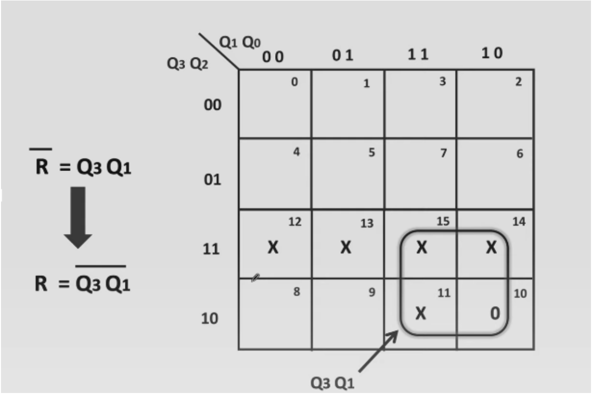


Figure 17: Karnaugh map of Figure 16

We use NAND gate in feedback to generate clear signal.Since initial state of flip flop is not known so they have been cleared with help of clear input and this signal is applied to multiplexer.So when select input is 0,the flip flops will get reset to 0 and when selection input is 1,the output of NAND gate will get connected to clear input of all flip flops.
Schematic diagram of D-flip flops is shown in Figure 16 and binary table of BCD ripple counter is shown in Figure 18.

## 3.4 Overall Working

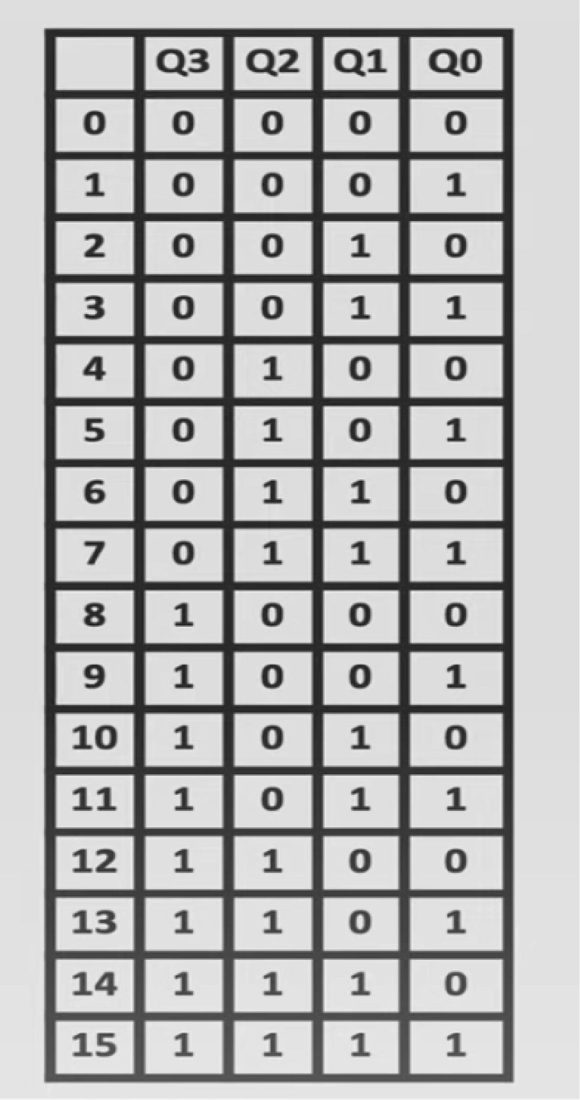
A random number generator using a 555 timer, D flip-flops, and a seven-segment display decoder is a digital circuit that generates random numbers and displays them on a seven-segment display. Here's how it works:

:-The 555 timer generates clock pulses, which are used to clock the D flip-flops. The frequency of the clock pulses determines the rate at which the random numbers are generated.

:-The D flip-flops store the random bits generated by the circuit. The number of flip-flops used determines the length of the random number generated. For example, if four flip-flops are used, the random number generated will be a four-bit number.

:-The output of the D flip-flops is connected to a seven-segment display decoder. The decoder converts the binary number stored in the flip-flops to a corresponding decimal digit that is displayed on the seven-segment display.

:-To generate a new random number, the circuit is reset by pressing a reset button, which resets



| | Q3 | Q2 | Q1 | Q0 |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 1 |
| 2 | 0 | 0 | 1 | 0 |
| 3 | 0 | 0 | 1 | 1 |
| 4 | 0 | 1 | 0 | 0 |
| 5 | 0 | 1 | 0 | 1 |
| 6 | 0 | 1 | 1 | 0 |
| 7 | 0 | 1 | 1 | 1 |
| 8 | 1 | 0 | 0 | 0 |
| 9 | 1 | 0 | 0 | 1 |
| 10 | 1 | 0 | 1 | 0 |
| 11 | 1 | 0 | 1 | 1 |
| 12 | 1 | 1 | 0 | 0 |
| 13 | 1 | 1 | 0 | 1 |
| 14 | 1 | 1 | 1 | 0 |
| 15 | 1 | 1 | 1 | 1 |

Figure 18: Binary table of BCD (Binary Coded Decimal) Ripple Counter

the flip-flops to a known state.

:-The random numbers generated by the circuit are not truly random, but rather are pseudo-random, as they are generated based on a deterministic algorithm. However, the circuit can be designed to generate numbers that are sufficiently random for most practical purposes.

To generate the numbers 0-9 using a seven-segment display decoder, the binary outputs of the D flip-flops need to be connected to the correct inputs of the decoder. The decoder converts the binary values into the corresponding decimal digit, which is then displayed on the seven-segment display.

The binary values for the numbers 0-9 are:
0: 0000
1: 0001
2: 0010
3: 0011
4: 0100
5: 0101
6: 0110
7: 0111
8: 1000
9: 1001

To display the number 0, all seven segments of the display must be turned on. To display the numbers 1-9, specific segments must be turned on or off, depending on the digit being displayed. The mapping of the binary values to the segments of the display is determined by the particular decoder being used.

Here's an example of how the binary outputs of four D flip-flops could be connected to a seven-segment display decoder to display the numbers 0-9:

Flip-flop 1 output connected to decoder input A Flip-flop 2 output connected to decoder input B Flip-flop 3 output connected to decoder input C Flip-flop 4 output connected to decoder input D The other inputs of the decoder are connected to appropriate logic levels to turn on or off specific segments of the display for each digit.

Overall, the method to generate the numbers 0-9 using a seven-segment display decoder involves connecting the binary outputs of the D flip-flops to the appropriate inputs of the decoder to produce the desired decimal digit on the display.

## 4 Construction

The method for designing and building a random number generator using a 555 timer, D flip-flops, and a seven-segment display decoder can be broken down into the following steps:

1.Determine the number of D flip-flops required for the desired length of the random number. Each D flip-flop stores one binary bit of the random number. For example, if a four-bit random number is desired, four D flip-flops will be required.

2.Design the clock circuit using a 555 timer. The clock circuit generates clock pulses at a regular frequency that is used to drive the clock input of the D flip-flops. The frequency of the clock pulses can be adjusted using a potentiometer or fixed resistor and capacitor values. Connect the clock circuit to the clock input of the D flip-flops. When the clock pulse arrives, the D flip-flops store the binary value at their inputs, which is then propagated to their outputs.

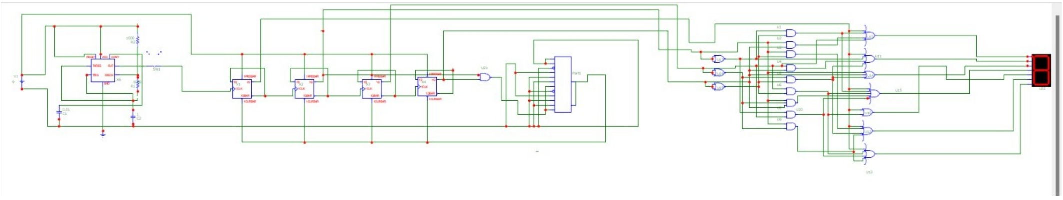


Figure 19: Schematic diagram of random number generator circuit

3.Connect the outputs of the D flip-flops to the inputs of the seven-segment display decoder. The decoder converts the binary number stored in the flip-flops to a corresponding decimal digit that is displayed on the seven-segment display. Test the circuit to ensure it is generating random numbers and displaying them correctly. To generate a new random number, press a reset button, which resets the flip-flops to a known state.

4.Introduce randomness to the circuit, if desired, by using external analog sources such as noise generators or by clocking the flip-flops asynchronously. Fine-tune the circuit as necessary to achieve the desired level of randomness and accuracy in the generated numbers.

5.Overall, the method for building a random number generator using a 555 timer, D flip-flops, and a seven-segment display decoder involves designing and connecting the necessary components to generate and display random numbers, and then testing and fine-tuning the circuit to ensure it is working correctly.

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