1. Figures to the right indicate maximum marks for that question.
2. The symbols used carry their usual meanings.
3. Assume suitable data, if required & mention them clearly.
4. Draw neat sketches wherever necessary.

Q.1 Do as directed.

(a) Explain ADSTB and AEN pin with respect to DMA controller. [12]

(b) What is vectored interrupt? Draw the simple architecture of it. [2]

(c) Derive the equation for the size of the architecture in terms of bits for the following. [2]
1) micro programmed
2) micro + nano programmed

(d) What is the function of TLB? Which memory technology is used to implement it? [2]

(e) Suppose 8085 uses a clock frequency of 3MHz and ADD instruction takes four states. How long it takes to process the instruction? Why the conditional jumps have different number of T states? [2]

(f) Why there is a need of cache coherence protocols? Explain with example. [2]

Q.2 Attempt ***Any Two*** from the following questions.

(a) Implement all the necessary control words with respect to DMA for the given Scenario:: [12]
A pen-drive is connected on Channel 2, request is coming on Channel 2, DMA can transfer the data from memory to memory, auto initialization is disabled, DMA is attached to 8085 in a simple timing mode, request is generated for 80 bytes and grant is given for 20 bytes, linux OS and channel 0 and 1 are masked. [6]

(b) Calculate the loss of clock cycles without using any branch prediction buffer and with using 1 bit and 2 bits branch prediction buffers. [6]

```
For (i=1 to 70)
{
  .....
  For (j = i to 50)
  {
    .....
    ......
    For(k = j to 25)
    {
      ......
    }
    .......
  }
.........
}
```

(c) Explain Daisy Chaining, Polling and independent requesting with respect to interrupts with neat and clean diagrams. [6]

Q.3 Answer the followings [12]

(a) Explain the Cache coherence protocol. Write a short note on MESI protocol. [6]

(b) i) Consider a byte-addressable computer with 24-bit addresses, a cache capable of storing a total of 64K bytes of data and blocks of 32 bytes. Show the format of a 24-bit memory address for: [3]
a. direct mapped
b. associative
c. 4-way set associative

ii) Suppose that a 2M x 16 main memory is built using 256K x 8 RAM chips and memory is word addressable. [3]

a) How many RAM chips are necessary?
b) How many banks will this memory have?
c) How many address bits are needed for all of the memory?

OR

Q.3 Answer the followings *[12]*

(a) i) Suppose the page table for the process currently executing on the processor looks like the following. All numbers are decimal, everything is numbered starting from 0, and all addresses are memory byte addresses. The page size is 1024 bytes. [4]

Virtual page number	Valid bit	Presence bit	Modify bit	Page frame number
0	1	1	0	4
1	1	1	1	7
2	0	0	0	-
3	1	1	0	2
4	0	0	0	-
5	1	0	1	0

What physical address, if any, would each of the following virtual addresses correspond to? (i) 2001 (ii) 2221 (iii) 5499

ii) All modern microprocessors have an on-chip cache which is called the L1 cache and another larger off chip cache called the L2 cache. Assume a L1 hit time of 1, a L2 hit time of 5 and a L2 miss penalty of 17 cycles. Find the average access time given a L1 hit rate of 98% and a L2 hit rate of 98%. [2]

(b) Explain all the processes about how any ISR would be executed on processors? [6]