DHARMSINH DESAI UNIVERSITY, NADIAD
FACULTY OF TECHNOLOGY
B.TECH. SEMESTER IV CE
SUBJECT: (CE 417) Computer System Architecture

Examination : 3rd Sessional **Seat No.** : CE 103
Date : 28/03/2017 **Day** : Tuesday
Time : 10.30 AM to 11.45 AM **Max. Marks** : 36

Q.1 Do as directed [12]

a Discuss cache coherence problem. [2]
b State the difference between anticipatory swapping and demand swapping. [2]
c Derive the expression to find the optimum page size in the paged segment system. [2]
d Why do we require Interrupt Flag inside the processor? Give an example of it. [2]
e Give an example where write invalidate is good with respect to write through protocol. [2]
f What is the difference between NMI and simple interrupt? Explain with an example. [2]

Q.2 Answer any two of the following [12]

a What is interrupt vector table? Explain the steps for the execution of "Keyboard ISR" with an example with Conventional Interrupt Vector Table. [6]
b Explain MESI protocol in detail with a state transition diagram. [6]
c Explain how we can generate priority and remove the priority in all the Arbitration Techniques. Explain each arbitration technique in detail. [6]

Daisy chain Polling Indepen

Q.3 Do as directed [12]

a A virtual memory has a page of size 1K words. There are eight pages and four blocks. The associative memory page table contains the following entries: [4]

Page	Block
0	3
1	1
4	2
6	0

Make a list of all virtual addresses(in decimal) that will cause a page fault if used by the CPU.

b A CPU generates 32 bit virtual addresses, the page size is 4KB, the processor has a TLB which can hold a total of 128 page table entries and is 4 way set associative. What is the minimum size of TLB tag? [2]
c Describe the ways to increase the speed of RAM interface. [4]
d What is the function of TLB? Which memory technology is used to implement TLB. [2]

OR

Q.3 Do as directed

a How many 128 X 8 RAM chips are needed to provide a memory capacity of 2048 bytes? How many lines of the address bus must be used to access 2048 bytes of the memory? [3]

b. A CPU has 32 bit memory address and a 256Kb cache memory, the cache is organized as a 4 way set associative cache with cache block size of 16 bytes. [5]
i) What is the number of sets in the cache?
ii) What is the size of tag filled per cache block?
iii) What is the number and size of comparators required for tag matching?
iv) How many address bits are required to find the byte offset within a cache block?
v) What is the total amount of extra memory (in bytes) required for the tag bits?

c. Determine the average access time for the specification given below: [4]
Access time of the cache = 5 ns, Cache hit rate = 80 percent.
Access time of the main memory =100ns. Main memory hit rate = 99.5 percent.
Access time of the virtual memory = 10 ms.

$t_a = H_1 t_{a_1} + (1-H) t_{a_2}$

$t_{a_1} = 100\ ns$