

Simulation Exercise - 1

The TSMC 180 nm technology which you will be using for your simulations in the course, can handle a voltage range from 0V to 1.8V for both V_{GS} and V_{DS} . If you exceed this range, the transistor will enter breakdown region, rendering it unusable.

Problem-1: Obtain the transfer characteristics (I_D v/s V_{GS}) and output characteristics (I_D v/s V_{DS}) of the NMOS and PMOS transistor. For the PMOS transistor, V_{GS} and V_{DS} will change to V_{SG} and V_{SD} respectively.

- Simulate the transfer characteristics of an NMOS transistor for $V_{DS} = 0V, 0.9V$ and $1.8V$. Vary V_{GS} from 0V to 1.8V and use $W/L = 1\mu m/0.18\mu m$. Plot the curves on a single graph and compare. What is the threshold voltage of NMOS and PMOS transistors you see in simulations?
- Repeat the above exercise for a PMOS transistor.
- Simulate the output characteristics of an NMOS transistor for $V_{GS} = 0V, 0.8V$ and $1.4V$. Vary V_{DS} from 0V to 1.8V and use $W/L = 1\mu m/0.18\mu m$. Plot the curves on a single graph and compare. Find the value of V_{DS} at which the transistor enters saturation region.
- Repeat the above exercise for a PMOS transistor.
- Calculate the value of $\mu_n C_{ox}$, $\mu_p C_{ox}$, λ_n and λ_p for the NMOS and PMOS transistors from these simulations. This will be useful later.

Problem-2: Determine the small signal parameters (g_m , r_{ds}) of the NMOS and PMOS transistors at $V_{GS} = 0.8V$.

Problem-3: For an NMOS device in saturation, plot I_D vs W (for a constant length) and I_D vs L (for a constant width). Use $V_{GS} = 0.8V$ and appropriate V_{DS} . Compare it with calculated values obtained from the equation discussed in class. Discuss your observations and explain any discrepancies you see.