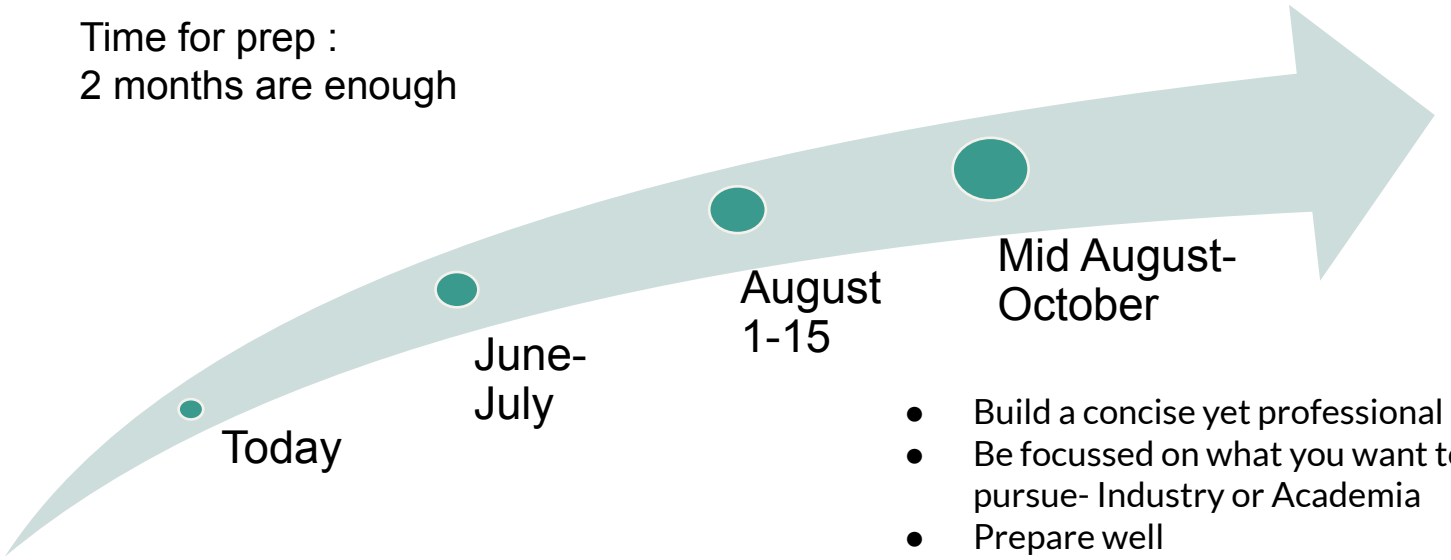
Core ECE Internship prep

Industry and Research based Internships- 2021

Timeline

Time for prep :
2 months are enough



- Build a concise yet professional resume
- Be focussed on what you want to pursue- Industry or Academia
- Prepare well
- Be confident

Companies to target

Frequent visitors:

- Texas Instruments
- Qualcomm
- Samsung Semiconductor

Less Frequent visitors:

- Google Hardware
- Nvidia Hardware
- Analog Devices (Mostly EE)

Company wise format

- Google Hardware
  - Resume based selection in round 1
  - 2 technical interviews, 1 hour each.
  - 1st interview - Analog, Verilog output prediction
  - 2nd interview - Digital, C++/Python coding, Verilog, Resume based questioning.
  - A brief HR round to finish it up
- Texas Instrument
  - Test: 3 sections. Analog (20 ques, 45 min), Digital (20 ques, 45 min) and aptitude (20 ques, 30 min)
  - Marking: +1, -0.5
  - 8-10 questions usually sufficient for interviews in respective profiles
  - Multiple round interview. RC related questions extensively asked

- Qualcomm
  - Test in round 1 containing basic digital,analog,basic programming(OOPS and data structures),verilog based questions and aptitude
  - Round 2 is a resume based interview,basic digital,analog and verilog questions also included(depending on resume)
  - Round 3 is a basic HR round to wrap things up
- Nvidia Graphics

What to prepare- Analog

- Network Theory Concepts: RC, RL, LC and RLC circuits with voltage source and current source. (Problems to start)
  - Finding poles and zeros etc. and frequency response. (Basic concepts) Links: [1], [2]
  - Develop intuitive understanding to plot direct response w/o solving it using Laplace. (most frequently asked in TI interviews).
- Op-AMP Basics and Circuit Topology for different Applications
  - Op-Amp Applications and Oscillator lectures. (Resources)
  - Concept of negative feedback and deciding signs of Op-Amp for the same. [Video Links]

- For studying Analog basics:
  - Topics: Single-Stage Amplifiers, Cascaded Topologies, Differential Amplifiers, Current Mirrors, Frequency Response of Amplifiers (concept of miller capacitance etc.) and Feedback.
  - Book: Design of CMOS Analog Integrated Circuits. [Link] Chapter: 2, 3, 4, 5, 6, 8,10,12
  - Or Consider Lectures by Shanti Pavan. [Videos Link]
  - Do problems after readings the topics. [Link]
- Must Do problem Sets [Link]
- Do the problems uploaded by seniors in their feedbacks in Channeli. [1] (Check others too).

What to prepare- Digital

- Digital Logic Design (Morris Mano) [Book] Chapter: 1 to 6
  - Moore and Mealy Machine Design for different type of problems. (Logical Design as well as Verilog Implementation) (Imp).
- Digital Integrated Circuit (Rabaey) [Book] Chapter: 1 and 5 (CMOS Inverter)
- Static Timings Analysis. Video links: [1], [2]. Questions: [1], [2].
- Miscellaneous Digital Ques (Must do and solve it thoroughly): [1]
- SRAM and DRAM Basics. [Link]
- Basic of 555 Timer.
- Quick go through of Digital CMOS circuits (Razavi chapter 15)

What to prepare - Verilog

- Go through videos 1-24 of NPTEL series : [1]
- For Tests: Do these ques: [1]
- Normal Syntax Practice: [1], [2]
- For interviews: basic syntax is asked and design flow for Moore and Mealy Machine in Verilog. Elaborated Design for simple latches mith be asked.

What to prepare - Computer Architecture

- Follow topics written below from your course slides or [Slide link].
- CPU Performance ques, Amdahl's law, Memory Hierarchy, Assembly language basic, MIPS instructions, Difference between multi-cycle, single cycle and pipelined architecture. (Basic info is enough)
- Addressing mode(Imp)
- Basic understanding of 8085 and 8086 architecture.
- Read about cache thoroughly. (Most Imp)

Miscellaneous

- Basic of semiconductor theory. (Few ques only in Samsung Semiconductor Analog test).
- Some programming i/p and o/p ques.
- Feedback (Control system). Already written in analog section.
- Basic signal processing. (Sometimes asked in TI).

Interviews

- Prepare the topics well and try to clear tests for most of the companies.
- Consult regularly with immediate seniors of test and interview patterns over the recent years.
- For interviews, you need to express yourself with the knowledge you have.
- Prepare resume thoroughly. You should know every spec and details of the projects.

- It’s ok not to know the answer of any ques. But speak what you are thinking. Interviewer will help.
- Be curious but don’t show yourself over-excited. Talk normally.
- If you know the solution of a problem, describe it such that you are solving it lively in front of interviewer.
- HR round is not an eliminator, but prepare the general HR ques asked to immediate seniors in Core ECE companies interviews.

General Advice

Try to do work with a professor in the summers to have some experience. It is not mandatory to do it but preferable if you do.

- Spark
- Project under any professor
- Certified Courses

“Believe in the process and
Get your basics right,
You will be able to make it.
Best of Luck!