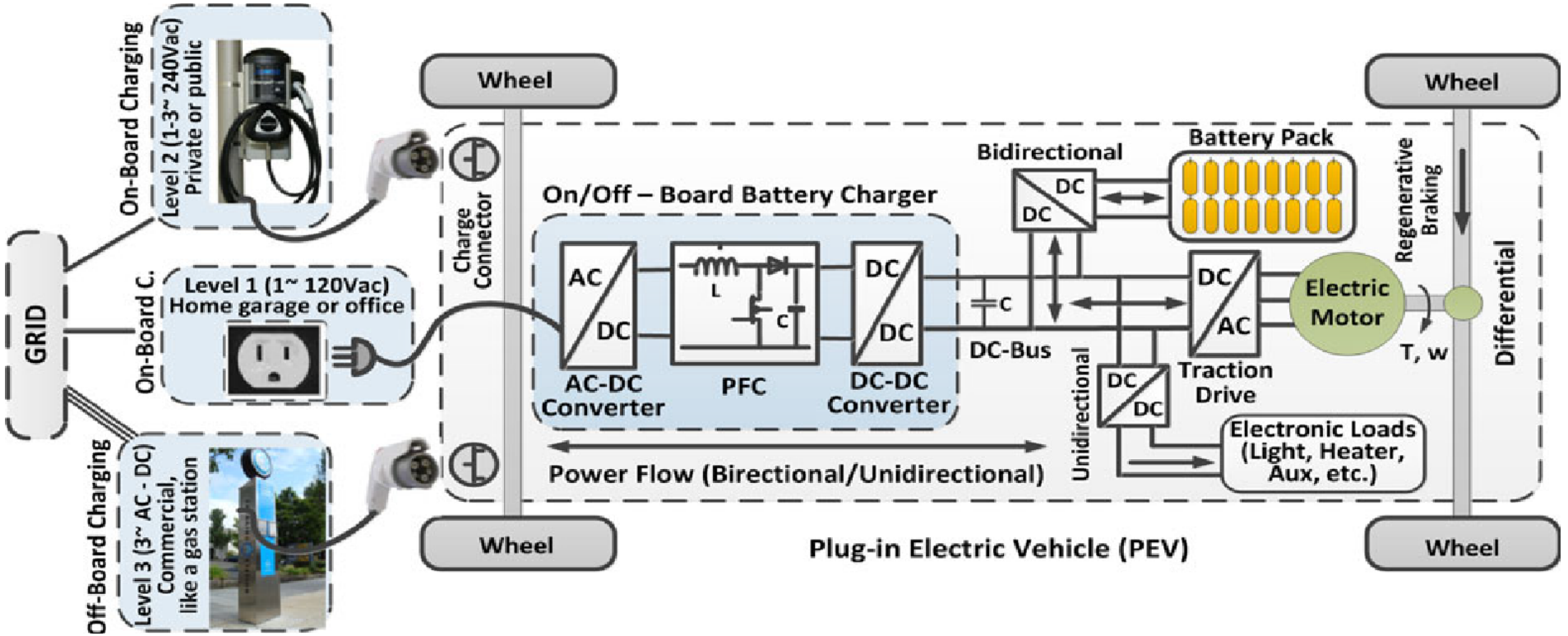
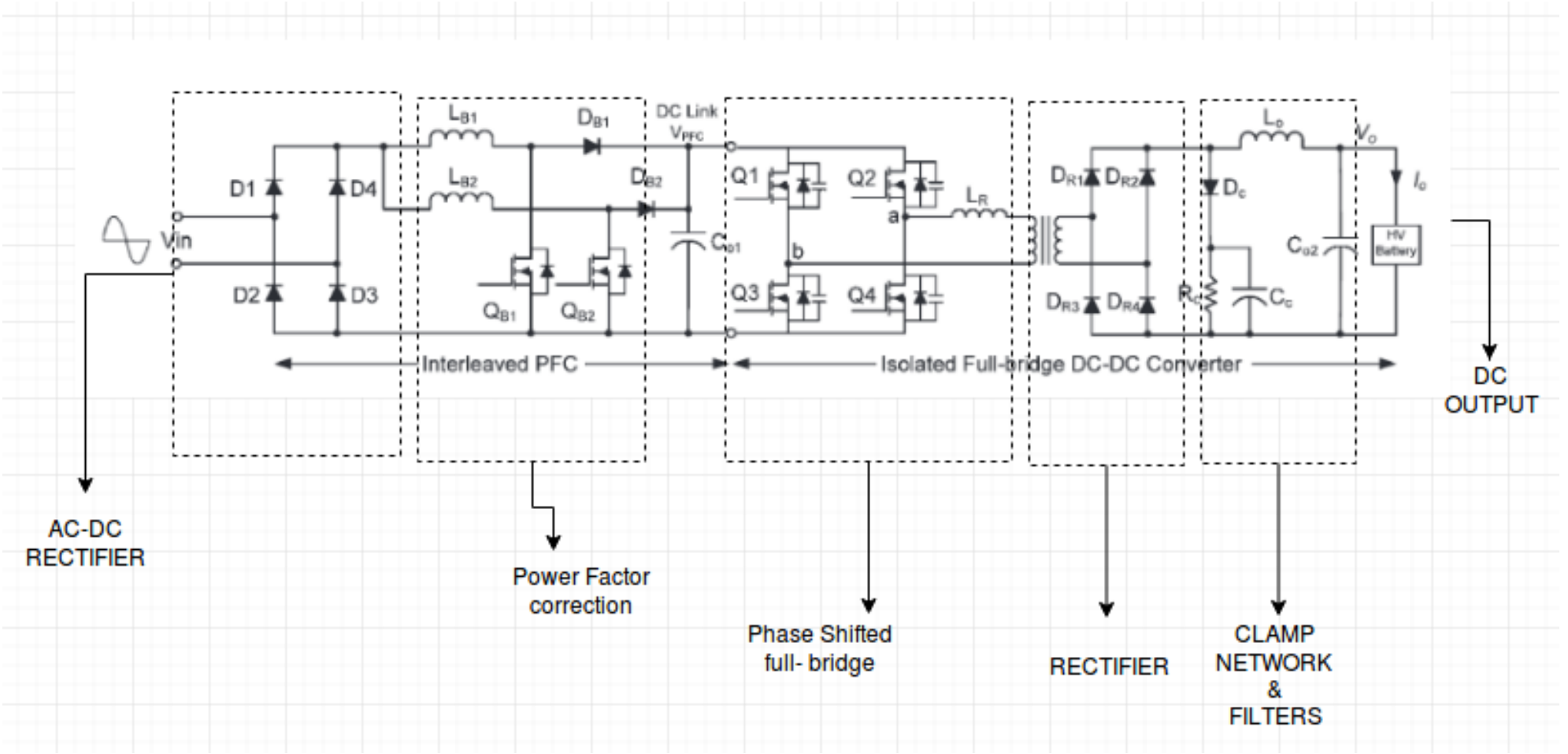
Implementation of phase shifted full bridge converter for PHEV




Vin
D1
D2
D3
D4
L_{B1}
L_{B2}
D_{B1}
D_{B2}
Q_{B1}
Q_{B2}
DC Link
V_{PFC}
C_{o1}
Q1
Q2
Q3
Q4
a
b
L_R
D_{R1}
D_{R2}
D_{R3}
D_{R4}
D_c
L_o
V_o
I_o
C_{o2}
R_c
C_c
HV Battery
Interleaved PFC
Isolated Full-bridge DC-DC Converter
AC-DC RECTIFIER
Power Factor correction
Phase Shifted full- bridge
RECTIFIER
CLAMP NETWORK & FILTERS
DC OUTPUT

A phase shift full bridge pwm based dc-dc converter is proposed and various design parts are explained that is useful for the PHEV application.

The most common charger power architecture includes an AC-DC converter with power factor correction(PFC) followed by an isolated DC-DC converter.\

Two stage battery charger is presented, including an AC-DC converter with an interleaved boost PFC followed by a PWM ZVS full-bridge DC-DC converter.

Converter can be divided in 3 major groups:

Front end First stage AC-DC PFC rectifier

Front end Second stage ZVS Full Bridge DC-DC Converter

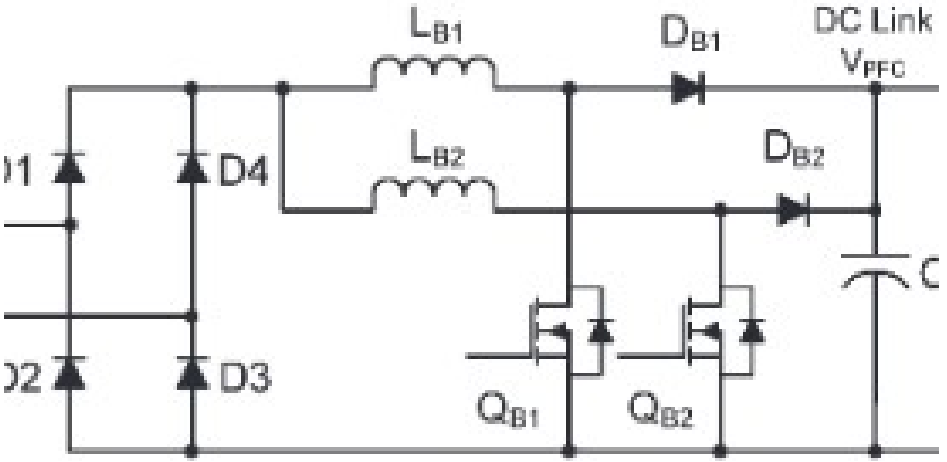
Last end First stage Rectifier

Last end Second stage Clamp Network

Last end Third stage Filter Circuit

Front-End First Stage AC-DC PFC Rectifier

The interleaved PFC consists of two CCM boost converters in parallel, which operate 180° out of phase. The maximum input inductor ripple current cancellation occurs at 50% duty cycle. Interleaving reduces the output capacitor ripple current as a function of the duty cycle. The interleaved boost converter inherently takes advantage of paralleled semiconductors to reduce conduction loss.



Second Stage ZVS Full-Bridge DC-DC Converter

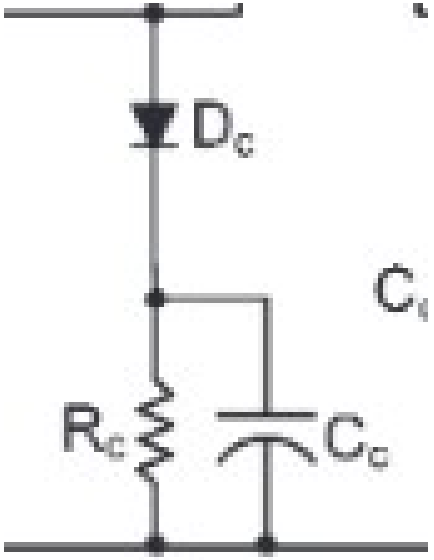
ZVS for the switches is realized by using the leakage inductance of the transformer, in addition to an external inductor and the output capacitance of the switch.

The resonant transition may be estimated by

$$\tau = \frac{\pi}{2} \frac{1}{\sqrt{\frac{1}{L_R \times C} - \frac{R^2}{4 \times (L_R)^2}}}$$

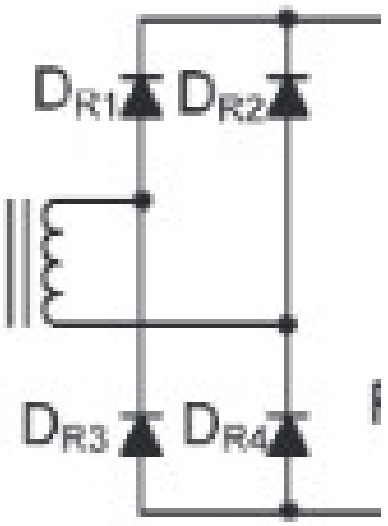
Last End Second stage Clamp Network

A clamp network consisting of diode, capacitor and resistor are needed across the output rectifier to clamp the voltage ringing due to diode junction capacitance with the leakage inductance of the transformer.



Last end First stage rectifier

Finally with the transformer output provides the voltage which is rectified and hence given to the clamp network. Synchronous Rectification with the mosfet can be applied for further improvement.



Action Plan

01.02.2018	• Paper downloaded and model identified.
08.02.2018	• Base papers • Software Simulation • Front end study Finalised
15.02.2018	• Final pcb designing in eagle
22.02.2018	• Final Simulation Pspice
01.03.2018	• Hardware Ratings and All calculation Finalised
13.03.2018	• Pcb fabrication
20.03.2018	• Troubleshooting and waveform generation.
27.03.2018	• Troubleshooting and waveform generation and casing.
5.04.2018	• Completed