Computer Architecture Final Project Report

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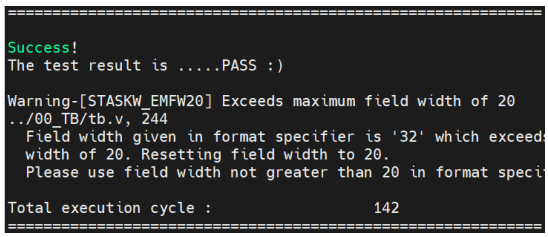
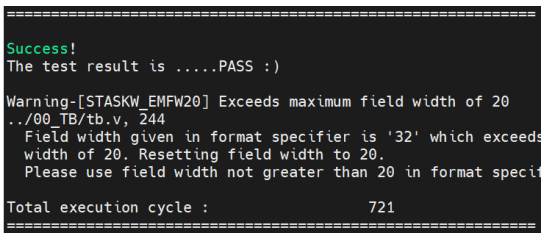
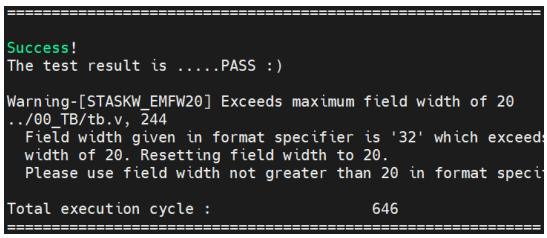
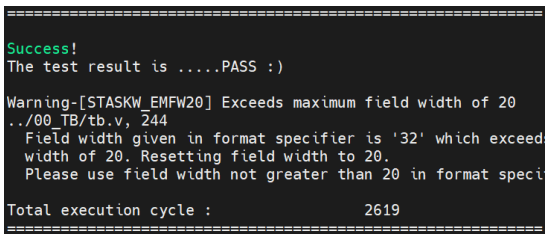
1. Execution Cycle Number









Instruction Set	Execution Cycle
I0	142
I1	721
I2	646
I3	2619

2. Synthesizable Check: all flip-flops

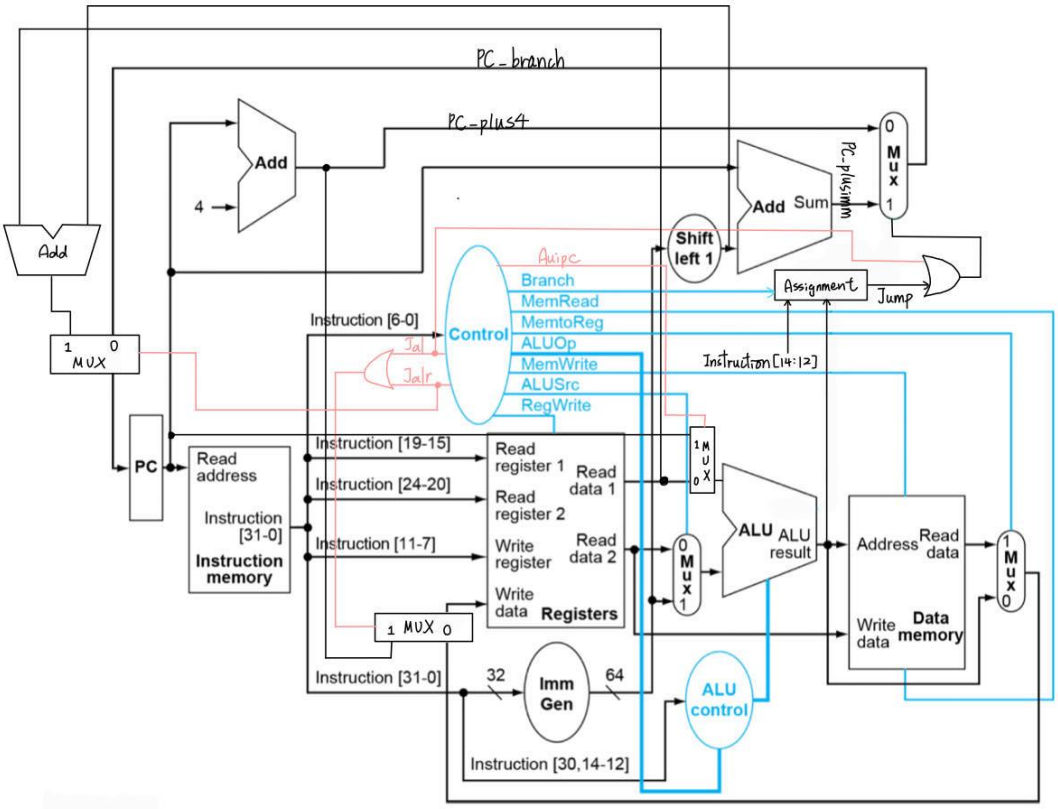
Register Name	Type	Width	Bus	MB	AR	AS	SR	SS	ST
PC_reg	Flip-flop	31	Y	N	Y	N	N	N	N
PC_reg	Flip-flop	1	N	N	N	Y	N	N	N
state_reg	Flip-flop	2	Y	N	Y	N	N	N	N

Register Name	Type	Width	Bus	MB	AR	AS	SR	SS	ST
mem_reg	Flip-flop	995	Y	N	Y	N	N	N	N
mem_reg	Flip-flop	29	Y	N	N	Y	N	N	N

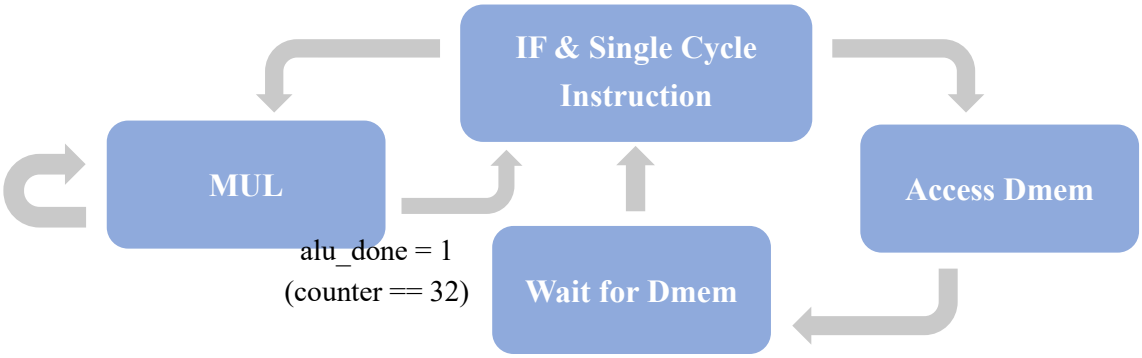
Register Name	Type	Width	Bus	MB	AR	AS	SR	SS	ST
instruc_delay_reg	Flip-flop	32	Y	N	N	N	N	N	N

Register Name	Type	Width	Bus	MB	AR	AS	SR	SS	ST
counter_reg	Flip-flop	7	Y	N	N	N	N	N	N
ans_reg	Flip-flop	64	Y	N	N	N	N	N	N
state_reg	Flip-flop	2	Y	N	Y	N	N	N	N
operand_a_reg	Flip-flop	32	Y	N	Y	N	N	N	N
operand_b_reg	Flip-flop	32	Y	N	Y	N	N	N	N

3. Design Description



CPU FSM



- Instruction fetch and handle single cycle instructions
- Access data memory
- Wait for data memory access finished
- MUL calculations

CPU Submodules

- ImmGen: Generate different immediate values for various instructions.
- Controller: Generate control signals (e.g. ALUSrc, Branch…) and ALUOp according to different instructions.
- ALUControl: Assign ALU control input depending on ALUOp and funct3, 7.
- ALU: Implement arithmetic operations according to ALU control input
- MULDIV_unit: Handle multiplications
- Reg_file

Special Instructions

- Jal
  - ✧ Decode opcode and use ImmGen to generate imm
  - ✧ PC_branch = PC + imm
  - ✧ Write PC + 4 into reg
- Jalr
  - ✧ Decode opcode and use ImmGen to generate imm
  - ✧ Jalr = 1, PC_nxt = rd1 + imm
  - ✧ Write PC + 4 into reg
- Auipc
  - ✧ Decode opcode and use ImmGen to generate imm
  - ✧ Use Auipc (pulled to high) signal to determine MUX value
  - ✧ MUX = 1, ALUresult = PC + imm
  - ✧ MUX = 0, ALUresult = rd1 + imm
  - ✧

Handling Multi-cycle Instructions

Once the CPU receives **mul** instruction, it will jump to multi-cycle state. During the calculations, use a counter to count how many cycles has passed. As soon as the counter reaches 32, pull up alu_done (which means the calculations is done) and the FSM will change to the next state.

4. Work distribution Table

Work \ Name	鄒昀樺	許蘊琰
ImmGen	70%	30%
Control	60%	40%
ALU related	30%	70%
MULDIV	40%	60%
Report	50%	50%