Report: Combinational Logic Circuit

Bilkent University Electrical and Electronics Department

EE102-01 Lab 3

Melih Ege Doğan – 22403329
February 24, 2025

Purpose:

Purpose of this lab was to set up a combinational logic circuit on the breadboard using binary counter, LEDs and logic gates.

Methodology:

This lab work practiced on creating a logic circuit using binary counter and LEDs. First, we turned on our binary counter using square waves which are created by function generator. Then we had to show that binary counter is working using LEDs. After that we used 2 logic gates XOR gate and NOR gate to complete our circuit. Finally, we connected our output to a LED to observe our circuit.

Design Specifications:

Our design has 4 input bits and 1 output bit. We used 2 XOR gates and a NOR gate in our design. Before creating the truth table to be clearer our Variables are assigned as:

A: First bit of the input.

B: Second bit of the input.

C: Third bit of the input.

D: Fourth bit of the input.

X: A XOR B.

Y: C XOR D.

Z: X NOR Y.

Creating the truth table showed us how our circuit should be behave (Table 1).

A B C D	X	Y	Z
0 0 0 0	0	0	1
0 0 0 1	0	1	0
0 0 1 0	0	1	0
0 0 1 1	0	0	1
0 1 0 0	1	0	0
0 1 0 1	1	1	0
0 1 1 0	1	1	0
0 1 1 1	1	0	0
1 0 0 0	1	0	0
1 0 0 1	1	1	0
1 0 1 0	1	1	0
1 0 1 1	1	0	0
1 1 0 0	0	0	1
1 1 0 1	0	1	0
1 1 1 0	0	1	0
1 1 1 1	0	0	1

Table 1: Truth table.

After checking the truth table, we created the circuit as seen in the Figure 1.

$$Z = \overline{(A \oplus B) + (C \oplus D)}$$

Figure 1: Equation of the Circuit.

This simple circuit can be created by using a 4-bit counter (74HC163), 2 XOR gates (74HC86N) and a NOR gate (74HC02N). One of the XOR gates used to create $A \oplus B$ = X, and other one used to create $C \oplus D = Y$. Lastly NOR gate used to create $\overline{X + Y} = Z$.

Results:

The combinational circuit has been designed on the breadboard using 4-bit counter (74HC163) and logic gates. By following the instructions on the datasheet, 4-

bit counter has been set to the count mode. VCC, MR, CET, CEP, PE pins set to 5V and GND pin to 0V. Also, CP pin connected to function generator so we can change the frequency by hand. Q_1, Q_2, Q_3, Q_4 pins were assigned as A, B, C, D. Then XOR and NOR gate have been inserted in the breadboard and connected A, B, C, D to gates (Figure 2).

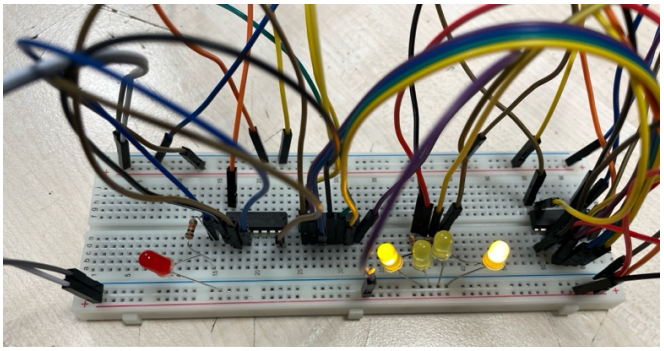

Figure 2: Circuit with 4-bit binary counter, XOR gate and NOR gate.

Output is also observed using an oscilloscope (Figure 3). When we observed the output from the oscilloscope, we noticed that waves on the oscilloscopes are 5V for output 1, 0V for output 0. We also noticed that waveform of the oscilloscope wave is proportional with the truth table.

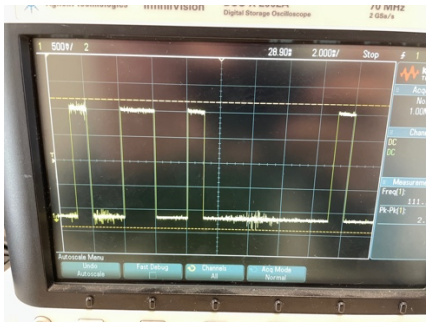

Figure 3: Oscilloscope Waves.

Using 4-bit counter all 4-bit combinations (0000 to 1111) has been tested. Here are some of the inputs and outputs of the circuit (Figures 4.1, 4.2, 4.3, 4.4, 4.5, 4.6).

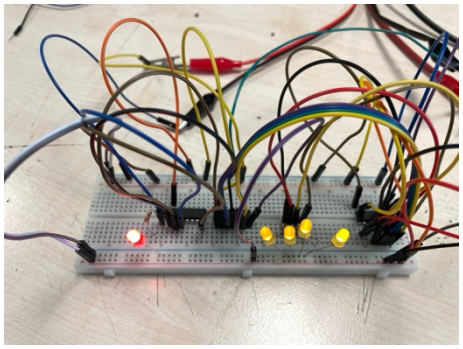

Figure 4.1: ‘1111’ Input.

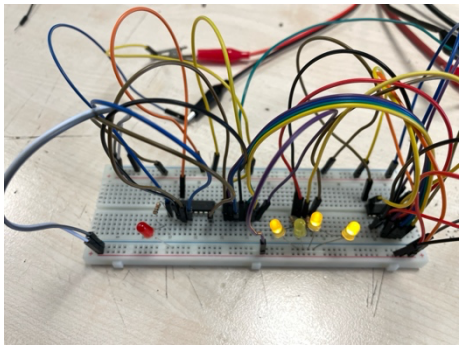

Figure 4.2: ‘1011’ Input.

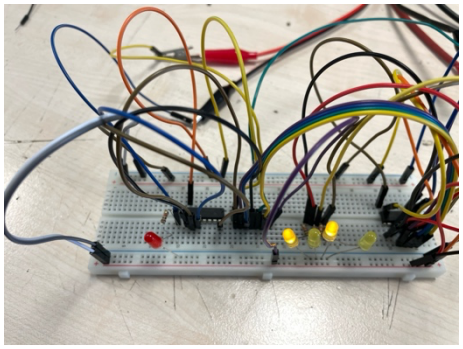

Figure 4.3: ‘1010’ Input.

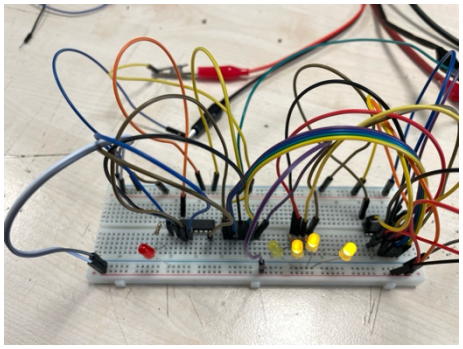

Figure 4.4: ‘0111’ Input.

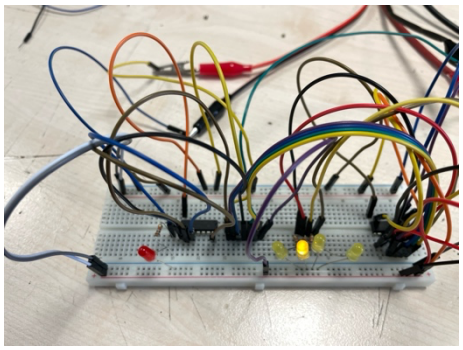

Figure 4.5: ‘0100’ Input.

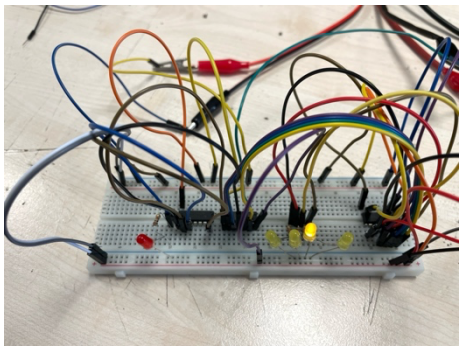

Figure 4.6: ‘0010’ Input.

Conclusion:

This lab successfully demonstrated the design and implementation of a combinational logic circuit using a 4-bit binary counter (74HC163), XOR gates (74HC86N), and a NOR gate (74HC02N) on a breadboard. The circuit, designed to implement the expression $\overline{(A \oplus B) + (C \oplus D)}$, was tested for all input combinations (0000-1111), and its output, observed via an LED and oscilloscope, perfectly matched the predicted behavior of the truth table. The oscilloscope confirmed clear 0V/5V digital signals, validating the circuit's functionality. This

experiment provided practical experience in translating a logical specification into a working digital circuit, reinforcing our understanding of binary counting, logic gate implementation, truth table verification, and datasheet interpretation.

References:

- https://github.com/SemihAkkoc/EEE102
- https://www.ti.com/lit/gpn/sn74hc86
- https://www.ti.com/lit/gpn/sn74hc02